

Electrical Integrity of State-of-the-Art 0.13 μm SOI CMOS Devices and Circuits Transferred for Three-Dimensional (3D) Integrated Circuit (IC) Fabrication

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Abstract

We introduce a new scheme for building three-dimensional (3D) integrated circuits (ICs) based on the layer transfer of completed devices. We demonstrate for the first time that the processes required for stacking active device layers preserve the intrinsic electrical characteristics of state-of-the-art short-channel MOSFETs and ring oscillator circuits, which is critical to the success of high performance 3D ICs.

Introduction

3D integration—in which multiple layers of active devices are stacked with vertical interconnects between the layers—promises to improve circuit performance even in the absence of continued device scaling because the reduced average interconnect length should yield fewer intrinsic delays per cycle, enhanced accessible die area, and reduced noise coupling [1]. The general techniques for building 3D ICs may also facilitate the integration of heterogeneous materials, devices, and signals to enable flexibility in device structure, system design, and routing [2]. Modeling of the power/performance tradeoff shows a significant projected benefit of circuits with multiple device layers (Fig. 1) [3].

While various wafer-level 3D IC fabrication approaches have been proposed [4], no process has yet been shown to be fully compatible with high performance devices and circuits. In this work we demonstrate for the first time that the techniques we developed for transferring fully-processed device layers off their original substrate and on top of another circuit preserve the electrical integrity of state-of-the-art 0.13 μm Cu/low-k SOI CMOS technology. We evaluate the impact of 3D IC fabrication processes on the performance and yield of intrinsic devices, ring oscillator circuits, and interconnects.

Process Integration

We adopt an “assembly” approach to 3D circuit fabrication [5] in which we begin with multiple completed 2D circuits fabricated by conventional means and individually tested, and then stack the device layers using wafer bonding. We believe this approach should improve yield and reduce manufacturing cost compared to “bottom up” techniques in which devices in each layer are processed sequentially.

After conventional processing of SOI devices and back-end metallization, the full wafer is attached to a glass handle wafer using polymeric adhesives [Fig. 2(a)]. The original silicon substrate is then removed by grinding and etching, stopping on the SOI buried oxide (BOX) (Fig. 3). X-ray diffraction data of a thin SOI layer transferred onto glass show well-resolved, symmetric fringes (Fig. 4), indicating a good quality transferred film with no strain. After circuit transfer onto glass, the stack is transparent (Fig. 5), which facilitates aligned bonding to another circuit [Fig. 2(b)]. Finally, the glass is released by laser ablation [6] and the adhesives are stripped, at which point shallow vias can be etched and metallized to interconnect the two circuit layers [Fig. 2(c)]. In principle, the process can be repeated with additional device layers.

Device and Circuit Evaluation

Care must be taken to prevent degradation of devices and circuits due to thermal or mechanical stresses brought on by the layer transfer processes. We performed a systematic study of the electrical integrity of high performance SOI FETs (of various geometries, down to $L=55$ nm) and ring oscillator circuits that were subjected to the processes required for layer transfer. Starting 200 mm wafers were composed of SOI circuits with a Cu/low-k dielectric back-end [7]. Each wafer was put through several stages of the layer transfer process, and electrical tests were performed on 25 chips per wafer after each stage. Measurements of individual 65 nm nFETs show only small percentage variations in on current (I_{on}) and negligible changes in linear threshold voltage ($V_{t,lin}$) after each process, including full layer transfer (Fig. 6). We observe similar results for pFETs.

We look more closely at the median data for a particular wafer at three stages: (A) after standard CMOS fabrication; (B) after additional “simulated” lamination process in which the pressure and temperature required to adhere the processed wafer to glass are applied without actually completing the adhesion; (C) after full attachment to glass, an anneal to simulate the thermal processing required for the second bonding step, and delamination of the glass plus adhesive removal (Figs. 7-11). Linear drain current, $I_{d,lin}$, and $V_{t,lin}$ of long-channel (5 μm) nFETs are not appreciably altered (Fig. 7), indicating that these processes do not influence the channel mobility. The short channel (65 nm) devices show a slight (<10%) degradation in $I_{d,lin}$ and $V_{t,lin}$, which we attribute to an increase in line resistance since small devices are more sensitive to resistance changes (Fig. 8). The I_{on} - I_{off} plot of $L=65$ nm nFET devices measured in different chips shows that the across-wafer distribution is preserved (Fig. 9).

Ring oscillator circuits composed of 55 nm CMOS inverters show a slight increase in stage delay after processing (Fig. 10), consistent with the device results, but circuit yield is still high. Even the wafer that had the full layer transfer process (G) exhibited preserved devices and circuits, including functional 65 nm CMOS ring oscillators with 11.8 ps stage delay.

Via chain test structures were used to evaluate the influence of these processing steps on back-end characteristics. Fig. 11 shows that the isolation yield is high in all cases. We do observe higher apparent resistivity for metal lines that went through the glass release step, which may result from an incomplete adhesive strip. This supports our conclusions that the slight circuit performance degradation observed is not due to the intrinsic device characteristics but instead to the apparent wiring resistance.

Conclusions

We described a layer transfer protocol for the fabrication of 3D ICs and demonstrated that these processes preserve the electrical integrity of state-of-the-art SOI devices and circuits, a vital step toward the realization of high performance 3D ICs.

16.6.1

Acknowledgment

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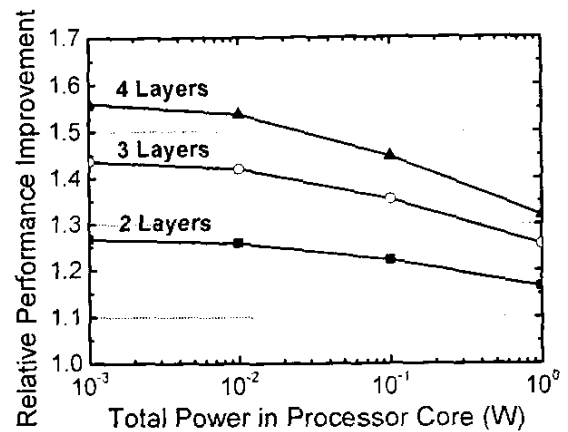


Fig. 1. Technology optimization model shows system level advantage of 3D integration.

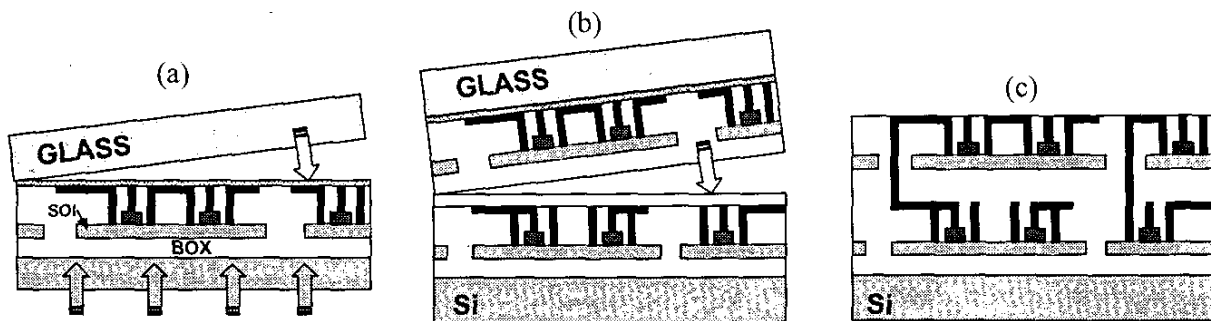


Fig. 2. Schematic diagrams of layer transfer process for 3D IC fabrication. (a) Circuit is attached to glass handle wafer and original substrate is removed. (b) Top circuit is aligned and bonded to second circuit. (c) Handle wafer and adhesives are removed, and vertical interconnects are formed between device layers.

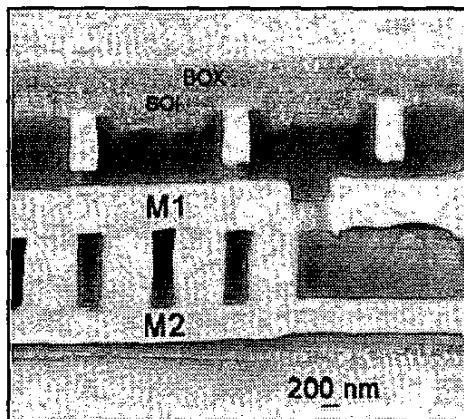


Fig. 3. Cross sectional SEM micrograph after circuit transfer onto glass and silicon substrate removal down to the BOX.

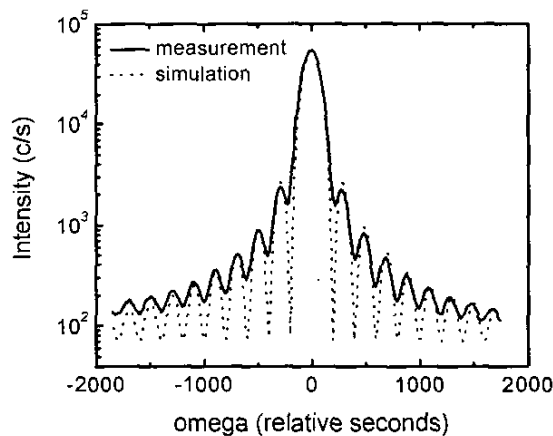


Fig. 4. X-ray diffraction data of a 160 nm SOI film transferred onto glass.

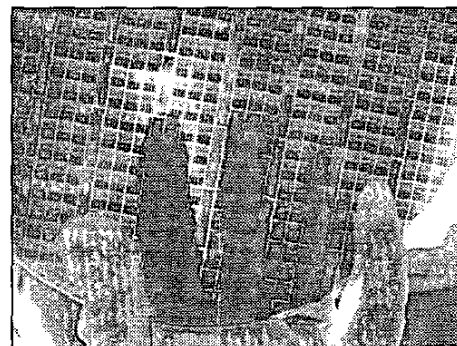


Fig. 5. Photograph of a 200 mm-diameter transparent stack showing a fully-processed circuit transferred onto glass.

	Process
A	none
B	simulated lamination
D	adhesive applied and stripped
E	laminated to glass, then glass released and adhesive stripped
C	laminated to glass, annealed (short), then glass released and adhesive stripped
F	laminated to glass, annealed (long), then glass released and adhesive stripped
G	laminated to glass, silicon substrate thinned by grinding, relaminated to silicon, then glass released and adhesive stripped

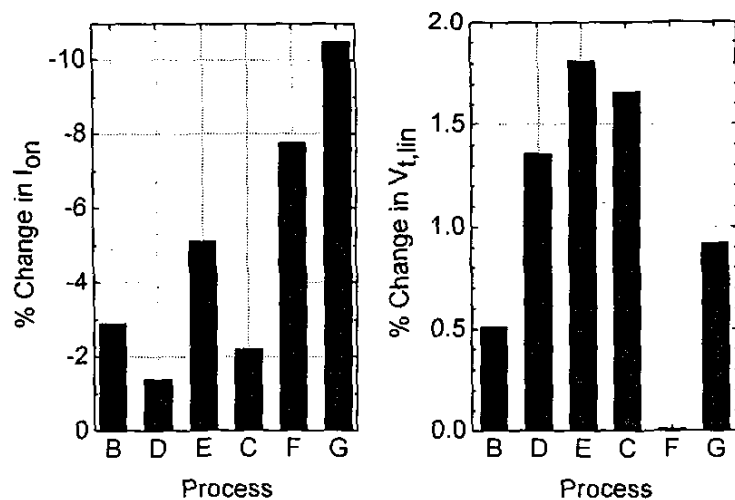


Fig. 6. Percentage change in I_{on} and $V_{t,lin}$ for an individual 65 nm n FET resulting from each process, as listed in the table (separate wafers).

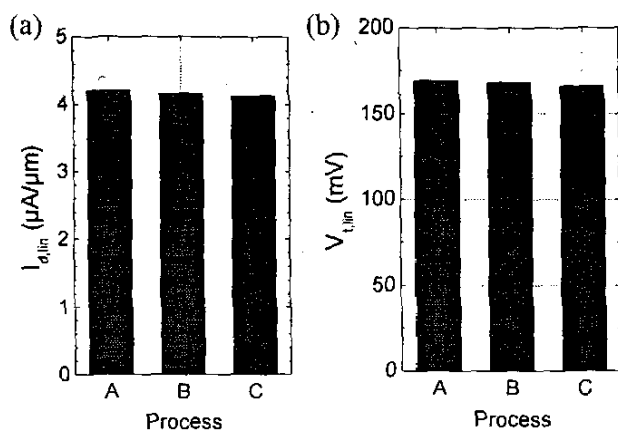


Fig. 7. Median wafer values for 5 μm n FETs after different stages (A,B,C) of layer transfer: (a) $I_{d,lin}$ and (b) $V_{t,lin}$.

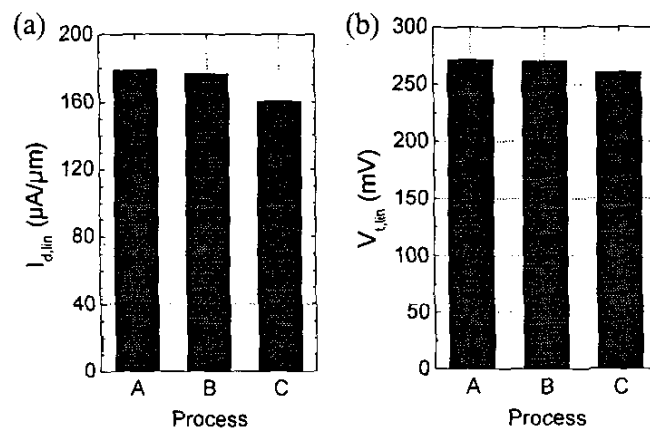


Fig. 8. Median wafer values for 65 nm n FETs after different stages (A,B,C) of layer transfer: (a) $I_{d,lin}$ and (b) $V_{t,lin}$.

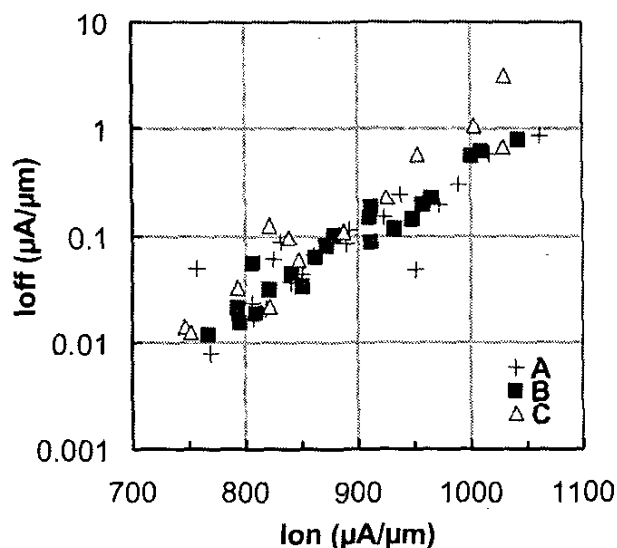


Fig. 9. I_{off} - I_{on} distribution for 65 nm n FETs after different stages (A,B,C) of layer transfer.

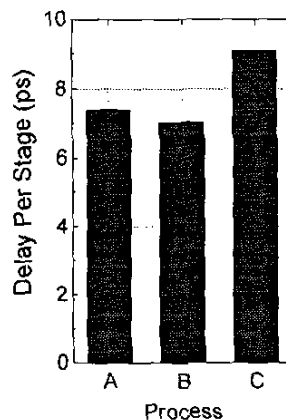


Fig. 10. Stage delay for 55 nm CMOS ring oscillators after different stages (A,B,C) of layer transfer.

Process	Normalized Chain-to-Chain Isolation Yield
A	100.0 %
B	84.2 %
C	87.8 %

Fig. 11. Via chain to via chain isolation yield after different stages of processing (normalized to process A).