

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner,

v.

BESANG INC.,

Patent Owner.

IPR2023-00991

Patent No. 7,378,702

PETITIONER'S REPLY

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EXHIBIT LIST

Exhibit No.	DESCRIPTION
1001	U.S. Patent 7,378,702 (“702Pat.”)
1002	File History of U.S. Patent 7,378,702 (“702FH”)
1003	Declaration of Dr. Carl Sechen (“Sechen”)
1004	Curriculum Vitae of Dr. Carl Sechen
1005	U.S. Patent 7,052,941 (“941Pat.”)
1006	File History of U.S. Patent 7,052,941 (“941FH”)
1007	U.S. Patent Appl. Publ. No. 2002/0028541 (“Lee”)
1008	U.S. Patent Appl. Publ. No. 2003/0157748 (“Kim”)
1009	Aspar, The Generic Nature of the Smart-Cut® Process for Thin Film Transfer, 30 J. Elec. Materials 834 (2001) (“Aspar”)
1010	U.S. Patent No. 6,034,882 (“Johnson”)
1011	U.S. Patent No. 5,571,730 (“Park”)
1012	U.S. Patent App. Publ. No. 2002/0154556 (“Endoh”)
1013	Complaint in <i>BeSang Inc. v. Intel Corporation</i> , 3:23-cv-00113-MAH (D. Or. January 23, 2023)
1014	Silicon Processing, Vol. 1 by Stanley Wolf (2000)
1015	Silicon Processing, Vol. 4 by Stanley Wolf (2002)
1016	U.S. Patent No. 6,355,501 (“Fung”)
1017	U.S. Patent No. 5,414,288 (“Fitch”)
1018	U.S. Patent No. 6,027,975 (“Hergenrother”)
1019	U.S. Patent No. 6,337,247 (“Schulz”)
1020	U.S. Patent No. 6,449,186 (“Noble”)
1021	U.S. Patent No. 6,943,067 (“Greenlaw”)
1022	IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition (2000)
1023	U.S. Patent No. 5,882,987 (“Srikrishnan”)
1024	Maleville et al., Multiple SOI layers by multiple Smart-Cut® transfers, 2000 IEEE International SOI Conference (Oct. 2000) (“Maleville”)
1025	U.S. Patent No. 5,615,148 (“Yamamura”)
1026	U.S. Patent No. 5,544,103 (“Lambertson”)
1027	U.S. Patent No. 6,381,173 (“Zatelli”)
1028	Declaration of J. Munford
1029	Minutes from Rule 16 Conference in <i>BeSang Inc. v. Intel Corporation</i> , 3:23-cv-00113-MAH

1030	March, 2023 Average Time to Trial Statistics for the District of Oregon
1031	Excerpts of Endoh (EX1012)
1032	Complaint, <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028
1033	Intel <i>Sotera</i> Stipulation Letter
1034	Notice of <i>Sotera</i> Stipulation in <i>BeSang Inc. v. Intel Corporation</i> , 3:23-cv-00113-MAH (D. Or.)
1035	Email Court Correspondence Confirming Stay of <i>Besang Inc. v. Intel Corp.</i> , Case No. 3:23-cv-00113
1036	Updated Docket, <i>BeSang, Inc. v. Micron Tech, Inc.</i> , Cas No. 2:23-cv-00028
1037	Reply Declaration of Dr. Carl Sechen
1038	Docket, <i>Besang Inc. v. Intel Corp.</i> , Case No. 3:23-cv-00113 (D. Or.)
1039	Updated Docket, <i>BeSang, Inc. v. Micron Tech, Inc.</i> , Case No. 2:23- cv-00028 (E.D. Tex.)
1040	Aspar et al., <i>Smart-Cut® process using metallic bonding: Application to transfer of Si, GaAs, InP thin films</i> , Electronics Letters, Vol. 35, No. 12 (June 10, 1999) (“Aspar II”)
1041	U. Gosële & Q. Y. Tong, <i>Semiconductor Wafer Bonding</i> , Annual Review of Materials Science, Vol. 28 (1998) (“Gosële”)
1042	Qin-Yi Tong & U. Gosële, <i>Wafer Bonding and Layer Splitting for Microsystems</i> , Advanced Materials, Vol. 11, No. 17 (1999) (“Tong”)
1043	Yongchai Kwon, <i>Wafer Bonding for Three Dimensional (3D) Integration</i> , Graduate Thesis, Rensselaer Polytechnic Institute (Aug. 2003) (“Kwon”)
1044	Y. Kwon et al., <i>Wafer bonding using low-k dielectrics as bonding glue in three-dimensional integration</i> , SEMICONDUCTOR WAFER BONDING: SCIENCE, TECHNOLOGY, AND APPLICATIONS VI, Proceedings of the International Symposium, Volume 2001, The Electrochemical Society (2002) (“Kwon II”)
1045	U.S. Patent No. 6,054,370 (“Doyle”)
1046	Krishna Parat & Chuck Dennison, <i>A Floating Gate Based 3D NAND Technology With CMOS Under Array</i> , 2015 IEEE International Electron Devices Meeting (IEDM), pp. 3.3.1-3.3.4 (2015) (“Parat”)

1047	Gower-Hall & Duane S. Boning, <i>Model-based uniformity control for epitaxial silicon deposition</i> , IEEE Transactions on Semiconductor Manufacturing, Vol. 15, No. 3, pp. 295-309 (Aug. 2002) (“Gower-Hall”)
1048	R.A. Street (Ed.), <i>Technology and applications of amorphous silicon</i> , Vol. 37, Springer Science & Business Media (1999) (“Street”)
1049	U.S. Patent No. 6,544,837 (“Divakauni”)
1050	Frank Niklaus, <i>Low-temperature wafer-level transfer bonding</i> , Journal of Microelectromechanical Systems, Vol. 10, No. 4, pp. 525-531 (Dec. 2001) (“Niklaus”)
1051	Alan B. Grebene, <i>Bipolar and MOS analog integrated circuit design</i> , John Wiley & Sons, 2003 (“Grebene”)
1052	U.S. Patent No. 5,978,258 (“Manning”)
1053	U.S. Patent No. 5,714,393 (“Wild”)
1054	U.S. Patent No. 6,621,722 (“Yu”)
1055	K. W. Guarini, et al., <i>Electrical integrity of state-of-the-art 0.13 μm SOI CMOS devices and circuits transferred for three-dimensional (3D) integrated circuit (IC) fabrication</i> , International Electron Devices Meeting, pp. 943-945, IEEE (2002) (“Guarini”).
1056	Deposition transcript of Steven Przybylski, dated May 24, 2024
1057	U.S. Patent No. 5,661,408 (“Kamieniecki”)

I. INTRODUCTION

PO's Response attempts to misdirect the Board, but when the Grounds are evaluated in light of the objective evidence, Intel has established the '702 Challenged Claims are unpatentable by a preponderance of the evidence.

II. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. "Stackable add-on layer [is]/[being] bonded" requires bonding separate structures

1. The difference between the Board's and Intel's constructions need not be resolved

Intel proposed construing "stackable add-on layer [is]/[being] bonded" to require wafer bonding of the "stackable add-on layer"—which must be its own structure and capable of being stacked—to the recited layer of the substrate. Pet., 10-13. The Board agreed as to "stackable add-on layer," construing it to be "formed separately from the substrate and then bonded to the substrate or a dielectric layer above the substrate," but not encompassing "memory cells that are formed by sequential deposition on or above a substrate or dielectric layer without being added to a separately formed substrate." DI, 9. The Board, however, declined to limit bonding to wafer bonding. *Id.*, 10-11 & n.10. Although Intel stands by its construction, the Board need not resolve the difference between its construction and Intel's because the Challenged Claims are unpatentable under either. EX1037, ¶7.

2. PO's approach has no legal basis

PO appears to argue the Board should not construe “stackable add-on layer [is]/[being] bonded” (POR, 15) and should not consider grounds based on PO's apparent construction from its district court infringement allegations (EX1013, ¶¶65; EX1032, ¶¶76) because Intel proposed a different construction. POR, 1, 31-32, 35-36, 52-56, 75-76. Intel is not aware of any authority supporting PO's request for the Board to (i) decline to construe the limitation *and* (ii) forego analyzing instituted grounds under all possible constructions. The Board can narrow its focus to certain grounds, but only if those grounds are tied to a construction issued by the Board, as described in *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-00967, Paper 43, 15-18, 24-62 (Nov. 19, 2021), affirmed in *Masimo Corp. v. Sotera Wireless Inc.*, 2022-1393, 2023 WL 6990542, *4-5 (Fed. Cir. 2023).

Here, PO cannot duck this limitation's construction and simultaneously avoid the Board addressing grounds under the construction implicated by PO's litigation allegations. PO says it “disagrees with the Board's preliminary construction” but fails to provide an alternative. POR, 15. Accordingly, the Board should construe the term, and can then focus on the grounds applying that construction. But if the Board decides not to construe the limitation, it should revisit all grounds based on all proposed constructions. *AC Techs. S.A. v. Amazon.com, Inc.*, 912 F.3d 1358, 1360 (Fed. Cir. 2019).

B. Intel's construction of "SOI pillar" is correct

PO contends "SOI pillar" does not require construction but provides one anyway: "a silicon-on-insulator structure taller than it is wide." POR, 16. For several reasons, the Board should adopt Intel's construction. DI, 12. PO's proposal (which encompasses any "silicon structures" "on or above an insulating layer" (POR, 16; EX2029, ¶90; EX1056, 35:17-36:6)) does not address the '702 patent's description of "SOI," relating to the composition of a pillar (containing crystalline silicon) and its creation; Intel's construction encompasses that description ("formed in a stackable add-on layer added using SOI technology"). Pet., 13-16 (citing incorporated '941Pat, 6:44-46); EX1037, ¶8.

Further, the '702 patent does not limit "pillar" to any particular shape. Indeed, PO's cited dictionaries recognize it could be "any upright, supporting part" or "post." EX2031; EX2032. PO mistakenly argues the '702 patent's disclosure of "doped stack structures (i.e., pillar structures)" does not define a "pillar" (POR, 18), but no other structures are described as such ('702Pat, 6:26-29, Figs. 4, 6, 8, 12, 20, 27). EX1037, ¶¶9-10.

Nevertheless, the cited references teach an "SOI pillar" under PO's construction. EX1037, ¶11.

C. Intel clearly described which constructions it was applying

Intel provides a table below showing which construction the Petition addressed in each ground.

Ground	Claim(s)	Reference(s)	“stackable add-on layer” (all Challenged Claims)	“SOI pillar” (claims 14-17)	Source
1A	13-17	Lee	PO	PO ¹	Pet., 16
1B	16-17	Lee, Endoh	PO	PO	Pet., 41-42
1C	13-17	Lee, Kim	Intel ²	PO	Pet., 50
1D	16-17	Lee, Kim, Endoh	Intel	PO	Pet., 55
1E	13-17	Lee, Aspar	Intel	Intel	Pet., 55
1F	16-17	Lee, Aspar, Endoh	Intel	Intel	Pet., 64
2A	13	Johnson	PO	N/A	Pet., 65
2B		Johnson, Kim	Intel	N/A	Pet., 74
2C		Johnson, Aspar	Intel	N/A	Pet., 77
3	1	Park, Kim	Intel, PO	N/A	Pet., 82

¹ Grounds 1A-1F apply also to PO’s POR proposed construction of “SOI pillar.”

² Grounds 1C-1F, 2B-2C apply also to PO’s apparent construction described in the Petition.

D. Lee-based Grounds 1A-1F render the Challenged Claims unpatentable

1. Claim 13 is unpatentable

Under the Board’s preliminary (or Intel’s) construction of “stackable add-on layer [is/being] bonded” (DI, 9, 11), claim 13 is unpatentable based on the combination of Lee with Kim or Aspar (Grounds 1C, 1E). The Petition describes a layer (Lee’s layer 3104 (Lee-Kim combination) or doped stack/conductive layer (Lee-Aspar combination)) formed separately from the substrate (Lee’s substrate 3105) and then bonded to a dielectric layer (Lee’s layer 3102) above the substrate, as required by the Board’s construction. DI, 9, 11; Pet., 51-53, 58-60, 62-63. For Grounds 1C, 1E (claim 13), PO contests only motivation to combine and reasonable expectation of success. POR, 20-31, 44-52; EX1037, ¶12. PO does not contest Lee teaches all claim 13 limitations under PO’s apparent construction of “stackable add-on layer [is/being] bonded” (Ground 1A). POR, 55-57.

a) Kim’s and Aspar’s techniques would have been obvious to combine with Lee (Grounds 1C, 1E)

PO asserts just because Kim’s and Aspar’s techniques were known does not mean they would have been obvious. POR, 26-27. But Intel also explained why the teachings would have (i) improved Lee and (ii) helped address the problem of fabricating 3D devices described in Lee, Kim, and Aspar. Pet., 53-54, 60-62.

Regarding the latter, demonstrating obviousness requires showing: “there’s a [1] known technique [2] to address a known problem [3] using ‘prior art elements

according to their established functions.” *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023). The Petition explains how this test is met (Pet., 53, 60-61), but PO did not address it. Further, PO does not address that Aspar itself provides motivation to combine with Lee: “multiple SOI layers stacks can be easily performed thanks to Smart-Cut technology” and Smart-Cut “transfer[s] thin layers of very good thickness homogeneity and with a high crystalline quality.” Pet. 60-61; EX1009, 834, 839; EX1037, ¶13. Instead, PO contends the combinations would not have improved Lee. POR, 26. Improvement in a categorical sense is not required: the Petition need only show Kim’s/Aspar’s techniques are “suitable option[s].” *PACT*, 61 F.4th at 1381.

b) Lee suggests using stacking techniques (Grounds 1C, 1E)

Contrary to PO’s position and the DI (POR, 21, 25-26; DI, 35), Lee does not mandate using deposition to add layers in Figure 35 and never says the bottom level of memory device levels 3104 is deposited onto insulating layer 3102 (EX1007, ¶111; Pet., 51-52). Although Lee uses “monolithic” to refer to depositing one array layer on another, the term does not address how the bottom array layer is attached to underlying structures. EX1007, ¶¶107, 294. Monolithic structures can be bonded together. EX2039, 62:2-18, 63:16-64:3; EX1037, ¶14.

Lee’s Figure 35 description lacks details POSITAs would have sought elsewhere, including in Lee’s other embodiments, Kim, and Aspar. Pet., 21-29, 50-

63. To argue Figure 35's first array level is deposited,³ PO relies on Lee's Figures 13-28 pillar embodiments, as well as Dr. Sechen's testimony. POR, 21-22. But those embodiments suggest just one potential Figure 35 implementation. EX1037, ¶15.

Lee discloses stacking by teaching packaging multiple two-dimensional arrays "together." Pet., 51-52, 56; EX1007, ¶¶107, 259, 294; EX1003, ¶¶192, 204; EX2039, 61:12-22. Lee further discloses Figure 35's array can have self-aligned configurations and contemplates using the techniques at ¶¶203-281 with SOI technology, including "wafer bonding." EX1007, ¶¶113, 115, 117, 208 (disclosing driver circuits like Figure 35 (EX1007, ¶¶110-111)), 211-212; Pet., 18-19, 21-22, 27-29, 50, 56, 62. Although these embodiments suggest Figure 35 implementations, they show the Figure 35 embodiment was not limited to deposition, or the Figures 13-28 embodiments or ¶122. EX1007, ¶¶110-111. Based on Figure 35's lack of detail, POSITAs would have investigated other useful stacking techniques, such as Kim and Aspar. Pet. 51-52, 56; EX1037, ¶16.

Lee's disclosures also do not support PO's assertion that stacking is incompatible with Lee. POR, 26. Lee's general statement about "increased density

³ The Board pointed to Lee's paragraph 122 as support (DI, 35), but that paragraph does not refer to deposition or Figure 35 (EX1007, ¶122).

and a lower cost” applies to all “monolithic” memory arrays, regardless of whether the bottom layer is deposited or bonded to an underlying structure. EX1007, ¶¶106-107, 110-117. Indeed, Lee teaches potential implementations involving SOI technology and wafer bonding “increase[] array density and decrease[] die size and cost.” EX1007, ¶¶204, 207-212; *see id.*, ¶110-112; EX1037, ¶17.

c) POSITAs would have combined the art for quality control (Grounds 1C, 1E)

PO argues “quality control” and “reduce[d] waste” would not have motivated combining Lee with Kim or Aspar. POR, 26-30, 49-50. The evidence supports otherwise. Fung teaches testing structures before bonding allows screening for defects. EX1016, 1:48-52. Testing allowed a chipmaker to identify potentially low-yield wafers and dispose of them before bonding, preventing wasting substrate materials after bonding. Pet., 53-54, 61-62; EX1003 ¶¶196, 213; EX2039, 112:6-113:11. Testing before bonding would have assured higher yield while conserving time, material, and cost compared to “bottom up” techniques like deposition. EX1055, 943; EX1037, ¶18.

PO’s criticisms lack merit. PO suggests Intel must provide data comparing yields for bonded and non-bonded devices. POR, 28. As the Board recognized, that is not necessary, though it inquired whether the quality control benefit “outweighed the...improved density and lowered costs of” making devices using only deposition. DI, 35-36. As described above, Lee’s own use of stacking still leads to increased

density and lower cost, and Kim teaches stacking with “low cost and high via density,” EX1008, ¶1. EX1037, ¶17. Intel’s combinations would result in the same memory structures with the same density as Lee, and a quality control benefit is sufficient motivation to support Intel’s combinations.

PO argues Fung identifies yield and alignment problems with wafer bonding. POR, 28-29. But testing would have increased yield by screening out defective structures. EX1016, 1:48-50; EX1055, 943. Fung describes the known technique of using “marks” to secure alignment, just like the ’702 patent. EX1016, 1:58-60, 5:28-31; ’702Pat, 6:13-18. Regardless, Aspar’s process transferred an unpatterned layer or layer stack and did not require wafer alignment, as the ’702 patent recognized (’702Pat, 6:18-25). EX1049, 5:26-28; EX1037, ¶19.

PO incorrectly asserts Kim’s bonding processes would have created more waste rather than less. POR, 29-30, 49-50. First, although PO makes much about whether dies or wafers would have been discarded, it admits there are errors. POR, 29. Errors resulting in low-yield wafers would have wasted substrate circuitry. EX1037, ¶20. Second, PO argues Kim generated waste by thinning the wafer, but thinning was optional. POR, 29; EX1008, ¶25.

PO incorrectly asserts there would be nothing to test in Lee-Aspar. POR, 49. In Aspar’s process, the bonded structures are single layers or layer stacks. EX1009, 838-839. POSITAs would have tested the layers by checking, for example, doping

concentration, thickness, and uniformity. EX1003, ¶213; EX1057, 1:14-18, 2:7-23; EX1047, 295; EX1041, 228; EX1043, 10-11; EX1037, ¶21.

d) Process optimization is a motivation to combine (Grounds 1C, 1E)

Dr. Sechen explained optimizing processes for separately-fabricated devices and memory structures that are eventually bonded would have been preferable because in a linear process “a later processing step can cause perturbations of previous processing steps.” EX2039, 91:17-98:9 (citing EX1003, ¶213); *see* EX1003, ¶196 (same for Lee-Kim). Issues included “heat...caus[ing] metal to deform possibly creating opens or shorts.” EX2039, 96:15-97:11.

Objective evidence supports Dr. Sechen’s testimony. In a deposition-only approach the “processes involved in forming successive devices can affect the characteristics of devices placed underneath.” EX1016, 1:25-27. Fabricating devices on separate substrates, each according to an optimized process, and then bonding them (as Kim/Aspar teach) avoids this issue and “offers the potential of...increasing the yield.” *See* EX1008, ¶22; EX1044, 145-146; EX1049, 6:42-56; EX1050, 525; EX1037, ¶¶22-23.

Accordingly, POSITAs would have recognized the combination’s optimized process benefits, including Aspar’s process would have benefited Lee by adding monocrystalline silicon, which improves performance. EX1037, ¶24.

e) Lee’s teachings do not undermine Intel’s motivations to combine (Grounds 1C, 1E)

PO incorrectly argues Intel has not shown a motivation to “fabricate Lee’s interleaved levels” allegedly shown in Figure 25A using Kim or Aspar. POR, 20-26, 30-31, 43-44, 50. Initially, although the POR extensively uses the term “interleave,” that term never appears in Lee. EX1037, ¶26.

Additionally, PO’s contention relates only to Lee’s Figure 25A showing two vertically-connected memory cells. PO mentions Lee’s memory in Figures 1A, 1B, 2, and 7 once (POR, 22), but does not argue “interleaved levels” affect those embodiments or Intel’s combinations for claims 13-15 based on them. Pet., 16-17, 17 n.9, 20-31, 50-54, 55-63. PO declares, without elaboration, those embodiments “are not what Lee discloses as a layer” in Figure 35. POR, 22. The Petition explains otherwise. Pet. 21-29; EX1037, ¶27.

Further, PO’s arguments fail for Lee’s Figure 25A embodiment. PO contends Intel offers no explanation for how Lee’s “interleaved” levels “could be recreated by stacking.” POR, 24-25. But the Challenged Claims do not require “interleaving” so that feature is not part of any Figure 25A-based combination. *Axonics, Inc. v Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023). Regardless, POSITAs would have easily created Figure 25A’s structure. In Lee-Kim, Figure 25A’s memory cells would have been fabricated as taught in Lee and then stacked on Lee’s insulating layer 3102 as shown in Figure 35. Pet., 52-53. In Lee-Aspar, a doped layer stack

would have been added by wafer bonding and processed using Lee's techniques to create Figure 25A's first level and then built upon using Lee's techniques to create the second level. Pet., 58-60, 62-63. Although claims 16-17 do not require an operational device, POSITAs desiring one based on either combination would have used Lee's additional processing techniques, including to form more even memory levels. EX1007, ¶169. Lee's multi-level approach is compatible with Intel's combinations. EX1037, ¶28.

f) PO misdescribes Aspar and Smart-Cut (Ground 1E)

PO argues POSITAs would not have combined Lee with Aspar with a reasonable expectation of success. POR, 50-52. PO's arguments are based on faulty descriptions of Aspar. First, PO states that "Aspar is plainly a non-starter because it instructs annealing the wafers at 1100°C." POR, 44; *see id.*, 69, 72, 74. Aspar describes no such annealing step. EX1037, ¶29. PO gets the idea from the Wolf textbooks, which are not part of Intel's combination, and suggests *any* Smart-Cut process, including Aspar's, required an 1100°C post-splitting anneal step. POR, 10-11, 45-46.⁴ The '702 patent disproves this conclusory assertion through its

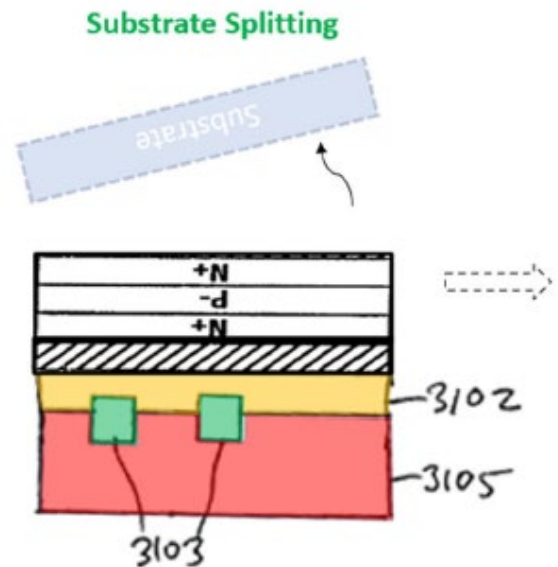
⁴ PO argues Dr. Sechen acknowledged "Smart-Cut taught" an anneal at 1100°C (POR, 46), but he simply acknowledged the Smart-Cut version in a Wolf textbook. EX2039, 120:18-121:18.

incorporated '941 parent ('702Pat, 1:7-10), which PO's expert apparently did not consider (EX2029, ¶12; EX1056, 29:23-30:16). Like Aspar, the '941 patent discloses a Smart-Cut process without any post-splitting anneal. '941Pat, 9:40-47, 10:19-21; Pet., 4-8; EX1009, 835. The '941 patent explains the substrate will not withstand temperatures over 650°C. '941Pat, 8:60-62. PO cannot reasonably argue an 1100°C post-wafer splitting anneal step is required when its own patent, incorporated by reference into the '702 patent, shows the opposite. EX1037, ¶30. Indeed, Aspar itself notes Smart-Cut is a “generic process” that “allows a great deal of combinations (material and bonding layer).” Pet. 58 (citing EX1009, 839). POSITAs would have recognized that would not be compatible with a one-size-fits-all post-splitting anneal temperature as PO argues. EX1037, ¶31.

g) POSITAs would have had reasonable expectation of success

Intel explained, based on Kim and Aspar, POSITAs would have expected success in the combinations. Pet., 54, 62; EX1037, ¶32. PO argues the contrary, mostly repeating criticisms of Intel's motivations to combine based on Lee's “interleaved levels” and an alleged high-temperature anneal not in Aspar. POR, 30-31, 50-51. Intel debunked these arguments above.

PO also argues Intel did not account for a thin silicon layer Aspar's process leaves behind that PO alleges would have obstructed access to Lee's upper electrical contact. POR, 50-51. PO misunderstands Aspar and Petitioner's combination. As shown in the figure below, POSITAs would have followed Aspar's teachings for the splitting step and left behind a thin layer including an N+/P-/N+ doped stack on top of insulating layer (yellow) and substrate (red). Pet., 57-60; EX1009, 834; EX1003, ¶¶209-210. That doped stack would have been used to fashion Lee's memory cells. Pet., 60; EX1007, ¶141; EX1037, ¶33.



When forming the memory cells, Lee teaches adding an upper electrical contact or forming a second set of memory cells with contacts over the underlying memory cells. EX1007, ¶¶122, 126, 141, 157, Fig. 9B; Pet., 17 n.9, 59-60; *see* EX1007, ¶141, Figs. 1A (I/O conductor 116), 2 (conductive input/output 210), 7 (same), 9B (I/O 906), 25A (M2). The added thin layer (i.e., transferred doped stack) serves as part of the memory cell and contacts the electrical contact. EX1037, ¶34.

2. Lee alone or in combination renders claims 14-17 unpatentable

Claims 14-17 are unpatentable regardless of whether the Board adopts Intel's or PO's "SOI pillar" construction. Lee-Aspar teaches an "SOI pillar" under Intel's

construction (which the Board preliminarily adopted (DI, 12)) because Lee taught the claimed memory structures, Pet., 63 (citing Pet. 31-41), Aspar’s Smart-Cut process is “SOI technology” (*id.* (citing Pet. 56-63; EX1009, 834, 837, 839), and the combination includes pillars formed using that SOI technology (*id.* (citing Pet. 56-63; Sechen, ¶217)). In other words, Lee’s Figure 2 (claim 14); Figures 1A, 1B, or 7 (claim 15); and Figure 25A (claims 16-17) teach “a pillar-shaped doped stacked structure,” and those structures would be “formed in a stackable add-on layer added using SOI technology.” Pet., 31-41, 55-63; EX1037, ¶35.

If the Board adopts PO’s “SOI pillar” construction, Lee alone, Lee-Kim, and Lee-Aspar each render claims 14-17 unpatentable. *Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1374, 1384 (Fed. Cir. 2023). The memory cells in Figures 1A, 1B, 2, 7, and 25A (i) involve silicon on or above an insulator (silicon pillars are formed in Figure 35’s bottom level 3104 and have insulating layer 3102 below them (Pet., 33, 36, 39-40; EX1056, 84:9-17)) and (ii) are depicted as taller than they are wide (Pet. 31-41; EX1056, 65:25-66:8, 69:12-14, 71:13-25, 73:1-9; EX1037, ¶36). *E.g.*, *Kingsford Prods. Co v. Creative Spark, LLC*, IPR2016-01831, Paper 32, 32-33 (Mar. 9, 2018) (“Figures that are not drawn to scale may be relied upon to disclose qualitative relationships between measured quantities.”).

Lee refers to the memory devices as “pillars” (EX1007, ¶¶38-39, 41, 46, 52, 118, 122, 125-126, 138, 165, Figs. 1A, 1B, 2, 7, 25A; Pet. 21-22), and PO’s expert

described Lee's Figure 1A structure as "meet[ing] the plain and ordinary meaning of the pillar as drawn" (EX1056, 65:25-66:8). PO does not contest the prior art teaches claims 14 and 15's additional limitations under its construction. EX1037, ¶36.

3. Claims 16-17 are rendered obvious

a) Lee discloses serially-connected memory cells

PO argues Lee discloses only memory cells connected *in parallel*. POR, 33-35, 53, 56. But Lee discloses serially-connected memory cells/pillars. Pet., 37-41; EX1037, ¶37. Lee's Figure 25A below illustrates a step in the process of "integrating [Lee's] pillar memory device...into a multilevel array." EX1007, ¶¶147-69. "The process...can be repeated again to complete the fabrication of memory devices" on several levels. *Id.*, ¶¶167-69; Pet., 38 n.12.

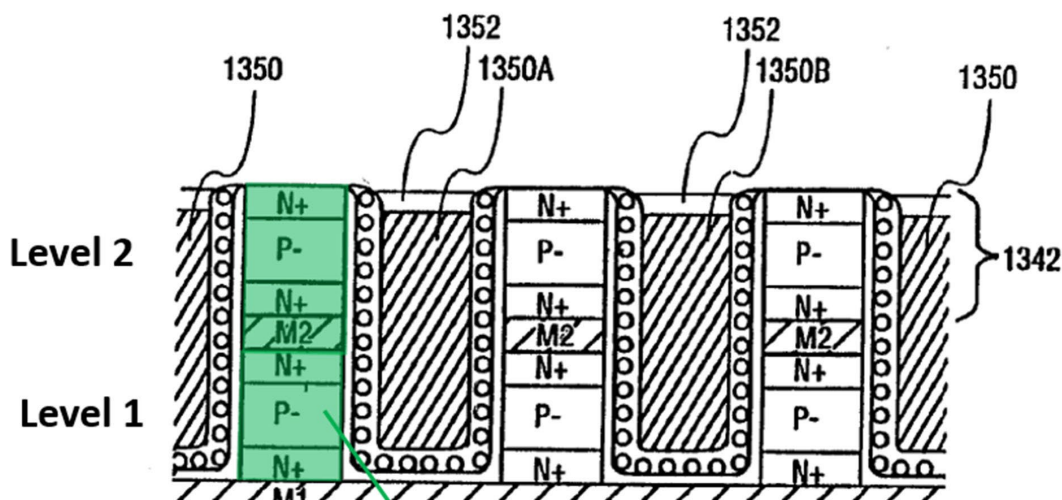


Figure 25A's vertical memory cells lack a conductor at the top of Level 2's memory cells. Without that upper conductor, Level 2's cells cannot be connected *in*

parallel with Level 1's cells because they have only one electrical connection to the cells in Level 1 through metal layer M2. EX1037, ¶38. Therefore, the memory cells are *serially connected*, one after another, as required by claim 16-17. Pet., 38-40; EX1037, ¶38.

That Figure 25A shows an intermediate step is immaterial because “[c]ommercial finality is not claimed” in the '702 patent. *E.g.*, *Abbott Labs. v. Baxter Pharm. Prods., Inc.*, 471 F.3d 1363, 1369 (Fed. Cir. 2006). Claims 16 and 17 do not preclude later configuring two memory cells in series or parallel; those cells need only be “serially connected” at some point. As a result, Lee discloses the claimed “vertically oriented and serially connected” memory pillars (claim 16) that are, in turn, connected serially to other pillars (claim 17). Pet., 37-41; EX1037, ¶38.

Dr. Sechen merely acknowledged that a NOR configuration “would be an implication” based on a possible connection of Figure 25A's M2. POR, 33-34 (citing EX2039, 58:10-60:7). That assumes a completed device with an upper electrical contact and supporting circuitry. EX1037, ¶39.

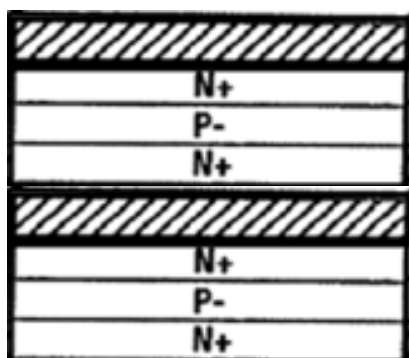
b) POSITAs would have combined Endoh with Lee, alone or together with Kim or Aspar

POSITAs would have applied Endoh's teaching of two serially-connected memory cells in a pillar to Lee, including in combination with Kim or Aspar. Pet., 47-48, 55, 64. Either combination would have resulted in, for example, implementing in Lee's layer 3104: (i) two of Lee's Figure 1B memory cells in a

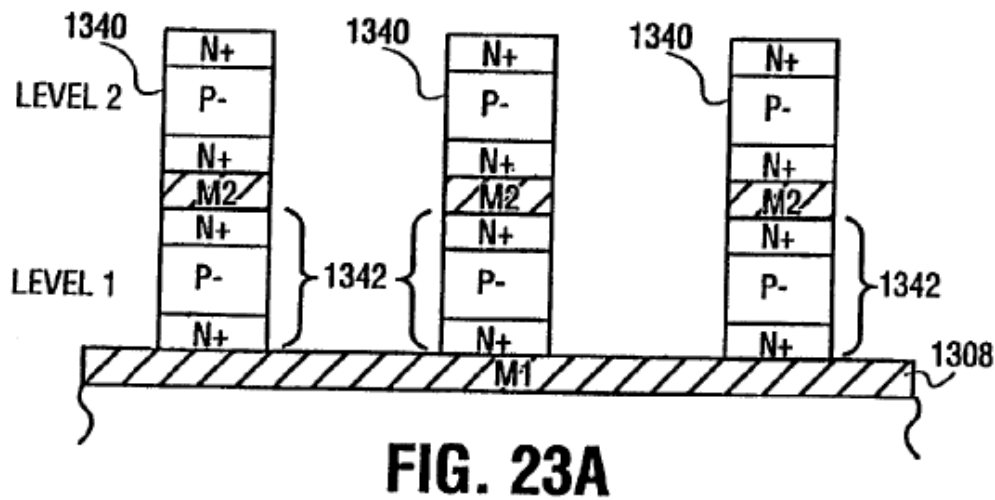
pillar or (ii) Endoh's two-cell pillar. Pet., 47-48, 55, 64; EX1037, ¶40. POSITAs would have found it obvious to use Kim's or Aspar's wafer bonding process for either option. Pet. 55, 64.

For Lee-Kim-Endoh, when implementing two of Lee's Figure 1B memory cells, Kim's process would have been used to transfer pillars with two of those already-formed memory cells to substrate 3105. Pet. 47-48 ("modify...level 3104...to incorporate two memory cells on each pillar"), 52-53 ("wafer bond level 3104 to layer 3102"), 55; EX1037, ¶41.

For Lee-Aspar-Endoh, when implementing two of Lee's Figure 1B memory cells, Aspar's process would have been used to transfer a layer stack repeating the layers shown in Lee's Fig. 9 (as shown below) to substrate 3105, flipping them upside down. Pet., 47-48, 58-60, 64 ("form a suitable doped stack...to form SOI pillars with two memory cells").



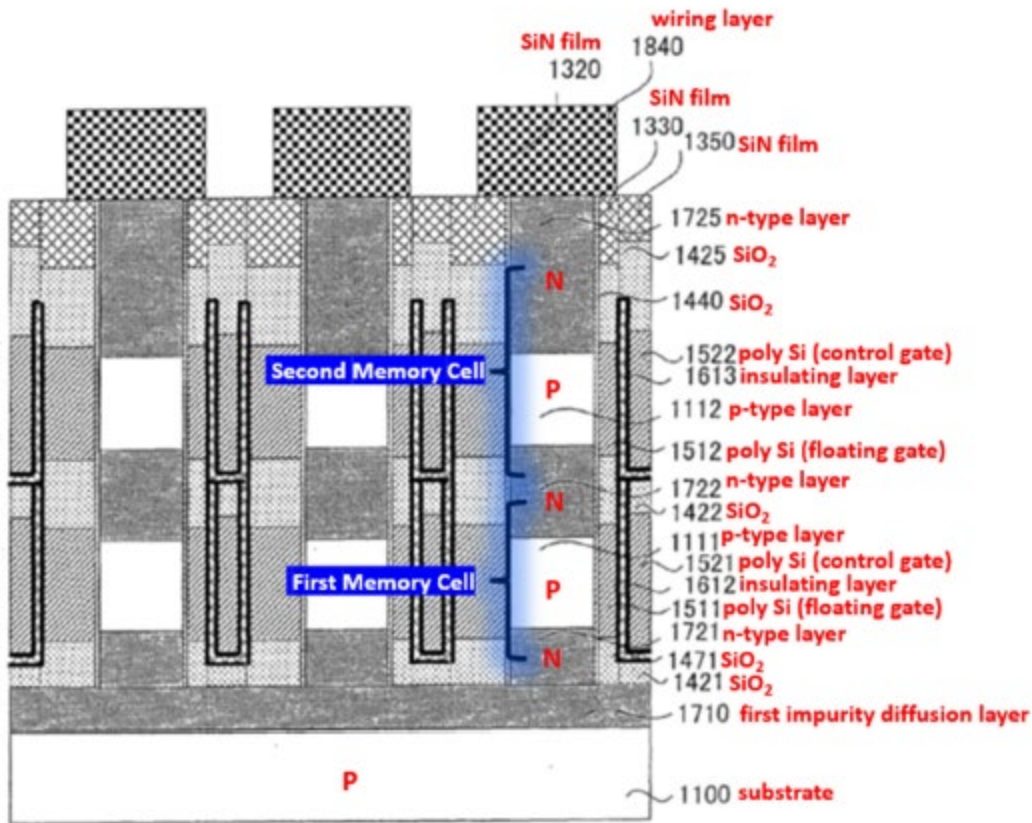
The two stacks would have been patterned to form Lee's Figure 1B's cylindrical pillar. The resulting pillar's cross-section would have resembled those in Lee's Figure 23A below. EX1037, ¶42.



When implementing Endoh's pillar in Lee-Kim, a two-memory cell pillar such as taught in Endoh would be transferred to substrate 3105 using Kim's process. Pet., 45-48, 52-53 ("wafer bond level 3104 to layer 3102"), 55; EX1037, ¶43.

When implementing Endoh's pillar in Lee-Aspar, an N-P-N-P-N stack with a conductive layer would be transferred to substrate 3105 using Aspar's process. Pet., 45-50, 58-60, 64 ("form a suitable doped stack"); EX1037, ¶43. That stack would have been patterned to form pillars shown below, with each pillar containing two memory cells. Pet., 44-45.

Fig. 1171



PO's Endoh-based criticisms are unavailing. First, PO argues reduced density because of decreased number of control gates per memory cell. POR, 39-40. PO misunderstands the combinations, which “modify Lee’s device level 3104 in array 3101 to incorporate two memory cells on each pillar as taught in Endoh.” Pet. 47-50, 55, 64; EX1037, ¶44. As one example, Lee’s Figure 1B cylindrical single-cell pillar embodiment includes a “single control gate [112]” (blue) that surrounds pillar

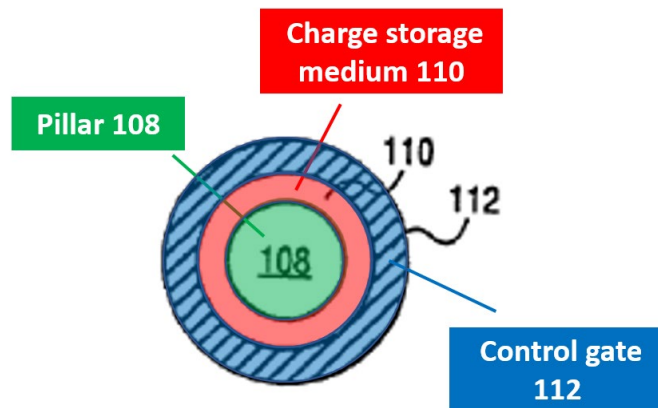


FIG. 1B

108 (green). Pet. 26, 47; EX1007, ¶¶39, 125. Implementing two of Lee’s Figure 1B cells in a pillar or Endoh’s two-cell pillar—which is also cylindrical—would have increased density (two memory cells per pillar instead of one) while

maintaining the number of control gates per cell (one). Pet. 42-46; EX1012, Figs. 1, 1171-72; EX1037, ¶44. The Grounds 1B, 1D, 1F combinations render each of claims 16 and 17 obvious with a reasonable expectation of success. Pet., 41-50, 55, 64.

PO hints that Intel did not explain how the combinations render claim 13 obvious. POR, 37-38. But the Petition explains how Lee’s Figures 1A, 1B, 2, and 7 memory cell meets the limitations of claim 13 (Pet., 16-31; EX1056, 63:17-23, 69:21-71:3, 72:10-19, 75:25-76:12, 79:18-25, 80:16-23, 81:10-16) and also describes that Endoh’s memory cells are “vertically oriented” and “nonvolatile,” and “hav[e] at least one transistor,” as claim 13 requires (Pet., 42, 45-46, 55, 64, 73). EX1037, ¶45.

PO asserts POSITAs would not have modified Lee’s Figure 25A based on Endoh. POR, 41-42. Intel does not rely on Lee’s Figure 25A in the combination;

instead, Intel pointed to Figure 25A in these grounds only as supporting “motivation to incorporate two memory cells on each pillar” and reasonable expectation of success. *See* Pet. 47-48, 50, 55, 64⁵; EX1037, ¶46.

PO faults Intel for not explaining exactly how POSITAs would have combined Lee and Endoh. POR, 42-43. But as explained above, implementing the combination was well within POSITAs’ knowledge and involved using known techniques to address a known problem according to their established functions to achieve predictable results. EX1037, ¶47.

c) Intel’s Lee-based combinations are fully supported

PO criticizes Intel’s Lee-based Ground 1D, arguing it is unclear to cross-reference to prior Grounds 1B and 1C that relate to different claim constructions. POR, 35-37. The Petition identifies exactly which constructions are addressed in Ground 1D. Pet., 55. Intel’s claim construction arguments are straightforward. *See* table, §II.C. Lee is the base reference for Grounds 1A-1F, and Johnson is the base reference for Grounds 2A-2C; Kim and Aspar are used for claims 13-17 in Grounds

⁵ Ground 1F’s Figure 25A reference explains Lee-Aspar, but the Petition continues: POSITAs “would have also found it obvious to form a suitable doped stack of the stackable add-on layer added using SOI technology to form SOI pillars with two memory cells as taught in Endoh.” Pet. 64.

1C-1F, which relate to Intel’s and the Board’s construction of “stackable add-on layer [is/being] bonded”; Aspar is used to address Intel’s construction of “SOI pillar”; and Endoh is an alternative to Lee for teaching the additional limitations of claims 16 and 17. Pet. 3; EX1037, ¶48.

PO further argues Intel cannot rely on rationales for combining Lee-Endoh and Lee-Kim/Aspar to support the combination of Lee-Endoh-Kim/Aspar. POR, 36-37 (citing DI, 42; *In re Magnum Oil Tools Int’l*, 829 F.3d 1364, 1380 (Fed. Cir. 2016)). *Magnum Oil* is inapplicable because in that case, the petitioner argued, without explanation, the same motivation to combine applied to combinations of *different art*. In contrast, Intel referred back to its obviousness arguments relating to the same art, adding analysis for the Lee-Kim/Aspar-Endoh combination. Pet., 55, 64; EX1037, ¶49.

E. Johnson, alone or in combination, renders Claim 13 obvious (Grounds 2A-2C)

Under PO’s apparent construction of “stackable add-on layer” encompassing deposition to add a memory layer, Johnson renders claim 13 obvious (Ground 2A). If the Board adopts its preliminary claim construction or Intel’s, Johnson-Kim or Johnson-Aspar renders claim 13 obvious (Grounds 2B, 2C). In those combinations, the Petition describes a layer formed separately from the substrate and then bonded to a dielectric layer above the substrate, as required by the Board’s construction. DI, 9, 11; Pet., 75, 79.

1. Under PO's apparent construction, Johnson alone or in combination renders obvious claim 13 (Ground 2A-C)

PO argues Johnson lacks just one limitation in claim 13: “memory cells having at least one transistor.” POR, 57-62. PO reaches that conclusion only by claiming the “transistors” described in Johnson are not in fact “transistors.” PO also argues POSITAs would not have modified Johnson’s memory cells to include transistors different from those described. POR, 59-60, 62-65, 70, 75. Intel never argued POSITAs would have made any such modifications. EX1037, ¶51.

a) Johnson teaches memory cells including transistors

PO incorrectly argues Johnson does not teach “memory cells having at least one transistor.” POR, 57-62, 75. Johnson expressly discloses using a “junction field-effect transistor” (JFET) or “MOSFET” (metal oxide semiconductor field-effect transistor) as a steering element in a memory cell. Pet., 72-73; EX1010, 2:30-31, 5:49-51, 7:61-8:5. Indeed, fabrication and operation of such diode-connected transistors had long been known, and their use in memory cells was also not new. EX1051, 271-3; EX1052, 1:57-61, 2:17-21, 5:33-37, 5:47-52 (collectively describing a memory cell where current flows in one direction in the MOS diode), Fig. 4; EX1053, Abstract, 1:39-57, 2:51-60, 3:9-11, 5:3-20 (fabrication of a reduced-size diode-connected semiconductor device and transistor); EX2045, 153 (JFET with gate connected to source), 180-183 (JFET diode); EX2029, ¶179; EX1037, ¶¶52-54.

b) Johnson does not teach away from using transistor memory cells

Johnson expressly teaches memory cells with transistors. EX1010, 7:61-8:5, 10:34-37; *contra* POR, 61-62. Although Johnson describes cost and density issues with some memories including transistors “built in planar the substrate” (EX1010, 2:6-36), Johnson avoided those issues by using memory cells with vertically-oriented state change and transistor-based steering elements “not built into planar substrates” (EX1010, 5:41-48). Johnson’s transistors provided additional benefits of no supporting circuitry and being self-activating. EX1037, ¶55.

c) Johnson JFETs and MOSFETs would have worked

PO argues Johnson does not “enable” the disclosed transistors. POR, 60-61. “[T]he claimed and unclaimed disclosures in a prior art patent,” like Johnson, “are [presumed] enabled.” *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1355 (Fed. Cir. 2003). Moreover, “a prior art reference asserted under §103 does not necessarily have to enable its own disclosure, i.e., be ‘self-enabling,’ to be relevant to the obviousness inquiry,” and may “supply claim elements enabled by...evidence of record.” *Raytheon Techs. Corp. v. Gen. Elec. Co.*, 993 F.3d 1374, 1380 (Fed. Cir. 2021). The MOSFET disclosed in Johnson was known to work just fine. EX1037, ¶¶58; §II.E.1.a

PO cannot avoid Johnson’s teachings. Johnson uses transistors in its memory cells (EX1010, 5:41-48, 7:58-8:5), and the Petition relies on those disclosures for

obviousness. Pet., 72-73; EX1037, ¶¶56-57. PO emphasizes Johnson’s teachings of a “self-aligned” fabrication technique for diode-only memory cells. POR, 64. But Johnson teaches “memory cell[s] may also be fabricated using alternative embodiments” (EX1010, 6:46-62; 15:12-26), such as photomasking steps used “to explicitly define the pillar itself” (*id.*, 15:12-26). Johnson describes the “memory cell: pillar” can include transistors. *Id.*, 7:31, 7:58-8:5. POSITAs knew how to form vertical transistors. EX1037, ¶59; EX1007, Figs. 1A, 8A-9B, 13A-16A, ¶¶122, 140-141, 148-154. Thus, a masking process would have been used to fabricate memory cell pillars with transistors. EX1037, ¶59. Furthermore, Johnson’s self-alignment techniques would still be used because Johnson-Aspar merely transfers layers of material, resulting in Johnson Figure 6(b). Pet., 78-79. Johnson’s self-alignment techniques can then be used. *See* EX1010, 12:42-65, 13:20-14:34. Those cells would have been part of Johnson-Kim/Aspar. EX1037, ¶59.

PO further asserts POSITAs would not have modified Johnson’s transistors. POR, 62-65, 70, 75. But Intel never suggested that any such modification was needed. EX1037, ¶60.

2. POSITAs would have combined Johnson with Kim/Aspar (Grounds 2B, 2C)

In resisting Johnson-Kim/Aspar, PO mostly parrots its arguments regarding Lee-Kim/Aspar. POR, 65-74. As the chart below describes, Intel already undercut those positions. EX1037, ¶61.

PO Argument	Intel Response
Bonding is not obvious just because it is known (POR, 66, 72)	§II.D.1.d; Pet., 74-76
Quality control is not a motivation to combine (POR, 67-68, 73)	§II.D.1.c
Alignment is a concern (POR 66, 68, 71-72)	§II.E.1.c
Aspar requires 1100°C annealing (POR, 72, 74)	§II.D.1.f; Pet., 74-75, 78-80

PO's other arguments relating to Johnson are similarly faulty.

- PO states Johnson does not disclose access points for testing. POR, 67, 73. POSITAs would have known how to test circuits, as PO admits (POR 27 (“There’s no dispute semiconductor fabs routinely test monolithic devices they build.”)). EX1016, 1:48-50; EX2039, 110:21-112:4; EX1037, ¶62.

- Regarding Johnson-Aspar, PO argues “Intel again doesn’t show how reversing Johnson’s self-aligned deposition process could be built using stacking instead, or how it would overcome the alignment pitfalls Johnson’s method avoided.” POR 71-72. Johnson’s self-alignment techniques can still be used because Johnson-Aspar merely transfers layers of material, resulting in Figure 6(b). Pet., 78-79. Johnson’s self-alignment techniques can then be used. EX1010, 12:42-65, 13:26-14:34. PO also argues Intel “says to fabricate [Johnson’s] Fig. 6(a) diode pillar upside down” without explaining how to do it.

POR, 74. In the combination, Johnson's Figure 6(b) is inverted, formed on the substrate of Wafer A, and then flipped and bonded onto Wafer B. Pet., 78; EX1010, 13:26-14:34, 15:44-55; EX1037, ¶63. PO's argument does not address the combination as presented.

- Regarding Johnson-Kim, PO argues "Intel never provides the required reason why one of skill would have abandoned Johnson's self-aligned deposition technique for Kim's wafer bonding." POR, 66. Johnson, however, is not limited to self-alignment. EX1010, 6:46-62, 15:12-26. PO also asserts the combination "reverses Johnson's process" and relies on "intermediate steps." POR, 68-69. None of that undermines the combination, and PO provides no support for its assertions about cost and yield except its expert's say-so. *See* EX-1010, 6:46-62, 7:49-57, 15:12-26, 15:32-57; EX1037, ¶64.

- PO argues Johnson-Kim leaves "strips 53a and 53b without any purpose." POR, 68-69. Nothing in claim 13 precludes having such strips, and POSITAs would have recognized Johnson's strips would be useful for forming additional memory layers if desired. EX1037, ¶65; EX-1010, 4:34-54, 13:19-20, 14:10-12, 14:25-27.

F. The Park-Kim combination renders claim 1 obvious

PO asserts Park does not disclose "memory cells separated from each other by dielectric material." POR, 75-79. Such material separates Park's memory cells'

transistors and capacitors from other structures. Pet., 88-89. Accordingly, the cells are electrically separated, as necessary for proper operation. *Id.*, 89; EX1037, ¶66. PO suggests a dielectric material must form the entire physical boundary between two cells. POR, 76-77. But the '702 patent supports Intel's position: floating devices "separated by dielectric isolated regions" as "electrically separated structures." '702Pat, 6:6-10. '702 Figure 1 does not support a complete-separation requirement (POR, 78) because it is never described as a DRAM embodiment ('702Pat., 2:13-15, 3:51-54, 5:17-7:60). Instead, Figures 9-10 support the '702 patent's DRAM embodiments are not limited in the way PO alleges.

III. CONCLUSION

The Challenged Claims are unpatentable.

Respectfully submitted,

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Date: June 5, 2024

CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(D)

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned Petition for *Inter Partes* Review of U.S. Patent 7,378,702, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Reply, that the number of words in this paper is 5,600. Pursuant to 37 C.F.R. §42.24(c), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served a true and correct copy of the foregoing: PETITIONER'S REPLY by email to the electronic service addresses for Patent Owner:

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