

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner

v.

BESANG INC.,

Patent Owner

Case IPR2023-00991

U.S. Patent No. 7,378,702

REPLY DECLARATION OF DR. CARL SECHEN
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,378,702

Table of Contents

	<u>Page</u>
I. INTRODUCTION	1
II. MATERIALS REVIEWED	1
III. CLAIM CONSTRUCTION	2
A. “Stackable add-on layer ... the stackable add-on layer [is]/[being] bonded” (Claims 1 and 13)	2
B. “SOI pillar” (Claims 14–17)	3
IV. GROUNDS OF UNPATENTABILITY.....	5
A. Lee-based Grounds 1A-1F	5
1. Claim 13 is unpatentable.....	5
a. Kim and Aspar in combination with Lee (Grounds 1C, 1E)	6
b. Lee suggests stacking (Grounds 1C, 1E).....	7
c. Quality control purposes provided motivation to combine (Grounds 1C, 1E)	9
d. Process optimization also provided motivation to combine (Grounds 1C, 1E)	10
e. Lee’s Figure 25A and purported “interleaved levels” (Grounds 1C-1F)	12
f. PO’s description of Aspar and the Smart-Cut process (Ground 1E)	14
g. Reasonable expectation of success	16
2. Lee alone or in combination renders claims 14-17 unpatentable	18
3. Claims 16-17 are obvious	19

a.	Lee’s serially-connected memory cells	19
b.	A POSITA would have combined Endoh with Lee and Endoh with Lee and Kim or Aspar	21
c.	The Lee-based combinations are fully supported.....	26
B.	Johnson, alone or in combination, renders Claim 13 obvious (Grounds 2A-2C).....	27
1.	Johnson alone or in combination renders obvious claim 13 under the Patent Owner’s apparent construction (Ground 2A).....	28
a.	Johnson teaches memory cells that include transistors.....	28
b.	Johnson expressly teaches using transistor memory cells without teaching away.....	30
c.	Johnson JFETs and MOSFETs would have worked	30
2.	Johnson in combination with with Kim or Aspar (Grounds 2B, 2C).....	34
C.	The Park-Kim combination renders claim 1 obvious	36

I, **Dr. Carl Sechen**, declare as follows:

I. INTRODUCTION

1. I have been asked by Counsel for Petitioner (“Counsel”) to respond to certain opinions expressed by Patent Owner’s (“PO”) expert in the Declaration of Dr. Steven A. Przybylski in support of Patent Owner’s Response to Petition for *Inter Partes* Review (Exhibit 2029) (“Przybylski Declaration”). My opinions, and the bases for those opinions, are set forth below.

2. As I stated in my earlier declaration in this proceeding (“Sechen Declaration”) (Ex. 1003), I am being paid at my ordinary and customary consulting rate of \$425 per hour. My compensation in no way depends on the outcome of this matter. I have no other financial interest in this proceeding. Ex. 1003, ¶3.

3. I provided my qualifications in the Sechen Declaration. Ex. 1003, ¶¶4-15.

II. MATERIALS REVIEWED

4. My opinions contained in this Reply Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge of the field.

5. In forming my opinions expressed in this Reply Declaration, I have reviewed and considered the Przybylski Declaration (Exhibit 2029), exhibits cited

by the Przybylski Declaration, materials identified in this Reply Declaration, and materials listed in the Sechen Declaration (Ex. 1003, ¶18).

6. As I stated in the Sechen Declaration (Ex. 1003, ¶19), my opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the claims and the specification of the '702 Patent, and the '941 Patent incorporated-by-reference in its entirety, at the time of the alleged invention, which I have been asked to initially consider as being no earlier than September 3, 2004 (the filing date of U.S. Patent Application No. 10/934,270). My opinions reflect how one of ordinary skill in the art would have understood the '702 Patent, the prior art to the patent, and the state of the art at the time of the alleged invention. My opinions would remain the same even if the '702 Patent were entitled to priority to U.S. Patent Application No. 10/873,969, such that the priority date would be June 21, 2004.

III. CLAIM CONSTRUCTION

A. “Stackable add-on layer ... the stackable add-on layer [is]/[being] bonded” (Claims 1 and 13)

7. Dr. Przybylski offers no opinion regarding the construction of “stackable add-on layer” and “the stackable add-on layer [is]/[being] bonded.” Instead, he assumed that Intel’s proposed construction of these terms is correct. Ex. 2029, ¶88. I stand by my construction of these terms (Ex. 1003, ¶¶71-83), which

matches Intel's (Petition for *Inter Partes* Review of U.S. Patent No. 7,378,702 (IPR2023-00991, Paper No. 1) ("Petition"), 10-13). I have also considered the Board's preliminary construction of these terms, which does not require wafer bonding: "a separate layer that is formed apart from the substrate and then subsequently bonded to the substrate or a dielectric layer above the substrate." Decision Granting Institution (IPR2023-00991, Paper No. 12) ("DI") 9, 11. The Board further stated it did "not understand a 'stackable add-on layer' to include memory cells that are formed by sequential deposition on or above a substrate or dielectric layer without being added to a separately formed substrate." DI, 9. In my opinion, the prior art and prior art combinations that render obvious claims 13-17 of the '702 patent under my construction also render those claims obvious under the Board's construction.

B. "SOI pillar" (Claims 14–17)

8. Dr. Przybylski opined that "SOI pillar" in the '702 patent means "a silicon-on-insulator structure taller than it is wide." Ex. 2029, ¶¶94. I disagree. Dr. Przybylski's proposal does not address the description of "SOI" in the '702 patent, which relates to the composition of a pillar containing crystalline silicon and how it is created, and is encompassed by my construction ("formed in a stackable add-on layer added using SOI technology"). Ex. 1003, ¶¶85-91. By contrast, Dr. Przybylski describes SOI as "silicon-on-insulator" and points to any "silicon structures" "on or

above an insulating layer.” EX2029, ¶90. This confirms the validity of analysis in my Declaration (Ex. 1003) based on the assumption (Ex. 1003, ¶92) that Patent Owner might construe “SOI pillar” as “any pillar-shaped structure with insulating material below it.”

9. The ’702 patent does not limit a “pillar” to any particular shape. Dr. Przybylski complains that I did not refer to dictionaries for the plain and ordinary meaning of “pillar.” EX2029, ¶95. His criticism is not well taken. Consistent with my understanding of the relevant law (Ex. 1003, ¶26), I provided a construction of “SOI pillar” consistent with the claims and specification of the ’702 patent (including the disclosure of the parent ’941 patent) and the knowledge of one of skill in the art at the time the ’702 patent was filed. Ex. 1003, ¶¶85-91; EX2039, 17:22-19:13. Moreover, Dr. Przybylski’s dictionaries do not appear helpful. Although he points to definitions that mention height relative to width, the dictionaries he cites recognize that “pillar” could be “any upright supporting part” or “post.” Ex. 2029, ¶93; EX2031; EX2032.

10. Even if Dr. Przybylski is correct that the ’702 patent specification does not “define what a pillar, is” (sic) in the sense of providing a definitional statement such as one would find in a dictionary (Ex. 2029, ¶93), the ’702 patent describes a “doped stacked structure” as a pillar and no other structures as a pillar. ’702 Patent, 6:26-29 (“doped stacked structures (i.e., pillar structures)”; Figs. 4, 6, 8, 12, 20, 27.

11. In any event, as I discuss below, in my opinion, the references that disclosed an “SOI pillar” under my construction also disclose it under Dr. Przybylski’s construction, which tracks what I assumed in the Sechen Declaration but adds “taller than it is wide.”

IV. GROUNDS OF UNPATENTABILITY

A. Lee-based Grounds 1A-1F

1. Claim 13 is unpatentable

12. If the Board adopts its preliminary construction relating to this phrase (“a separate layer that is formed apart from the substrate and then subsequently bonded to the substrate or a dielectric layer above the substrate”) (DI, 9, 11), claim 13 is unpatentable based on the combination of Lee with Kim or Aspar (Grounds 1C, 1E).¹ Although I applied Intel’s construction in those grounds, I described a layer (Lee’s layer 3104 for the Lee-Kim combination or doped stack/conductive layer for the Lee-Aspar combination) that is formed separately from the substrate (Lee’s substrate 3105) and then bonded to the substrate or a dielectric layer (Lee’s layer 3102) above the substrate, as required by the Board’s preliminary construction. DI, 9, 11; Ex. 1003, ¶¶190-194, 209-211, 215. As to claim 13 in grounds 1C and

¹ Prior art disclosing the limitation under Intel’s construction also discloses it under the Board’s construction.

1E, PO contests only motivation to combine and reasonable expectation of success. POR, 20-31, 44-52. Dr. Przybylski offers no opinion regarding whether Lee teaches all limitations of claim 13 if the Board adopts Patent Owner's apparent construction of "stackable add-on layer [is/being] bonded" (Ground 1A). Ex. 2029, ¶88; Ex. 1003, ¶84.

a. Kim and Aspar in combination with Lee (Grounds 1C, 1E)

13. PO argues that simply because Kim's and Aspar's bonding techniques were known does not mean they would have been obvious. POR, 26-27. Although I opined the techniques were known, I also explained the teachings would have (i) improved Lee and (ii) helped to address the problem described in Lee, Kim, and Aspar of fabricating 3D devices. Ex. 1003, ¶¶195-197, 210-215. In my opinion, the same teachings and the corresponding analysis in the Sechen Declaration show that a POSITA would have found Kim's and Aspar's techniques to have been suitable options for Lee's techniques. Further, Dr. Przybylski does not address that Aspar itself would have motivated a POSITA to combine with Lee: "multiple SOI layers stacks can be easily performed thanks to Smart-Cut technology" and Smart-Cut "transfer[s] thin layers of very good thickness homogeneity and with a high crystalline quality." Ex. 1003, ¶212; EX1009, 834, 839.

b. Lee suggests stacking (Grounds 1C, 1E)

14. I disagree with Dr. Przybylski and the Board as to whether Lee mandates using deposition to add layers in Figure 35. DI, 35; EX2029, 115-18, 123-24. It does not. Nowhere does Lee state that the bottom level of memory device levels 3104 is deposited onto insulating layer 3102. EX1007, ¶111; Ex. 1003, ¶¶190-192. Although Lee uses the term “monolithic” to refer to depositing one array layer *on another within the array*, it does not address how the bottom array layer is attached to underlying structures such as interlayer insulating layer 3102. EX1007, ¶¶107, 294; EX1003, ¶¶192, 204. As I stated at my deposition, monolithic structures can be bonded together. EX2039, 62:2-18, 63:16-64:3.

15. Lee’s description of Figure 35 lacks details that a POSITA would have sought elsewhere, including in Lee’s other embodiments, Kim, and Aspar. EX1003, ¶¶121-134, 189-215. In opining that the first array level in Figure 35 is deposited,² PO relies on Lee’s disclosures regarding the pillar embodiments of Figures 13-28 and my testimony regarding them. POR, 21-22. But those embodiments suggest just one potential implementation of Figure 35.

² The Board pointed to Lee’s paragraph 122 as support (DI, 35), but that paragraph does not refer to any deposition or discuss Figure 35. *See* EX1007, ¶122.

16. Lee also discloses stacking. Lee teaches packaging multiple two-dimensional arrays “together.” EX1007, ¶¶107, 259, 294; EX1003, ¶¶192, 204; EX2039, 61:12-22. Lee further discloses that Figure 35’s array can have self-aligned configurations and contemplates using the techniques at EX1007, ¶¶203-281 with SOI technology, including “wafer bonding. EX1007, ¶¶113, 115, 117, 208 (disclosing driver circuits like those for Figure 35 (EX1007, ¶¶110-111)), 211-212; EX1003, ¶¶116-117, 130-134, 204, 214. While these embodiments suggest implementations relating to Figure 35, they show that the Figure 35 embodiment was not limited to deposition, or the embodiments in Figures 13-28 or ¶122. EX1007, ¶¶110-111. Given Figure 35’s lack of detail, a POSITA would have investigated other useful stacking techniques, such as those found in Kim and Aspar. EX1003, ¶¶190-192, 204.

17. Lee’s disclosures do not support PO’s assertion that stacking is incompatible with Lee. POR, 26. Lee’s general statement about “increased density and a lower cost” applies to all “monolithic” memory arrays, regardless of whether the bottom layer is deposited or bonded to an underlying structure. EX1007, ¶¶106-107, 110-117. In fact, Lee teaches that potential implementations involving SOI technology and wafer bonding “increase[] array density and decrease[] die size and cost.” EX1007, ¶¶204, 207-212, 110-112. Furthermore, Kim teaches stacking with “low costs and high via density.” EX1008, ¶1.

c. Quality control purposes provided motivation to combine (Grounds 1C, 1E)

18. PO argues that “quality control” and “reduced waste” would not have motivated a POSITA to combine Lee with Kim or Aspar. POR, 26-30, 49-50. I disagree. Fung teaches that testing structures before bonding allows screening for defects. EX1016, 1:48-52. As I previously explained, testing would have allowed a chipmaker to identify potentially low-yield wafers and dispose of them before bonding. EX1003 ¶¶196, 213; Ex. 2039, 112:6-113:11. Therefore, testing before bonding would have increased predictability by assuring higher yield while conserving time, material, and cost compared to “bottom up” techniques like deposition. EX1055 (Guarini), 943.

19. PO argues that Fung identifies problems with wafer bonding relating to yield and alignment. POR, 28-29. But testing would have increased yield by screening out defective structures. EX1016, 1:48-50; EX1055 (Guarini), 943. And Fung describes the known technique of using “marks” to secure alignment, just like the ’702 patent. EX1016, 1:58-60, 5:28-31; ’702 Patent, 6:13-18. In any event, Aspar’s process transferred an unpatterned layer or layer stack and did not require wafer alignment, as the ’702 patent recognized (’702 Patent, 6:18-25). EX1049 (Divakauni), 5:26-28.

20. PO argues that Kim's bonding processes would have created more waste rather than less. POR, 29-30, 49-50. That is incorrect. First, although PO contends dies or wafers would have been discarded, he admits that errors in fabrication occur. POR, 29. Fabrication errors that resulted in low-yield wafers would have wasted substrate circuitry. Second, PO argues Kim generated waste by thinning the wafer. POR, 29 (citing EX1008, ¶25). But Kim teaches that thinning was optional (EX1008, ¶25).

21. PO argues that there would be nothing to test in the Lee-Aspar combination. POR, 49. I disagree. In Aspar's process the bonded structures are single layers or layer stacks. EX1009, 838-839. A POSITA would have tested the layers by checking, for example, thickness and uniformity. EX1003, ¶213; EX1047 (Gower-Hall), 295; EX1041 (Gosele), 228; EX1043 (Kwon), 10-11; EX1057 (Kamieniecki), 1:14-18, 2:7-23.

d. Process optimization also provided motivation to combine (Grounds 1C, 1E)

22. At my deposition, Patent Owner's counsel asked me about the benefits of the Lee-Aspar combination, including optimizing processes for separately-fabricated devices and memory structures that are eventually bonded. EX2039, 91:17-98:9 (citing EX1003, ¶213); *see also* EX1003, ¶196 (same opinion for Lee-Kim combination). In response to those questions, I explained it would have been

preferable to process layers separately because, in a linear process “a later processing step can cause perturbations of previous processing steps.” EX2039, 95:12-96:13. Issues that could cause such perturbations included “heat [that] can cause metal to deform possibly creating opens or shorts.” EX2039, 96:15-97:11.

23. My testimony is supported by several references demonstrating the state of the art and knowledge of a POSITA. As Fung confirms, in the sequential deposition approach involving only deposition the “processes involved in forming successive devices can affect the characteristics of devices placed underneath.” EX1016, 1:25-27. Fabricating devices on separate substrates, each according to an optimized process, and then bonding them (as taught in Kim or Aspar) avoids this issue and “offers the potential of...increasing the yield.” *See* EX1008, ¶22; EX1044 (Kwon II), 145-146 (“Processing for each wafer can be optimized for the technology on that wafer.”); EX1049 (Divakauni), 6:42-56 (parallel processing allows for different “heat treatment[s]”); EX1050 (Niklaus), 525 (“One of the main advantages of the new transfer bonding technology is that transducers and integrated circuits can be independently processed and optimized on different wafers....”).

24. Accordingly, a POSITA would have recognized the Lee-Aspar combination’s optimized process benefits, including that Aspar’s process would have benefited Lee by adding monocrystalline silicon, which improves performance, without the downsides of a recrystallization process such as taught in Lee. EX1007,

¶¶402, 404; EX1045 (Doyle), 1:62-66; EX1048 (Street), 98. High temperatures (1000 °C) were needed to form a monocrystalline silicon layer using epitaxy. EX1009, 834; EX1043 (Kwon), 4. But such temperatures damage logic circuits. EX1043 (Kwon), 4; EX1041 (Gosèle), 233. To avoid these issues, a POSITA would have processed a monocrystalline layer (such as used in Aspar) separately and then bonded it to the logic circuits. EX1043 (Kwon), 11. While Lee’s recrystallization process improves performance relative to amorphous or polycrystalline silicon, it requires a “high temperature anneal step” and introduces transition metal contaminants. EX1007, ¶¶405-411; *see* EX1043 (Kwon), 4; EX1045 (Doyle), 1:66-2:6. A POSITA would have understood that Aspar’s process, which provided monocrystalline silicon, did not suffer from these drawbacks.

25. Moreover, as to both the Lee-Aspar and the Lee-Kim combinations, the processing of separate wafers in parallel would have optimized processing by reducing overall processing time, as was known in the art.

e. Lee’s Figure 25A and purported “interleaved levels” (Grounds 1C-1F)

26. PO argues that there is no motivation to “fabricate Lee’s interleaved levels” of memory cells that he says are shown in Figure 25A using Kim’s or Aspar’s “stacking” method. POR, 20-26, 30-31, 43-44, 50. I disagree for several reasons. First, PO’s characterizations of Lee use language that is foreign to that reference.

Although his declaration uses variants of the term “interleave” over a dozen times, that term does not appear in Lee. Simply put, Lee doesn’t describe any of its structures as “interleaved.”

27. Second, PO’s characterization of Lee as teaching “interleaved” structures focuses on Lee’s Figure 25A showing two vertically-connected memory cells. But as I noted previously (Ex. 1003, ¶¶94-102), Lee Figures 1A, 1B, 2, and 7 each show a single memory cell. Yet PO does not argue that “interleaved levels” affect those embodiments or Intel’s combinations for claims 13-15 that are based on them. Pet., 16-17, 17 n.9, 20-31, 50-54, 55-63. Patent Owner declares without elaboration that the single-cell embodiments “are not what Lee discloses as a layer” in Figure 35. POR, 22. That is wrong. Ex. 1003, ¶¶96-102, 130-134. Patent Owner does not address my explanation that “Figure 35 is agnostic as to the particular type or structure of the memory devices in the levels 3104 of array 3101, which it depicts as a rectangular box (i.e., a cross-section showing levels in the array but not any of the details of the devices in each level)” (Ex. 1003, ¶95), “bottom level 3104 of Lee’s array 3101...contain[s] two or more of Lee’s pillar memory devices” (*id.*, ¶121), and that those two memory devices could be any one of Figures 1A, 1B, 2, and 7 (*id.*, ¶¶94-102, 121-134).

28. Third, I disagree with PO relating to Lee’s Figure 25A embodiment. PO contends Intel offers no explanation for how Lee’s “interleaved” levels “can be

recreated by stacking.” POR, 24-25. But the Challenged Claims do not require “interleaving.” In any event, a POSITA would have easily created Figure 25A’s structure. As to the Lee-Kim combination, the memory cells of Figure 25A would have been fabricated as taught in Lee and then stacked on Lee’s insulating layer 3102 as shown in Figure 35. Ex1003, ¶¶190-194. In the Lee-Aspar combination, each doped layer stack would have been added by wafer bonding and processed using Lee’s techniques to create the structures in the first level of Figure 25A and then built upon using Lee’s techniques to create the second level. Ex1003, ¶¶209-215. Although an operational device is not required by claims 16 and 17, a POSITA desiring one based on either combination would have used additional processing techniques taught by Lee, including to form more memory levels than those shown in Figure 25A, as desired. EX1007, ¶169. Lee’s multi-level approach is compatible with Intel’s combinations.

f. PO’s description of Aspar and the Smart-Cut process (Ground 1E)

29. PO argues that a POSITA could not have combined Lee with Aspar with a reasonable expectation of success. POR, 50-52. But that is based on faulty interpretations of Aspar and Smart-Cut. First, PO states that “Aspar is plainly a non-starter because it instructs annealing a wafer at 1100°C.” POR, 44; *see also id.*, 69, 72, 74. But Aspar does not describe annealing a wafer at 1100°C in its Smart-Cut

process. The source of this non-existent step is the Wolf textbooks, which are not included in the grounds based on Aspar.

30. Second, based on the Wolf textbooks, PO argues that *any* Smart-Cut process, including Aspar's, required a post-wafer-splitting anneal step at 1100°C. POR, 10-11, 45-46.³ The '702 patent shows this opinion is incorrect. The '702 patent incorporates the parent '941 patent by reference. '702 Patent, 1:7-10. Like Aspar, the '941 patent discloses a Smart-Cut process with a polishing step following splitting (detaching) without any post-splitting anneal step. '941 Patent, 9:40-47, 10:19-21; Ex1003, ¶¶59-65; EX1009, 835. The '941 patent explains the substrate will not withstand temperatures over 650°C—well below the 1100°C Dr. Przybylski says is necessarily a part of the Smart-Cut process. '941Pat, 8:60-62. Although the '941 patent is highly relevant to an understanding of the disclosures of the '702 patent, Dr. Przybylski appears not to have considered it in forming his opinions: the '941 patent is not listed among the materials he reviewed (EX2029, ¶12) and appears not to have been included in any other part of his declaration.

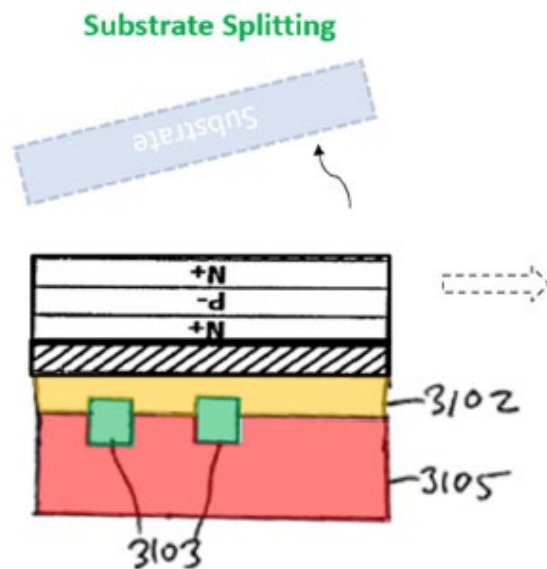
³ PO argues I acknowledged “Smart-Cut taught” an anneal at 1100°C. POR, 46. I did not say that. Rather, I simply acknowledged the version of Smart-Cut disclosed in a Wolf textbook. EX2039, 120:18-121:18.

31. Third, Aspar notes that “the Smart-Cut process really is a generic process. It allows a great deal of combinations (material and bonding layer) which open up new scope for developments.” Pet. 58 (citing EX1009, 839). A POSITA would have recognized that allowing for a “great deal” of material and bonding layer combinations would not be compatible with the one-size-fits-all post-splitting anneal temperature that Dr. Przybylski incorrectly ascribes to Aspar.

g. Reasonable expectation of success

32. I explained, based on Kim’s and Aspar’s teachings, that a POSITA would have expected success in those combinations. Pet., 54, 62. PO disagrees, but mostly he repeats criticisms of Intel’s motivations to combine based on Lee’s “interleaved levels” (for both combinations) and an alleged high-temperature anneal absent from Aspar’s description. POR, 30-31, 50-51. I showed above how those opinions are incorrect.

33. PO argues that I did not account for a thin silicon layer left behind by Aspar's process that, in his view, would have obstructed access to Lee's upper electrical contact. POR, 50-51. PO appears to have misunderstood Aspar and Intel's combination. As shown in the figure below, a POSITA would have followed Aspar's teachings for the splitting step and left behind a thin layer including an N+/P-/N+ doped stack on top of insulating layer (yellow), and substrate (red). Pet., 57-60; EX1009, 834; EX1003, ¶¶209-210. That doped stack would have been used to fashion Lee's memory cells. Pet., 60; EX1007, ¶141.



34. When forming the memory cells, Lee teaches adding an upper electrical contact or forming a second set of memory cells with contacts over the underlying memory cells. EX1007, ¶¶122, 126, 141, 157, Fig. 9B; Pet., 17 n.9, 59-60; *see* EX1007, ¶141, Figs. 1A (I/O conductor 116), 2 (conductive input/output 210), 7 (same), 9B (I/O 906), 25A (M2). The added thin layer (i.e., the transferred doped stack) serves as part of the memory cell and contacts the electrical contact. Accordingly, there is no layer that obstructs the contact in the Lee/Aspar combination.

2. Lee alone or in combination renders claims 14-17 unpatentable

35. Claims 14-17 are unpatentable regardless of whether the Board adopts Intel's or PO's construction of "SOI pillar." The Board preliminarily adopted Intel's construction (DI, 12). The Lee-Aspar combination teaches an "SOI pillar" under that construction because Lee taught the claimed memory structures, Pet., 63 (citing Pet. 31-41), Aspar's Smart-Cut process is "SOI technology" (*id.* (citing Pet. 56-63; EX1009, 834, 837, 839), and the combination includes pillars formed using that SOI technology (*id.* (citing Pet. 56-63; Ex. 1003, ¶217)). That is, Lee's Figure 2 (claim 14); Figures 1A, 1B, or 7 (claim 15); and Figure 25A (claims 16-17) teach "a pillar-shaped doped stacked structure," and those structures would be "formed in a stackable add-on layer added using SOI technology." Pet., 31-37, 56-63.

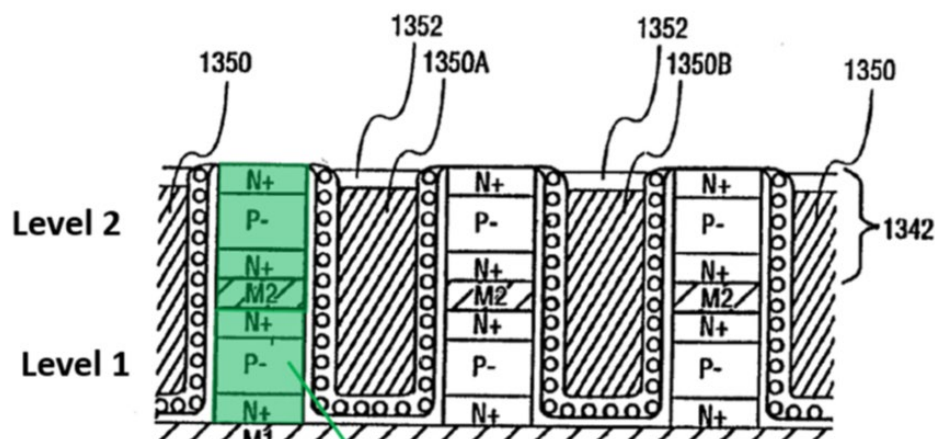
36. If the Board adopts PO's proposed construction for "SOI pillar," Lee alone and the Lee-Kim or Lee-Aspar combination each render claims 14-17 unpatentable. The memory cells in Figures 1A, 1B, 2, 7, and 25A (i) involve silicon on or above an insulator (silicon pillars are formed in Figure 35's bottom level 3104 and have insulating layer 3102 below them (Pet., 33, 36, 39-40; EX1056 (Przybylski Tr.), 84:9-17)) and (ii) are depicted in Lee's figures as taller than they are wide (Pet. 31-41; EX1056 (Przybylski Tr.), 65:25-66:8, 69:12-14, 71:13-25, 73:1-9). Indeed, Lee refers to the memory devices as "pillars" (EX1007, ¶¶38-39, 41, 46, 52, 118,

122, 125-126, 138, Figs. 1A, 1B, 2, 7, 25A; Pet. 21-22), and Dr. Przybylski described the structure in Lee's Figure 1A as "meet[ing] the plain and ordinary meaning of the pillar as drawn" (EX1056 (Przybylski Tr.), 65:25-66:8). Dr. Przybylski does not contest that the prior art teaches claims 14 and 15's additional limitations under Patent Owner's claim construction.

3. Claims 16-17 are obvious

a. Lee's serially-connected memory cells

37. PO argues Lee discloses only memory cells connected in parallel. POR, 33-35, 53, 56. I disagree. Lee discloses serially-connected memory cells/pillars. Pet., 37-41. Lee's Figure 25A below illustrates a step in the process of "integrating [Lee's] pillar memory device...into a multilevel array." EX1007, ¶¶147-69. Lee states, "[t]he process...can be repeated again to complete the fabrication of memory devices" on several levels. *Id.*, ¶¶167-69; Pet. 38 n.12.



38. The vertical memory cells in Figure 25A lack a conductor at the top of Level 2's memory cells. Without that upper conductor, the cells in Level 2 cannot be connected in parallel with the cells in Level 1 because they have only one electrical connection to the cells in Level 1. That sole connection between cells in Level 1 and Level 2 is through metal layer M2, and therefore, the memory cells are serially connected, one after another, as required by claims 16 and 17. Pet., 38-40. As a result, in view of the intermediate step in Lee's process that is depicted in Figure 25A, Lee discloses or suggests the claimed structure of "vertically oriented and serially connected" memory pillars (claim 16) that are, in turn, connected serially to other pillars (claim 17). Pet., 37-41. Claims 16 and 17 do not preclude later configuring two memory cells to be connected in series or parallel; those cells need only be "serially connected" at some point.

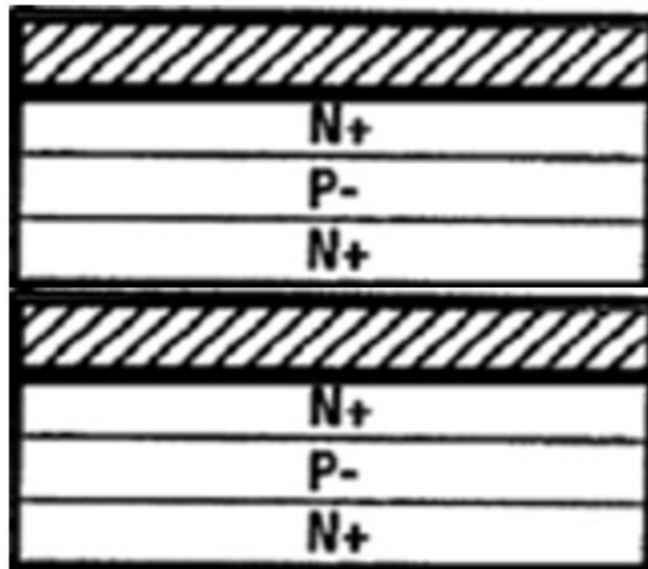
39. PO misinterprets my testimony regarding whether Lee's Figure 25A shows memory cells connected in parallel. POR, 33-34. I acknowledged that a NOR configuration "would be an implication" of a connection of M2 in Figure 25A. EX2039, 58:10-60:7. In that context, I was assuming a completed device with an upper electrical contact and supporting circuitry.

b. A POSITA would have combined Endoh with Lee and Endoh with Lee and Kim or Aspar

40. A POSITA would have applied Endoh's teaching of two serially-connected memory cells in a pillar to Lee, including in combination with Kim or Aspar. Pet., 47-48, 55, 64. These combinations would have resulted in, for example, implementing in Lee's layer 3104: (i) two of Lee's Figure 1B memory cells in a pillar or (ii) Endoh's two-cell pillar. Pet., 47-48, 55, 64. It would have been obvious to use Kim's or Aspar's wafer bonding process for either option. Pet. 55, 64.

41. For the Lee-Kim-Endoh combination, when implementing two of Lee's Figure 1B memory cells, Kim's process would have been used to transfer pillars with two of those already-formed memory cells to substrate 3105. Pet. 47-48 ("modify...level 3104...to incorporate two memory cells on each pillar"), 52-53 ("wafer bond level 3104 to layer 3102"), 55.

42. For the Lee-Aspar-Endoh combination, when implementing two of Lee's Figure 1B memory cells, Aspar's process would have been used to transfer a layer stack that repeats the layers shown in Lee's Fig. 9 (as shown in the figure below) to substrate 3105, flipping them upside down. Pet., 47-48, 58-60, 64 ("form a suitable doped stack...to form SOI pillars with two memory cells").



The two stacks would have been patterned to form the cylindrical pillar of Lee's Figure 1B. The cross-section of the resulting pillars would have resembled those shown in Lee's Figure 23A below.

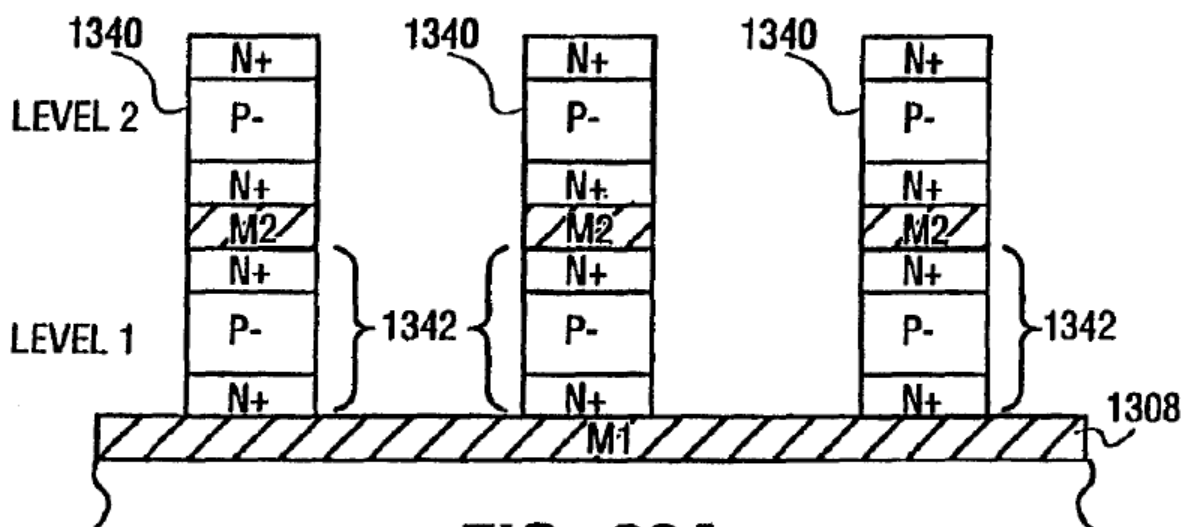
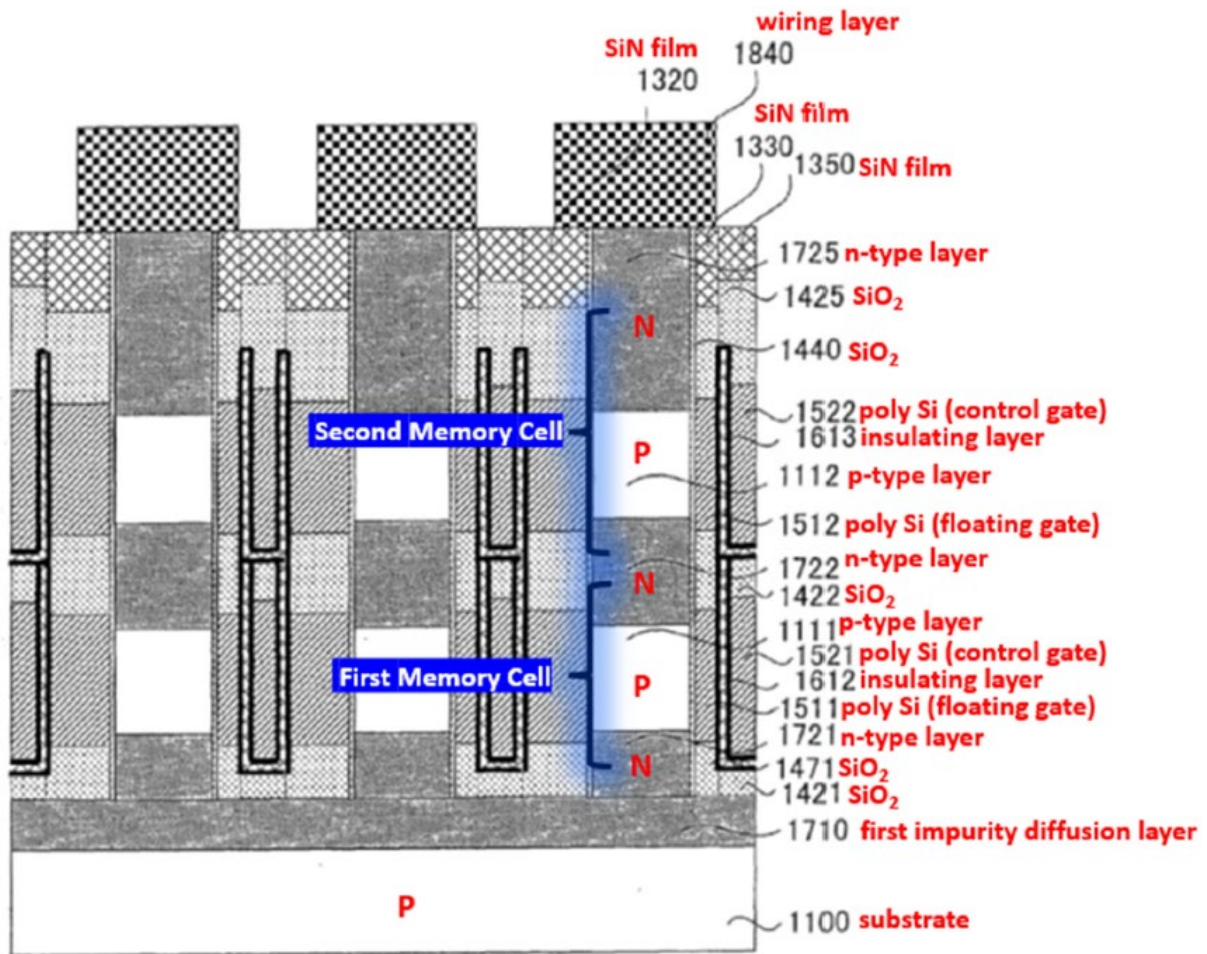


FIG. 23A

43. When implementing Endoh's pillar in the Lee-Kim combination, a two-memory cell pillar such as taught in Endoh would have been transferred to substrate 3105 using Kim's wafer bonding process. Pet., 45-46, 52-53 ("wafer bond level 3104 to layer 3102"), 55. When implementing Endoh's pillar in the Lee-Aspar combination, a POSITA would have transferred an N-P-N-P-N stack with a conductive layer to substrate 3105 using Aspar's wafer bonding process. Pet., 45-50, 58-60, 64 ("form a suitable doped stack"). That stack would have been patterned to form pillars shown in the figure below, with each pillar containing two memory cells. Pet., 44-45.

Fig. 1171



44. PO argues the combinations would have reduced density by decreasing the number of control gates per memory cell. POR, 39-40. PO appears to have misunderstood the combinations, which “modify Lee’s device level 3104 in array 3101 to incorporate two memory cells on each pillar as taught in Endoh.” Pet. 47-50, 55, 64. As one example, Lee’s Figure 1B (annotated below) cylindrical single-cell pillar embodiment includes a “single control gate [112]” (blue) that surrounds pillar 108 (green). Pet., 26; EX1007, ¶¶39, 125. Implementing two of Lee’s Figure

1B cells in a pillar or Endoh's two-cell pillar—which is also cylindrical—would have increased density (two memory cells per pillar instead of one) while maintaining the number of control gates per cell (one). Pet. 42-46; EX1012, Figures 1171-1172. In my opinion, a POSITA would have had a reasonable expectation of success in making the combinations of Grounds 1B, 1D, and 1F, and therefore claims 16 and 17 were obvious. Pet., 41-50, 55, 64.

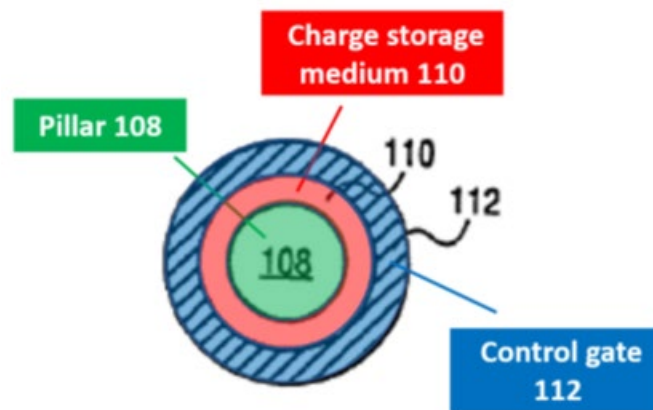


FIG. 1B

45. Although PO hints that I did not explain how the Lee-Endoh combinations render claim 13 obvious (POR, 37-38), I explained in the Sechen Declaration how each of Lee's Figures 1A, 1B, 2, and 7 memory cells meets the limitations of claim 13 (Pet., 16-31; EX1056 (Przybylski Tr.), 63:17-23, 69:21-71:3, 72:10-19, 75:25-76:12, 79:18-25, 80:16-23, 81:10-16) and showed that Endoh's memory cells are "vertically oriented," "nonvolatile," and "hav[e] at least one transistor," as claim 13 requires. Pet., 42, 45-46, 55, 64, 73.

46. PO argues that a POSITA would not have modified Lee's Figure 25A based on Endoh. POR, 41-42. However, I did not rely on Lee's Figure 25A in the combination; instead, as discussed above, I pointed to Figure 25A in these grounds only as supporting "motivation to incorporate two memory cells on each pillar" and reasonable expectation of success. *See* Pet. 47-48, 50, 55, 64.⁶

47. PO argues that I did not sufficiently explain exactly how a POSITA would have combined Lee and Endoh. POR, 42-43. But as explained above, implementing the combination was well within the knowledge of a POSITA and involved using known techniques to address a known problem according to their established functions to achieve predictable results.

c. The Lee-based combinations are fully supported

48. Dr. Przybylski criticizes Lee-based Ground 1D, complaining that it is unclear to cross-reference to prior Grounds 1B and 1C that relate to different claim constructions. Ex. 2029, ¶¶135-138 [POR, 35-37]. But the Sechen Declaration identified exactly which constructions are addressed in Ground 1D. Pet., 55. And

⁶ Ground 1F's reference to Figure 25A explains the Lee-Aspar combination, but the Petition continues: "A POSITA would have also found it obvious to form a suitable doped stack of the stackable add-on layer added using SOI technology to form SOI pillars with two memory cells as taught in Endoh." Pet. 64.

my claim construction arguments are straightforward. I used Lee as the base reference for Grounds 1A-1F, and Johnson as the base reference for Grounds 2A-2C. I used other references to address specific claim constructions. I used Kim and Aspar for claims 13-17 in Grounds 1C-1F, which relate to Intel's construction of "stackable add-on layer [is/being] bonded" and the Board's construction. I used Aspar to address Intel's construction of "SOI pillar." Endoh is an alternative to Lee for teaching the additional limitations of claims 16 and 17. Pet, 3.

49. Dr. Przybylski also appears to opine that Intel cannot rely on rationales for combining Lee and Endoh and Lee and Kim/Aspar to support the combination of Lee, Endoh, and Kim/Aspar. Ex. 2029, ¶¶136-138 [POR 36-37]. But I referred back to my obviousness arguments relating to the same art, adding analysis for the Lee-Kim/Aspar-Endoh combination. Pet., 55, 64. I provided further details relating to the combination above.

B. Johnson, alone or in combination, renders Claim 13 obvious (Grounds 2A-2C)

50. Under the Patent Owner's apparent construction of "stackable add-on layer" encompassing deposition to add a memory layer, in my opinion Johnson renders claim 13 obvious (Ground 2A). Ex. 1003, ¶¶220 to 243. Under the Board's preliminary claim construction or Intel's, the combination of Johnson and Kim or Aspar renders claim 13 obvious (Grounds 2B, 2C). Ex. 1003, ¶¶244 to 263. In those

combinations, I described a layer that is formed separately from the substrate and then bonded to a dielectric layer above the substrate, as required by the Board's construction. DI, 9, 11; Ex. 1003, ¶¶ 247-248, 257-259.

1. Johnson alone or in combination renders obvious claim 13 under the Patent Owner's apparent construction (Ground 2A)

51. PO argues that Johnson lacks just one limitation in claim 13: "memory cells having at least one transistor." POR, 57-62. PO reaches that conclusion only by claiming the "transistors" described in Johnson are not in fact "transistors." PO also argues that a POSITA would not have modified Johnson's memory cells to include transistors different from those described. POR, 59-60, 62-65, 70, 75. But I did not suggest that a POSITA would have made any such modifications.

a. Johnson teaches memory cells that include transistors

52. PO argues that Johnson does not teach "memory cells having at least one transistor." POR, 57-62, 75. That is incorrect. Johnson expressly discloses using a "junction field-effect transistor" (JFET) or "MOSFET" (metal oxide semiconductor field-effect transistor) as a steering element in a memory cell. Pet., 72-73; EX1010, 2:30-31, 5:49-51, 7:61-8:5.

53. Johnson further explains that its steering element "is a device with a strongly asymmetric current-versus-voltage characteristic; it conducts more readily in one direction than in the other." EX1010, 5:49-51. That is precisely what a diode-

connected JFET or MOSFET does. Moreover, fabrication and operation of such diode-connected transistors had long been known, and their use in memory cells was also not new. EX1051 (Grebene), 271-3; EX1052 (U.S. Manning), 1:57-61, 2:17-21, 5:33-35, 5:47-52 (collectively describing a memory cell where current flows in one direction in the MOS diode), Fig. 4; EX1053 (Wild), 1:39-57, 2:51-60, 3:9-11, 5:3-20 (fabrication of a reduced-size diode-connected semiconductor device and transistor); EX2045, 153 (JFET with gate connected to source), 180-183 (JFET diode); EX2029, ¶179.

54. I disagree with PO because its argument is contrary to Johnson's plain disclosures. PO argues that a diode-connected transistor would act as a diode. POR 59-60. That misses the point. The claim is structural, not functional. Like the claim, the '702 patent describes a memory cell as "hav[ing] at least one vertical transistor" without requiring any specific form or function. '702 Patent, 10:15-17. The question is whether Johnson's memory cells include a transistor structure, as claimed. They do. Given that claim 13 does not distinguish between "3-terminal" and "2-terminal" transistor configurations—it simply recites "transistor"—I do not believe PO's, or Dr. Przybylski's, discussion of "3-terminal" and "2-terminal" transistor configurations is relevant (POR, 57-62).

b. Johnson expressly teaches using transistor memory cells without teaching away

55. Dr. Przybylski opines (Ex. 2029, ¶¶178-180 [POR, 61-62]) that Johnson teaches away from using transistors in memory cell design. I disagree. On the contrary, Johnson (an issued U.S. patent) expressly discloses and claims memory cells with transistors. EX1010, 7:61-8:5, 10:33-36, 25:34-39 (claims 5-6). Dr. Przybylski quotes extensively from Johnson’s discussion *in the “Background of the Invention” section* that identifies shortcomings of *prior art memories*, including transistors “built in planar substrates”. Ex. 2029, ¶180; Ex. 1010, 1:13-3:12. But Johnson avoided those issues by using memory cells with vertically-oriented state change and diode-connected transistor-based steering elements “not built into planar substrates”. EX1010, 5:41-48. In addition, Johnson’s transistors provided additional benefits: they required no supporting circuitry and are self-activating.

c. Johnson JFETs and MOSFETs would have worked

56. PO argues that transistors, JFETs or MOSFETs, work so differently than a diode that they are completely incompatible with Johnson’s design. POR, 62-65, 70, 75. As one example, Dr. Przybylski claims that a specialized form of JFET called a “current regulator diode” (“CRD”) would not function in Johnson’s design “because it has different I-V characteristics than that of a regular PN junction diode or a Schottky diode.” EX2029, ¶175. Even if Dr. Dr. Przybylski is correct that a

diode-connected JFET would operate as a current regulator diode, his conclusions as to its performance in Johnson's memory cell are incorrect. A POSITA would have understood that the current-voltage characteristic shown by Dr. (EX2029, ¶176; reproduced below) satisfies Johnson's requirements for the steering device ("strongly asymmetric current-versus-voltage characteristic; it conducts more readily in one direction than in the other," EX1010, 5:49-51) because it has a low current regime (reverse bias), a high current regime (forward bias "operating range"), and an exponential current-voltage regime between those two regimes.

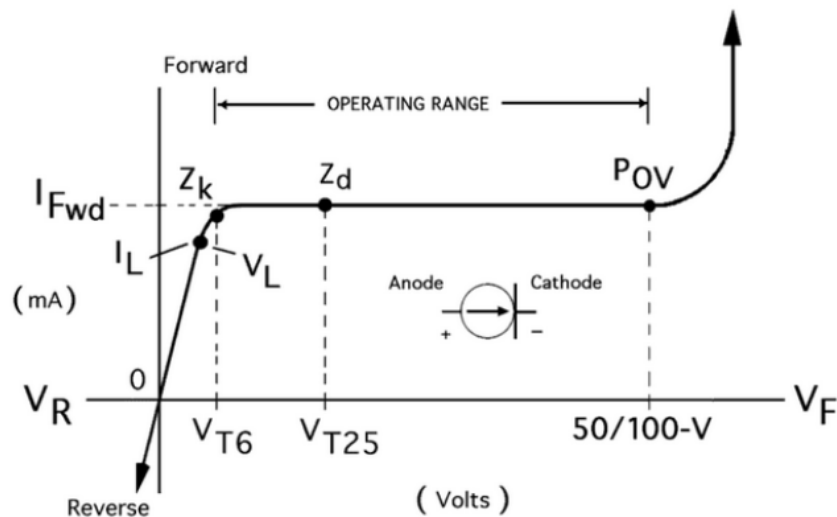


Figure 6.23. The current regulator diode's V-I characteristic curve.

Ex. 2045 (Current Sources & Voltage References), p. 170, Figure 6.23.

Furthermore, a POSITA would have known that the forward current value can be set higher or lower during fabrication of the CRD. Ex. 2045, 168 ("CRDs are monolithic two-terminal devices, specially designed for precise current regulation.

This is achieved by modifying their internal structure, thus creating the equivalent of an internal resistor at the JFET's source (see Figure 6.21A). This internal bulksource resistance sets the output current.”), Figure 6.21A (shown below, where R_s is the internal resistor).

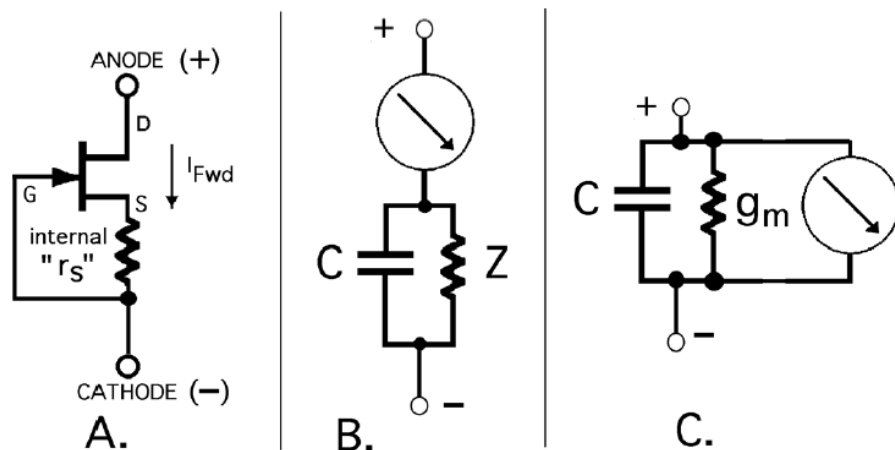


Figure 6.21. CRD equivalent circuits.

57. Moreover, it was well-known that a JFET could be connected in a manner to maintain reverse bias current on the order of pico amps. EX2045, 180-183. This diode-connected JFET also is strongly asymmetric and conducts more readily in one direction than in the other.

58. I note that Dr. Przybylski acknowledges that a diode-connected MOSFET is “configured appropriately” and therefore compatible with Johnson’s design. EX2029, ¶179. Indeed, the disclosed transistor configuration would “block current in one direction between source and drain and allow it to pass in the other”

(*id.*)—exactly what Johnson intended. There is no dispute that the MOSFET disclosed in Johnson was known to work just fine.

59. PO cannot avoid Johnson’s teachings. PO focuses on Johnson’s disclosure of diode-only memory cells. POR, 62-64. But Johnson also discloses using transistors in its memory cells (EX1010, 5:41-48, 7:58-8:5), and I relied on those disclosures to show the claims are obvious. Pet., 72-73. PO emphasizes Johnson’s teachings of a “self-aligned” fabrication technique for diode-only memory cells, as shown in Figure 6. POR, 64. But Johnson teaches “memory cell[s] may also be fabricated using alternative embodiments.” EX1010, 6:46-62, 15:12-26. For example, photomasking steps are used “to explicitly define the pillar itself.” EX1010, 15:12-26. Johnson describes that the “memory cell: pillar” can include transistors. EX1010, 7:31, 7:58-8:5. POSITAs knew how to form a vertical transistor. EX1007, Figs. 1A, 8A-9B, 13A-16A, ¶¶122, 140-141, 148-154. Thus, a masking process would have been used to fabricate memory cell pillars with transistors. Furthermore, Johnson’s self-alignment techniques would still be used because the Johnson-Aspar-based combination merely transfers layers of material, resulting in Johnson Figure 6(b). Pet., 78-79. Johnson’s self-alignment techniques could then be used. *See* EX1010, 12:42-65, 13:20-14:34. Those cells would have been part of the combination of Johnson with Kim or Aspar.

60. PO further asserts a POSITA would not have modified the transistors disclosed in Johnson. POR, 62-65, 70, 75. But I did not suggest that any such modification was needed.

2. Johnson in combination with with Kim or Aspar (Grounds 2B, 2C)

61. In resisting the Johnson-Kim/Aspar combinations, PO mostly repeats its arguments regarding the Lee-Kim/Aspar combinations. POR, 65-74. As described in the chart below, I already refuted those positions in this Reply Declaration.

PO Argument	My Response
Bonding is not obvious just because it is known (POR, 66, 72)	§IV.A.1.a
Quality control is not a motivation to combine (POR, 67-68, 73)	§IV.A.1.b
Alignment is a concern (POR 66, 68, 71-72)	§IV.A.1.c
Aspar requires 1100°C annealing (POR, 72, 74)	§IV.A.1.f

PO's other arguments relating to Johnson are similarly faulty.

62. PO states Johnson does not disclose access points for testing. POR, 67, 73. But a POSITA would have known how to test circuits, as PO admits (POR 27 ("There's no dispute semiconductor fabs routinely test monolithic devices they build.")). EX1016, 1:48-50; EX2039, 110:21-112:4.

63. As to the Johnson-Aspar combination, PO argues “Intel again doesn’t show how reversing Johnson’s self-aligned deposition process could be built using stacking instead, or how it would overcome the alignment pitfalls Johnson’s method avoided.” POR 71-72. Johnson’s self-alignment techniques can still be used because the Johnson-Aspar-based combination merely transfers layers of material, resulting in what is shown in Figure 6(b). Pet., 78-79. Johnson’s self-alignment techniques can then be used. EX1010, 12:42-65, 13:26-14:34. PO also argues Intel “says to fabricate [Johnson’s] Fig. 6(a) diode pillar upside down” without explaining how to do it. POR, 74. But in the combination, Figure 6(b) is inverted, formed on the substrate of Wafer A, and then flipped and bonded onto Wafer B. Pet., 78; EX1010, 13:26-14:34, 15:44-55. PO does not address this combination as presented, instead focusing only on Johnson’s Figure 6(a).

64. Regarding the Johnson-Kim combination, PO argues “Intel never provides the required reason why one of skill would have abandoned Johnson’s self-aligned deposition technique for Kim’s wafer bonding.” POR, 66. Johnson, however, is not limited to self-alignment. EX1010, 6:46-62, 15:12-26. PO asserts the combination “reverses Johnson’s process” and relies on “intermediate steps” in Johnson. POR, 68-69. None of that undermines the combination, and PO provides no support for its assertions about cost and yield. *See* EX-1010, 6:46-62, 7:49-57, 15:12-26, 15:32-57.

65. PO argues the Johnson-Kim combination leaves “strips 53a and 53b without any purpose.” POR, 68-69. But nothing in claim 13 precludes having such strips. In addition, a POSITA would have recognized Johnson’s strips could be used for forming additional memory layers if desired. EX-1010, 4:34-54, 13:19-20, 14:10-12, 14:25-27.

C. The Park-Kim combination renders claim 1 obvious

66. Dr. Przybylski opines Park does not disclose “memory cells separated from each other by dielectric material.” Ex. 2029, ¶¶207-211 [POR, 75-79]. But such material separates the transistors and capacitors of Park’s memory cells from other structures. Pet., 88-89. As a result, the cells are electrically separated, which is necessary for proper operation. *Id.*, 89. Dr. Przybylski suggests a dielectric material must form the entire physical boundary between two cells. Ex. 2029, ¶¶210-211 [POR, 76-77]. Neither ’702 patent claim 1 nor the specification requires that. Indeed, the ’702 patent supports Petitioner’s position, referring to floating devices “*separated by dielectric regions*” as “*electrically separate structures*.” ’702 Patent, 6:6-10 (emphasis added). ’702 Figure 1 does not support a complete-separation requirement for claim 1 (POR 78) because the ’702 patent never describes Figure 1 as a DRAM embodiment (’702Pat., 2:13-15, 3:51-54, 5:17-7:60). Instead, Figures 9-10 (among others) support that the ’702 patent’s DRAM embodiments are not limited in the way Dr. Przybylski alleges.

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 5th day of June, 2024 in Dallas, Texas.

By: Carl Sechen
Dr. Carl Sechen