

Filed on behalf of BeSang Inc.

By: Michelle E. Armond

Douglas R. Wilson

Joseph Li

Yue Han

ARMOND WILSON LLP

4685 MacArthur Court, Suite 390

Newport Beach, CA 92660

Telephone: (949) 932-0778

Email: ipr@armondwilson.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00991
U.S. Patent No. 7,378,702

PATENT OWNER'S SUR-REPLY

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<i>Kinaxis v. Blue Yonder</i> , IPR2021-01302, Paper 38 (P.T.A.B. Feb. 6, 2023)	25, 26
<i>In re Magnum Oil Tools</i> , 829 F.3d 1364 (Fed. Cir. 2016)	12, 21
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OTHER AUTHORITIES

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TABLE OF EXHIBITS

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2001	First Amended Docket Control Order, <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028, Dkt. 54 (E.D. Tex. June 21, 2023)
2002	Docket for <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028 (E.D. Tex.) (as of Sept. 14, 2023)
2003	Docket for <i>BeSang Inc. v. Intel Corp.</i> , Case No. 3:23-cv-00113 (D. Or.) (as of Sept. 14, 2023)
2004	Defendants' Patent Local Rule 3-3 Disclosure of Invalidity Contentions, <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028 (E.D. Tex. July 11, 2023) (cover pleading)
2005	Ann S. Mutschler, <i>Stanford, Korean nanofab center, Oregon-based semi startup claim 3D IC breakthrough</i> , EDN (Aug. 13, 2008), https://www.edn.com/stanford-korean-nanofab-center-oregon-based-semi-startup-claim-3d-ic-breakthrough/
2006	Press Release, <i>Micron and Intel Unveil New 3D NAND Flash Memory Technology Advancements Enable Three Times More Capacity than Other NAND Technologies</i> , Intel (Mar. 26, 2015), https://download.intel.com/newsroom/2021/archive/2015-03-26-news-releases-micron-and-intelunveil-new-3d-nand-flash-memory.pdf
2007	Peter Clarke, <i>EE Times updates list of emerging startups to version 8.0</i> , EE Times (Feb. 2, 2009), https://www.eetimes.com/ee-times-updates-list-of-emerging-startups-to-version-8-0/
2008	<i>Exploring the Potential of Emerging Semiconductor Technology</i> , Global Semiconductor Alliance Forum, Vol. 18, No. 2 (June 2011), https://www.gsaglobal.org/wp-content/uploads/2019/04/201102_GSA_Forum.pdf
2009	<i>Looking Beyond TSV For 3D IC Technology</i> , Frost & Sullivan (Mar. 2009), http://www.growthconsulting.frost.com/web/images.nsf/0/EF8B206A32BBD551652575B4002F3CD5/\$File/TIAlert.htm

Exhibit No.	Description
2010	Press Release, <i>Micron and Intel Extend their Leadership in 3D NAND Flash memory</i> , Globe News Wire (May 21, 2018), https://www.globenewswire.com/news-release/2018/05/21/1509614/14450/en/Micron-and-Intel-Extend-their-Leadership-in-3D-NAND-Flash-memory.html
2011	Micron Unveils 3D NAND (Mar. 26, 2015), https://www.youtube.com/watch?v=Lo-rsZ0vznw
2012	<i>Radar Scope</i> , Semiconductor Times, Vol. 12, No. 4 (Apr. 2007)
2013	RESERVED
2014	1/29/2007 Email from Peter Feeley to BeSang
2015	7/30/2007 Email exchange between Tom Arnold, Sang-Yun Lee, and others
2016	Andy Patrizio, <i>Impact of Intel and Micron ending their NAND partnership is negligible</i> , Network World (Jan. 12, 2018), https://www.networkworld.com/article/3247746/impact-of-intel-and-micron-ending-their-nand-partnership-is-negligible.html
2017	Intel Corporation’s Invalidity Contentions, <i>BeSang Inc. v. Intel Corp.</i> , Case No. 3:23-cv-00113 (D. Or. July 14, 2023) (cover pleading)
2018	USPTO Assignment Abstract of Title for U.S. Patent Application Publication No. 2003/0157748
2019	U.S. District Courts – Combined Civil and Criminal Federal Court Management Statistics (June 30, 2023), https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-june-2023
2020	9/22/2023 Email from Board to Counsel of Record Authorizing Preliminary Reply and Sur-Reply Briefing
2021	Intel Corporation’s Motion to Extend Temporary Stay for Three Months, <i>BeSang Inc. v. Intel Corp.</i> , Case No. 3:23-cv-00113, Dkt. 74 (D. Or. Sept. 15, 2023)
2022	Opinion & Order, <i>BeSang Inc. v. Intel Corp.</i> , Case No. 3:23-cv-00113, Dkt. 80 (D. Or. Oct. 10, 2023) (filing authorized by Board on 10/26/2023)

Exhibit No.	Description
2023	Series Circuit v. Parallel Circuit
2024	Kiyoo Itoh, <i>VLSI Memory Chip Design</i> (Kiyoo Itoh & Takayasu Sakurai eds., 1st ed. 2001) (excerpts)
2025	RESERVED
2026	RESERVED
2027	Perrine Batude, et al., <i>3-D Sequential Integration: A Key Enabling Technology for Heterogeneous Co-Integration of New Function with CMOS</i> , IEEE J. on Emerging & Selected Topics in Circuits and Systems, Vol. 2, No. 4 (Dec. 2012)
2028	Deposition of Dr. Jack C. Lee, <i>Micron Tech., Inc. v. BeSang Inc.</i> , IPR2023-00900, EX2028 (Feb. 6, 2024)
2029	Declaration of Steven A. Przybylski
2030	CV of Steven A. Przybylski
2031	<i>Webster's New Universal Unabridged Dictionary</i> (Barnes & Noble Publ'g 2003) (excerpt)
2032	<i>Random House Webster's College Dictionary</i> (2d ed. 1997) (excerpt)
2033	Gary S. May, Ph.D. & Costas J. Spanos, Ph.D., <i>Fundamentals of Semiconductor Manufacturing and Process Control</i> (2006) (excerpts)
2034	RESERVED
2035	RESERVED
2036	RESERVED
2037	RESERVED
2038	RESERVED
2039	Transcript of Deposition of Dr. Carl Sechen (Feb. 27, 2024)
2040	RESERVED

Exhibit No.	Description
2041	Tetsuo Endoh, et al., <i>Novel Ultrahigh-Density Flash Memory With a Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell</i> , IEEE Transactions on Electron Devices, Vol. 50, No. 4 (Apr. 2003) [Micron Ex. 1022]
2042	Hiroshi Sakuraba, et al., <i>New Three-Dimensional High-Density Stacked-Surrounding Gate Transistor (S-SGT) Flash Memory Architecture Using Self-Aligned Interconnection Fabrication Technology without Photolithography Process for Tera-Bits and Beyond</i> , Japanese J. of Applied Physics, Vol. 43, No. 4B (2004) [Micron Ex. 1030]
2043	U.S. Patent No. 6,982,905 (Nguyen) [Micron Ex. 1012]
2044	G. Groeseneken, et al., Basics of Nonvolatile Semiconductor Memory Devices, in <i>Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices</i> (William D. Brown & Joe Brewer eds., 1997) [Micron Ex. 1009]
2045	Linden T. Harrison, <i>Current Sources & Voltage References</i> (2005) (excerpts)
2046	<i>The Electrical Engineering Handbook</i> (Wai-Kai Chen ed., 2005) (excerpts)
2047	[Not Filed Version of EX2024] Kiyoo Itoh, <i>VLSI Memory Chip Design</i> (Kiyoo Itoh & Takayasu Sakurai eds., 1st ed. 2001)
2048	[Not Filed Version of EX2033] Gary S. May, Ph.D. & Costas J. Spanos, Ph.D., <i>Fundamentals of Semiconductor Manufacturing and Process Control</i> (2006)
2049	[Not Filed Version of EX2045] Linden T. Harrison, <i>Current Sources & Voltage References</i> (2005)
2050	[Not Filed Version of EX2046] <i>The Electrical Engineering Handbook</i> (Wai-Kai Chen ed., 2005)
2051	RESERVED
2052	RESERVED
2053	Transcript of Deposition of Dr. Carl Sechen (July 10, 2024)

I. INTRODUCTION

Intel's Reply only confirms that the Petition has not met its burden to establish unpatentability. Intel returns with new arguments and twenty-one exhibits, including another expert declaration, trying to paper over the Petition's flaws. EX1037-1057.

Instead of establishing how the Petition met its burden, Intel's Reply attempts to salvage its mishmash of ten grounds by further explaining its claim construction positions and redoing its cross-referencing. Its Reply confirms what BeSang already told the Board—claim construction is not determinative of any ground in this IPR.

For Grounds 1A-1F, Intel effectively forfeits its Lee-only challenges in Grounds 1A-1B. The remaining Grounds 1C-1F collapse because Intel and its expert admit that Lee's Figure 25A is inoperable, and thus combining it with Kim or Aspar's stacking techniques simply would not work. Intel now renounces the Petition's motivations to combine, asserting that Lee itself taught stacking. If Lee really disclosed stacking, then the Petition would have had no reason to include Grounds 1C-1F touting Kim and Aspar's stacking methods in the first place. This belated effort to reinvent the Petition only shows the claims should be confirmed.

For Grounds 2A-2C, Johnson's "steering element" diode design did not teach the claimed transistors and Intel has no good answer for Johnson's teaching away.

Finally, Intel effectively surrenders on Ground 3.

The Board should confirm patentability of all challenged claims.

II. INTEL’S PETITION FAILS TO ARTICULATE OR SUPPORT AN UNPATENTABILITY GROUND

A. The Petition Did Not Present Its Grounds With Particularity

The Petition did not meet its burden to identify its grounds with particularity. 35 U.S.C. §312(a)(3). The Reply first presents a chart showing the claim constructions it intended for each ground. Paper 21 (“Reply”) at 4. Intel says the Petition “clearly described” the constructions it applied, which if true begs the question of why it needs the nearly full-page chart at all. *Id.*

Chart notwithstanding, Ground 1E never articulated the claim construction it applied. Pet. at 63; Paper 17 (“POR”) at 52. And Intel has no answer for Dr. Sechen’s admission he never offered an opinion under Intel’s construction for Ground 1E. POR at 52 (citing EX2039 at 24:2-17).

Ground 1D cross-references back to 1B/1C, Pet. at 55; POR at 35-36, and Ground 1F to 1B/1E, Pet. at 64; POR at 53-54. Intel claims its “claim construction arguments are straightforward” for Ground 1D, Reply at 22, but needing a chart and narrative clarifying “what the petition really meant” shows otherwise, *see* Reply at 4, 22; *Netflix v. DivX*, 84 F.4th 1371, 1377 (Fed. Cir. 2023).

Intel’s own chart plainly shows the Petition’s Grounds 1D/1F cross-references resulted in an irreconcilable tangle of inconsistent claim constructions:

Ground	Claim(s)	Reference(s)	“stackable add-on layer” (all Challenged Claims)	“SOI pillar” (claims 14-17)	Source	
1A	13-17	Lee	PO	PO ¹	Pet., 16	
1B	16-17	Lee, Endoh	PO	PO	Pet., 41-42	Ground 1D
1C	13-17	Lee, Kim	Intel ²	PO	Pet., 50	
1D	16-17	Lee, Kim, Endoh	Intel	PO	Pet., 55	Ground 1F
1E	13-17	Lee, Aspar	Intel	Intel	Pet., 55	
1F	16-17	Lee, Aspar, Endoh	Intel	Intel	Pet., 64	

Reply at 4 (excerpted, annotated).

Further, Intel has no answer for how Grounds 1D/1F satisfied all the requirements of Claims 16-17, including from independent Claim 13. Reply at 22-23; POR at 35-38, 53-54.

III. CLAIM CONSTRUCTION

A. “stackable add-on layer” / “the stackable add-on layer [is]/[being] bonded”

The construction of “stackable add-on-layer” is unnecessary to resolve this IPR and confirm patentability of the claims. POR at 15. Trying to sort out its muddled claim constructions, Intel concedes the Petition may be decided

independent of the construction of “stackable add-on layer.” Reply at 4 n.2. Intel’s reply chart asserting that Grounds 1C-1F/2B-2C purportedly applied the “Intel” construction for “stackable add-on layer,” says these same grounds to “apply also to PO’s apparent construction” of the term. *Id.* While acknowledging the Board provided a different construction than the Petition, Intel urges “the Board need not resolve the difference” between them. Reply at 1; *but see* Reply at 2 (also Intel: “the Board should construe the term”).

Now that Intel apparently agrees the construction of this term is no longer needed, the Board need not construe it, *Realtime Data v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019), and Intel’s cited cases do not mandate otherwise, Reply at 2 (citing *Sotera v. Masimo*, IPR2020-00967, Paper 43 at 18 (P.T.A.B. Nov. 19, 2021); *AC Techs. v. Amazon.com*, 912 F.3d 1358, 1364-65 (Fed. Cir. 2019)).

The Board already found Petitioner failed to meet its burden for Grounds 1A/1C/2A under Intel’s constructions. Paper 12 (“I.D.”) at 28-29, 37-38, 46. Intel argues it’s “not aware of any authority” that the Board may disregard grounds based on constructions Intel refuses to endorse, Reply at 2, but has no answer for BeSang’s cited authority that Petition hasn’t met its burden based on constructions Intel repudiates, POR at 31-32 (citing *Hologic* and *Ebates*).

B. “SOI Pillar”

The construction of “SOI pillar” is not disputed and therefore required. POR at 16; *Realtime Data*, 912 F.3d at 1375. The Reply identifies no ground turning this construction, Reply at 3, and Intel concedes “Claims 14-17 are unpatentable regardless of whether the Board adopts Intel’s or PO’s ‘SOI pillar’ construction,” Reply at 14, 4 n.1.

If the Board wishes to address the construction of “SOI pillar,” BeSang’s should be adopted. POR at 16-18. Intel agrees “SOI” means “silicon-on-insulator.” Pet. at 4. Intel argues “the ’702 patent does not limit ‘pillar’ to any particular shape,” but the plain meaning of “pillar,” patent figures, and description of the pillar’s aspect ratio show otherwise. Reply at 3; POR at 16-17 (citing EX1001, Figs. 4, 20, 27, 8:5-10); EX2029 ¶¶90-92. Intel concedes that: “Figures that are not drawn to scale may be relied upon to disclose qualitative relationships between measured quantities.” Reply at 15 (quoting *Kingsford Prods. v. Creative Spark*, IPR2016-01831, 2018 WL 1230574, at *12 (P.T.A.B. Mar. 9, 2018)). Intel has no answer for its expert’s inability to provide a plain and ordinary meaning of “pillar.” See Reply at 3; POR at 18 (citing EX2039 at 17:14-22:2). Its citation to column 6 addresses an “unpatterned, SOI layer,” not the claimed “memory cell[s]” on an “SOI pillar.” Reply at 3 (citing EX1001 at 6:26-29); EX1001 at 6:23-25.

IV. THE PETITION FAILED TO ESTABLISH UNPATENTABILITY IN GROUNDS 1A-1F

A. The Reply Effectively Forfeits Grounds 1A-1B

Intel doesn't earnestly dispute that it failed to meet its burden to show obviousness over Lee (and Endoh) in Grounds 1A-1B. It barely mentions either, Reply at 5, 21, and does not separately address the four defects BeSang pointed out, POR at 55-56. The claims should be sustained over Grounds 1A-1B.

B. Intel Does Not Meet Its Burden To Show A Motivation To Combine Lee With Kim Or Aspar (Grounds 1C-1F)

Intel's Petition presented four separate combinations of Lee with Kim or Aspar (and Endoh) in four grounds under different claim constructions. Pet. at 3; Reply at 4. On reply, Intel aggregates them into a single discussion in an effort to mix-and-match unpatentability theories. Reply at 5-22. Not only is mixing grounds improper, but it only confirms that Intel failed to show a motivation to combine in its Petition. *Uber v. Surgetech*, IPR2023-00738, 2023 WL 6976089, at *10 (P.T.A.B. Oct. 23, 2023) ("Petitioner does not separately discuss each individual ground" which "obscures the specific arguments advanced and the claims challenged in each individual ground.").

Intel compounds its problematic approach by applying an incorrect legal standard. It argues it met its burden to show a motivation to combine because it "need only" show that Kim/Aspar's stacking are "suitable options." Reply at 6

(quoting *Intel v. PACT XPP*, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023)). That is not the law. “It does not suffice to meet the motivation to combine requirement to recognize that two alternative[s]... were both known in the art.” *Virtek Vision v. Assembly Guidance*, 97 F.4th 882, 886 (Fed. Cir. 2024). *PACT* is inapposite because it was undisputed that the secondary reference would solve a problem in the primary reference. 61 F.4th at 1380-81. Here Intel acknowledges that issue is hotly disputed: “PO contends the combinations would not have improved Lee.” Reply at 6.

The Reply’s eleventh-hour rationales for combining Lee with Kim or Aspar are unsupported, and the claims should be confirmed under each of Grounds 1C-1F.

1. The Reply Admits Its Original Combinations Were Inoperable (Grounds 1C-1F)

Because the Reply admits that Lee’s Figure 25A is inoperable, its original combinations of Figure 25A with Kim or Aspar’s stacking techniques collapse.

Intel does not dispute the key facts that Lee’s fabrication process for its memory cell array has no clean partition point, that its control gates are shared between two levels, that one level of the array is not complete until the next level is built, or that its expert did not appreciate any of this. Reply at 11-12; POR at 21-26; EX1007 ¶¶163-69.

Intel and its expert now admit that Lee’s Figure 25A is inoperable, with Dr.

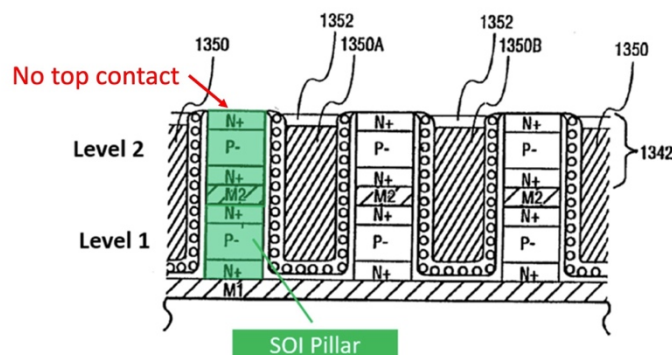


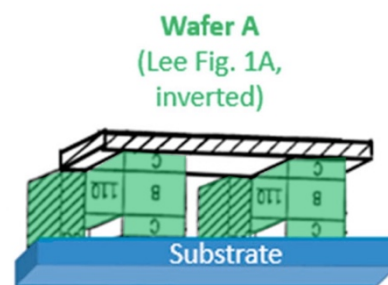
FIG. 25A

Sechen admitting that because Figure 25A is missing the top contact (left, annotated), no current can flow through the top NPN structure; thus, that memory cell “could not store or retrieve a

charge.” EX2053 at 45:7-22; EX1037 ¶38; Reply at 12. This entirely undoes Intel’s combinations in Grounds 1C-1F. *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984) (no motivation to modify a device by making it “inoperable for its intended purpose”).

The Reply suggests further modifying the Petition’s Lee/Kim and Lee/Aspar combinations to make them operable by “form[ing] more even memory levels.” Reply at 12. That is a new combination the Petition never proposed. Pet. at 52, 59-60. The Board cannot entertain a new combination now, *Juniper Networks v. Swarm Tech.*, IPR2021-01445, Paper 64 at 12-14 (P.T.A.B. Apr. 20, 2023), and Intel never explains exactly how this new combination would work, Reply at 12. Switching things up on reply concedes the Petition failed to meet its burden for Grounds 1C-1F.

Finally, Intel incorrectly asserts that the “interleaved levels” defect does not pertain to Lee’s individual memory cells in Figures 1A-1B, 2, or 7. Reply at 11. The Petition did not rely on simple memory cells, rather its combination proposed “wafer bond *level* 3104” to layer 3102, using “any of the memory structures in Figures 1A-1B, 2, 7, or 25A.” Pet. at 52 (emphasis added). Lee teaches those pillar memory cell embodiments are fabricated using the process described in Figures 13-28. EX1007 ¶147 (“A method of integrating the pillar memory device of the present invention into a multilevel array” starts with “FIG. 13”), ¶¶147-70; *see also id.* ¶¶38-46 (Figs. 1A-1B, 2, 7 each show a “pillar memory”). Indeed, as shown at right, the Petition depicts *two* Fig. 1A cells on level 3104 in its combination. Pet. at 52 (excerpted, annotated).



2. The Reply Abandons The Petition’s Original Rationale For Combining Lee With Kim/Aspar

The Reply confirms that the Petition’s original pretext for combining Lee with Kim or Aspar was error. Reply at 6-7. The Petition asserted that one of skill would have looked to either Kim or Aspar because “Lee does not clearly describe how the bottom level 3104 of array 3101 is formed.” Pet. at 51, 56. But Lee taught forming that level using deposition, EX1007 ¶¶107, 122, and Intel’s motivation gained no traction with BeSang’s expert, EX2029 ¶¶115-16, or the Board, I.D. at 35. Even

Intel’s Petition could not maintain the pretense, Pet. at 51 (citing EX1007 ¶107), and Intel’s own expert could not defend it, EX2039 at 88:2-89:6. Intel now walks away from the Petition’s pretext while weakly protesting that “Lee does not mandate using deposition” for Figure 35. Reply at 6.

Instead, the Reply pivots to a brand-new motivation: “Lee discloses stacking.” Reply at 7. This is the opposite of what the Petition argued. Pet. at 52-53. The Petition exclusively argued Lee taught “monolithic deposition,” Pet. at 53; Reply at 6 (“Lee uses ‘monolithic’ to refer to depositing one array layer on another.”), and its original motivation was that one of skill “would have been motivated to apply Kim’s wafer bonding teachings to implement Lee’s Figure 35 memory device as a non-monolithic one.” Pet. at 52.

Intel’s abandonment of the Petition’s motivation to combine concedes it failed to sustain its burden. *Wasica Fin. v. Cont’l Auto.*, 853 F.3d 1272, 1286 (Fed. Cir. 2017) (affirming patentability where petitioner’s “subsequent arguments amount to an entirely new theory of *prima facie* obviousness absent from the petition”); *Netflix v. Avago Techs.*, IPR2021-00542, 2022 WL 4111185, at *15 (P.T.A.B. Sept. 6, 2022) (Petitioner cannot prevail where its reply arguments “amount to a new theory distinct from the... theories offered in the Petition.”). The Board may freely disregard Intel’s effort to belatedly supply a different motivation to combine on

reply. *Intelligent Bio-Sys. v. Illumina Cambridge*, 821 F.3d 1359, 1369-70 (Fed. Cir. 2016); 37 C.F.R. §42.23(b).

Even if considered, Intel’s brand-new motivation is unsupported. Intel argues that “Lee discloses stacking” and “contemplates” using Figure 35 “with SOI technology, including ‘wafer bonding.’” Reply at 7 (citing EX1007 ¶¶113, 115, 117, 208, 211-12). Lee does not. *See id.* Dr. Sechen concedes that Lee’s paragraphs 113, 115, and 117 do not address wafer bonding. EX2053 at 34:13-35:7. The other paragraphs are not about Lee’s Figure 35 at all but about Figure 37-44 embodiments the Petition never discussed, EX1007 ¶¶207; Pet. at 51-54, 56-60, and Dr. Sechen admitted he never referred to in his opening declaration, EX2053 at 39:7-17. Lee’s paragraph 208 mentions “wafer bonding,” but only addresses Figure 37’s TFT substrate containing the peripheral or driver circuitry. EX1007 ¶¶208; EX2053 at 35:11-37:16.

The Reply asserts that “Lee teaches potential implementations involving SOI technology and wafer bonding ‘increase array density and decrease die size and cost.’” Reply at 8 (quoting EX1007 ¶¶204, 207-12). But Lee never links them. Lee’s teaching of an “ultra dense matrix array” with “an increased density and lower cost” was achieved by “arrang[ing] the devices in a monolithic three dimensional array,” not through non-monolithic stacking. EX1007 ¶¶106-07. Lee’s paragraph 204 refers to the aligned cell structure, but never mentions SOI technology or wafer

bonding. EX1007 ¶204. Dr. Sechen could not seriously defend his parroting opinion either. EX2053 at 41:1-43:12. Paragraphs 207-212 only discuss Lee’s Figure 37, not increasing density or decreasing cost in Lee’s array. *See* EX1007 ¶¶207-12.

3. Intel Has Not Sustained Its Quality Control And Less Waste Arguments

On reply, Intel does not salvage its “more efficient quality control” argument for the Kim or Aspar grounds. Pet. at 53-54, 61-62; Reply at 8-9. It does not dispute that none of Lee, Kim, or Aspar teach that wafer bonding would improve quality control. POR at 27-29, 49; EX2029 ¶¶125-34, 145. Nor does it dispute its own evidence showing that semiconductor fabs already routinely test the monolithic devices they fabricate. POR at 27-28 (citing EX1014, EX1016).

The Board requested data showing that Kim and Aspar’s stacking would improve quality compared to deposition, I.D. at 35-36, but Intel has nothing, saying it is “not necessary,” Reply at 8. That is plainly insufficient coming from the party that has a burden to meet. *In re Magnum Oil Tools*, 829 F.3d 1364, 1375 (Fed. Cir. 2016) (“[T]he burden of persuasion is on the petitioner... and that burden never shifts to the patentee.”).

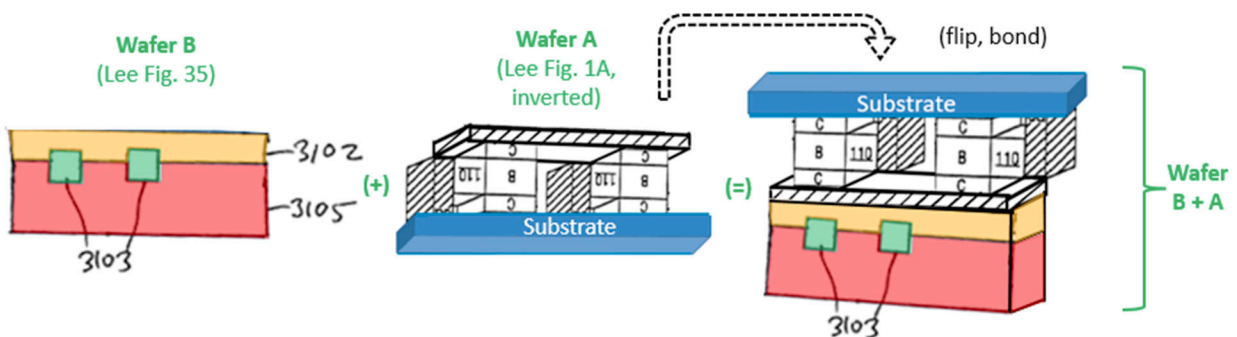
On reply, Intel claims that one of skill could have tested “doping concentration, thickness, and uniformity” in its stacked Lee-Aspar combination. Reply at 9-10 (citing EX1041, EX1043, EX1047, EX1057 and Sechen). Intel’s cited

exhibits do not support its claim and in fact show the opposite. EX1041 at 228 (no mention of testing, or stacking facilitating such testing); EX1043 at 10-11 (same). Worse, EX1047 and EX1057 address testing deposited (not stacked) wafers, and only underscore that Intel’s combination shows no improvement to the routine testing of semiconductor fabs on monolithic devices. EX1047 at 295 (describing “testbed system” for “epitaxially deposited silicon films”); EX1057 at 1:5-8, 1:33-34 (describing “in-line testing of semiconductor wafers during integrated circuit fabrication” for “the various processing steps t[he] silicon wafer is subjected”). The Reply demonstrates that the Petition’s improved quality control was only talk. *Icon Health v. Strava*, 849 F.3d 1034, 1043 (Fed. Cir. 2017) (attorney argument given no weight).

Intel acknowledges that one of skill knew that quality control focused on testing the “memory cells.” Pet. at 54 (Intel: “[A] POSITA would have recognized that quality control can be performed on the memory cells (e.g. testing for shorts).”); EX2029 ¶145; Reply at 8 (Intel: “Fung teaches testing **structures** before bonding.” (emphasis added)). Intel concedes “Aspar’s process transferred an unpatterned layer or layer stack” with no memory cells and identifies no structures to test. Reply at 9-10. Intel and its expert have no answer for their admissions that the memory cells are fabricated later, after Aspar’s bonding and cleaving. Pet. at 60; EX2039 at 90:21-

91:15; POR at 49; EX2029 ¶145. Intel has not met its burden on Grounds 1E-1F either.

The Reply also effectively abandons its less waste argument for Kim and Aspar. Reply at 8-9. It does not dispute that Aspar burning wafers at 1100°C makes more trash. *Id.*; POR at 49-50; EX2029 ¶145. Intel also does not dispute that “Kim generated waste by thinning the wafer,” but argues it was “optional.” Reply at 9. Kim’s thinning would not be optional in Intel’s fanciful combination. As shown in Intel’s conceptual drawing shows the top **blue substrate** (below right) would have to be ground off to form Lee’s top contact in Intel’s proposed combination:



Pet. at 52; EX1008 ¶25. Wasting an entire wafer for every device made is much more extravagant than discarding an individual die with an error. EX2029 ¶¶130-32; EX1014 at 841; POR at 29.

4. The Reply’s New “Process Optimization” Rationale Should Also Be Rejected

On reply, Intel tries to craft a new motivation to combine Lee with Kim or Aspar based on a conclusory sentence about “process optimization.” Reply at 10.

This motivation appears nowhere in the Petition and can be ignored. *Illumina*, 821 F.3d at 1369-70; *Fantasia Trading v. CogniPower*, IPR2021-00067, 2022 WL 1613101, at *12 (P.T.A.B. May 11, 2022) (“[I]t is too late to raise a new motivation to combine with the Reply.”). Even if considered, Intel’s assertion that “Aspar’s process would have benefited [sic] Lee by adding monocrystalline silicon,” Reply at 10, provides no motivation to look to Kim or Aspar’s stacking. Dr. Sechen even acknowledges that monocrystalline silicon could be added “using epitaxy.” EX1037 ¶24.

5. No Motivation For Applying Aspar’s High-Temperature Annealing To Lee (Grounds 1E-1F)

Intel’s only answer for Aspar’s 1100°C annealing step is to claim that “Aspar describes no such annealing step.” Reply at 12 (citing EX1037 ¶29 (Sechen: ditto)). Ignoring a problem does not make it go away. Dr. Sechen relied on this 1100°C annealing step in his declaration. EX1003 ¶46 (“Annealing 1100°C”). Intel concedes that its own “Wolf textbooks” (EX1014-EX1015) Intel relied on to support Grounds 1E-1F teach Aspar’s Smart-Cut as having an 1100°C annealing step, Reply at 12, and Dr. Sechen admits that Exhibit 1015 described the “same process” used in Aspar. EX2039 at 118:10-119:2.

Intel’s effort to disavow its own evidence and expert testimony exceeds the proper scope of reply, and shows the Petition failed to meet its burden. 37 C.F.R. §42.23(b); *Illumina*, 821 F.3d at 1369-70.

Intel also attempts to rely on the ’702 Patent and its ’941 parent application, but that only confirms the Petition’s use of “improper hindsight.” *New U Life v. Axxess Global*, IPR2019-01141, 2020 WL 6260644, at *14 (P.T.A.B. Oct. 23, 2020); *SPTS Techs. v. Plasma-Therm*, IPR2017-01674, 2019 WL 1154156, at *3 (P.T.A.B. Mar. 7, 2019). And unlike Aspar’s Smart-Cut and Intel’s proposed Aspar combinations, the ’702 Patent explained how to build its architecture with low-temperature processing. EX1001 at 7:15-35.

C. The Petition Established No Reasonable Expectation Of Success For Grounds 1C-1F

The Reply asserts reasonable expectation of success, attempting to sidestep the “thin silicon layer Aspar’s process leaves behind” by claiming BeSang “misunderstands” the combination, then pretending the thin layer is instead the “N+/P-/N+ doped stack.” Reply at 14.

There is no misunderstanding here; the mistake is that the Petition’s Lee/Aspar combination is inoperable. *See* Pet. at 56-60. As shown below, Aspar teaches leaving a thin layer of silicon on top of the oxide layers and Intel’s expert confirmed it:

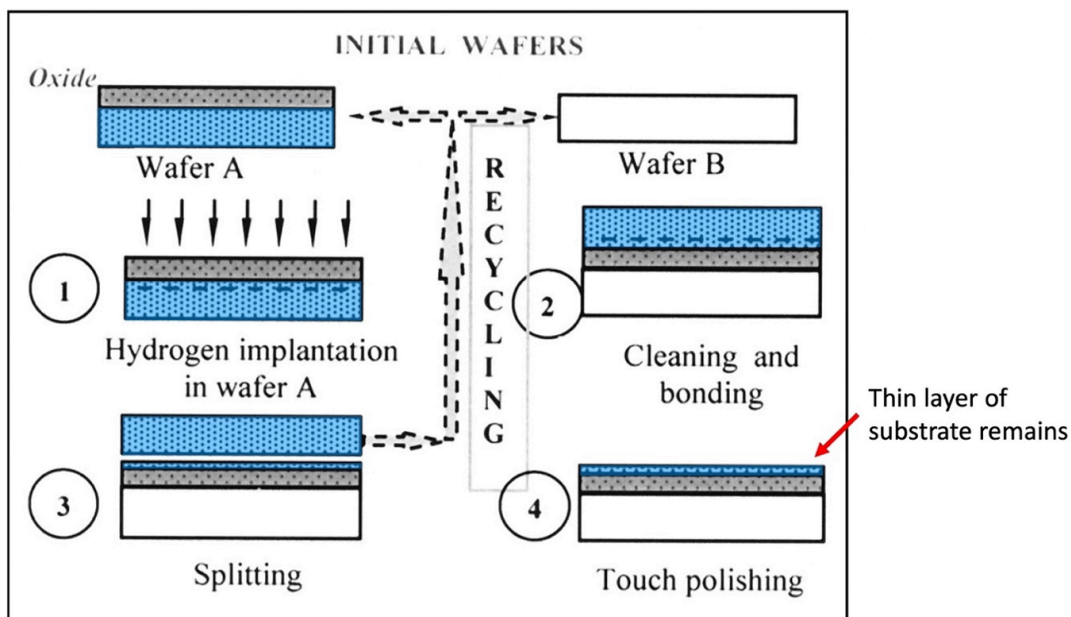
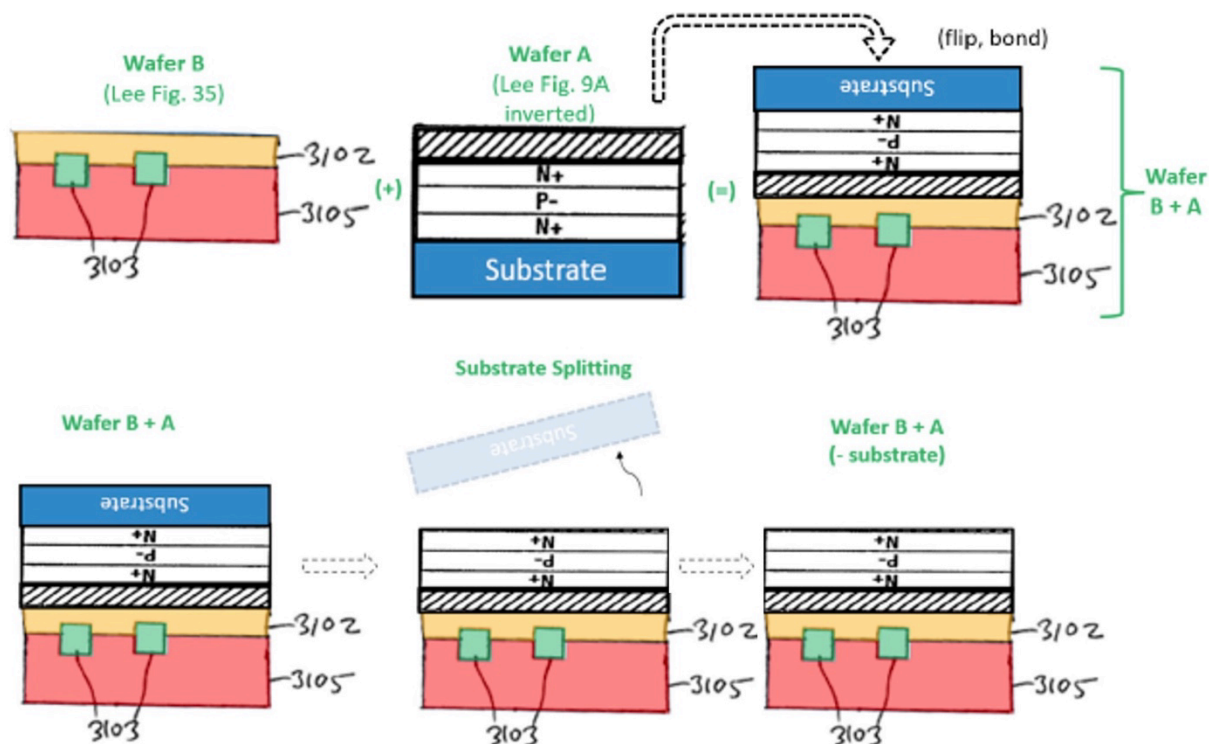


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

EX1009 at Fig 1 (annotated); POR at 50-51; EX2039 at 68:19-73:21; EX2029 ¶155.

The Petition proposed replacing Aspar's Wafer A with a reimagined version of Lee's Figure 9A, building an NPN stack on a substrate:



Pet. at 59-60. Intel’s combinations show the silicon layer from the **blue substrate** (above left) is *above* the NPN stack from Lee. *Compare* EX1009 at Fig. 1, with Pet. at 59-60. When Aspar splits off the substrate from the top of the NPN stack, there is no dispute it leaves a thin layer of the substrate behind. EX1009 at Fig. 1; EX2039 at 68:19-73:21, EX2029 ¶¶146-47, 153-56. Intel does not dispute that this thin layer of silicon would obstruct forming a metal contact atop the NPN stack, Reply at 14; EX2029 ¶¶155-56, and provided no explanation how to avoid that thin layer, *see* Pet. at 59-60; POR at 50-51. Claims 13-17 should be confirmed patentable because Intel has not sustained its burden to show one of skill could have combined Lee/Aspar in the way the Petition said.

D. Claims 16-17 Should Be Confirmed Because Lee’s Memory Cells Are Not “Serially Connected Together” (Grounds 1A/1C/1E)

The experts agree that Lee teaches an NOR array with memory cells connected in parallel. EX2039 at 53:3-22, 59:17-60:7; EX2029 ¶¶98-100, 108; POR at 33-35. The Reply tries to downplay Dr. Sechen’s testimony on this point but does not deny any of this. Reply at 16-17. Instead, Intel doubles down on the Petition’s error, now arguing Figure 25A’s memory cells in the two levels are momentarily “serially connected” before the top contact is formed. Reply at 17.

Even if considered, relying on an “inoperable” combination still does not satisfy Intel’s burden to show obviousness. *In re Gordon*, 733 F.2d at 902. There is no dispute that Figure 25A shows an “intermediate step” in Lee’s fabrication of the memory array and is not an “operational device.” Reply at 12, 17; EX1007 ¶¶165-66. Rather than being serially connected, Dr. Sechen confirmed that without the top contact, no current can flow through the top NPN structure and it “could not store or retrieve a charge,” rendering it not a “memory cell.” EX2053 at 45:7-22. After the top contact is added, Lee’s memory devices are connected in parallel. EX2029 ¶¶98-100.

Even if the Reply’s legally and technically flawed argument is credited, at no point are Lee’s Levels 1 and 2 NPN structures in Figure 25A serially connected “memory cells.”

**E. Claims 16-17 Should Be Confirmed Over Lee, Kim Or Aspar,
And Endoh (Grounds 1D/1F)**

The Reply devotes almost 20% of its briefing to an effort to provide new combinations of Lee and Endoh in Grounds 1B/1D/1F in place of the scant, cross-referenced, and internally inconsistent grounds in the Petition. *Compare* Pet. at 41-42, 55, 64, *with* Reply at 17-22. This is plainly insufficient to explain how or why one of skill would have transformed Lee’s NOR array into a less-dense NAND structure. POR at 39-43, 55-56. Intel attempting to lay out its *prima facie* obviousness case on reply only confirms the Petition did not, and it is too late to argue *prima facie* obviousness now. *Dexcom v. WaveForm Techs.*, IPR2016-01680, 2018 WL 1137089, at *13 (P.T.A.B. Feb. 28, 2018) (“prima facie case of unpatentability may not be introduced for the first time in the reply brief”). The Board may soundly disregard these new grounds. *Id.*

Even if considered, Intel’s new motivation to combine does not sustain its burden. *See* Reply at 17-22; POR at 39-43, 55-56.

First, Intel argued that one of skill would be motivated to combine Lee and Endoh to “further Lee’s stated goals of increasing device density.” Pet. at 47. Dr. Sechen concedes that Lee teaches “four memory cells in each pillar.” EX2053 at 46:20-47:3; *see also* EX1007 ¶166. Replacing Lee’s interleaved, four-memory-cell pillar memory with Endoh’s single-memory cell would indisputably result in up to

a four-fold reduction in density. POR at 39-40; EX2029 ¶¶59, 106. Intel provides no credible reason for doing this. Pet. at 47-48; Reply at 17-22.

Second, the Petition never explains why one of skill would have been motivated to replace Lee’s NOR memory device with the distinct architecture of a NAND device. Pet. at 42-48, 55, 64. Intel weakly offers it “was well within POSITAs’ knowledge,” Reply at 22, but that is far-fetched considering its own expert struggled to understand Lee, *e.g.*, EX2039 at 45:18-48:5; POR at 30, and the fundamental differences between Lee and Endoh, EX2029 ¶¶107-11.

Intel claims that Lee’s Figure 25A is not part of its combination, Reply at 21-22, but that carries little weight both with Intel backpedaling from its own citation to Figure 25A in the Petition, Reply at 22 n.5; Pet. at 48, 64, and the Petition never explaining its combinations for Grounds 1D/1F, Pet. at 55, 64.

Finally, *Magnum Oil* only supports finding that Intel’s cross-referencing to a separate prior art combination has not met its burden. 829 F.3d at 1379 (referencing Alpha/Cockrell/Kristansen inadequate to show obviousness over Lehr/Cockrell/Kristansen); Reply at 23; *see also* POR at 35-37 (Ground 1D), 53-54 (Ground 1F).

**V. THE PETITION FAILED TO ESTABLISH UNPATENTABILITY IN
GROUNDS 2A-2C**

A. Johnson Did Not Render Claim 13 Obvious (Grounds 2A-2C)

1. Johnson Did Not Teach The Claimed Transistors

There is no dispute that Johnson’s specific field-programmable memory design used 2-terminal steering elements. Reply at 24; POR at 57-61. Intel also does not dispute that Johnson’s sole mention in column 7 of a “JFET[] or ‘MOSFET’ [is] as a steering element,” which Intel admits is a diode. Reply at 24 (Johnson’s JFET/MOSFET are “diode-connected transistors”). Intel is stuck with Johnson’s column 7 teaching, now conceding its Petition never asserted one of skill would have modified Johnson’s 2-terminal steering element to include “different” transistors. *Id.*

Intel’s new exhibits only confirm the distinction between using a JFET/MOSFET as a transistor or as a diode. *See, e.g.*, EX1051 at 272 (referring to “diode-connected devices”); EX1052 at 5:44-46 (“the gate and drain of the transistor are shorted together, thereby **forming a MOS diode**” (emphasis added)); EX1053 at 1:17-19 (“Conventional Metal Oxide Semiconductor (MOS) type transistors can be **used as a diode** by connecting their gate to their drain.” (emphasis added)); EX2045 at 180 (“JFETs can be used to create *ultra-low-leakage* diodes”).

Because Johnson only taught diode-connected steering elements in column 7, it did not teach or suggest “memory cells having at least one transistor.” EX1001 at 12:33-34.

2. Johnson Taught Away From Transistor Memory Cells

The Reply admits Johnson criticized transistor-based memories. Reply at 25. It claims Johnson solved the problem of transistors “built in planar the substrate [sic],” by using “steering elements ‘not built into planar substrates.’” *Id.* (quoting EX1010 at 2:6-36, 5:41-48).

Intel gets it half right, admitting that Johnson’s 2-terminal steering device solved the problem with conventional transistor-based memories, but omitting that Johnson’s 2-terminal design did not allow for 3-terminal source/gate/drain transistor circuitry. EX1010 at 2:6-20. Intel cannot selectively seize on isolated words in column 7 while ignoring Johnson’s disclosures teaching away from the claimed invention. *Panduit v. Dennison Mfg.*, 810 F.2d 1561, 1568 (Fed. Cir. 1987) (A reference must be considered for all it teaches, “including portions that would lead away from the invention.”); POR at 61-62.

Johnson taught away from conventional transistor memories in favor of its diode design. POR at 57-62; EX2029 ¶¶167-89. Johnson criticized existing field-programmable memories for requiring separate transistors for read and write operations, resulting in lower density. EX1010 at 2:6-20. Johnson traded the

conventional 3-terminal design for a 2-terminal diode design with only an “input terminal” and an “output terminal.” *Id.* at 5:43-44. Johnson did not teach providing source/gate/drain circuitry in its self-aligned pillar to accommodate a 3-terminal transistor. EX1010 at Fig. 6, 12:1-41; EX2029 ¶¶187-88. Indeed, Dr. Sechen’s new declaration admits that Johnson’s design provided “no supporting circuitry” for the transistors. EX1037 ¶55. Instead, Johnson criticized the “contact” and “gate patterning” for these transistor-based “conventional nonvolatile memory cells” because they required “at least five photolithographic masking steps” and careful alignment. EX1010 at 2:38-52; EX2029 ¶180.

3. Johnson’s Disclosure Did Not Enable A 3-Terminal Design

Intel does not dispute that one of skill would not have been motivated to modify Johnson’s 2-terminal diode steering element into a 3-terminal design. Reply at 25-26; POR at 62-65. Instead, Intel disputes that Johnson enables the use of transistors. Reply at 25 (citing EX1037 ¶58); POR at 60-64. It asserts that Johnson’s MOSFET is presumed enabled, or that Johnson need not be self-enabled because it asserts Johnson in combination with other references. Reply at 25 (citing *Amgen v. Hoechst Marion*, 314 F.3d 1313, 1355 (Fed. Cir. 2003); *Raytheon v. GE*, 993 F.3d 1374, 1380 (Fed. Cir. 2021)). On the contrary, “to prevail... Petitioner must show that [the prior art] enables the portions of its disclosure relied upon in Petitioner’s

mapping... to the challenged claims.” *Kinaxis v. Blue Yonder*, IPR2021-01302, Paper 38 at 19 (P.T.A.B. Feb. 6, 2023).

Intel’s cited authority recognized “a non-enabled disclosure cannot be anticipatory (because it is not truly prior art).” *Amgen*, 314 F.3d at 1354. Because here Intel asserts that “Johnson expressly discloses” the claimed transistor in 13[d], that alleged anticipatory disclosure must be enabled. *See id.*; Pet. at 73; Reply at 24 (“Johnson expressly discloses” using a JFET or MOSFET), 25 (“Johnson expressly teaches memory cells with transistors.”). Dr. Przybylski provided extensive explanation why Johnson’s disclosed “transistor” embodiments would not work as “steering elements” or could not be constructed in his device due to use of self-alignment and density. EX2029 ¶¶171-89.

Intel asserts that Johnson also discloses “photomasking” rather than self-alignment, Reply at 26, but does not explain how to incorporate JFET or MOSFET gates using that “photomasking,” which a skilled artisan would not know, EX2029 ¶¶184-89. Its resort to adding Lee’s “vertical transistors” to Ground 1 confirms that its Ground 2 combinations are not enabled and does not explain how such structures could be used in Johnson’s design when Dr. Przybylski explained that they could not. Reply at 26 (citing EX1007); *Juniper*, IPR2021-01445, Paper 64 at 12-14; EX2029 ¶¶187-89.

Intel also points to nothing in Kim or Aspar showing how to implement a transistor in Johnson’s simplified diode design. *Raytheon*, 993 F.3d at 1381. And Intel provides nothing showing that Johnson’s “steering elements” would operate as transistors. Reply at 22; EX2029 ¶¶178, 186, 189; POR at 60-64.

Because Johnson is not enabled, Claim 13 should be confirmed over Grounds 2A-2C. *Raytheon*, 993 F.3d at 1382; *Kinaxis*, IPR2021-01302, Paper 38 at 22-24 (“Eicher provides no guidance regarding how a skilled artisan can implement Eicher’s system” and no showing that one of skill could “modify Eicher to arrive at the claimed invention.”).

**B. No Motivation For Combining Johnson With Kim Or Aspar
(Grounds 2B-2C)**

On reply, Intel concedes its arguments for a motivation to combine Johnson with Kim or Aspar are largely the same as for the Lee grounds. Reply at 26-27. Thus, Intel’s motivation fails for the same reasons previously discussed. *Supra* §§IV.A-IV.C.

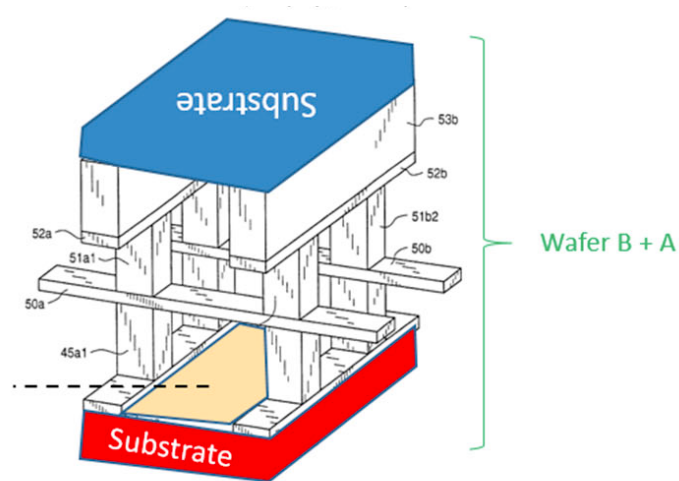
Its additional arguments also withstand no scrutiny:

- Intel does not seriously defend the Petition’s quality control or less waste rationales. Reply at 27; POR at 67-68, 73; Pet. at 76, 81. Intel and Dr. Sechen do not address his admission that Johnson disclosed no access points for Intel’s proposed testing. EX2039 at 107:18-112:4; Reply at 27; EX1037 ¶62.

They provide nothing showing how combining Johnson and Kim/Aspar would improve the routine testing they acknowledge semiconductor fabs already provide, Reply at 27, or what one of skill would test in Aspar's unpatterned stack, EX2029 ¶¶197, 202.

- Intel insists “Johnson’s self-alignment techniques can still be used” with Aspar’s stacking but has not identified why or how exactly one of skill would do so. Reply at 27-28. It makes a similar argument for Johnson/Kim. Reply at 28. Intel never explains how Johnson’s self-aligned deposition technique would (1) be replicated using stacking, (2) account for Johnson’s tight alignment requirements, or (3) avoid increasing costs and lowering yields. Reply at 27-28; POR at 65-69, 70-72; EX2029 ¶¶192-97, 204. Intel does not dispute that its expert needed to modify the Petition’s Johnson/Kim ground to try to accomplish the combination. Reply at 28; POR at 69; EX2039 at 105:14-107:17. Intel’s inability to defend its combinations only confirms its combinations are outside the abilities of one of skill. EX2029 ¶¶193-96, 199-201.

- Intel concedes the Petition’s Johnson/Kim combination leaves strips 53a-53b without purpose, increasing cost and lowering yield. Reply at 28; POR at 68-69; EX2029 ¶193. Instead, Intel tries to modify the ground by speculating that one of skill “would have recognized Johnson’s strips would be useful for forming additional memory layers,” Reply at 28; EX1037 ¶65, yet the Petition shows no layers beyond strips 53a-53b (excerpted, right), Pet. at 74-75.



Intel fails to sustain its burden on motivation to combine.

VI. THE PETITION FAILED TO ESTABLISH UNPATENTABILITY IN GROUND 3

The Reply's lone paragraph addressing Ground 3 shows Intel effectively forfeits it. Reply at 28-29. Intel has no answer for the fact that Park's memory cells

are electrically connected, sharing **plate electrode 66** and **gate electrode 77**

(annotated at right). *Id.*; POR at 76-77;

EX1011 at 5:49-54, 5:41-42, Fig. 9;

EX2029 ¶¶209-11. It continues to insist

that electrical separation is “necessary for proper operation,” Reply at 29, but never

addresses Park's configuration showing

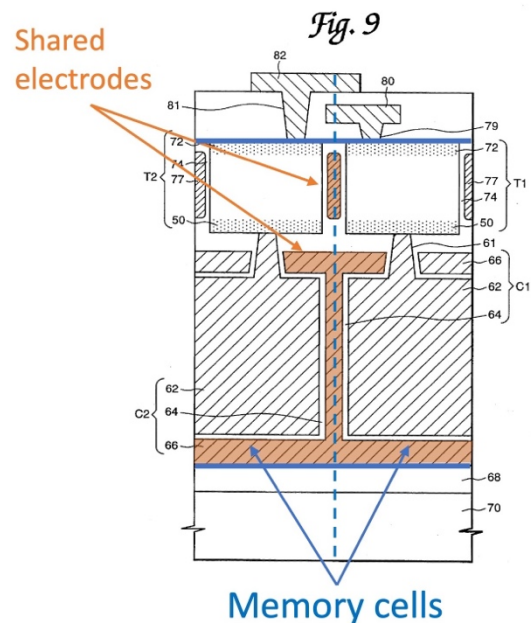
that instead of separating the two memory cells, the dielectric 64 forms an integral part of the capacitor of each memory cell, *see* POR at 76-78; EX2029 ¶210. Intel

also does not dispute Figure 1 of the '702 Patent depicts “memory cells separated from each other by dielectric material.” Reply at 29. Unasserted Claim 1 should be

confirmed over Park and Kim.

VII. CONCLUSION

BeSang respectfully requests the Board confirm patentability of the challenged claims.



Intel Corporation v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00991

ARMOND WILSON LLP

Dated: July 17, 2024

By: /Michelle E. Armond/
Michelle E. Armond (Reg. No. 53,954)
Douglas R. Wilson (Reg. No. 54,542)
Joseph Li (Reg. No. 74,998)
Yue Han (Reg. No. 80,950)
Attorneys for BeSang Inc.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. §42.24(d), the undersigned certifies that foregoing **PATENT OWNER’S SUR-REPLY**, exclusive of the parts exempted as provided in 37 C.F.R. §42.24, contains 5,587 words and therefore complies with the type-volume limitations of 37 C.F.R. §42.24.

ARMOND WILSON LLP

Dated: July 17, 2024

By: /Michelle E. Armond/
Michelle E. Armond (Reg. No. 53,954)
Douglas R. Wilson (Reg. No. 54,542)
Joseph Li (Reg. No. 74,998)
Yue Han (Reg. No. 80,950)
Attorneys for BeSang Inc.

CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a true copy of the foregoing **PATENT OWNER’S SUR-REPLY** and **EXHIBIT 2053** are being served electronically on July 17, 2024 to the following counsel for Petitioner to the following email addresses:

Jessica Kaiser
kaiser-ptab@perkinscoie.com

Tyler Bowen
bowen-ptab@perkinscoie.com

ARMOND WILSON LLP

Dated: July 17, 2024

By: /Michelle E. Armond/
Michelle E. Armond (Reg. No. 53,954)
Douglas R. Wilson (Reg. No. 54,542)
Joseph Li (Reg. No. 74,998)
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Attorneys for BeSang Inc.