

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner,

v.

BESANG INC.,

Patent Owner.

IPR2023-00991

Patent No. 7,378,702

**PETITIONER'S OPPOSITION TO PATENT OWNER'S
MOTION TO EXCLUDE EVIDENCE**

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I. INTRODUCTION

BeSang's motion to exclude paragraphs 22-25 of EX1037 (Dr. Sechen's reply declaration) and Exhibits 1041, 1043-1045, and 1048-1050 cited in the declaration and Reply suffers from several fatal flaws. First, under the regulations that govern IPRs and the Board's Consolidated Trial Practice Guide, challenges relating to the scope of a reply require filing a motion to strike after obtaining permission from the Board. BeSang did not follow the requisite procedure and may not raise the issue in a motion to exclude. Second, as confirmed by recent Federal Circuit case law, a petitioner may introduce evidence that responds to arguments in a patent owner's response and expands on arguments in a petition. In the POR, BeSang argued there were no motivations to combine the prior art references cited in the Petition. Intel responded by providing additional evidence buttressing previously presented motivations. Third, BeSang had notice of and an opportunity to respond to Intel's arguments; it simply chose not to, except for a few improper and incorrect statements in the current motion. The Board should deny BeSang's motion.¹

¹ BeSang's motion also seeks exclusion of Exhibits 1040, 1042, 1046, and 1054 (Paper 29, 4), but the Board granted Intel's request to expunge those exhibits (EX3001), rendering that portion of BeSang's motion moot.

II. BESANG’S MOTION IS PROCEDURALLY AND SUBSTANTIVELY DEFECTIVE

A. BeSang’s motion is improper

The Board’s Consolidated Trial Practice Guide (“CTPG”) is unequivocal: a motion to exclude should not “address arguments or evidence that a party believes exceeds the proper scope of reply.” CTPG, 79 (Nov. 2019). Instead, “[i]f a party believes that a brief...exceeds the proper scope of reply..., it may request authorization to file a motion to strike” and should generally do so “within one week of the allegedly improper submission.” *Id.*, 80-81. Obtaining Board authorization is required. 37 C.F.R. § 42.20(b) (“A motion will not be entered without Board authorization.”); CTPG, 37. BeSang is aware of the proper procedure. In a co-pending IPR relating to the same patent at issue here, BeSang filed a motion to strike asserting that evidence filed by petitioner Micron Technology, Inc. was “improper reply evidence.” *Micron Tech., Inc. v. BeSang Inc.*, IPR2023-00900, Paper 24, 1 (May 29, 2024). As required, BeSang sought and received the Board’s authorization before moving to strike. *Id.*

BeSang’s current request to exclude paragraphs 22-25 of EX1037 and Exhibits 1041, 1043-1045, and 1048-1050 runs afoul of the CPTG and 37 C.F.R. § 42.20(b). The motion should be denied on that basis alone. While BeSang objected to the testimony and exhibits (Paper 23, 1-7), it never asked the Board for authorization to file a motion to strike. Despite that failure, BeSang now relies on a

motion to exclude to raise issues about the Reply's scope. That is not allowed. CTPG, 79; *see also Apple Inc. v. Parus Holdings, Inc.*, IPR2020-00686, Paper 37, 41-42 (PTAB Sept. 9, 2021) (denying motion to exclude raising issues with a reply's scope).

BeSang cannot reasonably claim ignorance or prejudice: it is familiar with the Board's motion to strike procedure and followed it in IPR2023-00900. Further, the Board decisions cited by BeSang to justify its filing do not nullify that procedure. To the extent the ambiguous statement from *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-00912, Paper 30, 3 (PTAB June 10, 2021) (cited at Paper 29, 1), which was made during a telephonic conference, is inconsistent with the express statement in the CTPG (at 79) that a motion to exclude should not address reply scope issues, the Administrative Patent Judge's intent was to remain faithful to that document, not contradict it. *Id.*, EX2037, 3:13-6:1. As to *Dexcom, Inc. v. Waveform Techs., Inc.*, IPR2016-01680, Paper 46, 30-31 (PTAB Feb. 28, 2018) (cited at Paper 29, 4), that decision and the cases cited within it do not control the outcome here because they pre-date the CTPG, as well as the August 2018 revision of the Trial Practice Guide in which the Board first specified its motion to strike procedure for contesting issues regarding reply scope. *Compare* 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012) *with* Revised Trial Practice Guide, 16-17 (Aug. 2018). What is more, neither *Sotera* nor *Dexcom* is precedential.

B. Intel responded to the Board’s DI and BeSang’s POR by relying on arguments raised in the Petition

A petitioner’s reply brief may “respond to arguments raised” in a patent owner’s response. 37 C.F.R. § 42.23(b). In the POR, BeSang asserted that there were no motivations to combine Lee or Johnson with Aspar or Kim, as argued in the Petition. POR, 20-30 (Lee + Kim), 44-50 (Lee + Aspar), 65-68 (Johnson + Kim), 70-73 (Johnson + Aspar). In its Reply, Intel responded by providing additional explanation and support for motivations to combine raised in the Petition. Reply, 5-13.

BeSang now argues that paragraphs 22-25 of EX1037 and Exhibits 1041, 1043-1045, and 1048-1050 should be excluded because they allegedly “constitute new evidence and/or new argument exceeding the proper scope of reply.” Paper 29, 1. The expert testimony and exhibits at issue relate to monocrystalline silicon and process optimization as motivations to combine. Reply, 10. The Federal Circuit recently explained that a reply is proper “if it is responsive and simply expands on previously raised arguments.” *Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1384 (Fed. Cir. 2023); *see also W. Dig. Techs., Inc. v. Viasat, Inc.*, IPR2022-01171, Paper 33, 20-21, 25-26 (PTAB Dec. 13, 2023). So it is here.

Contrary to BeSang’s assertions (Paper 29, 2-3), Intel raised the monocrystalline silicon and process optimization arguments when the Petition was filed. Intel explained that a POSITA would have combined Lee or Johnson with

Aspar or Kim for several reasons. For one, Aspar’s Smart-Cut process had the “advantage[]” of “transferring thin layers...with a high crystalline quality.” Pet., 60-61, 80-81 (quoting EX1009, 834); EX1003, ¶¶ 212, 260; DI, 40. The transferred layer is made of “monocrystalline” silicon. Pet., 56-57, 78; EX1003, ¶¶205, 256.

Intel further argued that the prior art combinations would have “allow[ed] for more efficient quality control.” Pet., 53-54 (Lee + Kim), 61-62 (Lee + Aspar), 76 (Johnson + Kim), 81 (Johnson + Aspar). Citing Dr. Sechen’s original declaration, the Petition described one example to support this motivation to combine—testing to detect deficient structures that would have been discarded rather than bonded to acceptable structures. *Id.* (citing EX1003, ¶¶196, 213). In the cited paragraphs of his declaration, Dr. Sechen supplied another example:

In addition, a POSITA would have recognized that forming electrical devices on one substrate separately from the memory devices on another substrate would have allowed *optimization of the respective processes rather than forcing the memory devices to be formed with a sub-optimal process* tailored to preserving the electrical devices formed on the single wafer in the monolithic process.

EX1003 ¶¶196 (Lee + Kim), 213 (Lee + Aspar), 251 (Johnson + Kim), 261 (Johnson + Aspar) (emphasis added). The Petition advanced the process optimization argument by citing Dr. Sechen’s testimony to support the quality control motivation

to combine. *Life Spine, Inc. v. Globus Med., Inc.*, IPR2022-01435, Paper 36, 92 n.21 (PTAB Apr. 18, 2024) (petition citing an expert’s declaration was “sufficiently clear” to indicate that petitioner was relying on the benefit discussed in the declaration). The Petition also cited Kim’s disclosure of “integrat[ing] diverse process technologies” using, for example, “logic/memory stacking,” and described Kim’s approach as an improvement, citing testimony from Dr. Sechen. EX1008, ¶22; Pet., 51 (citing EX1008, ¶22), 53, 75-76; EX1003, ¶¶190, 195, 249.

The monocrystalline silicon and process optimization motivations to combine are linked because manufacturing different portions of a device separately would have facilitated use of Aspar’s monocrystalline silicon, which requires high-temperature processing that would otherwise have damaged logic circuits. EX1037, ¶24.

The Board instituted review, flagging that whether Intel’s combinations would have improved the prior art remained an open issue. *E.g.*, DI, 36-37. BeSang then took Dr. Sechen’s deposition. Paper 16. In response to BeSang’s questioning, including about paragraph 213 quoted above, Dr. Sechen testified about the benefits of monocrystalline silicon and process optimization. EX2039, 91:17-98:13. He explained that it was preferable to use “single crystalline silicon for forming...memory devices” (*id.*, 93:18-20, 94:8-14) and that fabricating portions of a device separately would have avoided damage due to, for example, ions passing

through layers and heat deforming metal (*id.*, 95:17-97:4). In the POR, BeSang argued that Intel had not provided any motivations to combine. POR, 20-30, 44-50, 65-68, 70-73. In the Reply, Intel responded to the Board’s DI and refuted BeSang’s POR by elaborating on the monocrystalline silicon and quality control arguments found in the Petition and providing additional testimony from Dr. Sechen and evidence tied directly to arguments first raised in the Petition. Reply, 10; EX1037, ¶¶22-25; EX1041; EX1043-EX1045; EX1048-EX1050.

The Federal Circuit approved of a similar approach. In *Rembrandt*, the petitioner originally argued that prior art combinations would have increased efficiency and provided benefits. 76 F.4th at 1384-85. The patent owner countered that there were no motivations to combine. *Id.* In its reply, the petitioner argued that the combinations would have “save[d] cost and time” for one combination and “reduc[ed] cost” and “simplif[ied] a device” for another. *Id.* The Federal Circuit found the cost-and-time explanation had “a nexus to...prior argument and [was] responsive.” *Id.* at 1385. The argument also “refuted...assertions that there [was] no motivation” and “properly expand[ed] on and [wa]s a fair extension of [the] previously raised efficiency argument.” *Id.* The court concluded the petitioner’s reduced cost and simplification motivations were responsive to the patent owner’s arguments and the Board’s observations in the institution decision and “elaborate[d] on the motivation-to-combine argument...made in [the] petition—that there were

benefits in the art” for the proposed combination. *Id.*

As in *Rembrandt*, Intel’s monocrystalline silicon and process optimization arguments in the Reply flow from arguments made in the Petition. When the Board raised questions about improvements tied to Intel’s prior art combinations (DI, 36-37) and BeSang argued motivations to combine were absent (POR, 20-30, 44-50, 65-68, 70-73), Intel responded in the Reply with more explanation and evidence to support its arguments. *Rembrandt*, 76 F.4th at 1384 (“[T]he introduction of new evidence in the course of the trial is to be expected in [IPR] trial proceedings....”) (citation and quotation marks omitted).

BeSang’s cited Federal Circuit cases are inapposite. In *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369-70 (Fed. Cir. 2016) (cited at Paper 29, 1), as noted in *Rembrandt*, the petitioner originally argued that a single reference disclosed a limitation but shifted to a combination of references on reply. 76 F.4th at 1383. Here, Intel’s Reply relies on the “same ‘legal ground[s]’” based on the “same prior art reference[s]” and the “same legal argument[s].” *Id.* at 1385. As to *Acceleration Bay, LLC v. Activision Blizzard Inc.*, 908 F.3d 765, 775 (Fed. Cir. 2018) (cited at Paper 29, 4), the Federal Circuit found the Board properly “declin[ed] to consider” paragraphs in a reply declaration that “raise[d] a new obviousness argument.” Here, Dr. Sechen’s reply declaration does not raise new arguments; it elaborates on arguments raised in the Petition and his original declaration.

BeSang cites several non-precedential Board decisions that are also distinguishable. In *Apple Inc. v. MemoryWeb, LLC*, PGR2022-00006, Paper 43, 8-9 (PTAB. Aug. 3, 2023) (cited at Paper 29, 2) and *Caterpillar Inc. v. Wirtgen Am., Inc.*, IPR2022-01310, Paper 34, 49 (PTAB Feb. 6, 2024) (cited at Paper 29, 3), the arguments at issue were not mentioned in the petition or the expert's original declaration, as they were here. In *Dexcom*, IPR2016-01680, Paper 46, 29-31 (cited at Paper 29, 4), the Board rejected references filed in a reply that the petitioner relied on to disclose a claim limitation. Intel's Reply did not add any references to its grounds of unpatentability.

BeSang also overreaches by asking the Board to exclude EX1041, EX1043, and EX1049 even though Intel relies on those exhibits as evidence to support its testing argument, which BeSang does not assert is "new." Paper 21, 9-10 (citing Exhibits 1041, 1043, and 1049). For this additional reason, these three exhibits should not be excluded.

C. BeSang elected not to substantively address Intel's arguments in its briefing and cannot do so now

Based on the Petition and Dr. Sechen's original declaration, BeSang has long known about Intel's monocrystalline silicon and process optimization arguments. The record reflects just that: BeSang cross-examined Dr. Sechen about both arguments nearly two weeks before the POR was due. Paper 15; Paper 16; Paper 21; EX2039, 74:10-75:10, 91:17-98:13. BeSang had ample opportunity to address

Intel's arguments. *E.g.*, *SanDisk Corp. v. NetList, Inc.*, IPR2015-01021, Paper 38, 20 (PTAB Sept. 28, 2016) (patent owner had "notice" and "an opportunity to refute" a position described at an expert's deposition 10 days before the deadline for patent owner's response). But it chose not to do so in the POR or its expert's declaration. Paper 17; EX2029. Even after receiving Intel's Reply and related evidence, BeSang did not address the arguments in its Sur-Reply or ask Dr. Sechen about them during his second deposition. Having deliberately decided not to contest the arguments, BeSang cannot claim prejudice if the Board denies its motion.

BeSang belatedly attempts to address the merits in its motion, arguing that Intel's arguments and Dr. Sechen's testimony "provide[] no motivation" to look to Aspar and are undermined by Dr. Sechen's purported concession that monocrystalline silicon can be added by epitaxy. Paper 29, 3. BeSang's assertions are both improper and unpersuasive. The Board has explained that "[a] motion to exclude...may not be used to challenge the sufficiency of the evidence to prove a particular fact" or to address "the weight to be given evidence." CTPG, 79. That prohibits BeSang from arguing that Dr. Sechen's testimony (EX1037, ¶24) fails to support Intel's motivations to combine. Paper 29, 3. As to the substance of BeSang's assertions, while BeSang says that Dr. Sechen's testimony "provides no motivation to look to Aspar's (or Kim's) stacking," his reply declaration described exactly why a POSITA would have looked to Aspar's techniques to obtain monocrystalline

silicon. Paper 29, 3; EX1037, ¶24. BeSang also suggests that Dr. Sechen opined that epitaxy can be used to form monocrystalline silicon, but he further explained that epitaxy requires high temperatures incompatible with logic circuits, which supports that a POSITA would have pursued separate optimized processes for memory and logic portions of a device. EX1037, ¶24.

III. CONCLUSION

BeSang's motion to exclude should be denied.

Dated: August 28, 2024

Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served a true and correct copy of the foregoing: PETITIONER’S OPPOSITION TO PATENT OWNER’S MOTION TO EXCLUDE EVIDENCE by email to the electronic service addresses for Patent Owner:

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