

Filed on behalf of BeSang Inc.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00991
U.S. Patent No. 7,378,702

**PATENT OWNER'S REPLY IN SUPPORT OF
MOTION TO EXCLUDE EVIDENCE**

Pursuant to 37 C.F.R. § 42.64(c) and the Scheduling Order (Paper 13), BeSang hereby submits its Reply in support of its Motion to Exclude Evidence (Paper 29).¹

I. BESANG’S MOTION PROPERLY SEEKS TO EXCLUDE INTEL’S IMPROPER NEW REPLY EVIDENCE AND ARGUMENTS

BeSang timely objected to Intel’s improper new evidence, as Intel admits, and appropriately filed its Motion to Exclude. *See* Paper 23 at 1-8; Paper 30 (“Opp.”) at 2. BeSang’s cited authority explained that “motions to exclude [are] a potential remedy to exclude certain evidence or argument that would exceed the proper scope of a reply.” *Sotera Wireless v. Masimo Corp.*, IPR2020-00912, 2021 WL 2384365, at *1 (P.T.A.B. June 10, 2021). Indeed, “Federal Circuit case law indicates that a motion to exclude is a proper vehicle for enforcing [the Board’s] rule and trial practice guide regarding the scope of evidence that may be submitted with a reply brief.” *Dexcom v. Waveform Techs.*, IPR2016-01680, 2018 WL 1137089, at *13 (P.T.A.B. Feb. 28, 2018).

Intel cites *Apple v. Parus Holdings*, IPR2020-00686, Paper 37 at 41-42 (P.T.A.B. Sept. 9, 2021), but that opinion is not binding on the Board. The Board may “construe [relevant] aspect[s] of the Motion as a Motion to Strike.” *Intuitive*

¹ Intel conceded that Exhibits 1040, 1042, 1046, and 1054 are inadmissible, and the Board granted Intel’s request to expunge them. *See* EX3001.

Surgical v. Ethicon, IPR2019-00991, Paper 48 at 41 (P.T.A.B. Jan. 12, 2021)

(striking portion of a reply containing argument not raised in the petition).

II. EXHIBITS 1041, 1043-1045, 1048-1050, AND PORTIONS OF EXHIBIT 1037 (¶¶22-25) ARE IMPROPER REPLY EVIDENCE

Intel’s assertion that it properly filed *new* Exhibits 1041, 1043-1045, 1048-1050, and Dr. Sechen’s reply declaration (EX1037 ¶¶22-25) to rebut BeSang’s argument that “there were no motivations to combine Lee or Johnson with Aspar or Kim” in the Petition, Opp. at 4-9, is as absurd as it sounds. To rebut an assertion that the Petition provided no motivation to combine, one might be expected to point to the Petition with its exhibits. Intel’s reliance on new evidence not submitted with the Petition only confirms rather than rebuts BeSang’s assertion.

Intel’s new process optimization motivation asserts that avoiding high temperatures, which damage logic circuits, was a reason to process a monocrystalline layer separately and then bond it as described in Aspar. EX1037 ¶24.

Intel cites only two alleged motivations in its Petition as supporting this new argument—transferring thin monocrystalline layers of high quality, and quality control—neither of which is its process optimization motivation argued in its Reply. Opp. at 4-5. Then, Intel asserts that the Petition advanced the high temperature process optimization argument not by making it but instead by citing a paragraph of

Dr. Sechen’s declaration that mentions in a single sentence “optimization of the respective processes” without discussing avoiding high temperature processes at all. *Id.* at 5 (quoting EX1003 ¶¶196, 213).

In fact, Dr. Sechen’s deposition directly contradicts any alleged connection between high temperature processing and optimization. When asked specifically about the optimization sentence now relied upon by Intel at his deposition, EX2039 at 91:21-93:1, Dr. Sechen disavowed any connection between “thermal budget” and this sentence, which he described as “talking about two different types of semiconductor materials being used for the substrate versus the upper layers which are memory cells for devices,” *id.* at 98:17-99:11 (responding when asked about “thermal budget”: “this sentence, by the way, we’re -- we’re diverting from it, it shouldn’t be highlighted because we’re not talking about it.”). Intel asserts that BeSang “has long known about” Intel’s arguments based on Dr. Sechen’s deposition, Opp. at 9, but the testimony shown above unequivocally asserted that Dr. Sechen’s opening declaration had nothing to do with thermal budget or high temperature processing. EX2039 at 98:17-99:11 (“This is talking about two different types of semiconductor materials....”).

Intel’s citation to a footnote in *Life Spine v. Globus Med.* is inapposite because there it was “sufficiently clear” that the petitioner cited its expert’s opinion “in connection with its argument” regarding the relevant motivation to combine.

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IPR2022-01435, Paper 36 at 92 n.21 (P.T.A.B. Apr. 18, 2024). Here, Intel relied on Dr. Sechen’s original declaration testimony to support a different motivation relating to quality control, *not* high temperature process optimization. *See* Pet. at 53-54 (citing EX1003 ¶196); *id.* at 61-62 (citing EX1003 ¶213); EX2039 at 98:17-99:11.

Intel’s reliance on *Rembrandt Diagnostics v. Alere*, 76 F.4th 1376 (Fed. Cir. 2023), and *Western Digital Techs. v. Viasat*, IPR2022-01171, Paper 33 (P.T.A.B. Dec. 13, 2023), is also misplaced. Unlike Intel’s Reply, which disclosed an entirely new motivation to combine, in *Rembrandt* and *Western Digital* the petitioner’s reply argument was a “fair extension of its previously raised efficiency argument.” 76 F.4th at 1385; IPR2022-01171, Paper 33 at 20-21, 25-26; *see also Fantasia Trading v. CogniPower*, IPR2021-00067, 2022 WL 1613101, at *12 (P.T.A.B. May 11, 2022) (“[I]t is too late to raise a new motivation to combine with the Reply.”).

Finally, Intel concludes with a passing argument that it also relies on EX1041, EX1043, and EX1049 “to support its testing argument.” Opp. at 9. Intel cites no authority that citing objectionable evidence in support of another argument renders them immune to exclusion. At a minimum, the Board should decline to consider those exhibits and corresponding portions of Dr. Sechen’s reply declaration in support of Intel’s new high temperature “process optimization” argument.

III. BESANG ADDRESSED INTEL’S ARGUMENTS IN ITS SUR-REPLY

Intel’s assertion that “BeSang belatedly attempts to address the merits in its motion” is a red herring. Opp. at 10. BeSang’s Sur-Reply timely raised the exact issue Intel claims BeSang failed to address—that Intel’s arguments and Dr. Sechen’s testimony provide no motivation to look to Aspar. See Paper 25 (“Sur-Reply”) at 15 (“Even if considered, Intel’s assertion that ‘Aspar’s process would have benefited [sic] Lee by adding monocrystalline silicon,’ provides no motivation to look to Kim or Aspar’s stacking. Dr. Sechen even acknowledges that monocrystalline silicon could be added ‘using epitaxy.’” (internal citations omitted)).

Responding to BeSang’s Sur-Reply argument, Intel asserts that Dr. Sechen “explained that epitaxy requires high temperatures incompatible with logic circuits, which supports that a POSITA would have pursued separate optimized processes for memory and logic portions of a device.” Opp. at 11 (citing EX1037 ¶24, which is the subject of BeSang’s Motion). But that ignores that Aspar itself included a 1100°C high-temperature annealing step, creating the same problem Intel claims it solves. Paper 17 at 45-49; Sur-Reply at 15-16.

IV. CONCLUSION

BeSang respectfully requests the Board exclude Exhibits 1041, 1043-1045, 1048-1050, and Exhibit 1037 ¶¶22-25.

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Dated: September 4, 2024

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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a true copy of the foregoing **PATENT OWNER’S REPLY IN SUPPORT OF MOTION TO EXCLUDE EVIDENCE** is being served electronically on September 4, 2024 to the following counsel for Petitioner to the following email addresses:

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