



Intel Corporation v. BeSang Inc.

U.S. Patent No. – IPR2023-00991

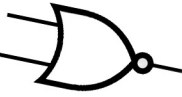
September 18, 2024

Judges Tornquist, McGraw, and Roesel

IPR Grounds

Ground (all under 35 U.S.C. §103)	Claims	References
1A	13–17	Lee
1B	16–17	Lee , Endoh
1C	13–17	Lee, Kim
1D	16–17	Lee, Kim, Endoh
1E	13–17	Lee, Aspar
1F	16–17	Lee, Aspar, Endoh
2A	13	Johnson
2B	13	Johnson, Kim
2C	13	Johnson, Aspar
3	1	Park , Kim

Grounds 1C/1D: Lee + Kim (and Endoh)



No Motivation:
NOR to NAND

Doesn't Address
All Claim
Limitations

Incoherent
Cross-Refs

No. 2 Memory
Cells "Serially
Connected
Together"

Incorrect
SOI Pillar
construction
doesn't meet
burden

Why modify
Lee's
design?

No motivation to stack
interleaved layers

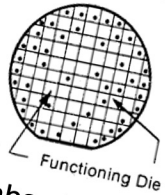
Lee teaches
deposition

Kim discards a
wafer every time

No motivation
to combine
[All Claims]

Fig. 25A inoperable

Fabs already
test



Functioning Die

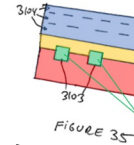
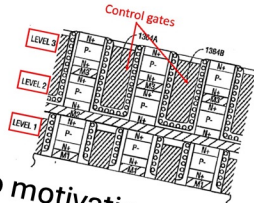
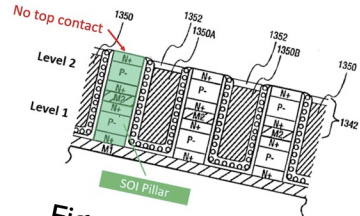
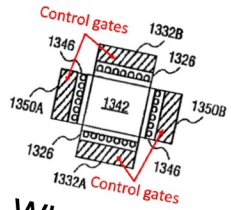
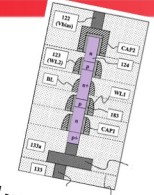


Figure 35



Grounds 2B/2C: Johnson + Kim (or Aspar)

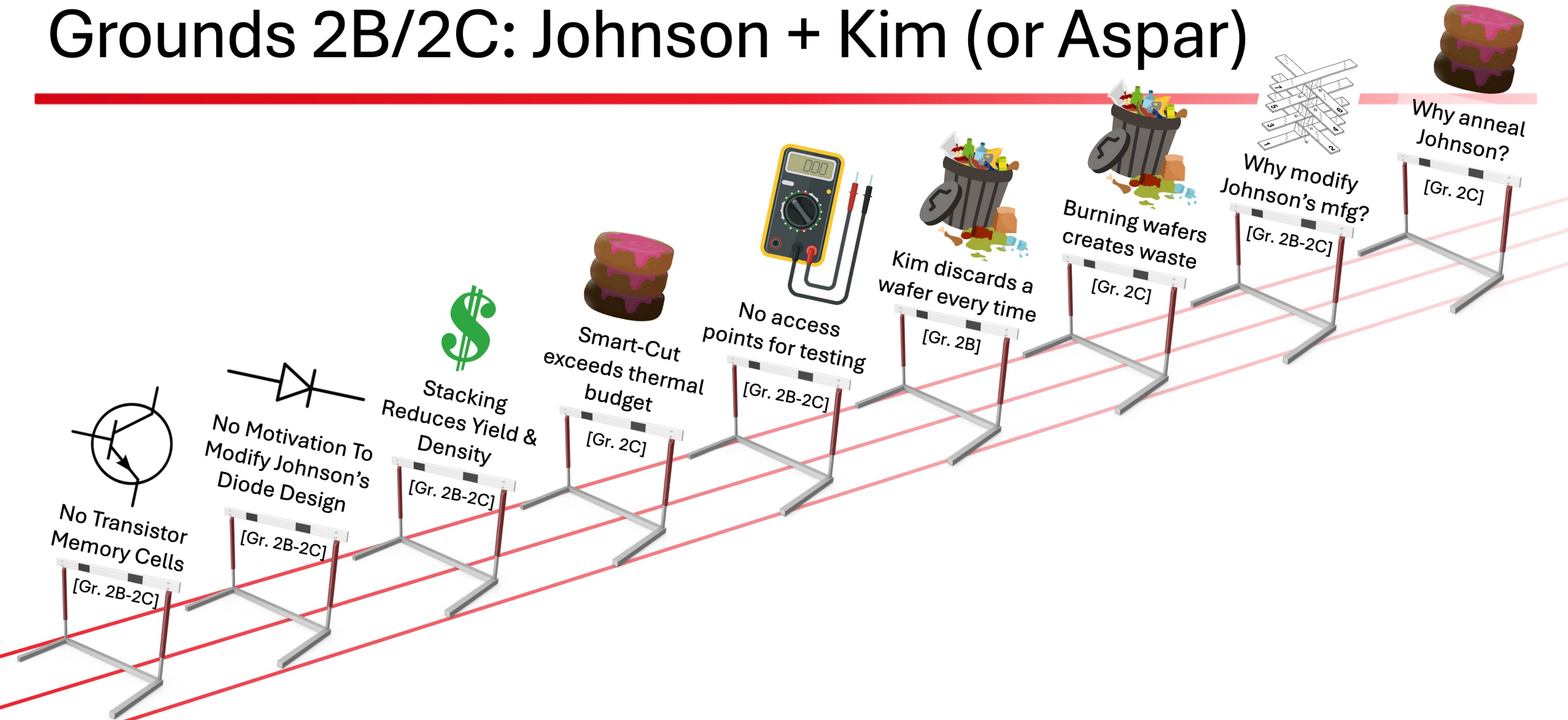




FIG. 2



FIG. 25B
(top down)

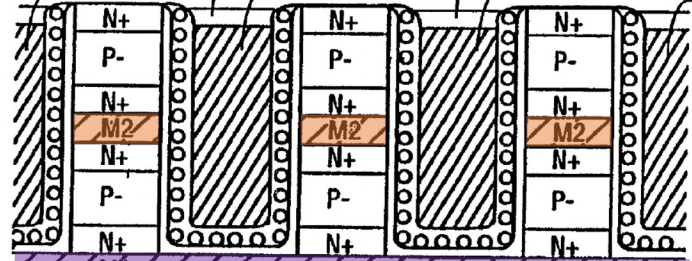


FIG. 25A
(cross section)

Sechen: Aspar Anneals at 1100°C

45. The Bond and Etch-Back method (pictured below) includes removing the heavily doped substrate of one wafer by mechanical methods (e.g., grinding). Exhibit 1014, 92; Exhibit 1015, 58–59.

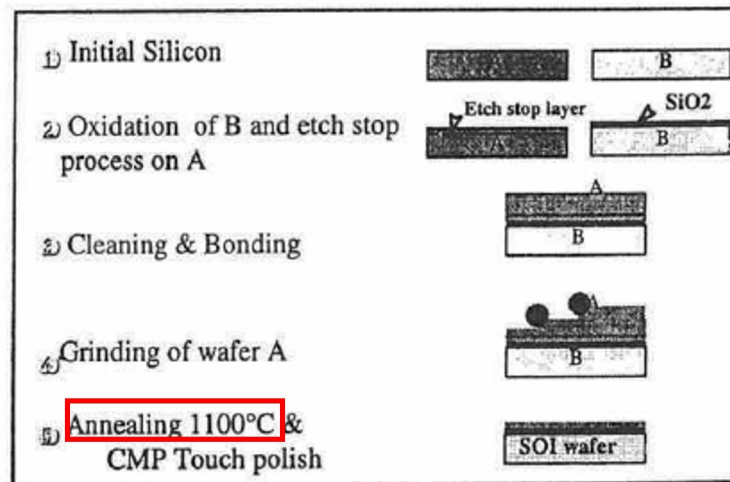
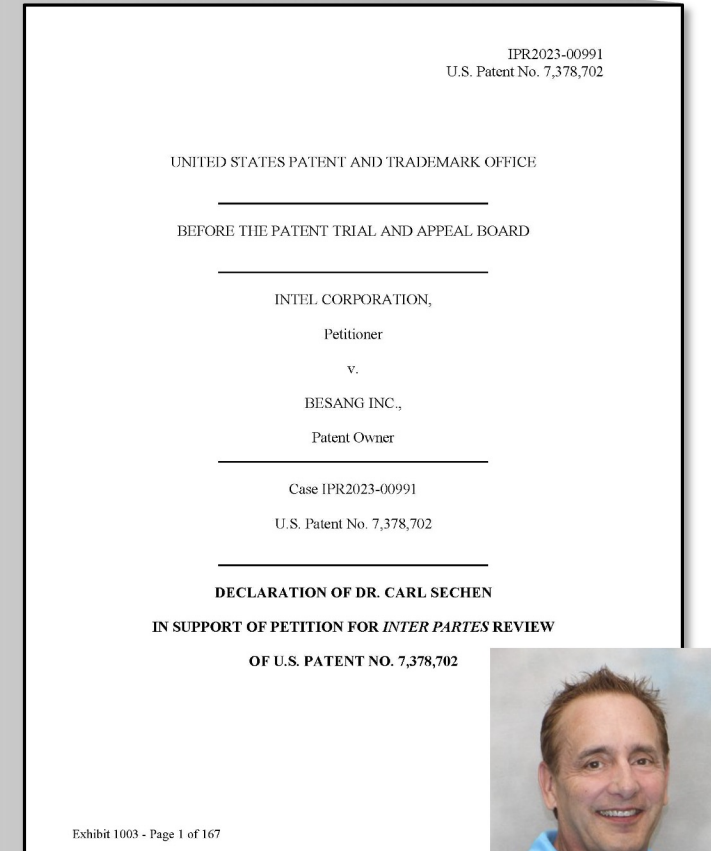


Fig. 11-23 Schematic of the Bonded-and-Etched-Back SOI technology (*BESOI*).

Exhibit 1015, Fig. 11-23 (p. 59)



Sechen: Aspar Anneals at 1100°C

46. The Smart-Cut® method (shown below) starts by oxidization and ion-implantation of wafer A. Exhibit 1014, 92–93; Exhibit 1015, 59–61.

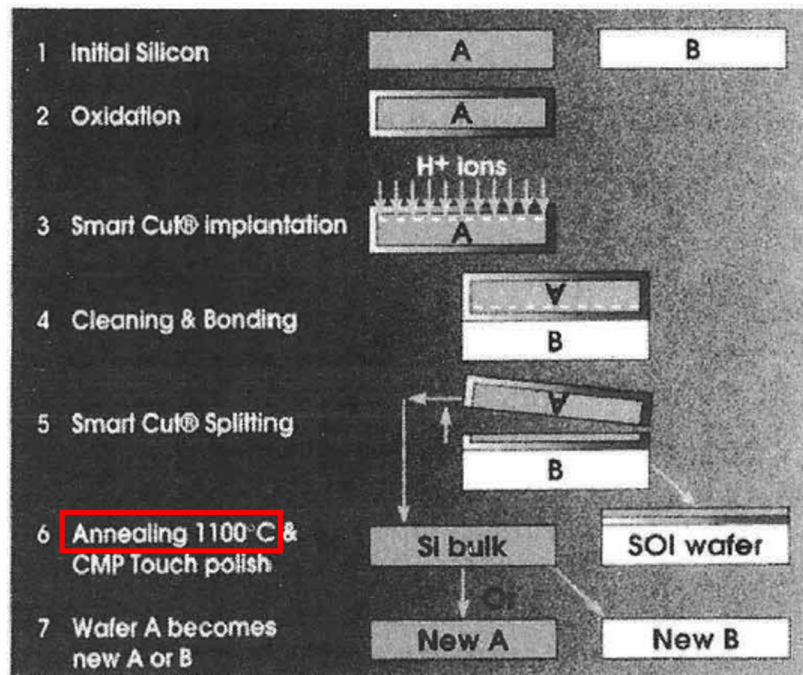
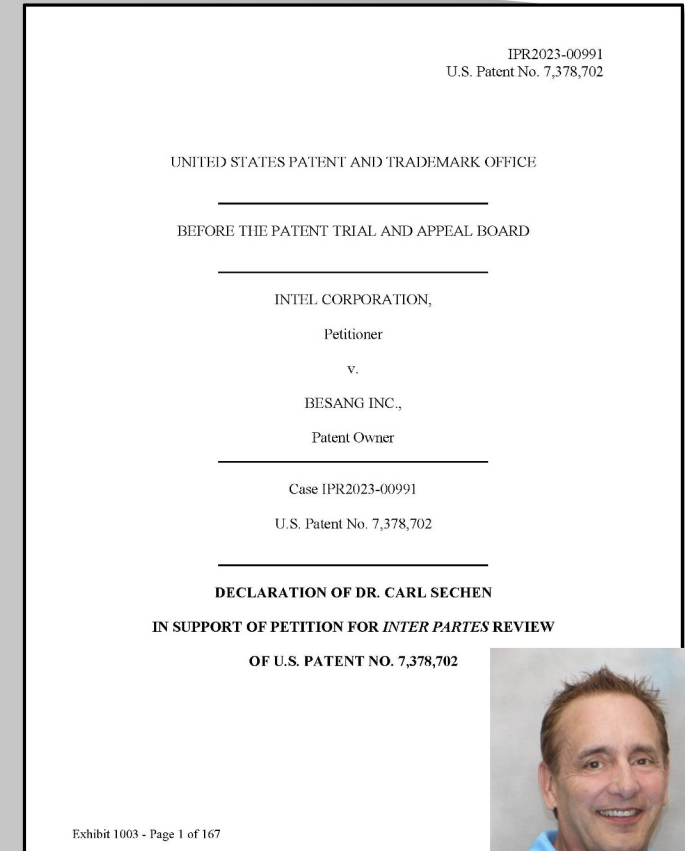
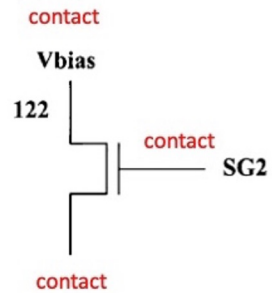


Fig. 11-24 Process flow for fabricating Smart-Cut® wafers.

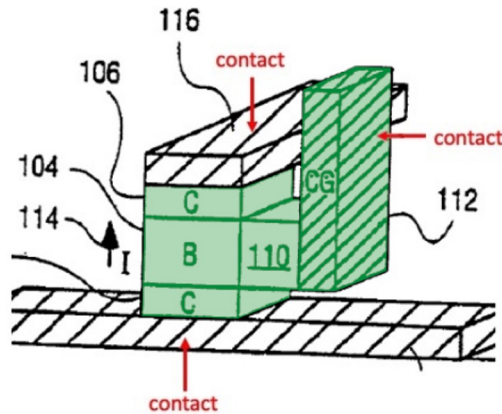
Exhibit 1015, Fig. 11-24 (pg. 60); *see also* Exhibit 1014, Fig. 7-29 (pg. 92).



Johnson's 2-Terminal Diode Design



'702 Patent
Fig. 30 (excerpted)



Lee's transistor
Fig. 1A (excerpted, annotated)



Johnson
Fig. 8(b)

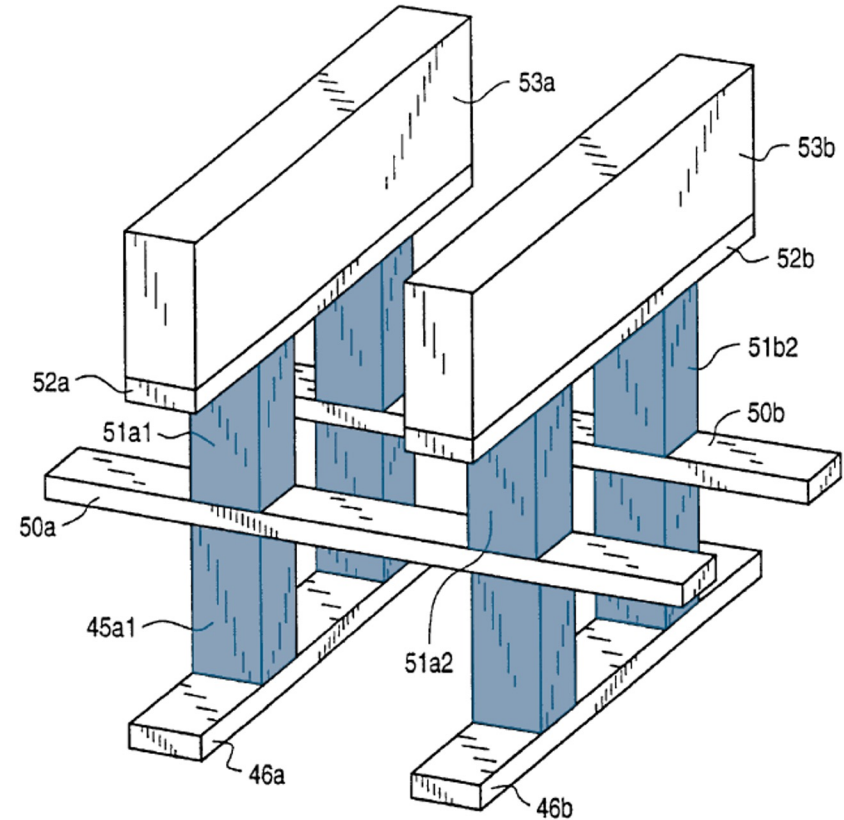


FIG. 6(g)

Grounds 1E/1F: Lee + Aspar

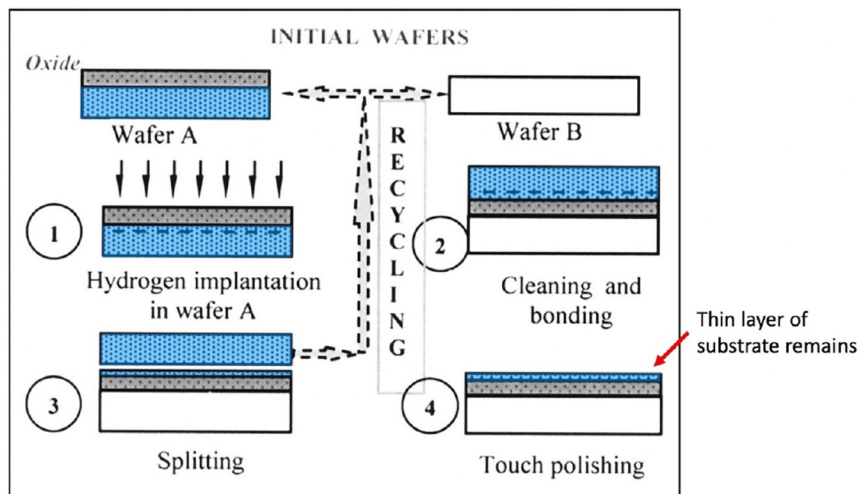
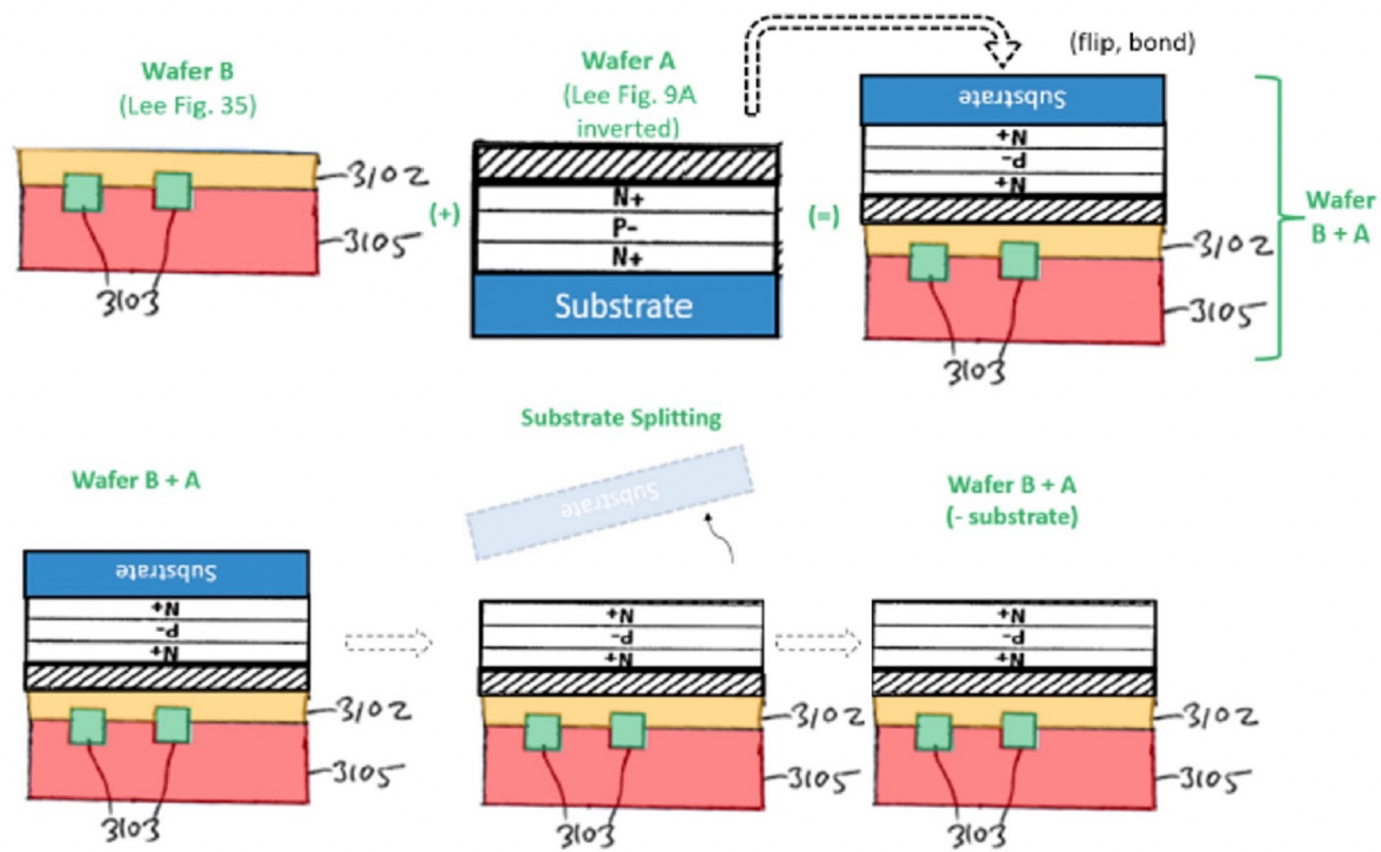


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.



Ground 2C: Johnson + Aspar

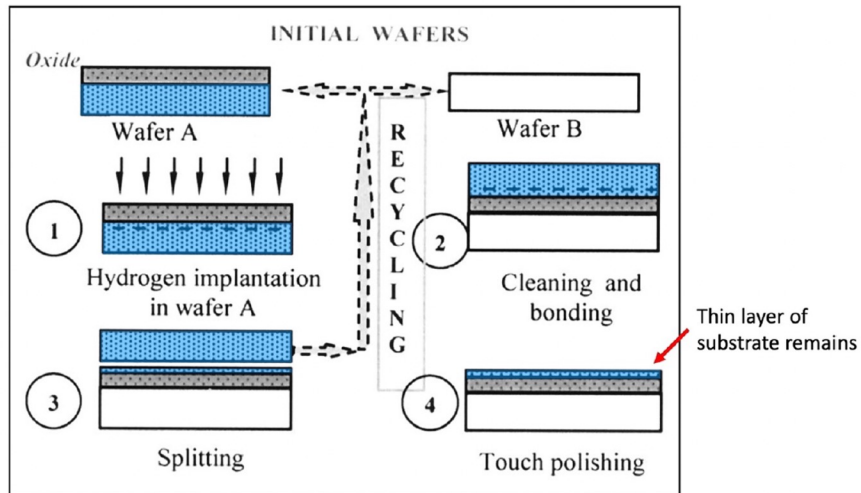
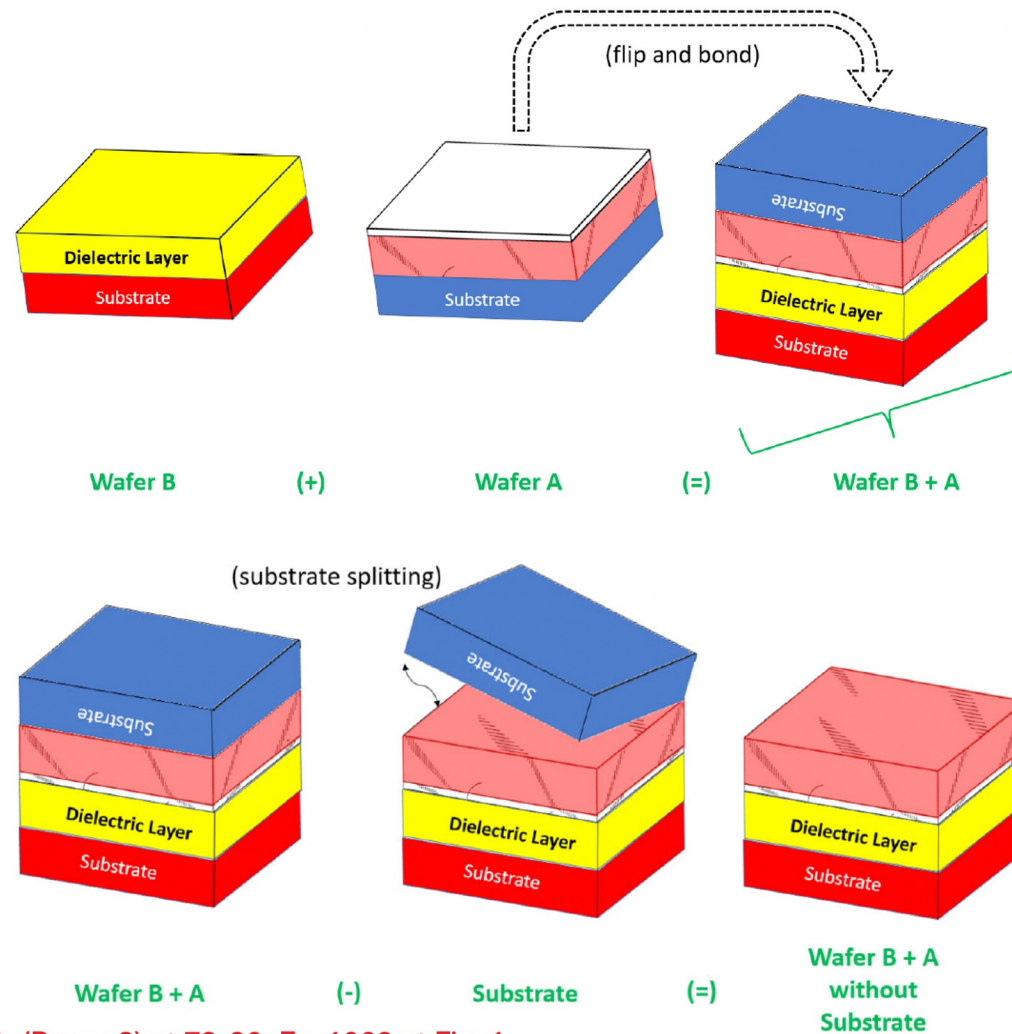
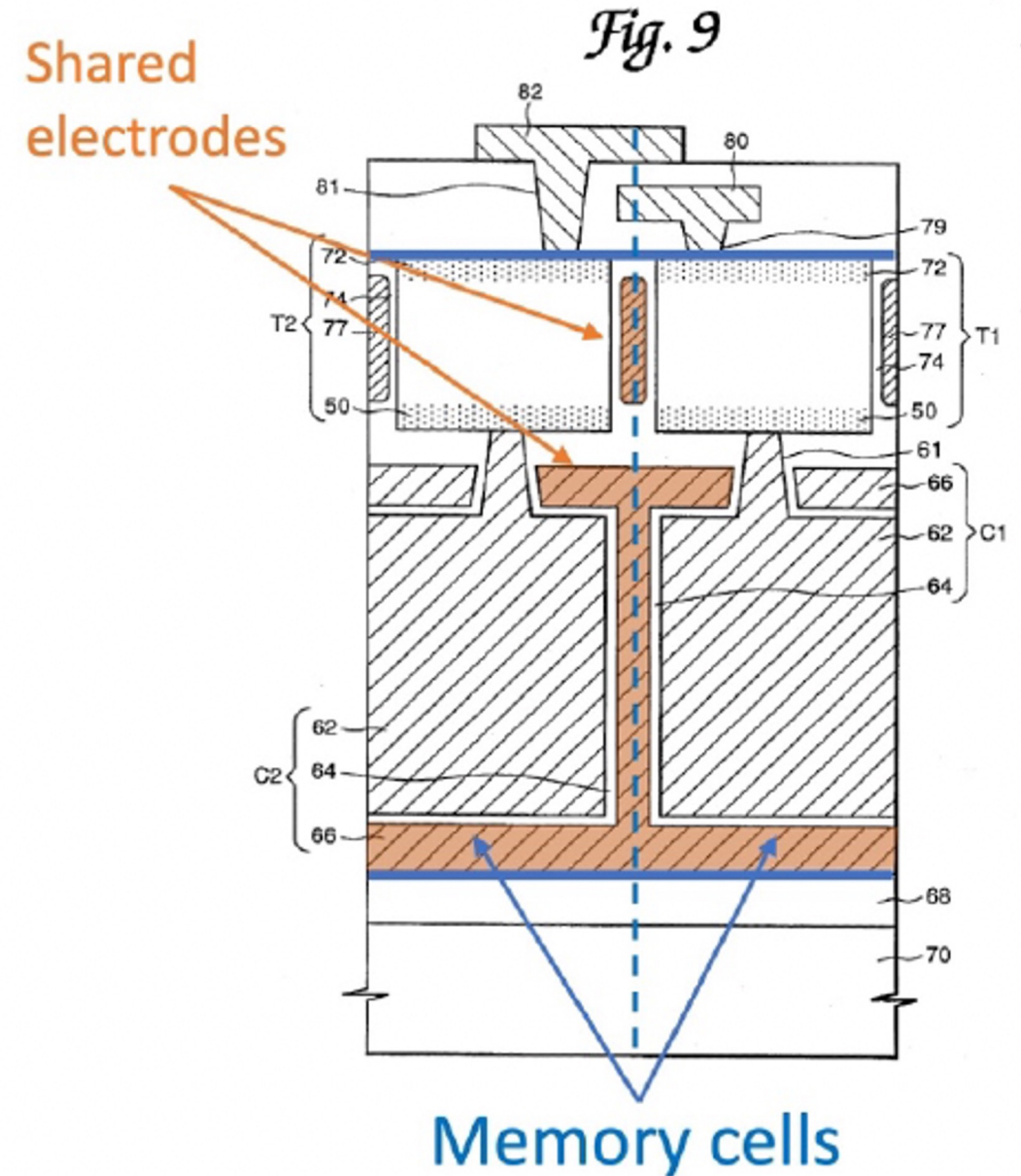


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.



Ground 3: Park + Kim



'702 Patent - Claim 1

1. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate;
and
a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;
wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate; and
wherein the memory cell is a DRAM having at least one transistor.

'702 Patent - Claim 13

13. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
the stackable add-on layer being bonded to the dielectric layer; and
wherein the memory cells are nonvolatile memory cells having at least one transistor.

'702 Patent - Claim 14

14. The semiconductor memory structure of claim **13**, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

'702 Patent - Claim 15

15. The semiconductor memory structure of claim **13**, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

'702 Patent - Claim 16

16. The semiconductor memory structure of claim **13**, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

'702 Patent - Claim 17

17. The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.