

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner,

v.

BESANG INC,

Patent Owner.

IPR2023-00991

Patent No. 7,378,702

PETITIONER'S DEMONSTRATIVE EXHIBITS

Intel Corp. v. BeSang, Inc., IPR2023-00991

September 18, 2024, Oral Hearing
Intel's Demonstratives

Roadmap

- Overview
- Claim construction
- Lee + Aspar/Kim – claims 13-15
- Lee + Aspar/Kim [+ Endoh] – claims 16-17
- Johnson + Aspar/Kim – claim 13
- Park + Kim – claim 1
- Intel's arguments are responsive/not new
- BeSang's motion to exclude

Overview

Intel's combinations

- **Lee** (Grounds 1A-1F) (claims 13-17) or **Johnson** (Grounds 2A-2C) (claim 13) is the base reference
- **Kim** or **Aspar** discloses “stackable add-on layer” (claims 13-17) under Board / Intel construction (Grounds 1C-1F, 2B-2C)
- **Aspar** is used to address “SOI pillar” (claims 14-17) under Board / Intel construction (Grounds 1E-1F)
- As an alternative to Lee, **Endoh** discloses “serially connected” memory cells (claims 16, 17) (Grounds 1B, 1D, 1F)
- **Park + Kim** renders claim 1 obvious (Ground 3)

Under Board / Intel constructions of “stackable add-on layer” and “SOI pillar,” just a few Intel arguments are relevant

Ground (all under 35 U.S.C. §103)	Claims	References
1A	13-17	Lee
1B	16-17	Lee, Endoh
1C	13-17	Lee, Kim
1D	16-17	Lee, Kim, Endoh
1E	13-17	Lee, Aspar
1F	16-17	Lee, Aspar, Endoh
2A	13	Johnson
2B	13	Johnson, Kim
2C	13	Johnson, Aspar
3	1	Park, Kim

Ground(s)	Claim(s)	References
1C	13	Lee + Kim
1E	13-17*	Lee + Aspar
1F	16-17*	Lee + Aspar + Endoh
2B-C	13	Johnson + Aspar/Kim
3	1	Park + Kim

*“SOI pillar” only appears in claims 14-17

BeSang does not propose an alternative construction for “stackable add-on layer”

Additional arguments based on Lee and Kim are relevant if the Board adopts BeSang's construction for "SOI pillar"

Ground	Claims	References
1C	14-17*	Lee + Kim
1D	16-17*	Lee + Kim + Endoh

*"SOI pillar" only appears in claims 14-17

Claim construction

BeSang contests the Board's preliminary claim constructions

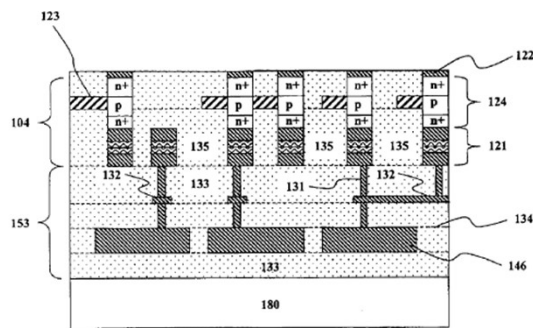
Limitation	Board / Intel Construction	BeSang Construction
“stackable add-on layer...the stackable add-on layer [is/being] bonded”* (Claims 1, 13)	“a layer that is formed separately from the substrate and then bonded to the substrate or a dielectric layer above the substrate” (DI, 9) does not include “memory cells that are formed by sequential deposition on or above a substrate or dielectric layer without being added to a separately formed substrate” (DI, 9) “a separate layer that is formed apart from the substrate and then subsequently bonded to the substrate or a dielectric layer above the substrate” (DI, 11)	Disputed but no alternative proposal (POR, 15; Sur-Reply, 3-4) Apparent construction from complaint in parallel district court proceedings: “any layer that is directly or indirectly adhered to the recited layer of the substrate” (Pet., 12)
“SOI pillar” (Claims 14-17)	“pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology” (DI, 12)	“a silicon-on-insulator structure taller than it is wide” (POR, 16)

*The demonstratives refer to these limitations jointly as “stackable add-on layer”

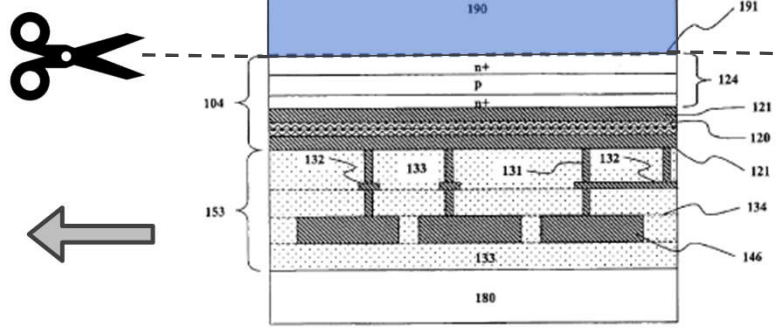
A “stackable add-on layer” requires bonding separate structures

SOI layers can be formed in a variety of ways. Unless otherwise noted, “SOI layer” is used herein to refer to a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate. In this context, the SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections. As a stackable add-on,

EX1001, 4:47-57 (see also EX1005, 6:4-17)

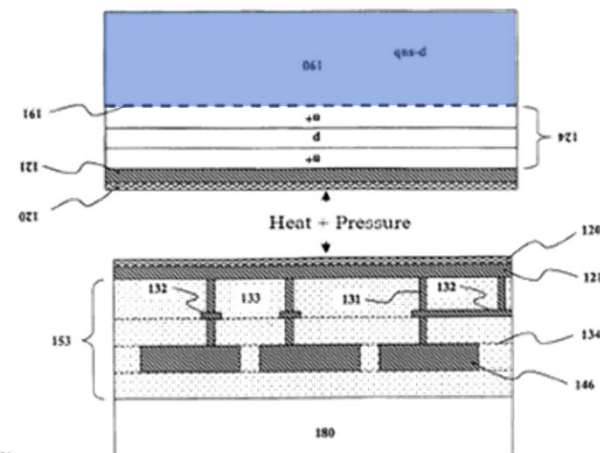


EX1005, Fig. 4D



EX1005, Fig. 4C (annotated)
(detach substrate)

EX1005, Fig. 4A (annotated)
(flip)



EX1005, Figs. 4A (annotated), 4B
(bond)

*Claims 1 and 13 both recite
“stackable add-on layer”

“Bonding” in Board construction encompasses “wafer bonding” in Intel construction

In summary, we preliminarily construe “stackable add-on layer . . . the first stackable add-on layer is/being bonded” to require a separate layer that is formed apart from the substrate and then subsequently bonded to the substrate or a dielectric layer above the substrate.⁹ We do not construe independent claims 1 or 13 to require any particular form or method of bonding.¹⁰

DI, 11

Intel construction requires “wafer bonding”

Board construction requires “bonding”

stackable add-on layer being bonded to the dielectric layer.” Based on the plain language and intrinsic record, a POSITA would have understood these limitations to require that the “stackable add-on layer” is wafer bonded to the recited layer of the substrate. Sechen, ¶71.

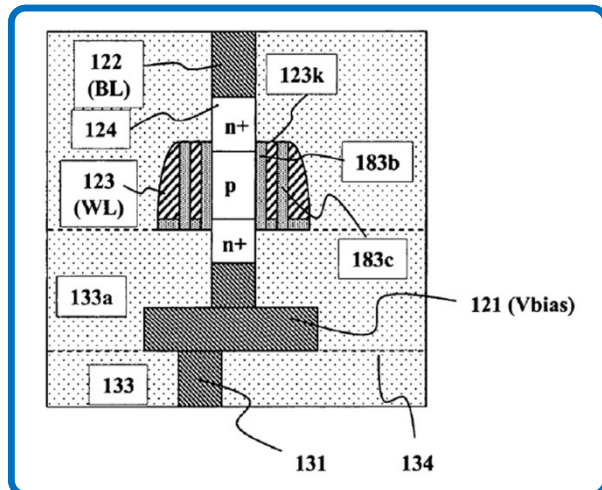
Based on the plain language, a POSITA would have understood that a “stackable add-on layer” must be its own structure capable of being stacked and added onto the other recited structures. *Id.* As a simplified analogy, when making a

The specification supports the construction of “pillar” proposed by Intel and applied by the Board

Petitioner contends the term “SOI pillar” in claims 14–17 “requires a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology.” Pet. 13. Petitioner provides intrinsic record

“representations at face value.” Prelim. Resp. 14. As such, for purposes of this decision and based on the intrinsic evidence provided by Petitioner, we apply Petitioner’s proposed construction of “SOI pillar.”

DI, 12



EX1001, Fig. 23

In various embodiments of the present invention, a FLD can be directly contacted by metal electrodes at top, bottom, and intermediate regions of the individual doped stack structures (i.e., pillar structures). The area of the metal

EX1001, 6:26-29

Pet., 13-16; EX1003, ¶¶ 85-91; Reply, 3
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

“SOI” refers to the claimed pillar’s creation and composition

Petitioner contends the term “SOI pillar” in claims 14–17 “requires a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology.” Pet. 13. Petitioner provides intrinsic record

“representations at face value.” Prelim. Resp. 14. As such, for purposes of this decision and based on the intrinsic evidence provided by Petitioner, we apply Petitioner’s proposed construction of “SOI pillar.”

DI, 12

individually working ICs. However, embodiments of the present invention do not use individually working ICs, but rather, as shown in FIG. 2, provide device integration technology using bonded SOI technology and a thin single crystalline semiconductor layer 124 without device formation before layer transfer. Because single crystalline semiconductor layer 124 is formed by SOI technology, it is referred to herein simply as an SOI.

EX1005, 6:44-46

regions. Individual semiconductor structures may be formed by etching through portions of the doped stack to electrically isolate those structures. These structures may be fitted with

EX1001, 4:62-64

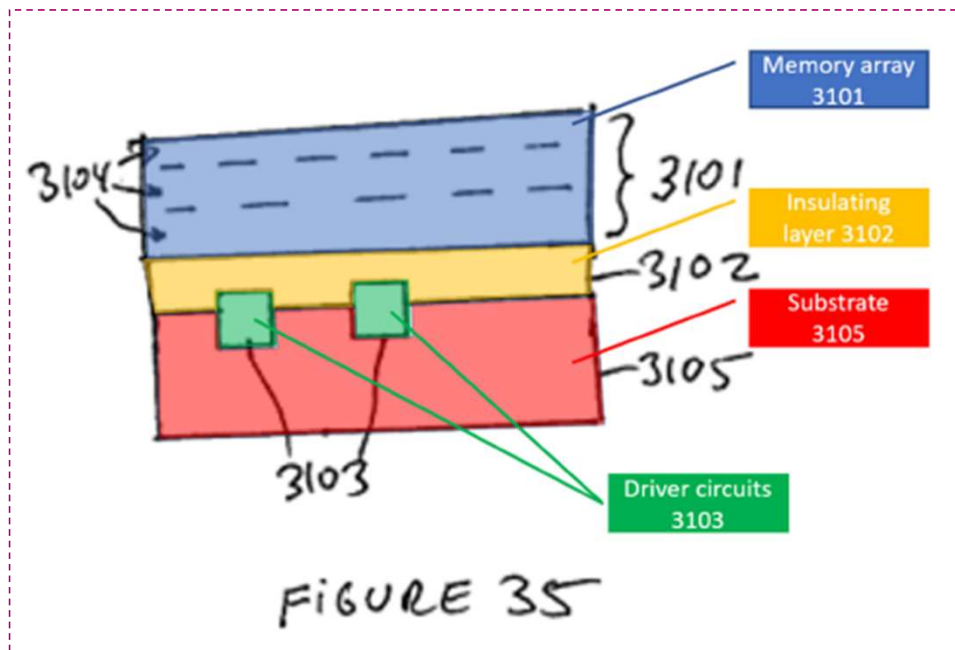
tric material. In this way, the stackable add-on layer may provide a plurality of memory cells suitable for connections to an underlying substrate.

EX1001, 5:5-7

Pet., 13-14; EX1003, ¶¶ 87, 90-91; Reply, 3
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Lee + Aspar/Kim – claims 13-15

Under Board / Intel construction, Lee teaches all limitations of claim 13 except “stackable add-on layer”

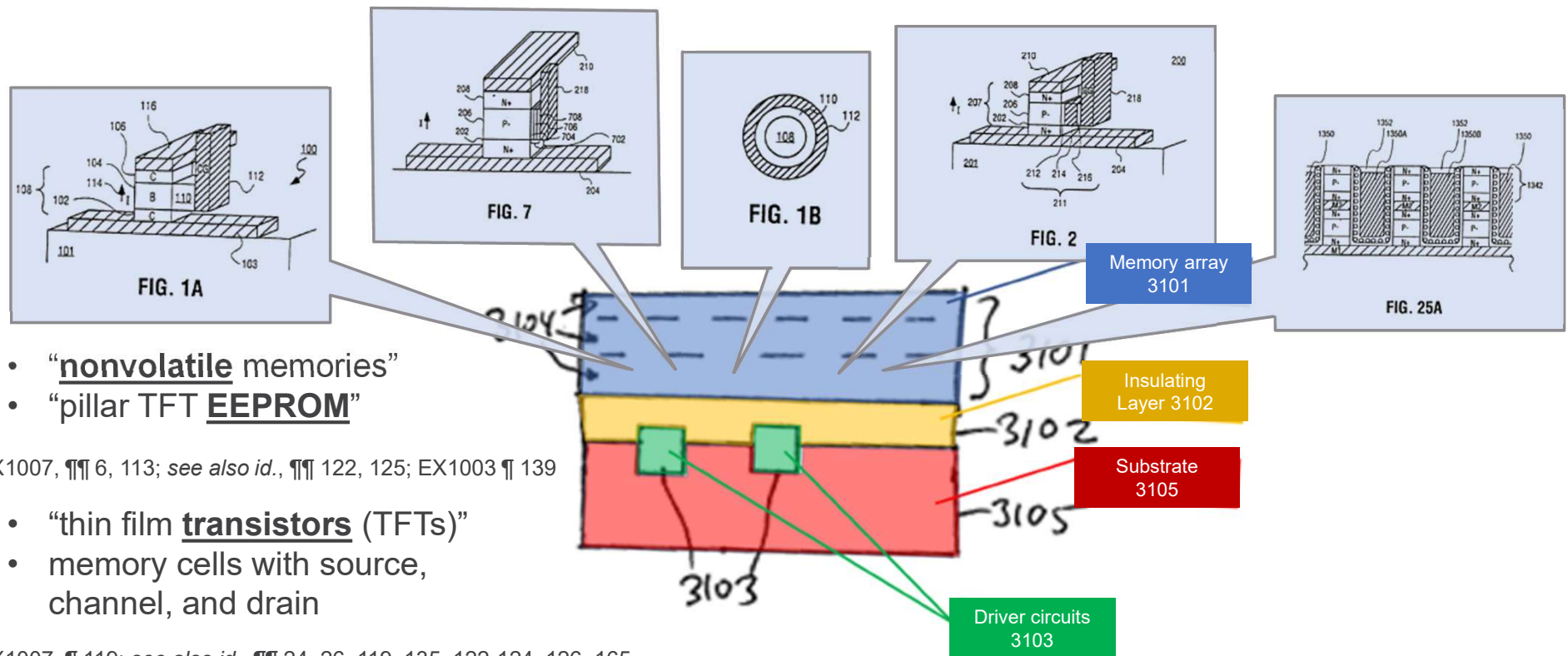


Pet., 19; EX1007, Fig. 35

13. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
the stackable add-on layer being bonded to the dielectric layer; and
wherein the memory cells are nonvolatile memory cells having at least one transistor.

EX1001, claim 13

Lee discloses many transistor-based nonvolatile memory cells for potential use in Figure 35's memory array



- “nonvolatile memories”
- “pillar TFT EEPROM”

EX1007, ¶¶ 6, 113; see also *id.*, ¶¶ 122, 125; EX1003 ¶ 139

- “thin film transistors (TFTs)”
- memory cells with source, channel, and drain

EX1007, ¶ 119; see also *id.*, ¶¶ 24, 26, 119, 135, 122-124, 126, 165

Pet., 19; EX1007, Figs. 1A, 1B, 2, 7, 25A, 35

Pet., 17-31; EX1003, ¶¶ 112-139
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Aspar discloses a Smart-Cut process to bond a stackable add-on layer

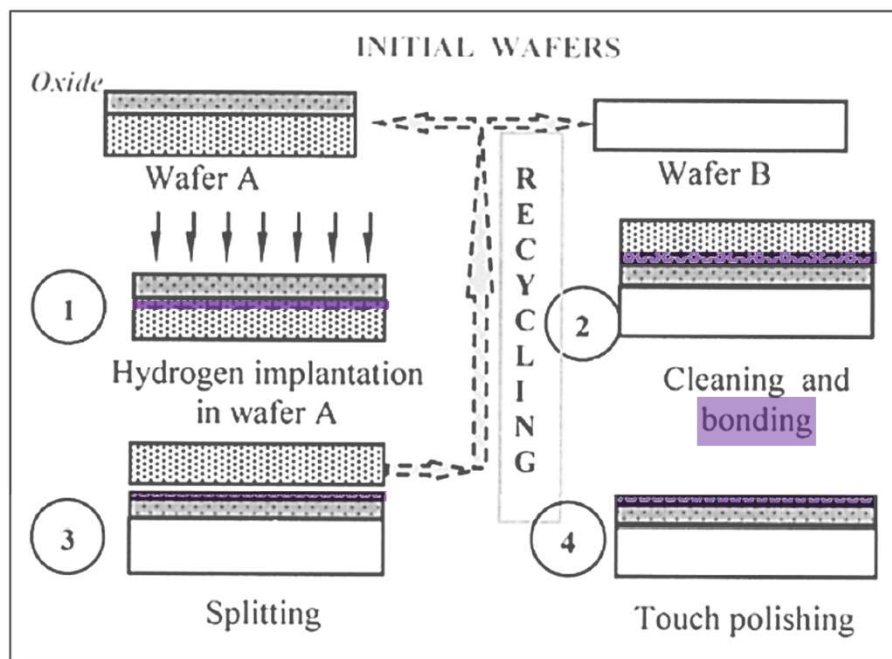


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

EX1009, Fig. 1 (annotated)

13. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
the stackable add-on layer being bonded to the dielectric layer; and
wherein the memory cells are nonvolatile memory cells having at least one transistor.

EX1001, claim 13

The '702 patent discloses using the prior art Smart-Cut process for bonding

This is a continuation-in-part of application Ser. No. 10/873,969, entitled "Three-Dimensional Integrated Circuit Structure and Method of Making Same", filed 21 Jun. 2004; and which is incorporated in its entirety herein by reference.

EX1001, 1:7-10

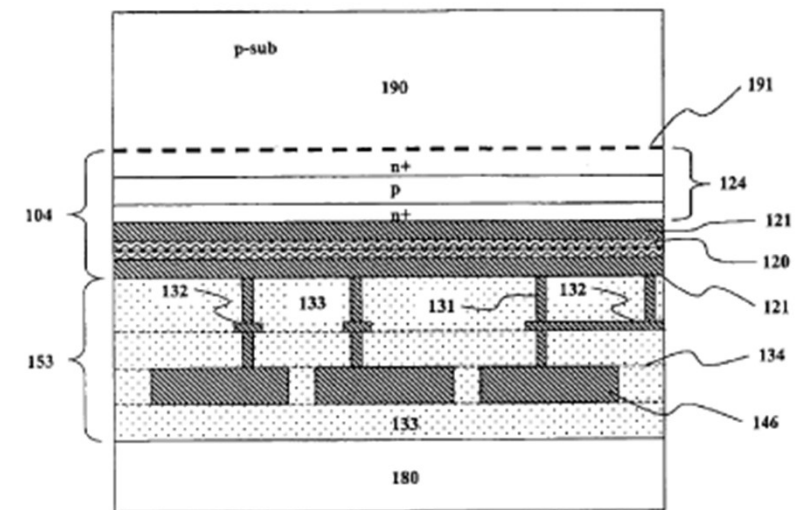
(10) **Patent No.:** **US 7,052,941 B2**

(21) Appl. No.: 10/873,969

EX1005, (10), (21)

SOI substrate **190** may have a detach layer **191**, which may be a porous or strained layer at a certain desired depth using, for example, SmartCut (U.S. Pat. No. 5,882,987), ELTRAN (U.S. Pat. No. 5,371,037), or SiGen technologies. Detach layer **191** is a defective region in the semiconductor lattice and, after bonding with dielectric layer **153**, SOI substrate **190** will be removed except for single crystal layer **124** which forms the FLD.

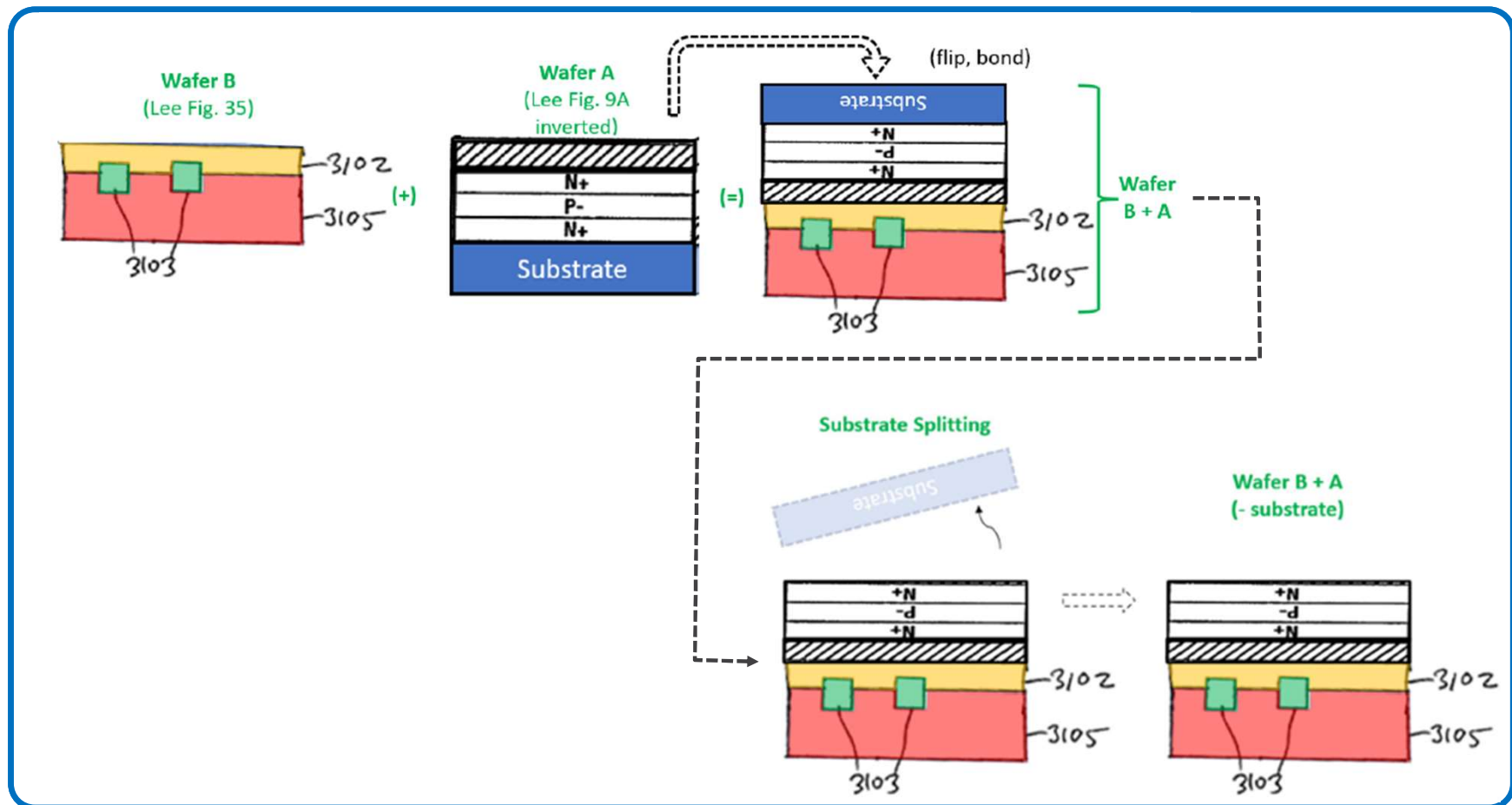
EX1005, 9:40-47, Fig. 4B



EX1005, Fig. 4C

Pet., 4-8, 11-12; EX1003, ¶¶ 59-65, 74; Reply, 12-13
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

A POSITA would have used Aspar's Smart-Cut process to fabricate Lee's memory structures



Pet., 58-60, EX1003, ¶¶ 209-211
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

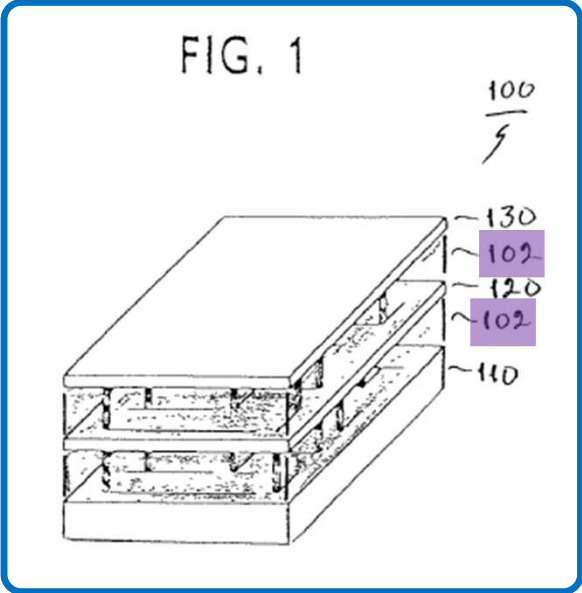
Kim discloses bonding a stackable add-on layer

a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
the stackable add-on layer being bonded to the dielectric layer; and

EX1001, claim 13

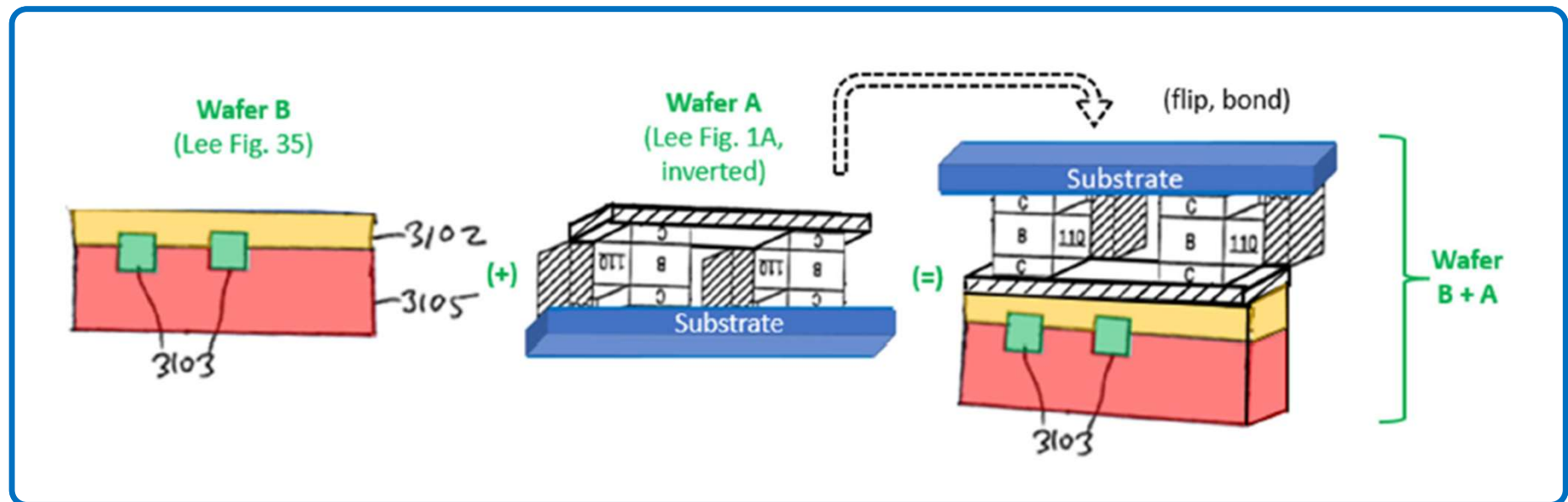
[0020] Attention now is directed to the drawings and particularly to FIG. 1, an example three-dimensional (3-D) wafer-to-wafer vertical stack is illustrated. As shown in FIG. 1, the 3-D vertical stack (chip) 100 may comprise any number of active device polysilicon (Si) wafers, such as wafer #1 110 including, for example, one or more microprocessors; wafer #2 120 including one or more memory devices; and wafer #3 130 including one or more radio-frequency (RF) or optical communication devices. Typically, a dielectric layer 102 is used to bond the active device wafers 110, 120 and 130.

EX1008, ¶ 20



EX1008, Fig. 1 (annotated)

A POSITA would have used Kim's bonding technique to manufacture Lee's memory structures



A POSITA would have combined Lee and Aspar/Kim for several reasons

Motivation to Combine	Support
Aspar's Smart-Cut transferred high-quality crystalline silicon and allowed for easy transfer of multiple layers (Lee + Aspar only)	Pet., 60-61 (citing EX1009, 834, 839; EX1003, ¶ 212) Reply, 6, 10 (additionally citing EX1037 ¶¶ 13, 24)
Bonding was a known technique that addressed a known problem using prior art elements according to their established functions	Pet., 53, 60-61 (citing EX1003, ¶¶ 195, 212) Reply, 5-6 (citing Pet., 53, 60-61)
Lee's Figure 35 lacks implementation details that a POSITA would have sought elsewhere, and Lee discloses stacking in other embodiments	Pet., 51-52, 56 (citing EX1007, ¶¶ 107-113; EX1003, ¶¶ 190-192, 204) Reply, 6-8 (additionally citing EX1007, ¶¶ 115, 117, 207-212, 259, 294; EX1037, ¶¶ 14-17; EX2029, 61:12-22)
The combinations would have improved quality control and reduced waste	Pet., 53-54, 61-62 (citing EX1003, ¶¶ 196, 213) Reply, 8-10 (additionally citing EX1016, 1:48-52; 1055, 943; EX1057, 1:14-18, 2:7-23; EX1047, 295; EX1041, 228; EX1043, 10-11; EX1037, ¶¶ 18-21)
The combinations would have allowed fabricating devices separately using optimized processing before bonding	Pet., 53-54, 61-62 (citing EX1003, ¶¶ 196, 213) Reply, 10 (additionally citing EX1016, 1:25-27; EX1008, ¶ 22; EX1044, 145-146; EX1049, 6:42-56; EX1050, 525; EX1037, ¶¶ 22-24; EX2039, 91:17-98:9)

Aspar describes benefits that would have motivated a POSITA to use its techniques

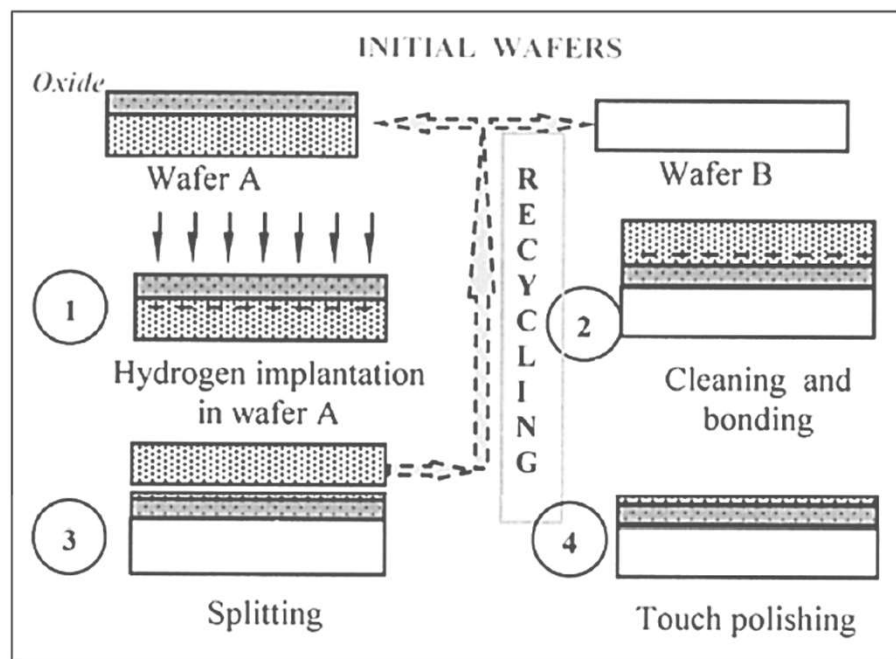


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

EX1009, 835

This process has several advantages from both the technical and economic points of view.⁷ Among these, the possibility of transferring thin layers of very good thickness homogeneity and with a high crystalline quality onto different materials deserves to be highlighted. From an economic point of view, the possibil-

EX1009, 834

complex structures. For example, this layer transfer process can be repeated several times on a same structure. Realizing multiple SOI layers based on a layer transfer process can be achieved in many different ways: repeating a single layer transfer several times onto a same wafer, transferring SOI layers stacks already formed onto a single substrate or a SOI wafer. So, multiple SOI layers stacks can be easily performed thanks to Smart-Cut technology (Fig. 14).¹⁹

EX1009, 839

Intel need only show that bonding is a suitable option, not an improvement



“And if there’s a **known technique** to address a **known problem** using ‘**prior art elements according to their established functions**,’ then there is a motivation to combine. ...

And contrary to the Board’s suggestion, **Intel never had to show** that replacing Kabemoto’s secondary cache with Bauman’s secondary cache was an ‘**improvement**’ in a categorical sense. See *Final Written Decision*, 2021 WL 3503434, at *11. Intel just had to show that Bauman’s secondary cache was a “**suitable option**” to replace Kabemoto’s secondary cache. *Intel [Corp. v. Qualcomm Inc.]*, 21 F.4th [784,] at 800 [(Fed. Cir. 2021)](emphasis omitted).”

Intel Corp. v. PACT XPP Schweiz AG, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023) (emphasis added)

“Consistent with our recent decision in *Intel [v. PACT]*, the Board should have addressed whether Cisco showed a motivation to combine Gleichauf with Lewis **independent of whether a skilled artisan would recognize any benefit** in making the proposed combination.”

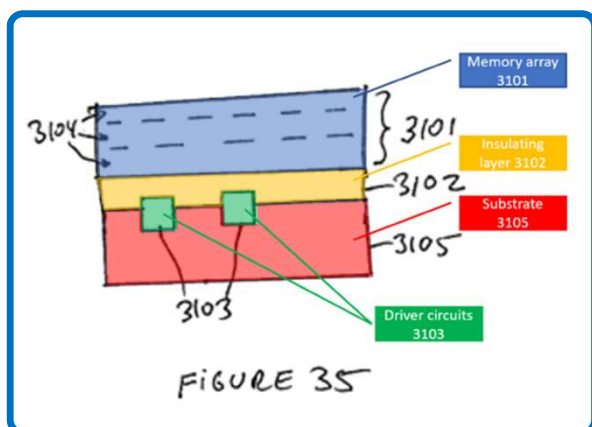
Cisco Sys., Inc. v. K.Mizra LLC, Nos. 2022-2290, 2023-1183, 2024 WL 3841809, *4 (Fed. Cir. Aug. 16, 2024) (emphasis added)

Pet., 48, 53, 61, 76, 81, 84; EX1003, ¶¶ 180, 194-196, 212-213, 249-250, 260-261, 267-269; Reply, 5-6; EX1037, ¶¶ 13-14

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Bonding was a known solution to known problems using prior art elements based on established functions

Fabricating 3D structures (Lee, Aspar) and memory arrays above a substrate containing electrical devices (Lee, Kim) were known problems. Aspar and Kim describe bonding as a known solution.



Pet., 19; EX1007, Fig. 35

[0111] FIG. 35 schematically illustrates an array of charge storage logic or memory devices 3101 formed above an interlayer insulating layer 3102 disposed above a monocrystalline substrate 3105. The array of charge storage logic

EX1007, ¶ 111

substrate. Wafer bonding and layer transfer enable different materials to be associated to form multi-layer substrates. This is particularly advantageous

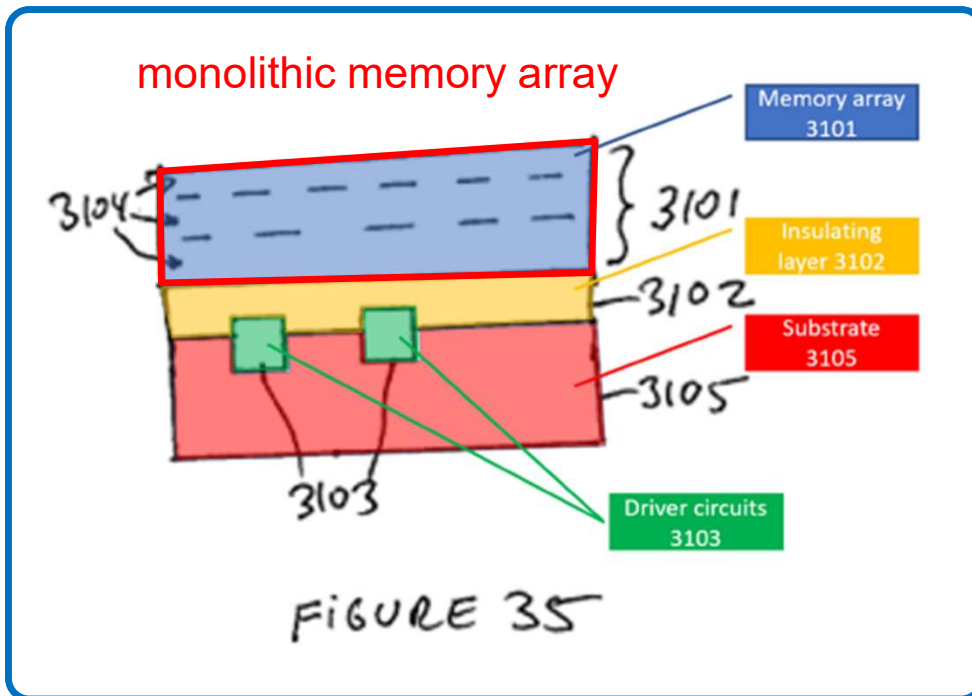
EX1009, 834

[0020] Attention now is directed to the drawings and particularly to FIG. 1, an example three-dimensional (3-D) wafer-to-wafer vertical stack is illustrated. As shown in FIG. 1, the 3-D vertical stack (chip) 100 may comprise any number of active device polysilicon (Si) wafers, such as wafer #1 110 including, for example, one or more microprocessors; wafer #2 120 including one or more memory devices; and wafer #3 130 including one or more radio-frequency (RF) or optical communication devices. Typically, a dielectric layer 102 is used to bond the active device wafers 110, 120 and 130.

EX1008, ¶ 20

Pet., 17-21, 28, 51-53, 56-61; EX1003, ¶¶ 112-124, 133, 189-195, 203-212; Reply, 5-6
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Lee describes a monolithic memory array in which array layers are deposited on other array layers



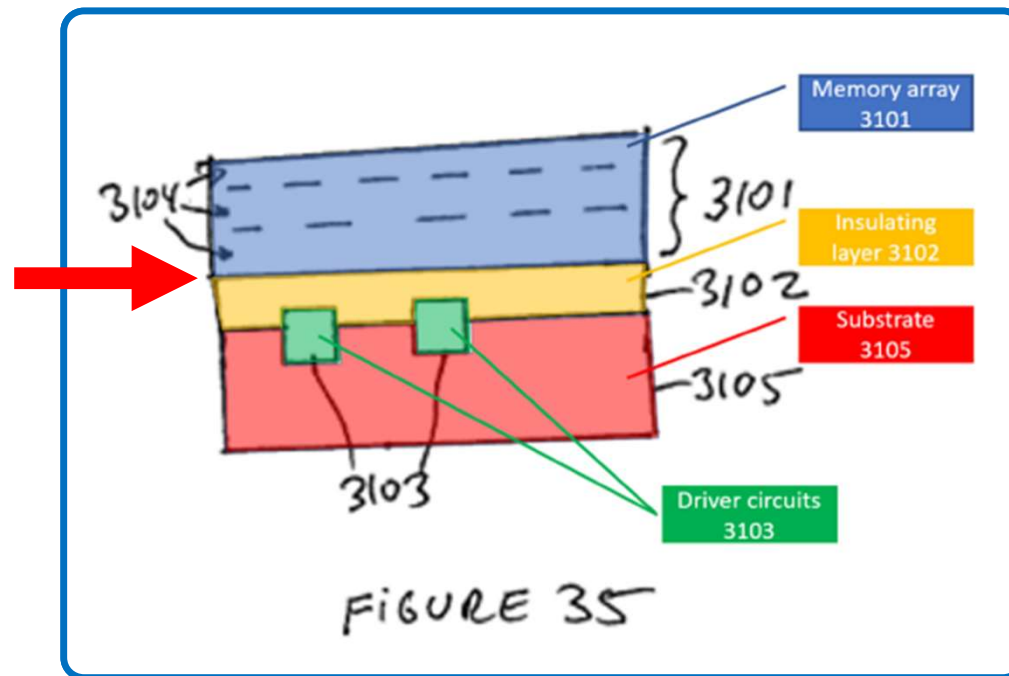
[0107] One method of improving device density is to arrange the devices in a **monolithic** three dimensional array of charge storage devices comprising a plurality of device levels. The term “monolithic” means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

EX1007, ¶ 107

Pet., 19 (annotated); EX1007, Fig. 35

Pet., 51-52, 56; EX1003 ¶¶ 191-192, 204; Reply, 6-7; EX1037, ¶¶ 14-15
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

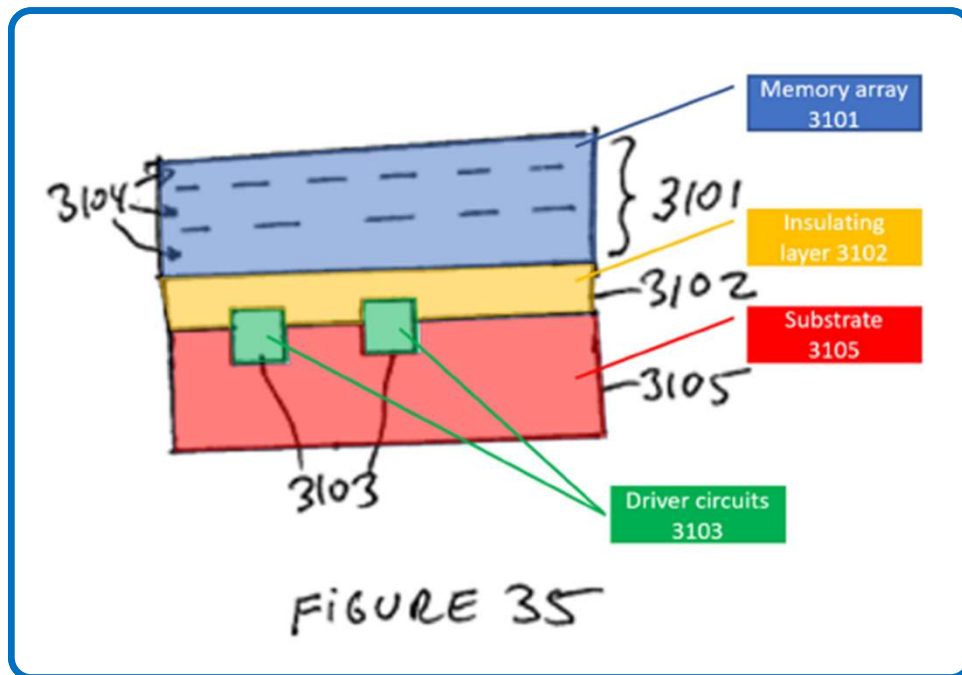
Lee's Figure 35 lacks details about attaching the bottom of the monolithic memory array to the substrate



Pet., 19 (annotated); EX1007, Fig. 35

Pet., 51-52, 56; EX1003 ¶¶ 191-192, 204; Reply, 6-7; EX1037, ¶¶ 14-15
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Lee discloses bonding and a POSITA would have considered the technique for attaching the bottom of the memory array



Pet., 19; EX1007, Fig. 35

[0107] One method of improving device density is to arrange the devices in a monolithic three dimensional array of charge storage devices comprising a plurality of device levels. The term “monolithic” means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

EX1007, ¶ 107

ceramic substrate. The silicon-on-insulator substrate may be formed by any conventional method, such as wafer bonding, Separation by Implantation of Oxygen (SIMOX), and formation of an insulating layer on a silicon substrate. After the

EX1007, ¶ 208

Density and cost benefits of monolithic memory arrays would have applied when bonding was used

stacked wafers. Prelim. Resp. 39. Nevertheless, there remains a fact issue as to whether Petitioner's asserted benefit would have outweighed the competing benefits of improved density and lowered costs of monolithic arrays identified in Lee (Ex. 1007 ¶¶ 106–107). This issue is best resolved

DI, 36

and decreases die size and cost. Furthermore, by optionally stacking the cells vertically in the Z-direction, the array density is further increased, which leads to further decreases in the die size and cost.

EX1007, ¶ 204

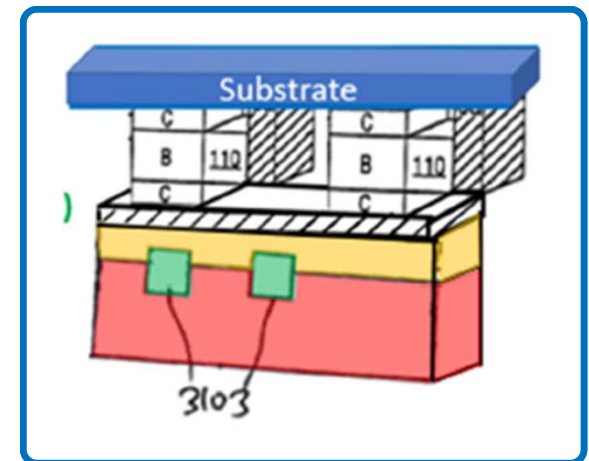
ceramic substrate. The silicon-on-insulator substrate may be formed by any conventional method, such as wafer bonding, Separation by Implantation of Oxygen (SIMOX), and formation of an insulating layer on a silicon substrate. After the

EX1007, ¶ 208

Lee teaches implementations that include bonding, increase density, and decrease cost

Reply, 7-9, 12; EX1037, ¶¶ 16-17, 28
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Intel's combinations result in the same memory array structure as Lee



Pet., 52

[0169] The above described processes can be repeated as many times as desired to add additional levels of pillar memory to the array. The final level of memory cells can be

EX1007, ¶ 169

BeSang ignores evidence confirming that testing improves yield

Since the chips in each wafer are tested to screen out defective ones, one must stack only good chips on top of good chips on a wafer to maintain a reasonable yield. If there is no yield loss during the stacking process, the final yield will coincide with the original wafer yield. In as much as one

EX1016, 1:48-52

We adopt an “assembly” approach to 3D circuit fabrication [5] in which we begin with multiple completed 2D circuits fabricated by conventional means and individually tested, and then stack the device layers using wafer bonding. We believe this approach should improve yield and reduce manufacturing cost compared to “bottom up” techniques in which devices in each layer are processed sequentially.

EX1055, 943

(e.g., testing for shorts) prior to bonding. If a quality issue is detected, then only that level 3104 would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited layer stacks, etc.) would need to be discarded. Testing layers of devices

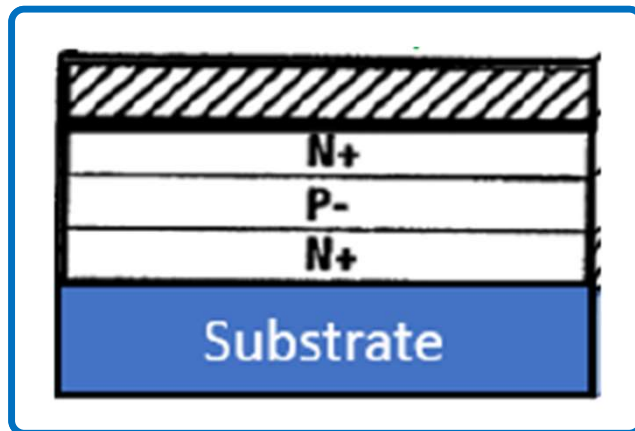
EX1003, ¶ 196

Pet., 53-54, 61-62; EX1003, ¶¶ 196, 213; Reply, 8-9; EX1037, ¶¶ 18-20
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

A POSITA would have tested layers in the Lee-Aspar combination before bonding

quality control at the layer formation stage. Specifically, when using Smart-Cut®, quality control can be performed on the stack prior to bonding (e.g., layer thickness, uniformity, etc.). If a quality issue is detected, then only that stack would need to be

EX1003, ¶ 213



Abstract—Semiconductor fabrication requires tight specification limits on thickness and resistivity for epitaxially deposited silicon films. Our testbed system for integrated, model-based, run-to-run control of epi films incorporates a Centura tool with an epi deposition chamber, an in-line epi film thickness measurement tool, and off-line thickness and resistivity measurement systems.

EX1047, 295

which then impinges upon the wafer. A sensor in the probe assembly measures the surface photovoltage induced by the modulated light. The signal from the sensor is sent to a computer which then uses the induced surface photovoltage to determine various electrical characteristics of the wafer, such as surface charge and surface doping concentration, among others.

Objective evidence supports Dr. Sechen's opinions on process optimization

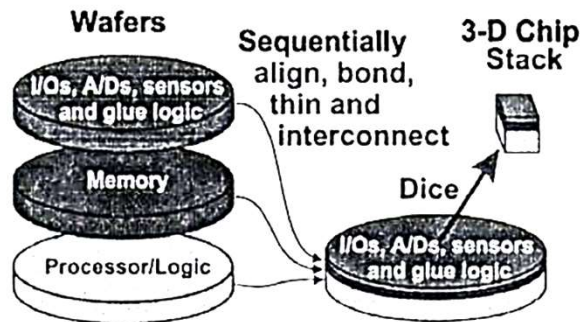
related to the materials used. Furthermore, the processes involved in forming successively devices can affect the characteristics of devices placed underneath it. In addition,

EX1016, 1:25-27

a faster signal and minimal interconnect RC delays. In addition, the vertical stack can effectively integrate diverse process technologies on a single wafer process, such as, for example, logic/memory stacking, processor stacking, optical interconnect, system-on-chip, and RF interconnect.

EX1008, ¶ 22

integration to increase both the performance and functionality. The use of optimized processing technology on separate wafers for implementations of ASICs/SOCs or heterogeneous systems also offers the potential of reducing processing complexity, increasing the yield and cutting the packaging steps, thus lowering the overall cost.

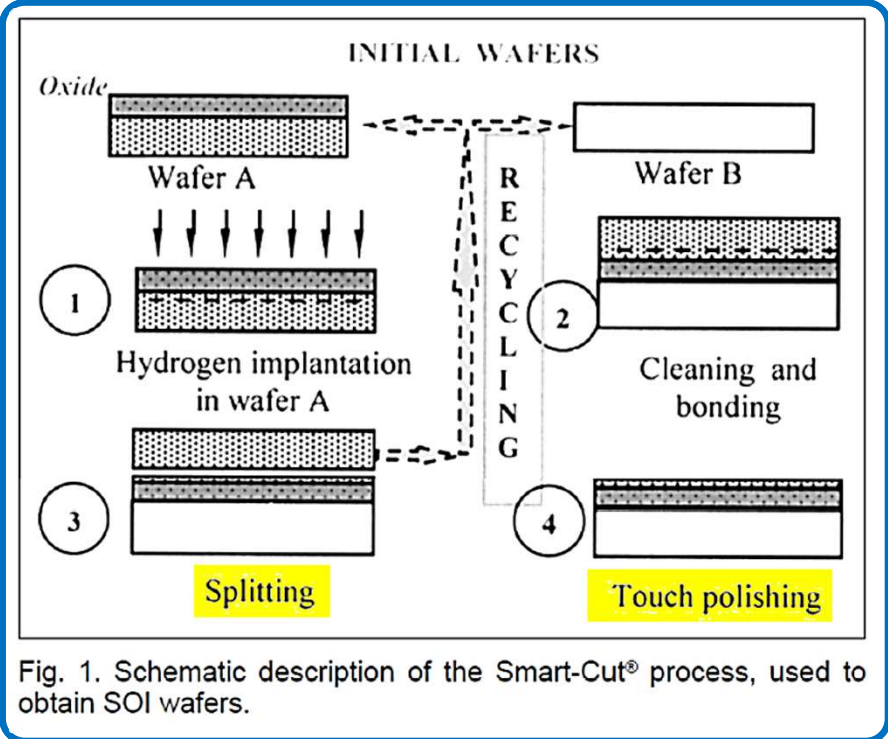


EX1044, 146

efficient of resistance measurements of thin-film materials. One of the main advantages of the new transfer bonding technology is that transducers and integrated circuits can be independently processed and optimized on different wafers before integrating the transducers on the integrated circuit wafer. Thus, the transducers can be made of, e.g., monocrystalline silicon or other high-temperature annealed, high-performance materials. Wafer-level transfer

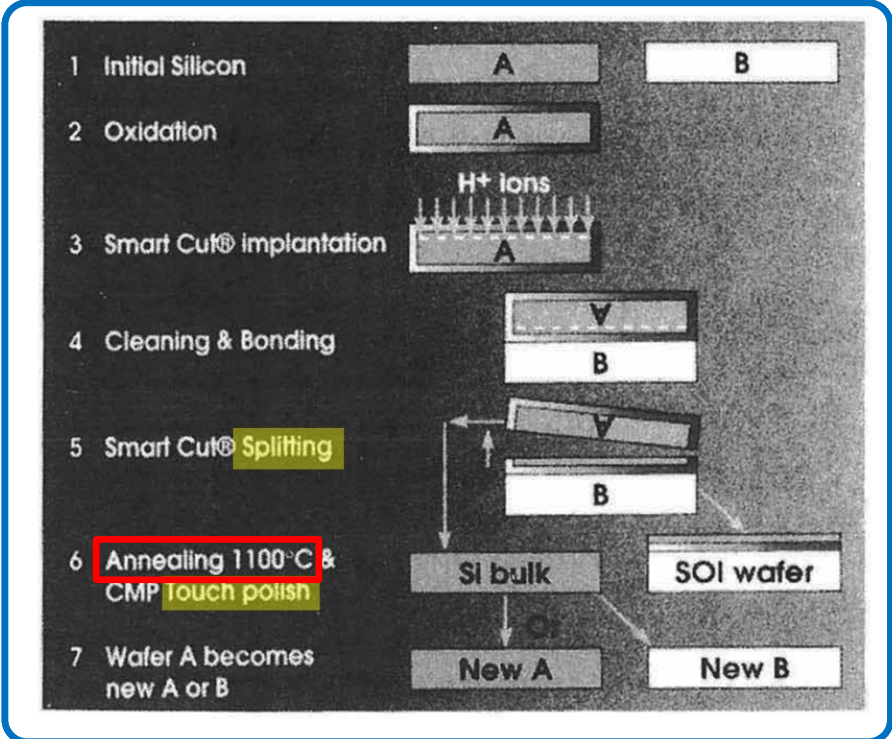
EX1050, 525

Aspar and Wolf describe different Smart-Cut processes



EX1009, Fig. 1 (annotated)

No anneal between splitting and polishing



EX1015, 543 (annotated)

1100°C anneal between splitting and polishing

Smart-Cut is a generic process, and Dr. Sechen distinguished Aspar's version from Wolf's

Based on these results, we can conclude that the Smart-Cut process really is a generic process. It allows a great deal of combinations (material and bonding layer) which open up new scope for developments.

EX1009, 839

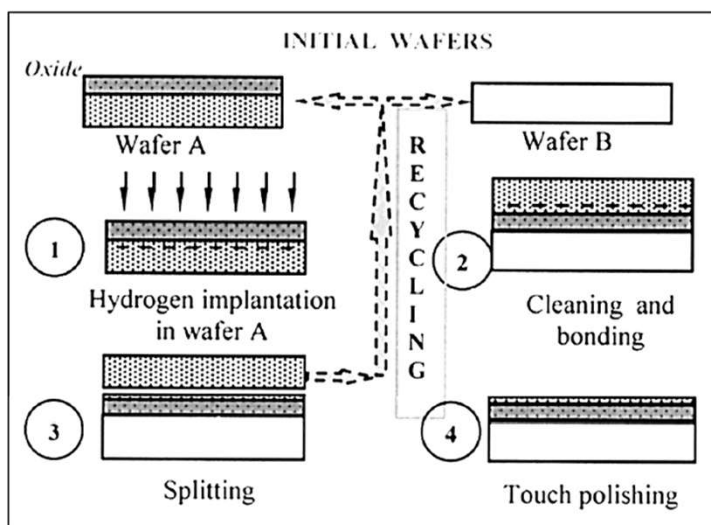


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

EX1009, 835

Aspar's Smart-Cut® process

EX1003, ¶¶ 209, 212-214, 217, 219, 257, 260-262

Wolf

Q. Okay. And it specifically suggests that it should be annealed at 1100-degree Celsius to correct those defects; correct?

A. That is this one article's opinion, yes.

EX2039, 120:18-22

Like Aspar, the incorporated '941 patent describes Smart-Cut without an 1100°C annealing step

SOI substrate **190** may have a detach layer **191**, which may be a porous or strained layer at a certain desired depth using, for example, **SmartCut** (U.S. Pat. No. 5,882,987), ELTRAN (U.S. Pat. No. 5,371,037), or SiGen technologies. Detach layer **191** is a defective region in the semiconductor lattice and, after bonding with dielectric layer **153**, SOI substrate **190** will be removed except for single crystal layer **124** which forms the FLD.

EX1005, 9:40-47

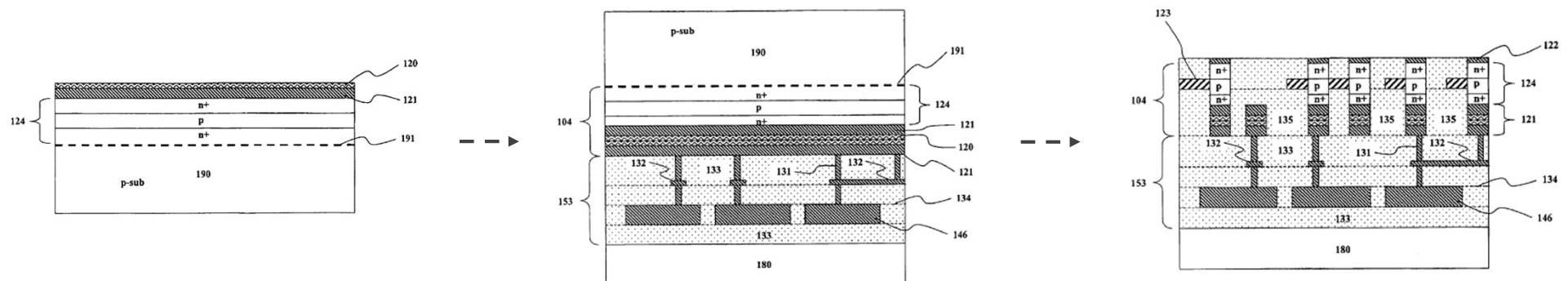
shown as dashed lines **134**. Base substrate **180** should withstand semiconductor processing temperatures in the range of **250° C.~650° C.** The conductors are formed of low

EX1005, 8:60-62

No anneal between splitting and polishing

side. Once the SOI substrate has been **detached**, Chemical-Mechanical **Polishing** (CMP) could be used to reduce surface roughness of the transferred SOI layer.

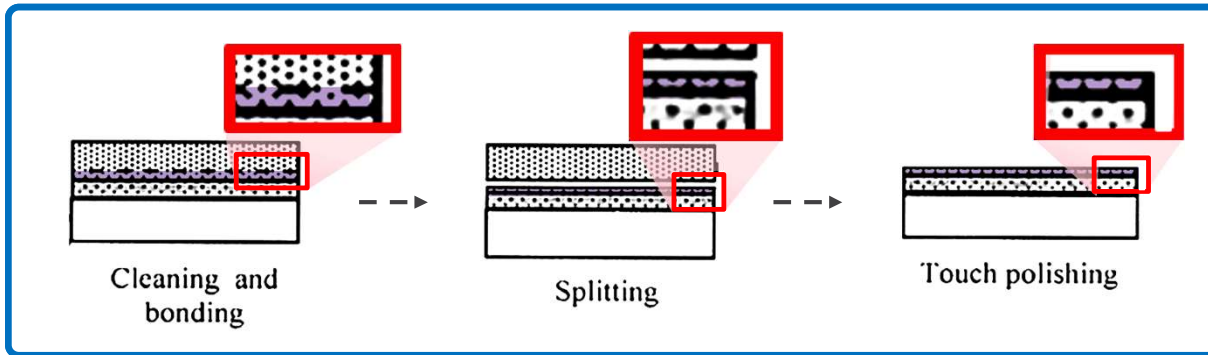
EX1005, 10:19-21



Pet., 11-12; EX1003, ¶¶ 74, 79-81; Reply, 12-13; EX1037, ¶¶ 29-31
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

EX1005, Fig. 4B-4D

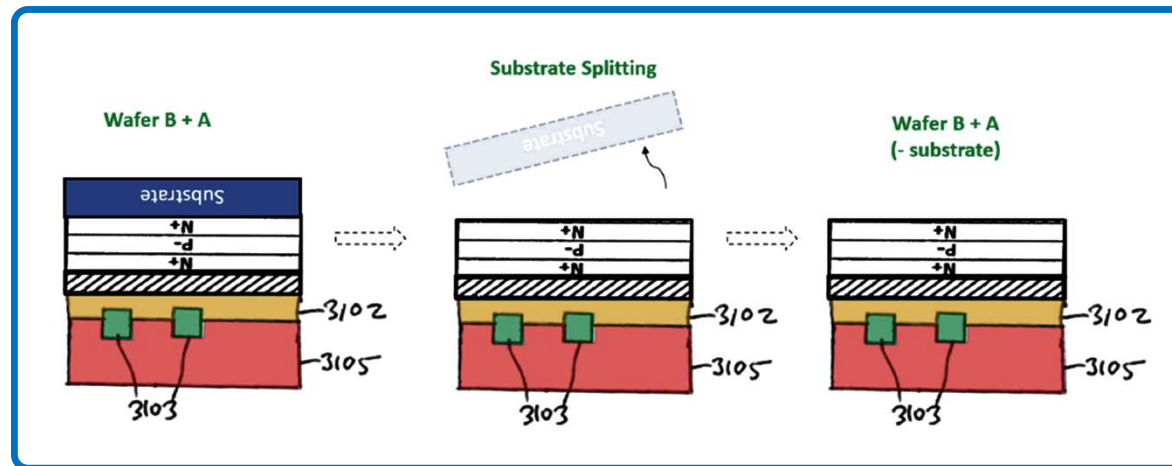
The thin layer created by Aspar's splitting step is the "stackable add-on layer" used to form memory cells



A splitting step, which takes place along the in-depth weakened layer, gives rise to transfer of a thin layer from the substrate A onto the support B.

EX1009, 834

EX1009, Fig. 1 (annotated)



Pet., 56-63; EX1003, ¶¶ 205-215; Reply, 14; EX1037, ¶¶ 33-34
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

A POSITA would have had a reasonable expectation of success in combining Lee and Aspar/Kim

Aspar

structure. Realizing multiple SOI layers based on a layer transfer process can be achieved in many different ways: repeating a single layer transfer several times onto a same wafer, transferring SOI layers stacks already formed onto a single substrate or a SOI wafer. So, multiple SOI layers stacks can be easily performed thanks to Smart-Cut technology (Fig. 14).¹⁹

split after hydrogen implantation. The ability to obtain thin films by means of the layer transfer process combined with specific bonding via thermally conductive or metallic layers has also been demonstrated. In this paper, we focused essentially on ho-

EX1009, 839

- **suitable** for use with Lee's substrate
- **compatible** with Lee's use of thin films to fabricate memory cells

Kim

[0019] The present invention is applicable for use with all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, MOS transistors, CMOS devices, MOSFETs, and new memory devices and communication devices such as smart card, cellular phone, electronic tags, gaming devices which may become available as semiconductor technology develops in the future. However,

EX1008, ¶¶ 19-20

- a **predictable** way to achieve 3D structure
- **within the skill** of a POSITA

Intel explained how Lee and Aspar rendered an “SOI pillar” obvious under the Board / Intel construction

construction Petitioner does not support and we do not adopt. In addition, Petitioner does not appear to explain how the combination of Lee and Aspar would have resulted in an “SOI pillar” under Petitioner’s construction for that term.

DI, 42

Petitioner contends the term “SOI pillar” in claims 14–17 “requires a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology.” Pet. 13. Petitioner provides intrinsic record

DI, 12

VII.A.2-VII.A.5. Additionally, Section VII.E.1.b describes that the stackable add-on layer is added using Aspar’s Smart-Cut® process which is SOI technology. EX1009, 834, 837 (“major application of this process is...fabrication SOI wafers”), 839. As described in that Section, the doped stack of the stackable add-on layer bonded to Wafer B is used to form pillars (“SOI pillars”) for the memory cell structures of Lee’s Figure 1A–1B, 2, 7, or 25A. Sechen, ¶217.

Pet., 63

above the substrate. *Id.* Wafer A would be separately fabricated with a single crystal surface layer with a doped stack, similar to stack 902 depicted in Lee’s Figure 9A to form the pillars for the memory cell structures of Figs. 1A–1B, 2, 7, and 25A. *Id.*; EX1007, ¶¶119, 122, 125, 138–141; *see also id.*, Fig. 13A, ¶¶147–148; Fn. 9. A

Pet., 59

pillar-shaped	✓
doped stacked structure	✓
stackable add-on layer	✓
SOI technology	✓

Intel primarily relies on Lee's embodiments other than the one shown in Figure 25A

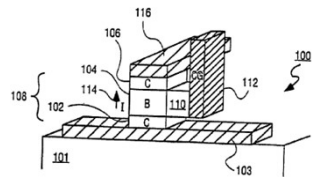


FIG. 1A

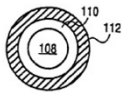


FIG. 1B

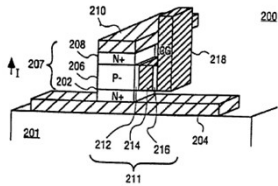


FIG. 2

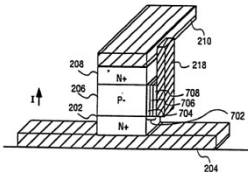


FIG. 7

Lee + Aspar/Kim

Claim	Lee embodiments	Support
13	Figs. 1A , 1B , 2 , 7 , 25A	Pet., 16-31, 50-54, 56-63
14	Fig. 2	Pet., 31-33, 54, 63
15	Figs. 1A , 1B , 7	Pet., 33-37, 54, 63
16-17	Fig. 25A	Pet., 37-41, 54, 63

Lee + Aspar/Kim + Endoh

Claim	Lee embodiments	Support
13-15	See above	See above
16-17	Fig. 1B (Intel also alternatively relies on Endoh's memory cells)	Pet., 47-50, 55, 64; Reply, 17-22

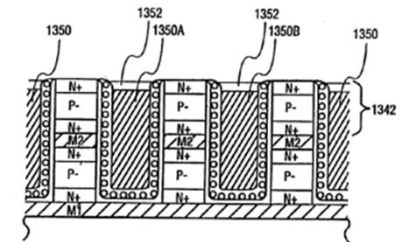


FIG. 25A

EX1007, Fig. 25A

EX1007, Figs. 1A, 1B, 2, 7

Reply, 11-12, 21-22; EX1037, ¶¶ 26-28, 46
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Lee + Aspar/Kim [+ Endoh] – claims 16-17

Lee discloses the “serially connected” nonvolatile memory cells of claim 16

16. The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

EX1001, claim 16

Level 2's memory cells. Without that upper conductor, the cells in Level 2 cannot be connected in parallel with the cells in Level 1 because they have only one electrical connection to the cells in Level 1. That sole connection between cells in Level 1 and Level 2 is through metal layer M2, and therefore, the memory cells are serially connected, one after another, as required by claims 16 and 17. Pet., 38-40.

EX1037, ¶ 38

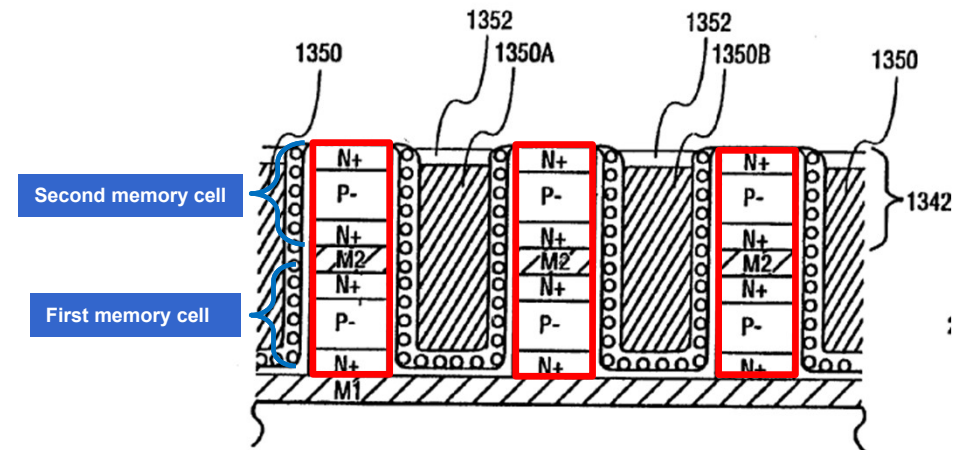


FIG. 25A

EX1007, Fig. 25A (annotated)

Lee discloses the “serially connected” nonvolatile memory cells of claim 17

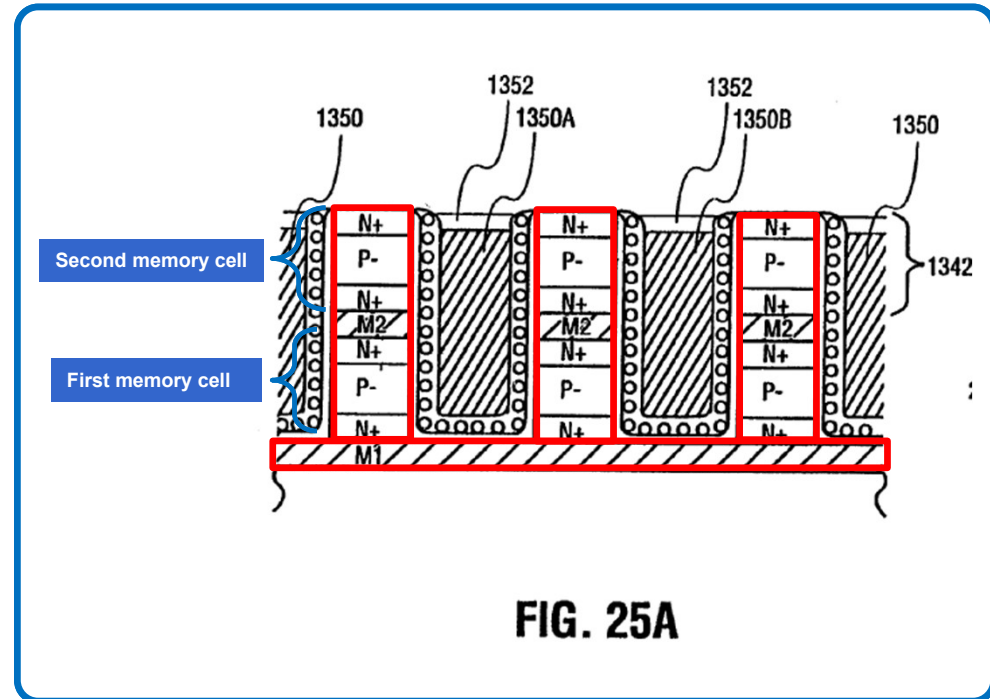
17. The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

EX1001, claim 17

“Memory cells” and “interconnect line” are separate

least two nonvolatile memory cells on the first SOI pillar.” Figure 25A further shows that those memory cells are serially connected to a conductive bitline or wordline M1 1308 (“interconnect line”) and M1 connects the first pillar to an adjacent pillar having a nonvolatile memory cell. Exhibit 1007, ¶¶148, 161, Fig. 25A. Further still,

EX1003, ¶ 164



EX1007, Fig. 25A (annotated)

Claims 16 and 17 require memory cell structure, not memory cell function

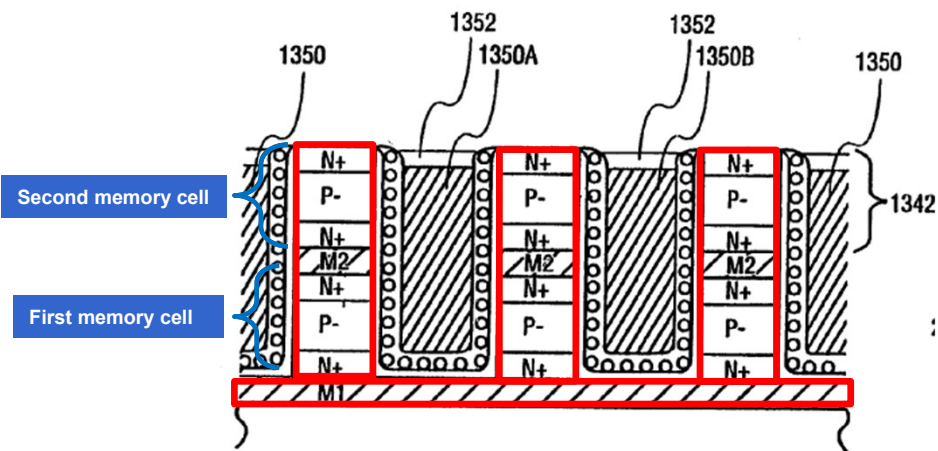


FIG. 25A

EX1007, Fig. 25A (annotated)

16. The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

17. The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

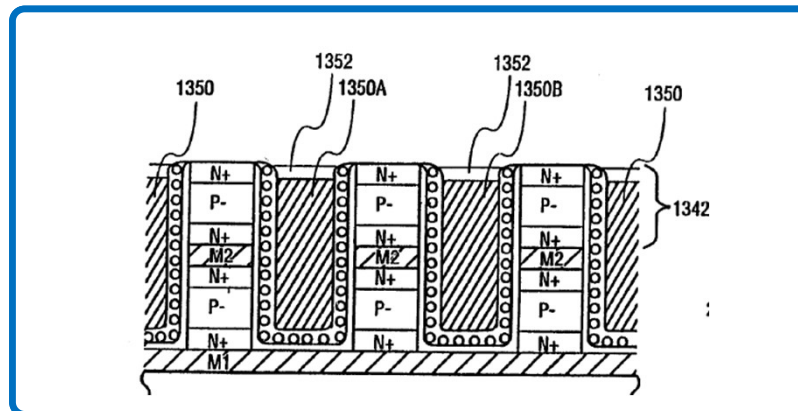
EX1007, claims 16-17

The intermediate step in Lee's prior art method renders the claimed memory structure unpatentable



"We also **do not find it material** that the district court found the anticipating method in the '211 patent to be 'an **intermediate step**' in the manufacture of sevoflurane. *Abbott*, No. 01-CV-1867, slip op. at 42. The product of that method was an anesthetic sevoflurane composition with sufficient water to prevent Lewis acid degradation—exactly what is claimed by the '176 patent. **Commercial finality is not claimed.**"

Abbott Labs. v. Baxter Pharm. Prods., Inc., 471 F.3d 1363, 1369 (Fed. Cir. 2006) (emphasis added)



EX1007, Fig. 25A

Reply, 16-17; EX1037, ¶¶ 37-39
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Endoh teaches “serially connected” non-volatile memory cells (claims 16-17)

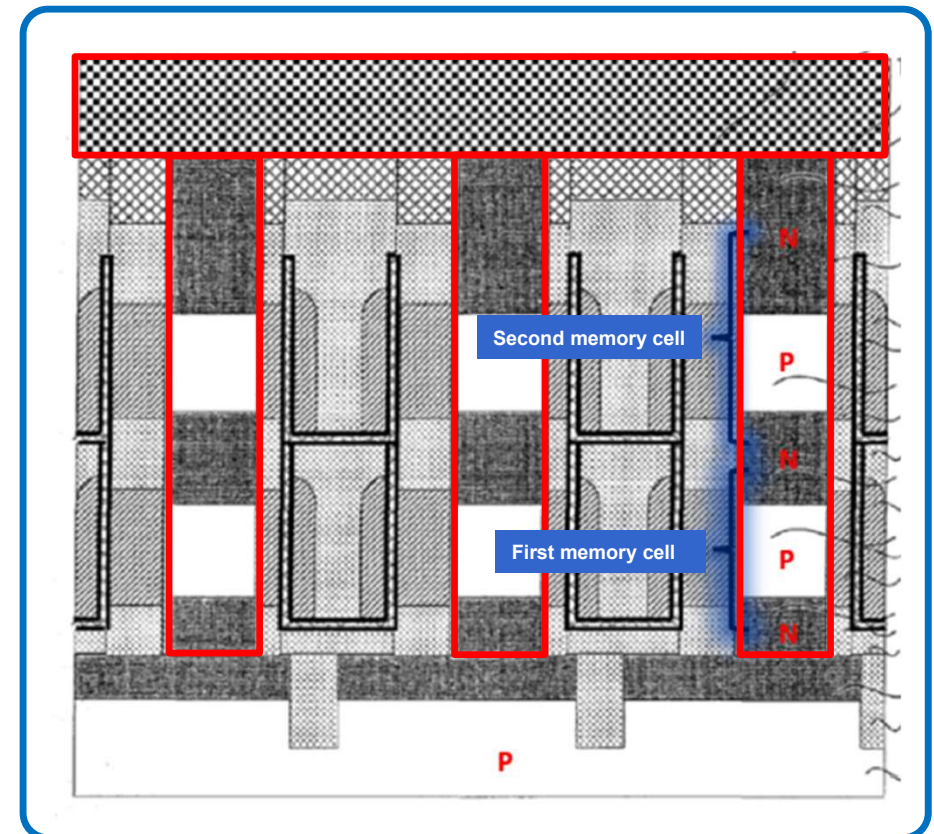
16. The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

17. The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

EX1001, claims 16-17

the transistors are connected in series along the island-like semiconductor layer, as shown in FIG. 1171 and FIG. 1172.

EX1012, ¶ 1206

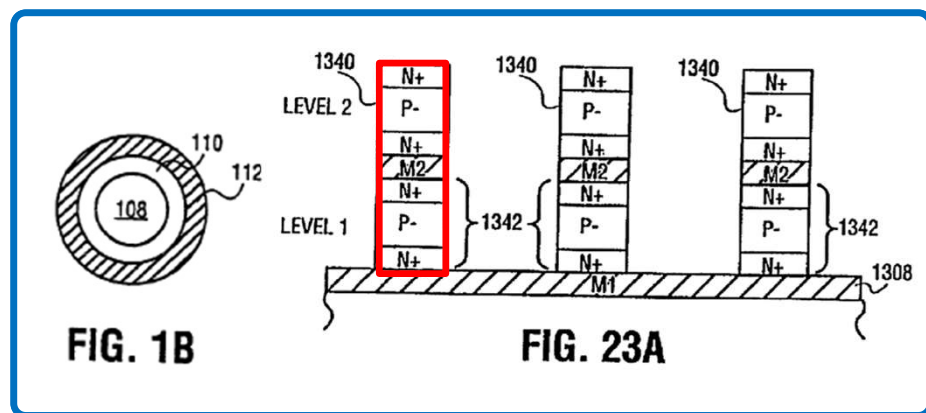


EX1012, Fig. 1172 (annotated)

Pet., 42-50, 55, 64; EX1003, ¶¶ 170-186, 200, 218-219
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

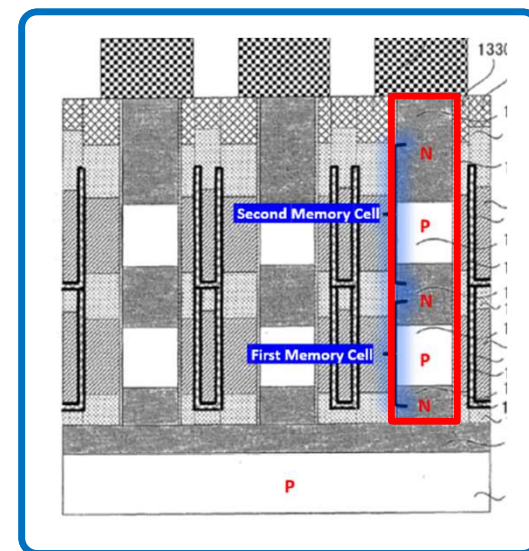
Based on Endoh, a POSITA would have used serially connected memory cells

Option 1: stack Lee's cylindrical memory cells



EX1007, Figs. 1B, 23A (annotated)

Option 2: implement Endoh's memory cells



EX1012, Fig. 1171 (annotated)

Motivations to combine / reasonable expectation of success:

- Increased device **density**
- Solving a **known problem** with a **known technique**
- Lee and Endoh both teach stacking memory cells (**predictable, within the skill in the art**)

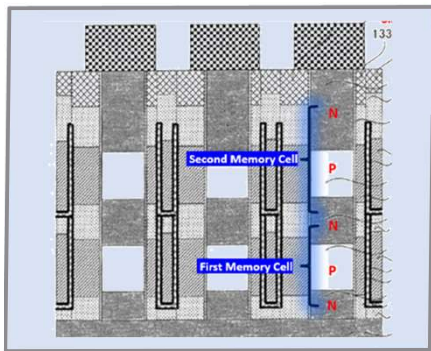
Lee suggests a POSITA would have implemented any memory structure, including Endoh's, in Lee's Figure 35 embodiment

[0113] The charge storage devices of the array may be any type of semiconductor devices which store charge, such as EPROMs or EEPROMs. In the preferred embodiments of

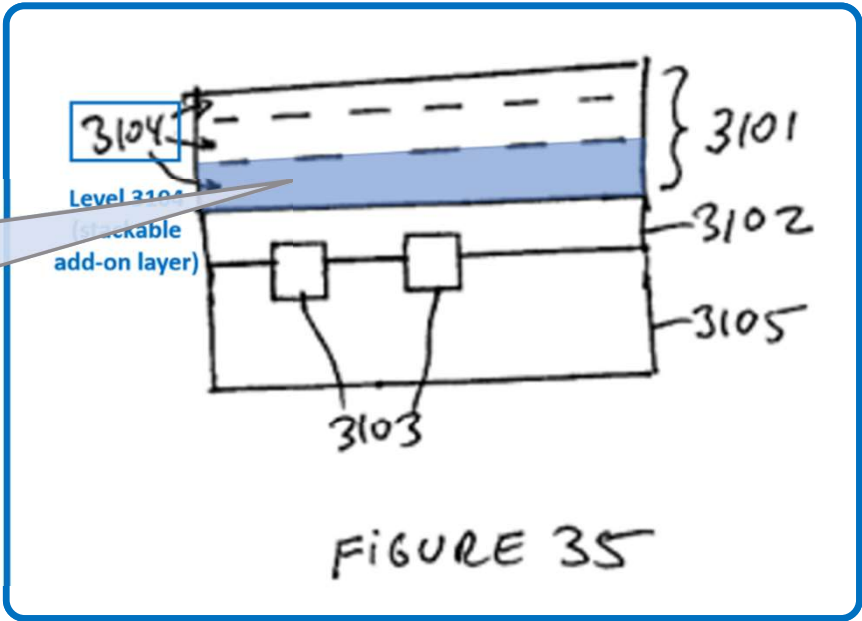
EX1007, ¶ 113

124. Figure 35 depicts level 3104 as a rectangular box (as shown above), and is agnostic as to the particular type or structure of the memory cells in it. Lee,

EX1003, ¶ 124; see also *id.*, ¶ 95



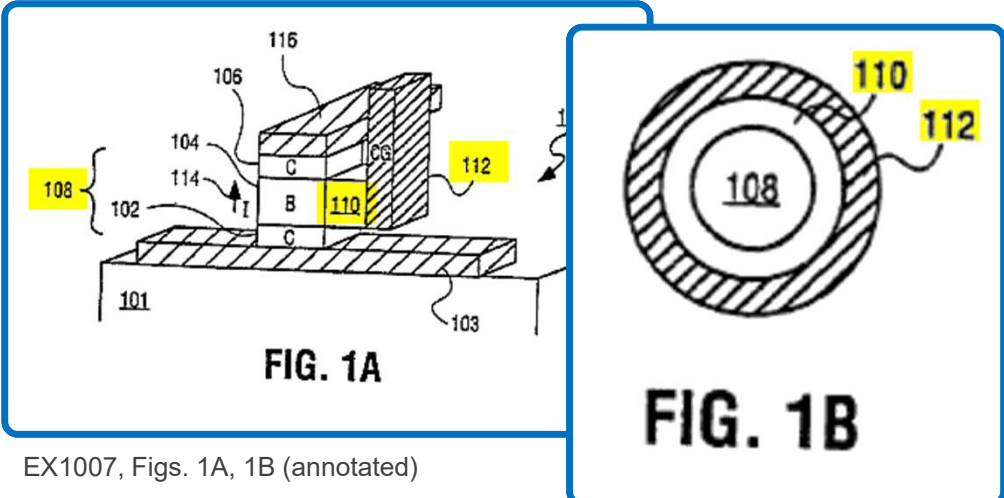
Pet., 44; EX1012, Fig. 1171



Pet., 21; EX1007, Fig. 35

Pet., 21, 47-48; EX1003, ¶¶ 123-124, 178-181; Reply, 17-22; EX1037, ¶¶ 40-47
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

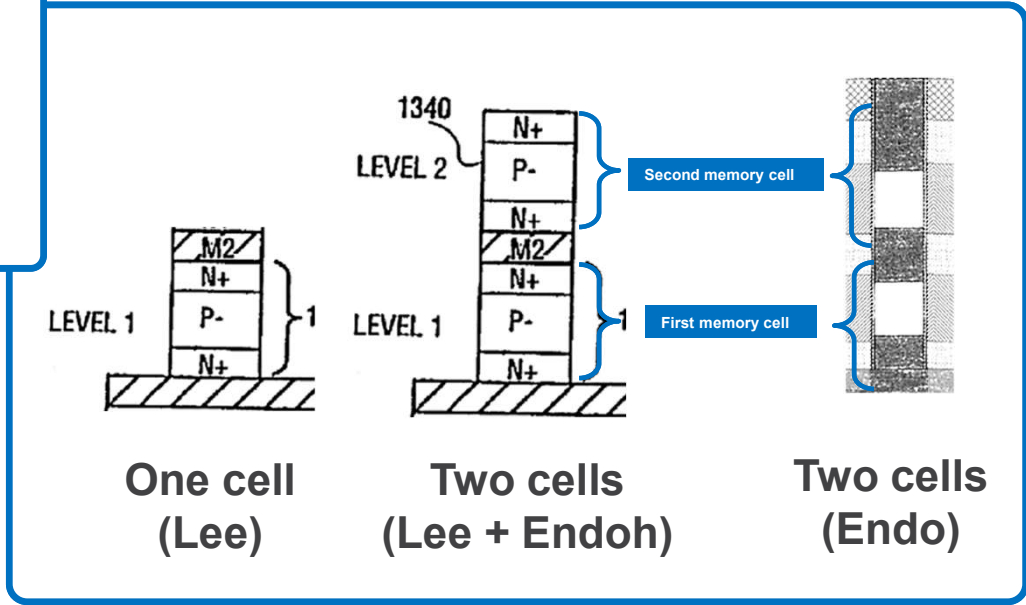
Combinations based on Endoh's teachings of stacked cells would have increased density



[0125] Although memory device 100 shown in FIG. 1A includes a charge storage medium 110 and a control gate 112 formed on only one side or surface of pillar 108, it is to be appreciated that the pillar memory device of the present invention can be fabricated so that the entire body 110 of the pillar 108 is surrounded by a single charge storage member 110 and a single control gate 112 as shown in FIG. 1B.

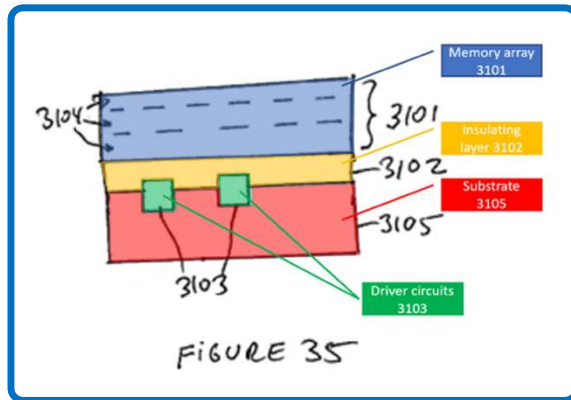
EX1007, ¶ 125

Applying two memory cells in a pillar increases density

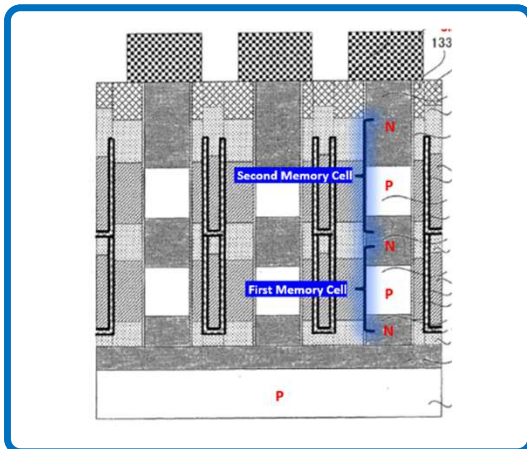


Pet., 47-48, 55, 64; EX1003, ¶¶ 177-180, 200, 218-219; Reply, 20-21; EX1037, ¶ 44
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Dr. Przybylski is wrong about implementing Endoh's memory cells in Lee's Figure 35 embodiment



Pet., 19; EX1007, Fig. 35



Pet. 44; EX1012, Fig. 1171

109. Petitioner fails to recognize the fundamental differences between Lee and Endoh that would prevent a POSITA from being able to make such a modification, or, alternatively, having any expectation of success in such an effort.

EX2029, ¶ 109

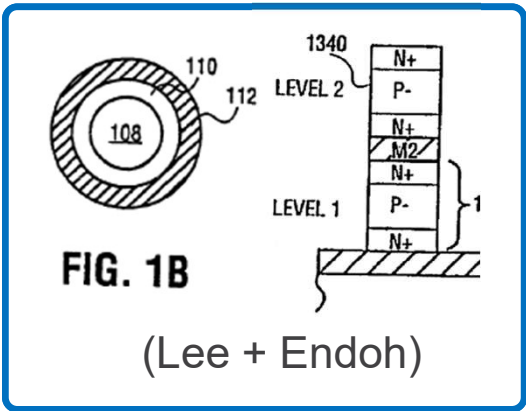
Dr. Przybylski errs by

- basing his opinions on Lee's Figure 25A, which is not part of Intel's combination (Pet. 47-48; Reply, 21-22; EX2029, ¶¶ 105, 110)
- identifying differences without explaining why they would prevent the proposed combination (EX2029, ¶¶ 109-111)
- failing to address whether implementing the combination was within a POSITA's knowledge (EX1037, ¶ 47)

Pet., 47-48; EX1003, ¶¶ 177-180; Reply, 21-22; EX1037, ¶¶ 46-47
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Lee + Aspar/Kim + Endoh render obvious all limitations of claim 13, from which claims 16-17 depend

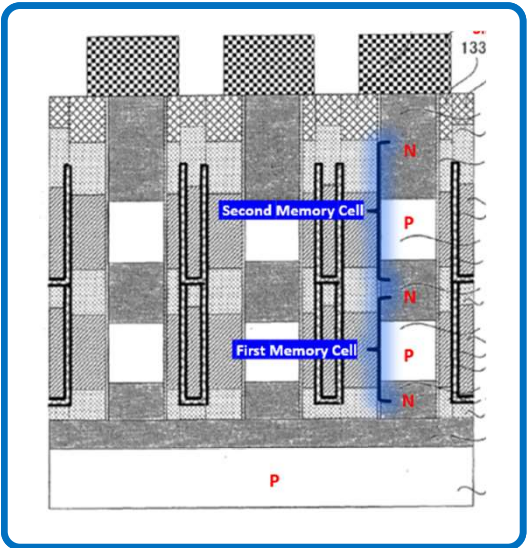
Lee’s Figure 1B memory cells



EX1007, Figs. 1B, 23A

Limitations	Support
13 <pre>[pre]</pre> , <pre>[a]</pre> , <pre>[b]</pre> , <pre>[d]</pre>	Pet., 16-29, 30-31
13 <pre>[c]</pre>	Pet., 51-54, 56-63 (Lee + Aspar/Kim)

Endoh’s memory cells



Pet. 44; EX1012, Fig. 1171

Limitations	Support
“vertically oriented semiconductor memory cells”	Pet., 46 (Endoh describes vertical cells)
“nonvolatile memory cells”	Pet., 42 (Endoh describes “EEPROM”)
“memory cells having at least one transistor”	Pet., 45-46 (Endoh describes “transistors”)
All other limitations	Pet., 16-31, 51-54, 56-63 (Lee + Aspar/Kim)

The Petition supports Ground 1F based on Lee, Aspar, and Endoh

On this record, we are concerned that Petitioner’s cross-reference to other sections of the Petition may not be sufficient to support a challenge based on Lee, Aspar, and Endoh. *See In re Magnum Oil Tools Int’l, Ltd.*,

DI, 42

Ground 1F supports that claims 16 and 17 are unpatentable	Support
Lee discloses all limitations of claim 13 except “stackable add-on layer”	Pet., 56, 63 (§VII.E) (citing Pet., 16-31)
Aspar discloses “stackable add-on layer”	Pet., 56-60 (§VII.E)
Motivation to combine Lee and Aspar	Pet., 60-63 (§VII.E.1.b)
Endoh discloses “serially connected” memory cells of claims 16 and 17 (which depend from claim 13);	Pet., 42-50 (§VII.B)
The combination of Lee, Aspar, and Endoh renders obvious “SOI pillar” of claims 16 and 17	Pet., 64
Motivation to combine Endoh with Lee and Aspar	Pet., 47-48 (§VII.B.1), 49-50

Pet., 64; EX1003, ¶¶ 218-219; DI, 42; Reply, 17-19, 22-23; EX1037, ¶¶ 40-43, 47-49
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Johnson + Aspar/Kim – claim 13

Johnson alone or Johnson + Aspar/Kim render obvious each limitation of claim 13

Claim 13 Limitation	“stackable add-on layer” construction	
	BeSang	Board / Intel
	Johnson	Johnson + Aspar/Kim
A semiconductor memory structure, comprising:	✓	✓
13[a]: a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;	✓	✓
13[b]: a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and	✓	✓
13[c]: the stackable add-on layer being bonded to the dielectric layer; and	✓	✓
13[d]: wherein the memory cells are nonvolatile memory cells having at least one transistor.	✓	✓

BeSang disputes motivation to combine and “transistor”

BeSang incorrectly argues that Johnson fails to disclose using a transistor

Memory Cell: Pillar

EX1010, 7:31

other. Some possible implementations of the steering element are (i) a PN junction diode, in amorphous, microcrystalline, polycrystalline or single crystal semiconductor (e.g. Si, Ge, SiGe, GaAs, InP, etc.); (ii) a metal-semiconductor Schottky diode; (iii) a junction field-effect transistor with gate connected to source (or to drain); (iv) a MOSFET with gate either floating, or connected to source or connected to drain; (v) a Zener diode, avalanche diode, or tunnel diode; (vi) a four-layer diode (SCR); (vii) a P-I-N diode in amorphous, microcrystalline, polycrystalline or single crystal semiconductor; and others that will be readily apparent to those skilled in the art.

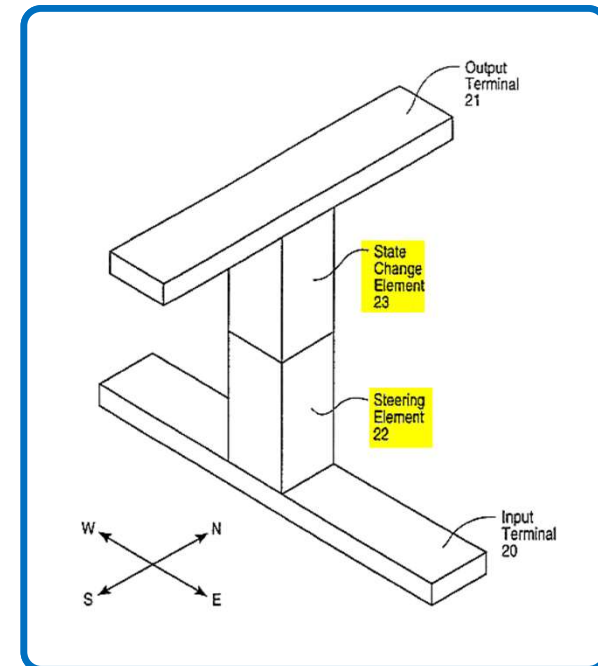
EX1010, 7:61-8:5

element. A floating gate MOS device allows numerous possible implementations of multi-level storage, providing more than 2 states for a state change element, as is well known in the art.

EX1010, 10:34-37

wherein the memory cells are nonvolatile memory cells having at least one transistor.

EX1001, claim 13



EX1010, Fig. 4a (annotated)

Pet., 65-73; EX1003, ¶¶221-243; Reply, 24-26; EX1037, ¶¶ 52-55, 59; POR, 58-59
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

A transistor used in a “2-terminal” memory cell is still a transistor

Johnson explains exactly how to use the diodes, JFET, or MOSFET in the steering element. All (including the JFET and MOSFET) are being used as 2-terminal devices, not a 3-terminal implementation. *See* EX1010 at 5:41-43, 7:44-

POR, 58

Simply put, Johnson’s exclusive teaching of 2-terminal memory cells does not disclose or render obvious “nonvolatile memory cells having at least one transistor” required by Claim 13. Nor to the extent it discloses them does it enable the use of a

POR, 60

Johnson does not disclose separately connecting the control gate in the JFET or MOSFET steering element and using it like a 3-terminal device. *See id.*; EX2029

POR, 59

claimed. They do. Given that claim 13 does not distinguish between “3-terminal” and “2-terminal” transistor configurations—it simply recites “transistor”—I do not believe PO’s, or Dr. Przybylski’s, discussion of “3-terminal” and “2-terminal” transistor configurations is relevant (POR, 57-62).

EX1037, ¶ 54

POR, 58-60; Reply, 24-25; EX1037, ¶¶ 52-55
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

The prior art describes a diode-connected transistor as a “transistor”

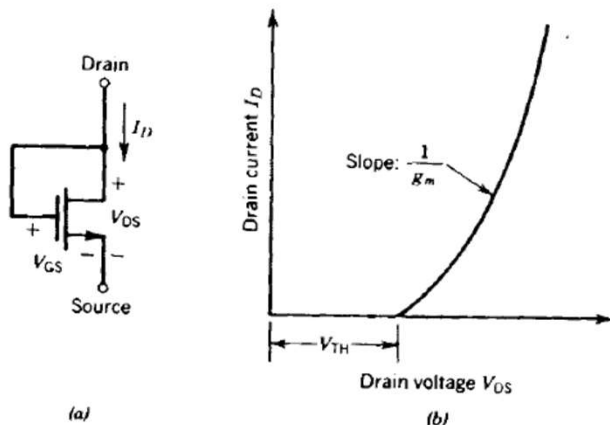


FIGURE 6.7. Diode-connected enhancement-mode MNOS transistor. (a) Circuit connection, (b) current-voltage characteristic.

SUMMARY OF THE INVENTION

The present invention provides a chalcogenide-based memory cell including a MOS diode for use in delivering large amounts of current to the chalcogenide material. The MOS diode may comprise a simple MOS transistor with its gate and drain shorted together. In a preferred operating

EX1052, 2:17-21

layer 43. Further, the drain extension region permits formation of a compact diode-connected transistor.

EX1053, 2:59-60

EX1051, 272

Reply, 24

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Contrary to BeSang's argument, claim 13 recites structure, not function

13. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
the stackable add-on layer being bonded to the dielectric layer; and
wherein the memory cells are nonvolatile memory cells having at least one transistor.

EX1001, claim 13

54. I disagree with PO because its argument is contrary to Johnson's plain disclosures. PO argues that a diode-connected transistor would act as a diode. POR 59-60. That misses the point. The claim is structural, not functional. Like the claim, the '702 patent describes a memory cell as "hav[ing] at least one vertical transistor" without requiring any specific form or function. '702 Patent, 10:15-17. The

EX1037, ¶ 54

Reply, 24

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Johnson does not teach away from using transistors, as BeSang argues



"A reference does not teach away, however, if it merely expresses a general preference for an alternative invention but **does not 'criticize, discredit, or otherwise discourage' investigation into the invention claimed.**"

DuPuy Spine, Inc. v. Medtronic Sofamor Danek, Inc., 567 F.3d 1314, 1327 (Fed. Cir. 2009) (emphasis added)

BeSang relies on prior art issues that Johnson avoids by building memory cells above the substrate

BACKGROUND OF THE INVENTION

Turning now to the design of the memory cell used in these memories, most nonvolatile memory cells have employed semiconductor devices such as MOS field-effect transistors, junction transistors, or junction diodes, built in a planar monocrystalline semiconductor substrate. This approach allows only very limited integration vertically into the third dimension (i.e. perpendicular to the plane of the substrate), since each memory cell contains some elements built in the substrate.

FIG. 4(a) shows one embodiment of our newly invented memory cell. It has two explicit terminals: an input terminal 20 and an output terminal 21. Between these terminals, the memory cell contains a steering element 22 and a state change element 23 connected in series. Neither the input terminal 20, nor the output terminal 21, nor the steering element 22, nor the state change element 23 is built in the planar semiconductor substrate.

EX1010, 5:41-48

EX1010, 2:6-36 (cited in POR, 61; Sur-Reply, 23)

Reply, 25; EX1037, ¶ 55; POR, 61-62; Sur-Reply, 23
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Although BeSang suggests otherwise, Johnson's JFET and MOSFET steering elements were enabled

[R]elying on our precedent, we hold a **presumption** arises that both the claimed and unclaimed **disclosures in a prior art patent are enabled**.

Amgen Inc. v. Hoechst Marion Roussel, Inc., 314 F.3d 1313, 1355 (Fed. Cir. 2003) (emphasis added)



“To render a claim obvious, the prior art, taken as a whole, must enable a skilled artisan to make and use the claimed invention. In general, a prior art reference asserted under § 103 does not necessarily have to enable its own disclosure, i.e., be ‘self-enabling,’ to be relevant to the obviousness inquiry. For example, a reference that does not provide an enabling disclosure for a particular claim limitation may nonetheless furnish the motivation to combine, and be combined with, another reference in which that limitation is enabled. **Alternatively, such a reference may be used to supply claim elements enabled by other prior art or evidence of record.”**

Raytheon Techs. Corp. v. Gen. Elec. Co., 993 F.3d 1374, 1380 (Fed. Cir. 2021) (citations omitted and emphasis added)

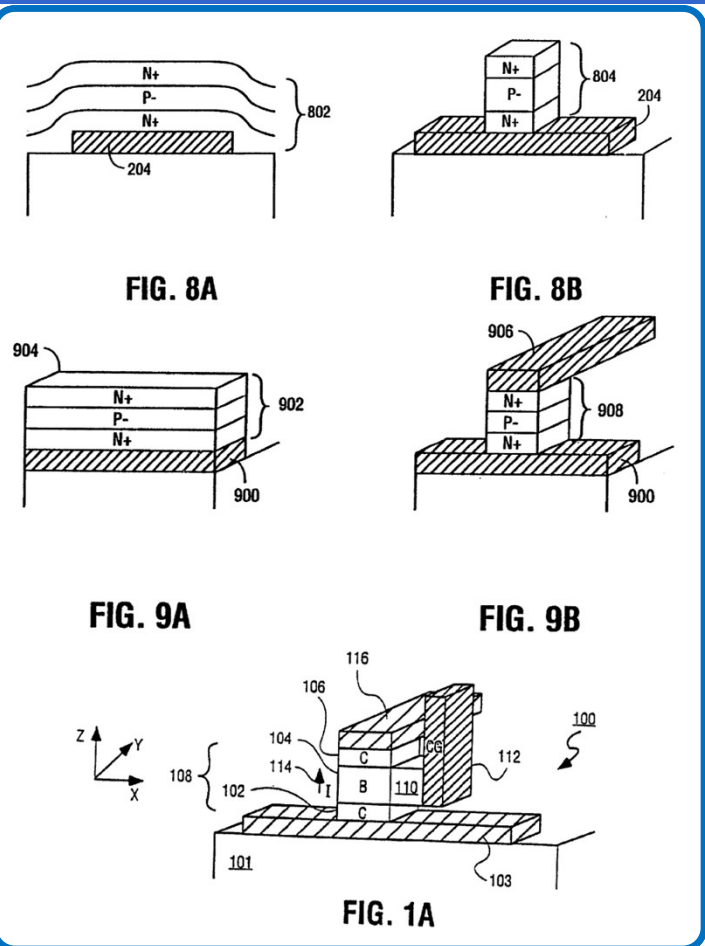
BeSang ignores that Johnson (like Lee) discloses making pillars using photomasking as well as self-aligned techniques

The memory cell may also be fabricated using alternative embodiments; the self-aligned pillar formation described above may be replaced by a formation involving the use of a pillar formation photomask. This would eliminate the self-alignment of the pillar to the conductors, but would be advantageous in fabrication processes that could potentially exploit the physics of free sidewalls. These processes

EX1010, 6:46-52

The foregoing process sequence exploits self-alignment to reduce the required alignment tolerances between the pillar and the conductors. This embodiment may be substituted with an embodiment involving one or more additional photomasking steps to explicitly define the pillar itself, rather than defining it using the intersection of two conductor photomasking steps, as is done in the self-aligned process. This may be advantageous in various processes that

EX1010, 15:12-19



Reply 26, EX1037, ¶¶ 56-60
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

EX1007, Figs. 1A, 8A-9B

Bonding was a known solution to known problems using prior art elements based on established functions

Fabricating 3D structures (Johnson, Aspar) and memory arrays above a substrate containing electrical devices (Johnson, Kim) were known problems. Aspar and Kim describe bonding as a known solution.

The field programmable nonvolatile memory cell of the present invention is built above, rather than in, a planar substrate. Therefore, this memory cell can be stacked vertically in numerous layers to form a three dimensional array. Each layer of memory cells interacts only with the layer above and the layer below, which makes vertical stacking of layers quite simple.

EX1010, 5:30-37

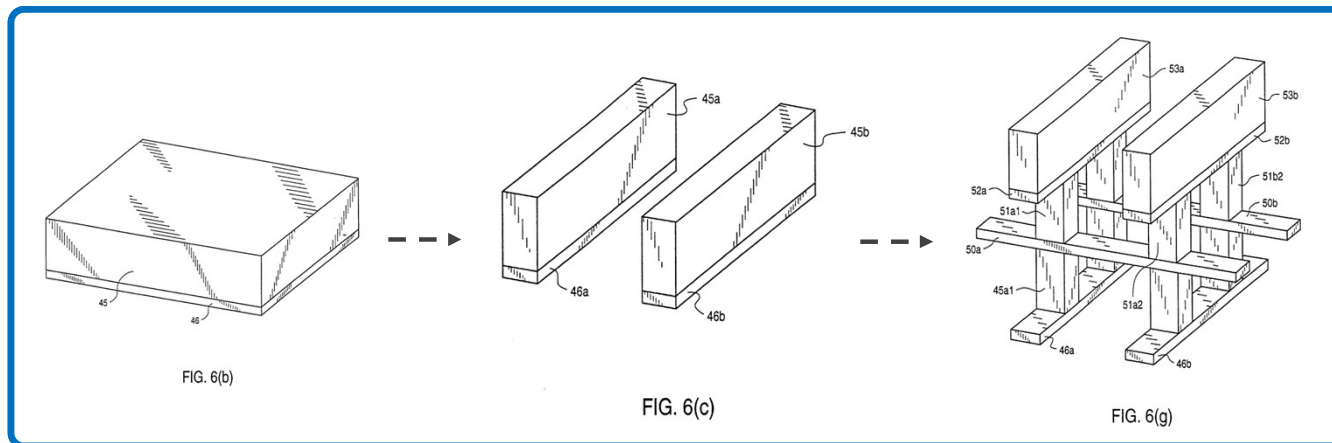
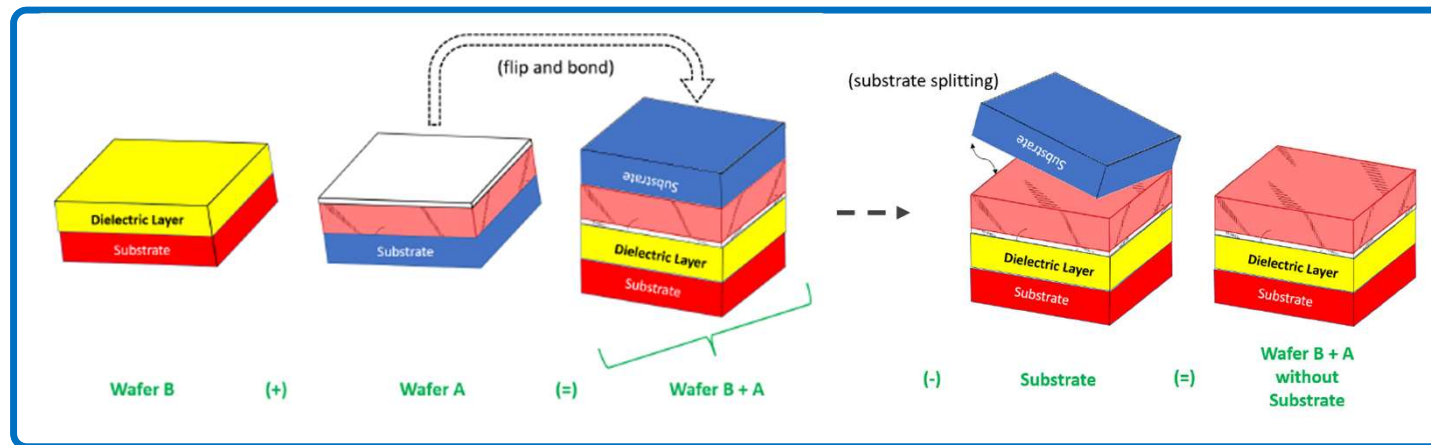
substrate. Wafer bonding and layer transfer enable different materials to be associated to form multi-layer substrates. This is particularly advantageous

EX1009, 834

[0020] Attention now is directed to the drawings and particularly to FIG. 1, an example three-dimensional (3-D) wafer-to-wafer vertical stack is illustrated. As shown in FIG. 1, the 3-D vertical stack (chip) 100 may comprise any number of active device polysilicon (Si) wafers, such as wafer #1 110 including, for example, one or more microprocessors; wafer #2 120 including one or more memory devices; and wafer #3 130 including one or more radio-frequency (RF) or optical communication devices. Typically, a dielectric layer 102 is used to bond the active device wafers 110, 120 and 130.

EX1008, ¶ 20

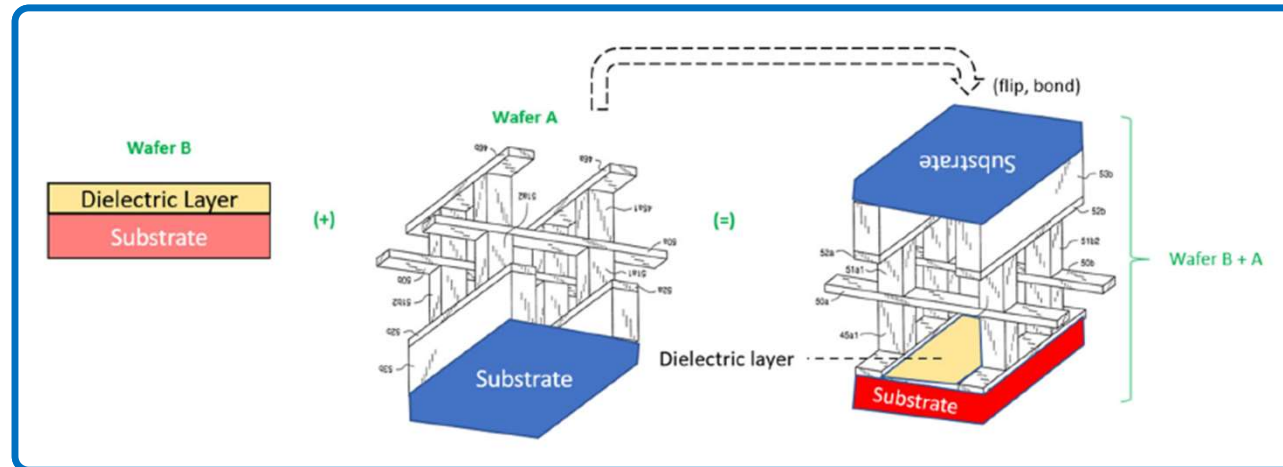
Aspar does not prevent using Johnson's self-alignment



EX1010, Figs. 6(b), (c), (g)

Pet., 79-80; EX1003, ¶¶ 258-260; Reply, 26-28, EX1037, ¶¶ 59, 63
 DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Leftover strips taught in Johnson can be used for additional layers in the combination with Kim



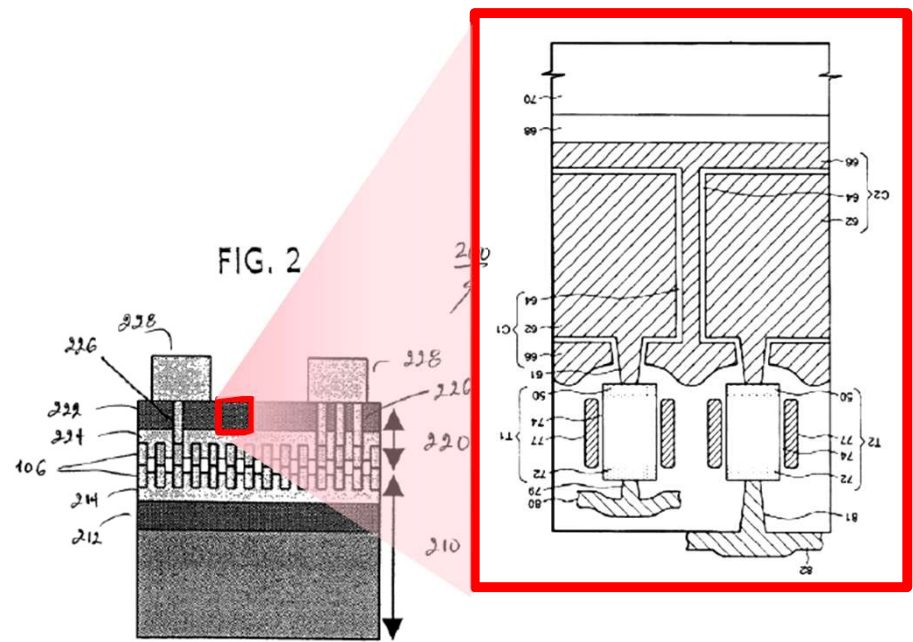
as 51a 1, 51a 2, 51b 2). FIG. 6(g) shows that $(N+1)=3$ conductor layers and hence $(N+1)=3$ masking steps, are required to pattern $(N=2)$ layers of pillar layerstack (not counting the interlevel via layers which are used in the peripheral circuits but not in the memory array). The wafer is now ready to receive more stack layers and conductor layers, at the discretion of the manufacturer.

EX1010, 14:21-27

Pet., 75; EX1003, ¶ 248; Reply, 26, 28; EX1037, ¶¶ 63, 65
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Park + Kim – claim 1

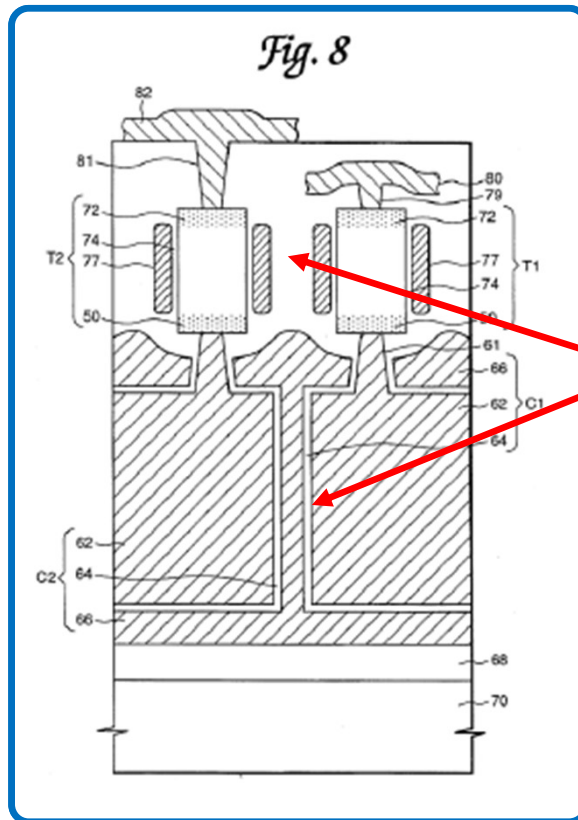
The combination of Park and Kim renders claim 1 obvious



EX1008, Fig. 2 (annotated); EX1011, Fig. 8

Limitation	Park and Kim
semiconductor memory structure	DRAM (EX1011, 2:11-14), vertically stacked layers (EX1008, ¶¶ 7, 22)
substrate	“active silicon (Si) layer 212” (EX1008, ¶ 23)
electrical devices	“active IC devices” (EX1008, ¶ 23)
dielectric layer	“ILD layers 214” (EX1008, ¶ 23)
interconnect layer	“bonding layer 106” (EX1008, ¶ 23)
stackable add-on layer	“active silicon layer 222” (EX1008, ¶¶ 20, 22-23, 25)
vertically oriented memory cells	memory cells formed from “silicon pillar[s]” (EX1011, 2:16-25, 2:46-56, 1:11-21)
separated	“surrounded [] with an insulating film” (EX1011, 2:16-21, 4:9-27)
bonded, greatest distance	“bonding layer 106” (EX1008, ¶¶ 23-25, see figure at left)
DRAM, transistor	DRAM memory cells (EX1011, 2:16-25, 5:20-22)

Park teaches DRAM memory cells electrically “separated” by dielectric material, as claimed/described in the '702 patent



EX1011, Fig. 8 (annotated)

dielectric material

1. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate; and
a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;
wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate; and
wherein the memory cell is a DRAM having at least one transistor

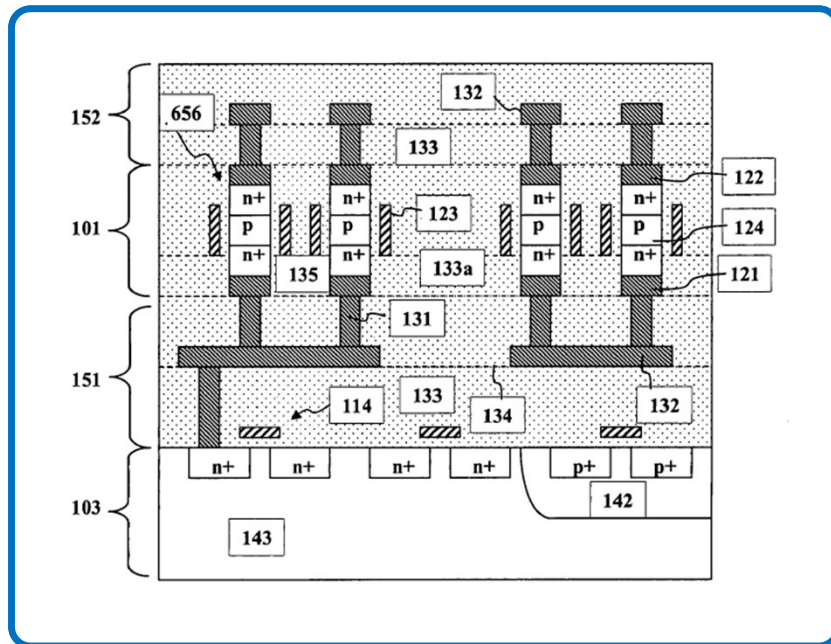
EX1001, claim 1

Various embodiments of the present invention provide floating devices that are separated by dielectric isolation regions. These electrically separated structures do not have the parasitic devices which are typically found in prior art approaches.

'702 patent Figure 1 does not support BeSang's argument; it is not described as DRAM, as required by claim 1

wherein the memory cell is a **DRAM** having at least one transistor.

EX1001, claim 1



EX1001, Fig. 1

FIG. 1 is a cross-sectional view of an embodiment the present invention that includes a base semiconductor substrate and add-on vertical memory devices.

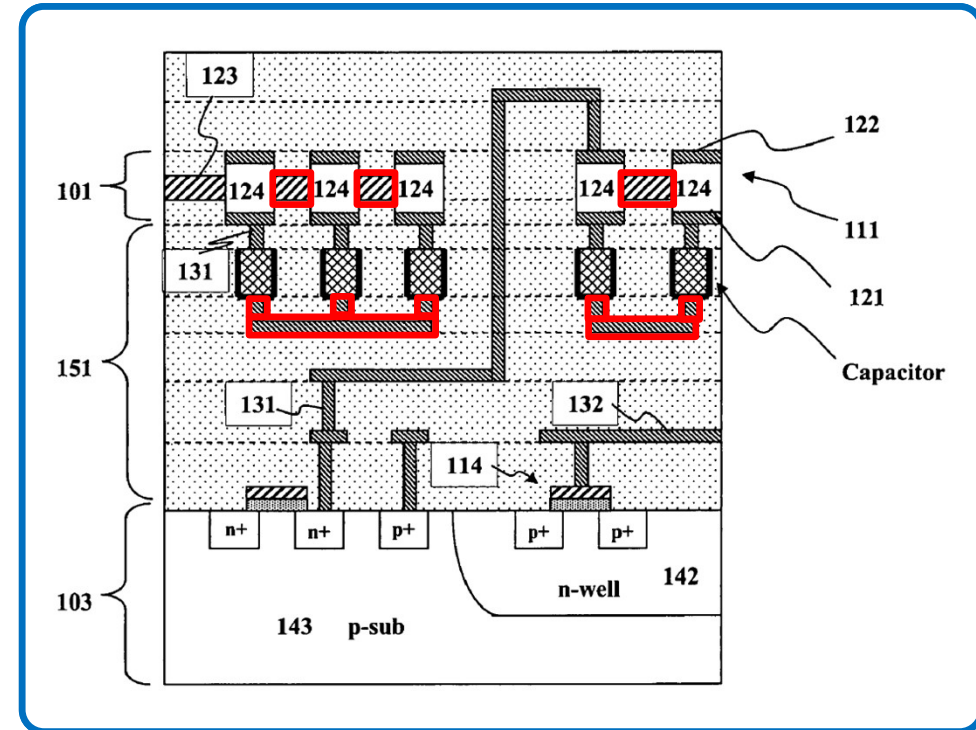
EX1001, 2:13-15

Vertically oriented memory structures constituting memory cells, or portions thereof, in a 3-D integrated circuit arrangement in accordance with the present invention, are shown in FIG. 1. Embodiments of the present invention

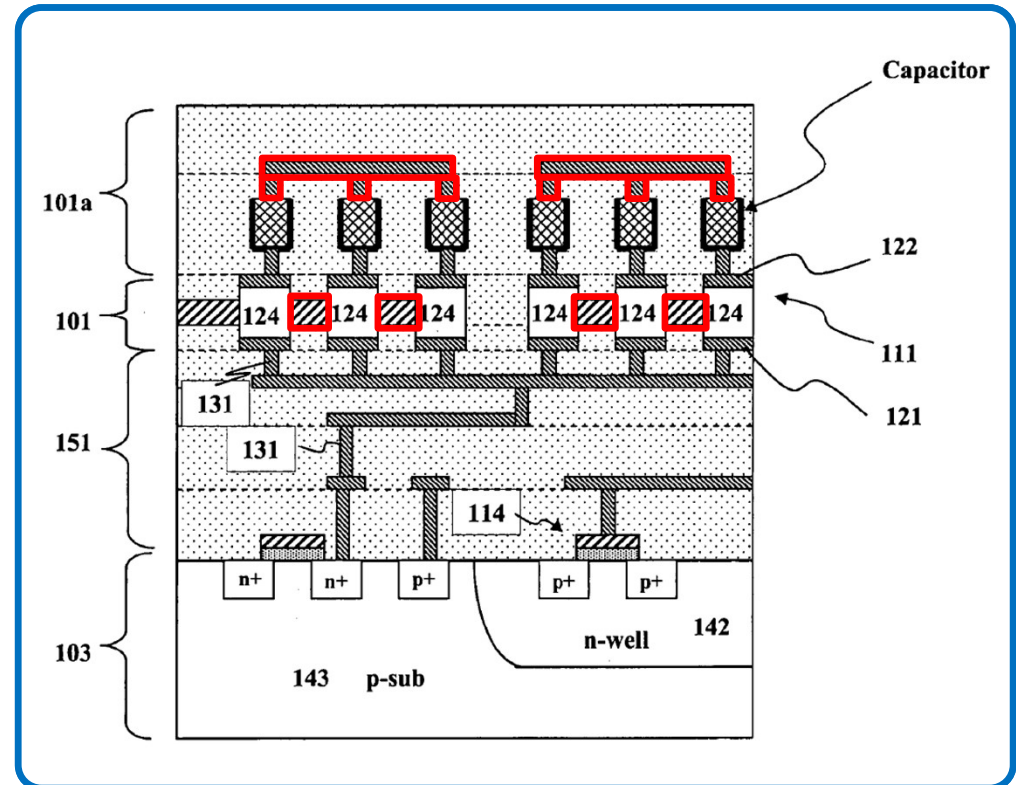
EX1001, 3:51-54

EX1001, 5:17-7:60 – no mention of DRAM

The '702 patent discloses that complete separation of DRAM memory cells by dielectric is not required



EX1001, Fig. 9 (annotated)



EX1001, Fig. 10 (annotated)

Reply, 29; EX1037, ¶ 66
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Intel's arguments are responsive and not new

Intel's arguments in the Reply properly responded to the Board's institution decision and BeSang's POR

"A reply **may** only **respond to arguments raised in the** corresponding opposition, patent owner preliminary response, **patent owner response**, or **decision on institution**."

37 C.F.R. § 42.23(b)

"A party **may also submit rebuttal evidence** in support of its reply."

Consolidated Trial Practice Guide, 73

Alleged "new" Intel argument	Support in Reply	Intel responds to
Forming more memory levels in Lee and Aspar/Kim (Sur-Reply, 7-8)	Reply, 11-12	POR, 24-25
Lee discloses and suggests stacking (Sur-Reply, 10-11)	Reply, 7	DI, 33-35; POR, 25-26
Process optimization as a motivation to combine Lee and Aspar/Kim (Sur-Reply, 14-15) (this is the only argument addressed in BeSang's motion to exclude)	Reply, 10	DI, 36-37; POR, 20-30, 45-50, 65-68, 70-73
Aspar does not teach an 1100°C annealing step (Sur-Reply, 15-16)	Reply, 12	POR, 10-11, 44-46, 69, 72, 74
Combinations involving Endoh (Sur-Reply, 20-21)	Reply, 17-22	DI, 42-43; POR, 39-40, 42-43

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

The arguments in Intel's Reply were not new

Alleged “new” Intel argument	Support in Reply	Support in Petition
Forming more memory levels in Lee and Aspar/Kim (Sur-Reply, 7-8)	Reply, 11-12	Pet., 27-28, 38 & n.12
Lee discloses and suggests stacking (Sur-Reply, 10-11)	Reply, 7	Pet., 51-52, 56
Process optimization as a motivation to combine Lee and Aspar/Kim (Sur-Reply, 14-15) (this is the only argument addressed in BeSang's motion to exclude)	Reply, 10	Pet., 53-54, 61-62 (citing EX1003, ¶¶ 196, 213); EX2039, 91:17-98:13 (citing EX1003, ¶ 213)
Aspar does not teach an 1100°C annealing step (Sur-Reply, 15-16)	Reply, 12	Pet., 56-58
Combinations involving Endoh (Sur-Reply, 20-21)	Reply, 17-22	Pet., 41-50, 52-53, 55, 58-60, 64

BeSang's motion to exclude should be denied

BeSang's motion to exclude raises improper issues: BeSang should have sought Board permission to move to strike



Patent Trial and Appeal Board
Consolidated Trial Practice Guide
November 2019

evidence—arguments regarding weight should appear only in the merits documents. Nor should a motion to exclude address arguments or evidence that a party believes exceeds the proper scope of reply or sur-reply.

Consolidated Trial Practice Guide, 79

Motions to Strike. If a party believes that a brief filed by the opposing party raises new issues, is accompanied by belatedly presented evidence, or otherwise exceeds the proper scope of reply or sur-reply, it may request authorization to file a motion to strike.

Consolidated Trial Practice Guide, 80

“Prior authorization. A motion will not be entered without Board authorization.”

37 C.F.R. § 42.20(b)

- BeSang relies on decisions dated before the Guide was updated
- *Intuitive Surgical* departs from the Guide and is not precedential

Paper 30, 2-3; Paper 31, 1-2
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

A reply is proper if it is responsive and elaborates on previously presented arguments



“[A] reply may be proper if it is **responsive** and **simply expands on previously raised arguments**. ...

Alere’s reply argument discussing cost and time savings has a **nexus to Rembrandt’s prior argument** and is **responsive**. It **refutes** Rembrandt’s assertions that there is no motivation [I]t also **properly expands on and is a fair extension of** [Alere’s] **previously raised efficiency argument**. ...

Alere’s reply argument is **responsive** to Rembrandt’s arguments and the Board’s observations. Alere **disputes** Rembrandt’s contention ... [and] **elaborates on the motivation-to-combine argument that Alere made in its petition**

Alere’s reply argument involves the **same ‘legal ground’** based on ‘the **same prior art reference[s]**’ and the ‘same legal argument’”

Rembrandt Diagnostics, LP v. Alere, Inc., 76 F.4th 1376, 1384-85 (Fed. Cir. 2023) (citations omitted and emphasis added)

The Petition raises motivation arguments relating to crystalline silicon and process optimization

stacks can be easily performed thanks to Smart-Cut technology.” EX1009, 839. In addition, the Smart-Cut® process was known to have several advantages including “transferring thin layers of very good thickness homogeneity and with a high crystalline quality.” Sechen, ¶212; (quoting EX1009, 834). This combination merely

Pet., 60-61; see also *id.*, 80-81 (quoting EX1009, 834)

devices, MOSFETs, and new memory devices.” *Id.*, ¶19. Kim also discloses that its 3D vertical wafer stack may comprise “any number” of wafers, and provides an example bonding wafer 110 having one or more microprocessors and wafer 120 including one or more memory devices using a dielectric layer 102. *Id.*, ¶20, Fig. 1; see also *id.*, ¶22 (contemplating “logic/memory stacking”).

Pet., 51

a faster signal and minimal interconnect RC delays. In addition, the vertical stack can effectively integrate diverse process technologies on a single wafer process, such as, for example, logic/memory stacking, processor stacking, optical interconnect, system-on-chip, and RF interconnect.

EX1008, ¶ 22

A POSITA would have also recognized that Aspar’s Smart-Cut® process as compared to monolithic deposition allows for more efficient quality control at the layer formation stage Sechen, ¶213 (citing EX1016). Specifically, when using

Pet., 61-62; see also *id.*, 53-54, 76, 81

control. In addition, a POSITA would have recognized that forming electrical devices on one substrate separately from the memory devices on another substrate would have allowed optimization of the respective processes rather than forcing the memory devices to be formed with a sub-optimal process tailored to preserving the electrical devices formed on the single wafer in the monolithic process.

EX1003, ¶ 213

Paper 30, 4-6

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BeSang was aware of Intel's arguments but chose not to address them specifically in the POR

BeSang asked Dr. Sechen about crystalline silicon and process optimization before filing the POR

Q. So first it says -- Aspar says this process has several advantages; correct?

A. Yes.

Q. And it says, "Among these, the possibility of transferring thin layers of very good thickness homogeneity and with a high crystalline quality onto different materials deserves to be highlighted."

Did I read that correctly?

A. Yes. And they do highlight

EX2039, 74:10-19; *see also id.*, 94:3-21, 96:15-97:11

Q. Okay. That sentence says, "In addition, a POSITA would have recognized that forming electrical devices on one substrate separately from the memory devices on another substrate would have allowed optimization of the respective processes rather than forcing the memory devices to be formed with a suboptimal process tailored to preserving the electrical devices formed on the single wafer on the monolithic process."

Did I read that correctly?

A. Yes.

EX2039, 92:12-93:1; *see also id.*, 91:17-92:11, 93:2-98:13

The Reply expands on the Petition in responding to Board comments and BeSang's arguments

Second, the parties' contentions present a **fact issue** as to whether fabricating Lee's vertical memory structure using Kim's wafer bonding method would have amounted to nothing more than applying a known technique to address a known problem using prior art elements according to their established functions, as Petitioner contends (Pet. 53), or **whether the combination would not have been viewed as an improvement** of Lee's monolithic three-dimensional arrays, as Patent Owner contends (Prelim. Resp. 38–39). *See KSR*, 550 U.S. at 417 (“[A] court must ask whether the

Board

DI, 36-37

BeSang

A. **Intel Does Not Establish A Motivation To Combine Lee With Aspar (Grounds 1E-1F | Claims 13-17)**

Intel also does not meet its burden to show that a skilled artisan would have departed from Lee to use Aspar's stacking technique. *Intel never shows: (1) Aspar's*

Paper 30, 6-7

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

POR, 44; *see also id.*, 20-30, 45-50, 65-68, 70-73

Though BeSang says the opposite, Dr. Sechen testified about the problems with high temperature processing

A. Well, you also -- I mean, there's various things that -- that you worry about when you have lots of layers. Like, you know, a later processing step can cause perturbations of previous processing steps, so that's always something you worry about so --

EX2039, 95:17-22

Q. Okay. In -- in what ways can subsequent processing steps perturb earlier layers when doing monolithic processing?

A. It can be as simple as ions, for example, passing through layers, it can be -- the heat can cause metal to deform possibly creating opens or shorts. There's a number of

EX2039, 96:15-21

Backup

Intel specifies the claim constructions addressed in Grounds 1D, 1E, and 1F

D. Ground 1D: Obviousness over Lee, Kim, and Endoh (claims 16–17)

Lee and Kim render obvious claims 16 and 17 under the proper construction of “the stackable add-on layer being bonded” and PO’s apparent construction of “SOI pillar.” Claims 16 and 17 would have also been obvious over Lee, Kim, and Endoh under those constructions. The description of the Lee-Kim combination

“stackable add-on layer” = **Board / Intel construction**

“SOI pillar” = **BeSang apparent construction**

E. Ground 1E: Obviousness over Lee and Aspar (Claims 13–17)

As discussed in Section VI.A, a POSITA would have understood “the stackable add-on layer being bonded” as recited in claim 13 to require that the “stackable add-on layer” is wafer bonded to “the dielectric layer.” Additionally, as discussed in Section VI.B, a POSITA would have understood that “SOI pillar” means a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology. Under these proper constructions, claims 13–17 would

“stackable add-on layer” and “SOI pillar” = **Board / Intel construction**

F. Ground 1F: Obviousness over Lee, Aspar, and Endoh (claims 16–17)

Lee and Endoh render obvious claims 16–17 under PO’s apparent constructions as discussed in Section VII.B. Under the proper constructions of “stackable add-on layer being bonded” and “SOI pillar,” claims 16–17 would have been obvious over Lee, Aspar, and Endoh. The description of the Lee-Aspar

Intel relies on relevant Federal Circuit claim construction decisions; BeSang's non-precedential cases do not apply

Intel raised **alternative constructions** in **multiple grounds**; the Board issued preliminary constructions at institution.

AC Techs. S.A. v. Amazon.com, Inc., 912 F.3d 1358, 1360 (Fed. Cir. 2019):

- “The Board must consider all grounds of unpatentability raised in an instituted petition.”
- Petitioner raised multiple grounds based on alternative claim constructions
- The Board adopted a broad construction of the challenged claims, instituted the grounds corresponding to that construction, and found the claims unpatentable on those grounds

Masimo Corp. v. Sotera Wireless Inc., Techs. S.A., 2023 WL 6990542, *4-5 (Fed. Cir. Oct. 24, 2023): facing facts similar to this IPR, the court affirmed that the Board can narrow its focus to certain grounds but only if they are tied to issued constructions



Ebates Performance Mktg., Inc. v. Int'l Bus. Machs. Corp., IPR2022-00439, Paper 11, 8-12 (PTAB Oct. 3, 2022):

- The Board denied institution; it declined to adopt a construction for a means-plus-function limitation where the petitioner argued (i) the construction was incorrect and (ii) the limitation was indefinite for lack of corresponding structure.

Hologic, Inc. v. Enzo Life Scis., Inc., IPR2018-00019, Paper 17, 5-9 (PTAB Apr. 18, 2018):

- The Board denied institution; petitioner presented only grounds based on a construction it asserted was incorrect.

Intel's combinations

Lee
(structure)

+

Aspar (or Kim)
"stackable add-on layer"

+

Endoh
(structure for claims 16-17 only)

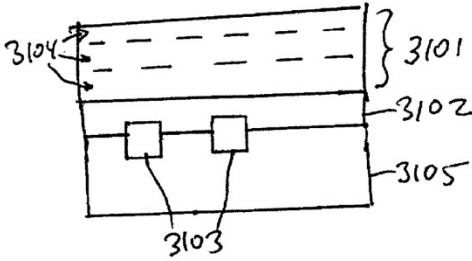


FIGURE 35

+

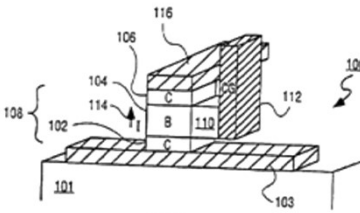
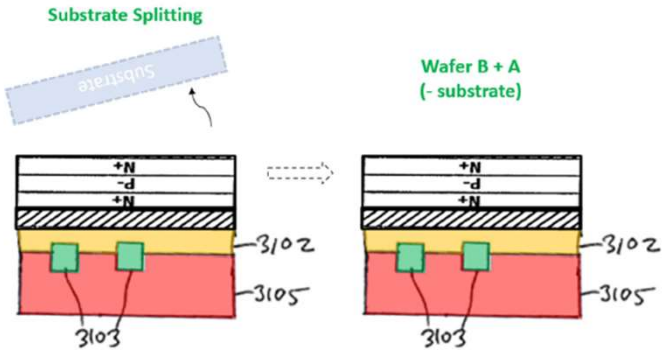


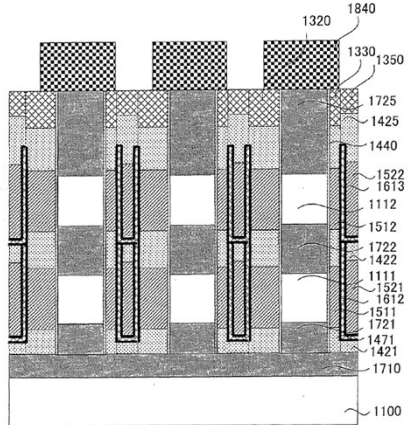
FIG. 1A



AND

"SOI pillar"

Fig. 1171



Pet., 19, 22, 45, 59-60; Ex. 1003, ¶¶ 114-34, 170-88, 209-11
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

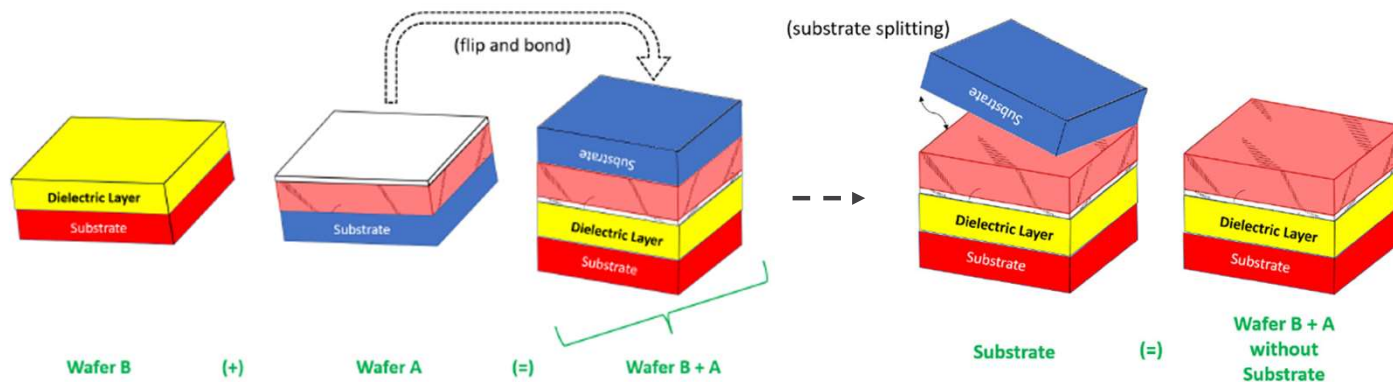
Under Board / Intel construction, Johnson teaches all limitations of claim 13 except “stackable add-on layer”

Limitation	Johnson
semiconductor memory structure	“semiconductor memory” (EX1010, 1:7-12)
substrate	“substrate” (<i>id.</i> , 13:26-35)
electrical devices	“CMOS transistors” (<i>id.</i>)
dielectric layer	“insulator” (<i>id.</i>)
memory cells	“memory cell” (<i>id.</i> , 2:33-37), “transistor” (<i>id.</i> , 5:41-49, 7:61-8:5)

13. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
the stackable add-on layer being bonded to the dielectric layer; and
wherein the memory cells are nonvolatile memory cells having at least one transistor.

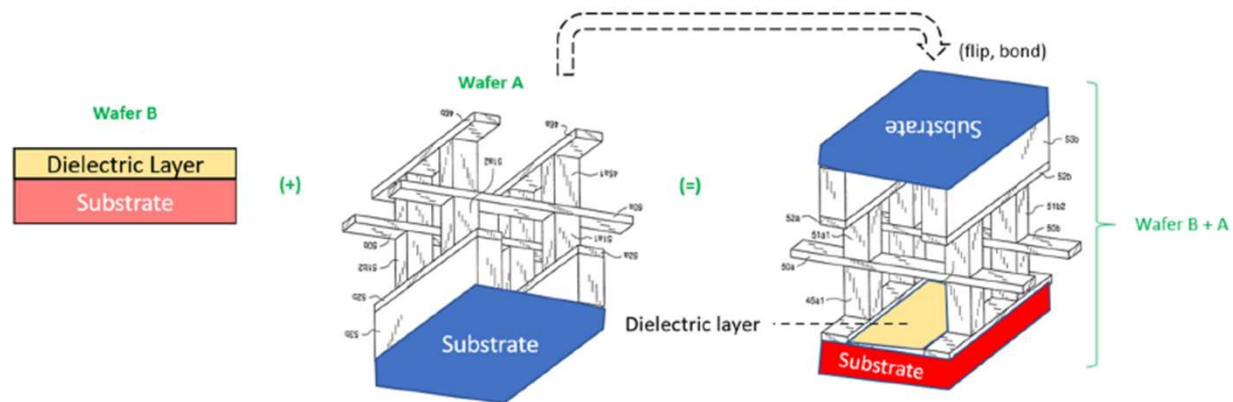
EX1001, claim 13

A POSITA would have used Aspar's or Kim's bonding techniques to make Johnson's memory cells



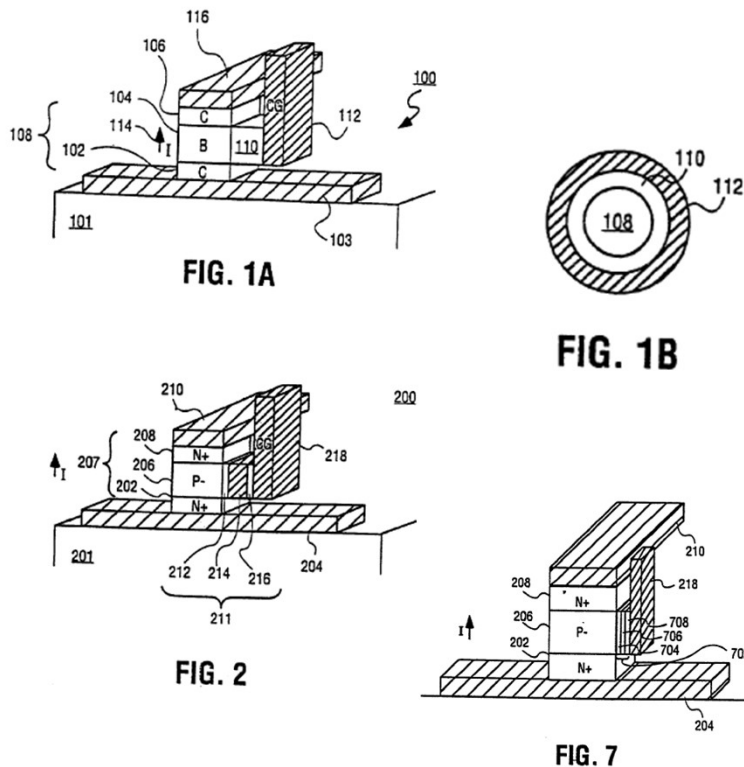
Aspar

Kim



Pet., 74-82; EX1003, ¶¶ 246-262
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

The process relating to Lee's Figures 13-28 is separate from and inconsistent with other embodiments



EX1007, Figs. 1A, 1B, 2, 7

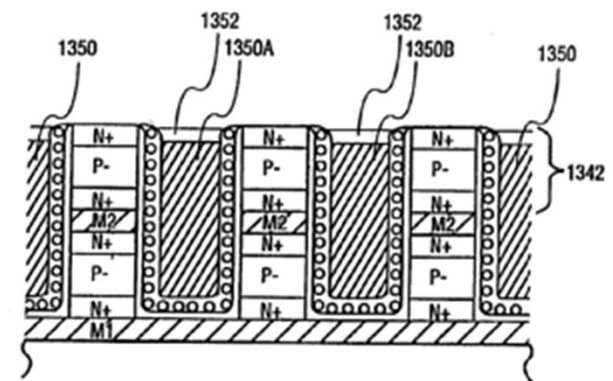


FIG. 25A

EX1007, Fig. 25A

[0052] FIG. 13 to FIG. 28 illustrate a method of fabricating multiple levels of pillar memories in accordance with an embodiment of the present invention.

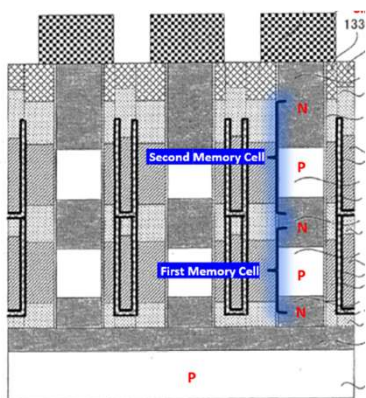
EX1007, ¶ 52

Implementing pillars with two memory cells was a known solution to a known problem using prior art elements

Fabricating memory arrays using pillar structures (Lee, Endoh) was a known problem. Endoh describes two memory cells in a pillar as a known solution.

EPROMs or EEPROMs. In the preferred embodiments of the present invention described in detail below, the charge storage devices are formed in various configurations, such as a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM, a rail stack TFT EEPROM, and various other configurations. Each of these

EX1007, ¶ 113



Pet., 44; EX1012, Fig. 1171

[1206] In this production example, a semiconductor memory device has a structure in which a plurality of floating gates are formed as the charge storage layers; selection gate transistors are formed, and then tunnel oxide films are formed; island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate; active regions of the memory cells are electrically floated; two memory cells are arranged on each island-like semiconductor layer; the tunnel oxide films of the memory transistors are formed at the same time; and the transistors are connected in series along the island-like semiconductor layer, as shown in FIG. 1171 and FIG. 1172.

EX1012, ¶ 1206

Thereby two memory transistors are arranged on the island-like semiconductor layer. A semiconductor memory device

EX1012, ¶ 1207

Pet., 21-22, 42-48, 55, 64; EX1003, ¶¶ 96, 170-173, 179, 200, 218-219; Reply, 5-6
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

'702 patent, claims 1 and 13

1. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate; and
a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;
wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate; and
wherein the memory cell is a DRAM having at least one transistor.

13. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
the stackable add-on layer being bonded to the dielectric layer; and
wherein the memory cells are nonvolatile memory cells having at least one transistor.

'702 patent, claims 14-17

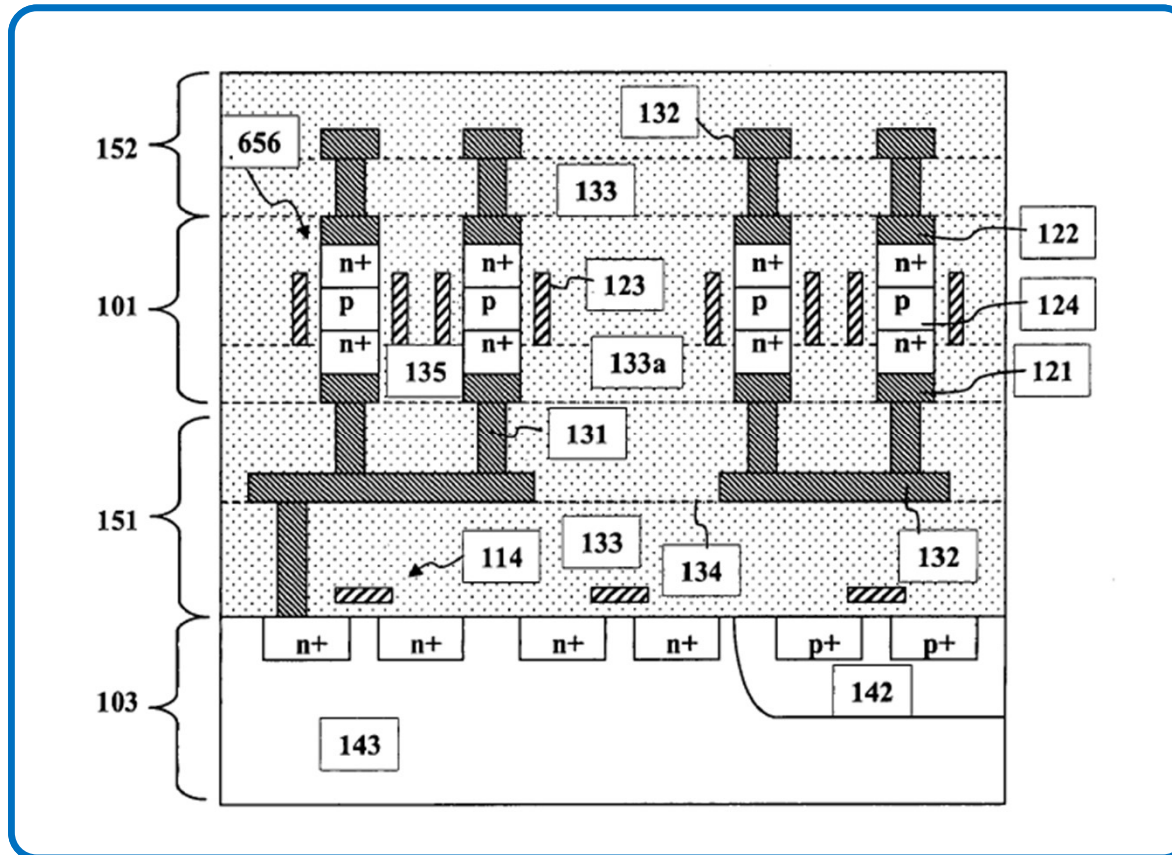
14. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

15. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

16. The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

17. The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

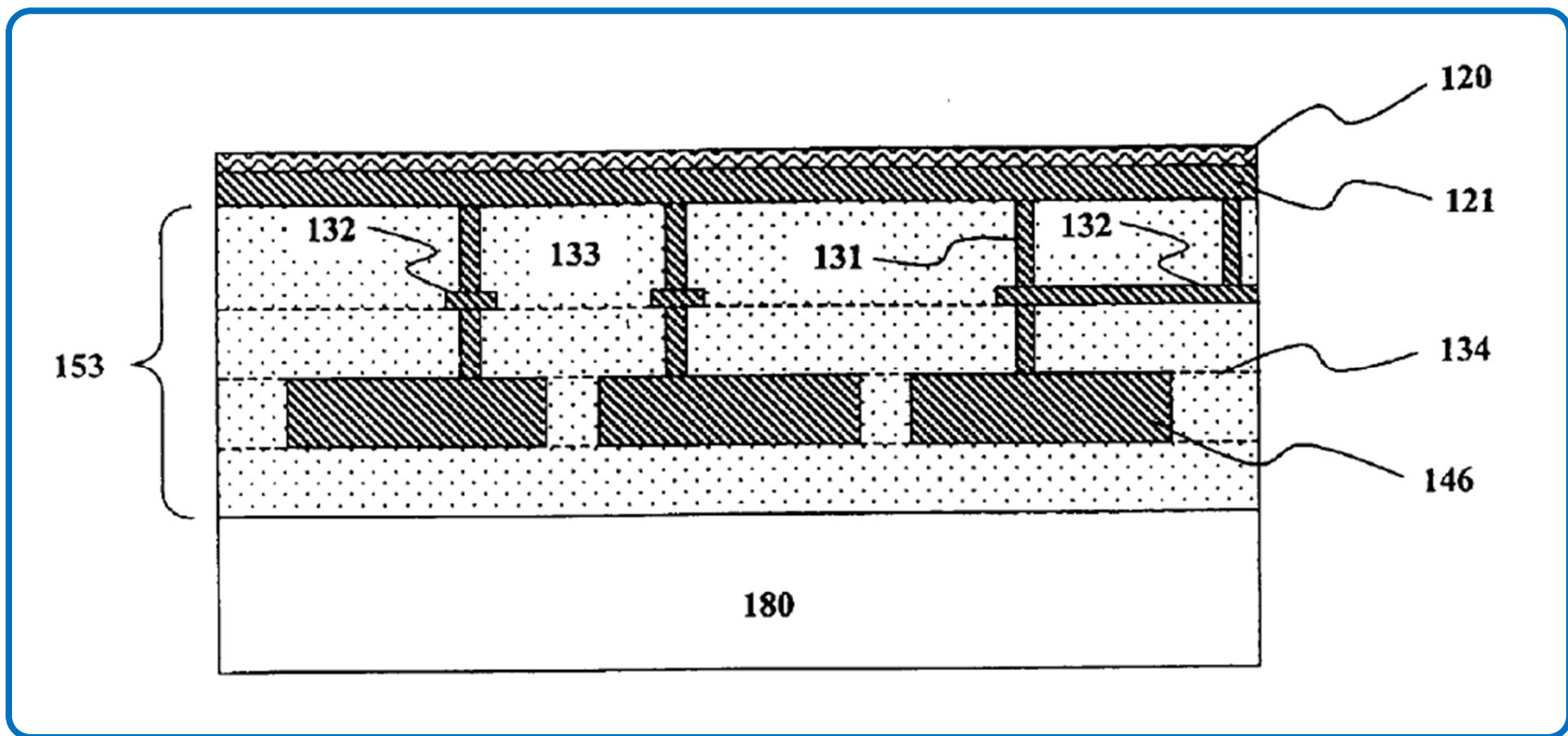
'702 patent, Figure 1



Ex. 1001, Fig. 1

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

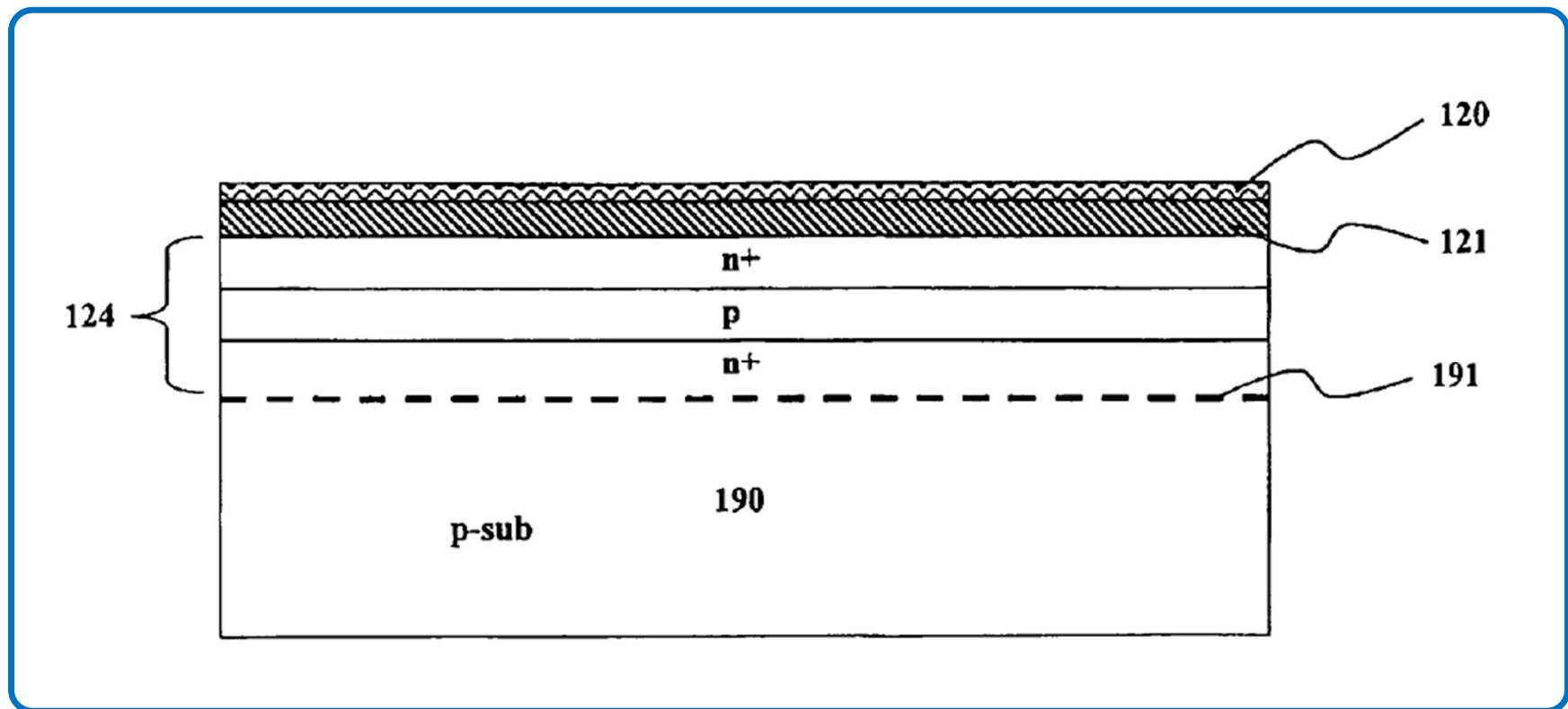
'941 patent, Figure 4A



Ex. 1005, Fig. 4A

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

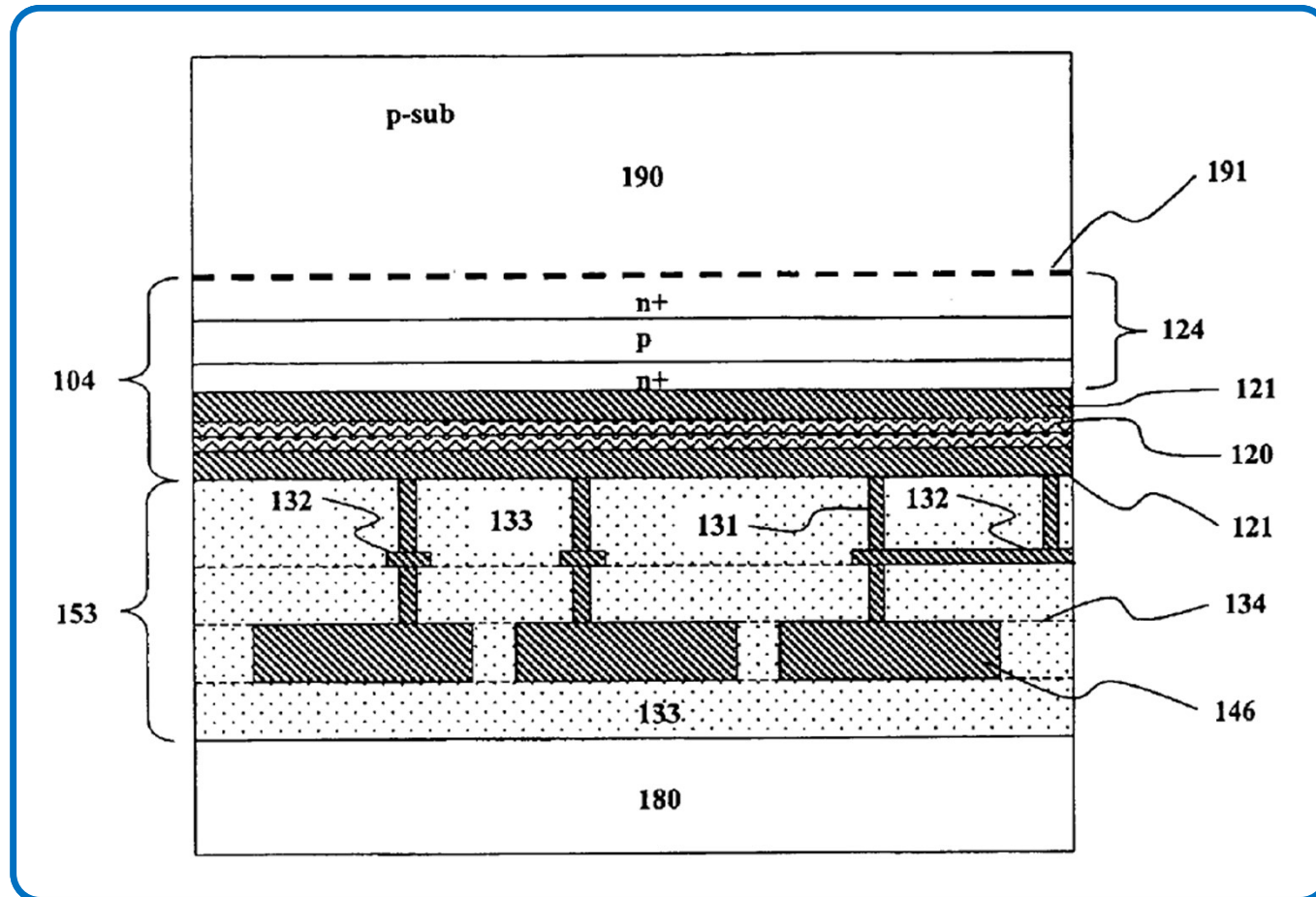
'941 patent, Figure 4B



Ex. 1005, Fig. 4B

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

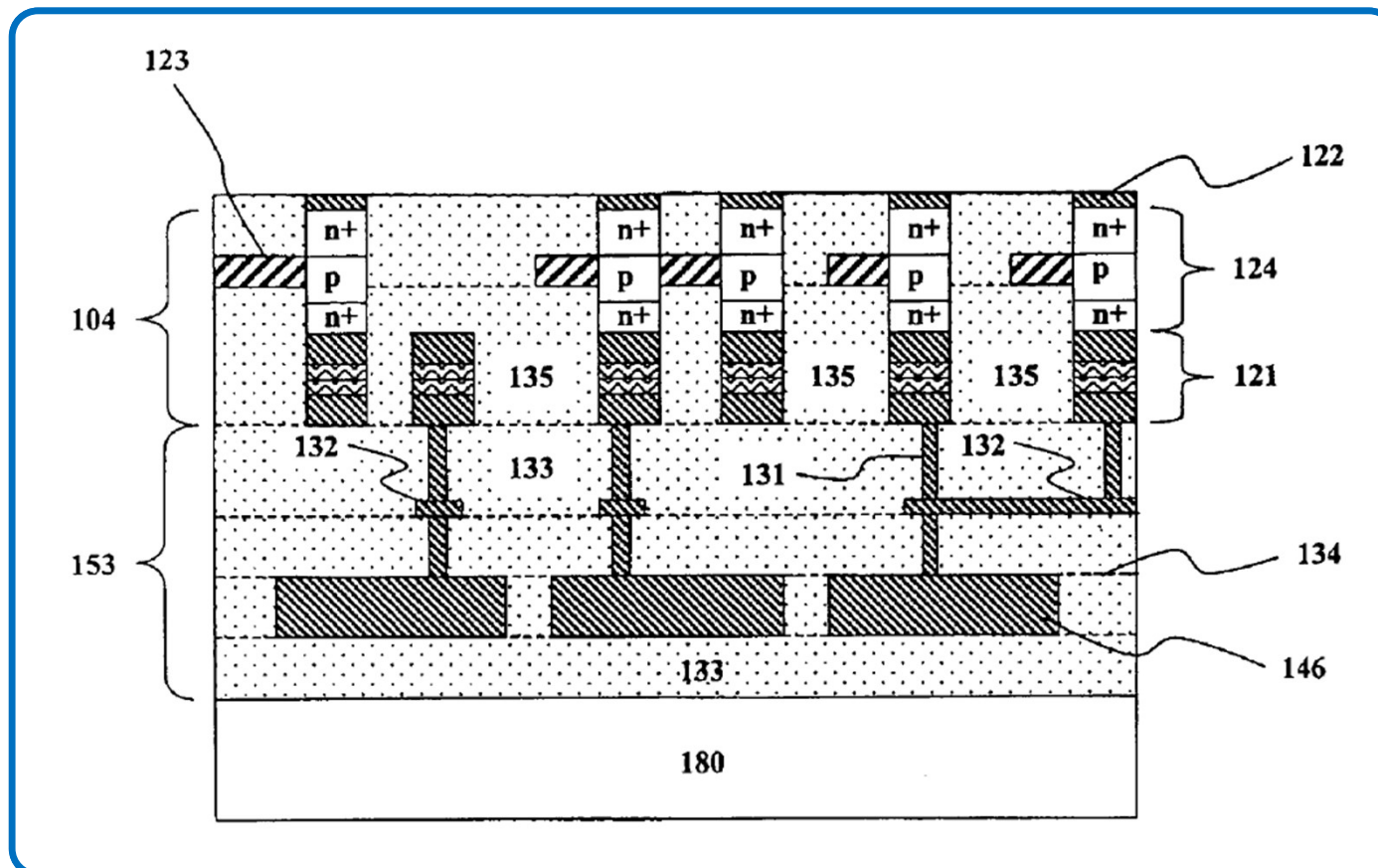
'941 patent, Figure 4C



Ex. 1005, Fig. 4C

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

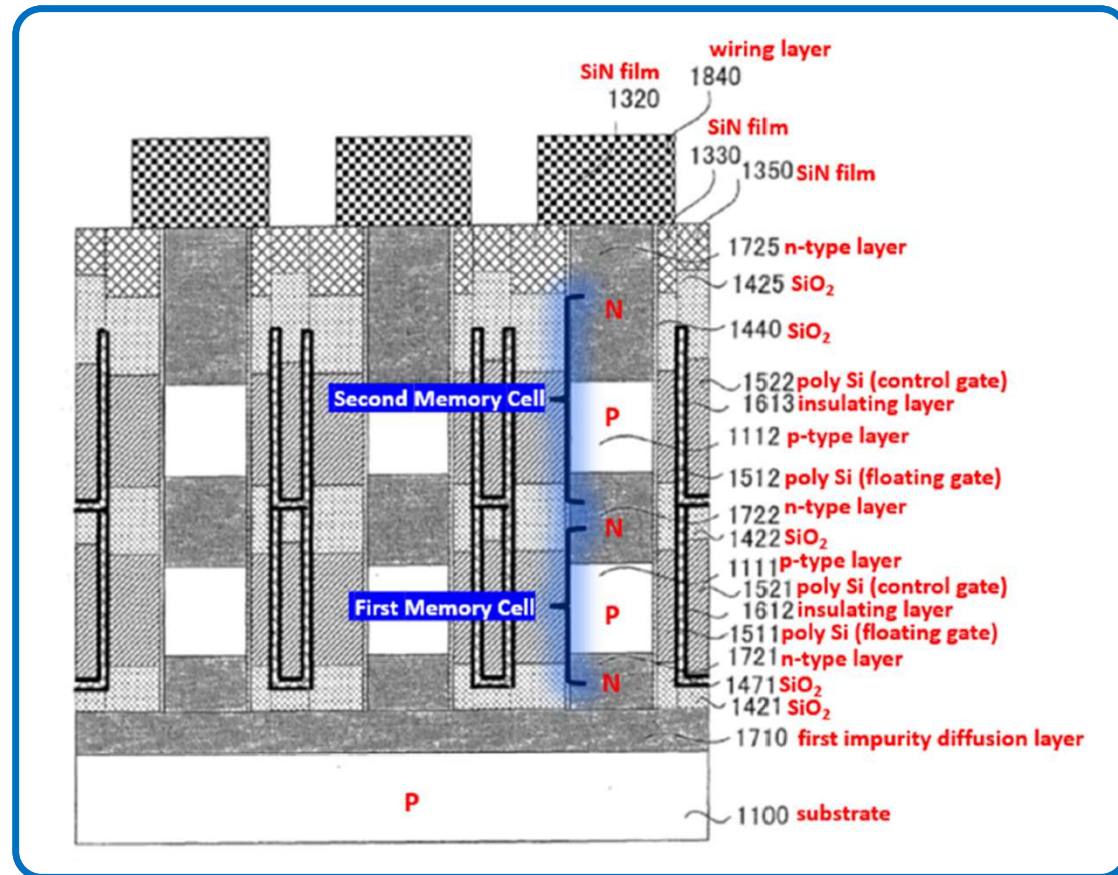
'941 patent, Figure 4D



Ex. 1005, Fig. 4D

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

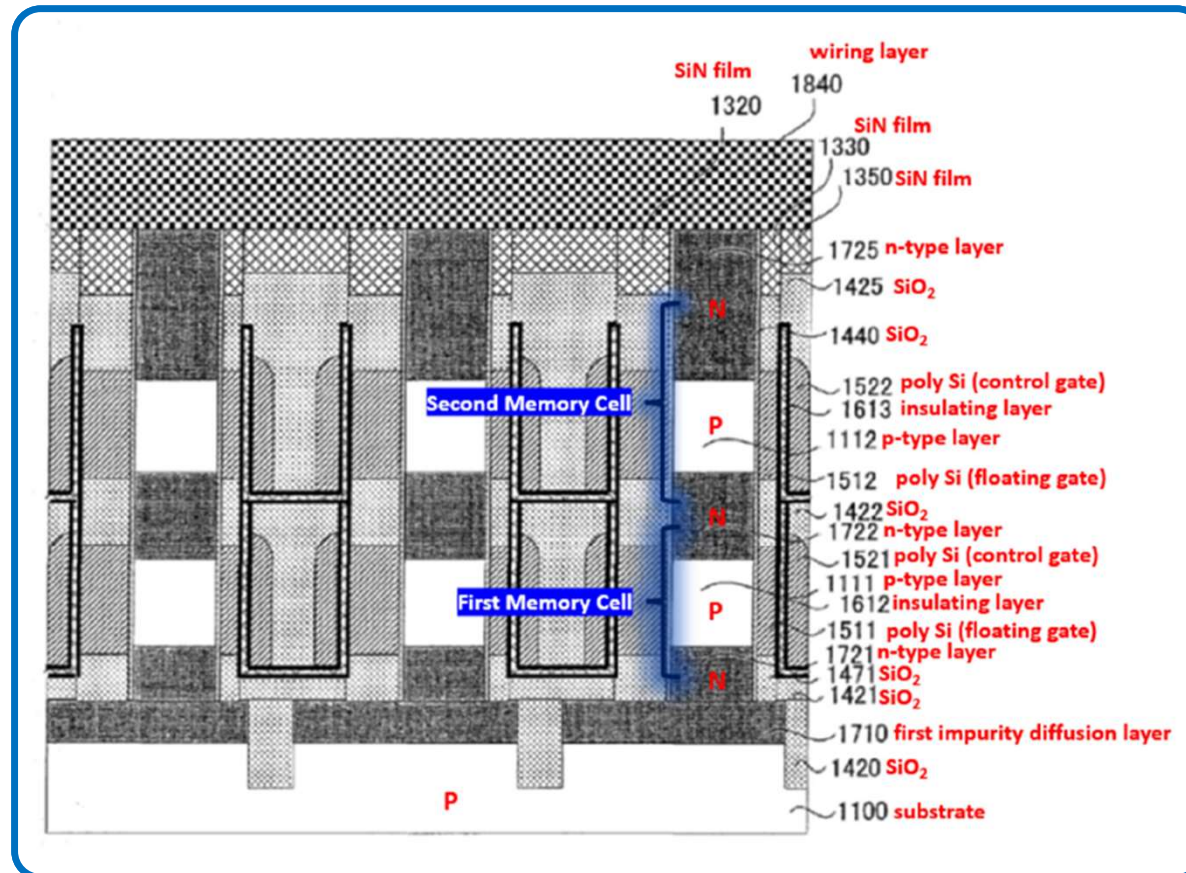
Endoh, Figure 1171



Pet., 44; Ex.1012

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Endoh, Figure 1172



Pet., 45; Ex. 1012, Fig. 1172

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served a true and correct copy of the foregoing: **PETITIONER’S DEMONSTRATIVE EXHIBITS** by email to the electronic service addresses for Patent Owner:

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