

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,
v.
BESANG INC.,
Patent Owner.

IPR2023-00991
Patent 7,378,702 B2

Record of Oral Hearing
Held: September 18, 2024

Before JON B. TORNQUIST, KIMBERLY McGRAW, and
ELIZABETH M. ROESEL, Administrative Patent Judges.

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P-R-O-C-E-E-D-I-N-G-S

1:02 p.m.

JUDGE TORNQUIST: Good afternoon. We are here for an oral hearing in IPR2023-00991, Intel Corporation versus BeSang. The involved patent is U.S. Patent number 7,378,702. I am Judge Tornquist, and with me are Judges Roesel and McGraw. Who do we have from Petitioner today?

MS. KAISER: Good morning, Judge Tornquist, this is Jessica Kaiser from Perkins Coie LLP, on behalf of Petitioner Intel, with me is LEAP practitioner Dr. Chris Moulder, and we also have on the line in house counsel from Intel.

JUDGE TORNQUIST: Okay, welcome, and Patent Owner?

MS. ARMOND: Good morning, Your Honor. This is Michelle Armond from Armond Wilson, representing the Patent Owner BeSang, and I have with me our LEAP practitioner Yue Amy Han, and this is her first court appearance. She is very excited, she is going to be arguing our motion to exclude.

JUDGE TORNQUIST: Okay, welcome. Per our oral hearing order, each side will have 60 minutes to argue today, but as you both mentioned, you both have a LEAP practitioner today, so 15 minutes extra per side, so 75 minutes total. Petitioner, bearing the ultimate burden of proof, will go first. You can reserve time for rebuttal. Then we'll hear from Patent Owner who can also reserve a short period of time for rebuttal, and then we'll hear the rebuttal and sur-rebuttal arguments.

We have the parties' demonstratives, but if you could make sure as you're going through them to clearly identify what page you're on, it will be helpful for the record. Okay, with that, Petitioner, when you're ready.

1 MS. ARMOND: Your Honor, I'm sorry to interrupt, can I ask a
2 procedural question?

3 JUDGE TORNQUIST: Sure.

4 MS. ARMOND: If the LEAP practitioners are both arguing the
5 motion to exclude, do you want that to be done separately at the end so they
6 get their 15 minutes, or do you want it to all happen at the same time?

7 MS. KAISER: And maybe for clarity, I'll say my LEAP practitioner
8 Dr. Moulder is not arguing the motion to exclude, he's going to argue the
9 Johnson based grounds.

10 MS. ARMOND: Okay, well then never mind.

11 JUDGE TORNQUIST: Perfect. Okay, then Petitioner, when you're
12 ready, and please let us know how much time you'd like to reserve for
13 rebuttal.

14 MS. KAISER: All right, thank you Your Honor, and may it please the
15 Board. I'm Jessica Kaiser, as I said, and I'd like to reserve 20 minutes for
16 rebuttal.

17 JUDGE TORNQUIST: Okay.

18 MS. KAISER: And we're going to share our demonstratives, but I'll
19 also let you know the slide numbers as I go through. So Your Honors, this is
20 a straightforward case of obviousness. BeSang tries its level best to make it
21 seem complicated, identifying hurdles that simply don't exist and are not
22 supported by the record. During the argument, I'll break those down to cut
23 through to what the Board really needs to decide and what the record really
24 supports.

25 And when all of the misdirection and false confusion are cleared
26 away, the facts here are really quite simple. The challenged claims recite

1 generic memory structures that were clearly known in the art, and under the
2 proper constructions of stackable add-on layer being bonded and SOI pillar,
3 those terms require a certain type of fabrication, which was also known. The
4 record here including stacks of objective evidence shows that fabricating the
5 recited structures using known fabrication techniques would have been
6 obvious. Accordingly, the Board should find Intel has proven all of the
7 challenged claims are unpatentable by a preponderance of the evidence.

8 If we go to slide 2, I'm going to start first with an overview of the
9 unpatentability arguments, then I'll turn to claim construction issues, and
10 then the Lee based grounds. As I said, I'll then turn it over to my colleague
11 Dr. Moulder to discuss the Johnson based grounds, and finally, time
12 permitting, I'll touch on the Park/Kim ground for claim 1 and BeSang's
13 motion to exclude.

14 If we go to slide 4, I know the Panel is already familiar with the '702
15 Patent from the recent oral hearing in which Micron is the petitioner,
16 involving the same patent, so I'll dive right into what's at issue here. For
17 slide 4, I want to start out with a brief overview of Intel's combinations.
18 Intel presented its grounds for claims 13 through 17 like building blocks. So
19 for claim 13, Intel presented two base references, Lee or Johnson. Either of
20 those references teach most of the structural limitations of claim 13, and Lee
21 teaches the structural limitations of dependent claims 14 through 17. Intel
22 then added to the base references Kim or Aspar, for teaching the stackable
23 add-on layer, under the Board's preliminary construction or Intel's proposed
24 construction for that limitation. In addition, Aspar teaches an SOI pillar
25 under Intel's proposed construction, which the Board preliminary adopted at
26 institution. And Endoh is an alternative to Lee for the structural limitations

1 of dependent claims 16 through 17. Finally, we have a ground, ground 3,
2 the Park and Kim combination, which renders independent claim 1 obvious.

3 If we go to slide 5. So the bottom line here is that if the Board adopts
4 its preliminary constructions from the institution decision, only certain of
5 Intel's grounds for certain claims are in play, and those are shown here. For
6 the Lee based grounds, I'm going to focus in this argument on grounds 1E
7 and F, which cover all the challenged claims other than claim 1, but of
8 course I'm happy to answer any questions that the panel has about other Lee
9 based grounds, and I want to emphasize that focusing on these two grounds
10 for purposes of this argument doesn't mean Intel is abandoning the other
11 grounds, rather what I'm saying is that assuming that the Board adopts its
12 preliminary constructions, these are the grounds that the Board needs to
13 focus on or should analyze.

14 JUDGE ROESEL: So Counsel, why is Lee and Aspar stronger than
15 Lee and Kim?

16 MS. KAISER: Lee and Aspar, for purposes of claim 13, I think Lee
17 and Aspar, they're both strong, so I don't think one is stronger than the
18 other. The reason that I'm going to focus on Lee and Aspar is that it also
19 covers the Petitioner's proposed construction of SOI pillar, which the Board
20 preliminarily adopted at institution.

21 If we go to slide 8, I'm going to transition to claim construction, and
22 this slide shows the constructions at issue here, that is for the claim term,
23 stackable add-on layer being bonded, and the term SOI pillar, which is in the
24 dependent claims. And notably, these terms both need to be construed for
25 the Board to determine which grounds it needs to analyze. For stackable
26 add-on layer, the Board preliminarily construed this term at institution based

1 on the intrinsic evidence, and the record has not changed in the way that the
2 Board should deviate from its preliminary construction for purposes of its
3 final written decision. BeSang had the opportunity to propose an alternative
4 construction, they chose not to, and so the construction that the Board
5 preliminary adopted is the one that it should adopt for purposes of the final
6 written decision.

7 As to SOI pillar, at institution the Board preliminarily adopted Intel's
8 proposed construction, and after institution BeSang did propose a
9 construction for this term as a silicon non-insulator structure taller than it is
10 wide. But it's our position that BeSang's proposed construction is incorrect
11 because it merely expands the SOI acronym and seeks to limit the term to an
12 aspect ratio that is not required by the intrinsic record.

13 If we go to slide 11. Intel's construction of pillar is supported by the
14 intrinsic record. Here, this slide shows for example at column 6 and in its
15 figures that the '702 Patent refers to its SOI pillar as a vertical stack
16 structure, but it doesn't limit those structures to any particular aspect ratio.
17 If we go to slide 12, in addition, SOI and SOI pillar is not a simple
18 expansion of the acronym as BeSang argues, but rather refers to the claimed
19 pillar's creation and composition. And I want to flag in particular the call
20 out that is at the bottom left of this slide. This is from the '941 Patent, which
21 is the parent of the '702 Patent, it has the same named inventor, and it was
22 incorporated by reference in its entirety in the '702 Patent. So this
23 effectively is part in parcel of the '702's written description.

24 And you can see here the last sentence of that call out says, because
25 single crystalline semiconductor layer 124 is formed by SOI technology, it is
26 referred to herein simply as an SOI. And so that is the intrinsic support for

1 the portion of Intel's proposed construction, formed in a stackable add on
2 layer added using SOI technology.

3 And one last note on claim construction, there's no contention from
4 BeSang that any of the references that Intel relies on as teaching as SOI
5 pillar don't meet BeSang's proposed construction for that term. And
6 BeSang's expert admitted as much at his deposition. If there are --

7 JUDGE TORNQUIST: This is Judge Tornquist. I have a question on
8 the stackable add-on layer. How much of that do we actually have to
9 construe, to pick which grounds we're going to go forward addressing here.
10 Because, could we just do the last sentence that we put in, that stackable
11 add-on layer does not cover a device that's formed by sequential deposition?

12 MS. KAISER: So if you can go back to slide 8. So Your Honor, I
13 believe that in order to make that determination, it would be both of the first
14 two parts on this slide, a layer that's formed separately from the substrate
15 and then bonded to the substrate or dielectric layer above the substrate, and
16 then additionally that it's formed by -- or does not include memory cells that
17 are formed by sequential deposition. I think both of those pieces together
18 show that you wouldn't need, for example, to analyze the Lee only ground,
19 or the Johnson only ground.

20 JUDGE TORNQUIST: Okay.

21 MS. KAISER: If there are no other questions about claim
22 construction, I'll turn to the Lee based grounds. And if we can go to slide
23 14. So I'm going to start first by talking about claims 13 through 15,
24 because they present different issues for the Board to decide than claims 16
25 and 17, which I'll turn to next. So on slide 14, Lee's Figure 35 shows most
26 of the structural limitations of claim 13. And that's not disputed. For claim

1 13, the only disputed issue for ground 1E, which is the Lee and Aspar
2 ground, is motivation to combine.

3 And so if we skip to slide 21, this slide summarizes the motivations to
4 combine the Intel presented in this case for Lee and Aspar and Lee and Kim.
5 As I said, I'm going to focus on Lee and Aspar. And this slide provides the
6 various motivations that Intel provided as well as the support in the petition,
7 the reply, and the expert testimony and objective evidence that support those
8 motivations. If you go to slide 22, this slide shows that Aspar itself
9 describes benefits that would have motivated a person of ordinary skill in the
10 art to use its techniques with Lee's structure. And those are shown here at
11 Aspar page 834 and 839, including transferring thin layers of very good
12 thickness, homogeneity, and with a high crystalline quality. And Patent
13 Owner BeSang never addressed this in the POPR, and so this alone, the
14 evidence in Aspar itself is enough to support motivation to combine Aspar
15 with Lee.

16 But Intel didn't stop there. If we go to slide 23, Intel also showed that
17 the obviousness rationale from the Intel versus PACT case is met here. In its
18 sur-reply, BeSang invites the Board to commit error by requiring too high a
19 bar for motivation to combine, in arguing that the Federal Circuit in Intel
20 versus PACT not find a showing of suitable options sufficient. But as
21 shown on this slide, the court clearly said that improvement in a categorical
22 sense was not required, and the Federal Circuit reiterated this just a month
23 ago in the Cisco versus K. Mizra decision, where the court found the Board
24 should have evaluated motivation independent of whether a POSITA would
25 recognize any benefit in making the proposed combination.

1 If we go to slide 24. Intel, in its petition, applied the test from Intel
2 versus PACT and showed that there was a known problem in Lee that is
3 fabricating 3D memory structures, and explained that Aspar's wafer bonding
4 described a known solution to that problem.

5 JUDGE TORNQUIST: Counsel, this is Judge Tornquist. Was there
6 actually a problem, or it is just a method? Because Lee doesn't say that it
7 had any problem with depositing the layers, right?

8 MS. KAISER: That's fair. I think the problem that Lee identified
9 was increasing density through the 3D structures, so it's not necessarily
10 identifying a problem with its own method, but it's identifying a problem in
11 the art that you want to create these 3D structures to increase density. And
12 Aspar provides a known technique for doing that, in other words, deposition
13 as discussed in Lee was a known technique, wafer bonding, which is also
14 discussed in Lee was a known technique. And both of these known
15 techniques would have been an obvious way to create these 3D memory
16 structures.

17 JUDGE TORNQUIST: But Lee also gets that increased density,
18 correct?

19 MS. KAISER: That's true. So if we go, for example, to slide 28, our
20 combination, the Lee/Aspar combination, results in the same structure. And
21 so I believe at institution the Board had questioned whether doing bonding
22 would result in some sort of density deficit, and the answer in what the
23 evidence shows in the record here is that that's not true, because the
24 combination forms the same structure, so therefore would have the same
25 density of devices. So I agree with you that density is the same, but Intel has

1 shown other benefits that would have motivated the Lee/Aspar combination.
2 And if we go to slide 29 --

3 JUDGE ROESEL: Counsel, this is Judge Roesel, before we move
4 away from slide 28, the excerpt from the petition there, the diagram, that's
5 the Lee and Kim combination, correct? Not the Lee and Aspar
6 combination?

7 MS. KAISER: Oh, I believe you're correct, Your Honor. So let me
8 clarify that, thank you for that. So -- but the ultimate result is the same. So,
9 because what the Lee and Aspar combination does is it transfers the layer
10 stack and then splits off the substrate and then forms the memory cells. And
11 so the Lee/Aspar combination would ultimately be just like what's shown in
12 here from the petition, it just wouldn't have the substrate on the top, because
13 that would be split off before the memory cells are fabricated from the layer
14 stack. But either way, either combination, Lee/Kim or Lee and Aspar
15 ultimately results in the same structure that Lee has, and so the density
16 would not be different.

17 JUDGE ROESEL: Okay, so the way that Petitioner proposed to
18 combine Lee and Aspar, that's shown on Petitioner's slide 18, is that right?

19 MS. KAISER: Can we go to that slide, 18? That's correct, and then
20 as I was saying, then after the layer stack transfer, the petition explains that
21 the memory cell devices would be fabricated from the dope stack structure
22 that was transferred.

23 JUDGE ROESEL: Yes, but the process that Petitioner has depicted
24 on slide 18 and also in the petition at pages 59 and 60, that omits the
25 hydrogen implantation step described in Aspar, is that right?

1 MS. KAISER: That detail is not discussed in that figure, that's
2 correct.

3 JUDGE ROESEL: Yeah, but that step is critical to Aspar's bonding
4 and cleaving method, isn't that right?

5 MS. KAISER: So Your Honor, it is correct, and there's been no
6 argument raised about the implantation step, but the idea behind this
7 combination and in implementing Aspar's process in the combination would
8 be that you would have that detached layer or the hydrogen implantation at
9 the place that you want to perform the substrate splitting. And so that would
10 be at the interface between the dope stack and the substrate.

11 JUDGE TORNQUIST: So this is Judge Tornquist, can I ask a
12 question, I think you'll probably get to it, it's my understanding that this
13 stack of the N positive, P minus, N positive, is actually the thin silicon layer
14 that's shown in Aspar?

15 MS. KAISER: That's correct, Your Honor, and I think that is at slide
16 35, if you go to that. This is an argument that BeSang made that Aspar
17 would leave a thin silicon layer, and so that would somehow prevent the
18 combination, but as you said, Judge Tornquist, the thin silicon layer that we
19 would be transferring in the combination is the dope stack, and so that's
20 what's desirable for the combination, not an impediment to it.

21 JUDGE TORNQUIST: Okay. Let me ask one more question. The
22 claims require that the stackable add-on layer that's bonded has memory
23 cells. I don't think anyone's arguing this, but how is the stack that's un-
24 patterned a memory cell?

25 MS. KAISER: So the stack that's un-patterned isn't a memory cell
26 itself, it's the stackable add-on layer that's bonded, and then ultimately in

1 the structure it has memory cells, and that's consistent with the process that,
2 for example, is in the incorporated by reference '941 Patent, to transfer the
3 layer stack and then form the memory cells. And BeSang hasn't argued that
4 that wouldn't meet Intel's proposed construction of stackable add-on layer.

5 JUDGE TORNQUIST: Okay.

6 JUDGE ROESEL: So Counsel, the objective of your combinations,
7 Petitioner's combinations of Lee and Aspar and Lee and Kim, is to get at the
8 Lee Figure 35 structure, right, with the multiple layers of memory cells, a
9 vertical -- a three dimensional array of memory cells, isn't that right?

10 MS. KAISER: Your Honor, it would be at least to get to the first
11 level, 3104 of Figure 35, you know, a person of ordinary skill in the art
12 could then decide how many levels they wanted to have in the array and
13 what processes they wanted to do for the next levels, but claim 13 only
14 requires one level.

15 JUDGE ROESEL: Yes, but the person of ordinary skill in the art
16 wouldn't want to combine these references in a way that yields something
17 that's less advantageous than what Lee itself teaches, right, which is this 3D
18 memory array?

19 MS. KAISER: That's true. And --

20 JUDGE ROESEL: So what does Petitioner's combination of Lee and
21 Aspar and then Lee and Kim, how does that reach the structure shown in Lee
22 Figure 35? That's not shown in Petitioner's combinations, is it?

23 MS. KAISER: So if we can go to the slide that has -- 14 would be
24 fine. So Your Honor, it is correct that Lee shows a three level memory array
25 here. And BeSang hasn't argued as in opposition to the motivation to
26 combine, that our combinations have fewer levels. That said, I believe the

1 petition does address the idea of adding additional levels, and that a person
2 of ordinary skill in the art would understand that that could be performed
3 either with additional wafer bonding steps, so essentially you wafer bond
4 one level with Aspar, you form the memory cells, then you form an
5 additional dope stack, wafer bond that. It's really no different than how Lee
6 itself does it, it's just Lee is, you know, we've talked in our papers about
7 how it's ambiguous for the first level how that's formed, but the subsequent
8 levels, we disclose those are deposited, and doing that, transferring the dope
9 stacks by bonding would really be a similar process and would be obvious
10 for the same reasons that Lee talks about for deposition.

11 JUDGE ROESEL: So where is that multiple levels of wafer bonding,
12 where is that proposed in the petition?

13 MS. KAISER: I can get you that cite and come back to it, if that's all
14 right. So Judge Roesel, I'll get you that cite and come back to it. But in the
15 interest of time, I want to go back to motivations to combine that Intel did
16 show. And as I mentioned before, if we go to slide 27, Lee discloses
17 bonding as a potential technique for use in its structures. And so you see
18 here in paragraph 208, Lee discloses wafer bonding specifically, and in 107,
19 it at least suggests bonding techniques by talking about two dimensional
20 arrays that are formed separately and then packaged together.

21 If we go to slide 29, Intel also explained that a person of ordinary skill
22 in the art would have recognized that bonding allows for testing that
23 improves yield, and so for example, the top right call out on the slide,
24 Exhibit 1055, is the Guarini reference, and it says, it's talking about
25 individually testing and then stacking layer devices using wafer bonding,
26 and it says, we believe this approach should improve yield and reduce

1 manufacturing costs compared to “bottom up” techniques in which devices
2 in each layer are sequentially processed.

3 JUDGE TORNQUIST: Counsel, this is Judge Tornquist, can I ask
4 just a fundamental question about your combination as I understand it? As I
5 understand, you can have a large wafer, with individual dies throughout that
6 wafer, and then they could be tested and see which one’s working or not.
7 Are you going to bond that entire wafer with another wafer? Or are you
8 cutting those dies and making chips and stacking only the good chips on
9 other good chips?

10 MS. KAISER: So this is a question that’s a little bit different between
11 Kim or between Aspar. So for Aspar, because what’s being transferred is
12 the layer stack, you’re going to be bonding the entire wafer transferring the
13 layer stack. For Kim, where you’re forming complete devices prior to
14 bonding, you would again be likely doing the whole wafer. The question I
15 suppose would be if you had a very problematic wafer, where you had a lot
16 of bad devices, you might choose to scrap that part of the wafer and start
17 over before you bonded them. So it wouldn’t necessarily be scrapping
18 individual dies prior to bonding, but it would allow a person of ordinary skill
19 in the art the choice whether to bond or not before they found a big problem.

20 JUDGE TORNQUIST: Okay, because I understand your reference to
21 say hey, there could be a 70% yield for one wafer, and 70% for another, so
22 you’re coming down to like 49%. How are you changing that by testing,
23 because you’re going to have the same problem, if you’re putting the wafers
24 together?

25 MS. KAISER: Well, if we go to slide 30, maybe first focusing on the
26 Aspar combination, what the Aspar combination would allow you to do, and

1 BeSang argues that you can't test layers, or there's nothing to test in this
2 combination, and the objective evidence shows otherwise. We've pointed to
3 references, for example, here on this slide that show that a person of
4 ordinary skill in the art understood how to test layers. And what this would
5 allow you to do is if you had, for example, a defect in your layers, whether it
6 was thickness problem, a problem with the doping in your stacked layer, it
7 would allow you to scrap the layer and start over on that separate wafer
8 before you bonded, so that what you're not doing is you're not affecting the
9 structure that you've already formed. So that's the benefit to testing and the
10 yield improvement that is through the Lee/Aspar combination.

11 JUDGE TORNQUIST: So you would take the entire wafer, and if
12 you felt that too many were defective, you would take that whole layer off
13 and start over again?

14 MS. KAISER: That would be one option that a person of ordinary
15 skill in the art would recognize. And the important thing about that is it
16 gives you the option to do that before you've affected the structures
17 underneath, whereas if you're doing deposition and you lay something bad
18 on top of it, or you have some sort of problem, you might have to scrap the
19 entire thing, because now you've affected your entire underlying wafer and
20 all the fabrication that you've done underneath.

21 JUDGE TORNQUIST: Okay, that makes a little more sense to me.
22 Is that put into your petition or in the expert's report, to just scrap the layer
23 and re-do it?

24 MS. KAISER: Certainly Dr. Sechen talked about both process
25 optimization and the testing of layers. Whether he went into that additional
26 detail, I'd have to go back and look, Your Honor.

1 JUDGE TORNQUIST: That's fine, if you have a cite that would be
2 helpful.

3 MS. KAISER: Okay.

4 JUDGE TORNQUIST: Thank you.

5 JUDGE ROESEL: Counsel, this is Judge Roesel. I'm still a little
6 confused about this issue of testing in Aspar, because in Aspar it's talking
7 about building an entire wafer, right, and then wafer bonding that entire
8 wafer on another wafer. And you're saying that first these N plus, P minus,
9 N plus layers would be formed and tested, right? But you're testing the
10 entire wafer that's not yet been subdivided into chips, right, so how is that
11 going to improve the yield? I'm still a little confused by that.

12 MS. KAISER: Sure. So for example, if you did testing and you saw,
13 for example, that your layers had large thickness variations across them, for
14 example, then that could affect whether that was a layer stack that you
15 wanted to transfer. If you did testing and you saw --

16 JUDGE ROESEL: Excuse me, let me interrupt there. When you say
17 a layer stack that you would want to transfer, I mean, in Aspar, they're
18 talking about either you transfer the entire wafer or you don't, so there are
19 no chips yet, there's no subdivision into chips, right? So I don't understand
20 what you mean by layer stack.

21 MS. KAISER: So Your Honor, what I mean by layer stack is exactly
22 what's depicted here on slide 30, where you have the substrate underneath.
23 And you can imagine this is a cross section, for example, of an entire wafer.
24 And so you have the substrate and you have then the layer stack on top of it,
25 the NPN layer stack that you've doped and then you have a bonding metal
26 layer that's the cross hatched portion.

1 And what I'm saying is, there's testing that can be done on layer
2 thickness even if it's a big layer, for example, to see are you getting
3 variations, et cetera. And the point is then, you could look at that and decide
4 whether you wanted to do the wafer bonding before you did the transfer, so
5 that if there was a problem, instead of doing what Lee says, which I believe
6 Figure 9 of Lee shows the deposition, so instead of doing the deposition on
7 what already has been formed underneath, you're looking at, okay, I've
8 formed this on a separate wafer, is this of the quality that I want to then
9 move forward to the next step, which would be wafer bonding. And you can
10 make that choice when you haven't already put things onto all of your
11 underlying structure.

12 JUDGE ROESEL: I guess I still don't see how that reduces waste,
13 you know, because if you've got a defect in your layer you're going to have
14 to throw out the entire wafer, whereas if you have divided it into chips and
15 you test each chip, then at most you're going to throw away one chip, which
16 is a very small portion of a semiconductor wafer.

17 MS. KAISER: Well Your Honor, first of all, you wouldn't have to
18 throw out the entire wafer, because you could simply detach it and use the
19 remaining underlying substrate to do your doped stack structure again. So
20 we're really only talking about discarding the dope stack. And the other
21 difference is, you're talking about discarding entire dies or entire devices,
22 and what I'm saying is, you haven't even gotten to that point. So if you've
23 got your substrate, you've got your underlying devices that are in your
24 substrate, you've put all of that circuitry together, now you don't have to
25 discard all of those pieces, because the only thing you're -- if you have a
26 defect, if you have a problem with the dope stack that you've put over here,

1 you just scrap that layer, use the underlying substrate and do it again, and
2 then you haven't wasted everything that you've already fabricated before.
3 So that's the point about the testing before bonding.

4 But I want to turn to another rationale that Intel provided both expert
5 testimony and objective evidence for, and if we go to slide 31, this goes
6 hand in hand with quality control that Intel talked about in its petition, and
7 that's process optimization. And maybe before I even get into the nitty
8 gritty of this, this is the issue that was raised in BeSang's motion to exclude,
9 is Dr. Sechen's reply testimony about process optimization as well as the
10 objective evidence supporting this rationale.

11 But it's important to note that Dr. Sechen included a process
12 optimization rationale in his original declaration that was filed with the
13 petition. And that's Exhibit 1003, paragraph 213. And the last sentence of
14 that paragraph reads, a POSITA would have recognized that forming
15 electrical devices on one substrate, separately from the memory devices on
16 another substrate would have allowed optimization of respective processes,
17 rather than forcing the memory devices to be formed with a sub-optimal
18 process tailored to preserve any electrical devices formed on a single wafer
19 in a monolithic process. So process optimization was a rationale that was in
20 Dr. Sechen's original declaration. BeSang asked him about it in his first
21 deposition, before the POR was filed, and so this is the proper subjective
22 reply.

23 And you can see here, for example, Exhibit 1050, which is the
24 Niklaus reference at the bottom right, very clearly talks about the advantages
25 of wafer bonding, allows circuits to be independently processed and
26 optimized on different wafers before integrating the transducers on the

1 integrated circuit wafers, and also notes that the devices can be made of
2 monocrystalline silicon.

3 JUDGE ROESEL: I'm going to interrupt you there, Counsel, this is
4 Judge Roesel. That motivation, however, does not apply to Lee plus Aspar,
5 right, because with Aspar, you're not forming your memory devices before
6 you do the wafer bonding?

7 MS. KAISER: So it would still apply, because you would still get the
8 benefit of the monocrystalline silicon, being able to form your dope stack
9 from monocrystalline silicon, which the record shows has improved
10 properties over polycrystalline silicon, which is what you would have to use
11 in deposition. So that separate processing is still a benefit, because it
12 provides a benefit to Aspar's layer stack.

13 JUDGE TORNQUIST: Counsel, this is Judge Tornquist, let me ask a
14 question. Obviously you said that, your declarant mentioned this, but is it in
15 the petition itself that Patent Owner would be sufficiently on notice of it?
16 We see this all the time, experts say a lot of things in the report, but if you
17 don't cite to it, that's going to be a tough thing for us rely on.

18 MS. KAISER: So Your Honor, we did cite to that paragraph of Dr.
19 Sechen's declaration in the petition, and it's at petition 60 to 61. And on the
20 question of notice, it's clear that BeSang did have notice, because they spent
21 at least several pages, I think it's in his deposition, in Dr. Sechen's
22 deposition, which is -- and this is, by the way, his deposition about his
23 original declaration, not his deposition about his reply declaration. So this is
24 the deposition that was based only on the petition and his original
25 declaration. So at Exhibit 2039, at pages 91, line 17 to 98, 13, BeSang asked
26 Dr. Sechen specifically about that statement in his original declaration. So

1 BeSang had notice about it, had an opportunity to question Dr. Sechen about
2 it before they put in their Patent Owner response, before they put in Dr.
3 Pryzbylski's testimony, so they had an opportunity for Dr. Pryzbylski to
4 testify about that rationale if they had wanted.

5 JUDGE TORNQUIST: Okay.

6 MS. KAISER: Okay, I'm going to turn now to slide 32. And I want
7 to discuss this notion that Aspar requires an 1100 degree anneal, which
8 BeSang talks a lot about in its papers, but it's simply a red herring. As you
9 can see on the right hand side, BeSang brings this in from a reference, the
10 Wolf textbook, which is not part of any of the invalidity grounds. And as
11 you can see on the left hand side of this slide, Aspar's process does not
12 include a high-temperature anneal.

13 Instead, if we go to slide 33, Aspar explains that its Smart-Cut process
14 really is a generic process, that it allows a great deal of combinations for
15 material and bonding layer. And so this shows that Aspar's Smart-Cut
16 process is not a rigid process requiring a specific high-temperature anneal
17 that would make it unsuitable for many materials. And so accordingly, Dr.
18 Sechen consistently refers to Aspar's Smart-Cut process, not Smart-Cut
19 generally, and certainly not Wolf's Smart-Cut process. And in BeSang's
20 arguments where BeSang is contending that Dr. Sechen admitted otherwise,
21 they're simply pointing to testimony where he was specifically asked about
22 what the Wolf textbook and its figure showed, he did not admit at any point
23 that Aspar's Smart-Cut process required an 1100 degree anneal.

24 This is further underscored, if we go to slide 34, by the '941 Patent
25 disclosure, again this is the same inventor, so the same inventor as the '702
26 Patent, incorporated by reference into the '702 Patent, and here the same

1 inventor referred to the Smart-Cut process, used it for low-temperature
2 processing, here below 650 degrees, just like what '702 Patent says, and the
3 '702 inventor in this disclosure also did not disclose a high-temperature
4 anneal between the splitting step and the polishing step, just like Aspar.

5 Now I don't point to this as some sort of hindsight way to say, to use
6 the patent as support for obviousness, but only to show that the same
7 inventor recognized in the prior art, or recognized that Smart-Cut didn't
8 require a high-temperature anneal, and that's, again, just to support that
9 that's how a person of ordinary skill in the art would have understood Aspar,
10 which also doesn't mention a high-temperature anneal.

11 If we can go to slide 37. There was a question at institution decision
12 for the Lee/Aspar ground about whether Petitioner has explained how that
13 combination would have resulted in the SOI pillar under Petitioner's
14 construction for that term, and so this slide simply shows with cites to the
15 petition how we mapped SOI pillar to the Lee/Aspar combination in the
16 petition itself.

17 If we go to slide 38, I wanted to flag here that Lee Figure 25A isn't
18 needed for Intel's grounds as to claims 13 through 15. And so anytime in
19 BeSang's briefing or in Ms. Armond's argument today, you see a reference
20 to Lee's Figure 25A, I want you to remember that that argument only applies
21 to claims 16 and 17, and only to those grounds that don't include Endoh for
22 those claims.

23 I'm going to turn now to claims 16 and 17, so if we go to slide 40. So
24 where Lee's Figure 25A does matter is for ground 1E, which is the
25 Lee/Aspar ground, and for claim 16 and 17. Intel did map Figure 25A to
26 those claims, and for claim 16 you can see here there are two memory cells

1 in a single pillar, and those memory cells are electrically connected by metal
2 layer M2. If you go to slide 41, this is claim 17, and you can see here that in
3 Figure 25A, the first pillar with two memory cells is electrically connected
4 to a second pillar which also has two memory cells through metal layer M1.

5 BeSang argues that the memory cells in Figure 25A cannot be serially
6 connected because there is no top interconnect line, but it's important to note
7 that interconnect line is a separately recited element in the claims, and so
8 claim 16 doesn't recite an interconnect layer at all, and for that claim, two
9 memory cells are serially connected when they are electrically connected
10 one after the other, and that's disclosed in Lee Figure 25A. Claim 17 recites
11 only one interconnect line, that's the interconnect line that's disposed on the
12 dielectric layer, and so the pillar from the first pillar is serially connected if
13 it's electrically connected one after the other to another pillar, which is again
14 shown in Figure 25A.

15 JUDGE TORNQUIST: So Counsel, this is Judge Tornquist. I'm
16 having a little difficulty with this, because we know that Lee is a NOR
17 memory structure, right, which is parallel connected?

18 MS. KAISER: Well in Figure 25A, it's not NOR or NAND.

19 JUDGE TORNQUIST: I know, but we know what they're trying to
20 get to, you've picked a processing step, a point in the processing step, but we
21 know that's not what they were trying to do, right?

22 MS. KAISER: Well certainly we know that when Lee applied other
23 processing steps to its Figure 25A and got to a commercially final structure,
24 it did show a NOR structure, but commercial finality is not required for
25 obviousness, and so the structure that is in Figure 25A meets the limitations
26 of these claims as BeSang chose to claim them.

1 JUDGE TORNQUIST: Just so I understand scientifically, can this
2 particular embodiment at 25A work? Does it actually work as a memory
3 cell?

4 MS. KAISER: It does work as a memory -- so it's not connected, in
5 other words, it doesn't have enough interconnection layer, or interconnect
6 lines so that you could use it as a final product. But it does have the
7 structural components of a memory cell, because it has its transistor and it
8 has a charge storage member. And so structurally, it is a memory cell.

9 JUDGE TORNQUIST: So you could store data in these structures as
10 it's showing in 25A?

11 MS. KAISER: In 25A you could choose to connect the memory cells
12 however you want, you could choose to connect them in a NAND fashion,
13 you can choose to connect them in a NOR fashion, and when you have
14 connected them in whatever fashion a person of ordinary skill in the art
15 chose to do, then you would be able to store charge in them, yes.

16 JUDGE TORNQUIST: Yeah, but you're saying right here, 25A is
17 serially connected. That doesn't look like it's operable yet, so it's not really
18 a memory. That's what I'm struggling with, it's sort of picking this
19 independent spot in the processing and saying that's our memory cell,
20 serially connected.

21 MS. KAISER: So all the claims here require structure, they don't
22 require function, they don't recite the memory cells functioning in a
23 particular way. And what they recite is how the different pieces of structure
24 are connected to each other, and as shown in Figure 25A, the two memory
25 cells are serially connected to each other by virtue of the fact that they're
26 electrically connected to each other one after the other.

1 JUDGE TORNQUIST: Okay.

2 MS. KAISER: But Your Honor --

3 JUDGE ROESEL: Counsel, before you move on, this is Judge
4 Roesel, I'm still very confused here, because you're talking about Figure
5 25A of Lee, but we've already looked at Petitioner's slide 18, which you
6 said shows how Petitioner proposes to combine Lee and Aspar, and that
7 slide as well as the corresponding portion of the petition shows combining
8 Lee Figure 9a with Aspar. And there's no memory structures there at all, no
9 first memory cell, second memory cell at all, so I'm not sure how Petitioner
10 showed how you get from this combination to Figure 25A.

11 MS. KAISER: Well Your Honor, so Petitioner, I believe it's in our
12 reply, talked about how you would, if you were making Figure 25A in the
13 Lee/Aspar combination, you would have a dope stack, you would have a
14 metal layer, and then you would have another dope stack, and that's what
15 you would transfer. And then just like in the combination that used Lee's
16 other single level memory cell structures like Figure 1A, like Figure 1B,
17 then you would do your processing afterwards, to make the separate pillar
18 structures.

19 JUDGE ROESEL: That's not in the petition, is it?

20 MS. KAISER: Your Honor, I'll go back and look, but certainly the
21 petition has the concept of transferring what layer stack is needed for the
22 specific memory structure, and then forming the memory cells from the
23 transferred stack.

24 JUDGE ROESEL: Where is that discussed?

1 MS. KAISER: That is discussed at petition page 60, this is in the
2 Lee/Aspar ground. And there in particular on page 60, the petition discusses
3 that Aspar teaches that you can transfer multiple SOI layer stacks.

4 JUDGE TORNQUIST: So Counsel, this is Judge Tornquist, as you
5 get going, you're kind of getting close to your reserved time, and we haven't
6 heard from the LEAP, I just want to make sure that you take that into
7 account as you move forward. We've asked you a lot of questions, but I just
8 want you to keep that in the back of your mind.

9 MS. KAISER: Yes Your Honor, and I certainly do not want to
10 impinge upon Dr. Moulder's time. I'll just briefly make a couple of points
11 about the Lee/Aspar/Endoh combination. And if we go to slide 44. So in
12 addition to Lee alone, Endoh is explicitly clear that its transistors are
13 connected in series, so to the extent that the Panel has concerns about that, I
14 just wanted to point out that there's no question and no dispute that in Endoh
15 the transistors are serially connected. And then if we go to slide 45.

16 BeSang's arguments about the Endoh combination seem to be focused
17 on an idea that Intel's combination is somehow combining Lee Figure 25A
18 with Endoh's memory cells, and in this combination, the only thing that Intel
19 relied on Lee's Figure 25A was just to show that Lee contemplated the
20 concept of having multiple cells in the same pillar, but in the combination
21 itself, Intel proposed two different options. One is using Lee's Figure 1B
22 structure, and using that essentially to stack two in the same pillar, and the
23 other option would be implementing Endoh's memory cells in a level of
24 Lee's Figure 35.

25 Just very briefly, if we go to slide 49, this slide just, one of the things
26 that BeSang argued was that Intel didn't show that the Lee/Endoh/Aspar

1 combination meets the limitations of claim 13 from which claim 16 and 17
2 depend. This slide just shows that the petition did address that issue and did
3 show how Intel's proposed combinations met the limitations of claim 13
4 from which 16 and 17 depend. And then if we go to slide 50, I just want to
5 touch briefly on at institution the Board expressed some concerns about
6 Petitioner's cross references for 1F, and this slide just shows again the
7 building blocks in the petition that show how what's in the petition adds up
8 to the Lee/Aspar/Endoh combination to teach all the limitations of those
9 claims as well as to address the motivations to combine.

10 So at this point, I'll hand it off to my colleague Dr. Moulder, who is
11 going to discuss the Johnson based grounds for claim 13.

12 JUDGE TORNQUIST: Okay, so we've asked a lot of questions and
13 there's been a lot going on in this case, so we're going to give your LEAP
14 practitioner up to 15 minutes without going into your rebuttal time, but
15 whatever time he uses we're also going to give to Patent Owner to use as
16 well, okay?

17 MS. KAISER: Okay. Thank you, Judge Tornquist.

18 DR. MOULDER: Thank you, and may it please the Board. Sorry,
19 we're having technical difficulties. Testing. Okay. Thank you, may it
20 please the Board, Dr. Chris Moulder for Intel. Can you please turn to slide
21 52? So the disputes regarding Johnson's, the grounds 2A to 2C are quite
22 simple. Does Johnson include a transistor in its vertical memory cell? It
23 does. And would a person of skill in the art have combined Johnson with
24 Aspar or Kim? Again, yes, and for the same reasons as my colleague Ms.
25 Kaiser has explained for Lee.

1 Turn to slide 53. So let's delve a little deeper. BeSang's argument
2 that Johnson does not disclose a transistor cuts across all Johnson grounds,
3 but as shown here, Johnson expressly discloses using JFETs or MOSFETs in
4 its memory cells, and both of those are transistors, and those transistors are
5 configured to act as a diode, known in the art, well known in the art to be a
6 diode-connected transistor. So this type of transistor configuration has one
7 input and one output, because the gate is being controlled by either the
8 source or the drain, depending on which one it is connected to.

9 Turn to slide 54. Now BeSang will tell you that because Johnson's
10 memory cell has two explicit terminals, a transistor cannot be used as its
11 steering element, but Johnson also explains that each memory cell has
12 additional terminals which are implicit rather than explicit, and that those are
13 unavoidable consequences of its construction. BeSang bases its theory on
14 the notion that a diode-connected transistor's function transforms it from a
15 diode into a -- sorry, transforms it from a transistor into a diode with a
16 different number of terminals. But even though the transistor may act as a
17 diode, it's still a transistor.

18 Turn to slide 55. In fact, the objective evidence shows that diode-
19 connected transistors are consistently described as transistors in the art. As
20 shown here, Intel has shown that even when the transistor operates like a
21 diode, it's still described as a transistor.

22 JUDGE TORNQUIST: Counsel, this is Judge Tornquist. In the stack
23 that we see, so the --

24 DR. MOULDER: BeSang would have you believe that the function
25 of a diode-connected transistor does not meet the claim language, but as Dr.
26 Sechen has explained, claim 13 recites a memory structure, not any specific

1 function of that memory or the transistor contained within it. Neither claim
2 13 nor the '702 specification limit how the transistor is used or connected,
3 and BeSang has not argued otherwise. Claim 13 only recites a memory cell
4 containing the structure of a transistor, no matter how it is used. But in an
5 attempt to show its transistor is not a transistor argument, BeSang goes on to
6 claim that first Johnson either taught away from using transistors, but even if
7 it didn't, those transistors were not enabled. Both of those arguments are
8 contrary to the evidence in record. Turn to slide 57.

9 JUDGE TORNQUIST: Counsel, can I ask a question? I'm thinking
10 you may not be able to hear me.

11 DR. MOULDER: BeSang's only evidence that --

12 JUDGE TORNQUIST: Maybe Ms. Kaiser, if you're there, you can
13 see if we're having a technical problem?

14 DR. MOULDER: -- is a discussion in Johnson in its background of
15 the invention where it's discussing prior art memory cells, and still those
16 criticisms are only that transistors were used in a planar substrate, and had
17 complicated gate circuitry. Johnson disclosed however to use the transistors
18 above the substrate with circuitry.

19 PARTICIPANT: Can you hear the Board? I think the Judge has been
20 asking you questions.

21 DR. MOULDER: No I cannot, I'm sorry. I'm sorry.

22 JUDGE TORNQUIST: Okay, this is Judge Tornquist, can you hear
23 me now?

24 DR. MOULDER: Yes, I can hear you now.

1 JUDGE TORNQUIST: Okay, okay. If we could step back just a little
2 bit. I had a question about the transistor. In the stack that is shown in
3 Johnson, the transistor isn't shown there, right, correct?

4 DR. MOULDER: Can we go back to, back one, I think? Sorry, two,
5 sorry, slide 53 I believe. Yeah. So you're talking about the pillars here in
6 the figure?

7 JUDGE TORNQUIST: Yes.

8 DR. MOULDER: Yep.

9 JUDGE TORNQUIST: So these change elements 23 and as pillars, it
10 goes up, are the actual MOSFET or field-effect transistor?

11 DR. MOULDER: Yes, Johnson describes that the MOSFET or the
12 junction field-effect transistor is contained in the steering element, so the
13 bottom portion of that figure.

14 JUDGE TORNQUIST: Okay, so if I could boil this dispute down
15 between the parties, it's is a transistor that's not actually operating
16 necessarily as a transistor, is it still a transistor for the purposes of all the
17 claims?

18 DR. MOULDER: Yes, I think that's correct.

19 JUDGE TORNQUIST: Okay, and your feeling is it definitely is a
20 transistor, no matter how it's wired, so the claims are covered in Johnson.

21 DR. MOULDER: Correct, the claims are only to the structure of
22 transistor, not how the transistor is being used.

23 JUDGE TORNQUIST: Okay, okay thank you.

24 DR. MOULDER: Okay, if we can go back to slide 57? So as I was
25 saying, the criticisms of Johnson for prior art memory cells were that those
26 transistors were used in a planar substrate and also had complicated gate

1 circuitry, but Johnson's invention disclosed that those transistors are used
2 above the substrate, and since they're diode-connected, they removed the
3 complicated gate circuitry. So quite the opposite of BeSang's argument,
4 Johnson actually does teach to use the transistors in a vertically oriented
5 memory cell.

6 Go to slide 58. So regarding enablement, BeSang argues that because
7 Johnson did not provide an in-depth recitation of fabricating vertical
8 transistors, they weren't enabled, but Johnson is presumed to be enabled,
9 and even so, other objective evidence shows that a person of skill knew
10 exactly how to fabricate such transistors in a vertical array. So please turn to
11 slide 59.

12 So Johnson discloses at least two ways of making its memory cells.
13 The first way is using a self-aligning technique, but Johnson also teaches to
14 use photo masking steps to make its pillars and other ancillary features. And
15 as explained in Intel's reply, it was well known to persons of skill how to
16 fabricate vertical transistors this way. And other prior art, specifically Lee,
17 also taught just that, including how to wire the gate using photo masking
18 steps. So in short, Johnson isn't limited to just a self-aligning method, and a
19 person of skill would have understood that. And persons of skill would have
20 further understood to either use the photo masking method or Johnson's self-
21 aligning method, depending on the structure of the memory cell.

22 Can we go to slide 60? BeSang also argues that a person of skill
23 would not have combined Johnson with either Aspar or Kim, but just as my
24 colleague Ms. Kaiser explained for Lee, Johnson also identified the problem
25 of fabricating 3D structures above a substrate with other circuitry, like

1 memory arrays, and Aspar and Kim both addressed the same problem using
2 bonding.

3 I'd like to discuss a couple of specific issues with motivation to
4 combine that are specific to Johnson. Go to slide 61. So first, BeSang
5 argues that combining Johnson with Aspar would prevent a person of skill
6 from using Johnson's self-aligning technique, but it's quite the opposite.
7 Aspar's Smart-Cut allows using Johnsons self-aligned process. Because as
8 shown here, using Aspar's teachings, first the layer of the dope material is
9 transferred to the base substrate using Smart-Cut, which would then be
10 etched and fabricated using Johnson's self-aligned method. Then, if the
11 manufacturer wanted to, additional layers could be fabricated above the
12 transferred layer, also just as Johnson discloses, thus the different layers of
13 the vertical memory cells would be fabricated using Johnson's self-aligned
14 process.

15 Go to slide 62. And finally, BeSang also faults the combination of
16 Johnson with Kim, because so-called strips 53a and 53b are shown as being
17 left after bonding, and this composite figure that was in the petition. But
18 claim 13 does not preclude such strips and besides, Johnson explains that
19 this is just a stopping point, where either more levels can be fabricated on
20 top of them or another metal layer could be placed and etched to end the
21 process.

22 So what's fabricated on wafer A is what the manufacturer would want
23 the structure to be. In short, a person of skill in the art would have known
24 how many levels to fabricate separately before using Kim's technique to
25 transfer them to the substrate with the other circuitry.

1 JUDGE ROESEL: Counsel, let me interrupt you there, this is Judge
2 Roesel. In Petitioner's combination of Johnson and Kim, would that blue
3 substrate be removed?

4 DR. MOULDER: Yes, it would, I believe it would be ground down
5 with CMP.

6 JUDGE ROESEL: Is that taught by Kim?

7 DR. MOULDER: Yes, I believe it is taught by Kim.

8 JUDGE ROESEL: Can you give us a cite for that, please?

9 DR. MOULDER: Yeah, I will look for it and I will provide that to
10 you. So I will get you that cite, but if there are no other further questions, I
11 will turn it back over to Ms. Kaiser.

12 JUDGE TORNQUIST: I have one quick question, this is Judge
13 Tornquist, and maybe this was answered before, but what does Johnson
14 bring that Lee does not? Like why do we have two of these grounds here?

15 DR. MOULDER: So Johnson discloses basically every limitation of
16 claim 13, including the transistors, and the increased density, but as we've
17 shown in the petition, it's only valid for claim 13, and not the other claims.

18 JUDGE TORNQUIST: Okay.

19 MS. KAISER: Trying to avoid creating audio problems. I just want
20 to make sure the Panel can hear me. Your Honor, maybe just to add to your
21 question, I think as the record is developed during trial, I think Johnson and
22 Lee provide similar things for the unpatentability grounds, so you know, I do
23 think that in terms of how they disclose the limitations other than the
24 stackable add-on layer for claim 13, they are similar disclosures.

25 At the risk of eating into a bit of my rebuttal time, I just wanted to
26 circle back quickly to address a couple of Judge Roesel's questions. Judge

1 Roesel, you had asked about Figure 25A in the Lee/Aspar combination, and
2 I just wanted to point you to petition page 59, where the discussion
3 specifically references the Figure 25A structure and transferring that layer
4 stack using Aspar. It doesn't go into the same detail of, you know, showing
5 an annotated figure to show that, but it does discuss it in text.

6 If we could go to slide 25. Oh, maybe before I go there, in Kim, I
7 believe paragraph 25 it does discuss the thinning and polishing step that Dr.
8 Moulder was just mentioning. Okay, so and then if we could go maybe to
9 slide 26. Judge Roesel, you had asked earlier in my presentation about the
10 number of layers in Lee's Figure 35 memory array, and I just wanted to
11 stress that really the modification that Intel is proposing here relates to how
12 the bottom level is attached to the insulating layer, 3102. And the
13 modification doesn't affect then how, or isn't required to affect how,
14 additional levels are formed. So really the modification is simply, instead of
15 depositing that first level, you're doing the first level using bonding instead
16 of deposition, then you could make the additional levels, although they're
17 not required by the claim, you could still form them according to what is
18 disclosed in Lee. So I just wanted to clarify that that is the combination.

19 JUDGE ROESEL: So that description, Counsel, does that apply to
20 both Lee and Aspar, as well as Lee and Kim?

21 MS. KAISER: It does, Your Honor. So again, a person of ordinary
22 skill in the art could choose, for example, in the second level of the array to
23 use bonding or deposition, same for the third, but really the only
24 modification that's required for the combination to meet the limitations of
25 claim 13 is the modification to that first level, because additional levels

1 aren't claimed. And so the claim wouldn't specify that those had to be
2 stackable add-on layers, for example.

3 JUDGE ROESEL: Okay, so in other words, the result of Petitioner's
4 proposed combination does not have multiple memory array layers, such that
5 you get a 3D structure.

6 MS. KAISER: Oh no, you would, you would, because the result of
7 the combination is Lee's Figure 35, it's just that what you're modifying in
8 Lee's Figure 35 is the fabrication step for how that first level is attached to
9 the insulating layer 3102, and that modification is what we showed in our
10 annotated figures. But the resulting structure ultimately from the
11 combination is going to be Lee's Figure 35.

12 JUDGE ROESEL: Okay, one more question, and that is, is there
13 anything about the Johnson plus Aspar, Johnson plus Kim combinations that
14 makes them any more robust as far as combinability of the teachings, as
15 compared with the Lee-led grounds?

16 MS. KAISER: As I sit here right now, I'm not thinking of a specific
17 distinction, but let me go back and look at the petition, and I can address that
18 in rebuttal. So if the Panel has no -- well, let me just say, I think we're
19 happy to stand on our papers for ground 3, which is the ground for claim 1,
20 we obviously still are asserting that ground, and as well as the motion to
21 exclude, which I addressed at least briefly in the context of the motivation to
22 combine.

23 JUDGE TORNQUIST: Okay. All right, so are you finished,
24 Petitioner?

25 MS. KAISER: Yes, Your Honor, thanks for clarifying.

1 JUDGE TORNQUIST: Perfect. Okay, so what we're going to do is
2 we're going to give 15 minutes additional over to Patent Owner, and then we
3 have about six minutes that you went into your rebuttal time, so you'll have
4 14 left when you come back. Okay, with that, Patent Owner, when you're
5 ready.

6 MS. ARMOND: Good morning, Your Honor. So just to clarify, I'd
7 like to reserve 20 minutes for rebuttal, and of course we have 15 minutes for
8 our LEAP practitioner Amy. So how much time do I have?

9 JUDGE TORNQUIST: By my calculations, you have an extra 15
10 above what you already had, and you'd have 90 minutes total.

11 MS. ARMOND: I have like 55 minutes for my case in chief. Okay,
12 great. All right, so let's kind of start where Intel ended, which is what do
13 these grounds mean? So Intel, as we all know, submitted a 95 page petition
14 in this IPR and it included 10 separate -- well, it said it contained 10 separate
15 grounds, and today, Intel spent the bulk of its time talking about the
16 Lee/Aspar grounds, which are grounds 1E and F, and then dipping in and out
17 of the Lee/Kim grounds, which are 1C and D. But most of the pages of their
18 petition are actually about other grounds, like the Lee only ground. And so
19 that silence acknowledges that what's in their petition didn't come close to
20 meeting their burden, particularly on grounds 1A and B, so we can just set
21 those aside.

22 So let me talk about what they did talk about. So let's talk about, let's
23 start with ground 1D. I am going to share my screen, and let's look together
24 at what the Petition actually says. So can everyone see Intel's petition here?
25 Okay, so let's go and start with ground 1D. So this is Intel's petition, we're
26 looking together at page 55, or PDF page 63 for those following along at

1 home. So this is the sum total of Intel's ground 1D, where they are
2 challenging claims 16 and 17 as being obvious over Lee, Kim, and Endoh.
3 It's one paragraph, and that is all that Intel has given the Board and Patent
4 Owner to go on in this IPR.

5 So let's see what it says. Lee and Kim render obvious claims 16 and
6 17 under the proper construction of "the stackable add-on layer being
7 bonded," and Patent Owner's apparent construction of "SOI pillar," and this
8 is, we're getting, here's your analysis. Claims 16 and 17 would have also
9 been obvious over Lee, Kim, and Endoh, under those circumstances. The
10 descriptions of the Lee/Kim combination, section VII.C, the description of
11 the Lee/Endoh combination, section VII.B, and the motivation to combine
12 and reasonable expectation of success discussion for the Lee/Kim, section
13 VII.C.1.b, and Lee/Endoh, section VII.B.1, combinations apply equally to
14 this ground, cite Dr. Sechen's declaration paragraph 200.

15 So that's a lot of cross references. And Intel did a similar thing for
16 ground 1F, which we will get to. And the Board flagged that at institution
17 and said that it had concerns that the cross referencing was not enough to
18 meet Intel's burden here, because they're the petitioner, to show obviousness
19 of the claims. And that is a very valid concern. This paragraph does not set
20 forth a ground of unpatentability with any measure of particularity as
21 required by the statute or board rules, and it certainly doesn't give the Board
22 anything to hang its hat on to rely on to cancel the patent claims. Obviously
23 here the combination is Lee, Kim, and Endoh, but they're relying on
24 different grounds, they're relying on Lee and Kim, and Lee and Endoh,
25 which are different combinations, and then incorporating other motivations
26 to combine and reasonable expectation of success. And as the Board

1 recognized at institution, in ground 1F, that is not good enough to meet its
2 burden under Magnum Oil Tools.

3 So you could stop here and confirm the claims over what is presented
4 here as ground 1D, which is not even a ground, but let's keep going. So as
5 you noticed when I was reading, there's a reference here to section VII.C,
6 which is the Lee/Kim combination, that's actually ground 1C, and then
7 there's another cross reference back to ground 1B. So the problem with this
8 is, ground 1B and ground 1C rely on different claim construction positions.

9 And you don't have to take my word for it, let's look at what Intel
10 said. So again remember, cross referencing back to 1B and 1C. So let's
11 look at, this is Intel's reply brief, and they had to give everyone on reply a
12 table to try to decrypt this, because it doesn't make any sense. So this is
13 what Intel said that they were trying to do, or supposedly, in the petition. So
14 ground 1C, they said they're relying here on Intel's construction,
15 supposedly, for stackable add-on layer, and let's not even get to the
16 footnotes where now they're modifying that, and then they're relying on
17 Patent Owner's apparent construction for SOI pillar and then for 1B they're
18 relying on Patent Owner's construction, the stackable add-on layer, and then
19 Patent Owner's construction for SOI pillar.

20 So if you start to even tease apart what's happening here in 1D, it
21 doesn't make any sense. We have a ground that's supposed to hang together
22 that's relying on inconsistent claim constructions, and again, that's another
23 issue that the Board flagged because there's a similar issue for ground 1F,
24 which is the Aspar/Lee ground, which we're going to get to, and this again
25 doesn't meet their burden. We don't know what the precise combination is
26 here. Under Section 312 of 35 U.S.C., Intel has the burden here to provide

1 grounds with particularity. The Board rules say that you need to have a
2 statement of the precise relief requested for each claim, and you need to
3 identify your claim construction, and then you have to show how your claim
4 is unpatentable under that construction and where each element of it is found
5 in the claims, and that is not here.

6 And of course we have a huge APA problem, because there's no
7 notice and no opportunity to respond here. You know, it's been a guess the
8 whole time. And if you notice, every time the Court was asking Intel, where
9 is this in your petition, it was like, well we have the building blocks there,
10 we have the concepts, because literally their petition has been a moving
11 target through this entire proceeding. But anyway, we're not done, because
12 there's another problem. Claims 16 and 17 are dependent claims. So they
13 incorporate, as we all know, the limitations of claim 13, and here they're
14 relying on a combination purportedly of Lee, Kim, and Endoh to satisfy
15 those limitations, but they never actually go back and do the work and show
16 that that combination of three references actually satisfies the requirements
17 of claim 13.

18 And this isn't like a ticky-tack problem here, the problem is claims 16
19 and 17, those are the ones that require certain things of the memory cells,
20 like they're connected in serial, and claim 13 has other requirements, you
21 have to have vertically oriented memory cells, you have to have non-volatile
22 memory cells with at least one transistor, and they don't ever show that this
23 combination includes those things, and that's like kind of important, because
24 they need to check all their boxes to meet their burden. So this is what we
25 have for ground 1D, this falls far short of Intel's burden, and for any of these
26 reasons, the claims can be confirmed over 1D.

1 But, this isn't the only problem with this petition, because Intel did
2 this over and over again, so we'll go a little faster. So now let's look at
3 ground 1F. This is the other one that we were kind of talking about today
4 for the most part, right? This is Lee, Aspar, and Endoh, and as you can see,
5 it's the same problem. Here we have two paragraphs, not one, but this is it,
6 this is going back to 1E, and look, now we're to Johnson. It's one page of
7 analysis, and again, they're cross referencing back to 1E and 1B. Again, the
8 Board flagged this, too many cross references, who knows what this means?
9 They have the same problem with cross referencing back to 1B and E.
10 These claim constructions, according to Intel in their own reply brief chart
11 are different, so we don't even know what claim construction they're
12 applying, and then again, they never went back and showed that the claims
13 are unpatentable for claim 13. So again, they didn't rebut their case.

14 And then I'm going to just scroll backwards one page on the petition,
15 now we're looking at page 63 of the petition. This is Lee and Aspar, that
16 ground alone, and here Intel is trying to prove unpatentability of claims 14
17 through 17, and again, it's one paragraph with cross references. The Board
18 also flagged, they don't even make an attempt to show what claim
19 construction position they're adopting here. And I'm not actually sure what
20 the combination is, there's a lot of cross references back, but again, who
21 knows?

22 So Intel just spent about an hour talking about grounds that don't
23 actually exist in the petition, and this whole proceeding, every time we point
24 out issues as we try to pick this apart and figure out what they're trying to
25 say here, the grounds always become whatever Intel wants them to be. And
26 I didn't hear a single time where Intel was able to actually identify where

1 these arguments were. At best, at one point Counsel said well, the concepts
2 are in the petition, but the concepts of a ground are not a ground that meets
3 the requirements to meet Intel's burden to show unpatentability. So most of
4 this petition and basically everything that we talked about today on ground
5 1, Intel has not met its burden, and the claims can all be confirmed, just
6 because they didn't do their homework.

7 So we're done talking about cross referencing, let's move on to
8 everything else. Okay, so I'm going to stop sharing for a sec. So let's now
9 talk about why you would depart from Lee to stack, because remember Intel
10 has to prove that up too. Okay, so I'm going to share my screen again.
11 Let's look at Intel's slide, this is Intel's slide 14.

12 So the Petition's original rationale for departing from Lee's teachings
13 about making this monolithic device and going to Kim or Aspar is that
14 nobody understood how this bottom layer of 3104 was deposited on the
15 oxide layer 3102. So of course, that's all fallen apart, and even Intel
16 acknowledged it in the petition and has had to retreat from the fact that of
17 course we know how to do it, Lee tells you that it's deposited. So there's no
18 rationale to do this. And then we pointed out that why would anyone want
19 to do this? Because stacking results in a device that is less dense, it would
20 have higher cost, like this just doesn't make sense, Lee has come up with
21 this very, very unique design with the shared control gates to get a really
22 dense device.

23 And so suddenly on reply, and we didn't hear any discussion about
24 that today, but if you look at their reply brief, Intel is arguing that Lee now
25 discloses stacking. So they basically abandon the rationale that's in their
26 petition, and now they're like well, it's in Lee. But of course, Dr. Sechen

1 couldn't defend that at his deposition, so if you look at his testimony, at his
2 second deposition, which is Exhibit 2053, at pages 34 through 35, and this is
3 cited in our sur-reply, you know, he's starting to point to some other parts of
4 Lee, but those are on a totally different set of embodiments, it's all about
5 Figures 37 to 44, which are not cited in the petition or his expert declaration
6 at all, and he acknowledged that during his deposition.

7 So we've kind of gone full circle, like first we said that we would
8 need to go to Lee and Aspar to stack, and then suddenly well, but Lee
9 discloses stacking, like none of this motivation to depart from Lee and go
10 and look at Aspar or Kim is credible at all.

11 Now let's move on to Figure 25 of Lee. So let's go back and look at
12 the petition again, so you should be able to see now the petition at -- well,
13 once I get there. Let's go and look at petition at 52. So here we are, and this
14 is the Kim, the Lee/Kim ground, right? So Intel's kind of rationale here is
15 that you would wafer bond level 3104 to level 3102, and they propose other
16 figures in Lee, Figures 1A, 2, 7, or 25A to do that. Now if you notice,
17 they're not actually just proposing putting one memory cell, which is shown
18 in Lee's Figure 1A or B, and doing it, they have to do a layer, and indeed
19 they said that, right there. You're going to wafer bond level 3104 to layer
20 3102, they're doing a whole level. And if you look at their demonstrative,
21 which I'm highlighting here on the bottom of 52, you can see they put like
22 two of Lee's Figure 1's there, because there's going to be a whole bunch.
23 And the only place that that's actually disclosed, this combination, would be
24 in a structure like Figure 25, where you're fabricating like the level, you
25 know.

1 And so Intel is now trying to disavow Figure 25A, but that's their
2 combination here in the petition, and Figure 25 simply won't work. So let's
3 go back to Intel's slides.

4 JUDGE TORNQUIST: Counsel, as you're doing this -- this is Judge
5 Tornquist.

6 MS. ARMOND: Yes.

7 JUDGE TORNQUIST: Figure 1A has a single control gate on one
8 side of the pillar.

9 MS. ARMOND: Yeah.

10 JUDGE TORNQUIST: What's in figure 25 has four control gates on
11 each face, one on each face of the pillar.

12 MS. ARMOND: Mm-hmm.

13 JUDGE TORNQUIST: So there's something different, right?

14 MS. ARMOND: So again, Intel's doing this mix and match. I mean,
15 look, figure 25A has this shared control gate. Figures 1, 2, 7 are just trying
16 to show concepts of different kinds of memory cells, but the only level that
17 they're showing is one that has this really unique shared control gate
18 configuration in Lee.

19 JUDGE TORNQUIST: So if I remember quickly, I don't have it up.
20 That's 1C of Lee, right? Where there's a control gate on each face of the
21 pillar, and they're not relying on that.

22 MS. ARMOND: Say that again, in 1C.

23 JUDGE TORNQUIST: I believe it's 1C. I should pull it up.

24 MS. ARMOND: Yeah, that's what we're looking -- that's what we
25 were looking at right now together. This is ground 1C. This is Lee --

26 JUDGE TORNQUIST: No, I'm sorry, figure 1C.

1 MS. ARMOND: Oh, You're talking about Lee.

2 JUDGE TORNQUIST: I'm sorry.

3 MS. ARMOND: Okay --

4 JUDGE TORNQUIST: These are figure 1A, I understand that they've
5 put multiple on a substrate.

6 MS. ARMOND: Well, they're not relying on figure 1C, but here let's
7 look at this together.

8 JUDGE TORNQUIST: Well, I guess that's my point. 1C has four
9 control gates.

10 MS. ARMOND: So this is a top down version, right? So like figure 1
11 is just an illustration, so you can kind of get a sense of what's going on. But
12 what's really happening, figure 1C is like the top down version, and you can
13 do this like circular or you can do it square. So figure 1A and all of these are
14 designed to have multiple control gates, and that description on how to build
15 it is now in that figures 13-28, which, you know, figure 25A is an
16 intermediate point. So I don't --

17 JUDGE TORNQUIST: I'm not sure. So walk me through that. Go to
18 paragraph 125 of Lee that has three different types of memory devices,
19 figure 1A, 1B and 1C. I understand 1A to have a single control gate. I
20 understand 1B to be a circular one that surrounds it. And then 1C to be the
21 version that actually goes and has multiple -- so only 1C can store multiple
22 bits of data. Am I wrong on that?

23 MS. ARMOND: That's what it says. So, but again, their layer -- you
24 know, their theory is you would take a layer of these memory devices, right?
25 And you would put them on the substrate. So I agree with you, but that
26 doesn't like change what their combination is, which is you would take a

1 layer. And so, yes, there is three with figure, figure 1C that has four control
2 gates. But, you know, figure 1A has one, right?

3 So if you go back to their petition, you know, they're putting the
4 whole layer on, but the problem is that figure 25A, it's an intermediate point.
5 And I mean, there's a lot of problems with figure 25A. So let's look at their
6 slide together. I'm looking at Intel slide 40 and you should be able to see
7 that on the screen.

8 So this is an intermediate point. There is -- again, Lee teaches when
9 you make this structure, you're using the upper levels to complete the lower
10 level. So they're interleaved. So there's not really a clear partition point. So
11 the whole notion that you would kind of look at this and think I should stack
12 this doesn't hold water as our expert explained. But, you know, their expert
13 acknowledged that this is inoperable, like this whole combination falls apart.

14 Dr. Sechen at his most recent deposition acknowledged that there's no
15 top contact. So there is no current that's flowing through this top NPN stack.
16 So it's not actually even a memory cell, can't store or retrieve charge. So
17 they haven't even identified an operable combination within Lee. It's not
18 again in their petition.

19 JUDGE TORNQUIST: But again, you keep going to 25A and I
20 understand why.

21 MS. ARMOND: Yeah.

22 JUDGE TORNQUIST: But how do we know that if that stack that
23 they have, the 1A type memories cells would also have this type of stack
24 that's interleaved with shared control gates? Seems like it would not.

25 MS. ARMOND: Well, again we -- look, Intel today is saying, well,
26 you would just change 25A or you would just add it. Like, you know, we

1 have to stick with what their combination is in the petition, and their
2 combination is you would put a layer of these things on there, right? And
3 they don't actually explain how they would accomplish that. They're the one
4 that has the burden there.

5 It's not my job to disprove this one paragraph that I can't really
6 understand. Like, you know, they haven't shown how this is going to be
7 pulled off. And when we start looking at things, like none of it ever works.
8 So you know, that's an excellent question to ask them, and also where it is in
9 their petition.

10 Okay. So they're also trying to disavow that there is the relationship
11 between 25A and figures 1C. And if you actually look at their petition,
12 they're saying something a little bit different than they are today.

13 So if you look at page 38, which we can look at now that I guess I
14 have it up. You know, they said that figures 1, 2, 7 -- there we go. That
15 figures 25A and 2 and 7, they're all showing basically the same structure, the
16 same pillar memory. So, you know, again all these things interrelate, and
17 Intel cannot disavow figure 25 at this point.

18 All right. So while we're on this whole figure 25 thing, figure 25 is
19 also important for other grounds, which is grounds 1A, 1C, and 1E where
20 they're relying on this stack, this inoperable NPN stack, to satisfy the serial
21 requirement that you have two memory cells that are vertically oriented and
22 serially connected together.

23 Again, this has been discredited by both experts. And so now on
24 reply, and we heard a little bit about this today, Intel is saying that the
25 petition met its burden because 25A has these things like momentarily
26 connected. And as I just explained, of course not, it's inoperable. Their own

1 expert admits that they have not met their burden. And of course, because
2 it's on reply, you can disregard it because it's too late.

3 JUDGE TORNQUIST: So, counsel, this is Judge Tornquist. Let me
4 just ask. I asked Petitioner's counsel about this as well. Could this in 25A,
5 as it's currently structured there, store memory? Store a bit?

6 MS. ARMOND: No, the NPN, it's not connected. This is like an
7 intermediate stage that they've picked. So, and counsel for --

8 JUDGE TORNQUIST: So I guess the question is we require non-
9 volatile memory, right?

10 MS. ARMOND: What?

11 JUDGE TORNQUIST: The claims, claim 13 requires non-volatile
12 memory. In this state, is this a non-volatile memory cell?

13 MS. ARMOND: But again, we're talking about claims 16 to 17. You
14 need 2, right? And there's no top contact on there. There's no current for --
15 and again, the other thing that you need a serial connection, and remember,
16 there's no dispute, this is a NOR connection. It's parallel. So there's a lot of
17 reasons that this particular one does not work. And again --

18 JUDGE TORNQUIST: Okay. So let's step back there.

19 MS. ARMOND: Yes.

20 JUDGE TORNQUIST: Because my thinking was that this actually, if
21 it's not operable, it's not a non-volatile memory cell.

22 MS. ARMOND: Yeah, exactly.

23 JUDGE TORNQUIST: Okay. I almost got the feeling from what you
24 just said that you were disagreeing with that.

25 MS. ARMOND: No, no, I totally agree. No, this -- look, it's not
26 wired up. The structure is not there for it to be a memory cell. It's just an

1 NPN stack. Like, an NPN stack could be a lot of things, right? Like, I
2 completely agree with you. And Intel agreed, like, you know, this doesn't
3 work.

4 And again, here we're hearing again, well, we'll just keep going. We'll
5 add the top contact. Again, that's like not in the petition at all. And because
6 we're just making it up, it's one paragraph. So we're still hearing new
7 theories. It's too late. We have to stick with what they gave from the
8 petition, which is basically nothing.

9 Okay. If you have more questions about 25A and Lee, I'm happy to
10 answer them. Otherwise, let's keep going on motivation to combine. So
11 besides the motivation that was, we don't know how Lee makes its layers,
12 which has been discredited, the next thing that Intel said was, well, it's going
13 to improve testing and create less waste. And the Board ordered trial to look
14 at that. And as we heard today at the hearing, even Intel admits that none of
15 this holds any water.

16 So, first of all, as we know, Lee, Kim, and Aspar have nothing to do
17 with quality control. And there's no dispute that the fabs already test when
18 they make devices, right? They go through and they see which dies are
19 good, and they take probably almost all of them. If there's one or two bad
20 ones, they discard them. That's in Intel's own exhibits, Exhibit 1014 and
21 1016.

22 So in terms of testing, you know, Intel has the burden here to show
23 that there would be an improvement over Lee's technique. And there isn't.
24 They declined to provide the data that the Board asked for, which is an
25 interesting position when you bear the burden here. And, you know, the
26 problem with Aspar is Aspar's layers are unpatterned stacks.

1 So if you have a problem with the stack, you're discarding the whole
2 layer because it's not separated at all. And so, and this was a question that
3 Judge Roesel asked, and it's exactly. So you're not saving anything. If you
4 have a problem with the layer in Aspar, you're throwing the whole wafer
5 away. That is not creating less waste compared to a typical deposition
6 process where maybe you lose a die or two.

7 And then the solution I heard today was, well, you would just throw
8 the layer away. Okay. Again, that's not in the petition. Because, again the
9 petition is -- like these grounds are one paragraph. So they're always
10 whatever Intel wants them to be. And that, as we previously discussed, is
11 really problematic. Because, again, everything's a moving target. Because
12 they don't actually explain what the ground is.

13 So let's talk about Kim. So counsel acknowledged at the hearing that
14 Kim's a little different than Aspar, because in Kim, you're actually
15 fabricating devices before you bond them. But here's the problem. If you're
16 making those devices by, you know, deposition basically, the semiconductor
17 fabs already test. And so there's no testing advantage because those wafers,
18 regardless of what's happening with the bonding, they're already made and
19 they would already have been tested by the fab. They're like fully created
20 devices. So there's no quality control benefit at all. So that rationale, they
21 haven't met their burden.

22 And then let's talk about waste. Counsel acknowledged that in Kim,
23 you grind off the entire substrate after you transfer the layer. And that is
24 correct. So you're basically throwing an entire wafer away every time you
25 bond. So that's not saving anything. You're making more trash.

26 And Aspar has that 1100 degree anneal step, which we're going to be

1 talking about very shortly. And, you know, burning your wafers also doesn't
2 minimize waste. So there's really -- they presented no reason that one would
3 leave Lee and go and combine it with these stacking methods, which would
4 result in memory devices, which are less dense and higher cost, which is
5 exactly the opposite of Lee was trying to accomplish.

6 JUDGE TORNQUIST: So, counsel, this is Judge Tornquist. Let me
7 just step back on this quality control, because I think --

8 MS. ARMOND: Yeah.

9 JUDGE TORNQUIST: -- at least initially, that was one of the more
10 compelling things for me. So I want to make sure I understand it. If you --
11 their argument is that you could have a substrate with the devices formed in
12 it separate. You can test that, make sure it's working, then you can form
13 these memory cells separately and test those and only combine good ones.
14 How does the fact that things are tested in the fab take that benefit away?

15 MS. ARMOND: Sure, let me explain. And remember, again, we're
16 on grounds where they're not really explained. So this is all like hand
17 waving that's happening later. So but, you know, let's pretend that's in the
18 petition, even though it's not. But, so we have two different things
19 happening, right? So in Aspar, you're transferring unpatterned wafers.
20 There's actually no memory devices. So you're not testing devices, because
21 there's like nothing there yet. So that's one issue.

22 And then in Kim, like what is being bonded are actually completed
23 devices. So they've already been fabricated. So what is in Intel's exhibits,
24 Exhibit 1014 and 1016, which they're reproduced in our brief, or we can
25 look at them together. You know, the fabs, when they're depositing and
26 making a bunch of devices on a wafer, before they cut them up, they go

1 through and test each one. And if there's a problem, they put an ink dot, and
2 they discard it.

3 So they're already testing. Of course they're testing. They don't want
4 to put bad devices out. So that's your benchmark. Intel needs to show that
5 there would be a reason that stacking would somehow improve the process
6 that everyone is already doing, and they haven't done it. Like, again, there's
7 nothing to test in Aspar.

8 And in Kim, they acknowledge, like, what's being bonded are
9 completed devices. Those would already have gone through the standard
10 fab testing. So there's nothing there. And notice there's no statistics.
11 There's no prior art. There's nothing to show that this would be an
12 advantage.

13 JUDGE TORNQUIST: Okay. So this is Judge Tornquist again. Let
14 me just make sure I understand. Do you understand the combination to be
15 two entire wafers being bonded together? Or is it individual dies that have
16 been tested and working that are bonded together?

17 MS. ARMOND: So again, as we talked about at the beginning, I
18 don't really know what they're arguing. This has been a problem the whole
19 way. So what Intel previously said was that they were bonding entire layers,
20 right? And then today at the hearing, now they're acknowledging that Kim
21 talks about bonding individual devices.

22 So I'm just trying to keep up with like all of what's happening. But no
23 matter how much they're ducking and weaving here, they still haven't shown
24 any improvement. Like, because, again, this is all really complicated stuff,
25 and it's just not all hanging together. And, of course, look at the petition.
26 Not there.

1 Okay. So let's talk about annealing really, really, really briefly. And
2 let's look at Intel's slide 32. So this is a slide they showed earlier. And
3 they're claiming that Aspar doesn't include an 1100-degree annealing step.
4 Of course Aspar anneals at 1100 degrees C. You know, Aspar uses Smart-
5 Cut, it tells us. And this image on the right from Exhibit 1015, which is
6 Intel's own exhibit, the Wolf textbook, this is in Dr. Sechen's expert
7 declaration at paragraph 43 fully reproduced.

8 And when we showed him this at his deposition, he admitted that
9 Exhibit 1015 describes the same process as in Aspar. He's like, this is the
10 same process. So now on reply, we have Intel that is repudiating its own
11 exhibits that are cited in its own expert declaration and their own expert
12 testimony.

13 Like, first of all, that's improper that it exceeds the proper scope of
14 reply. But even if you want to entertain it, it just shows that all of this is not
15 credible. And the cite, if you want Dr. Sechen's testimony where he testified
16 that this figure from Wolf, which is at -- he said Wolf is entirely consistent,
17 if not outright the same as Aspar's. That is in his deposition, Exhibit 2039 at
18 118, line 10 to 119, line 2.

19 So the kind of red herring that Intel tries to throw in this is they're like,
20 look, you don't need to do high temperature with Smart-Cut because, look,
21 BeSang's inventor, Mr. Sang-Yun Lee, like he didn't do it. But the only
22 thing they're pointing to is the parent to the '702 Patent that's asserted here.

23 And that was one of the many things that Mr. Lee realized -- not Lee
24 because there's a lot of Lees in all these cases, but Mr. Sang-Yun Lee. Like,
25 he figured out how to do this at a low temperature, and his patent and the
26 '941 Patent talk about keeping the processing below 650. So again, they are

1 using hindsight. They don't have anything else that shows that you would do
2 this at low temperature. All they have is the patent itself and its parent
3 patent.

4 So let's actually talk about one more thing and relating to this
5 combination that they're proposing. And, again, this applies to both. So let's
6 look actually at now BeSang's slide -- you should be able to see BeSang's
7 slide 10. So this is the combination that is actually in Intel's petition. So if
8 you look over here on the left-hand side of BeSang's slide 10, this is Aspar.
9 Okay? And then this on the right is a reproduction of how Intel is proposing
10 combining these two references, Lee and Aspar, right?

11 So it's a little nonsensical, I have to say. So remember in Aspar, you
12 have a wafer A, and it has like an oxide layer, right? And then a very
13 important thing happens, which Judge Roesel like pointed out earlier.
14 There's this hydrogen implantation that happens under that oxide layer, and
15 that's going to allow the splitting later.

16 And so they're actually implanting, and there's going to be cuts, like
17 little bubbles in that blue substrate. And that's what's going to let you like
18 peel off the top layer later when you do the transfer. Okay? And that's
19 what's happening here, plainly taught in Aspar, and nobody's disputing that.

20 So Intel kind of does something bizarre, and so remember the oxide
21 layer is wafer A in Aspar, but when they do the combination, they actually
22 flip it. And so they say Lee's figure 35, which is the one with the, you know,
23 insulating layer and the substrate, they actually assign that to be wafer B,
24 which is -- yeah, okay. We won't go down that rabbit hole, but that's a
25 whole other thing.

26 So they actually switch it up and they say, okay, well, wafer A, which

1 is the NPN stack with a contact on top, from their, you know, imagining of
2 how this would work. So they're actually splitting this substrate, I guess,
3 somehow under the NPN stack, which I would really like to know how they
4 do it. Since there's metal here, like how they're going to be shooting
5 hydrogen in, but again, they don't explain that. But there's a lot of questions
6 about these grounds.

7 So here's the problem. When they flip it over, and there's --
8 remember, the substrate has that hydrogen implantation, there's like a little
9 cut in there, right? So to transfer the stack, there's going to be a cut, they flip
10 it over, and then they peel off the stack. But what you clearly see in Aspar is
11 after you've like flipped it over, like there's still a little bit of that substrate
12 there where you did the hydrogen implantation and got the crack. And so
13 there's still a little like silicon substrate, or whatever your substrate is, on
14 top.

15 But again here, like, you have a problem because you can't just have
16 silicon on top of your NPN stack. You have to get a top contact on it. And
17 they never address it. Like, you know, again, this is their combination, their
18 burden, and they never like show how one of skill would do that. And, you
19 know, and so now they're coming back and saying, oh, no, no, that little
20 thing that's left behind, that's the thin layer. No, it's not. No, it's not.

21 They're showing it here, the blue substrate corresponds, that's the little
22 bit that's left after that hydrogen implantation. Again, doesn't make any
23 sense. They haven't met their burden. It just isn't going to work.

24 And I mean, one problem with just this transfer of the NPN stack is,
25 you know, Aspar is like an academic paper. There's no memory devices.
26 They're taking Aspar way beyond its teachings. Like Aspar is like

1 transferring oxide layers and they're like trying to move over NPN stacks
2 and metal, like in one paragraph. Okay. So --

3 JUDGE TORNQUIST: Counsel, let's -- this is Judge Tornquist. Let's
4 look at this again because this is important, the point you've raised.

5 MS. ARMOND: Yes.

6 JUDGE TORNQUIST: So it looks like this is an SOI process where
7 that little blue strip is actually what you're after. That's the monocrystalline
8 silicon coming off of that wafer.

9 MS. ARMOND: You're transferring this oxide layer. That's what
10 you're trying to transfer, it's the gray.

11 JUDGE TORNQUIST: So that's an important question, and what is
12 that little blue piece? Is that not monocrystalline silicon?

13 MS. ARMOND: No, it's oxide. See it's --

14 JUDGE TORNQUIST: The oxide is the gray.

15 MS. ARMOND: A gray, yes.

16 JUDGE TORNQUIST: A little piece.

17 MS. ARMOND: To make a silicon on insulator, you want to transfer
18 the oxide layer, this insulating layer. That's what this is. So this is where it
19 makes no sense because you already have that here, and so what they're
20 saying is -- again, they're assigning this wafer A. They're like trying to say
21 the NPN stack in the middle contact is the oxide that you're transferring, like
22 it's backwards. It like makes no sense. But if you take them at your word,
23 which is what I'm doing because it's a petition, like they're leaving substrate
24 on top.

25 JUDGE TORNQUIST: Okay. Can you go to the other one where
26 you're showing us the anneal temperature of 1100?

1 MS. ARMOND: Or do you want to go to their slide where they say,
2 no, it's just a little thing, because it's not.

3 JUDGE TORNQUIST: No, I want to go to the slide you had about
4 the 1100 anneal, because that's the other reference. The Wolf reference I
5 think.

6 MS. ARMOND: Oh, yeah. The one in my slide or their slide?

7 JUDGE TORNQUIST: You had it in your slide. There.

8 MS. ARMOND: Okay, yeah.

9 JUDGE TORNQUIST: So you have the initial silicon layer A, you
10 make an oxide layer 2 around it, you implant down. And then the oxide
11 layer stays underneath and be with the little strip of so, silicon stays on top.
12 That's why I was thinking the blue layer actually is that monocrystalline
13 silicon.

14 MS. ARMOND: So, again, you know, if you look and this is the
15 same process as in Aspar, right? You have A, wafer A. It's just a wafer.
16 Who knows, right? Maybe it's not, maybe it's. But again, they haven't really
17 gone into that. So this is silicon. They oxidize the top layer and they're
18 trying to get this top layer off and onto the other wafer B, right? So they
19 implant, and then you're right.

20 So the oxide layer goes and then they have a little layer of
21 monocrystalline. But the problem is they're saying that wafer A is the stack
22 they're trying to transfer. And so when they put it down, it -- this oxide is
23 corresponding to that NPN stack with the contact on the bottom.

24 So they're leaving silicon on the top. And that's a problem because
25 they got to form that top contact, otherwise that NPN is not going to act as a
26 memory device, and they just totally ignore it. Like, you know, they're

1 relying on, and Aspar clearly shows it and they just like, you know, ignore a
2 problem. Because again, none of this makes any sense, and they're
3 simplifying and ignoring stuff they don't like because, again, it's not obvious
4 and nobody came up with this first. So --

5 JUDGE ROESEL: Counsel?

6 MS. ARMOND: Yes.

7 JUDGE ROESEL: Sorry, this is Judge Roesel. So this thin
8 monocrystalline layer is actually the objective of Aspar, is that right?

9 MS. ARMOND: No, the objective is to get the layer of oxide on,
10 silicon on insulator. Trying to get an insulated layer on wafer B from wafer
11 A.

12 JUDGE ROESEL: Yes, also the monocrystalline silicon, right? I
13 heard from Petitioner's counsel that it's advantageous to build devices in
14 monocrystalline silicon.

15 MS. ARMOND: Well, yeah, that relates to another argument which
16 we're going to get to. But again, look at their combination. Let's go back to
17 the slide. They're not doing that. What they're telling you to do is wafer A
18 is this, and so they're splitting -- they're trying to split this layer off the
19 substrate and then cut it off.

20 So what might work in Aspar doesn't work here, because they're
21 trying to transfer this and they can't just have that layer because it's going to
22 obstruct the top contact that has to happen up here. So, again, it might make
23 sense in Aspar, but it doesn't make sense the way they're applying it.

24 JUDGE ROESEL: Yes. But my point was, I mean, the title of Aspar
25 is Smart-Cut process for thin film transfer. So the whole objective of Aspar
26 is to transfer this thin film, which Petitioner doesn't seem to be doing in their

1 combination.

2 MS. ARMOND: Exactly. Exactly, you got it. Yeah, so again,
3 Aspar's trying to transfer a thin layer of oxide and then silicon on it where
4 you can build off of it, but that's not what they're using it for. They're trying
5 to use it to transfer these NPN stacks, and you can't have that
6 monocrystalline layer. Also, it makes no sense because there you have an
7 oxide on here to begin with, right? Wafer B does not need another layer of
8 oxide. They already have one.

9 But anyway, like we're taking them at their word, sort of, to the extent
10 we can understand it. So, yeah, they're not even using like Aspar. What it is
11 because again they already have that layer of oxide. So this is just all like
12 made up, and it does not hang together.

13 Okay. So let's move on to NAND to NOR, which impacts the Lee
14 and Kim or Aspar grounds. And this is where they're targeting claims 16 to
15 17, and they say, oh, we should just pull the memory cells out of Lee, the
16 NORs, and we'll just make them NAND. So, again, those are fundamentally
17 incompatible, going from -- it's an entirely new chip. Our expert explained,
18 you know, at length, how that's basically going to cause a cascading set of
19 changes.

20 And also doing it, they haven't shown that you're going to maintain
21 density, because again, Lee has this really specific combination with these
22 interleaved layers and the shared control gates, and they don't grapple with
23 the fact that like if you're just pulling a couple things out of Lee's stack,
24 you're actually potentially going to be decreasing things. So that is yet
25 another reason. And they don't have a good answer for that either.

26 So, let's see. Let me just make sure I've covered the Lee territory

1 before we move on to Johnson. Actually, there's one thing I wanted to say.
2 So, again, one thing I will point out, I'm going to again share my screen. So,
3 again, like I don't even know what any of this means. Like, Judge Roesel
4 earlier pointed out on -- I'm going the wrong way, sorry. Scroll along with
5 me.

6 Okay. It was the slide that Intel showed where they said, here's a
7 combination for Lee and Aspar, but they actually have the layers from Kim.
8 And they're saying, well, yeah, you can just apply it to Kim.

9 Again, we're just on this thing where everything is constantly in flux
10 and we don't actually know what the grounds are. And that included this
11 new theory that we heard about for the first time on reply, which is their
12 high temperature process optimization. And this is actually the subject of
13 our motion to exclude, and I'm going to pass the baton to Ms. Han shortly to
14 argue it. But just on the substantive level, this is a new motivation to
15 combine. It's not in the petition.

16 Again, counsel has asked for it and couldn't supply it because it's not
17 there. And there is an oblique kind of reference to an optimization process
18 in Dr. Sechen's original declaration. And Intel is right. We asked Dr.
19 Sechen at his first deposition, like, tell us more about that. And we had a
20 long line of questions. I encourage you to read it at pages -- Exhibit 2039.
21 That's his first deposition transcript at pages 90, 91 to 98.

22 And we went through that whole thing. And at the end, we said, hey,
23 what are you saying here? Does this apply to the thermal budget? And he's
24 like, no, no, this is just about combining two different materials.

25 So, Dr. Sechen told us at his first deposition that his opinion was not
26 about optimizing to deal with thermal budget. And now they're -- and we of

1 course relied on that. And now, of course in reply, they're like, yeah. Like,
2 coming up with a new opinion that's exactly that.

3 So, of course, it's not in his original declaration. It's definitely not in
4 the petition. And he disavowed it at his deposition. And so, obviously, it's a
5 new opinion. It's improper reply. It should have been in the petition if they
6 wanted to raise it. But if you actually look at the deposition testimony, this
7 is exactly the opposite of what they're saying now. And unless -- hold on a
8 second. Unless you have more.

9 JUDGE ROESEL: This is Judge Roesel. So the slide that I asked
10 Petitioner's counsel about was slide 28.

11 MS. ARMOND: Okay. I was off by -- let's see. Yes, exactly. So,
12 yes. So thank you for that. Like, again, everything's a mix and match here
13 because we just don't know what the grounds are. So thank you for that. So
14 that's kind of what I have to say about Lee for now. I can briefly move on to
15 Johnson, unless you have more questions about Lee.

16 Okay. So let's talk about Johnson. I'm going to stop sharing for the
17 moment. Okay. So the Johnson grounds, yeah. I mean, counsel said they're
18 no different than the Lee grounds. I would agree with that. They also do not
19 meet their burden. And there's nothing different about why you would go to
20 stacking.

21 And Johnson has very similar disclosures about how, again, he has
22 this interconnected, dense memory cell structure that are these, you know,
23 pillars with a steering element in them. And he's using the upper layers to
24 do the bottom layers. And so, again, he's relying on a very specific
25 manufacturing technique that's based on deposition.

26 So in order to try to meet the limitations of claim 13, because claim 13

1 is the only claim challenged in the Johnson ground, they're relying on
2 Johnson's steering element in the pillar. And so I am going to share my
3 screen again. So let's look together at Johnson's figure 8B, right? So, you
4 know, this is kind of like in the array. So you have a steering element and
5 then your charge element, which is like a fuse. And that's what's in the
6 pillars that we were looking at earlier.

7 So the purpose of the steering element is to make sure that the current
8 only goes in one direction and not the other. And it's a two terminal device.
9 So the only thing that Intel relies on to try to satisfy the transistor limitation
10 of the claim is a stray reference to a JFET and a MOSFET in column 7 of
11 Johnson, which -- hold on a second. Okay. Which is right here, and it's so
12 small that no one can read it.

13 Okay. So they're talking about what the steering element can be,
14 which of course it has to pass the current in one direction and not the other.
15 And so we're not talking about the function of this, we're just talking about
16 the circuitry here. This is a two terminal device. They're not saying just use
17 a transistor.

18 They're explaining exactly how this JFET and MOSFET are
19 connected. They say it's the JFET, the junction field effect transistor with a
20 gate connected to source or drain. Okay. Oh, shoot, what did I just do? All
21 right. Okay, hold on.

22 So they say the gate is connected to source or drain, right? So they
23 tell you exactly how it's wired up. It's a two terminal device. And it's
24 basically a jerry-rigged diode, and everybody agrees that that's the way that
25 this JFET is being used, or you have a MOSFET and you either leave the
26 gate floating or it's also connected to source or the drain, right? I mean,

1 that's it.

2 And so we all know and basic like electronics. You know, you have a
3 diode that's a two terminal device and that passes current more readily in one
4 direction than the other, and that is exactly what Johnson is teaching.

5 Johnson was aware of transistors and three terminal transistor designs
6 and he said don't do that because there's these extra masking steps, it makes
7 for larger memory cells, more complicated manufacturing. And so he was
8 teaching away from doing that. You know, he didn't want to do that. He
9 wanted this denser two terminal thing, and he had a good reason for doing it.

10 So, but again we know from electronics 101, like a transistor operates
11 differently. It's a switch. So, and we just know that, and one of skill in the
12 art knows it. And you don't have to take my word for it. I have my IEEE
13 dictionary from my college years here. And the definition of a transistor is
14 an active semiconductor device with three or more terminals. It is an analog
15 device.

16 I mean, none of this stuff is really disputed. Like, it's not a transistor,
17 and Intel is treating this like a word search and looking for words. But if
18 you look at actually what Johnson teaches and how it's hooked up, it's not a
19 transistor. It's a diode. So structurally, it's the transistor because that's the
20 way it's wired.

21 So now I just heard a new argument that I've never heard before,
22 which is certainly not in the petition about, oh, well, you know, you could
23 use photo masking. Johnson knew about photo masking. But again, you
24 know, Johnson's trying to like optimize the manufacturing and cram a whole
25 bunch of memory cells. And Johnson was not -- again, Johnson was aware
26 of all this. He was not teaching a three terminal device.

1 And then if you start departing from Johnson and then stacking things,
2 that's not helping you with density, it's not helping with cost. It's going
3 against everything that Johnson taught against or warned against and why he
4 selected this diode design. So, unless you have more questions, I'm going to
5 turn it over to our favorite LEAP, Amy Han.

6 MS. HAN: Thank you, Ms. Armond. Good afternoon, Your Honors.
7 Yue Amy Han for Patent Owner BeSang, and I will start by addressing Ms.
8 Kaiser's argument about paragraph 213 of Dr. Sechen's declaration.

9 So Ms. Kaiser asserts that this paragraph was cited to in the petition,
10 and it supports their argument that their high temperature process
11 optimization theory was not new and was in fact brought in the petition.

12 And as my co-counsel Ms. Armond brought up, this was actually not
13 true. So in Dr. Sechen's deposition testimony, and I will share my screen to
14 show that. So can everyone see this? This should be Exhibit 2039 at pages
15 98-99, which I would like to point out that Dr. Kaiser has actually
16 conveniently failed to cite because she was citing to 2039 at pages 91-98,
17 and the relevant portions of his deposition testimony are on 98 and 99.

18 Here he was directly asked about paragraph 213, and he was asked if
19 this was relating to the high temperature process optimization theory that
20 they had just brought up on reply, and he expressly disclaims this. In fact he
21 testifies, no, this is talking about two different types of semiconductor
22 materials being used for the substrate versus the upper layers, which are
23 memory cells for the devices.

24 So, again, according to Dr. Sechen's own testimony, he did not discuss
25 high temperature processing in his declaration nor did he discuss it in his
26 deposition testimony. And I will stop sharing. And so, you know, the Board

1 should really exclude Exhibits 1041, 1043-1045, 1048-1050, and the
2 portions of Dr. Sechen's reply declaration that rely on these exhibits, because
3 they were new evidence that were not brought up in the petition.

4 And it's very telling that Petitioner has decided to bring these new
5 exhibits in its reply brief, instead of relying on the petition and the petition's
6 existing exhibits to support this high temperature processing theory that
7 they're now bringing. Because they couldn't point to anything in the petition
8 that actually supports this theory, so they felt the need to bring in these new
9 exhibits.

10 So, Patent Owner is now moving to exclude these exhibits from the
11 record. And if Your Honors don't have any additional questions, I will
12 reserve my time.

13 JUDGE TORNQUIST: Thank you. This is Judge Tornquist. Under
14 our consolidated practice guide, it says motions to exclude shouldn't be used
15 to exclude evidence that you believe exceeds the scope of a proper reply.

16 MS. HAN: Mm-hmm.

17 JUDGE TORNQUIST: So I know you cite some cases, , but what
18 you're really asking us to do is just not consider it, right? Do you really
19 want us to exclude it?

20 MS. HAN: Well, I think this could go a few different ways. So, first
21 off, the Board's cases clearly show that a motion to exclude is a proper
22 avenue in this situation, and the Board can decide to exclude improper reply
23 evidence. But on the off chance that the Board decides that this isn't proper,
24 the Board's cases, prior cases, have also mentioned that the Board can
25 choose to construe this motion to exclude also as a motion to strike and
26 strike these exhibits instead.

1 But regardless of which way the Board chooses, it always has the
2 authority to refuse to consider this improper reply evidence. So if it chooses
3 not to exclude or not to strike, it should not consider this improper evidence
4 regardless.

5 JUDGE TORNQUIST: Okay.

6 MS. HAN: Thank you, Your Honors.

7 MS. KAISER: I'm just checking to make sure that Patent Owner is
8 done before I dive back in.

9 MS. HAN: Yeah.

10 MS. KAISER: I wasn't sure if Ms. Armond had more to say.

11 MS. ARMOND: No, Amy did a great job.

12 MS. KAISER: Awesome. I have to say it is a very -- it makes my
13 heart happy to see two LEAP Practitioners in an argument. So I'll just say
14 that -- put my former judge hat on and say that before I dive back in. So, if
15 we could bring up slide 77. There we go. There's always a little technical
16 issues in these things. So thanks for bearing with us while we got our slides
17 back up. But these are excerpts from Dr. Sechen's original deposition.

18 So again, this is based on just the petition and his original declaration.
19 And this is his testimony. And both Ms. Armond and Ms. Han suggested
20 that Dr. Sechen hadn't testified about heat as part of process optimization.
21 And you can see here that that's just not correct. He was asked about
22 subsequent processing steps perturbing earlier layers when doing monolithic
23 processing. And he talked about how heat could possibly cause metal to
24 deform, creating opens and shorts.

25 He also talked, you can see on the left hand side, about how later
26 processing steps can cause perturbations of previous processing steps. And

1 so process optimization generally, and as to do with heat, was discussed in
2 his deposition, his original deposition. And the reply evidence and his reply
3 declaration both expanded on what he was specifically asked about by
4 BeSang's counsel at his original deposition.

5 I briefly want to go to Johnson just very quickly. And Judge Roesel,
6 you had asked earlier was there any particular benefit in the combinations of
7 Johnson versus Lee for the combinations with Kim or Aspar? I think
8 generally as the record developed during trial, and again, when we filed the
9 petition, we didn't know what arguments BeSang would raise.

10 But I think Lee itself, by suggesting bonding and discussing bonding
11 is, you know, if you have to pick one or the other, that's the one that has a
12 more disclosure to support the motivation to combine.

13 If we can pull up, it's Petitioner's slide that has -- I'm sorry, Patent
14 Owner's slide that has Aspar and has the annotated figure. So, Judge Roesel,
15 in your questions to Ms. Armond, you mentioned that you didn't believe that
16 Intel's combination was transferring the blue. And actually this is the
17 Johnson combination. If you could go to their slide that has the Lee-Aspar
18 combination. Yes, this one.

19 And I just want to be clear that the blue layer is what's being
20 transferred in that combination. And so the blue layer is the thin layer of
21 monocrystalline silicon and rather than, you know, instead of being just an
22 unprocessed layer of monocrystalline silicon, it's a doped layer of
23 monocrystalline silicon.

24 Aspar's all about transferring monocrystalline silicon layers, and that's
25 what we're doing here. I also just want to clarify and point out, if you go to,
26 I believe it's our slide 90. This is a figure again from the parent '941 Patent,

1 where it is --

2 JUDGE ROESEL: Petitioner, could I ask you to please go back to the
3 previous slide from BeSang?

4 MS. KAISER: Yes, Your Honor. Here we go. Yes.

5 JUDGE ROESEL: I believe I heard Patent Owner's counsel talk
6 about the hydrogen implantation through the metal layer. And the -- can you
7 respond to that argument from Patent Owner please?

8 MS. KAISER: Yes, Your Honor. So the -- so you wouldn't have to
9 do hydrogen implantation necessarily through the metal layer. Because the -
10 - and this isn't an issue, by the way, that's raised in any of BeSang's papers.
11 So they never before talked about implantation at all in their papers. They
12 talked about the oxide layer for Aspar in their papers.

13 But, and so we haven't, you know, specifically addressed in the
14 petition this issue, yeah. But we have addressed is where the detached layer
15 is, which is illustrated in this annotated figure. You wouldn't have to do that
16 -- as I understand it, you wouldn't have to do that through the metal layer
17 because you would do your doping to get the stack and then you would put
18 the metal layer on top. So it wouldn't be as if you're implanting through the
19 metal layer, you would be implanting through the silicon.

20 And I was going to expound on that a little bit, because that's actually
21 shown in the '941 Patent, which is the parent. If we go back, I believe it's
22 our slide 90. This is a similar structure to what we've proposed in the
23 combination, again which doesn't require a high temperature anneal because
24 the inventor himself didn't talk about a high temperature anneal.

25 But this shows the detached layer, 191 just below the NPN stack so
26 that when you do the detach, what you have is the bonding layers, including

1 a metal layer as well, you know, and your monocrystalline silicon stack.

2 JUDGE TORNQUIST: This is Judge Tornquist. Just so I understand,
3 where did the oxide go in this?

4 MS. KAISER: The oxide isn't in our combination. I agree with Ms.
5 Armond about that. If you go back to that same slide again. Because what
6 we don't -- in our combination, you don't need the oxide because the oxide is
7 already on wafer B. So what you're trying to transfer -- if you read the text
8 of Aspar, what it's talking about being important for the transfer is the thin
9 layer of monocrystalline silicon. And so that's what's being transferred in
10 our combination. Not the oxide.

11 JUDGE TORNQUIST: Okay.

12 MS. KAISER: But you still do end up with a silicon on oxide
13 structure because you have the monocrystalline silicon over the oxide layer.
14 It's just that you transfer it. It's already on one wafer instead of the other.

15 I want to get to the notion of that, our petition, you can't understand it.
16 And I think Ms. Armond talked about that, you can't understand that the
17 layers that are being transferred include more than one memory cell unless
18 you go to figure 25A.

19 And the only way you can understand the petition that way is if you
20 do what, it seems like Ms. Armond did, which is ignore the first, 54 pages of
21 the petition. And if you look, for example, at petition page 27. The petition
22 is very clear, and this is in ground 1A, which explains how Lee teaches all
23 the limitations of claims 13, 14 and 15. And other than we have an
24 alternative for explaining the modification for stackable add on layer.

25 And on page 27, the petition explains how you would take the
26 memory structure in any one of figures 1A, 1B, 2, 7, or 25A. So any one of

1 them, they're all as alternatives. And use multiple cells in each level of
2 figure 35. And it explains the motivation why you would combine that with
3 figure 35. And BeSang never disputed that in any of their papers. And
4 that's supported by Dr. Sechen's testimony as well as the disclosure of Lee.

5 So the fact that this ground is under the parent construction of BeSang
6 from litigation doesn't detract from what we said in the petition. And then
7 when we went and proposed the alternative for Lee in combination with
8 either Aspar or Kim. Then we explained as I showed in my opening
9 presentation, why you would use a different fabrication process to bond that
10 first level of the 3104 with the -- to the insulating layer.

11 So it's essentially ground 1A has your Lee structure, and then grounds
12 D and E -- I'm sorry, grounds C and E explain the fabrication modification.
13 And same thing for the grounds that include Endoh. We explained the
14 structural pieces in the Lee plus Endoh ground. So we explained how and
15 why you would use Endoh's structure, for example, in the level of figure 35
16 in Lee.

17 And then the same rationale for why you would fabricate that first
18 level using either Kim or Aspar applies because it's the same sort of idea,
19 and I know Ms. Armond gave me a hard time about using the word concept.
20 But the structure is the same and just the fabrication method is different.
21 And all of those motivations apply to Lee plus Endoh in the same way they
22 applied to Lee alone.

23 So the building blocks are all there. But you -- I agree with Ms.
24 Armond. You can't just read -- You can't read one page and throw the rest
25 of the petition away. You have to read the whole petition.

26 JUDGE ROESEL: So just to be clear, this is Judge Roesel. I mean,

1 Petitioner's proposed modification of Lee is only affecting how you attach
2 the first layer of memory cells to the oxide layer. And all the subsequent
3 layers, if you're going to build a structure like figure 35, all the subsequent
4 layers of memory cells would be made by sequential deposition?

5 MS. KAISER: They could be made by sequential deposition. They
6 could also be made by bonding. It would depend on, you know, the person
7 of ordinary skill in the art and what they wanted to do.

8 On the single crystalline silicon point, I mentioned that Aspar
9 discloses single crystalline silicon as being what's transferred. And Dr.
10 Sechen explained why a person of ordinary skill in the art would understand
11 that as a benefit. Lee itself expressly discloses using recrystallized silicon.
12 And Dr. Sechen said that using monocrystalline silicon would have known
13 benefits over recrystallized or polycrystalline silicon. And that's in his reply
14 declaration at paragraph 24.

15 Judge Tornquist, you said in your questioning that you thought that if
16 something wasn't operable, it's not a memory cell. But if you had a claim
17 that only disclosed memory cell, and someone had the structure of a memory
18 cell, even if it wasn't part of a total functional embodiment, if the claims
19 didn't require a total functional embodiment, the memory cell wouldn't cease
20 to be a memory cell before it was connected in a commercial embodiment.

21 Ms. Armond talked about data from --

22 JUDGE TORNQUIST: Just a follow up on that. Is it non-volatile
23 though? It's not just a memory, it's non-volatile.

24 MS. KAISER: That's true. There's no dispute that the structure that is
25 in figure 25A is non-volatile though. And that would be true, whether it was
26 connected up as NOR or NAND.

1 JUDGE TORNQUIST: Okay. Even without the other input line on
2 the top, conductor on the top?

3 MS. KAISER: There's no dispute that ultimately when you wanted to
4 use the memory in figure 25A, you would connect it in some way. The
5 question is whether you would connect it as NOR or NAND. And my point
6 is, regardless of how you connected it as NOR or NAND, it doesn't -- it's
7 non-volatile either way.

8 JUDGE TORNQUIST: Okay.

9 MS. KAISER: Ms. Armond mentioned that we didn't provide specific
10 additional data during trial. But data isn't required for motivation to
11 combine. And we provided lots of objective evidence to support Dr.
12 Sechen's opinions about process optimization, about yield, about quality
13 control. And we don't just throw all of that data out, or all of that objective
14 evidence out because we didn't provide quantitative data.

15 Ms. Armond also mentioned about fabs already testing. And that's
16 true, but fabs don't wait until you get to the very end to test things. And, you
17 know, fabs are testing as you go in different steps because you want to make
18 different decisions throughout the process. And that's what our combination
19 looks at.

20 Ms. Armond talked about Smart-Cut, again, and the 1100 degrees C.
21 And if -- so first of all, Dr. Sechen never said that Aspar's process is the
22 same process as Wolf. He said generally it's the same process. And then
23 when he was asked about the 1100 degrees C, he said that's one article's
24 opinion.

25 If you think about this sort of idea of fabrication, persons of ordinary
26 skill in the art are not automatons. They're not sort of saying, okay, we have

1 this generalized process. And for all materials, for all things, we have to use
2 this one temperature step, particularly when Aspar is saying it's suitable for
3 many different materials.

4 In my mind, it's like sort of saying -- I don't know why this analogy
5 keeps coming into my mind. But one time I was at Thanksgiving and I had a
6 sweet potato casserole with marshmallows on top. And I decided the best
7 way to brown the marshmallows would be to put it under the broiler on high.
8 And it set the whole thing on fire.

9 And so, Ms. Armond's argument here is essentially saying people of
10 skill in the art would just keep doing this, even though they knew it would
11 set the whole thing on fire. And the reality here is that that's not how
12 persons of ordinary skill in the art think. Aspar doesn't explicitly disclose an
13 1100 degrees C anneal step. No one ever admitted that it had to have that.
14 The '702 inventor also didn't talk about a 1100 degree anneal step.

15 So it's simply just not part of Aspar, not required, not part of Intel's
16 combination. And I think unless the Board has further questions, I concede
17 the rest of my time.

18 JUDGE TORNQUIST: Okay. I see no further questions. Thank you
19 very much. Patent Owner?

20 MS. ARMOND: Thank you, Your Honor. I'll try to make this really
21 quick. Okay. So, Intel talked about process optimization over and over
22 again. Remember, that's a new argument that came in on reply. And shows
23 you that they need this to show motivation to combine. It's not in the
24 petition. They've identified nowhere in the petition where it is.

25 And, you'll notice that counsel showed you on Intel slide 77, a couple
26 of questions that we asked their expert, Dr. Sechen, about his opinion, his

1 really vague opinion, where he's obliquely referencing the optimization.
2 And he did mention those temperature things. And so that's why we went
3 there at that part that Ms. Han showed you and said, hey, are you talking
4 about the thermal budget here? And he's like, no, I'm just talking about
5 combining materials. He repudiated their new theory on reply.

6 And again, you can't put in your prima facie case on reply. We don't
7 get a chance to respond to it with our own expert testimony. All of that
8 should be stricken.

9 Counsel brought up how, in their opinion, Lee teaches bonding, and
10 that further supports their motivation to combine. Because again, that's not
11 in the petition. And even if you consider it, and of course, we discussed
12 earlier how Dr. Sechen agrees that he didn't talk about in his declaration and
13 all of his new opinions on reply about how Lee suddenly now talks about
14 bonding, are about figures 37 to 44 of Lee, which they never rely on in the
15 petition. Because again, this is a new theory. They can't rely on this to meet
16 their prima facie case to show motivation to combine.

17 Okay. And then, we spent some time trying to look at the
18 combination of Lee and Aspar, and how this all works with taking off layers.
19 And I am still not sure now what the new combination is, because it sounds
20 like there was a new one. They acknowledge they don't need the oxide, but
21 again, the main point here is where is any of this in their petition?

22 Their own expert confirmed there's a thin layer of silicon on top of
23 that stack that they're proposing transferring. And of course, that would
24 obstruct the top contact as in their way that they have decided to do Aspar.
25 Again, like, I don't have a proposal here. I'm just trying to respond to what's
26 in the petition.

1 And, you know, they're using Aspar in a very weird way. And it just
2 doesn't make sense. There's that top layer, and we cited where Dr. Sechen
3 gave that up in our Patent Owner response at page 51. His testimony is, Dr.
4 Sechen's is at Exhibit 2039 at page 68, 19 to 73, 21. And again, we
5 discussed that.

6 Again, how after you implant, you're going to pull off and transfer the
7 layer and you're going to have that thin layer of silicon. And the way that
8 they're doing Aspar, which again, doesn't make any sense to me, it doesn't
9 work because it's going to obstruct the top contact that they need in their
10 combination.

11 Okay. And then they said about the testing point, which again, they
12 haven't met their burden to show any testing benefit, that fabs test as they go.
13 Okay, great. Show why building these devices using stacking as opposed to
14 deposition like Lee did would improve what is already happening in any
15 way. And they haven't done it. They've provided nothing, no data and no
16 articles, nothing. So that does not meet their burden.

17 Okay. So one last point -- well, actually two last points. So they're
18 continuing to dispute their own expert testimony and evidence that plainly
19 shows that Smart-Cut, which is what Aspar uses, has that annealing step at
20 1100 after you bond it. I mean, that's what helps bonding in that transfer of
21 the oxide layer. There is nothing in this record that says that Aspar does not
22 anneal at 1100 degrees C. Their expert says it, their own exhibits say it.

23 And the only thing they point to say, well, maybe you don't need to do
24 it is Dr. Sang-Yun Lee's own patents. They cannot use our invention as the
25 roadmap to get there. Like, again, they don't have anything else. So of
26 course, Aspar anneals at 1100 degrees.

1 And then finally, let's end where we started. I heard lots of talk about
2 where you should go search in the rest of the petition to try to find a
3 supported ground for the grounds we talked about at the beginning, Lee and
4 Aspar, Lee and Kim, grounds 1D, 1E, 1F. And they still haven't shown
5 where they met their burden in the petition. They have no answer.

6 And the only answer that I heard today was, well, just go troll back
7 somewhere through my petition and maybe you can piece this sentence here
8 and that sentence there and we can come up with something. That doesn't
9 meet their burden under the statute, the rules, SAS, which says the petitioner
10 needs to do it. They have not given us anything to work with here to make a
11 supportive finding of unpatentability.

12 And with that, I respectfully ask the Board to confirm the patent
13 claims over every ground in this mess of a petition. Thank you.

14 JUDGE TORNQUIST: Okay. Thank you very much. Excellent
15 argument today. And thank you very much to the LEAP Practitioners. You
16 both did an excellent job. I'm glad you were able to participate today. With
17 that, this hearing is adjourned.

18 (Whereupon, the above-entitled matter went off the record at 3:48
19 p.m.)

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