UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner,

v.

BESANG INC.,

Patent Owner.

IPR2023-00991

Patent No. 7,378,702

PETITIONER'S NOTICE OF APPEAL

Notice is hereby given that Petitioner Intel Corporation ("Intel") appeals to the United States Court of Appeals for the Federal Circuit under 37 C.F.R. § 90.2(a) and 35 U.S.C. §§ 141-142. Intel appeals from the Final Written Decision of the Patent Trial and Appeal Board issued on December 11, 2024, and the [Corrected] Final Written Decision issued on December 26, 2024 (Paper Nos. 39 and 40), and from all underlying orders, decisions, rulings, and opinions.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Intel states that the issues on appeal include, but are not limited to, the Board's determination that claims 1 and 13-17 of U.S. Patent No. 7,378,702 have not been shown to be unpatentable, including all subsidiary findings of fact and conclusions of law with respect to that determination (including, but not limited to, the Board's failure to address or misapprehension of several of Intel's arguments, the Board's failure to address or misapprehension of undisputed facts relating to the motivation to combine the asserted references, and the Board's substitution of its own rationale for the Patent Owner's without adequate notice to Intel).

Intel is filing one copy of this Notice of Appeal by electronic mail with the Director of the United States Patent and Trademark Office, and a copy of this Notice of Appeal is being filed electronically with the Board. In addition, a copy of this Notice of Appeal is being electronically filed with the United States Court of Appeals for the Federal Circuit, along with the required docketing fee.

Dated: January 17, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PETITIONER'S NOTICE OF APPEAL was electronically filed with the Board via P-TACTS and copies were caused to be served upon the Director of the United States Patent and Trademark Office (via electronic mail), the Court of Appeals for the Federal Circuit (via CM/ECF), and counsel of record (via electronic mail) in this matter on January 17, 2025 as follows:

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Paper 39
Date: December 11, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION
Petitioner,

v.

BESANG INC.,
Patent Owner.

IPR2023-00991
Patent 7,378,702 B2

Before JON B. TORNQUIST, KIMBERLY McGRAW, and ELIZABETH M. ROESEL, *Administrative Patent Judges.*

TORNQUIST, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Denying-in-Part and Dismissing-in-Part
Patent Owner's Motion to Exclude
37 C.F.R. § 42.71

I. INTRODUCTION

Intel Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1 and 13–17 of U.S. Patent No. 7,378,702 B2 (Ex. 1001, "the '702 patent"). BeSang Inc. ("Patent Owner") filed a Preliminary Response to the Petition. Paper 6. We instituted review with respect to all grounds and claims set forth in the Petition. Paper 12 ("Institution Decision" or "Inst. Dec."). After institution, Patent Owner filed a Response (Paper 17, "PO Resp."), to which Petitioner filed a Reply (Paper 21, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 25, "Sur-reply").

Petitioner relies, *inter alia*, upon two declarations from Dr. Carl Sechen (Ex. 1003 (original declaration); Ex. 1037 (reply declaration)), and Patent Owner relies upon a declaration from Dr. Steven A. Przybylski (Ex. 2029).

Patent Owner filed a motion to exclude evidence (Paper 29, "Mot.") to which Petitioner filed an opposition (Paper 30, "Opp.").

An oral hearing was held on September 18, 2024, and a transcript of the hearing is included in the record (Paper 38, "Tr.").

For the reasons that follow, we conclude that Petitioner has not demonstrated that claims 1 and 13–17 of the '702 are unpatentable. We also dismiss-in-part and deny-in-part Patent Owner's Motion to Exclude.

II. BACKGROUND

A. Related Matters

The parties identify the following district court proceedings as related matters: *BeSang Inc. v. Micron Tech., Inc.*, No. 2:23-cv-00028 (E.D. Tex.)

and *BeSang Inc. v. Intel Corp.*, No. 3:23-cv-00113 (D. Or.). Pet. 94; Paper 4, 1. The parties also note that the '702 patent was challenged in IPR2023-00900. Pet. 93; Paper 4, 1.

B. Real Parties in Interest

Petitioner and Patent Owner identify themselves as the real parties in interest. Pet. 93; Paper 4, 1.

C. The '702 patent

The '702 patent is titled "Vertical Memory Device Structures" and issued May 27, 2008, from an application filed September 3, 2004, which is a continuation-in-part of an application filed June 21, 2004. Ex. 1001, codes (22), (45), (54), (63).

The '702 patent explains that "integrated circuits contain transistors that are primarily implemented on a single major surface of a substrate, such as a semiconductor wafer." Ex. 1001, 1:27–30. "These laterally oriented devices," however, "consume significant amounts of chip area." *Id.* at 1:30–31. The '702 patent explains that one method of reducing the lateral area consumed by the transistors was to reduce the lateral dimensions of the transistors and interconnects, but the equipment and technology needed to support the manufacture of such chips "becomes increasingly expensive with each new generation of smaller devices." *Id.* at 1:31–39. To address this problem, the '702 patent discloses the use of "a plurality of vertically oriented semiconductor memory devices, or cells," that "may be added to a separately fabricated substrate that includes electrical devices and/or interconnect lines." *Id.* at 1:40–50; *see id.* at code (57) ("Vertically oriented

semiconductor memory cells are added to a separately fabricated substrate that includes electrical devices and/or interconnect.”).

Figure 1 of the ’702 patent is reproduced below:

Fig. 1

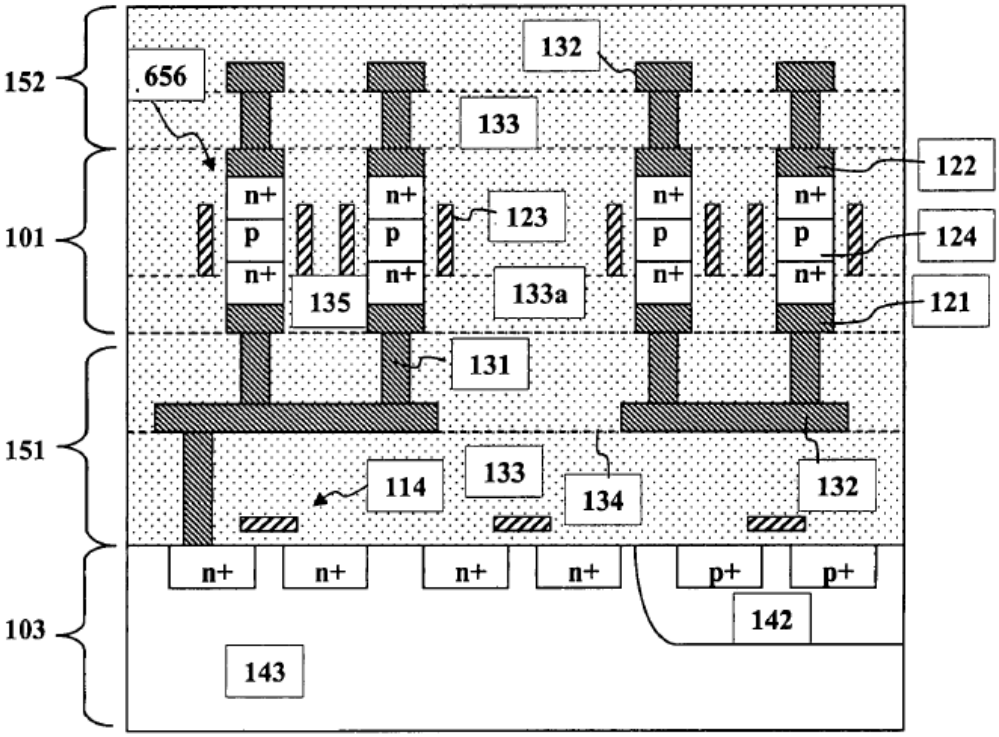


Figure 1 is a cross-sectional view of an embodiment that includes “a base semiconductor substrate and add-on vertical memory devices.” Ex. 1001, 2:13–15. As shown in Figure 1, vertical memory devices 656 are separated by isolation 135 and have floating structures in filled dielectric materials 133*a*. *Id.* at 5:18–21. These vertical memory devices are referred to in the ’702 patent as floating devices (FLD). *Id.* at 5:21–22. “Inter-layer dielectric (ILD) layers 133 are disposed above and below FLD layer 101.” *Id.* at

5:29–32. Interconnect lines 132 and vias 131 connect FLDs directly or indirectly within an FLD layer, or to another FLD layer, or to a base substrate. *Id.* at 5:32–36.

In the embodiment shown in Figure 1, base substrate 103 is bonded to lower dielectric layer 151. Ex. 1001, 5:37–38. Dashed line 134 denotes a border, or interface, between two ILD layers. *Id.* at 5:43–44. First ILD layer 151 has interconnections and vias, and base substrate 103 shares these interconnections and vias with first FLD layer 101. *Id.* at 5:44–47. The bottom of the FLD layer is connected to metal layer 121, which is also directly connected to vias 131 in ILD layer 151, thereby forming a preformed electrode and contact. *Id.* at 6:35–38. The top of the FLD layer may be connected to metal layer 122, which is also directly connected to vias 131 in ILD layer 152. *Id.* at 6:38–40. The ’702 patent notes that multiple FLD layers can be stacked, thereby increasing the effective device density. *Id.* at 6:41–42; *see also id* at 5:38–41, 5:47–50 (disclosing a “second FLD layer” not shown in Figure 1).

According to the ’702 patent, “[t]he plurality of vertically oriented semiconductor memory cells can be added to the separately fabricated substrate as a thin layer including several doped semiconductor regions which, subsequent to attachment, are etched to produce individual doped stack structures.” Ex. 1001, code (57), 1:57–62. “Alternatively, the plurality of vertically oriented semiconductor memory cells may be completely fabricated prior to attachment” to the separately fabricated substrate. *Id.* at code (57), 1:67–2:3.

The ’702 patent explains that the “FLDs may, but are not required to, have a pillar structure.” Ex. 1001, 6:43. The FLD of the ’702 patent also

"has a gate dielectric layer which may be implemented with process operations at temperatures below 650° C." *Id.* at 7:15–17, 7:20–22 ("Any suitable dielectric material could be used except films requiring processing at temperatures more than 650° C.").

D. Illustrative Claim

Petitioner challenges claims 1 and 13–17 of the '702 patent. Pet. 1. Claim 13, reproduced below, is illustrative of the challenged claims:

> 13. A semiconductor memory structure, comprising:
>
> [a] a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
>
> [b] a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
>
> [c] the stackable add-on layer being bonded to the dielectric layer; and
>
> [d] wherein the memory cells are nonvolatile memory cells having at least one transistor.

Ex. 1001, 12:24–34 (paragraph identifications [a]–[d] are added to align with the parties' arguments); Pet. vi (claims listing).

E. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1 and 13–17 of the '702 patent are unpatentable on the following grounds (Pet. 3):

Ground	Claim(s) Challenged	35 U.S.C. §[1]	Reference(s)/Basis
1A	13–17	103(a)	Lee[2]
1B	16, 17	103(a)	Lee, Endoh[3]
1C	13–17	103(a)	Lee, Kim[4]
1D	16, 17	103(a)	Lee, Kim, Endoh
1E	13–17	103(a)	Lee, Aspar[5]
1F	16, 17	103(a)	Lee, Aspar, Endoh
2A	13	103(a)	Johnson[6]
2B	13	103(a)	Johnson, Kim
2C	13	103(a)	Johnson, Aspar
3	1	103(a)	Park[7], Kim

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. The '702 patent issued May 27, 2008. Ex. 1001, code (45). Accordingly, we apply the pre-AIA version of § 103. *See* 35 U.S.C. § 100(i)(1)(B).

[2] US 2002/0028541 A1, published March 7, 2002. Ex. 1007 ("Lee").

[3] US 2002/0154556 A1, published October 24, 2002. Ex. 1012 ("Endoh").

[4] US 2003/0157748 A1, published August 21, 2003. Ex. 1008 ("Kim").

[5] Aspar, et. al., *The Generic Nature of the Smart-Cut® Process for Thin Film Transfer*, 30 J. Elec. Materials, 834–840 (2001). Ex. 1009 ("Aspar").

[6] US 6,034,882, issued March 7, 2000. Ex. 1010 ("Johnson").

[7] US 5,571,730, issued November 5, 1996. Ex. 1011 ("Park").

III. ANALYSIS

A. Legal Standard

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and "the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner contends that one of ordinary skill in the art would have had "a bachelor's degree in electrical engineering, computer engineering, materials science, or a related field, and at least three years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa." Pet. 9; Ex. 1003 ¶ 37.

Patent Owner contends that one of ordinary skill in the art "would have had a bachelor's degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device

structures, or the equivalent, with additional education substituting for experience and vice versa." PO Resp. 14 (citing Ex. 2029 ¶¶ 34–38).

The parties proposed definitions differ in that Petitioner would permit a degree in "materials science" and require three years, as opposed to two years, of relevant experience. *Compare* Pet. 9 *with* PO Resp. 14. On this record, we adopt Patent Owner's proposed definition, as it is more consistent with the prior art of record and the disclosures of the '702 patent. We note, however, that neither party contends that the outcome of this case depends on the slight differences in the proposed definitions of a person of ordinary skill in the art.

C. Claim Construction

In this proceeding, the claims of the '702 patent are construed "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)." 37 C.F.R. § 42.100(b). Under that standard, the words of a claim are generally given their "ordinary and customary meaning," which is the meaning the term would have had to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Petitioner provides proposed definitions for the terms "stackable add-on layer . . . the stackable add-on layer [is]/[being] bonded" and "SOI pillar." Pet. 10–16. In the Institution Decision, we provided preliminary constructions for both terms. Inst. Dec. 7–12. Patent Owner disagrees with our preliminary constructions, but contends construction of the disputed

terms is not necessary to confirm the patentability of the challenged claims. PO Resp. 15–16.

Upon review of the prior art and the parties' arguments, we determine that only the term "stackable add-on layer" requires construction.[8] *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.")).

"stackable add-on layer"

Claim 1 requires "a first stackable add-on layer" that "is bonded to a layer of the substrate." Ex. 1001, 10:52–53, 10:58–59. Claim 13 requires "a stackable add-on layer" "being bonded to the dielectric layer." *Id.* at 12:29–32. Petitioner contends that based on the plain language of the claim "a stackable add-on layer" "must be its own structure capable of being stacked and added onto the other recited structures." Pet. 10 (citing Ex. 1003 ¶ 71). Petitioner analogizes the claimed memory structure to a layer cake in which each layer is baked individually and then stacked on top of each other to form the final product. *Id.* at 10–11.

[8] Petitioner contends that "the stackable add-on layer [is]/[being] bonded" portion of the claim requires that the "stackable add-on layer" be "wafer bonded to the recited layer of the substrate." Pet. 12. In the Institution Decision, we declined to limit the claims to wafer bonding. Inst. Dec. 10–11 & 10 n.10. The parties now agree that this issue does not need to be addressed in order to resolve the dispute between the parties. PO Resp. 15; Pet. Reply 1.

Petitioner contends the intrinsic record supports this understanding. Pet. 11. According to Petitioner, the '702 patent describes a Silicon-on-Insulator ("SOI") layer as "a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer," and explains that such an SOI layer may be thought of as a "stackable add-on structure." *Id.* (quoting Ex. 1001, 4:48–57).

In the Institution Decision, we preliminarily construed "stackable add-on layer" to be "a layer that is formed separately from the substrate and then bonded to the substrate or a dielectric layer above the substrate." Inst. Dec. 9. We further noted that "[w]e do not understand a 'stackable add-on layer' to include memory cells that are formed by sequential deposition on or above a substrate or dielectric layer without being added to a separately formed substrate." *Id.*

Patent Owner "respectfully disagrees with the Board's preliminary constructions because they are incorrect," but does not propose its own construction or explain why the Board's construction is incorrect. PO Resp. 15. Patent Owner contends the Board may confirm the patentability of the challenged claims for reasons unrelated to the construction of this term. *Id.*

Neither party asserts that "stackable add-on layer" has an accepted meaning in the art. *See Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004) (stating that, absent an accepted meaning in the art, "we construe a claim term only as broadly as provided for by the patent itself"). Thus, we must attempt to discern the meaning of this term from the claim language itself and from the remainder of the intrinsic record. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir.

1996) ("It is well-settled that, in interpreting an asserted claim, the court should look first to the intrinsic evidence of record, *i.e.*, the patent itself, including the claims, the specification and, if in evidence, the prosecution history."). Upon review of the parties' arguments and the intrinsic record, we agree with Petitioner that the '702 patent does not support a construction of "stackable add-on layer" that encompasses memory cells formed by sequential deposition on a substrate without being formed and then added to a separately formed substrate. Pet. 11–12.

First, the plain language of the claim does not require merely a "layer" having a plurality of vertically oriented semiconductor memory cells, but rather "a stackable add-on layer" having a plurality of vertically oriented semiconductor memory cells; that plurality is bonded to the dielectric layer. Ex. 1001, 12:29–32. A construction that gives meaning to all words of the claim is preferred. *Merck & Co., Inc. v. Teva Pharm. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.").

Second, the written description of the '702 patent summarizes the invention by stating that "a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells" is formed separately from the substrate and then stacked on and bonded to the substrate. Ex. 1001, 1:47–50 ("Briefly, a plurality of vertically oriented semiconductor memory devices, or cells, may be ***added to a separately fabricated substrate*** that includes electrical devices and/or interconnect lines.") (emphasis added). The '702 patent discloses two ways of adding a memory cell layer. "The plurality of vertically oriented semiconductor memory cells [can be] added to the separately fabricated substrate as a thin layer including several doped

semiconductor regions which, subsequent to attachment, are etched to produce individual doped stack structures." *Id.* at code (57), 1:57–62. "Alternatively, the plurality of vertically oriented semiconductor memory cells may be completely fabricated prior to attachment" to the separately fabricated substrate. *Id.* at code (57), 1:67–2:3. In both of these methods, the memory cells are added as a completed layer to a separately fabricated substrate.

Generally supporting this understanding, the specification explains that a Silicon-on-Insulator ("SOI") layer refers to "a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate." Ex. 1001, 4:47–53. According to the '702 patent, "[i]n this context, the SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections." *Id.* at 4:53–57. Consistent with the summary of the invention discussed above, this description in the '702 patent suggests that a "stackable add-on layer" is a layer that is formed separately from the semiconductor substrate and then bonded to substrate that already contains devices and/or interconnections, i.e., a separately fabricated substrate. We further note that we are directed to no embodiment of the '702 patent wherein layers that are sequentially deposited on the substrate are identified as a "stackable add-on layer."

In view of the foregoing, we construe "stackable add-on layer" to mean "a layer formed separately from the substrate suitable to be bonded to

the dielectric layer positioned above the substrate." Our construction also provides that a "stackable add-on layer" should not be read to include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate.

D. Claims 13–17 over Lee (Ground 1A)

Petitioner contends the subject matter of claims 13–17 would have been obvious over the disclosures of Lee. Pet. 16–41.

1. *Lee*

Lee is titled "Dense Arrays and Charge Storage Devices, and Methods for Making Same" and published March 7, 2002. Ex. 1007, codes (43), (54).

Lee aims to reduce the cost of memory and logic devices by increasing device density. Ex. 1007 ¶ 106. Lee states it achieves these objectives by providing "a monolithic three dimensional array of charge storage devices comprising a plurality of device levels." *Id.* ¶ 107. In this context "monolithic" means that the layers of each level of the array are directly deposited on the layers of each underlying level of the array. *Id*. This is in contrast to two-dimensional arrays, which "may be formed separately and then packaged together to form a non-monolithic memory device." *Id.*

Figure 35 is reproduced below:

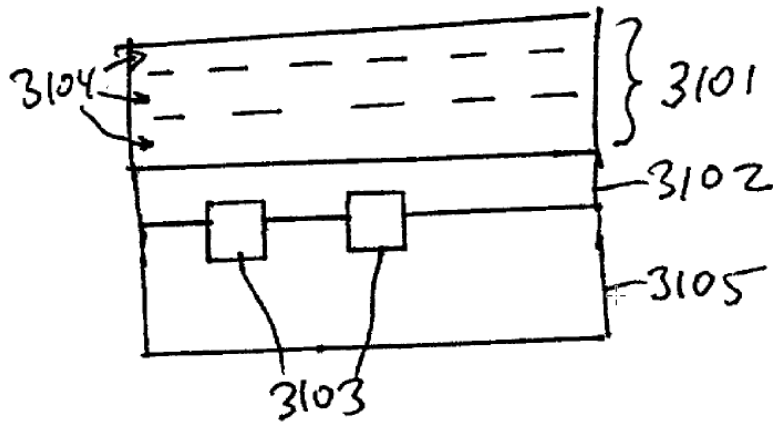


FIGURE 35

Figure 35 is a schematic of a three-dimensional array of devices. Ex. 1007 ¶ 60. In the device of Figure 35, driver circuits 3103 are disposed in monocrystalline substrate 3105 as CMOS or other transistors, and interlayer insulating layer 3102 is then disposed on monocrystalline substrate 3105. *Id.* ¶ 111. Charge storage logic or memory devices 3101 have a plurality of device levels 3104 that are preferably separated by interlayer insulating layers. *Id*.

Lee explains that "[t]he charge storage devices of the array may be any type of semiconductor devices which store charge, such as EPROMs or EEPROMs." Ex. 1007 ¶ 113. Such charge storage devices may be formed in various configurations, "such as a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM, a rail stack TFT EEPROM, and various other configurations." *Id.*

Figure 1A of Lee is reproduced below:

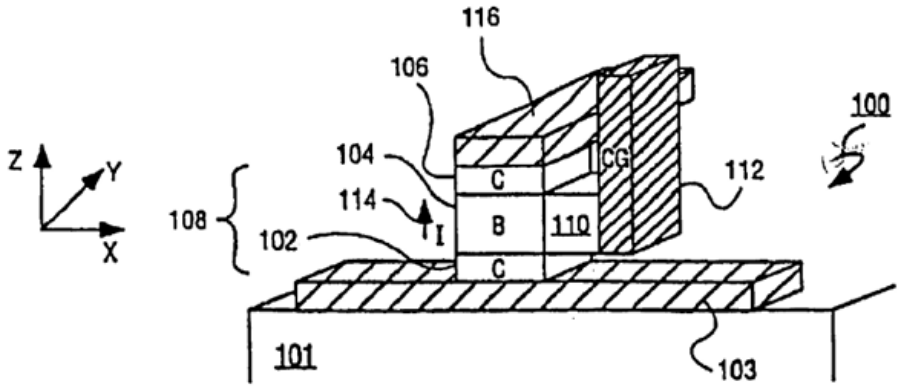


FIG. 1A

Figure 1A "is an illustration of a pillar memory." Ex. 1007 ¶ 38. In Figure 1, "[p]illar memory device 100 includes a first contact region 102 formed on a first input/output (I/O) 103 conductor formed on or above a plane (x-y) of a single crystal substate 101." *Id.* ¶ 122. Semiconductor body 104 is formed directly on first contact region 102 and a second contact region 106 is formed on the body 104. *Id.* "A second I/O region 116 is formed on the second contact region 106." *Id.* Lee explains that first contact region 102, body 104, and the second contact region 106 are each vertically aligned to form a pillar 108. *Id.* "Adjacent to and in contact with body 104 is a charge storage medium 110," with control gate 112 formed adjacent to and in direct contact with charge storage medium 110. *Id.*

Lee explains that:

> The programmed and unprogrammed state of the pillar memory device is determined by whether or not charge is stored in charge storage medium 110. The charge stored in the charge storage medium adds or subtracts from the voltage applied to the control gate, thereby altering the voltage required to form a conducting channel in body 104 to enable a current (e.g., read

current I_R) to flow between the first and second contact (source/drain) regions.

Ex. 1007 ¶ 123.

Figure 2 is reproduced below:

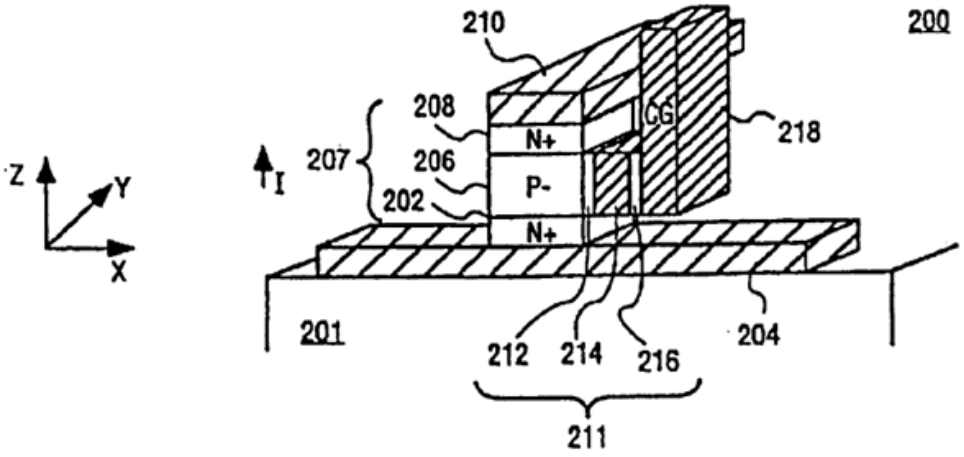


FIG. 2

Figure 2 is an illustration of a pillar memory. Ex. 1007 ¶ 41. In this embodiment, pillar 207 includes a first source/drain contact region 202 comprising a heavily doped N+ silicon film that is formed on a first input/output 204 (e.g. bit line) that is formed on or above a substrate 201. *Id.* ¶ 126. Body 206 is composed of a lightly doped P- type silicon film 206 that is formed on and in direct contact with N+ source/drain contact region 202. *Id*. Second drain region 208 is composed of a heavily doped N+ silicon film and is formed on and in direct contact with P type silicon film 206. *Id*. "A second conductive input/output (e.g. word line/bit line) 210 is formed on the second N+ source/drain region 208." *Id*. Charge storage medium 211 comprises a tunnel dielectric 212, floating gate 214, and control gate dielectric 216. *Id* ¶ 127. Control gate 218 is formed adjacent to, and in

direct contact with, control gate dielectric 216. *Id*. "Control gate 218 is formed of a conductor such as but not limited to doped silicon or a metal such as tungsten." *Id.*

Figure 9A is reproduced below:

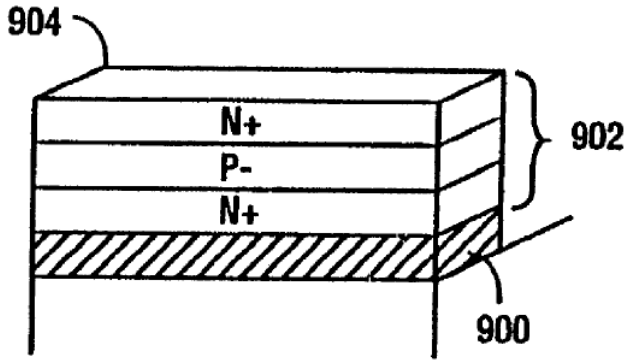


FIG. 9A

Figure 9A "illustrates a method of forming a pillar utilizing an intersection etch technique." Ex. 1007 ¶ 48. In Figure 9A, first I/O conductor 900 is blanket deposited, "followed by the sequential blanket deposition of the film stack 902 (e.g., N+/P-/N+) of the desired pillar." *Id.* ¶ 141. "The first I/O film 900 and the pillar film stack 902 are then etched to form a plurality of pillar strips 904 as shown in Fig. 9a." *Id.* Pillar strips 904 may then be etched to form individual pillars with associated I/O films. *Id.*

2. *Analysis—Claim 13*

Petitioner contends Lee discloses every limitation of independent claim 13. Pet. 16–31. With respect to the preamble and element 13[a], Petitioner contends that Figure 35 of Lee discloses a "semiconductor

memory structure" including substrate 3105 having driver circuits 3103 disposed therein. *Id.* at 17–19 (citing Ex. 1007 ¶¶ 110–111). Petitioner further contends that Figure 35 discloses interlayer insulating layer 3102 that is above substrate 3105 and driver circuits 3103. *Id.* at 20 (citing Ex. 1007 ¶ 111; Ex. 1003 ¶ 118). With respect to elements 13[b] and 13[c], Petitioner asserts that, if Patent Owner argues that a "stackable add-on layer" encompasses any type of layer that is directly or indirectly adhered to the "dielectric layer," then bottom-most level 3104 in Figure 35 teaches elements 13[b] and 13[c]. *Id.* at 20–27, 29–30. With respect to element 13[d], Petitioner contends that one of ordinary skill in the art would have understood that the memory cells depicted in Figures 1A–1B, 2, 7, and 25A, are all nonvolatile memory cells. *Id.* at 30–31 (citing Ex. 1007 ¶¶ 6, 113, 122, 125; Ex. 1003 ¶ 139).

As discussed above, we do not understand a "stackable add-on layer" to include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate. It is undisputed, and indeed it is Petitioner's assertion, that Lee's memory devices are formed by sequential deposition. Pet. 16, 29 n.11, 51 ("In Lee, each level 3104 is deposited on the underlying level of array 3101."). Therefore, Petitioner has not shown that Lee discloses every limitation of independent claim 13 under our claim construction. Thus, Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious in view of Lee.

3. *Analysis: Claims 14–17*

Claims 14–17 each depend, directly or indirectly, from claim 13. Petitioner's arguments with respect to these claims do not remedy the deficiencies noted above with respect to claim 13. Pet. 31–41. Accordingly, Petitioner does not demonstrate by a preponderance of the evidence that claims 14–17 would have been obvious over Lee.

E. Claims 16 and 17 over Lee and Endoh (Ground 1B)

Petitioner contends "Lee and Endoh teach claims 16 and 17's additional limitations under [Patent Owner's] apparent interpretation of 'SOI pillar.'" Pet. 41–42. Claims 16 and 17 depend from claim 13, and Petitioner's arguments with respect to these claims do not remedy the deficiencies noted above with respect to claim 13. Pet. 41–50. As such, Petitioner does not demonstrate by a preponderance of the evidence that claims 16 and 17 would have been obvious based on the combined disclosures of Lee and Endoh.

F. Claims 13–17 over Lee and Aspar (Ground 1E)

Petitioner contends the subject matter of claims 13–17 would have been obvious over the combined disclosures of Lee and Aspar. Pet. 55–63.

1. *Aspar*

Aspar is an article published in the Journal of Electronic Materials and is titled *The Generic Nature of the Smart-Cut® Process for Thin Film Transfer*. Ex. 1009. Aspar explains that the Smart-Cut process "is based on ion implantation and wafer bonding." *Id.* at 834. Aspar states that ion implantation induces formation of an in-depth weakened layer that leads to delamination of a thin film from a thick substrate. *Id.* Wafer bonding and

layer transfer then enable different materials to be associated to form multilayer substrates. *Id.* According to Aspar, the Smart-Cut process was "first developed to obtain silicon-on-insulator (SOI) materials," and is now "an industrial process which provides high quality materials in large quantities." *Id.*

Figure 1 of Aspar is reproduced below:

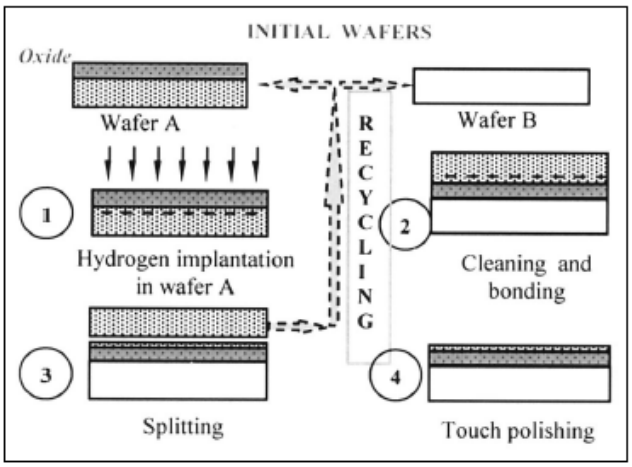


Figure 1 is a "[s]chematic description of the Smart-Cut® process, used to obtain SOI wafers." Ex. 1009, 835. The process for obtaining an SOI wafer begins with substrate A having an oxide layer on monocrystalline silicon. *Id.* at 834. Hydrogen implantation in substrate A induces formation of an in-depth weakened layer beneath the oxide layer. *Id.* Substrate A is then bonded to a support B by wafer bonding. *Id.* A splitting step is then performed, allowing the transfer of an oxide layer and a thin layer of monocrystalline silicon from substrate A onto support B. *Id.* A final treatment may then be performed to remove the rough surface left after splitting. *Id.* According to Aspar, this technique enabled the authors to obtain SOI wafers with "very good crystalline quality of the top silicon layer." *Id.* at 837.

Aspar notes that "[r]ealizing multiple SOI layers based on a layer transfer process can be achieved in many different ways: repeating a single layer transfer several times onto a same wafer, [or] transferring SOI layers stacks already formed onto a single substrate or a SOI wafer." Ex. 1009, 839. Thus, according to Aspar, "multiple SOI layers stacks can be easily performed thanks to Smart-Cut technology (Fig. 14)." *Id.*

Figure 14 of Aspar is reproduced below:

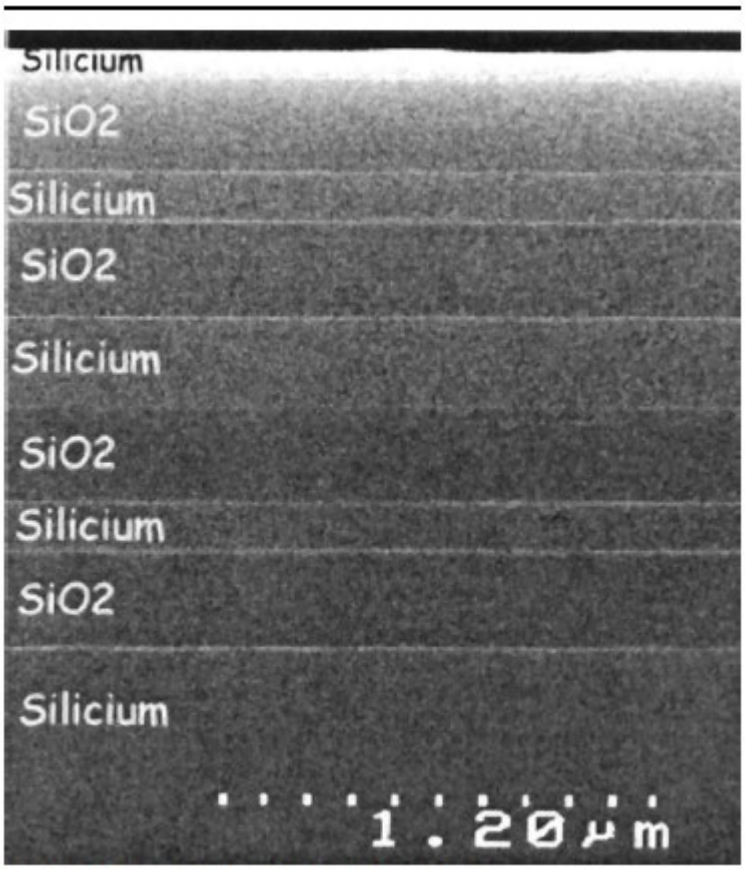
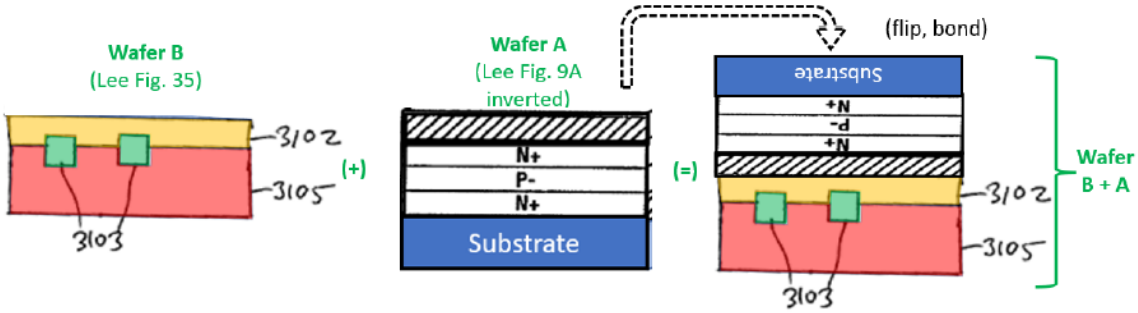


Fig 14. SEM view of multiple SOI layer stack.

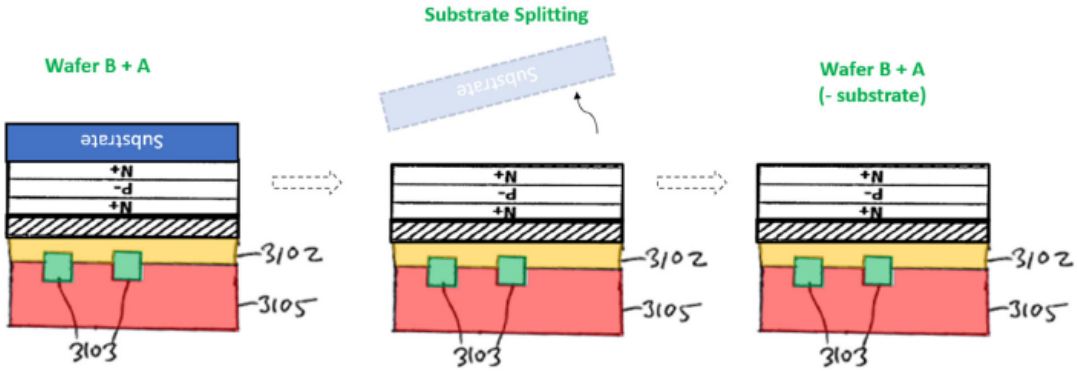
Figure 14 of Aspar depicts a "multiple SOI layer stack," consisting of alternating layers of silicium (silicon) and SiO_2. Ex. 1009, 838, Fig. 14.

2. *Analysis – Claim 13*

Petitioner contends that Lee and Aspar disclose the preamble and limitations 13[a], [b], and [d] for the same reasons discussed above with respect to the ground based on Lee alone.[9] Pet. 56, 63. With respect to limitation 13[c], Petitioner contends that Aspar discloses "transferring SOI layer stacks already formed onto a single substrate or a SOI wafer," and one of ordinary skill in the art would have sought to use this method to wafer bond bottom level 3104 ("stackable add-on layer") in Lee's Figure 35 to insulating layer 3102 ("dielectric layer"). *Id.* at 56–58. Petitioner provides the following illustrations of its proposed combination:



[9] As discussed above, we determine that Petitioner has not shown that Lee teaches or suggests limitation 13[b] under our construction for "stackable add-on layer." Petitioner's arguments regarding Lee and Aspar rely on its arguments with respect to Lee alone for limitation 13[b] and do not expressly address how the combination of Lee and Aspar teaches this limitation. Pet. 56; *see also* C.F.R. § 104(b)(4) ("The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon."). Accordingly, for at least this reason, Petitioner has not shown that the combination of Lee and Aspar teaches or suggests limitation 13[b].



Id. at 59–60. The illustrations above are Petitioner's depiction of the combination of Wafer B (a portion of Figure 35 of Lee) and Wafer A (Figure 9A of Lee (inverted and applied to a substrate)) to form a combined Wafer B + A. *Id.* at 59. Petitioner contends that, after bonding, the substrate (blue) would be removed and individual memory cells in level 3104 would be fabricated from the transferred thin layer in the same way they are fabricated in Lee. *Id.* at 60.

Petitioner contends one of ordinary skill in the art would have been motivated to make such a combination for several reasons. Pet. 60. First, Petitioner contends that it is unclear in Lee how the bottom level 3104 of array 3101 is formed on insulating layer 3102. *Id.* at 56.

Second, Petitioner contends that the proposed combination would have amounted to using a known technique both to improve a similar known device in the same way and to address the same known problem recognized by both Lee and Aspar using prior art elements according to their established functions. Pet. 61,

Third, Petitioner contends that use of Aspar's process as compared to monolithic deposition would allow "for more efficient quality control at the layer formation stage." Pet. 61 (citing Ex. 1003 ¶ 213).

Patent Owner argues that Petitioner does not establish a motivation to combine Lee and Aspar and advances several reasons why one of ordinary skill in the art would not have combined the references in the manner proposed by Petitioner. PO Resp. 18–20, 44–52; PO Sur-reply 6–7.

For the reasons discussed below, we are not persuaded by Petitioner's rationales for combining Lee and Aspar and credit several of Patent Owner's counter-arguments. In addition, we determine that Petitioner's process optimization argument exceeds the proper scope of a reply.

a. *Bonding Level 3104 of Array 3101 on Insulating Layer 3102*

Petitioner contends that Lee does not clearly describe how bottom level 3104 of array 3101 is formed on insulating layer 3102 and that one of ordinary skill in the art would have looked to other art to determine how to perform this step. Pet. 56. We disagree with this premise. Lee discloses that in its monolithic array of memory devices "each level of the array [is] directly deposited on the layers of each underlying level of the array." Ex. 1007 ¶¶ 107, 111, 141 (noting that the pillar of Figure 9 may be formed by "blanked depositing a first I/O conductor 900 followed by the sequential blanket deposition of the film stack 902 (e.g., N+/P-/N+) of the desired pillar"). Thus, as asserted persuasively by Patent Owner, Lee explains how each level of its array is formed, i.e., by direct deposition on the underlying layer. *See id.*; PO Resp. 21, 44; Ex. 2029 ¶¶ 115–116, 142–143.

Petitioner contends that deposition is just one potential implementation technique for the embodiment depicted in Figure 35 of Lee, and Lee contemplates using techniques with SOI technology, including "wafer bonding." Pet. Reply 6–7. This argument is not persuasive. Lee

expressly states that each level of its memory array is directly deposited on the underlying level of the array. Ex. 1007 ¶¶ 107, 111, 141. Moreover, although Lee discusses SOI technology and wafer bonding, it is with respect to other embodiments and with respect to forming the substrate on which the semiconductor active area is "deposited." *Id.* ¶¶ 208–209; Sur-reply 11.

In view of the foregoing, we are not persuaded by Petitioner's first rationale that one of ordinary skill in the art would have looked to art beyond Lee, including the wafer bonding art of Aspar, to determine how to attach or bond bottom level 3104 to insulating layer 3102 in Lee.

b. *Known Process to Solve a Known Problem*

As explained in *KSR*, "if a technique has been used to improve one device, and a person of ordinary skill would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *KSR*, 550 U.S. at 417. In addition, "if there is a known technique to address a known problem using prior art elements according to their established functions, then there may be a motivation to combine." *See Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023).

Petitioner contends that Aspar teaches realizing "multiple SOI layers based on a layer transfer process . . . [such as] transferring SOI layers stacks already formed onto a single substrate or SOI wafer. So multiple SOI layers can be easily performed thanks to Smart-Cut technology." Pet. 60 (quoting Ex. 1009, 839). Petitioner also contends that Aspar's Smart-Cut process was known to have several advantages, including "transferring thin layers of very good thickness homogeneity and with a high crystalline quality." *Id*. at 60–

61 (quoting Ex. 1003 ¶ 212; Ex. 1009, 834); Pet. Reply 6 (citing Ex. 1009, 834, 839; Ex. 1037 ¶ 13). Applying *KSR*, Petitioner contends that the combination of Lee and Aspar would have amounted to using a known technique (Aspar's Smart-Cut process) both "to improve a similar known device (the structure in Lee's Figure 35) in the same way (vertically stacking memory devices using SOI technology)" and "to address the same known problem recognized by both Lee and Aspar (fabricating 3D structures) using prior art elements according to their established functions (Aspar's Smart-Cut® process and Lee's Figure 35 memory device using the memory cell structures of Figure 1A-1B, 2, 7, or 25A)." *Id.* at 61; Pet. Reply 5.

We agree with Patent Owner that Petitioner has not demonstrated that Aspar would improve Lee, would solve a problem in Lee, and that Petitioner is proposing to use Aspar in a way that is not disclosed in the reference. PO Resp. 49–50 (citing Ex. 2029 ¶¶ 153–162); Tr. 57:24–58:12; Pet. 61; *KSR*, 550 U.S. at 417 (asking whether a technique "would improve similar devices in the same way"), 420 (asking whether there was a known problem in the art), 421 (asking whether one of ordinary skill in the art had reason to "pursue the known options"); *Intel*, 61 F.4th at 1381 (explaining that obviousness may be demonstrated by showing that there was a known problem in the art ("cache coherency in multiprocessor systems") and that a person of ordinary skill in the art would recognize that that the prior art solution to this problem ("global segmented secondary cache") would improve the system of another prior art reference).

Petitioner does not persuasively show that there was any known problem in the art with respect to Lee or its monolithic method of constructing memory arrays. Nor does Petitioner provide persuasive

argument or evidence that Aspar's wafer bonding would improve Lee's memory device.[10] For example, Petitioner states in a conclusory fashion that Aspar would address the known problem of "fabricating 3D structures," but does not explain what those problems were or why Lee fails to solve them. Pet. 61. Dr. Sechen's testimony merely parrots the Petition, providing no further analysis or explanation of what problem might exist in Lee when fabricating its 3D structures. Ex. 1003 ¶ 212. The Petition notes that Aspar transfers "thin layers of very good thickness homogeneity and with a high crystalline quality," but the Petition never asserts that Lee's direct deposition method fails to provide these same or similar qualities. Pet. 60–61.

Moreover, as noted by Patent Owner, Petitioner appears to use Aspar in a way that is not disclosed in the reference. PO Resp. 49–50. Aspar discloses transferring a layer of SiO_2 (insulator) and a thin layer of silicon having high crystalline quality. Ex. 1009, 834–835, 838 (Figs. 12 and 14). In Petitioner's proposed combination, "Wafer A" would consist of a substrate, an N+/P-/N+ (NPN) doped stacked structure (silicon layer), and a metal layer. Pet. 59. Petitioner points to no disclosure in Aspar, however, of transferring a doped stacked structure (N+/P-/N+), eliminating the SiO_2 layer, or applying the splitting process to a wafer having a metal layer above the silicon layer. Pet. 60; Tr. 58:6–8, 68:4 ("The oxide isn't in our combination."); Ex. 2029 ¶ 155 ("Aspar's Figure 1 shows only an

[10] As discussed below, Petitioner contends there were advantages to using Aspar's method, including reduced waste. Petitioner does not persuasively demonstrate, however, that Aspar would improve Lee's memory device in terms of performance or costs.

unpatterned oxide layer on Wafer A and a clean Wafer B prior to bonding and cleaving.”).

Petitioner argues that “[i]mprovement in a categorical sense is not required: the Petition need only show Kim’s/Aspar’s techniques are ‘suitable options.’” Pet. Reply 6 (citing *Intel*, 61 F.4th at 1381). Petitioner has not, however, shown that Aspar’s technique was known to be a suitable option for making vertically stacked memory cells, as disclosed in Lee, in the relevant time period. As discussed above, Aspar’s Smart-Cut technique is disclosed for making SOI wafers and multiple *SOI layer* stacks. Ex. 1009, 834–835, 838 (Figs. 12 and 14). Petitioner points to no disclosure in Aspar of creating the doped stacked structures posited in the Petition (Pet. 59–60), especially without the SiO_2 layer. Even if Petitioner had shown that Aspar’s technique was a known alternative for making vertically stacked memory cells, simply showing that two options were known in the art is not sufficient to explain why one would be substituted for the other. *Virtek Vision Int’l ULC v. Assembly Guidance Sys.*, 97 4th 882, 887–888 (Fed. Cir. 2024).

Because the proposed combination has not been shown to improve Lee, solve a problem in Lee, or apply a known method in a known way, Petitioner has not persuasively demonstrated that its *KSR*-based arguments support the combination of Lee and Aspar. PO Resp. 51 (“In the complicated field of semiconductors, [Petitioner] needs to provide ‘specific evidence’ justifying its significant departures and extensions from Aspar’s actual disclosure.”).

c. *Quality Control, Minimized Waste, and Process Optimization*

Petitioner contends one of ordinary skill would have sought to

construct the memory of Lee using Aspar's Smart-Cut process because this would "minimize waste resulting from defects detected in quality control." Pet. 62. Specifically, Petitioner contends that Aspar's Smart-Cut process allows "quality control [to] be performed on the stack prior to bonding (e.g., thickness, uniformity, etc.)" and, "[i]f a quality control issue is detected, then only that stack would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited stacks, etc.) would need to be discarded." *Id.* at 61–62 (citing Ex. 1003 ¶ 213).

Petitioner's rationale is not persuasive. First, as noted by both parties, in the proposed combination of Lee and Aspar the unpatterned, doped stacked structure is transferred to the substrate. Pet. 60; PO Resp. 49; Pet. Reply 14. Petitioner does not persuasively demonstrate any need in the art for discarding doped stacked structures for quality control reasons, for example, because they do not have an appropriate thickness or uniformity. *See* Sur-reply 12–13 (noting that quality control in the art focused on testing of memory cells, not unpatterned layers); Ex. 2029 ¶ 145 (asserting that the memory cell errors a person of ordinary skill in the art would have wanted to test for "would necessarily arise after Smart-Cut's bonding and cleaving"). Indeed, as noted by Patent Owner, references provided by Petitioner indicate that the deposition process for doped silicon layers can be effectively quality controlled and tested during fabrication. Ex. 1047, 308 (noting that the deposition rate and resistivity may be effectively controlled during the deposition process); PO Resp. 49; Sur-reply 12–13.

Second, Petitioner's counsel explained that if such a thickness or uniformity problem were detected, the layers could simply be scraped off

and redeposited. Tr. 18:12–19:3. It is unclear, on this record, why such a scraping method could not likewise be used if the first NPN layer directly deposited on Lee's substrate were determined to have a defect in uniformity or thickness.

Third, to the extent quality control were a motivating factor for combining Lee and Aspar, we find persuasive Patent Owner's argument that the risk of damaging the NPN stack through the high temperature anneal step of Aspar would create increased waste and outweigh any perceived quality control benefits. Ex. 2039 ¶ 145; *see Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 795–96 (Fed. Cir. 2021) (noting that simultaneous advantages and disadvantages to a proposed combination must be analyzed to determine whether the disadvantages "outweighed any reason to combine").

d. *Process Optimization*

In its Reply, Petitioner contends that process optimization would have motivated the proposed combination of Lee and Aspar. Pet. Reply 10. Petitioner reasons that it was known in the art that in a linear process "a later processing step can cause perturbations of previous processing steps." *Id.* (citing Ex. 2039, 91:17–98:9). For example, heat used during subsequent processing steps could cause metal to deform possibly creating opens or shorts. *Id.* (citing Ex. 2039, 96:15–97:11). According to Petitioner, fabricating devices on separate substrates, "each according to an optimized process," would avoid such issues and potentially increase yields. *Id.* (citing Ex. 1008 ¶ 22; Ex. 1044, 145–146; Ex. 1049, 6:42–56; Ex. 1050, 525; Ex. 1037 ¶¶ 22–23). Petitioner also contends that using the proposed combination one could provide "monocrystalline" silicon, which would

improve Lee's device. *Id.*

"It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify 'with particularity' the 'evidence that supports the grounds for the challenge to each claim.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3)). Any marked departure from the grounds identified with particularity in the petition would impose "unfair surprise" on the patent owner and, consequently, violate both the Administrative Procedure Act and the *inter partes* review statute. *Arthrex Inc. v. Smith & Nephew, Inc.*, 935 F.3d 1319, 1328 (Fed. Cir. 2019). Strikingly absent from Petitioner's argument is any citation to the Petition that raises this specific motivation to combine Lee and Aspar. Pet. Reply 10. Thus, we agree with Patent Owner that process optimization is a new argument supporting the combination of Lee and Aspar that should have been raised in the Petition. Sur-reply 14–15. As such, we do not consider this new argument. *Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1383 (Fed. Cir. 2023) ("[T]he Board acts within its discretion when declining to consider a new theory of unpatentability raised by petitioner in reply.").

e. *Patent Owner's Counterarguments*

Petitioner does not meet its burden to show obviousness of combining Lee and Aspar for the reasons stated above. Our determination is reinforced by consideration of Patent Owner's counterarguments, as discussed below.

1. High Temperature Annealing

Patent Owner contends that Aspar's method includes a high temperature annealing step that would risk frying the underlying electronics of the substrate. PO Resp. 45–49. In support of this argument, Patent Owner turns to the disclosure of Aspar's Smart-Cut process in Wolf,[11] including Figure 11.24 reproduced below.

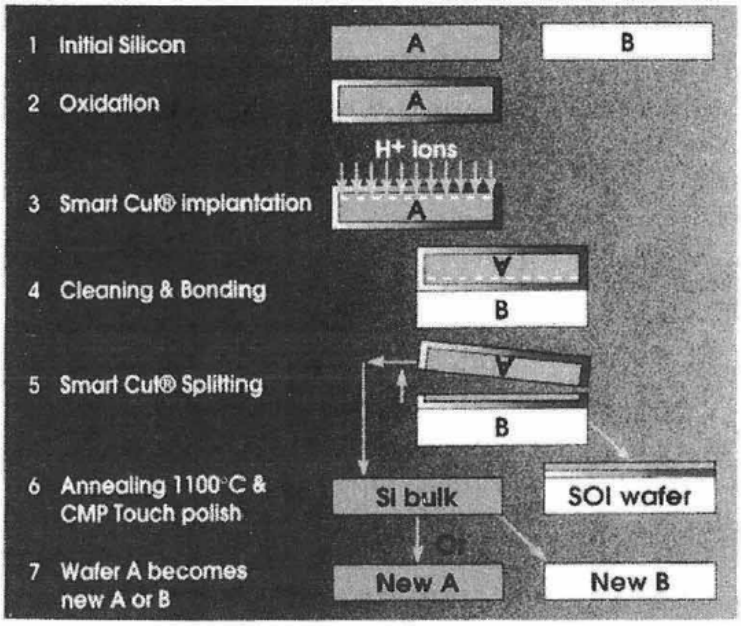


Fig. 11-24 Process flow for fabricating Smart-Cut® wafers.

Figure 11-24 of Wolf depicts the process flow for fabricating Smart-Cut wafers. Ex. 1015, 543. As shown in this figure, Wolf describes the same general process steps as Aspar, but expressly includes a 1100° C annealing step, that is used to "remove defects." *Id.* at 543–44. Patent Owner contends this annealing step would exceed the thermal budget of the underlying substrate and would damage the control circuitry (transistors) in

[11] S. Wolf, *Silicon Processing for the VLSI Era*, *Volume 4 – Deep-Submicron Process Technology*, Lattice Press, 2002. Ex. 1015.

the substrate and/or the doped stacked structure in Petitioner's proposed combination of Lee and Aspar. PO Resp. 47–48; Ex. 2029 ¶¶ 150–152.

Petitioner contends that the 1100° C annealing step is not required in Aspar, and it was known in the art to use much lower temperatures during the Smart-Cut process, as confirmed by the '702 patent's parent, the '941 patent.[12] Pet. Reply 12–13 (citing Ex. 1005, 8:60–62, 9:40–47, 10:19–21).

Patent Owner argues in its Sur-reply that Dr. Sechen relied upon Wolf's annealing step in his declaration and that Petitioner's attempts to rely on the '702 and '941 patents only confirms Petitioner is using "improper hindsight" to reconstruct the claimed invention. Sur-Reply 15–16 (citing Ex. 1003 ¶ 46). According to Patent Owner, it was the '702 patent that "explained how to build its architecture with low-temperature processing." *Id.* at 16.

For the following reasons, we find that Patent Owner has the better side of the high temperature annealing arguments.

Aspar discloses a process for obtaining SOI wafers that includes a "touch polishing" step after Wafers A and B are split, but Aspar does not expressly discuss an annealing step at 1100° C. Ex. 1009, 835. Both Dr. Przybylski and Dr. Sechen, however, present evidence that one of ordinary skill in the art would have understood that Aspar's process includes a high-temperature annealing step, which was often performed at up to 1100° C. Ex. 1003 ¶¶ 46, 80–81; Ex. 2029 ¶ 148. For example, in his declaration Dr. Sechen indicates that the Smart-Cut method is "shown" in Figure 11-24 of Wolf, which includes an 1100° C annealing step for both

[12] US 7,052,941 B2, issued May 30, 2006, "the '941 patent" (Ex. 1005).

Wafers A and B (containing the SOI layer). Ex. 1003 ¶ 46 (asserting that "[t]he Smart-Cut® method (shown below) starts by oxidization and ion-implantation of wafer A."); Ex. 1015, 543, Fig. 11-24; Ex. 2039, 118:10–119:2 (Dr. Sechen testifying that Wolf Figure 11-24 is describing the same process he referenced in Aspar—"This figure is entirely consistent, if not outright the same as Aspar's"). Likewise, Dr. Sechen points to Srikrishnan[13] as disclosing the Smart-Cut process, and Srikrishnan discloses applying a high temperature (approximately 1000° C) annealing step during the Smart-Cut process. Ex. 1003 ¶¶ 80–81; Ex. 1023, 5:16–50 ("Then, preferably, the support substrate 530 with the thin silicon layer 510 (device layer) still bonded to it is annealed at a high temperature (approximately 1000° C) for about 30 minutes to 8 hours to promote a stronger bonding.").

Petitioner contends Wolf is not part of its combination and the '941 patent, incorporated by reference in the '702 patent, "discloses a Smart-Cut process without any post-splitting anneal." Pet. Reply 12–13 (citing Ex. 1005, 8:60–62, 9:40–47, 10:19–21). This is so, according to Petitioner, because the substrate will not withstand temperatures over 650° C. *Id.* at 13. The '941 patent, however, is part of the priority chain of the '702 patent and Petitioner has not demonstrated that the disclosures of the '941 patent are prior art with respect to the '702 patent.

Given the disclosures of Wolf and Srikrishnan and the testimony of Dr. Sechen cited above, we credit the testimony of Dr. Przybylski that, in the relevant time period, one of ordinary skill in the art would have understood the Smart-Cut process to include a high-temperature annealing step that

[13] US 5,882,987, issued March 16, 1999. Ex. 1023.

would potentially damage transistors or the NPN stack in Petitioner's proposed combination. Ex. 2029 ¶¶ 148–152. As such, Petitioner has not demonstrated by a preponderance of the evidence that one of ordinary skill in the art would have combined Lee and Aspar to arrive at the claimed invention with a reasonable expectation of success.[14]

2. Remaining Thin Layer

Patent Owner contends that the Smart-Cut process "indisputedly left a thin film remaining" after the splitting process that would obstruct Lee's upper metal contact, and which Petitioner never explains how to avoid. PO Resp. 51. In the reply brief, Petitioner contends that, in the proposed combination of Aspar and Lee, the remaining silicon layer identified by Patent Owner is the doped stacked structure of Lee. Pet. Reply 14.

Even taking into account Petitioner's reply contention, the proposed combination remains poorly defined and tainted by hindsight bias. In Aspar, hydrogen is implanted through the SiO_2 layer and into the underlying monocrystalline silicon of Wafer A. Ex. 1009, 834. Then, after Wafers A and B are bonded, a splitting step takes place that gives rise to the transfer of the SiO_2 layer and a thin layer of silicon from Wafer A to Wafer B. *Id.* Petitioner's proposed combination, however, does not use a monocrystalline silicon wafer with a SiO_2 layer, and Petitioner does not explain where

[14] Even if it were known in the art that Aspar's wafer bonding method could be used at 650° C or less, our conclusion regarding the combination of Lee and Aspar would remain the same. The evidence that Aspar's method was known to use a 1000° or 1100° C annealing step merely serves to reinforce our determination that Petitioner has not met its burden to show obviousness based on Lee and Aspar.

hydrogen implantation would take place in the proposed sequence of process steps (Pet. 59–60) or where the resulting "weakened layer" (Ex. 1009, 834) would be in its proposed combination. Petitioner also does not explain how the substrate (blue) could be removed during the splitting process without either leaving a small portion of substrate on the upper surface, or removing a portion of the N+ layer that is in contact with the substrate.

In our view, Petitioner's proposed combination of Lee and Aspar appears to have been guided by hindsight reconstruction rather than the knowledge and skill of the ordinarily skilled artisan. Petitioner's proposed sequence of process steps (Pet. 59–60) is insufficiently supported by the references, which do not teach or suggest inverting an NPN stack with a conductive layer (Petitioner's Wafer A) and flip-bonding it a substrate having control circuitry and a conductive layer (Petitioner's Wafer B), with the conductive layer being bonded to the insulating layer. Aspar discloses the Smart-Cut process for making SOI wafers, not transferring NPN stacks with conductive layers to substrates with control circuitry and an insulating layer.

The poorly defined nature of the combination and Petitioner's apparent reliance on hindsight reconstruction reinforces our determination that Petitioner fails to show that it would have been obvious to combine Lee and Aspar. PO Resp. 51 (asserting that Petitioner provides only a "vague idea" of how Lee and Aspar would be combined).

f. *Conclusion – Reason to Combine and Reasonable Expectation of Success*

For the reasons discussed above, Petitioner does not persuasively demonstrate that one of ordinary skill in the art would have sought to

combine Lee and Aspar to arrive at the claimed invention. Nor does Petitioner demonstrate that one of ordinary skill in the art would have had a reasonable expectation of success in so doing, as Aspar's high temperature anneal step would damage the device.

G. Claims 13–17 over Lee and Kim (Ground 1C)

Petitioner contends that claims 13–17 would have been obvious over the combined disclosures of Lee and Kim. Pet. 50–54.

1. *Kim*

Kim discloses a "process of vertically stacking multiple wafers supporting different active IC devices on a single die with low cost and high via density with optimum metal bonding areas." Ex. 1008 ¶ 1. Kim notes that as integrated circuit (IC) technology progresses, there is a desire for a "system on a chip" in which the functionality of all the IC devices of the system are packaged together without a conventional printed circuit board. *Id.* ¶ 4. "In practice, however, it is very difficult to implement a truly high-performance 'system on a chip' because of vastly different fabrication processes and different manufacturing yields for the logic and memory circuits." *Id.*

Kim explains that one known method of vertically stacking wafers was three-dimensional (3D) wafer-to-wafer vertical stack technology, in which multiple layers of active IC devices, such as processors, programmable devices and memory devices, are vertically stacked inside a single chip. Ex. 1008 ¶ 7. A major challenge to such methods "is the bonding between wafers and between die in a single chip." *Id.* ¶ 8. For example, in one prior art method, polymer glue may be required to bond the

vertically stacked wafers. *Id.* In another prior art method, copper may be used to bond the vertically stacked wafers. *Id.* One drawback to this second method is that a carrier wafer is required to transport thinly stacked wafers, and a polymer glue is used to affix the carrier wafer on the top wafer during the vertically stacked wafer processing. *Id.* According to Kim, there therefore existed a need "for a simpler but more efficient process of vertically stacking multiple wafers supporting different active IC devices on a single die with low cost and high via density with optimal metal bonding areas." *Id.*

Figure 1 of Kim is reproduced below:

FIG. 1

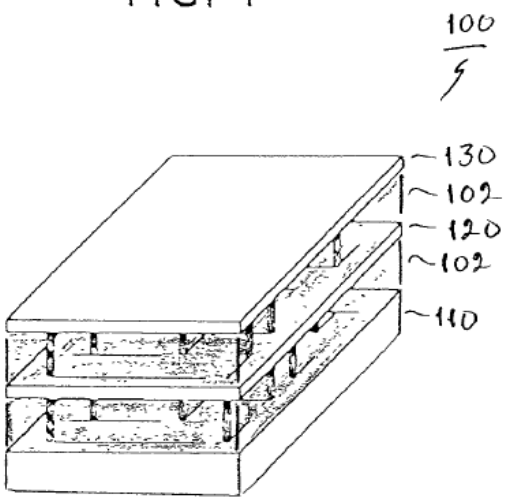


Figure 1 "illustrates an example three-dimensional (3-D) wafer-to-wafer vertical stack forming a single chip." Ex. 1008 ¶ 10. In Figure 1, 3-D vertical stack (chip) 100 may comprise any number of active device polysilicon (Si) wafers, such as wafers #1 (110), #2 (120), and #3 (130). *Id.* ¶ 20. Wafer #1 may include, for example, one or more microprocessors; wafer #2 may include one or more memory devices; and wafer #3 may include one or more radiofrequency (RF) or optical communication devices.

Id. Kim notes that the disclosed invention is "applicable for use with all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, MOS transistors, CMOS devices, MOSFETs, and new memory devices and communication devices." *Id.* ¶ 19.

Kim notes that, "[t]ypically, a dielectric layer 102 is used to bond the active device wafers 110, 120 and 130." Ex. 1008 ¶ 20. However, a "metal to metal" bond can also be used to stack wafers 110, 120, and 130 to form vertical stack 100. *Id.* ¶ 21. "This metal to metal bond method may serve not only as electrical connections to active IC devices on the vertically stacked wafers 110, 120, and 130 . . . but also [to] bond adjacent wafers 110, 120, and 130." *Id.*

Kim also discloses a "three-dimensional (3-D) wafer-to-wafer vertical stack," such as a "2-wafers vertical stack." Ex. 1008 ¶ 22, Fig. 2. According to Kim, this "vertical stack can effectively integrate diverse process technologies on a single wafer process, such as, for example, logic/memory stacking, processor stacking, optical interconnect, system-on-chip, and RF interconnect." *Id.*

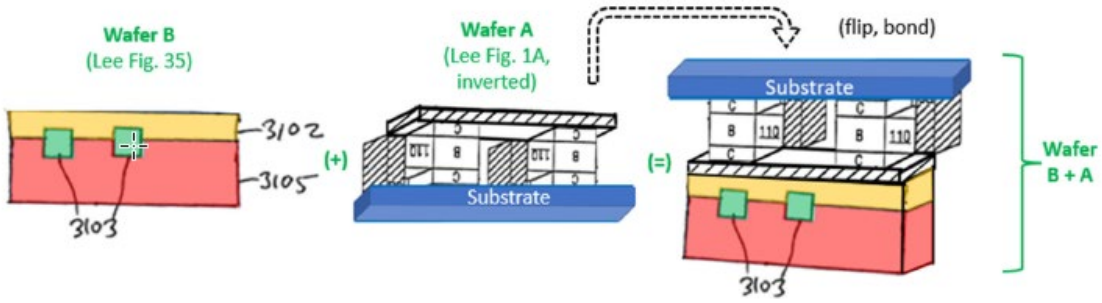
2. *Analysis – Claim 13*

With respect to the preamble and limitations 13[a], [b], and [d], Petitioner contends that Lee discloses these limitations for the same reasons discussed above with respect to obviousness based on Lee alone.[15] Pet. 50,

[15] As discussed above, we determine that Petitioner has not shown that Lee teaches or suggests limitation 13[b] under our construction for "stackable add-on layer." Petitioner's arguments regarding Lee and Kim rely on its arguments with respect to Lee alone for limitation 13[b] and do not

54. With respect to limitation 13[c], Petitioner contends that Kim discloses a method of forming a three-dimensional (3-D) wafer-to-wafer vertical stack that is applicable for use with "all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, . . . CMOS devices, MOSFETs, and new memory devices." *Id.* at 51 (citing Ex. 1008 ¶¶ 19–20). Petitioner further contends that Kim teaches that the vertical stack may comprise "any number" of wafers, including a wafer with one or more microprocessors and a wafer including one or more memory devices, and that dielectric layer 102 may be used to separate and bond the wafers. *Id.* (citing Ex. 1008 ¶¶ 20, 22, Fig. 1).

Petitioner's proposed combination is depicted below. Pet. 52.



The depiction above shows Petitioner's proposed method of combining the memory structure of Figures 1A–1B, 2, 7, or 25A of Lee and the substrate of Figure 35 of Lee. *Id*. In this combination, substrate 3105 of Lee having CMOS transistors (driver circuits 3103) and insulating layer 3102 is

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expressly address how the combination of Lee and Kim teaches this limitation. Pet. 50; *see also* C.F.R. § 104(b)(4) ("The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon."). Accordingly, for at least this reason, Petitioner has not shown that the combination of Lee and Kim teaches or suggests limitation 13[b].

identified as Wafer B. *Id.* Separately fabricated memory cells (e.g., from Lee's Figure 1A) are formed on their own substrate, identified as Wafer A. *Id.* Wafer A is then flipped and bonded to wafer B. *Id.*

Petitioner contends one of ordinary skill in the art would have been motivated to make such a combination for several reasons. First, Petitioner contends it is unclear in Lee how the bottom level 3104 of array 3101 is formed on insulating layer 3102. Pet. 51. Second, Petitioner contends the proposed combination would have amounted to using a known technique both to improve a similar known device in the same way and to address the same problem recognized by both Lee and Kim using prior art elements according to their established function. *Id.* at 53. Third, Petitioner contends a person of ordinary skill in the art would have understood that wafer-bonding Lee's bottom level 3104 to insulating layer 3102 would allow for more efficient quality control with less potential waste, as compared to monolithic deposition. *Id.* at 53–54

Patent Owner argues that Petitioner does not establish a motivation to combine Lee and Aspar and advances several reasons why one of ordinary skill in the art would not have combined the references in the manner proposed by Petitioner. PO Resp. 21–30.

For the reasons set forth below, we are not persuaded by Petitioner's rationales for combining Lee and Kim and credit several of Patent Owner's counterarguments.

a. *Bonding Level 3104 of Array 3101 on Insulating Layer 3102*

Petitioner contends that Lee discloses that each level 3104 is deposited on the underlying level of array 3101, but "does not clearly

describe how the bottom level 3104 of array 3101 is formed on insulating layer 3102." Pet. 51 (citing Ex. 1007 ¶¶ 107–113). Consequently, Petitioner contends that one of ordinary skill in the art would have looked to other art, such as Kim, for details about attaching bottom level 3104 to insulating layer 3102. *Id.* This is "especially so," according to Petitioner, where a person of ordinary skill in the art, "at the suggestion of Lee, was looking to separately form a two-dimensional array of memory devices and 'package [it] together' with Lee's substrate 3105 having driver circuits 3103 formed therein and insulating layer 3102 on top 'to form a non-monolithic memory device.'" *Id.* at 51–52 (citing Ex. 1003 ¶¶ 190–192; Ex. 1007 ¶ 107); *see also id.* at 52 (asserting that Kim contemplates bonding a wafer having CMOS devices, like Lee's substrate 3105, with a wafer having memory devices, like Lee's level 3104).

Lee discloses that in its monolithic array of memory devices "each level of the array [is] directly deposited on the layers of each underlying level of the array." Ex. 1007 ¶¶ 107, 111, 141 (noting that the pillar of Figure 9 may be formed by "blanket depositing a first I/O conductor 900 followed by the sequential blanket deposition of the film stack 902 (e.g., N+/P-/N+) of the desired pillar). Thus, Lee explains how each level of its array is formed, i.e., by direct deposition on the underlying layer. *See id.*; PO Resp. 21; Ex. 2029 ¶¶ 115–116.

Petitioner contends that deposition is just one potential implementation technique for the embodiment depicted in Figure 35 of Lee and that Lee contemplates using techniques with SOI technology, including "wafer bonding." Pet. Reply 6–7. Lee expressly states, however, that each level of its memory array is directly deposited on the underlying level of the

array. Ex. 1007 ¶¶ 107, 111, 141. Moreover, although Lee discusses SOI technology and wafer bonding, it does not suggest wafer bonding an array of memory devices to the substrate having a dielectric layer. *Id.* ¶¶ 208–209; Sur-reply 11.

In view of the foregoing, we are not persuaded by Petitioner's first rationale that one of ordinary skill in the art would have looked to art beyond Lee, including the wafer bonding art identified by Petitioner, in order to determine how to attach bottom level 3104 to insulating layer 3102 in Lee.

b. *Lee's Disclosures*

Petitioner contends that Lee was "looking to separately form a two-dimensional array of memory devices and 'package [it] together' with Lee's substrate 3105." Pet. 51–52 (citing Ex. 1003 ¶¶ 19–20; Ex. 1007 ¶ 111).

The relevant disclosure of Lee is

> One method of improving device density is to arrange the devices in a monolithic three dimensional array of charge storage devices comprising a plurality of device levels. The term "monolithic" means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

Ex. 1007 ¶ 107. We credit the testimony of Dr. Przybylski that one of ordinary skill in the art would read this disclosure, as well as the disclosures of Lee as a whole, as expressing a preference for monolithic memory structures, which provide specific benefits over stacks of two-dimensional arrays, including increased density and lower cost. Ex. 2029 ¶¶ 117–118; Ex. 1007 ¶¶ 106–107 (explaining that the disclosed monolithic arrays have "an increased density and lower cost" than prior art devices). Thus,

Petitioner's argument that one of ordinary skill in the art would have looked to the disclosures of Kim in view of Lee's desire to package two-dimensional arrays is not persuasive.

c. *KSR Rationales*

As explained in *KSR*, "if a technique has been used to improve one device, and a person of ordinary skill would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *KSR*, 550 U.S. at 417. *KSR* also notes that when there is a design need or market pressure to solve a problem, and one of ordinary skill in the art would have recognized that a known technique would address this problem, the use of the technique may be obvious. *KSR*, 550 U.S. at 420–421.

Petitioner asserts that a person of ordinary skill in the art would have recognized that using wafer-bonding to bond level 3104 to insulating layer 3102 would constitute "nothing more than using a known technique (Kim's wafer bonding) to improve a similar device (the structure in Lee's Figure 35) in the same way (logic/memory stacking using a wafer bonding process)." Pet. 53. Petitioner further asserts that using Kim's method of wafer bonding to bond level 3104 to insulating layer 3102 "would have amounted to applying a known technique (Kim's wafer bonding) to address the same known problem recognized by both Lee and Kim (fabricating 3D memory arrays above a substrate containing electrical devices) using prior art elements according to their established functions (Kim's wafer bonding and Lee's memory cell structures in Figures 1A–B, 2, 7, or 25A in Lee's Figure 35 structure)." *Id.* (citing Ex. 1003 ¶ 195; *Intel*, 61 F.4th at 1380; *KSR*, 550

U.S. at 417).

Petitioner's arguments are not persuasive. Both of Petitioner's *KSR*-based rationales depend on Kim's technique solving a known problem or improving Lee's device. Petitioner identifies no problem in Lee, however, that would motivate one of ordinary skill in the art to turn to wafer bonding. For example, there is no known problem identified by Petitioner in forming Lee's memory cells by sequential deposition over an existing substrate. Nor has Petitioner identified any particular benefit to the operation of Lee's device that would flow from the proposed modification. Pet. Reply 6 (failing to assert that the proposed combination would have "improved Lee"). This is especially true because Lee acknowledges that stacking of two-dimensional arrays of memory devices was known in the art, and Lee expresses a preference for high-density, low cost, monolithic arrays. Ex. 1007 ¶ 107 (contrasting monolithic arrays to stacked arrays).

Petitioner argues that "[i]mprovement in a categorical sense is not required: the Petition need only show Kim's/Aspar's techniques are 'suitable options.'" Pet. Reply 6 (citing *Intel*, 61 F.4th at 1381). For the reasons discussed below, however, Patent Owner persuasively demonstrates that using Kim's method of wafer stacking, as applied in the Petition, was not a suitable replacement for Lee's direct deposition method of constructing memory arrays. In particular, using Kim's method of wafer stacking would result in low yields and a high level of waste.

Given the lack of improvement to Lee's device from the use of Kim's stacking method, and given the there is no clear problem with Lee's monolithic, direct deposition method that would suggest the need for changing manufacturing methods, we are not persuaded that Petitioner's

KSR-based rationales would have motivated one of ordinary skill in the art to combine Lee and Kim. This conclusion is strengthened by the fact that, for the reasons set forth below, Patent Owner persuasively argues that Kim's method of wafer stacking would significantly reduce yields and increase waste while providing little to no benefit.

d. *Quality Control and Reduced Waste*

Petitioner contends that one of ordinary skill in the art would have used wafer bonding to add the pre-formed memory cells of Lee to a separately fabricated substrate because this would allow for quality control to be performed on the memory cells prior to stacking. Pet. 54. Petitioner asserts, "[i]f a quality control issue is detected, only that level 3104 would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously deposited stacks, etc.) would need to be discarded." *Id.* (citing Ex. 1003 ¶ 196). According to Petitioner, use of Kim's stacking method would therefore minimize waste resulting from defects detected during the quality control process. *Id.*

In support of its quality control benefit, Petitioner looks to Dr. Sechen's testimony and the disclosures of Fung. Pet. 53–54 (citing Ex. 1003 ¶ 196; Ex. 1016). Fung notes that "[d]ensity can be upgraded many fold by stacking chips or wafers" and "[s]ignificant speed improvement can also be expected because the interconnecting wires linking the chips are shortened substantially." *Id.* 1:15–19. There are, however, "several problems associated with stacking wafers." *Id.* at 1:33–38. "First, the yield loss is very large," with some potential yields for a two-wafer stack

as low as 49%. *Id.* at 1:34–39. Second, there are alignment problems with stacking wafers, requiring the feature sizes of the interconnects to be very large, thereby degrading "the density and performance of the [three-dimensional integrated circuits]." *Id.* at 1:39–47. Given these issues, Fung explains that "one must stack only good chips on top of good chips on a wafer to maintain a reasonable yield." *Id.* at 1:48–50. Stacking chips as opposed to wafers also allows the alignment tolerance to be "significantly superior" to "stacking wafers on top of one another." *Id*. at 1:52–55. As such, Fung reports that "stacking *chips* is definitely the preferred approach." *Id.* at 1:55–56 (emphasis added); *see also id.* at 5:6–12 (noting that wafer level testing is performed *before* dicing the SOI wafer into individual chips for stacking).

The Petition proposes to bond two wafers, Wafer A (substrate with electrical devices and a dielectric layer) and Wafer B (preformed memory cells on a substrate). Pet. 52. In other words, the Petition proposes to stack an entire wafer, as opposed to individual, previously-tested chips. Pet. 52; Tr. 15:3–14 ("For Kim, where you're forming complete devices prior to bonding, you would again be likely doing the whole wafer."). Given the disclosures of Fung, which are expressly relied upon in the Petition, we credit the testimony of Dr. Przybylski that Petitioner's proposed method of wafer stacking would actually result in lower yields, increased waste, and suffer from alignment problems. Ex. 2029 ¶¶ 125–127, 130 (explaining that even if there were errors in some dies, "fabs would not discard the entire wafer because that would waste an entire wafer's worth of dies"); PO Resp. 28–29. We also credit the testimony of Dr. Przybylski that Kim's method of wafer bonding would essentially discard an entire wafer for every

bonding step, as the substrate would need to be ground or etched off each time a layer is bonded in Kim's method. Ex. 2029 ¶¶ 130–131; PO Resp. 29 ("Kim's technique does not reduce waste, it multiplies it.").

Petitioner contends wafer thinning was optional in Kim. Pet. Reply 9. Patent Owner persuasively demonstrates, however, that thinning would not have been optional in Petitioner's proposed combination because the deposited memory cells require an additional conductive layer in order to operate, and the wafer would interfere with forming this conductive layer. Sur-reply 14 (citing Ex. 2029 ¶¶ 130–132); Tr. 33:1–5 (Petitioner's counsel agreeing that the blue substrate in the proposed combination would be "ground down"). Given that nearly an entire wafer would need to be ground away when using Kim's method to construct the memory device of Lee, Petitioner does not persuasively explain why Kim's stacking method would have reduced waste or have been preferable to Lee's direct deposition method. Ex. 2029 ¶¶ 130–134.

In view of the foregoing, we credit the testimony of Dr. Przybylski that one of ordinary skill in the art would not have used Kim's wafer bonding method to construct Lee's device due to the decreased yields and increased waste.

e. *Conclusion – Reason to Combine*

Petitioner identifies no persuasive, specific benefit to wafer bonding that would have led one of ordinary skill in the art to the combination of Lee and Kim. In contrast, Patent Owner and Dr. Przybylski persuasively explain why wafer bonding would have resulted in reduced yields and significantly increased waste. As such, Petitioner has not demonstrated by a

preponderance of the evidence that one of ordinary skill in the art would have combined Lee and Kim to arrive at the claimed invention.

3. *Analysis – Claims 14–17*

Claims 14–17 each require an "SOI pillar." Ex. 1001, 12:35–52. Petitioner contends that if Patent Owner argues that an "SOI pillar" "encompasses any pillar-shaped structure with insulating material below it," then Lee discloses or suggests the subject matter of claims 14–17. Pet. 31–41 (contentions based on Lee alone), 54 (relying on the same contentions for combination of Lee and Kim as presented for Lee alone).

Petitioner's arguments with respect to these claims do not remedy the deficiencies noted above with respect to independent claim 13. As such, Petitioner does not demonstrate by a preponderance of the evidence that the subject matter of claims 14–17 would have been obvious over Lee and Kim.

H. Claims 16 and 17 over Lee, Kim, and Endoh (Ground 1D)

Petitioner contends that, to the extent Patent Owner's apparent construction of "SOI pillar" is adopted, the subject matter of claims 16–17 would have been obvious over the combined disclosures of Lee, Kim, and Endoh. Pet. 55.

Petitioner's arguments with respect to this ground do not remedy the deficiencies noted above with respect to the reasons to combine Lee and Kim. Accordingly, Petitioner does not demonstrate by a preponderance of the evidence that claims 16 and 17 would have been obvious over the combined disclosures of Lee, Kim, and Endoh.

I. Claim 13 over Johnson

Petitioner contends the subject matter of claim 13 would have been

obvious over the disclosures of Johnson. Pet. 65–73.

1. *Johnson*

Johnson is titled "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication," and issued March 7, 2000. Ex. 1010, codes (45), (54).

Johnson discloses a "very high density field programmable memory" that includes an array that "is formed vertically above a substrate using several layers, each layer of which includes vertically fabricated memory cells." Ex. 1010, code (57). The fabrication process for the memory cells of Johnson is schematically illustrated in Figures 6(b)–6(g). *Id.* at 12:42–43. Figure 6(b) is reproduced below:

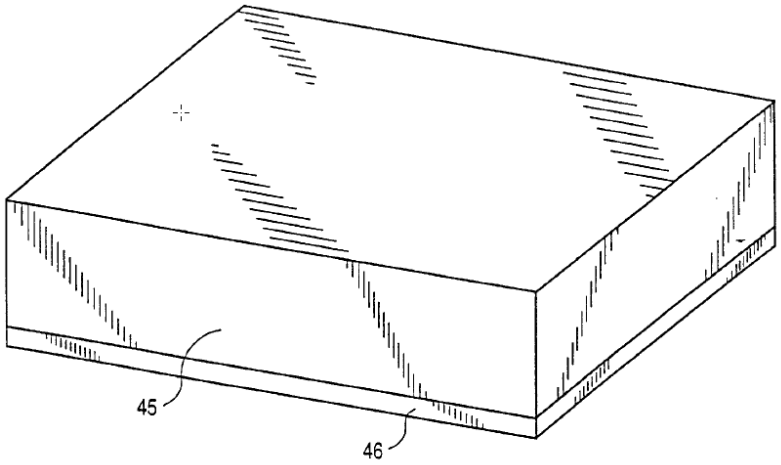

FIG. 6(b)

Figure 6(b) is a perspective view of a conductor layer and layer stack used in the fabrication of a memory cell. *Id.* at 4:38–39. Johnson explains that fabrication of the memory cell begins with a wafer that may have CMOS transistors for the peripheral circuitry fabricated in the monocrystalline

substrate. *Id.* at 13:26–29. An insulator is then deposited and, preferably, planarized (neither of these steps or structures is depicted in Figure 6(b)). *Id.* at 13:30–36. Then, first conductor layer 46 and layer stack 45 are sequentially deposited. *Id.* at 13:32–35. Next, a mask that defines the features of the conductor layer is applied and these features are etched into both pillar layer stack 45 and first conductor layer 46. *Id.* at 13:37–39. An insulator is then deposited on the wafer and planarized. *Id.* at 13:39–40.

Figure 6(c) is reproduced below:

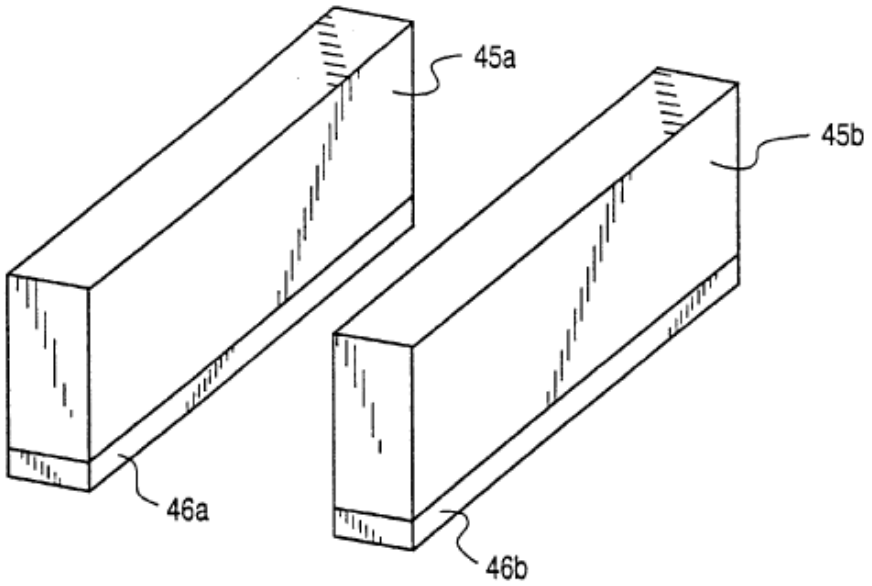

Figure 6(c) depicts the wafer after etching and depositing of the insulator layer on the wafer, and shows individual pillar layer strips, as opposed to isolated individual pillars. Ex. 1010, 13:41–45. Although not shown in Figure 6(c), Johnson explains that a dielectric fills the voids between the strips and pillars, adding support to the array. *Id.* at 13:51–53.

Johnson explains that this process is repeated multiple times to form multiple levels of conductors and vertically stacked pillars. Ex. 1010,

13:58–14:27. Figure 6(g) depicts a stack with three conductor layers. *Id.* at 14:21–22.

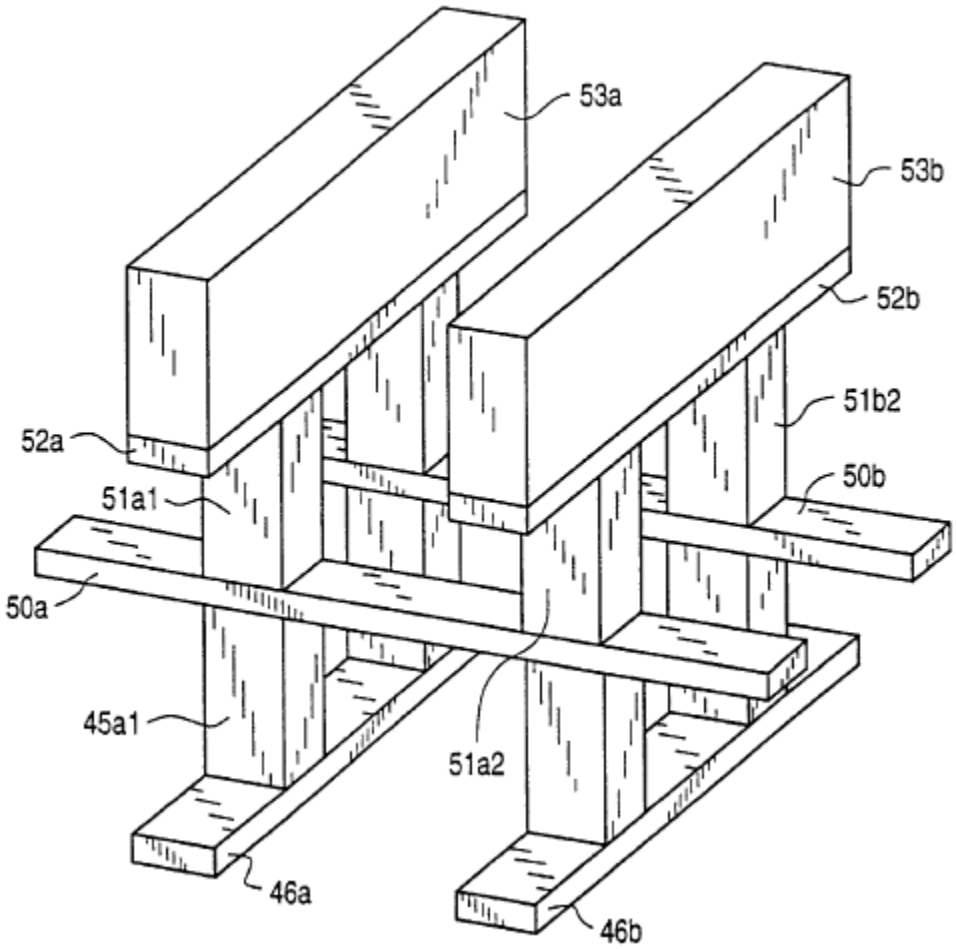

Figure 6(g) depicts the wafer after three levels of conductors and layer stacks have been deposited, but before all of the masking and etching steps have been applied to the upper most layer. *Id.* at 14:10–19.

Figure 8(b) of Johnson is reproduced below.

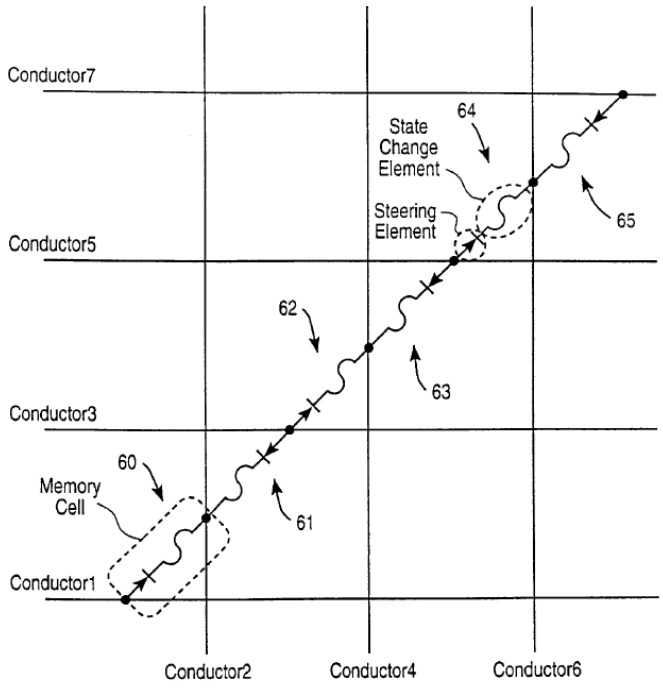

FIG. 8(b)

Figure 8(b) is a schematic of the vertically stacked cells of Johnson. Ex. 1010, 4:56. In Figure 8(b), there are six memory cells 60–65. Ex. 1010, 19:30–31. As shown in this schematic, memory cells are located between where conductor 3 crosses conductor 2, where conductor 4 crosses conductor 3, etc. *Id.* at 19:37–46. Johnson explains that each memory cell contains a steering element and a state change element. *Id.* at 19:40–42.

Johnson explains that the steering element is a semiconductor element that has a strongly asymmetric current-versus-voltage characteristic and conducts much more readily in one direction than in the other. Ex. 1010, 7:58–61.

> Some possible implementations of the steering element are (i) a PN junction diode, in amorphous, microcrystalline,

> polycrystalline or single crystal semiconductor (e.g., Si, Ge, SiGe, GaAs, InP, etc.); (ii) a metal-semiconductors Schottky diode; (iii) a junction field-effect transistor with gate connected to source (or to drain); (iv) a MOSFET with gate either floating, or connected to source or connected to drain; (v) a Zener diode, avalanche diode, or tunnel diode; (vi) a four-layer diode (SCR); (vii) a P-I-N diode in amorphous, microcrystalline, polycrystalline or single crystal semiconductor; and others that will be readily apparent to those skilled in the art.

Id. at 7:61–8:5. Johnson further explains that the state change element is where data is actually stored and may take many forms, including various fuses or anti-fuses. *Id.* at 8:32–45.

2. *Analysis – Claim 13*

Petitioner contends that Johnson discloses or suggest every limitation of claim 13, at least under Patent Owner's apparent construction of "stackable add-on layer." Pet. 65–73. With respect to element 13[a], Petitioner contends that Johnson discloses forming CMOS transistors, i.e., electrical devices, within a monocrystalline substrate and depositing a dielectric insulating layer over the substrate and electrical devices. *Id.* at 65–66 (citing Ex. 1010, 13:26–35; Ex. 1003 ¶ 226). With respect to element 13[b], Petitioner contends that Johnson discloses vertically oriented semiconductor memory cells and a "stackable add-on layer" under Patent Owner's apparent construction of this term, i.e., a monolithically and directly deposited layer created on an insulator. *Id.* at 66–68, 72. With respect to element 13[c], Petitioner contends that the "stackable add-on layer" of Johnson is bonded to an insulator deposited on a wafer. *Id.* at 69–72 (citing Ex. 1010, 12:8–12, 12:42–65, 13:26–35, Fig. 6(b)). With respect

to element 13[d], Petitioner contends that Johnson is directed to non-volatile memory cells that include at least one transistor. *Id.* at 72–73.

As discussed above, we adopt Petitioner's construction of "stackable add-on layer." Petitioner does not assert that Johnson discloses a "stackable add-on layer" under its construction of that term. Pet. 65. As such, Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious based on Johnson alone.

J. Claim 13 over Johnson and Kim or Johnson and Aspar

Petitioner contends the subject matter of claim 13 would have been obvious over both the combined disclosures of Johnson and Kim and the combined disclosures of Johnson and Aspar. Pet. 74–82.

With respect to the preamble and limitations 13[a], [b], and [d], Petitioner contends that Johnson discloses these limitations for the same reasons discussed above with respect to obviousness based on Johnson alone.[16] Pet. 74, 77, 82. With respect to limitation 13[c], Petitioner contends that Kim and Aspar each teach "the stackable add-on layer being bonded" under Petitioner's proposed claim construction and that a person of ordinary skill in the art would have combined that teaching with Johnson.

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[16] As discussed above, we determine that Petitioner has not shown that Johnson teaches or suggests limitation 13[b] under our construction for "stackable add-on layer." Petitioner does not expressly assert that Aspar or Kim teach or suggest limitation 13[b]. Pet. 74, 77; *see also* C.F.R. § 104(b)(4) ("The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon."). Accordingly, for at least this reason, Petitioner has not shown that the combination of Johnson and Kim or Aspar teaches or suggests limitation 13[b].

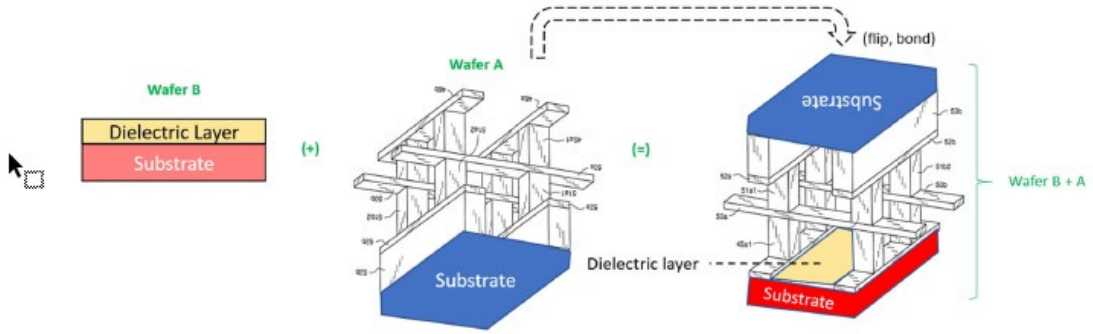
Id. at 74–82; *see, e.g., id.* at 75 ("A [person of ordinary skill in the art] would have been motivated to wafer bond Johnson's layer of memory cells ("stackable add-on layer") to its insulating layer ("dielectric layer") based on Kim's teachings."), *id.* at 78 ("A [person of ordinary skill in the art] would have been motivated to wafer bond a layer of semiconductor pillars as depicted in Johnson's Figures 6(a)–(b) ("stackable add-on layer") to the insulating layer above the substrate ("dielectric layer")" in view of Aspar).

Patent Owner disputes Petitioner's contentions concerning the teachings of Johnson and Petitioner's asserted reasons to modify Johnson and combine its teachings with Kim or Aspar. PO Resp. 57–74.

For the reasons discussed below, we are not persuaded by Petitioner's obviousness contention based on Johnson in combination with Kim or Aspar.

1. *Petitioner's Combination of Johnson and Kim*

Petitioner contends that one of ordinary skill in the art would have separately fabricated the memory cells of Johnson on their own substrate (Wafer A) and then Wafer A would be flipped and bonded to Wafer B having, for example, Johnson's "CMOS transistors" and insulating layer. Pet. 75. Petitioner illustrates this combination as follows:



In the proposed combination depicted above, Petitioner contends that, as in

Kim Figure 1, Johnson's layer of memory cells ("stackable add-on layer") would be wafer bonded to Johnson's insulating layer ("dielectric layer"). *Id.* (citing Ex. 1003 ¶ 248).

Petitioner contends one of ordinary skill in the art would have sought to combine Johnson and Kim because wafer-bonding Johnson's level of memory cells to its insulating layer "allows for more efficient quality control with less potential waste," as compared to monolithic deposition. Pet. 76 (citing Ex. 1003 ¶ 250). According to Petitioner, quality control could be performed on the memory cells (e.g., testing for shorts) and if a quality control issue is detected, then only that level would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited stacks, etc.) would need to be discarded. *Id.*

> Petitioner further contends that the proposed combination
>
> consists of nothing more than using a known technique (Kim's wafer bonding) to improve a similar known device (Johnson's structure) in the same way (logic/memory stacking using a wafer bonding process). *Id.* In addition the combination would have amounted to applying a known technique (Kim's wafer bonding) to address the same known problem recognized by both Johnson and Kim (fabricating 3D memory arrays above a substrate containing electrical devices) using prior art elements according to their established functions (Kim's wafer bonding and Johnson's structure).

Pet. 75–76.

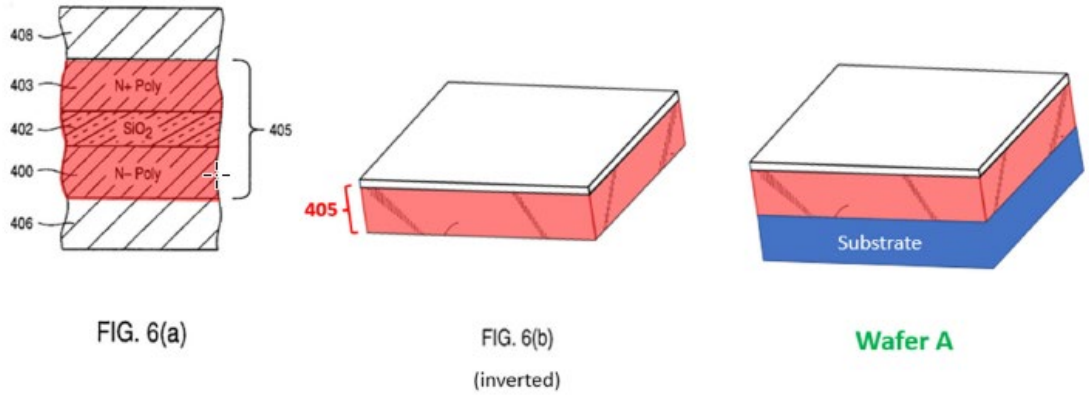
Petitioner's arguments regarding Johnson and Kim are similar to Petitioner's arguments regarding Lee and Kim in that Petitioner relies on Johnson or Lee for teaching limitations 13[pre]–13[b] and 13[d], and Petitioner relies on Kim to teach limitation 13[c], "the stackable add-on

layer being bonded to the dielectric layer." *Compare* Pet. 50–54 (addressing Lee and Kim for claim 13), *with* Pet. 74–77 (addressing Johnson and Kim for claim 13). Petitioner's reasons to combine Johnson and Kim are also substantively the same as those for combining Lee and Kim. *Id.* at 53–54, 75–77.

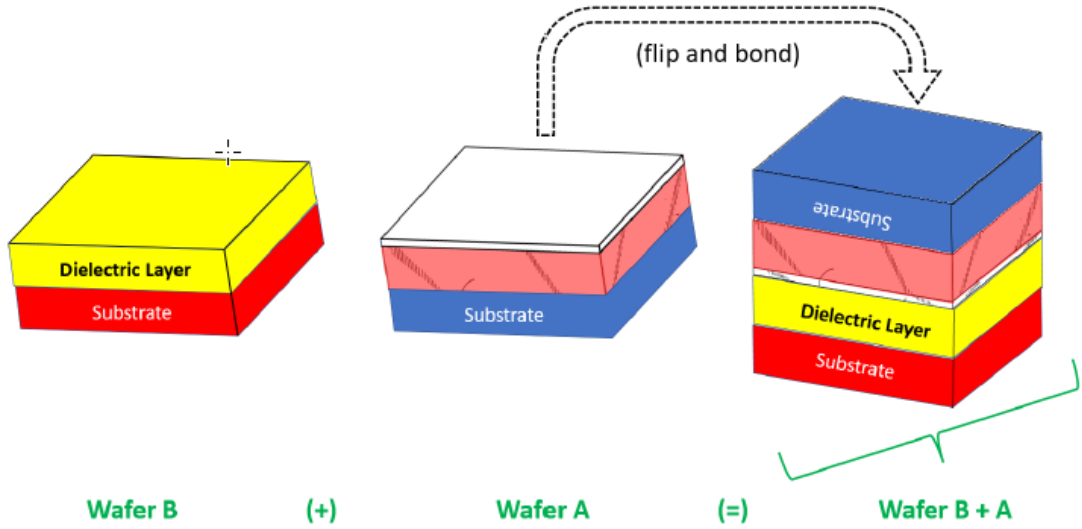
For the same reasons discussed above with respect Lee and Kim, we determine that Petitioner has not demonstrated that one of ordinary skill in the art would have sought to combine Johnson and Kim. In particular, Petitioner fails to identify any problem in Johnson that would have been solved by using Kim's manufacturing technique or any benefit to using Kim's method as opposed to Johnson's method of direct deposition. PO Resp. 65–69. We also find that, contrary to Petitioner's arguments, Patent Owner provides persuasive evidence, supported by the testimony of Dr. Przybylski which we credit, that a skilled artisan would not favorably consider modifying the device of Johnson (or Lee) to include Kim's three-dimensional (3-D) wafer-to-wafer vertical stack because the modification would lead to significantly reduced yields (potentially less than 50%) and increased waste (grinding away an entire wafer). PO Resp. 28–29, 66 (citing Ex. 1016, 1:32–52; Ex. 2029 ¶¶ 125–129, 193, 195).

2. *Petitioner's Combination of Johnson and Aspar*

Petitioner contends one of ordinary skill in the art would have deposited the doped stack depicted in Figures 6(a) and 6(b) of Johnson on a substrate, with a conductive layer then deposited over the doped stack. Pet. 79. Petitioner illustrates its contention as follows:



In Petitioner's proposed combination, Wafer A includes a substrate, Johnson's doped stacked structure, and a conductive layer. Pet. 78–79. Petitioner's Wafer A would be flipped upside down and bonded to Wafer B, which consists of Johnsons's substrate with "CMOS transistors" and insulating layer ("dielectric layer"). *Id.* This process is depicted below:



Petitioner contends that, when combined in the proposed fashion, the combination of Johnson and Aspar teaches or suggests every limitation of challenged claim 13. Pet. 74–82.

Petitioner's contention about how a person of ordinary skill in the art would have combined Johnson and Aspar is nearly identical to Petitioner's contention for the combination of Lee and Aspar. In both cases, Petitioner contends it would have been obvious to wafer bond an unpatterned, doped stacked structure to a separately fabricated substrate containing electric devices. *Compare* Pet. 59–60 (addressing Lee and Aspar), *with* Pet. 79–80 (addressing Johnson and Aspar). Petitioner's arguments as to why a person of ordinary skill in the art would have modified Johnson in view of Aspar to arrive at the subject matter of claim 13 are also nearly identical to those for combining Aspar with Johnson. *Compare* Pet. 60–63 (addressing Lee and Aspar), *with* Pet. 77–82 (addressing Johnson and Aspar); *see also* Pet. Reply 26–27 (identifying the overlapping arguments for Johnson-Kim/Aspar). For the reasons set forth above with respect to the combination of Lee and Aspar, we determine that Petitioner has not persuasively demonstrated that one of ordinary skill in the art would have combined Johnson and Aspar to arrive at the claimed invention with a reasonable expectation of success. Tr. 35:12–18 (Petitioner's counsel asserting that there is no "specific distinction" between the Johnson-Aspar or Johnson-Kim grounds that would make them more robust than the Lee-based grounds); *id.* at 66:5–12 (Petitioner's counsel asserting that the Lee-based grounds generally have "more disclosure to support the motivation to combine" as compared to the Johnson-based grounds). In particular, Petitioner fails to persuasively identify any problem with Johnson's direct deposition technique or any benefit achieved by modifying Johnson with Aspar's technique. In contrast, Patent Owner persuasively demonstrates that using Aspar's technique to form Johnson's doped stacked structure would use Aspar in a manner not

disclosed in the reference (which discloses a technique for making SOI wafers and SOI layer stacks having layers of SiO_2 and undoped silicon). PO Resp. 70–74. Patent Owner also persuasively demonstrates that Petitioner's proposed combination of Johnson and Aspar would lead to damage during an annealing step, and Petitioner's proposed combination could potentially lead to either a thin layer of the substrate remaining after the splitting step or removal of a portion of the doped stack structure. *Id*.

In view of the foregoing, Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious in view of Johnson and Aspar.

K. Obviousness of Claim 1 over Park and Kim

Petitioner contends the subject matter of claim 1 would have been obvious over the combined disclosures of Park and Kim. Pet. 82–91.

1. *Park*

Park is titled "Semiconductor Device Having Vertical Metal Oxide Semiconductors and a Method for Manufacturing the Same," and issued November 5, 1996. Ex. 1011, codes (45), (54).

Park notes that conventional memory devices "traditionally form a transistor in a lateral direction on a semiconductor substrate." Ex. 1011, 1:22–23. Park explains, however, that "it is substantially impossible to realize a semiconductor memory device of a continued higher capacity using the conventional planar layout." *Id.* at 1:31–33.

To allow for higher capacity memory devices, Park discloses the use of a silicon pillar that "is extended in a perpendicular (vertical) direction with respect to the semiconductor substrate" and surrounded by an insulating

film. Ex. 1011, 2:15–20. "A gate insulating film is interposed between the silicon pillar and a gate electrode surrounding the silicon pillar" and impurity regions "are formed in upper and lower portions of the silicon pillar to form the source and drain regions." *Id.* at 2:20–25.

Figure 9 of Park is reproduced below:

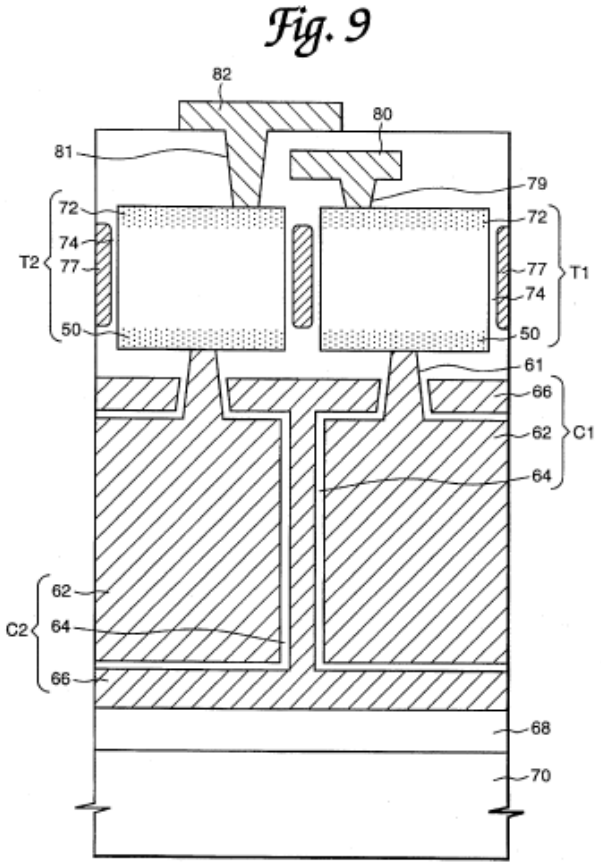


Figure 9 is a cross-sectional view of a DRAM cell manufactured according to the invention of Park. Ex. 1011, 5:33–35. In Figure 9, transistors T1 and T2 are formed with a vertical channel structure. *Id.* at 5:36–37. Capacitors C1 and C2 are formed under first and second transistors T1 and T2 and are comprised of storage electrodes 62 connected to source regions 50 of the first and second transistors T1 and T2. *Id.* at 5:39–41. Plate electrode 66 surrounds the entire surface of the storage electrode 62, with a dielectric film

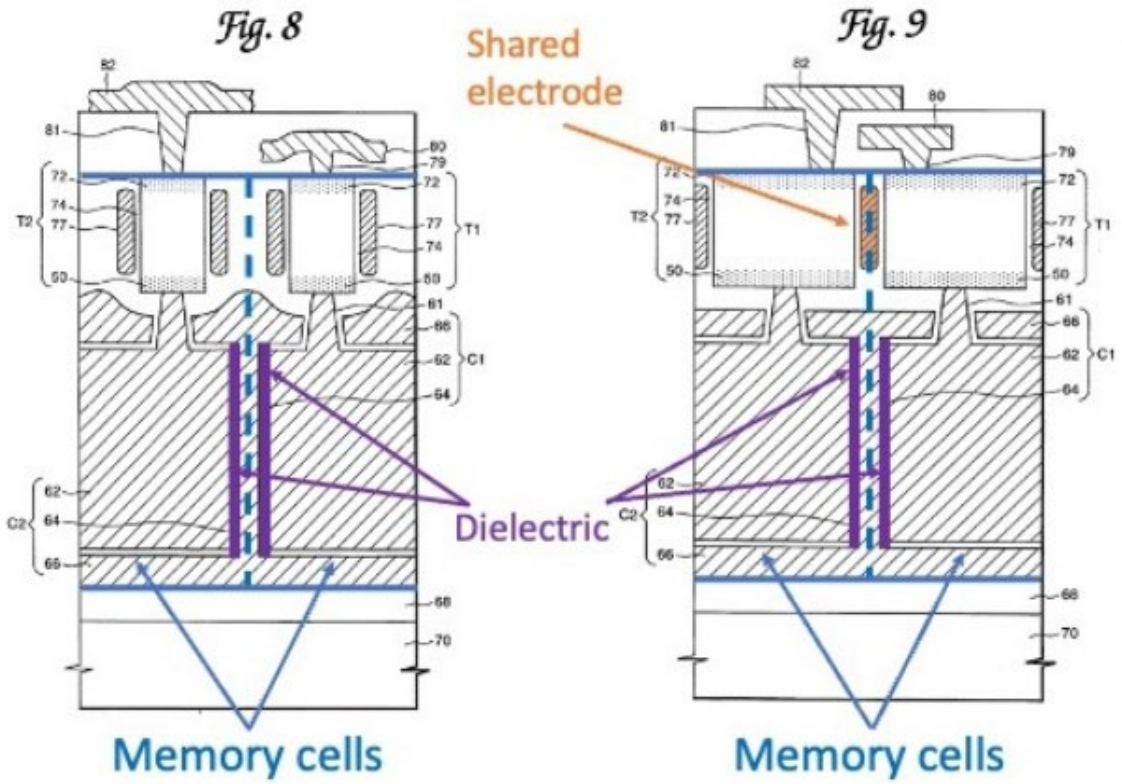
64 interposed therebetween. *Id.* at 5:41–43. First bitline 80 is connected to drain region 72 of first transistor T1, and second bitline 82 is connected to drain region 72 of second transistor T2. *Id.* at 5:43–46.

2. *Analysis*

Petitioner contends the use of Kim's wafer stack comprising logic devices in combination with Park's DRAM cells teaches or suggests every limitation of claim 1. Pet. 83–93. Petitioner further contends that one of ordinary skill in the art would have been motivated to vertically stack Park's DRAM memory cells using Kim's wafer stack method because this combination would "increase integration" and result in reduced interconnect RC delay and increased system performance. *Id.* at 83–84.

The parties' dispute regarding this combination centers around whether Park discloses "memory cells [] separated from each other by dielectric material." Pet. 88–89; PO Resp. 76–77. Petitioner contends that Park discloses that each of its vertically structured transistors are "surrounded [] with an insulating film" and that dielectric film 64 is also interposed between the plate and storage electrodes of capacitors C1 and C2. Pet. 88–89 (citing Ex. 1011, 2:16–21, 4:6–27, 5:21–22, 5:37–43, Fig. 3). Petitioner further contends that one of ordinary skill in the art "would have . . . understood the need to separate the memory cells with dielectric material for proper operation (e.g., avoiding shorts)." *Id.* at 89. According to Petitioner, "because both the transistors and capacitors of each memory cell are surrounded by insulating material," each of Park's DRAM memory cells are "separated from each other by dielectric material," as recited in claim 1. *Id.*

Patent Owner contends that the capacitors disclosed in Park are not isolated by the dielectric, as asserted by Petitioner. PO Resp. 76–77. Patent Owner provides an annotated version of Figures 8 and 9 of Park:



Figures 8 and 9 of Park are annotated above to identify the shared electrode and dielectric of Park. *Id.* at 77. Patent Owner contends that Figures 8 and 9 plainly show that the adjoining memory cells "share plate electrode 66," and thus the capacitors are not isolated by dielectric material. *Id.* at 76. According to Patent Owner, the transistors are only isolated by an insulating material between the gate electrodes 33 in the bitline direction (Figure 8), whereas they share gate electrode 77 (Fig. 9 in orange) in the wordline direction. *Id.* at 77 (citing Ex. 1011, 5:49–54).

Petitioner argues in response that dielectric material in fact separates the memory cells of Park from one another. Pet. Reply 28–29 (citing Pet. 88–89). Petitioner does not contest that the memory cells share a common electrode or that the dielectric material is part of the capacitor of each memory cell, but asserts that the '702 patent "does not support a complete-separation requirement." *Id.* at 29. Petitioner further contends that one of ordinary skill in the art would have understood the need to separate the memory cells with dielectric material for proper operation. Pet. 89.

On this record, Petitioner does not persuasively contest that the memory cells of Figure 9 of Park share plate electrode 66 and gate electrode 77 and that dielectric 64 forms an integral part of the capacitor of each memory cell, as asserted by Patent Owner. Sur-reply 29. Nor does Petitioner persuasively assert that the claim term "the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material" is broad enough to encompass memory cells that are electrically connected to each other through a common conductive plate electrode. *See* Ex. 1001, 10:55–57; Pet. Reply 28–29. In other words, the presence of some dielectric material between the memory cells, but not enough to electrically separate the cells from each other, does not meet the claim. As such, Petitioner does not persuasively demonstrate that Park and Kim teach or suggest "memory cells separated from each other by dielectric material," as recited in independent claim 1.

In view of the foregoing, Petitioner fails to demonstrate by a preponderance of the evidence that claim 1 would have been obvious over the combined disclosures of Park and Kim.

IV. MOTION TO EXCLUDE EVIDENCE

Patent Owner moves to exclude Exhibits 1040–1046, 1048–1050, and 1054, as well as corresponding paragraphs 22–25 of Dr. Schen's reply declaration (Ex. 1037). Mot. 1. According to Patent Owner, "[t]hese exhibits are either irrelevant because [Petitioner] never cites to them, or are cited to support [Petitioner's] improper new theory on reply." *Id.*

A. Exhibits 1040, 1042, 1046, and 1054

Patent Owner contends Exhibits 1040, 1042, 1046, and 1054 should be excluded because neither Patent Owner nor its expert cites or relies on these four exhibits. Mot. 4.

As Petitioner notes in its Opposition, however, the Board previously granted Petitioner's request to expunge Exhibits 1040, 1042, 1046, and 1054. Opp. 1 n.1. As these exhibits have been expunged, Patent Owner's request to exclude these exhibits is denied as moot.

B. Exhibits 1041, 1043–1045, 1048–1050, and Paragraphs 22–25 of Exhibit 1037

Petitioner contends Exhibits 1041, 1043–1045, 1048–1050, and Paragraphs 22–25 of Exhibit 1037 constitute new evidence and/or new argument that exceeds the proper scope of reply. Mot. 1. In particular, Patent Owner contends these exhibits were submitted to support Petitioner's new theory that "[p]rocess optimization [is a] motivation to combine" Lee and Kim or Aspar. *Id.* (quoting Pet. Reply 10).

As noted by Petitioner in its Opposition, a motion to exclude is not a vehicle to "address arguments or evidence that a party believes exceeds the proper scope of reply or sur-reply." Patent Trial and Appeal Board

Consolidated Trial Practice Guide November 2019, at 79. Rather, the proper vehicle to challenge whether arguments or evidence are beyond the proper scope of reply is a motion to strike. *Id.* at 80. A motion to strike, however, is not required for the Board to identify and disregard "new issues or belatedly presented evidence that exceeds the proper scope of reply." *Id.* This is because "the Board is capable of identifying new issues or belatedly presented evidence when weighing the evidence at the close of trial." *Id.* And, for the reasons discussed above, we determine that Petitioner's "process optimization" arguments are new and exceed the proper scope of reply.

In view of the foregoing, Patent Owner's motion to exclude Exhibits 1041, 1043–1045, 1048–1050, and Paragraphs 22–25 of Exhibit 1037 is denied.

V. CONCLUSION

For the foregoing reasons, we determine that Petitioner does not demonstrate by a preponderance of the evidence that claims 1 and 13–17 are unpatentable. Our conclusions are summarized in the following table.

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claims Not Shown Unpatentable
13–17	103(a)	Lee		13–17
16, 17	103(a)	Lee, Endoh		16, 17
13–17	103(a)	Lee, Kim		13–17
16, 17	103(a)	Lee, Kim, Endoh		16, 17
13–17	103(a)	Lee, Aspar		13–17
16, 17	103(a)	Lee, Aspar, Endoh		16, 17
13	103(a)	Johnson		13
13	103(a)	Johnson, Kim		13
13	103(a)	Johnson, Aspar		13

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claims Not Shown Unpatentable
1	103(a)	Park, Kim		1
Overall Outcome				1, 13–17

VI. ORDER

For the foregoing reasons, it is:

ORDERED that Petitioner does not demonstrate by a preponderance of the evidence that any challenged claim of the ’702 patent is unpatentable;

FURTHER ORDERED that Patent Owner’s Motion to Exclude is dismissed-in-part and denied-in-part; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Paper 40
Entered: December 26, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION
Petitioner,

v.

BESANG INC.,
Patent Owner.

IPR2023-00991
Patent 7,378,702 B2

Before JON B. TORNQUIST, KIMBERLY McGRAW, and ELIZABETH M. ROESEL, *Administrative Patent Judges.*

TORNQUIST, *Administrative Patent Judge*.

JUDGMENT[1]
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Denying-in-Part and Dismissing-in-Part
Patent Owner's Motion to Exclude
37 C.F.R. § 42.71

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[1] This Decision is entered to correct mistakes and omissions in the original Final Written Decision issued on December 11, 2024.

I. INTRODUCTION

Intel Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1 and 13–17 of U.S. Patent No. 7,378,702 B2 (Ex. 1001, "the '702 patent"). BeSang Inc. ("Patent Owner") filed a Preliminary Response to the Petition. Paper 6. We instituted review with respect to all grounds and claims set forth in the Petition. Paper 12 ("Institution Decision" or "Inst. Dec."). After institution, Patent Owner filed a Response (Paper 17, "PO Resp."), to which Petitioner filed a Reply (Paper 21, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 25, "Sur-reply").

Petitioner relies, *inter alia*, upon two declarations from Dr. Carl Sechen (Ex. 1003 (original declaration); Ex. 1037 (reply declaration)), and Patent Owner relies upon a declaration from Dr. Steven A. Przybylski (Ex. 2029).

Patent Owner filed a motion to exclude evidence (Paper 29, "Mot.") to which Petitioner filed an opposition (Paper 30, "Opp.").

An oral hearing was held on September 18, 2024, and a transcript of the hearing is included in the record (Paper 38, "Tr.").

For the reasons that follow, we conclude that Petitioner has not demonstrated that claims 1 and 13–17 of the '702 are unpatentable. We also dismiss-in-part and deny-in-part Patent Owner's Motion to Exclude.

II. BACKGROUND

A. Related Matters

The parties identify the following district court proceedings as related matters: *BeSang Inc. v. Micron Tech., Inc.*, No. 2:23-cv-00028 (E.D. Tex.)

and *BeSang Inc. v. Intel Corp.*, No. 3:23-cv-00113 (D. Or.). Pet. 94; Paper 4, 1. The parties also note that the '702 patent was challenged in IPR2023-00900. Pet. 93; Paper 4, 1.

B. Real Parties in Interest

Petitioner and Patent Owner identify themselves as the real parties in interest. Pet. 93; Paper 4, 1.

C. The '702 patent

The '702 patent is titled "Vertical Memory Device Structures" and issued May 27, 2008, from an application filed September 3, 2004, which is a continuation-in-part of an application filed June 21, 2004. Ex. 1001, codes (22), (45), (54), (63).

The '702 patent explains that "integrated circuits contain transistors that are primarily implemented on a single major surface of a substrate, such as a semiconductor wafer." Ex. 1001, 1:27–30. "These laterally oriented devices," however, "consume significant amounts of chip area." *Id.* at 1:30–31. The '702 patent explains that one method of reducing the lateral area consumed by the transistors was to reduce the lateral dimensions of the transistors and interconnects, but the equipment and technology needed to support the manufacture of such chips "becomes increasingly expensive with each new generation of smaller devices." *Id.* at 1:31–39. To address this problem, the '702 patent discloses the use of "a plurality of vertically oriented semiconductor memory devices, or cells," that "may be added to a separately fabricated substrate that includes electrical devices and/or interconnect lines." *Id.* at 1:40–50; *see id.* at code (57) ("Vertically oriented

semiconductor memory cells are added to a separately fabricated substrate that includes electrical devices and/or interconnect.”).

Figure 1 of the ’702 patent is reproduced below:

Fig. 1

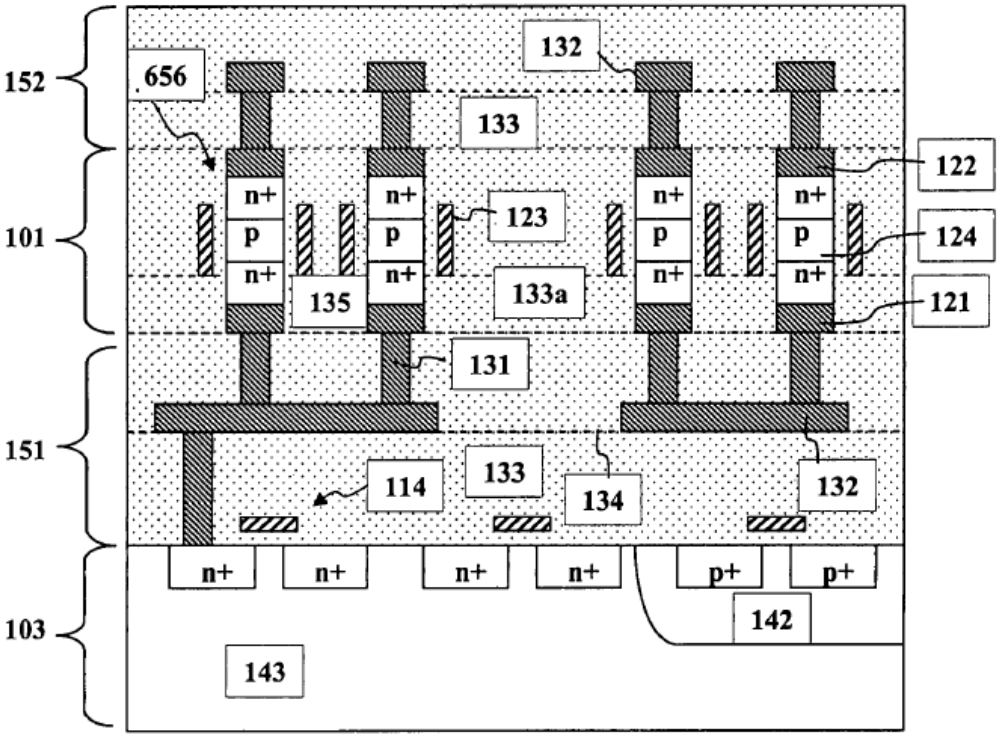


Figure 1 is a cross-sectional view of an embodiment that includes “a base semiconductor substrate and add-on vertical memory devices.” Ex. 1001, 2:13–15. As shown in Figure 1, vertical memory devices 656 are separated by isolation 135 and have floating structures in filled dielectric materials 133*a*. *Id.* at 5:18–21. These vertical memory devices are referred to in the ’702 patent as floating devices (FLD). *Id.* at 5:21–22. “Inter-layer dielectric (ILD) layers 133 are disposed above and below FLD layer 101.” *Id.* at

5:29–32. Interconnect lines 132 and vias 131 connect FLDs directly or indirectly within an FLD layer, or to another FLD layer, or to a base substrate. *Id.* at 5:32–36.

In the embodiment shown in Figure 1, base substrate 103 is bonded to lower dielectric layer 151. Ex. 1001, 5:37–38. Dashed line 134 denotes a border, or interface, between two ILD layers. *Id.* at 5:43–44. First ILD layer 151 has interconnections and vias, and base substrate 103 shares these interconnections and vias with first FLD layer 101. *Id.* at 5:44–47. The bottom of the FLD layer is connected to metal layer 121, which is also directly connected to vias 131 in ILD layer 151, thereby forming a preformed electrode and contact. *Id.* at 6:35–38. The top of the FLD layer may be connected to metal layer 122, which is also directly connected to vias 131 in ILD layer 152. *Id.* at 6:38–40. The '702 patent notes that multiple FLD layers can be stacked, thereby increasing the effective device density. *Id.* at 6:41–42; *see also id* at 5:38–41, 5:47–50 (disclosing a "second FLD layer" not shown in Figure 1).

According to the '702 patent, "[t]he plurality of vertically oriented semiconductor memory cells can be added to the separately fabricated substrate as a thin layer including several doped semiconductor regions which, subsequent to attachment, are etched to produce individual doped stack structures." Ex. 1001, code (57), 1:57–62. "Alternatively, the plurality of vertically oriented semiconductor memory cells may be completely fabricated prior to attachment" to the separately fabricated substrate. *Id.* at code (57), 1:67–2:3.

The '702 patent explains that the "FLDs may, but are not required to, have a pillar structure." Ex. 1001, 6:43. The FLD of the '702 patent also

"has a gate dielectric layer which may be implemented with process operations at temperatures below 650° C." *Id.* at 7:15–17, 7:20–22 ("Any suitable dielectric material could be used except films requiring processing at temperatures more than 650° C.").

D. Illustrative Claim

Petitioner challenges claims 1 and 13–17 of the '702 patent. Pet. 1. Claim 13, reproduced below, is illustrative of the challenged claims:

> 13. A semiconductor memory structure, comprising:
>
> [a] a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
>
> [b] a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
>
> [c] the stackable add-on layer being bonded to the dielectric layer; and
>
> [d] wherein the memory cells are nonvolatile memory cells having at least one transistor.

Ex. 1001, 12:24–34 (paragraph identifications [a]–[d] are added to align with the parties' arguments); Pet. vi (claims listing).

E. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1 and 13–17 of the '702 patent are unpatentable on the following grounds (Pet. 3):

Ground	Claim(s) Challenged	35 U.S.C. §[2]	Reference(s)/Basis
1A	13–17	103(a)	Lee[3]
1B	16, 17	103(a)	Lee, Endoh[4]
1C	13–17	103(a)	Lee, Kim[5]
1D	16, 17	103(a)	Lee, Kim, Endoh
1E	13–17	103(a)	Lee, Aspar[6]
1F	16, 17	103(a)	Lee, Aspar, Endoh
2A	13	103(a)	Johnson[7]
2B	13	103(a)	Johnson, Kim
2C	13	103(a)	Johnson, Aspar
3	1	103(a)	Park[8], Kim

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. The '702 patent issued May 27, 2008. Ex. 1001, code (45). Accordingly, we apply the pre-AIA version of § 103. *See* 35 U.S.C. § 100(i)(1)(B).

[3] US 2002/0028541 A1, published March 7, 2002. Ex. 1007 ("Lee").

[4] US 2002/0154556 A1, published October 24, 2002. Ex. 1012 ("Endoh").

[5] US 2003/0157748 A1, published August 21, 2003. Ex. 1008 ("Kim").

[6] Aspar, et. al., *The Generic Nature of the Smart-Cut® Process for Thin Film Transfer*, 30 J. Elec. Materials, 834–840 (2001). Ex. 1009 ("Aspar").

[7] US 6,034,882, issued March 7, 2000. Ex. 1010 ("Johnson").

[8] US 5,571,730, issued November 5, 1996. Ex. 1011 ("Park").

III. ANALYSIS

A. Legal Standard

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and "the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner contends that one of ordinary skill in the art would have had "a bachelor's degree in electrical engineering, computer engineering, materials science, or a related field, and at least three years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa." Pet. 9; Ex. 1003 ¶ 37.

Patent Owner contends that one of ordinary skill in the art "would have had a bachelor's degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device

structures, or the equivalent, with additional education substituting for experience and vice versa." PO Resp. 14 (citing Ex. 2029 ¶¶ 34–38).

The parties proposed definitions differ in that Petitioner would permit a degree in "materials science" and require three years, as opposed to two years, of relevant experience. *Compare* Pet. 9 *with* PO Resp. 14. On this record, we adopt Patent Owner's proposed definition, as it is more consistent with the prior art of record and the disclosures of the '702 patent. We note, however, that neither party contends that the outcome of this case depends on the slight differences in the proposed definitions of a person of ordinary skill in the art.

C. Claim Construction

In this proceeding, the claims of the '702 patent are construed "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)." 37 C.F.R. § 42.100(b). Under that standard, the words of a claim are generally given their "ordinary and customary meaning," which is the meaning the term would have had to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Petitioner provides proposed definitions for the terms "stackable add-on layer . . . the stackable add-on layer [is]/[being] bonded" and "SOI pillar." Pet. 10–16. In the Institution Decision, we provided preliminary constructions for both terms. Inst. Dec. 7–12. Patent Owner disagrees with our preliminary constructions, but contends construction of the disputed

terms is not necessary to confirm the patentability of the challenged claims. PO Resp. 15–16.

Upon review of the prior art and the parties' arguments, we determine that only the term "stackable add-on layer" requires construction.[9] *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.")).

"stackable add-on layer"

Claim 1 requires "a first stackable add-on layer" that "is bonded to a layer of the substrate." Ex. 1001, 10:52–53, 10:58–59. Claim 13 requires "a stackable add-on layer" "being bonded to the dielectric layer." *Id.* at 12:29–32. Petitioner contends that based on the plain language of the claim "a stackable add-on layer" "must be its own structure capable of being stacked and added onto the other recited structures." Pet. 10 (citing Ex. 1003 ¶ 71). Petitioner analogizes the claimed memory structure to a layer cake in which each layer is baked individually and then stacked on top of each other to form the final product. *Id.* at 10–11.

[9] Petitioner contends that "the stackable add-on layer [is]/[being] bonded" portion of the claim requires that the "stackable add-on layer" be "wafer bonded to the recited layer of the substrate." Pet. 12. In the Institution Decision, we declined to limit the claims to wafer bonding. Inst. Dec. 10–11 & 10 n.10. The parties now agree that this issue does not need to be addressed in order to resolve the dispute between the parties. PO Resp. 15; Pet. Reply 1.

Petitioner contends the intrinsic record supports this understanding. Pet. 11. According to Petitioner, the '702 patent describes a Silicon-on-Insulator ("SOI") layer as "a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer," and explains that such an SOI layer may be thought of as a "stackable add-on structure." *Id.* (quoting Ex. 1001, 4:48–57).

In the Institution Decision, we preliminarily construed "stackable add-on layer" to be "a layer that is formed separately from the substrate and then bonded to the substrate or a dielectric layer above the substrate." Inst. Dec. 9. We further noted that "[w]e do not understand a 'stackable add-on layer' to include memory cells that are formed by sequential deposition on or above a substrate or dielectric layer without being added to a separately formed substrate." *Id.*

Patent Owner "respectfully disagrees with the Board's preliminary constructions because they are incorrect," but does not propose its own construction or explain why the Board's construction is incorrect. PO Resp. 15. Patent Owner contends the Board may confirm the patentability of the challenged claims for reasons unrelated to the construction of this term. *Id.*

Neither party asserts that "stackable add-on layer" has an accepted meaning in the art. *See Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004) (stating that, absent an accepted meaning in the art, "we construe a claim term only as broadly as provided for by the patent itself"). Thus, we must attempt to discern the meaning of this term from the claim language itself and from the remainder of the intrinsic record. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir.

1996) ("It is well-settled that, in interpreting an asserted claim, the court should look first to the intrinsic evidence of record, *i.e.*, the patent itself, including the claims, the specification and, if in evidence, the prosecution history."). Upon review of the parties' arguments and the intrinsic record, we agree with Petitioner that the '702 patent does not support a construction of "stackable add-on layer" that encompasses memory cells formed by sequential deposition on a substrate without being formed and then added to a separately formed substrate. Pet. 11–12.

First, the plain language of the claim does not require merely a "layer" having a plurality of vertically oriented semiconductor memory cells, but rather "a stackable add-on layer" having a plurality of vertically oriented semiconductor memory cells; that plurality is bonded to the dielectric layer. Ex. 1001, 12:29–32. A construction that gives meaning to all words of the claim is preferred. *Merck & Co., Inc. v. Teva Pharm. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.").

Second, the written description of the '702 patent summarizes the invention by stating that "a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells" is formed separately from the substrate and then stacked on and bonded to the substrate. Ex. 1001, 1:47–50 ("Briefly, a plurality of vertically oriented semiconductor memory devices, or cells, may be ***added to a separately fabricated substrate*** that includes electrical devices and/or interconnect lines.") (emphasis added). The '702 patent discloses two ways of adding a memory cell layer. "The plurality of vertically oriented semiconductor memory cells [can be] added to the separately fabricated substrate as a thin layer including several doped

semiconductor regions which, subsequent to attachment, are etched to produce individual doped stack structures." *Id.* at code (57), 1:57–62. "Alternatively, the plurality of vertically oriented semiconductor memory cells may be completely fabricated prior to attachment" to the separately fabricated substrate. *Id.* at code (57), 1:67–2:3. In both of these methods, the memory cells are added as a completed layer to a separately fabricated substrate.

Generally supporting this understanding, the specification explains that a Silicon-on-Insulator ("SOI") layer refers to "a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate." Ex. 1001, 4:47–53. According to the '702 patent, "[i]n this context, the SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections." *Id.* at 4:53–57. Consistent with the summary of the invention discussed above, this description in the '702 patent suggests that a "stackable add-on layer" is a layer that is formed separately from the semiconductor substrate and then bonded to substrate that already contains devices and/or interconnections, i.e., a separately fabricated substrate. We further note that we are directed to no embodiment of the '702 patent wherein layers that are sequentially deposited on the substrate are identified as a "stackable add-on layer."

In view of the foregoing, we construe "stackable add-on layer" to mean "a layer formed separately from the substrate suitable to be bonded to

the dielectric layer positioned above the substrate." Our construction also provides that a "stackable add-on layer" should not be read to include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate.

D. Claims 13–17 over Lee (Ground 1A)

Petitioner contends the subject matter of claims 13–17 would have been obvious over the disclosures of Lee. Pet. 16–41.

1. *Lee*

Lee is titled "Dense Arrays and Charge Storage Devices, and Methods for Making Same" and published March 7, 2002. Ex. 1007, codes (43), (54).

Lee aims to reduce the cost of memory and logic devices by increasing device density. Ex. 1007 ¶ 106. Lee states it achieves these objectives by providing "a monolithic three dimensional array of charge storage devices comprising a plurality of device levels." *Id.* ¶ 107. In this context "monolithic" means that the layers of each level of the array are directly deposited on the layers of each underlying level of the array. *Id.* This is in contrast to two-dimensional arrays, which "may be formed separately and then packaged together to form a non-monolithic memory device." *Id.*

Figure 35 is reproduced below:

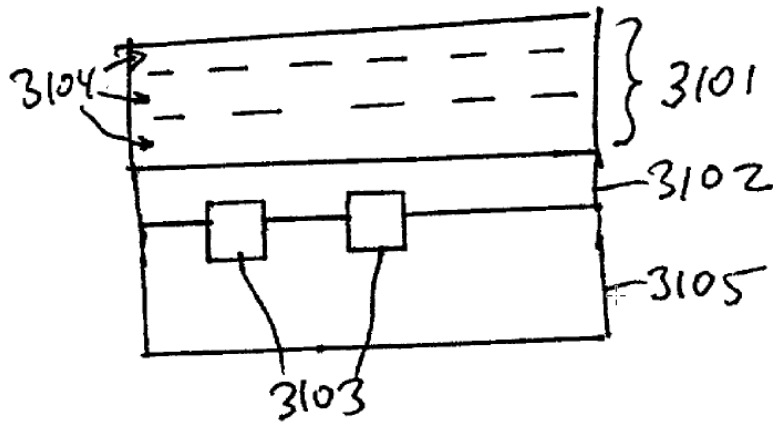


FIGURE 35

Figure 35 is a schematic of a three-dimensional array of devices. Ex. 1007 ¶ 60. In the device of Figure 35, driver circuits 3103 are disposed in monocrystalline substrate 3105 as CMOS or other transistors, and interlayer insulating layer 3102 is then disposed on monocrystalline substrate 3105. *Id.* ¶ 111. Charge storage logic or memory devices 3101 have a plurality of device levels 3104 that are preferably separated by interlayer insulating layers. *Id.*

Lee explains that "[t]he charge storage devices of the array may be any type of semiconductor devices which store charge, such as EPROMs or EEPROMs." Ex. 1007 ¶ 113. Such charge storage devices may be formed in various configurations, "such as a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM, a rail stack TFT EEPROM, and various other configurations." *Id.*

Figure 1A of Lee is reproduced below:

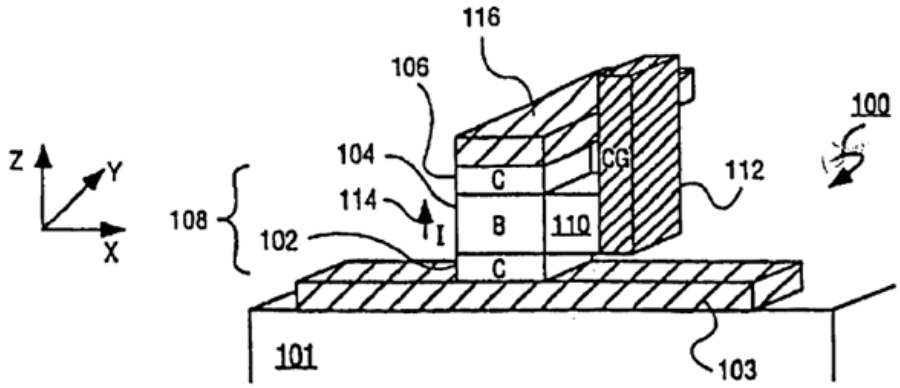


FIG. 1A

Figure 1A "is an illustration of a pillar memory." Ex. 1007 ¶ 38. In Figure 1, "[p]illar memory device 100 includes a first contact region 102 formed on a first input/output (I/O) 103 conductor formed on or above a plane (x-y) of a single crystal substate 101." *Id.* ¶ 122. Semiconductor body 104 is formed directly on first contact region 102 and a second contact region 106 is formed on the body 104. *Id.* "A second I/O region 116 is formed on the second contact region 106." *Id.* Lee explains that first contact region 102, body 104, and the second contact region 106 are each vertically aligned to form a pillar 108. *Id.* "Adjacent to and in contact with body 104 is a charge storage medium 110," with control gate 112 formed adjacent to and in direct contact with charge storage medium 110. *Id.*

Lee explains that:

> The programmed and unprogrammed state of the pillar memory device is determined by whether or not charge is stored in charge storage medium 110. The charge stored in the charge storage medium adds or subtracts from the voltage applied to the control gate, thereby altering the voltage required to form a conducting channel in body 104 to enable a current (e.g., read

current I_R) to flow between the first and second contact (source/drain) regions.

Ex. 1007 ¶ 123.

Figure 2 is reproduced below:

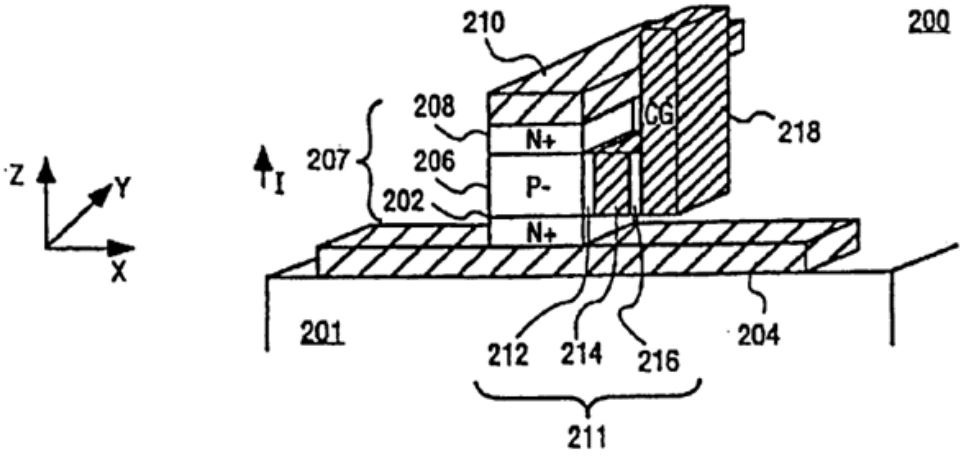


FIG. 2

Figure 2 is an illustration of a pillar memory. Ex. 1007 ¶ 41. In this embodiment, pillar 207 includes a first source/drain contact region 202 comprising a heavily doped N+ silicon film that is formed on a first input/output 204 (e.g. bit line) that is formed on or above a substrate 201. *Id.* ¶ 126. Body 206 is composed of a lightly doped P- type silicon film 206 that is formed on and in direct contact with N+ source/drain contact region 202. *Id.* Second drain region 208 is composed of a heavily doped N+ silicon film and is formed on and in direct contact with P type silicon film 206. *Id.* "A second conductive input/output (e.g. word line/bit line) 210 is formed on the second N+ source/drain region 208." *Id.* Charge storage medium 211 comprises a tunnel dielectric 212, floating gate 214, and control gate dielectric 216. *Id* ¶ 127. Control gate 218 is formed adjacent to, and in

direct contact with, control gate dielectric 216. *Id.* "Control gate 218 is formed of a conductor such as but not limited to doped silicon or a metal such as tungsten." *Id.*

Figure 9A is reproduced below:

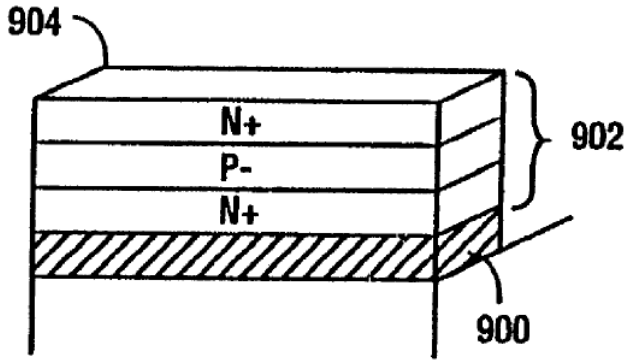


FIG. 9A

Figure 9A "illustrates a method of forming a pillar utilizing an intersection etch technique." Ex. 1007 ¶ 48. In Figure 9A, first I/O conductor 900 is blanket deposited, "followed by the sequential blanket deposition of the film stack 902 (e.g., N+/P-/N+) of the desired pillar." *Id.* ¶ 141. "The first I/O film 900 and the pillar film stack 902 are then etched to form a plurality of pillar strips 904 as shown in Fig. 9a." *Id.* Pillar strips 904 may then be etched to form individual pillars with associated I/O films. *Id.*

2. *Analysis—Claim 13*

Petitioner contends Lee discloses every limitation of independent claim 13. Pet. 16–31. With respect to the preamble and element 13[a], Petitioner contends that Figure 35 of Lee discloses a "semiconductor

memory structure" including substrate 3105 having driver circuits 3103 disposed therein. *Id.* at 17–19 (citing Ex. 1007 ¶¶ 110–111). Petitioner further contends that Figure 35 discloses interlayer insulating layer 3102 that is above substrate 3105 and driver circuits 3103. *Id.* at 20 (citing Ex. 1007 ¶ 111; Ex. 1003 ¶ 118). With respect to elements 13[b] and 13[c], Petitioner asserts that, if Patent Owner argues that a "stackable add-on layer" encompasses any type of layer that is directly or indirectly adhered to the "dielectric layer," then bottom-most level 3104 in Figure 35 teaches elements 13[b] and 13[c]. *Id.* at 20–27, 29–30. With respect to element 13[d], Petitioner contends that one of ordinary skill in the art would have understood that the memory cells depicted in Figures 1A–1B, 2, 7, and 25A, are all nonvolatile memory cells. *Id.* at 30–31 (citing Ex. 1007 ¶¶ 6, 113, 122, 125; Ex. 1003 ¶ 139).

As discussed above, we do not understand a "stackable add-on layer" to include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate. It is undisputed, and indeed it is Petitioner's assertion, that Lee's memory devices are formed by sequential deposition. Pet. 16, 29 n.11, 51 ("In Lee, each level 3104 is deposited on the underlying level of array 3101."). Therefore, Petitioner has not shown that Lee discloses every limitation of independent claim 13 under our claim construction. Thus, Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious in view of Lee.

3. *Analysis—Claims 14–17*

Claims 14–17 each depend, directly or indirectly, from claim 13. Petitioner's arguments with respect to these claims do not remedy the deficiencies noted above with respect to claim 13. Pet. 31–41. Accordingly, Petitioner does not demonstrate by a preponderance of the evidence that claims 14–17 would have been obvious over Lee.

E. Claims 16 and 17 over Lee and Endoh (Ground 1B)

Petitioner contends "Lee and Endoh teach claims 16 and 17's additional limitations under [Patent Owner's] apparent interpretation of 'SOI pillar.'" Pet. 41–42. Claims 16 and 17 depend from claim 13, and Petitioner's arguments with respect to these claims do not remedy the deficiencies noted above with respect to claim 13. Pet. 41–50. As such, Petitioner does not demonstrate by a preponderance of the evidence that claims 16 and 17 would have been obvious based on the combined disclosures of Lee and Endoh.

F. Claims 13–17 over Lee and Aspar (Ground 1E)

Petitioner contends the subject matter of claims 13–17 would have been obvious over the combined disclosures of Lee and Aspar. Pet. 55–63.

1. *Aspar*

Aspar is an article published in the Journal of Electronic Materials and is titled *The Generic Nature of the Smart-Cut® Process for Thin Film Transfer*. Ex. 1009. Aspar explains that the Smart-Cut process "is based on ion implantation and wafer bonding." *Id.* at 834. Aspar states that ion implantation induces formation of an in-depth weakened layer that leads to delamination of a thin film from a thick substrate. *Id.* Wafer bonding and

layer transfer then enable different materials to be associated to form multilayer substrates. *Id.* According to Aspar, the Smart-Cut process was "first developed to obtain silicon-on-insulator (SOI) materials," and is now "an industrial process which provides high quality materials in large quantities." *Id.*

Figure 1 of Aspar is reproduced below:

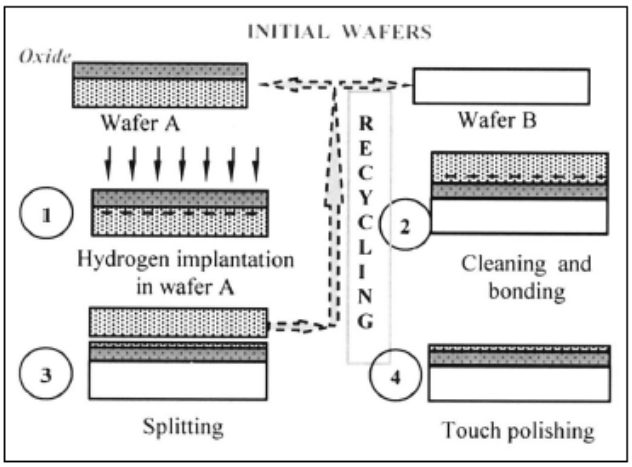


Figure 1 is a "[s]chematic description of the Smart-Cut® process, used to obtain SOI wafers." Ex. 1009, 835. The process for obtaining an SOI wafer begins with substrate A having an oxide layer on monocrystalline silicon. *Id.* at 834. Hydrogen implantation in substrate A induces formation of an in-depth weakened layer beneath the oxide layer. *Id.* Substrate A is then bonded to a support B by wafer bonding. *Id.* A splitting step is then performed, allowing the transfer of an oxide layer and a thin layer of monocrystalline silicon from substrate A onto support B. *Id.* A final treatment may then be performed to remove the rough surface left after splitting. *Id.* According to Aspar, this technique enabled the authors to obtain SOI wafers with "very good crystalline quality of the top silicon layer." *Id.* at 837.

Aspar notes that "[r]ealizing multiple SOI layers based on a layer transfer process can be achieved in many different ways: repeating a single layer transfer several times onto a same wafer, [or] transferring SOI layers stacks already formed onto a single substrate or a SOI wafer." Ex. 1009, 839. Thus, according to Aspar, "multiple SOI layers stacks can be easily performed thanks to Smart-Cut technology (Fig. 14)." *Id.*

Figure 14 of Aspar is reproduced below:

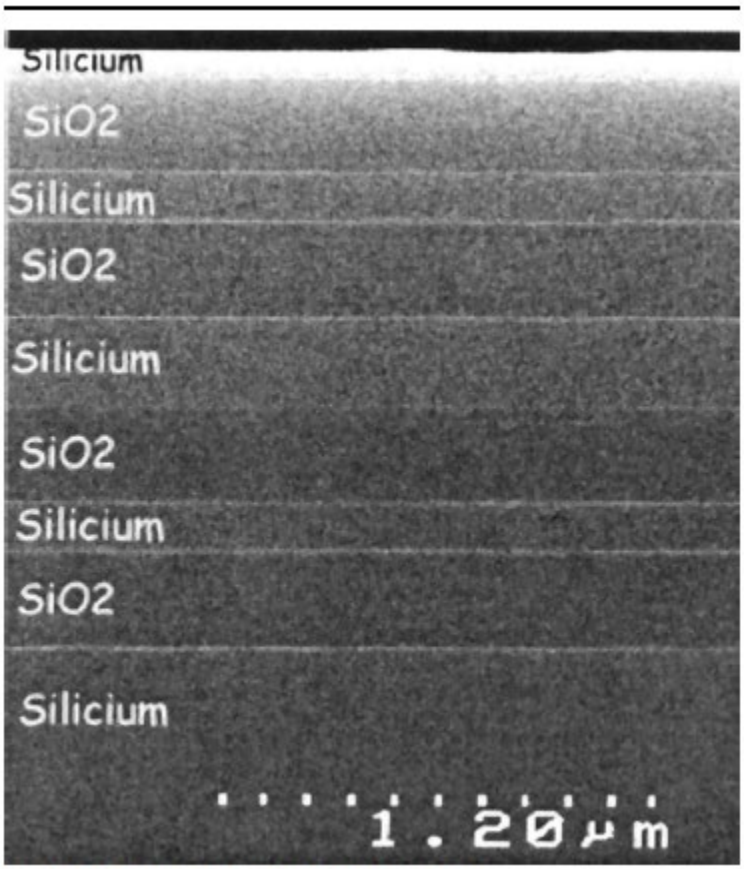
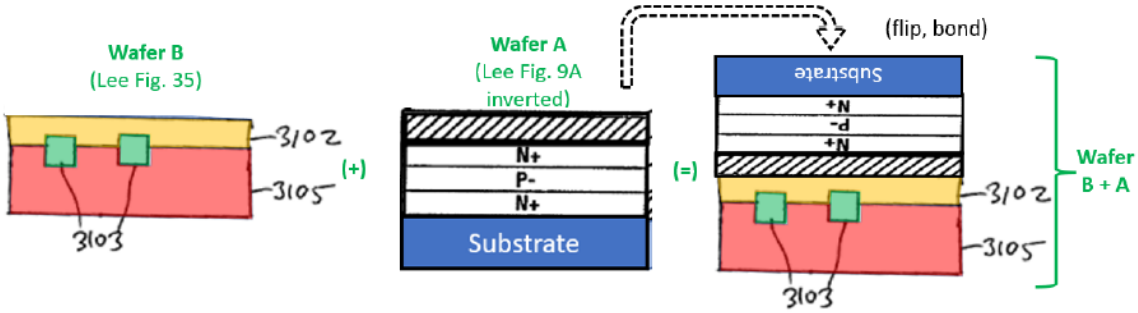


Fig 14. SEM view of multiple SOI layer stack.

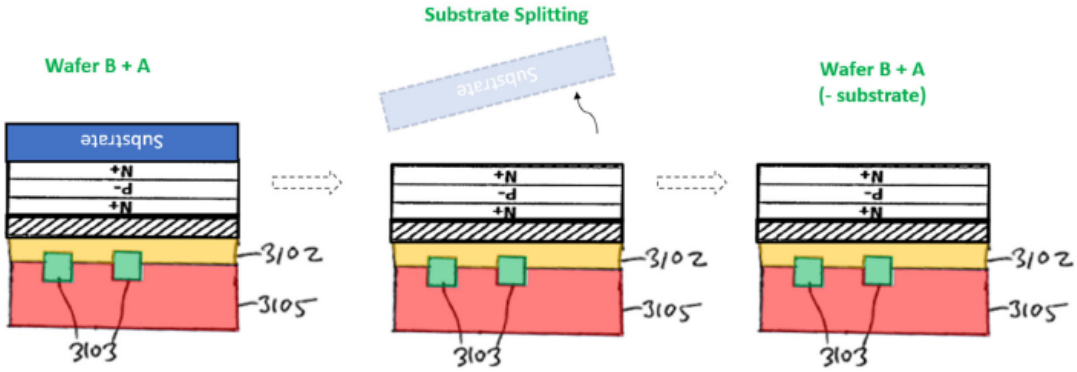
Figure 14 of Aspar depicts a "multiple SOI layer stack," consisting of alternating layers of silicium (silicon) and SiO_2. Ex. 1009, 838, Fig. 14.

2. *Analysis—Claim 13*

Petitioner contends that Lee and Aspar disclose the preamble and limitations 13[a], [b], and [d] for the same reasons discussed above with respect to the ground based on Lee alone.[10] Pet. 56, 63. With respect to limitation 13[c], Petitioner contends that Aspar discloses "transferring SOI layer stacks already formed onto a single substrate or a SOI wafer," and one of ordinary skill in the art would have sought to use this method to wafer bond bottom level 3104 ("stackable add-on layer") in Lee's Figure 35 to insulating layer 3102 ("dielectric layer"). *Id.* at 56–58. Petitioner provides the following illustrations of its proposed combination:



[10] As discussed above, we determine that Petitioner has not shown that Lee teaches or suggests limitation 13[b] under our construction for "stackable add-on layer." Petitioner's arguments regarding Lee and Aspar rely on its arguments with respect to Lee alone for limitation 13[b] and do not expressly address how the combination of Lee and Aspar teaches this limitation. Pet. 56; *see also* C.F.R. § 104(b)(4) ("The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon."). Accordingly, for at least this reason, Petitioner has not shown that the combination of Lee and Aspar teaches or suggests limitation 13[b].



Id. at 59–60. The illustrations above are Petitioner's depiction of the combination of Wafer B (a portion of Figure 35 of Lee) and Wafer A (Figure 9A of Lee (inverted and applied to a substrate)) to form a combined Wafer B + A. *Id.* at 59. Petitioner contends that, after bonding, the substrate (blue) would be removed and individual memory cells in level 3104 would be fabricated from the transferred thin layer in the same way they are fabricated in Lee. *Id.* at 60.

Petitioner contends one of ordinary skill in the art would have been motivated to make such a combination for several reasons. Pet. 60. First, Petitioner contends that it is unclear in Lee how the bottom level 3104 of array 3101 is formed on insulating layer 3102 and that one of ordinary skill in the art would have looked to other art to determine how to perform this step, including the wafer bonding technique described in Aspar. *Id.* at 56.

Second, Petitioner contends that the proposed combination would have amounted to using a known technique both to improve a similar known device in the same way and to address the same known problem recognized by both Lee and Aspar using prior art elements according to their established functions. *Id.* at 61.

Third, Petitioner contends that use of Aspar's process as compared to monolithic deposition would allow "for more efficient quality control at the layer formation stage." *Id.* (citing Ex. 1003 ¶ 213).

Patent Owner argues that Petitioner does not establish a motivation to combine Lee and Aspar and advances several reasons why one of ordinary skill in the art would not have combined the references in the manner proposed by Petitioner. PO Resp. 18–20, 44–52; PO Sur-reply 6–7.

For the reasons discussed below, we are not persuaded by Petitioner's rationales for combining Lee and Aspar and credit several of Patent Owner's counter-arguments. In addition, we determine that Petitioner's process optimization argument exceeds the proper scope of a reply.

a. *Bonding Level 3104 of Array 3101 on Insulating Layer 3102*

Petitioner contends that Lee does not clearly describe how bottom level 3104 of array 3101 is formed on insulating layer 3102 and that one of ordinary skill in the art would have looked to other art to determine how to perform this step. Pet. 56. We disagree with this premise. Lee discloses that in its monolithic array of memory devices "each level of the array [is] directly deposited on the layers of each underlying level of the array." Ex. 1007 ¶¶ 107, 111, 141 (noting that the pillar of Figure 9 may be formed by "blanked depositing a first I/O conductor 900 followed by the sequential blanket deposition of the film stack 902 (e.g., N+/P-/N+) of the desired pillar"). Thus, as asserted persuasively by Patent Owner, Lee explains how each level of its array is formed, i.e., by direct deposition on the underlying layer. *See id.*; PO Resp. 21, 44; Ex. 2029 ¶¶ 115–116, 142–143.

Petitioner contends that deposition is just one potential implementation technique for the embodiment depicted in Figure 35 of Lee, and Lee contemplates using techniques with SOI technology, including "wafer bonding." Pet. Reply 6–7. This argument is not persuasive. Lee expressly states that each level of its memory array is directly deposited on the underlying level of the array. Ex. 1007 ¶¶ 107, 111, 141. Moreover, although Lee discusses SOI technology and wafer bonding, it is with respect to other embodiments and with respect to forming the substrate on which the semiconductor active area is "deposited." *Id.* ¶¶ 208–209; Sur-reply 11.

In view of the foregoing, we are not persuaded by Petitioner's first rationale that one of ordinary skill in the art would have looked to art beyond Lee, including the wafer bonding art of Aspar, to determine how to attach or bond bottom level 3104 to insulating layer 3102 in Lee.

b. *Known Process to Solve a Known Problem*

As explained in *KSR*, "if a technique has been used to improve one device, and a person of ordinary skill would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *KSR*, 550 U.S. at 417. In addition, "if there is a known technique to address a known problem using prior art elements according to their established functions, then there may be a motivation to combine." *See Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023).

Petitioner contends that Aspar teaches realizing "multiple SOI layers based on a layer transfer process . . . [such as] transferring SOI layers stacks already formed onto a single substrate or SOI wafer. So multiple SOI layers

can be easily performed thanks to Smart-Cut technology." Pet. 60 (quoting Ex. 1009, 839). Petitioner also contends that Aspar's Smart-Cut process was known to have several advantages, including "transferring thin layers of very good thickness homogeneity and with a high crystalline quality." *Id*. at 60–61 (quoting Ex. 1003 ¶ 212; Ex. 1009, 834); Pet. Reply 6 (citing Ex. 1009, 834, 839; Ex. 1037 ¶ 13). Applying *KSR*, Petitioner contends that the combination of Lee and Aspar would have amounted to using a known technique (Aspar's Smart-Cut process) both "to improve a similar known device (the structure in Lee's Figure 35) in the same way (vertically stacking memory devices using SOI technology)" and "to address the same known problem recognized by both Lee and Aspar (fabricating 3D structures) using prior art elements according to their established functions (Aspar's Smart-Cut® process and Lee's Figure 35 memory device using the memory cell structures of Figure 1A-1B, 2, 7, or 25A)." Pet. at 61; Pet. Reply 5.

We agree with Patent Owner that Petitioner has not demonstrated that Aspar would improve Lee or would solve a problem in Lee and that Petitioner is proposing to use Aspar in a way that is not disclosed in the reference. PO Resp. 49–50 (citing Ex. 2029 ¶¶ 153–162); Tr. 57:24–58:12; Pet. 61; *KSR*, 550 U.S. at 417 (asking whether a technique "would improve similar devices in the same way"), 420 (asking whether there was a known problem in the art), 421 (asking whether one of ordinary skill in the art had reason to "pursue the known options"); *Intel*, 61 F.4th at 1381 (explaining that obviousness may be demonstrated by showing that there was a known problem in the art ("cache coherency in multiprocessor systems") and that a person of ordinary skill in the art would recognize that that the prior art

solution to this problem ("global segmented secondary cache") would improve the system of another prior art reference).

Petitioner does not persuasively show that there was any known problem in the art with respect to Lee or its monolithic method of constructing memory arrays. Nor does Petitioner provide persuasive argument or evidence that Aspar's wafer bonding would improve Lee's memory device.[11] For example, Petitioner states in a conclusory fashion that Aspar would address the known problem of "fabricating 3D structures," but does not explain what those problems were or why Lee fails to solve them. Pet. 61. Dr. Sechen's testimony merely parrots the Petition, providing no further analysis or explanation of what problem might exist in Lee when fabricating its 3D structures. Ex. 1003 ¶ 212. The Petition notes that Aspar transfers "thin layers of very good thickness homogeneity and with a high crystalline quality," but the Petition never asserts that Lee's direct deposition method fails to provide these same or similar qualities. Pet. 60–61.

Moreover, as noted by Patent Owner, Petitioner appears to use Aspar in a way that is not disclosed in the reference. PO Resp. 49–50. Aspar discloses transferring a layer of SiO_2 (insulator) and a thin layer of silicon having high crystalline quality. Ex. 1009, 834–835, 838 (Figs. 12 and 14). In Petitioner's proposed combination, "Wafer A" would consist of a substrate, an N+/P-/N+ (NPN) doped stacked structure (silicon layer), and a metal layer. Pet. 59. Petitioner points to no disclosure in Aspar, however, of

[11] As discussed below, Petitioner contends there were advantages to using Aspar's method, including reduced waste. Petitioner does not persuasively demonstrate, however, that Aspar would improve Lee's memory device in terms of performance or costs.

transferring a doped stacked structure (N+/P-/N+), eliminating the SiO_2 layer, or applying the splitting process to a wafer having a metal layer above the silicon layer. Pet. 60; Tr. 58:6–8, 68:4 ("The oxide isn't in our combination."); Ex. 2029 ¶ 155 ("Aspar's Figure 1 shows only an unpatterned oxide layer on Wafer A and a clean Wafer B prior to bonding and cleaving.").

Petitioner argues that "[i]mprovement in a categorical sense is not required: the Petition need only show Kim's/Aspar's techniques are 'suitable options.'" Pet. Reply 6 (citing *Intel*, 61 F.4th at 1381). Petitioner has not, however, shown that Aspar's technique was known to be a suitable option for making vertically stacked memory cells, as disclosed in Lee, in the relevant time period. As discussed above, Aspar's Smart-Cut technique is disclosed for making SOI wafers and multiple *SOI layer* stacks. Ex. 1009, 834–835, 838 (Figs. 12 and 14). Petitioner points to no disclosure in Aspar of creating the doped stacked structures posited in the Petition (Pet. 59–60), especially without the SiO_2 layer. Even if Petitioner had shown that Aspar's technique was a known alternative for making vertically stacked memory cells, simply showing that two options were known in the art is not sufficient to explain why one would be substituted for the other. *Virtek Vision Int'l ULC v. Assembly Guidance Sys.*, 97 4th 882, 887–888 (Fed. Cir. 2024).

Because the proposed combination has not been shown to improve Lee, solve a problem in Lee, or apply a known method in a known way, Petitioner has not persuasively demonstrated that its *KSR*-based arguments support the combination of Lee and Aspar. PO Resp. 51 ("In the complicated field of semiconductors, [Petitioner] needs to provide 'specific

evidence' justifying its significant departures and extensions from Aspar's actual disclosure.").

c. *Quality Control and Minimized Waste*

Petitioner contends one of ordinary skill would have sought to construct the memory of Lee using Aspar's Smart-Cut process because this would "minimize waste resulting from defects detected in quality control." Pet. 62. Specifically, Petitioner contends that Aspar's Smart-Cut process allows "quality control [to] be performed on the stack prior to bonding (e.g., thickness, uniformity, etc.)" and, "[i]f a quality control issue is detected, then only that stack would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited stacks, etc.) would need to be discarded." *Id.* at 61–62 (citing Ex. 1003 ¶ 213).

Petitioner's rationale is not persuasive. First, as noted by both parties, in the proposed combination of Lee and Aspar the unpatterned, doped stacked structure is transferred to the substrate. Pet. 60; PO Resp. 49; Pet. Reply 14. Petitioner does not persuasively demonstrate any need in the art for discarding doped stacked structures for quality control reasons, for example, because they do not have an appropriate thickness or uniformity. *See* Sur-reply 12–13 (noting that quality control in the art focused on testing of memory cells, not unpatterned layers); Ex. 2029 ¶ 145 (asserting that the memory cell errors a person of ordinary skill in the art would have wanted to test for "would necessarily arise after Smart-Cut's bonding and cleaving"). Indeed, as noted by Patent Owner, references provided by Petitioner indicate that the deposition process for doped silicon layers can be effectively quality

controlled and tested during fabrication. Ex. 1047, 308 (noting that the deposition rate and resistivity may be effectively controlled during the deposition process); PO Resp. 49; Sur-reply 12–13.

Second, Petitioner's counsel explained that if such a thickness or uniformity problem were detected, the layers could simply be scraped off and redeposited. Tr. 18:12–19:3. It is unclear, on this record, why such a scraping method could not likewise be used if the first NPN layer directly deposited on Lee's substrate were determined to have a defect in uniformity or thickness.

Third, to the extent quality control were a motivating factor for combining Lee and Aspar, we find persuasive Patent Owner's argument that the risk of damaging the NPN stack through the high temperature anneal step of Aspar would create increased waste and outweigh any perceived quality control benefits. Ex. 2039 ¶ 145; *see Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 795–96 (Fed. Cir. 2021) (noting that simultaneous advantages and disadvantages to a proposed combination must be analyzed to determine whether the disadvantages "outweighed any reason to combine").

d. *Process Optimization*

In its Reply, Petitioner contends that process optimization would have motivated the proposed combination of Lee and Aspar. Pet. Reply 10. Petitioner reasons that it was known in the art that in a linear process "a later processing step can cause perturbations of previous processing steps." *Id.* (citing Ex. 2039, 91:17–98:9). For example, heat used during subsequent processing steps could cause metal to deform possibly creating opens or shorts. *Id.* (citing Ex. 2039, 96:15–97:11). According to Petitioner,

fabricating devices on separate substrates, "each according to an optimized process," would avoid such issues and potentially increase yields. *Id.* (citing Ex. 1008 ¶ 22; Ex. 1044, 145–146; Ex. 1049, 6:42–56; Ex. 1050, 525; Ex. 1037 ¶¶ 22–23). Petitioner also contends that using the proposed combination one could provide "monocrystalline" silicon, which would improve Lee's device. *Id.*

"It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify 'with particularity' the 'evidence that supports the grounds for the challenge to each claim.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3)). Any marked departure from the grounds identified with particularity in the petition would impose "unfair surprise" on the patent owner and, consequently, violate both the Administrative Procedure Act and the *inter partes* review statute. *Arthrex Inc. v. Smith & Nephew, Inc.*, 935 F.3d 1319, 1328 (Fed. Cir. 2019). Strikingly absent from Petitioner's argument is any citation to the Petition that raises this specific motivation to combine Lee and Aspar. Pet. Reply 10. Thus, we agree with Patent Owner that process optimization is a new argument supporting the combination of Lee and Aspar that should have been raised in the Petition. Sur-reply 14–15. As such, we do not consider this new argument. *Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1383 (Fed. Cir. 2023) ("[T]he Board acts within its discretion when declining to consider a new theory of unpatentability raised by petitioner in reply.").

e. *Patent Owner's Counterarguments*

Petitioner does not meet its burden to show obviousness of combining Lee and Aspar for the reasons stated above. Our determination is reinforced by consideration of Patent Owner's counterarguments, as discussed below.

1. High Temperature Annealing

Patent Owner contends that Aspar's method includes a high temperature annealing step that would risk frying the underlying electronics of the substrate. PO Resp. 45–49. In support of this argument, Patent Owner turns to the disclosure of Aspar's Smart-Cut process in Wolf,[12] including Figure 11.24 reproduced below.

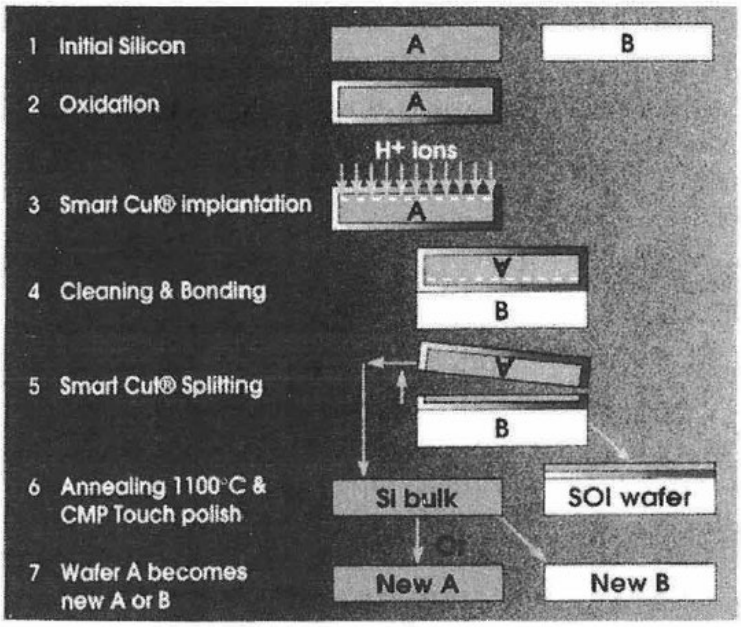


Fig. 11-24 Process flow for fabricating Smart-Cut® wafers.

Figure 11-24 of Wolf depicts the process flow for fabricating Smart-Cut wafers. Ex. 1015, 543. As shown in this figure, Wolf describes the same

[12] S. Wolf, *Silicon Processing for the VLSI Era*, *Volume 4 – Deep-Submicron Process Technology*, Lattice Press, 2002. Ex. 1015.

general process steps as Aspar, but expressly includes a 1100° C annealing step, that is used to "remove defects." *Id.* at 543–44. Patent Owner contends this annealing step would exceed the thermal budget of the underlying substrate and would damage the control circuitry (transistors) in the substrate and/or the doped stacked structure in Petitioner's proposed combination of Lee and Aspar. PO Resp. 47–48; Ex. 2029 ¶¶ 150–152.

Petitioner contends that the 1100° C annealing step is not required in Aspar, and it was known in the art to use much lower temperatures during the Smart-Cut process, as confirmed by the '702 patent's parent, the '941 patent.[13] Pet. Reply 12–13 (citing Ex. 1005, 8:60–62, 9:40–47, 10:19–21).

Patent Owner argues in its Sur-reply that Dr. Sechen relied upon Wolf's annealing step in his declaration and that Petitioner's attempts to rely on the '702 and '941 patents only confirms Petitioner is using "improper hindsight" to reconstruct the claimed invention. Sur-Reply 15–16 (citing Ex. 1003 ¶ 46). According to Patent Owner, it was the '702 patent that "explained how to build its architecture with low-temperature processing." *Id.* at 16.

For the following reasons, we find that Patent Owner has the better side of the high temperature annealing arguments.

Aspar discloses a process for obtaining SOI wafers that includes a "touch polishing" step after Wafers A and B are split, but Aspar does not expressly discuss an annealing step at 1100° C. Ex. 1009, 835. Both Dr. Przybylski and Dr. Sechen, however, present evidence that one of ordinary skill in the art would have understood that Aspar's process includes

[13] US 7,052,941 B2, issued May 30, 2006, "the '941 patent" (Ex. 1005).

a high-temperature annealing step, which was often performed at up to 1100° C. Ex. 1003 ¶¶ 46, 80–81; Ex. 2029 ¶ 148. For example, in his declaration Dr. Sechen indicates that the Smart-Cut method is "shown" in Figure 11-24 of Wolf, which includes an 1100° C annealing step for both Wafers A and B (containing the SOI layer). Ex. 1003 ¶ 46 (asserting that "[t]he Smart-Cut® method (shown below) starts by oxidization and ion-implantation of wafer A."); Ex. 1015, 543, Fig. 11-24; Ex. 2039, 118:10–119:2 (Dr. Sechen testifying that Wolf Figure 11-24 is describing the same process he referenced in Aspar—"This figure is entirely consistent, if not outright the same as Aspar's"). Likewise, Dr. Sechen points to Srikrishnan[14] as disclosing the Smart-Cut process, and Srikrishnan discloses applying a high temperature (approximately 1000° C) annealing step during the Smart-Cut process. Ex. 1003 ¶¶ 80–81; Ex. 1023, 5:16–50 ("Then, preferably, the support substrate 530 with the thin silicon layer 510 (device layer) still bonded to it is annealed at a high temperature (approximately 1000° C) for about 30 minutes to 8 hours to promote a stronger bonding.").

Petitioner contends Wolf is not part of its combination and the '941 patent, incorporated by reference in the '702 patent, "discloses a Smart-Cut process without any post-splitting anneal." Pet. Reply 12–13 (citing Ex. 1005, 8:60–62, 9:40–47, 10:19–21). This is so, according to Petitioner, because the substrate will not withstand temperatures over 650° C. *Id.* at 13. The '941 patent, however, is part of the priority chain of the '702 patent and

[14] US 5,882,987, issued March 16, 1999. Ex. 1023.

Petitioner has not demonstrated that the disclosures of the '941 patent are prior art with respect to the '702 patent.

Given the disclosures of Wolf and Srikrishnan and the testimony of Dr. Sechen cited above, we credit the testimony of Dr. Przybylski that, in the relevant time period, one of ordinary skill in the art would have understood the Smart-Cut process to include a high-temperature annealing step that would potentially damage transistors or the NPN stack in Petitioner's proposed combination. Ex. 2029 ¶¶ 148–152. As such, Petitioner has not demonstrated by a preponderance of the evidence that one of ordinary skill in the art would have combined Lee and Aspar to arrive at the claimed invention with a reasonable expectation of success.[15]

2. Remaining Thin Layer

Patent Owner contends that the Smart-Cut process "indisputedly left a thin film remaining" after the splitting process that would obstruct Lee's upper metal contact, and which Petitioner never explains how to avoid. PO Resp. 51. In the reply brief, Petitioner contends that, in the proposed combination of Aspar and Lee, the remaining silicon layer identified by Patent Owner is the doped stacked structure of Lee. Pet. Reply 14.

Even taking into account Petitioner's reply contention, the proposed combination remains poorly defined and tainted by hindsight bias. In Aspar,

[15] Even if it were known in the art that Aspar's wafer bonding method could be used at 650° C or less, our conclusion regarding the combination of Lee and Aspar would remain the same. The evidence that Aspar's method was known to use a 1000° or 1100° C annealing step merely serves to reinforce our determination that Petitioner has not met its burden to show obviousness based on Lee and Aspar.

hydrogen is implanted through the SiO_2 layer and into the underlying monocrystalline silicon of Wafer A. Ex. 1009, 834. Then, after Wafers A and B are bonded, a splitting step takes place that gives rise to the transfer of the SiO_2 layer and a thin layer of silicon from Wafer A to Wafer B. *Id.* Petitioner's proposed combination, however, does not use a monocrystalline silicon wafer with a SiO_2 layer, and Petitioner does not explain where hydrogen implantation would take place in the proposed sequence of process steps (Pet. 59–60) or where the resulting "weakened layer" (Ex. 1009, 834) would be in its proposed combination. Petitioner also does not explain how the substrate (blue) could be removed during the splitting process without either leaving a small portion of substrate on the upper surface, or removing a portion of the N+ layer that is in contact with the substrate.

In our view, Petitioner's proposed combination of Lee and Aspar appears to have been guided by hindsight reconstruction rather than the knowledge and skill of the ordinarily skilled artisan. Petitioner's proposed sequence of process steps (Pet. 59–60) is insufficiently supported by the references, which do not teach or suggest inverting an NPN stack with a conductive layer (Petitioner's Wafer A) and flip-bonding it a substrate having control circuitry and a conductive layer (Petitioner's Wafer B), with the conductive layer being bonded to the insulating layer. Aspar discloses the Smart-Cut process for making SOI wafers, not transferring NPN stacks with conductive layers to substrates with control circuitry and an insulating layer.

The poorly defined nature of the combination and Petitioner's apparent reliance on hindsight reconstruction reinforces our determination that Petitioner fails to show that it would have been obvious to combine Lee

and Aspar. PO Resp. 51 (asserting that Petitioner provides only a "vague idea" of how Lee and Aspar would be combined).

f. *Conclusion – Reason to Combine and Reasonable Expectation of Success*

For the reasons discussed above, Petitioner does not persuasively demonstrate that one of ordinary skill in the art would have sought to combine Lee and Aspar to arrive at the claimed invention. Nor does Petitioner demonstrate that one of ordinary skill in the art would have had a reasonable expectation of success in so doing, as Aspar's high temperature anneal step would damage the device. As such, Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious over Lee and Aspar.

3. *Analysis – Claims 14–17*

Claims 14–17 each require an "SOI pillar." Ex. 1001, 12:35–52. Petitioner contends that Aspar's Smart-Cut process is SOI technology and "the doped stack of the stackable add-on layer bonded to Wafer B is used to form pillars ('SOI pillars') for the memory cell structures of Lee's Figure 1A–1B, 2, 7, or 25A." Pet. 63 (citing Ex. 2003 ¶ 217; Ex. 1009, 834, 837).

Claims 14–17 depend from claim 13, however, and Petitioner's arguments with respect to these claims do not remedy the deficiencies noted above with respect to independent claim 13. As such, Petitioner does not demonstrate by a preponderance of the evidence that the subject matter of claims 14–17 would have been obvious over Lee and Aspar.

G. Claims 16 and 17 over Lee, Aspar, and Endoh (Ground 1F)

Petitioner contends that "[u]nder the proper constructions of 'stackable add-on layer being bonded' and 'SOI pillar,' the subject matter of claims 16–17 would have been obvious over Lee, Aspar, and Endoh." Pet. 64. For this combination, Petitioner contends the motivation to combine and reasonable expectation of success discussions related to Lee and Aspar and Lee and Endoh "apply equally to this ground." *Id.* Because Petitioner's arguments with respect to the combination of Lee, Aspar, and Endoh specifically rely on its arguments related to the Lee and Aspar combination discussed above, and do not remedy the deficiencies noted above with respect to this combination, Petitioner does not demonstrate by a preponderance of the evidence that claims 16 and 17 would have been obvious over the combined disclosures of Lee, Aspar, and Endoh.

H. Claims 13–17 over Lee and Kim (Ground 1C)

Petitioner contends that claims 13–17 would have been obvious over the combined disclosures of Lee and Kim. Pet. 50–54.

1. *Kim*

Kim discloses a "process of vertically stacking multiple wafers supporting different active IC devices on a single die with low cost and high via density with optimum metal bonding areas." Ex. 1008 ¶ 1. Kim notes that as integrated circuit (IC) technology progresses, there is a desire for a "system on a chip" in which the functionality of all the IC devices of the system are packaged together without a conventional printed circuit board. *Id.* ¶ 4. "In practice, however, it is very difficult to implement a truly high-performance 'system on a chip' because of vastly different fabrication

processes and different manufacturing yields for the logic and memory circuits." *Id.*

Kim explains that one known method of vertically stacking wafers was three-dimensional (3D) wafer-to-wafer vertical stack technology, in which multiple layers of active IC devices, such as processors, programmable devices and memory devices, are vertically stacked inside a single chip. Ex. 1008 ¶ 7. A major challenge to such methods "is the bonding between wafers and between die in a single chip." *Id.* ¶ 8. For example, in one prior art method, polymer glue may be required to bond the vertically stacked wafers. *Id.* In another prior art method, copper may be used to bond the vertically stacked wafers. *Id.* One drawback to this second method is that a carrier wafer is required to transport thinly stacked wafers, and a polymer glue is used to affix the carrier wafer on the top wafer during the vertically stacked wafer processing. *Id.* According to Kim, there therefore existed a need "for a simpler but more efficient process of vertically stacking multiple wafers supporting different active IC devices on a single die with low cost and high via density with optimal metal bonding areas." *Id.*

Figure 1 of Kim is reproduced below:

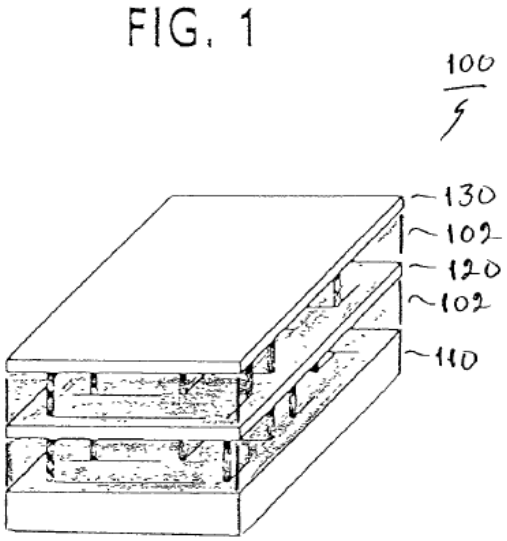


Figure 1 "illustrates an example three-dimensional (3-D) wafer-to-wafer vertical stack forming a single chip." Ex. 1008 ¶ 10. In Figure 1, 3-D vertical stack (chip) 100 may comprise any number of active device polysilicon (Si) wafers, such as wafers #1 (110), #2 (120), and #3 (130). *Id.* ¶ 20. Wafer #1 may include, for example, one or more microprocessors; wafer #2 may include one or more memory devices; and wafer #3 may include one or more radiofrequency (RF) or optical communication devices. *Id.* Kim notes that the disclosed invention is "applicable for use with all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, MOS transistors, CMOS devices, MOSFETs, and new memory devices and communication devices." *Id.* ¶ 19.

Kim notes that, "[t]ypically, a dielectric layer 102 is used to bond the active device wafers 110, 120 and 130." Ex. 1008 ¶ 20. However, a "metal to metal" bond can also be used to stack wafers 110, 120, and 130 to form vertical stack 100. *Id.* ¶ 21. "This metal to metal bond method may serve not only as electrical connections to active IC devices on the vertically

stacked wafers 110, 120, and 130 . . . but also [to] bond adjacent wafers 110, 120, and 130." *Id.*

Kim also discloses a "three-dimensional (3-D) wafer-to-wafer vertical stack," such as a "2-wafers vertical stack." Ex. 1008 ¶ 22, Fig. 2. According to Kim, this "vertical stack can effectively integrate diverse process technologies on a single wafer process, such as, for example, logic/memory stacking, processor stacking, optical interconnect, system-on-chip, and RF interconnect." *Id.*

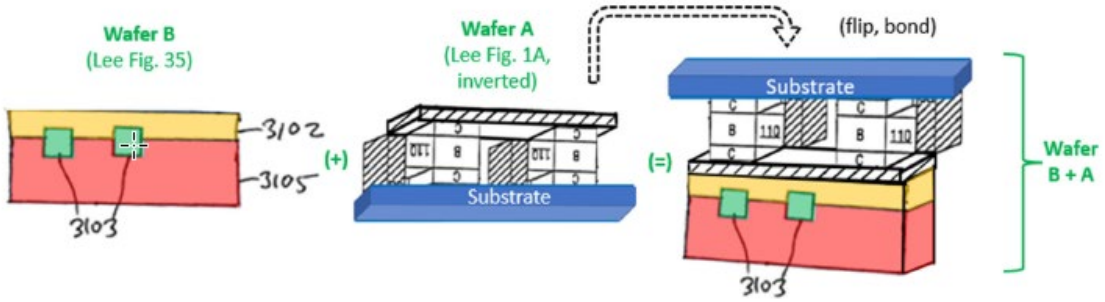
2. *Analysis – Claim 13*

With respect to the preamble and limitations 13[a], [b], and [d], Petitioner contends that Lee discloses these limitations for the same reasons discussed above with respect to obviousness based on Lee alone.[16] Pet. 50, 54. With respect to limitation 13[c], Petitioner contends that Kim discloses a method of forming a three-dimensional (3-D) wafer-to-wafer vertical stack that is applicable for use with "all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, . . . CMOS devices, MOSFETs, and new memory devices." *Id.* at 51 (citing Ex. 1008 ¶¶ 19–20). Petitioner further contends that Kim teaches that the vertical stack may

[16] As discussed above, we determine that Petitioner has not shown that Lee teaches or suggests limitation 13[b] under our construction for "stackable add-on layer." Petitioner's arguments regarding Lee and Kim rely on its arguments with respect to Lee alone for limitation 13[b] and do not expressly address how the combination of Lee and Kim teaches this limitation. Pet. 50; *see also* C.F.R. § 104(b)(4) ("The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon."). Accordingly, for at least this reason, Petitioner has not shown that the combination of Lee and Kim teaches or suggests limitation 13[b].

comprise "any number" of wafers, including a wafer with one or more microprocessors and a wafer including one or more memory devices, and that dielectric layer 102 may be used to separate and bond the wafers. *Id.* (citing Ex. 1008 ¶¶ 20, 22, Fig. 1).

Petitioner's proposed combination is depicted below. Pet. 52.



The depiction above shows Petitioner's proposed method of combining the memory structure of Figures 1A–1B, 2, 7, or 25A of Lee and the substrate of Figure 35 of Lee. *Id.* In this combination, substrate 3105 of Lee having CMOS transistors (driver circuits 3103) and insulating layer 3102 is identified as Wafer B. *Id.* Separately fabricated memory cells (e.g., from Lee's Figure 1A) are formed on their own substrate, identified as Wafer A. *Id.* Wafer A is then flipped and bonded to wafer B. *Id.*

Petitioner contends one of ordinary skill in the art would have been motivated to make such a combination for several reasons. First, Petitioner contends it is unclear in Lee how the bottom level 3104 of array 3101 is formed on insulating layer 3102. Pet. 51. Second, Petitioner contends the proposed combination would have amounted to using a known technique both to improve a similar known device in the same way and to address the same problem recognized by both Lee and Kim using prior art elements according to their established function. *Id.* at 53. Third, Petitioner contends

a person of ordinary skill in the art would have understood that wafer-bonding Lee's bottom level 3104 to insulating layer 3102 would allow for more efficient quality control with less potential waste, as compared to monolithic deposition. *Id.* at 53–54

Patent Owner argues that Petitioner does not establish a motivation to combine Lee and Aspar and advances several reasons why one of ordinary skill in the art would not have combined the references in the manner proposed by Petitioner. PO Resp. 21–30.

For the reasons set forth below, we are not persuaded by Petitioner's rationales for combining Lee and Kim and credit several of Patent Owner's counterarguments.

a. *Bonding Level 3104 of Array 3101 on Insulating Layer 3102*

Petitioner contends that Lee discloses that each level 3104 is deposited on the underlying level of array 3101, but "does not clearly describe how the bottom level 3104 of array 3101 is formed on insulating layer 3102." Pet. 51 (citing Ex. 1007 ¶¶ 107–113). Consequently, Petitioner contends that one of ordinary skill in the art would have looked to other art, such as Kim, for details about attaching bottom level 3104 to insulating layer 3102. *Id.* This is "especially so," according to Petitioner, where a person of ordinary skill in the art, "at the suggestion of Lee, was looking to separately form a two-dimensional array of memory devices and 'package [it] together' with Lee's substrate 3105 having driver circuits 3103 formed therein and insulating layer 3102 on top 'to form a non-monolithic memory device.'" *Id.* at 51–52 (citing Ex. 1003 ¶¶ 190–192; Ex. 1007 ¶ 107); *see also id.* at 52 (asserting that Kim contemplates bonding a wafer having CMOS devices,

like Lee's substrate 3105, with a wafer having memory devices, like Lee's level 3104).

Lee discloses that in its monolithic array of memory devices "each level of the array [is] directly deposited on the layers of each underlying level of the array." Ex. 1007 ¶¶ 107, 111, 141 (noting that the pillar of Figure 9 may be formed by "blanket depositing a first I/O conductor 900 followed by the sequential blanket deposition of the film stack 902 (e.g., N+/P-/N+) of the desired pillar). Thus, Lee explains how each level of its array is formed, i.e., by direct deposition on the underlying layer. *See id.*; PO Resp. 21; Ex. 2029 ¶¶ 115–116.

Petitioner contends that deposition is just one potential implementation technique for the embodiment depicted in Figure 35 of Lee and that Lee contemplates using techniques with SOI technology, including "wafer bonding." Pet. Reply 6–7. Lee expressly states, however, that each level of its memory array is directly deposited on the underlying level of the array. Ex. 1007 ¶¶ 107, 111, 141. Moreover, although Lee discusses SOI technology and wafer bonding, it does not suggest wafer bonding an array of memory devices to the substrate having a dielectric layer. *Id.* ¶¶ 208–209; Sur-reply 11.

In view of the foregoing, we are not persuaded by Petitioner's first rationale that one of ordinary skill in the art would have looked to art beyond Lee, including the wafer bonding art identified by Petitioner, in order to determine how to attach bottom level 3104 to insulating layer 3102 in Lee.

b. *Lee's Disclosures*

Petitioner contends that Lee was "looking to separately form a two-dimensional array of memory devices and 'package [it] together' with Lee's substrate 3105." Pet. 51–52 (citing Ex. 1003 ¶¶ 19–20; Ex. 1007 ¶ 111).

The relevant disclosure of Lee is

> One method of improving device density is to arrange the devices in a monolithic three dimensional array of charge storage devices comprising a plurality of device levels. The term "monolithic" means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

Ex. 1007 ¶ 107. We credit the testimony of Dr. Przybylski that one of ordinary skill in the art would read this disclosure, as well as the disclosures of Lee as a whole, as expressing a preference for monolithic memory structures, which provide specific benefits over stacks of two-dimensional arrays, including increased density and lower cost. Ex. 2029 ¶¶ 117–118; Ex. 1007 ¶¶ 106–107 (explaining that the disclosed monolithic arrays have "an increased density and lower cost" than prior art devices). Thus, Petitioner's argument that one of ordinary skill in the art would have looked to the disclosures of Kim in view of Lee's desire to package two-dimensional arrays is not persuasive.

c. *KSR Rationales*

As explained in *KSR*, "if a technique has been used to improve one device, and a person of ordinary skill would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *KSR*, 550 U.S. at 417. *KSR*

also notes that when there is a design need or market pressure to solve a problem, and one of ordinary skill in the art would have recognized that a known technique would address this problem, the use of the technique may be obvious. *KSR*, 550 U.S. at 420–421.

Petitioner asserts that a person of ordinary skill in the art would have recognized that using wafer-bonding to bond level 3104 to insulating layer 3102 would constitute "nothing more than using a known technique (Kim's wafer bonding) to improve a similar device (the structure in Lee's Figure 35) in the same way (logic/memory stacking using a wafer bonding process)." Pet. 53. Petitioner further asserts that using Kim's method of wafer bonding to bond level 3104 to insulating layer 3102 "would have amounted to applying a known technique (Kim's wafer bonding) to address the same known problem recognized by both Lee and Kim (fabricating 3D memory arrays above a substrate containing electrical devices) using prior art elements according to their established functions (Kim's wafer bonding and Lee's memory cell structures in Figures 1A–B, 2, 7, or 25A in Lee's Figure 35 structure)." *Id.* (citing Ex. 1003 ¶ 195; *Intel*, 61 F.4th at 1380; *KSR*, 550 U.S. at 417).

Petitioner's arguments are not persuasive. Both of Petitioner's *KSR*-based rationales depend on Kim's technique solving a known problem or improving Lee's device. Petitioner identifies no problem in Lee, however, that would motivate one of ordinary skill in the art to turn to wafer bonding. For example, there is no known problem identified by Petitioner in forming Lee's memory cells by sequential deposition over an existing substrate. Nor has Petitioner identified any particular benefit to the operation of Lee's device that would flow from the proposed modification.

Pet. Reply 6 (failing to assert that the proposed combination would have "improved Lee"). This is especially true because Lee acknowledges that stacking of two-dimensional arrays of memory devices was known in the art, and Lee expresses a preference for high-density, low cost, monolithic arrays. Ex. 1007 ¶ 107 (contrasting monolithic arrays to stacked arrays).

Petitioner argues that "[i]mprovement in a categorical sense is not required: the Petition need only show Kim's/Aspar's techniques are 'suitable options.'" Pet. Reply 6 (citing *Intel*, 61 F.4th at 1381). For the reasons discussed below, however, Patent Owner persuasively demonstrates that using Kim's method of wafer stacking, as applied in the Petition, was not a suitable replacement for Lee's direct deposition method of constructing memory arrays. In particular, using Kim's method of wafer stacking would result in low yields and a high level of waste.

Given the lack of improvement to Lee's device from the use of Kim's stacking method, and given the there is no clear problem with Lee's monolithic, direct deposition method that would suggest the need for changing manufacturing methods, we are not persuaded that Petitioner's *KSR*-based rationales would have motivated one of ordinary skill in the art to combine Lee and Kim. This conclusion is strengthened by the fact that, for the reasons set forth below, Patent Owner persuasively argues that Kim's method of wafer stacking would significantly reduce yields and increase waste while providing little to no benefit.

d. *Quality Control and Reduced Waste*

Petitioner contends that one of ordinary skill in the art would have used wafer bonding to add the pre-formed memory cells of Lee to a

separately fabricated substrate because this would allow for quality control to be performed on the memory cells prior to stacking. Pet. 54. Petitioner asserts, "[i]f a quality control issue is detected, only that level 3104 would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously deposited stacks, etc.) would need to be discarded." *Id.* (citing Ex. 1003 ¶ 196). According to Petitioner, use of Kim's stacking method would therefore minimize waste resulting from defects detected during the quality control process. *Id.*

In support of its quality control benefit, Petitioner looks to Dr. Sechen's testimony and the disclosures of Fung. Pet. 53–54 (citing Ex. 1003 ¶ 196; Ex. 1016). Fung notes that "[d]ensity can be upgraded many fold by stacking chips or wafers" and "[s]ignificant speed improvement can also be expected because the interconnecting wires linking the chips are shortened substantially." *Id.* 1:15–19. There are, however, "several problems associated with stacking wafers." *Id.* at 1:33–38. "First, the yield loss is very large," with some potential yields for a two-wafer stack as low as 49%. *Id.* at 1:34–39. Second, there are alignment problems with stacking wafers, requiring the feature sizes of the interconnects to be very large, thereby degrading "the density and performance of the [three-dimensional integrated circuits]." *Id.* at 1:39–47. Given these issues, Fung explains that "one must stack only good chips on top of good chips on a wafer to maintain a reasonable yield." *Id.* at 1:48–50. Stacking chips as opposed to wafers also allows the alignment tolerance to be "significantly superior" to "stacking wafers on top of one another." *Id.* at 1:52–55. As such, Fung reports that "stacking *chips* is definitely the preferred approach."

Id. at 1:55–56 (emphasis added); *see also id.* at 5:6–12 (noting that wafer level testing is performed *before* dicing the SOI wafer into individual chips for stacking).

The Petition proposes to bond two wafers, Wafer A (substrate with electrical devices and a dielectric layer) and Wafer B (preformed memory cells on a substrate). Pet. 52. In other words, the Petition proposes to stack an entire wafer, as opposed to individual, previously-tested chips. Pet. 52; Tr. 15:3–14 ("For Kim, where you're forming complete devices prior to bonding, you would again be likely doing the whole wafer."). Given the disclosures of Fung, which are expressly relied upon in the Petition, we credit the testimony of Dr. Przybylski that Petitioner's proposed method of wafer stacking would actually result in lower yields, increased waste, and suffer from alignment problems. Ex. 2029 ¶¶ 125–127, 130 (explaining that even if there were errors in some dies, "fabs would not discard the entire wafer because that would waste an entire wafer's worth of dies"); PO Resp. 28–29. We also credit the testimony of Dr. Przybylski that Kim's method of wafer bonding would essentially discard an entire wafer for every bonding step, as the substrate would need to be ground or etched off each time a layer is bonded in Kim's method. Ex. 2029 ¶¶ 130–131; PO Resp. 29 ("Kim's technique does not reduce waste, it multiplies it.").

Petitioner contends wafer thinning was optional in Kim. Pet. Reply 9. Patent Owner persuasively demonstrates, however, that thinning would not have been optional in Petitioner's proposed combination because the deposited memory cells require an additional conductive layer in order to operate, and the wafer would interfere with forming this conductive layer. Sur-reply 14 (citing Ex. 2029 ¶¶ 130–132); Tr. 33:1–5 (Petitioner's counsel

agreeing that the blue substrate in the proposed combination would be "ground down"). Given that nearly an entire wafer would need to be ground away when using Kim's method to construct the memory device of Lee, Petitioner does not persuasively explain why Kim's stacking method would have reduced waste or have been preferable to Lee's direct deposition method. Ex. 2029 ¶¶ 130–134.

In view of the foregoing, we credit the testimony of Dr. Przybylski that one of ordinary skill in the art would not have used Kim's wafer bonding method to construct Lee's device due to the decreased yields and increased waste.

e. *Conclusion – Reason to Combine*

Petitioner identifies no persuasive, specific benefit to wafer bonding that would have led one of ordinary skill in the art to the combination of Lee and Kim. In contrast, Patent Owner and Dr. Przybylski persuasively explain why wafer bonding would have resulted in reduced yields and significantly increased waste. As such, Petitioner has not demonstrated by a preponderance of the evidence that one of ordinary skill in the art would have combined Lee and Kim to arrive at the claimed invention.

3. *Analysis – Claims 14–17*

Claims 14–17 each require an "SOI pillar." Ex. 1001, 12:35–52. Petitioner contends that if Patent Owner argues that an "SOI pillar" "encompasses any pillar-shaped structure with insulating material below it," then Lee discloses or suggests the subject matter of claims 14–17. Pet. 31–41 (contentions based on Lee alone), 54 (relying on the same contentions for combination of Lee and Kim as presented for Lee alone).

Petitioner's arguments with respect to these claims do not remedy the deficiencies noted above with respect to independent claim 13. As such, Petitioner does not demonstrate by a preponderance of the evidence that the subject matter of claims 14–17 would have been obvious over Lee and Kim.

I. Claims 16 and 17 over Lee, Kim, and Endoh (Ground 1D)

Petitioner contends that, to the extent Patent Owner's apparent construction of "SOI pillar" is adopted, the subject matter of claims 16–17 would have been obvious over the combined disclosures of Lee, Kim, and Endoh. Pet. 55.

Petitioner's arguments with respect to this ground do not remedy the deficiencies noted above with respect to the reasons to combine Lee and Kim. Accordingly, Petitioner does not demonstrate by a preponderance of the evidence that claims 16 and 17 would have been obvious over the combined disclosures of Lee, Kim, and Endoh.

J. Claim 13 over Johnson (Ground 2A)

Petitioner contends the subject matter of claim 13 would have been obvious over the disclosures of Johnson. Pet. 65–73.

1. *Johnson*

Johnson is titled "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication," and issued March 7, 2000. Ex. 1010, codes (45), (54).

Johnson discloses a "very high density field programmable memory" that includes an array that "is formed vertically above a substrate using several layers, each layer of which includes vertically fabricated memory cells." Ex. 1010, code (57). The fabrication process for the memory cells of

Johnson is schematically illustrated in Figures 6(b)–6(g). *Id.* at 12:42–43. Figure 6(b) is reproduced below:

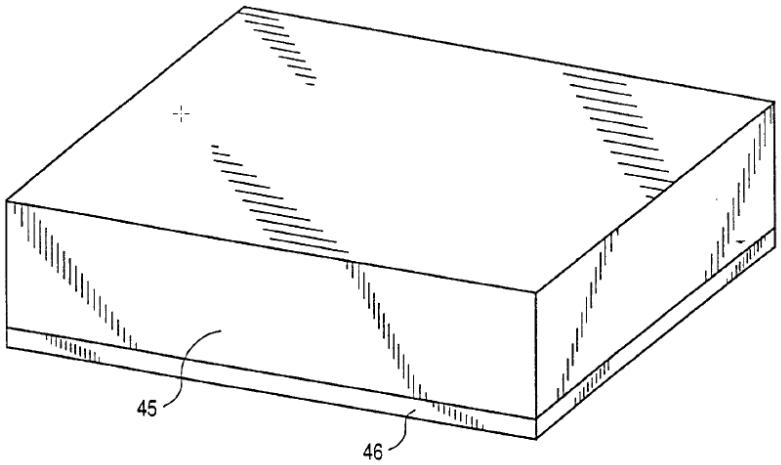


FIG. 6(b)

Figure 6(b) is a perspective view of a conductor layer and layer stack used in the fabrication of a memory cell. *Id.* at 4:38–39. Johnson explains that fabrication of the memory cell begins with a wafer that may have CMOS transistors for the peripheral circuitry fabricated in the monocrystalline substrate. *Id.* at 13:26–29. An insulator is then deposited and, preferably, planarized (neither of these steps or structures is depicted in Figure 6(b)). *Id.* at 13:30–36. Then, first conductor layer 46 and layer stack 45 are sequentially deposited. *Id.* at 13:32–35. Next, a mask that defines the features of the conductor layer is applied and these features are etched into both pillar layer stack 45 and first conductor layer 46. *Id.* at 13:37–39. An insulator is then deposited on the wafer and planarized. *Id.* at 13:39–40.

Figure 6(c) is reproduced below:

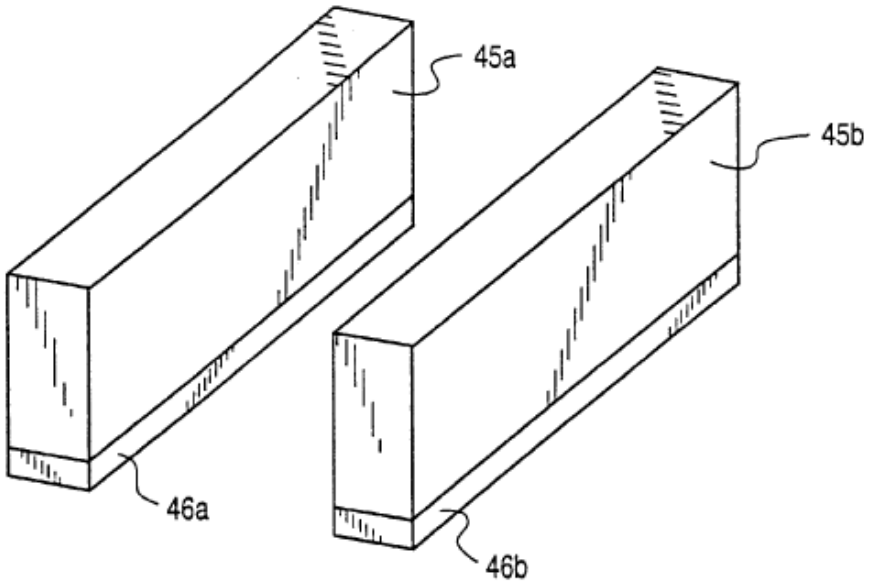


Figure 6(c) depicts the wafer after etching and depositing of the insulator layer on the wafer, and shows individual pillar layer strips, as opposed to isolated individual pillars. Ex. 1010, 13:41–45. Although not shown in Figure 6(c), Johnson explains that a dielectric fills the voids between the strips and pillars, adding support to the array. *Id.* at 13:51–53.

Johnson explains that this process is repeated multiple times to form multiple levels of conductors and vertically stacked pillars. Ex. 1010, 13:58–14:27. Figure 6(g) depicts a stack with three conductor layers. *Id.* at 14:21–22.

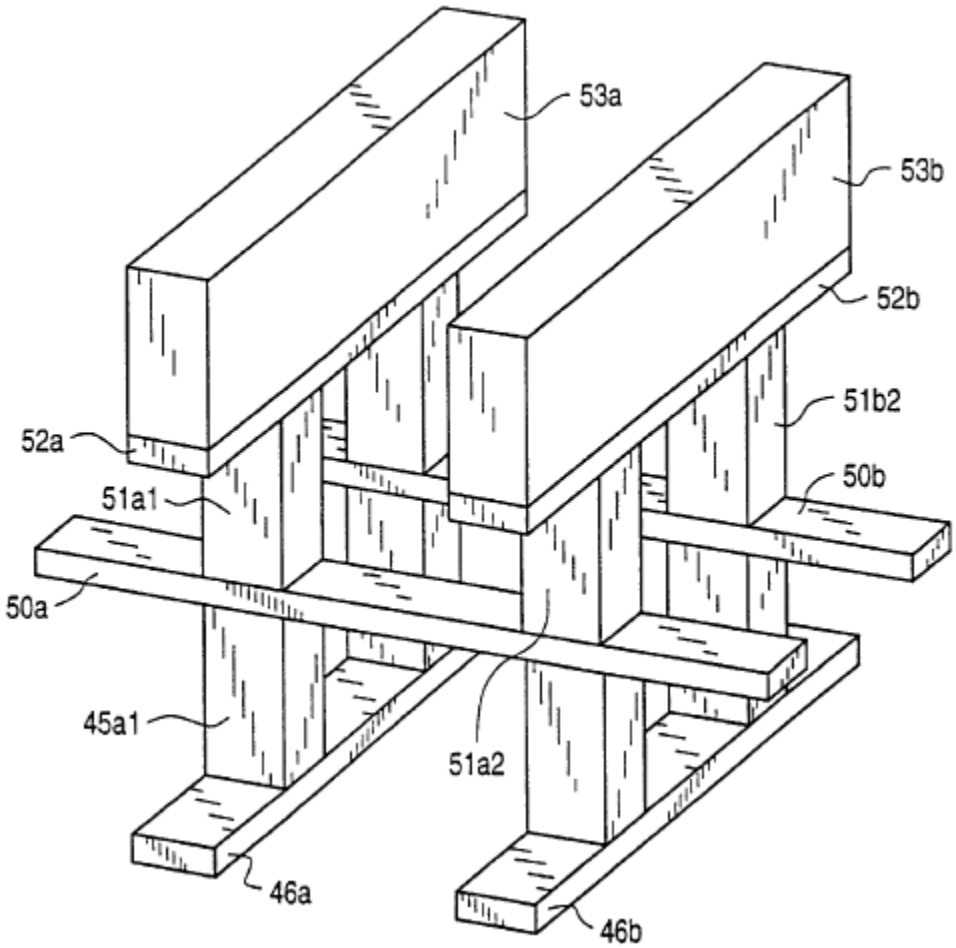


Figure 6(g) depicts the wafer after three levels of conductors and layer stacks have been deposited, but before all of the masking and etching steps have been applied to the upper most layer. *Id.* at 14:10–19.

Figure 8(b) of Johnson is reproduced below.

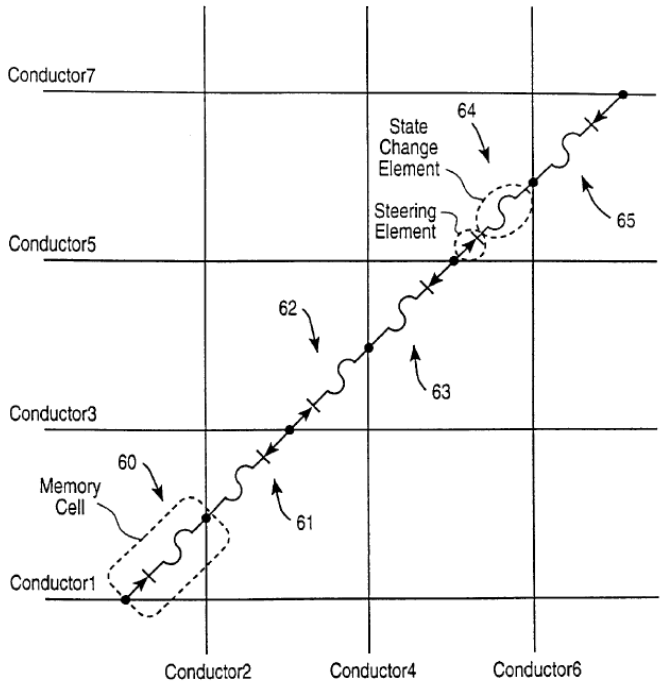


FIG. 8(b)

Figure 8(b) is a schematic of the vertically stacked cells of Johnson. Ex. 1010, 4:56. In Figure 8(b), there are six memory cells 60–65. Ex. 1010, 19:30–31. As shown in this schematic, memory cells are located between where conductor 3 crosses conductor 2, where conductor 4 crosses conductor 3, etc. *Id.* at 19:37–46. Johnson explains that each memory cell contains a steering element and a state change element. *Id.* at 19:40–42.

Johnson explains that the steering element is a semiconductor element that has a strongly asymmetric current-versus-voltage characteristic and conducts much more readily in one direction than in the other. Ex. 1010, 7:58–61.

> Some possible implementations of the steering element are (i) a PN junction diode, in amorphous, microcrystalline,

> polycrystalline or single crystal semiconductor (e.g., Si, Ge, SiGe, GaAs, InP, etc.); (ii) a metal-semiconductors Schottky diode; (iii) a junction field-effect transistor with gate connected to source (or to drain); (iv) a MOSFET with gate either floating, or connected to source or connected to drain; (v) a Zener diode, avalanche diode, or tunnel diode; (vi) a four-layer diode (SCR); (vii) a P-I-N diode in amorphous, microcrystalline, polycrystalline or single crystal semiconductor; and others that will be readily apparent to those skilled in the art.

Id. at 7:61–8:5. Johnson further explains that the state change element is where data is actually stored and may take many forms, including various fuses or anti-fuses. *Id.* at 8:32–45.

2. *Analysis – Claim 13*

Petitioner contends that Johnson discloses or suggest every limitation of claim 13, at least under Patent Owner's apparent construction of "stackable add-on layer." Pet. 65–73. With respect to element 13[a], Petitioner contends that Johnson discloses forming CMOS transistors, i.e., electrical devices, within a monocrystalline substrate and depositing a dielectric insulating layer over the substrate and electrical devices. *Id.* at 65–66 (citing Ex. 1010, 13:26–35; Ex. 1003 ¶ 226). With respect to element 13[b], Petitioner contends that Johnson discloses vertically oriented semiconductor memory cells and a "stackable add-on layer" under Patent Owner's apparent construction of this term, i.e., a monolithically and directly deposited layer created on an insulator. *Id.* at 66–68, 72. With respect to element 13[c], Petitioner contends that the "stackable add-on layer" of Johnson is bonded to an insulator deposited on a wafer. *Id.* at 69–72 (citing Ex. 1010, 12:8–12, 12:42–65, 13:26–35, Fig. 6(b)). With respect

to element 13[d], Petitioner contends that Johnson is directed to non-volatile memory cells that include at least one transistor. *Id.* at 72–73.

As discussed above, we adopt Petitioner's construction of "stackable add-on layer." Petitioner does not assert that Johnson discloses a "stackable add-on layer" under its construction of that term. Pet. 65. As such, Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious based on Johnson alone.

K. Claim 13 over Johnson and Kim (Ground 2B) or Johnson and Aspar (Ground 2C)

Petitioner contends the subject matter of claim 13 would have been obvious over both the combined disclosures of Johnson and Kim and the combined disclosures of Johnson and Aspar. Pet. 74–82.

With respect to the preamble and limitations 13[a], [b], and [d], Petitioner contends that Johnson discloses these limitations for the same reasons discussed above with respect to obviousness based on Johnson alone.[17] Pet. 74, 77, 82. With respect to limitation 13[c], Petitioner contends that Kim and Aspar each teach "the stackable add-on layer being bonded" under Petitioner's proposed claim construction and that a person of

[17] As discussed above, we determine that Petitioner has not shown that Johnson teaches or suggests limitation 13[b] under our construction for "stackable add-on layer." Petitioner does not expressly assert that Aspar or Kim teach or suggest limitation 13[b]. Pet. 74, 77; *see also* C.F.R. § 104(b)(4) ("The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon."). Accordingly, for at least this reason, Petitioner has not shown that the combination of Johnson and Kim or Aspar teaches or suggests limitation 13[b].

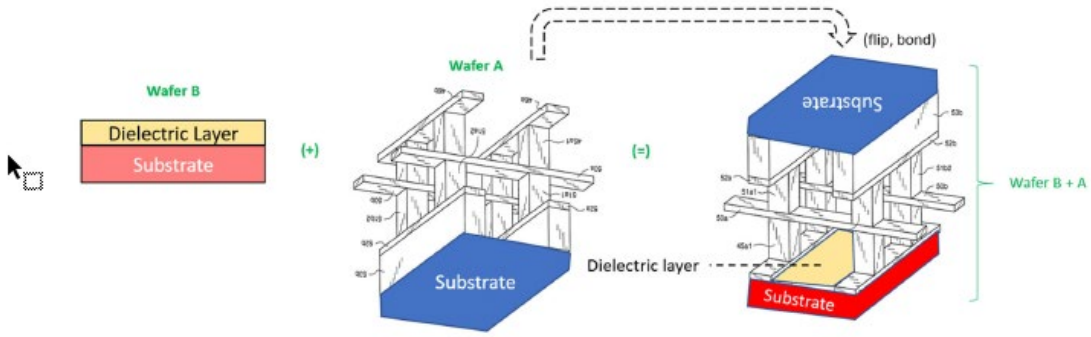
ordinary skill in the art would have combined that teaching with Johnson. *Id.* at 74–82; *see, e.g., id.* at 75 ("A [person of ordinary skill in the art] would have been motivated to wafer bond Johnson's layer of memory cells ("stackable add-on layer") to its insulating layer ("dielectric layer") based on Kim's teachings."), *id.* at 78 ("A [person of ordinary skill in the art] would have been motivated to wafer bond a layer of semiconductor pillars as depicted in Johnson's Figures 6(a)–(b) ("stackable add-on layer") to the insulating layer above the substrate ("dielectric layer")" in view of Aspar).

Patent Owner disputes Petitioner's contentions concerning the teachings of Johnson and Petitioner's asserted reasons to modify Johnson and combine its teachings with Kim or Aspar. PO Resp. 57–74.

For the reasons discussed below, we are not persuaded by Petitioner's obviousness contention based on Johnson in combination with Kim or Aspar.

1. *Petitioner's Combination of Johnson and Kim*

Petitioner contends that one of ordinary skill in the art would have separately fabricated the memory cells of Johnson on their own substrate (Wafer A) and then Wafer A would be flipped and bonded to Wafer B having, for example, Johnson's "CMOS transistors" and insulating layer. Pet. 75. Petitioner illustrates this combination as follows:



In the proposed combination depicted above, Petitioner contends that, as in Kim Figure 1, Johnson's layer of memory cells ("stackable add-on layer") would be wafer bonded to Johnson's insulating layer ("dielectric layer"). *Id.* (citing Ex. 1003 ¶ 248).

Petitioner contends one of ordinary skill in the art would have sought to combine Johnson and Kim because wafer-bonding Johnson's level of memory cells to its insulating layer "allows for more efficient quality control with less potential waste," as compared to monolithic deposition. Pet. 76 (citing Ex. 1003 ¶ 250). According to Petitioner, quality control could be performed on the memory cells (e.g., testing for shorts) and if a quality control issue is detected, then only that level would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited stacks, etc.) would need to be discarded. *Id.*

> Petitioner further contends that the proposed combination consists of nothing more than using a known technique (Kim's wafer bonding) to improve a similar known device (Johnson's structure) in the same way (logic/memory stacking using a wafer bonding process). *Id.* In addition the combination would have amounted to applying a known technique (Kim's wafer bonding) to address the same known problem recognized by both Johnson and Kim (fabricating 3D memory arrays above a substrate containing electrical devices) using prior art elements according to their established functions (Kim's wafer bonding and Johnson's structure).

Pet. 75–76.

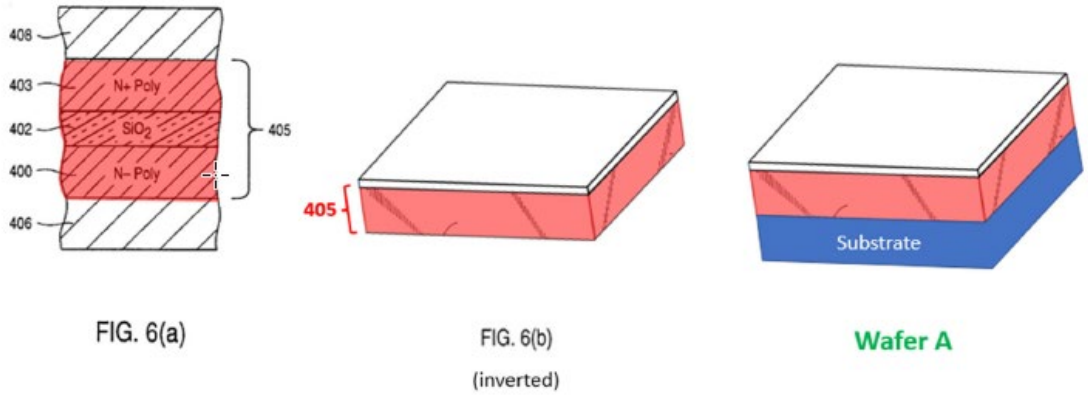
Petitioner's arguments regarding Johnson and Kim are similar to Petitioner's arguments regarding Lee and Kim in that Petitioner relies on Johnson or Lee for teaching limitations 13[pre]–13[b] and 13[d], and

Petitioner relies on Kim to teach limitation 13[c], "the stackable add-on layer being bonded to the dielectric layer." *Compare* Pet. 50–54 (addressing Lee and Kim for claim 13), *with* Pet. 74–77 (addressing Johnson and Kim for claim 13). Petitioner's reasons to combine Johnson and Kim are also substantively the same as those for combining Lee and Kim. *Id.* at 53–54, 75–77.

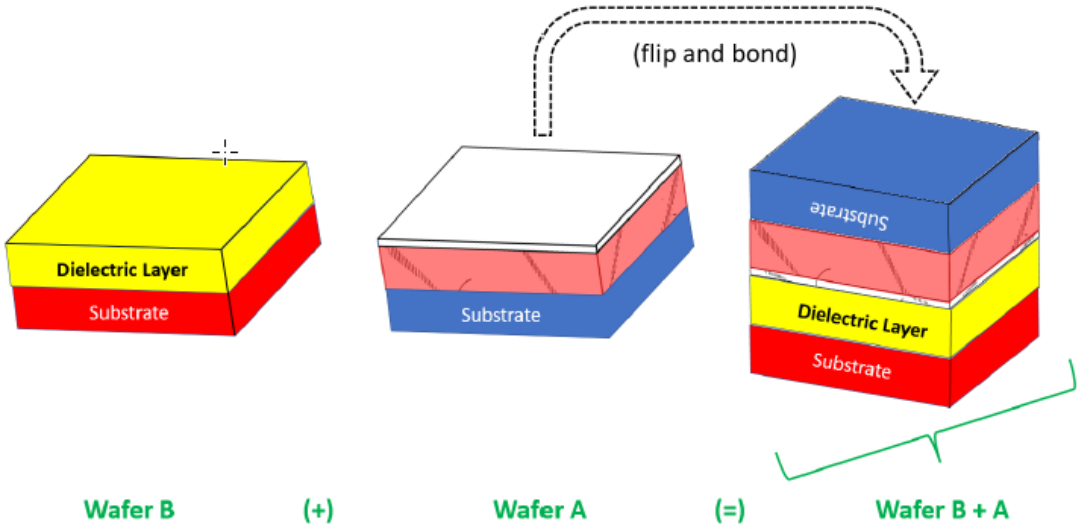
For the same reasons discussed above with respect Lee and Kim, we determine that Petitioner has not demonstrated that one of ordinary skill in the art would have sought to combine Johnson and Kim. In particular, Petitioner fails to identify any problem in Johnson that would have been solved by using Kim's manufacturing technique or any benefit to using Kim's method as opposed to Johnson's method of direct deposition. PO Resp. 65–69. We also find that, contrary to Petitioner's arguments, Patent Owner provides persuasive evidence, supported by the testimony of Dr. Przybylski which we credit, that a skilled artisan would not favorably consider modifying the device of Johnson (or Lee) to include Kim's three-dimensional (3-D) wafer-to-wafer vertical stack because the modification would lead to significantly reduced yields (potentially less than 50%) and increased waste (grinding away an entire wafer). PO Resp. 28–29, 66 (citing Ex. 1016, 1:32–52; Ex. 2029 ¶¶ 125–129, 193, 195).

2. *Petitioner's Combination of Johnson and Aspar*

Petitioner contends one of ordinary skill in the art would have deposited the doped stack depicted in Figures 6(a) and 6(b) of Johnson on a substrate, with a conductive layer then deposited over the doped stack. Pet. 79. Petitioner illustrates its contention as follows:



In Petitioner's proposed combination, Wafer A includes a substrate, Johnson's doped stacked structure, and a conductive layer. Pet. 78–79. Petitioner's Wafer A would be flipped upside down and bonded to Wafer B, which consists of Johnsons's substrate with "CMOS transistors" and insulating layer ("dielectric layer"). *Id.* This process is depicted below:



Petitioner contends that, when combined in the proposed fashion, the combination of Johnson and Aspar teaches or suggests every limitation of challenged claim 13. Pet. 74–82.

Petitioner's contention about how a person of ordinary skill in the art would have combined Johnson and Aspar is nearly identical to Petitioner's contention for the combination of Lee and Aspar. In both cases, Petitioner contends it would have been obvious to wafer bond an unpatterned, doped stacked structure to a separately fabricated substrate containing electric devices. *Compare* Pet. 59–60 (addressing Lee and Aspar), *with* Pet. 79–80 (addressing Johnson and Aspar). Petitioner's arguments as to why a person of ordinary skill in the art would have modified Johnson in view of Aspar to arrive at the subject matter of claim 13 are also nearly identical to those for combining Aspar with Johnson. *Compare* Pet. 60–63 (addressing Lee and Aspar), *with* Pet. 77–82 (addressing Johnson and Aspar); *see also* Pet. Reply 26–27 (identifying the overlapping arguments for Johnson-Kim/Aspar). For the reasons set forth above with respect to the combination of Lee and Aspar, we determine that Petitioner has not persuasively demonstrated that one of ordinary skill in the art would have combined Johnson and Aspar to arrive at the claimed invention with a reasonable expectation of success. Tr. 35:12–18 (Petitioner's counsel asserting that there is no "specific distinction" between the Johnson-Aspar or Johnson-Kim grounds that would make them more robust than the Lee-based grounds); *id.* at 66:5–12 (Petitioner's counsel asserting that the Lee-based grounds generally have "more disclosure to support the motivation to combine" as compared to the Johnson-based grounds). In particular, Petitioner fails to persuasively identify any problem with Johnson's direct deposition technique or any benefit achieved by modifying Johnson with Aspar's technique. In contrast, Patent Owner persuasively demonstrates that using Aspar's technique to form Johnson's doped stacked structure would use Aspar in a manner not

disclosed in the reference (which discloses a technique for making SOI wafers and SOI layer stacks having layers of SiO_2 and undoped silicon). PO Resp. 70–74. Patent Owner also persuasively demonstrates that Petitioner's proposed combination of Johnson and Aspar would lead to damage during an annealing step, and Petitioner's proposed combination could potentially lead to either a thin layer of the substrate remaining after the splitting step or removal of a portion of the doped stack structure. *Id.*

In view of the foregoing, Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious in view of Johnson and Aspar.

L. Obviousness of Claim 1 over Park and Kim (Ground 3)

Petitioner contends the subject matter of claim 1 would have been obvious over the combined disclosures of Park and Kim. Pet. 82–91.

1. *Park*

Park is titled "Semiconductor Device Having Vertical Metal Oxide Semiconductors and a Method for Manufacturing the Same," and issued November 5, 1996. Ex. 1011, codes (45), (54).

Park notes that conventional memory devices "traditionally form a transistor in a lateral direction on a semiconductor substrate." Ex. 1011, 1:22–23. Park explains, however, that "it is substantially impossible to realize a semiconductor memory device of a continued higher capacity using the conventional planar layout." *Id.* at 1:31–33.

To allow for higher capacity memory devices, Park discloses the use of a silicon pillar that "is extended in a perpendicular (vertical) direction with respect to the semiconductor substrate" and surrounded by an insulating

film. Ex. 1011, 2:15–20. "A gate insulating film is interposed between the silicon pillar and a gate electrode surrounding the silicon pillar" and impurity regions "are formed in upper and lower portions of the silicon pillar to form the source and drain regions." *Id.* at 2:20–25.

Figure 9 of Park is reproduced below:

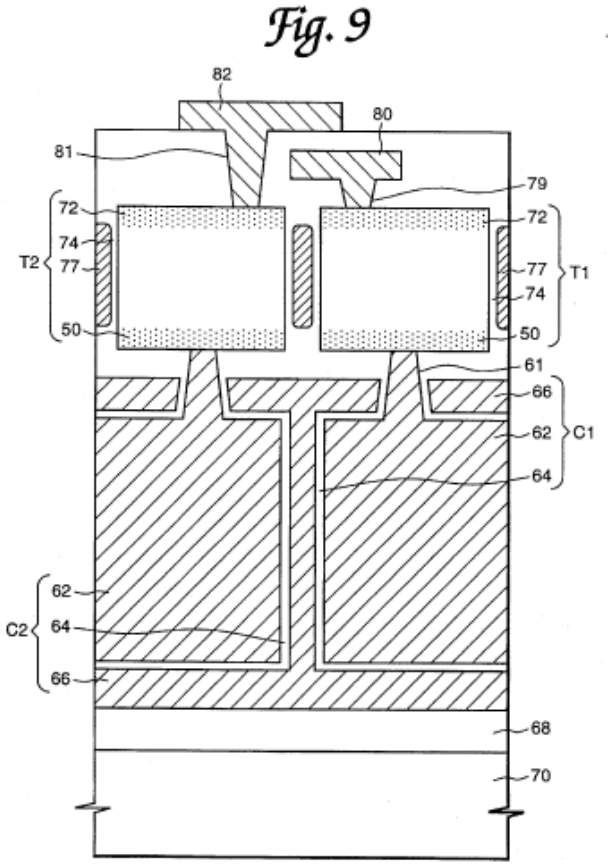


Figure 9 is a cross-sectional view of a DRAM cell manufactured according to the invention of Park. Ex. 1011, 5:33–35. In Figure 9, transistors T1 and T2 are formed with a vertical channel structure. *Id.* at 5:36–37. Capacitors C1 and C2 are formed under first and second transistors T1 and T2 and are comprised of storage electrodes 62 connected to source regions 50 of the first and second transistors T1 and T2. *Id.* at 5:39–41. Plate electrode 66 surrounds the entire surface of the storage electrode 62, with a dielectric film

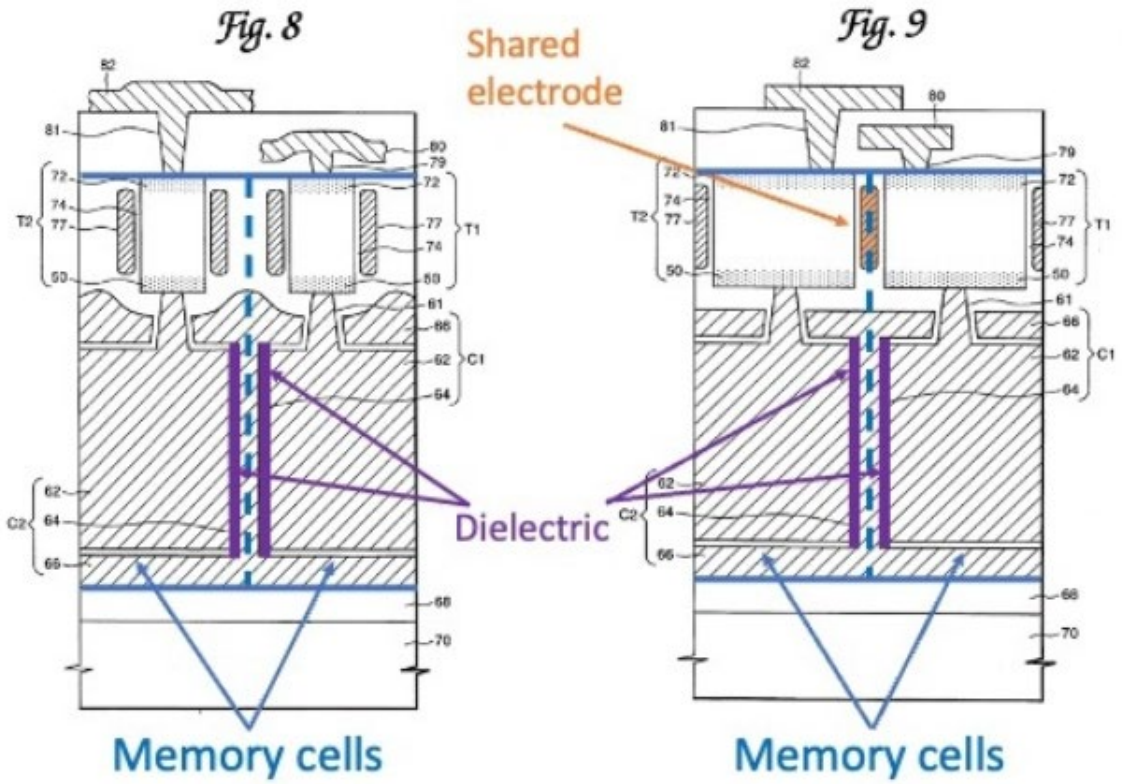
64 interposed therebetween. *Id.* at 5:41–43. First bitline 80 is connected to drain region 72 of first transistor T1, and second bitline 82 is connected to drain region 72 of second transistor T2. *Id.* at 5:43–46.

2. *Analysis*

Petitioner contends the use of Kim's wafer stack comprising logic devices in combination with Park's DRAM cells teaches or suggests every limitation of claim 1. Pet. 83–93. Petitioner further contends that one of ordinary skill in the art would have been motivated to vertically stack Park's DRAM memory cells using Kim's wafer stack method because this combination would "increase integration" and result in reduced interconnect RC delay and increased system performance. *Id.* at 83–84.

The parties' dispute regarding this combination centers around whether Park discloses "memory cells [] separated from each other by dielectric material." Pet. 88–89; PO Resp. 76–77. Petitioner contends that Park discloses that each of its vertically structured transistors are "surrounded [] with an insulating film" and that dielectric film 64 is also interposed between the plate and storage electrodes of capacitors C1 and C2. Pet. 88–89 (citing Ex. 1011, 2:16–21, 4:6–27, 5:21–22, 5:37–43, Fig. 3). Petitioner further contends that one of ordinary skill in the art "would have . . . understood the need to separate the memory cells with dielectric material for proper operation (e.g., avoiding shorts)." *Id.* at 89. According to Petitioner, "because both the transistors and capacitors of each memory cell are surrounded by insulating material," each of Park's DRAM memory cells are "separated from each other by dielectric material," as recited in claim 1. *Id.*

Patent Owner contends that the capacitors disclosed in Park are not isolated by the dielectric, as asserted by Petitioner. PO Resp. 76–77. Patent Owner provides an annotated version of Figures 8 and 9 of Park:



Figures 8 and 9 of Park are annotated above to identify the shared electrode and dielectric of Park. *Id.* at 77. Patent Owner contends that Figures 8 and 9 plainly show that the adjoining memory cells "share plate electrode 66," and thus the capacitors are not isolated by dielectric material. *Id.* at 76. According to Patent Owner, the transistors are only isolated by an insulating material between the gate electrodes 33 in the bitline direction (Figure 8), whereas they share gate electrode 77 (Fig. 9 in orange) in the wordline direction. *Id.* at 77 (citing Ex. 1011, 5:49–54).

Petitioner argues in response that dielectric material in fact separates the memory cells of Park from one another. Pet. Reply 28–29 (citing Pet. 88–89). Petitioner does not contest that the memory cells share a common electrode or that the dielectric material is part of the capacitor of each memory cell, but asserts that the '702 patent "does not support a complete-separation requirement." *Id.* at 29. Petitioner further contends that one of ordinary skill in the art would have understood the need to separate the memory cells with dielectric material for proper operation. Pet. 89.

On this record, Petitioner does not persuasively contest that the memory cells of Figure 9 of Park share plate electrode 66 and gate electrode 77 and that dielectric 64 forms an integral part of the capacitor of each memory cell, as asserted by Patent Owner. Sur-reply 29. Nor does Petitioner persuasively assert that the claim term "the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material" is broad enough to encompass memory cells that are electrically connected to each other through a common conductive plate electrode. *See* Ex. 1001, 10:55–57; Pet. Reply 28–29. In other words, the presence of some dielectric material between the memory cells, but not enough to electrically separate the cells from each other, does not meet the claim. As such, Petitioner does not persuasively demonstrate that Park and Kim teach or suggest "memory cells separated from each other by dielectric material," as recited in independent claim 1.

In view of the foregoing, Petitioner fails to demonstrate by a preponderance of the evidence that claim 1 would have been obvious over the combined disclosures of Park and Kim.

IV. MOTION TO EXCLUDE EVIDENCE

Patent Owner moves to exclude Exhibits 1040–1046, 1048–1050, and 1054, as well as corresponding paragraphs 22–25 of Dr. Schen's reply declaration (Ex. 1037). Mot. 1. According to Patent Owner, "[t]hese exhibits are either irrelevant because [Petitioner] never cites to them, or are cited to support [Petitioner's] improper new theory on reply." *Id.*

A. Exhibits 1040, 1042, 1046, and 1054

Patent Owner contends Exhibits 1040, 1042, 1046, and 1054 should be excluded because neither Patent Owner nor its expert cites or relies on these four exhibits. Mot. 4.

As Petitioner notes in its Opposition, however, the Board previously granted Petitioner's request to expunge Exhibits 1040, 1042, 1046, and 1054. Opp. 1 n.1. As these exhibits have been expunged, Patent Owner's request to exclude these exhibits is denied as moot.

B. Exhibits 1041, 1043–1045, 1048–1050, and Paragraphs 22–25 of Exhibit 1037

Petitioner contends Exhibits 1041, 1043–1045, 1048–1050, and Paragraphs 22–25 of Exhibit 1037 constitute new evidence and/or new argument that exceeds the proper scope of reply. Mot. 1. In particular, Patent Owner contends these exhibits were submitted to support Petitioner's new theory that "[p]rocess optimization [is a] motivation to combine" Lee and Kim or Aspar. *Id.* (quoting Pet. Reply 10).

As noted by Petitioner in its Opposition, a motion to exclude is not a vehicle to "address arguments or evidence that a party believes exceeds the proper scope of reply or sur-reply." Patent Trial and Appeal Board

Consolidated Trial Practice Guide November 2019, at 79. Rather, the proper vehicle to challenge whether arguments or evidence are beyond the proper scope of reply is a motion to strike. *Id.* at 80. A motion to strike, however, is not required for the Board to identify and disregard "new issues or belatedly presented evidence that exceeds the proper scope of reply." *Id.* This is because "the Board is capable of identifying new issues or belatedly presented evidence when weighing the evidence at the close of trial." *Id.* And, for the reasons discussed above, we determine that Petitioner's "process optimization" arguments are new and exceed the proper scope of reply.

In view of the foregoing, Patent Owner's motion to exclude Exhibits 1041, 1043–1045, 1048–1050, and Paragraphs 22–25 of Exhibit 1037 is denied.

V. CONCLUSION

For the foregoing reasons, we determine that Petitioner does not demonstrate by a preponderance of the evidence that claims 1 and 13–17 are unpatentable. Our conclusions are summarized in the following table.

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claims Not Shown Unpatentable
13–17	103(a)	Lee		13–17
16, 17	103(a)	Lee, Endoh		16, 17
13–17	103(a)	Lee, Kim		13–17
16, 17	103(a)	Lee, Kim, Endoh		16, 17
13–17	103(a)	Lee, Aspar		13–17
16, 17	103(a)	Lee, Aspar, Endoh		16, 17
13	103(a)	Johnson		13
13	103(a)	Johnson, Kim		13
13	103(a)	Johnson, Aspar		13

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claims Not Shown Unpatentable
1	103(a)	Park, Kim		1
Overall Outcome				1, 13–17

VI. ORDER

For the foregoing reasons, it is:

ORDERED that Petitioner does not demonstrate by a preponderance of the evidence that any challenged claim of the '702 patent is unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude is dismissed-in-part and denied-in-part; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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