

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner

IPR2023-01047
U.S. Patent No. 7,921,323

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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PETITIONER’S EXHIBIT LIST

Ex.1001	U.S. Patent No. 7,921,323 to Yancey et al.
Ex.1002	File History of U.S. Patent No. 7,921,323
Ex.1003	Declaration of Dr. Daniel Blumenthal
Ex.1004	<i>Curriculum Vitae</i> of Dr. Daniel Blumenthal
Ex.1005	U.S. Patent Publication No. 2002/0059274 to Hartsell et al.
Ex.1006	U.S. Patent No. 6,907,595 to Curd et al.
Ex.1007	U.S. Patent No. 6,496,291 to Raj et al.
Ex.1008	<i>Lionra Techs. Ltd. v. Fortinet, Inc.</i> , 2:22-cv-00322-JPR-RSP, Dkt. 78 (E.D. Tex. Dec. 23, 2022)
Ex.1009	Microsoft Press, <i>Computer Dictionary</i> , Third Edition, 1997 (excerpts)
Ex.1010	“Virtex-II Pro™ Platform FPGAs: Introduction and Overview,” Xilinx, March 24, 2003 (Internet Archive Capture)
Ex.1011	“Virtex-II Pro™ Platform FPGA User Guide,” Xilinx, June 30, 2003 (Internet Archive Capture)
Ex.1012	Internet Archive Affidavit for Ex.1010, Ex.1011
Ex.1013	U.S. Patent No. 7,680,054 to Acharya
Ex.1014	U.S. Patent No. 7,039,057 to Acharya et al.
Ex.1015	U.S. Patent No. 7,382,787 to Barnes et al.
Ex.1016	United States District Court – National Judicial Caseload Profile (March 2023), available at https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2023/03/31-1
Ex.1017	Complaint, <i>Lionra Techs. Ltd. v. Cisco Sys., Inc.</i> , No. 2:22-cv-

	00305 (E.D. Tex. Aug. 8, 2022)
Ex.1018	Docket Control Order, <i>Lionra Techs. Ltd. v. Cisco Sys., Inc.</i> , No. 2:22-cv-00305, Paper 55-1 (E.D. Tex. Dec. 1, 2022)
Ex.1019	Memorandum of Director Katherine K. Vidal, “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation,” June 21, 2022 (“ <i>Fintiv</i> Guidance”)
Ex.1020	PACER Calendar Events Report for Judge Rodney Gilstrap, May 20, 2024
Ex.1021	L. Kazovsky et al., “Optical Fiber Communication Systems,” 1996
Ex.1022	J. Goodman, “Optical Interconnection in Microelectronics,” SPIE Vol. 456 Optical Computing, 1984
Ex.1023	R. Michalzik, “Optical Backplanes, Board and Chip Interconnects,” Fiber Optic Data Communication: Technological Trends and Advances, 2002
Ex.1024	K. Hahn et al., “Gigabyte/s Data Communications with the POLO Parallel Optical Link,” Electronics Components and Technology Conference, 1996
Ex.1025	D. Blumenthal, “Routing Packets with Light,” Scientific American, Jan. 2001
Ex.1026	M. O’Mahony et al., “The Application of Optical Packet Switching in Future Communication Networks,” IEEE Communications Magazine, Mar. 2001
Ex.1027	N. Sherwani et al., “Introduction to Multichip Modules,” 1995
Ex.1028	C. Maxfield, “The Design Warrior’s Guide to FPGAs: Devices, Tools, and Flows,” 2004
Ex.1029	U.S. Patent No. 5,898,801 to Braun
Ex.1030	Scott Hauck, “The Roles of FPGA’s in Reprogrammable Systems,” Proceedings of the IEEE, vol. 86, no. 4 (April 1998)

Ex.1031	J. Lockwood et. al., “Reprogrammable Network Packet Processing on the Field Programmable Port Extender (FPX),” FPGA 2001 (Feb. 11-12, 2001)
Ex.1032	U.S. Patent No. 6,891,397 to Brebner
Ex.1033	U.S. Patent Publication No. 2004/0249964 to Mougel

I. INTRODUCTION

Pursuant to 35 U.S.C. §§311, 314(a), and 37 C.F.R. §42.100, Cisco Systems, Inc. (“Petitioner”) respectfully requests that the Board review and cancel as unpatentable under (pre-AIA) 35 U.S.C. §103(a) claims 27-28, 31, and 33 (“Challenged Claims”) of U.S. 7,921,323 (the “’323 Patent,” Ex.1001).

The ’323 Patent describes the interconnection of multiple Application Specific Integrated Circuit (“ASIC”) devices, such as Field Programmable Gate Arrays (“FPGAs”), using high speed serial connections. Ex.1001, Abstract. As shown below and confirmed in the Declaration of Dr. Daniel Blumenthal (Ex.1003; *see also* Ex.1004 (Blumenthal CV)), these concepts were known in the prior art well before the priority date of the ’323 Patent. For example, Hartsell (Ex.1005) teaches a content delivery system that utilizes high bandwidth interconnections to communicatively couple the FPGAs of various processing engines. Therefore, the references presented in this Petition teach and render obvious the challenged claims.

Because the Challenged Claims merely recite concepts that were already known, Petitioner asks the Board to institute trial and find the claims unpatentable.

II. GROUNDS FOR STANDING

Petitioner certifies that the ’323 Patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR of the Challenged Claims.

III. NOTE

Petitioner cites to exhibits' original page numbers. **Emphasis** in quoted material has been added. Claim terms are presented in *italics*.

IV. TECHNOLOGY BACKGROUND

Dr. Daniel Blumenthal's Declaration (Ex.1003) provides a background of the relevant technology. Ex.1003, ¶¶29-49 (citing Ex.1021, Ex.1022, Ex.1023, Ex.1024, Ex.1025, Ex.1026, Ex.1027, Ex.1028, Ex.1031).

V. SUMMARY OF THE '323 PATENT

The '323 Patent describes "[r]econfigurable communications infrastructures...implemented to interconnect ASIC devices," e.g., Field Programmable Gate Arrays ("FPGAs"), "using high bandwidth interconnection mediums." Ex.1001, Abstract. "[H]igh speed serial I/O connections...may be employed to interconnect a pair of ASICs to create a high bandwidth, low signal count connection." Ex.1001, 2:53-57. Such systems "may be implemented using a predictable and uniform or standardized interface across the boundaries between each pair of board-level components (e.g., FPGAs, ASICs, general-purpose processors, etc.) to help promote consistent communications[.]" Ex.1001, 4:15-19.

These concepts were well known before the priority date of the '323 Patent.

VI. PROSECUTION HISTORY

The application which led to the '323 Patent was filed November 16, 2006, as U.S. Patent Application No. 11/600,934 as a continuation-in-part of U.S. Patent Application No. 10/843,226, filed May 11, 2004. Ex.1002, 256, 259. The application faced a single office action, rejecting all claims under 35 U.S.C. § 112 because the use of “ASIC device” included “any device that has at least one ASIC chip and/or at least one form of programmable logic chip.” Ex.1002, 61-63. All claims were also rejected as obvious by U.S. Patent No. 7,506,297 to Mukherjee, with the examiner taking official notice of missing elements. Ex.1002, 64-67.

In response, the applicant made significant amendments to the independent claims. Ex.1002, 40-42. The changes to independent claim 27 are provided below:

27. (Currently Amended) A communications infrastructure, comprising two or more ~~ASIC devices~~ separate signal processing circuits, each one of said two or more ~~ASIC devices~~ signal processing circuits including multiple ASIC devices that each itself includes ~~comprising~~ a packet router, said packet router of each one of said ~~two or more~~ ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a each respective packet router of each of the ASIC devices of each other of said two or more ~~ASIC devices~~ signal processing circuits ~~by an interconnection comprising a high speed serial optical link with no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits.~~

Ex.1002, 40-41.

In addition, the applicant argued that the use of the term “ASIC device” in the claims was clear and consistent with the definition of the term. Ex.1002, 44-45, 51-52 (supporting arguments with “ASIC Definition from PC Magazine Encyclopedia”). The applicant also argued against the examiner’s use of official notice in the obviousness rejection. Ex.1002, 46-49. A Notice of Allowance then issued with no additional statements or reasons for allowance provided by the examiner. Ex.1002, 15. The ’323 Patent issued on April 5, 2011. Ex.1002, 9.

VII. EFFECTIVE PRIORITY DATE OF THE ’323 PATENT

The ’323 Patent was filed November 16, 2006, as a continuation-in-part of application 10/843,226, filed May 11, 2004. Determining whether the ’323 Patent is entitled to an earlier priority date is unnecessary in this proceeding, however, as all of the cited and relied-upon prior art predates May 2004. Accordingly, Petitioner does not provide herein a priority date analysis. Petitioner does not waive any right or opportunity it may have to dispute the priority date of the ’323 Patent in this or another forum where the issue is relevant.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A Person of Ordinary Skill in The Art (“POSITA”) in May 2004 would have had a working knowledge of communications infrastructures and the integration of ASIC devices on a fabric interface. A POSITA would have had a master’s degree in computer science, computer engineering, electrical engineering, or an equivalent

training, and approximately four to six years of work experience in the field of communication networks. Lack of work experience can be remedied by additional education, and vice versa. Ex.1003, ¶22.

IX. CLAIM CONSTRUCTION

Claim terms in IPR are construed according to their “ordinary and customary meaning” to those of skill in the art. 37 C.F.R. §42.100(b). Petitioner submits that, for the purposes of this proceeding and the grounds presented herein, no claim terms require express construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). For clarity, however, Petitioner notes below example embodiments and prosecution arguments raised in relation to one term.

a. ASIC devices

Claims 27 and 31 recite “*signal processing circuits including multiple ASIC devices.*” ASIC stands for “Application Specific Integrated Circuit,” and the ’323 Patent explains that ASIC devices include “Field Programmable Gate Arrays (‘FPGAs’) or other field programmable devices (‘FPDs’) or programmable logic devices (‘PLDs’).” Ex.1001, 2:45-50; *see also* Ex.1001, 4:50-53, 10:3-6, 14:49-54, 19:28-35; Ex.1002, 44-46 (applicant arguing that ASIC devices include FPGAs), 51-52 (applicant-provided “ASIC Definition from PC Magazine Encyclopedia” supporting ASIC devices as encompassing FPGAs). The ’323 Patent provides an

example where ASIC devices, provided in the form of FPGA devices, are implemented as “Xilinx Virtex-II Pro® XC2VP50 FPGA device[s].” Ex.1001, 10:3-6, 10:22-24; *see also* Ex.1001, 13:12-19. To the extent Patent Owner would seek to read this example into the claim language, it would have been obvious to a POSITA to use commercially available FPGAs like the Xilinx Virtex-II Pro, as outlined in the analysis below. Ex.1003, ¶¶57-60.

The applicant also referred to an ASIC (specifically an FPGA) in prosecution as a “chip.” To the extent Patent Owner would seek to limit an *ASIC device* to a single semiconductor chip, the prior art discussed below also renders such an interpretation obvious.

X. RELIEF REQUESTED AND THE REASONS FOR THE REQUESTED RELIEF

Petitioner asks the Board to institute trial and cancel the Challenged Claims.

XI. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

A. Challenged Claims

Petitioner challenges claims 27-28, 31, and 33 of the '323 Patent. These claims are asserted against Petitioner in co-pending district court litigation, so a finding that the Challenged Claims are unpatentable at the PTAB will obviate the need for trial in the co-pending litigation, substantially reducing the time and expense of the litigation for all parties.

B. Grounds

Ground	Claims	Basis
#1	27-28, 31, and 33	35 U.S.C. §103 (Pre-AIA) over Hartsell
#2	27-28, 31, and 33	35 U.S.C. §103 (Pre-AIA) over Hartsell and Hauck
#3	27-28, 31, and 33	35 U.S.C. §103 (Pre-AIA) over Hartsell and Raj
#4	27-28, 31, and 33	35 U.S.C. §103 (Pre-AIA) over Hartsell, Hauck, and Raj

U.S. 2002/0059274 (Ex.1005, “Hartsell”) was filed June 12, 2001 and published May 16, 2002.

“The Roles of FPGA’s in Reprogrammable Systems” by Scott Hauck (Ex.1030, “Hauck”) was published April 1998 in Proceedings of the IEEE, vol. 86, no. 4.

U.S. 6,496,291 (Ex.1007, “Raj”) was filed October 17, 2000 and issued December 17, 2002.

Hartsell and Raj are prior art under (pre-AIA) 35 U.S.C. §102(b) and (e).
Hauck is prior art under (pre-AIA) 35 U.S.C. §102(b).

The primary reference applied in this Petition, Hartsell, was not before the Examiner during prosecution of the ’323 Patent. Hauck and Raj were also not considered.

Hartsell, Hauck, and Raj are analogous art to the '323 Patent because each is at least (1) in the same field of endeavor (reconfigurable communication infrastructures); or (2) reasonably pertinent to a problem with which the inventor of the '323 Patent was involved (e.g., high speed serial I/O connections between ASIC devices, such as FPGAs, using a fabric interface). *Compare* Ex.1001, Abstract (“Reconfigurable communications infrastructures may be implemented to interconnect ASIC devices”), 1:14-17 (relating to “interconnection of multiple ASIC devices” such as “Field Programmable Gate Array (FPGA) devices”), 2:41-50 *with* Ex.1005, [0047], [0053] (providing an infrastructure using “multiple system engines...communicatively coupled” to perform “one or more dedicated tasks or sub-tasks associated with the delivery or transmittal of content from one or more content sources to one or more networks”); Ex.1007, 1:55-67 (connecting circuits through high speed optical serial links); Ex.1030, Abstract (“Reprogrammable systems based on field programmable gate arrays are revolutionizing some forms of computation and digital logic.”), 618 (“With this rich sea of routing resources, the Xilinx 4000 series is able to handle fairly arbitrary routing demands, though mappings emphasizing local communication will still be handled more efficiently.”); Ex.1003, ¶63.

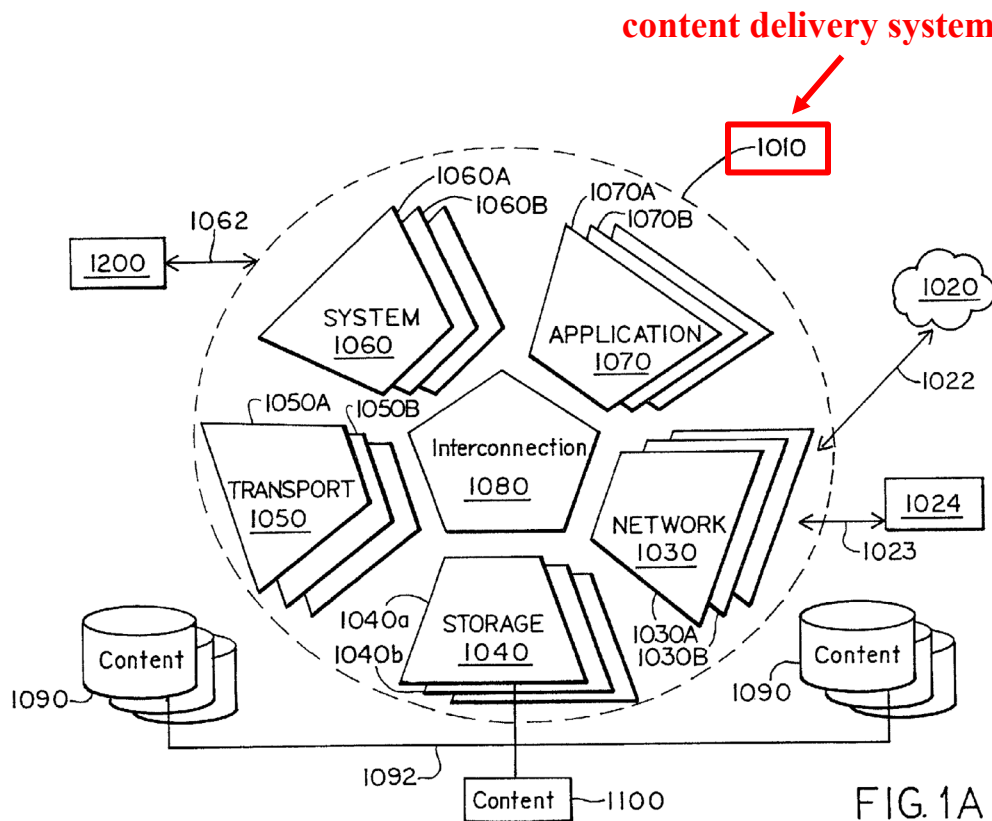
C. Ground 1: Hartsell Renders Obvious Claims 27-28, 31, and 33

1. Claim Analysis

a) Claim 27

[27.1] A communications infrastructure, comprising two or more separate signal processing circuits,

First, Hartsell teaches a content delivery system 1010 that “receives requests for content from remote browser clients via the network, accesses a file system to retrieve the requested content, and delivers the content to the client.” Ex.1005, [0047]. Content delivery system 1010 “includes multiple system engines...communicatively coupled,” which perform “one or more dedicated tasks or sub-tasks associated with the delivery or transmittal of content from one or more content sources to one or more networks.” Ex.1005, [0053]. Fig. 1, below, provides an illustrated example of Hartsell’s content delivery system:



Ex.1005, Fig. 1A (annotated); Ex.1003, ¶65

As described in further detail below, Hartsell’s content delivery system teaches the claimed *communications infrastructure*. Ex.1003, ¶66.

Second, content delivery system 1010 contains multiple “processing modules that may be configured to operate as content delivery engines 1030, 1040, 1050, 1060, and 1070 communicatively coupled via distributive interconnection

1080.” Ex.1005, [0143].¹ “Content delivery engines 1030, 1040, 1050, 1060 and 1070 are present to independently perform selected sub-tasks” where “any one or more of such subtasks may be combined and performed by a single engine, or subdivided to be performed by more than one engine.” Ex.1005, [0055]. Various numbers and configurations of content delivery engines are employed in content delivery system 1010 “to fit particular needs of a given application or installation.” Ex.1005, [0054]. For example, Hartsell’s content delivery system includes one or more transport processing engines 1050, each of which is a *signal processing circuit*. Ex.1005, [0071]-[0072], [0123]; Ex.1003, ¶67.

It would have been obvious to implement Hartsell’s content delivery engine, like transport processing engine 1050, as a *circuit* because Hartsell explains that each of its content delivery engines, including transport processing engine 1050, “generally includes any hardware...capable of **performing one or more dedicated tasks** or subtasks[.]” Ex.1005, [0053]; Ex.1003, ¶68; *see also* Ex.1009, 90 (Microsoft Computer Dictionary defining *circuit* as “[a] combination of

¹ Hartsell refers to element 1080 as both “interconnection 1080” and “interconnect 1080.” *Compare* Ex.1005, [0058], *with* Ex.1005, [0059]. For consistency, this Petition uses “interconnect 1080” unless directly quoting from Hartsell.

electrical components interconnected to perform a particular task”). It was also well-known and common to implement such computer-centric technologies using a *circuit*. Ex.1003, ¶68; *see also* Ex.1015, 15:56-59 (listing a “forwarding engine” as a type of “integrated circuit...which determines the destination of a packet”). Hartsell elaborates that transport processing engine 1050 “may employ one or more independent processor modules (e.g., CPU modules) having independent processor and memory subsystems and **suitable for performance of a given function[.]**” Ex.1005, [0055]; Ex.1003, ¶68.

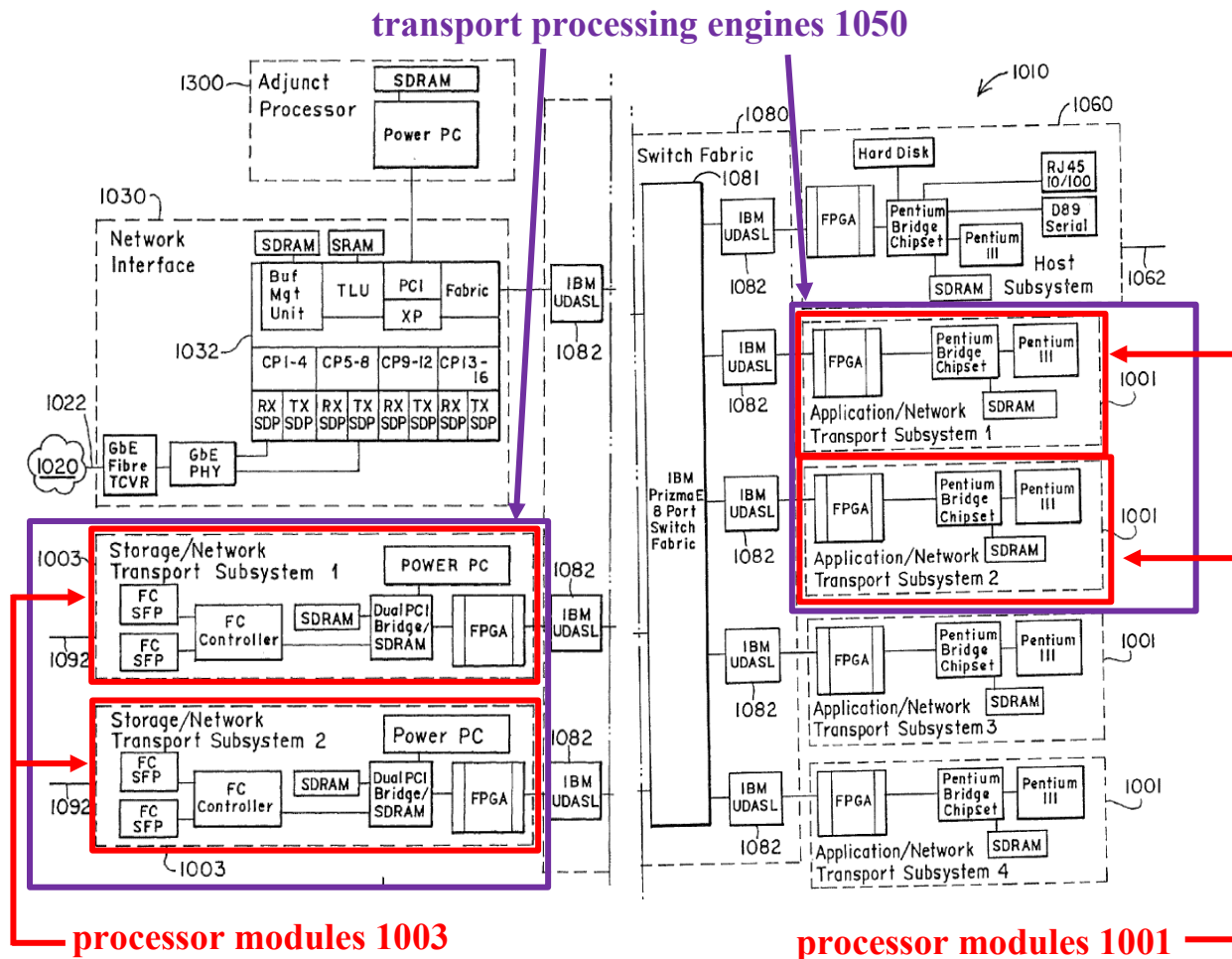
Hartsell explains that transport processing engine 1050 “performs transport and protocol processing” and “may be any hardware...subsystem suitable for TCP/UDP processing, other protocol processing, transport processing, etc.” Ex.1005, [0071]-[0072]. Hartsell further explains how a transport processing engine 1050 facilitates and engages in data communications activities, since “content may also be routed through transport processing engine 1050,” so as “to fulfill requests from one or more clients[.]” Ex.1005, [0123]. Because data is commonly communicated within and between computer systems (e.g., delivering requested content) in the form of a signal, it would have been obvious to a POSITA that Hartsell’s transport processing engine 1050 performs *signal processing*. Ex.1003, ¶69.

Accordingly, Hartsell’s transport processing engine 1050, which comprises hardware configured to perform transport and protocol processing or to route TCP/UDP content data signals, renders obvious a *signal processing circuit*. Ex.1003, ¶70.

Hartsell also describes a “network interface processing engine 1030” that performs a variety of network protocol stack operations, such as “handling queue management, buffer management, TCP connect sequence, checksum, IP address lookup, internal load balancing, packet switching, etc.” Ex.1005, [0063]; *see also id.* [0075]-[0084]. Hartsell suggests combining the functions of network interface processing engine 1030 with those of the transport processing engine 1050. Ex.1005, [0084]. Thus, as an alternative mapping of the claim language to the prior art, the combination of network interface processing engine 1030 and transport processing engine 1050 render obvious a *signal processing circuit*[]. Ex.1003, ¶71.

Third, Hartsell’s content delivery system comprises two transport processing engines that operate individually (*two or more separate signal processing circuits*). Hartsell’s content delivery engines utilize “processor modules 1001 and 1003” that are configured “to implement the content delivery processing engines” 1030, 1040, 1050, 1060, and 1070. Ex.1005, [0150]-[0151]. In other words, the processor modules 1001 and 1003 are flexibly reconfigurable to perform a variety of functions, including operating as transport processing engines

1050 and network interface processing engines 1030. Figure 1C, below, shows “one possible network content delivery system hardware configuration” where “[f]our processor modules 1001 may be configured to operate as...the transport processing engine 1050,” and “[t]wo processor modules 1003 may operate as...the transport processing engine 1050.” Ex.1005, [0020], [0143]. As with the transport processing engine 1050, Hartsell contemplates having “two or more individual network interface processing modules 1030a and 1030b.” Ex.1005, [0105]. Hartsell further explains that the “processor modules 1001 and 1003 of FIG. 1C may be configured in alternative manners to implement the content delivery processing engines such as the network interface processing engine 1030....” Ex.1005, [0151]. Thus, Hartsell contemplates multiple processor modules acting together as one transport processing engine, and Hartsell further contemplates that the content delivery system may include multiple transport processing engines and network interface processing engines. Ex.1003, ¶72.



Ex.1005, Fig. 1C (combining Figs. 1C' and 1C'', annotated); Ex.1003, ¶72

Hartsell explains that the processor modules of each transport processing engine 1050 and network interface processing engine 1030 have “independent processor and memory subsystems...suitable for performance of a given function[.]” Ex.1005, [0055]. Thus, each processor module 1001 or 1003 has its own independent components “allowing independent operation without interference from other engines or modules”. Ex.1005, [0055]. Further, Hartsell notes that “[a]ny two modules of a given engine may communicate with **separate**

modules of another engine or may communicate with the same module of another engine.” Ex.1005, [0120]. Accordingly, “content delivery system 1010 is capable of providing multiple dedicated and independent processing engines...each of which is substantially self-contained.” Ex.1005, [0053].

Since each processor module 1001 or 1003 operates independently, it would have been obvious to a POSITA that one transport processing engine 1050 (e.g., composed of processor modules 1001) would operate independently from another transport processor engine 1050 (e.g., composed of processor modules 1003). Ex.1003, ¶74. Hartsell’s two transport processing engines 1050, which operate independently, therefore render obvious *two or more separate signal processing circuits*. Ex.1003, ¶74. As previously noted, Hartsell contemplates that transport processing engine 1050 may be integrated with the functionality of the network interface processing engine 1030. Ex.1005, [0084].

In summary, Hartsell’s teaching of content delivery system 1010 coupled to a network (*communications infrastructure*) including two transport processing engines 1050 (alone or together with network interface processing engines 1030) that each employ respective processor modules to allow independent operation from other system engines (*comprising two or more separate signal processing circuits*) renders obvious this limitation. Ex.1003, ¶75.

[27.2] each one of said two or more signal processing circuits including multiple ASIC devices that each itself includes a packet router,

As discussed in [27.1], Hartsell's two transport processing engines 1050 (signal processing circuits) each include a plurality of processor modules 1001 and 1003. Ex.1003, ¶¶76, 72. These plurality of processor modules render obvious multiple ASIC [(Application-Specific Integrated Circuit)] devices because, as detailed further below, each processor module is a device that includes an FPGA (ASIC device). Ex.1003, ¶76.

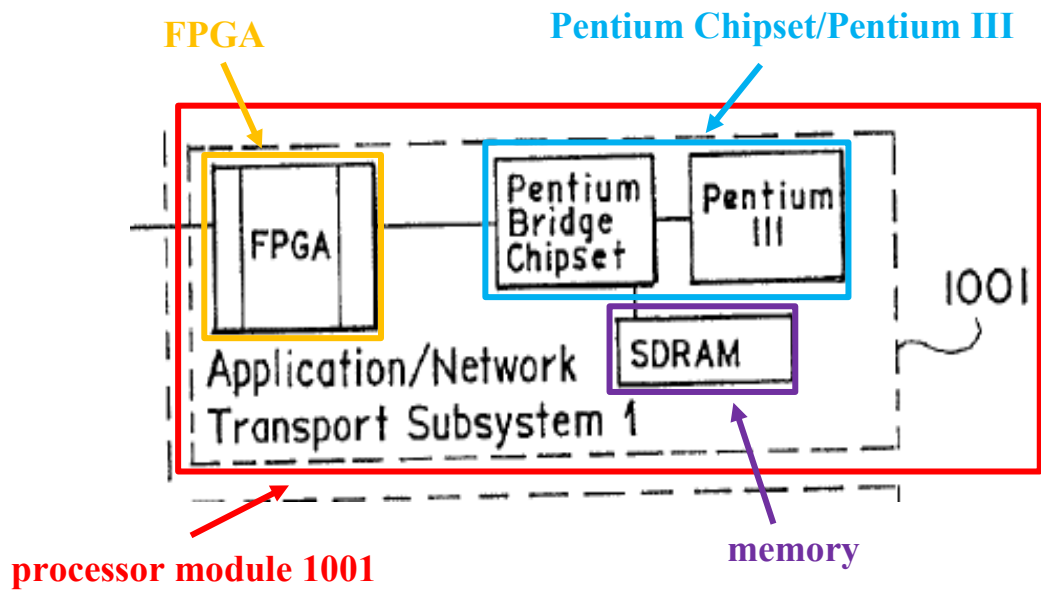
First, Hartsell's processor modules² 1001 and 1003 are *ASIC devices* because they are application-specific devices that include an FPGA. The '323 Patent explains that it relates to "interconnection of multiple ASIC devices, for example, multiple Field Programmable Gate Array (FPGA) devices." Ex.1001, 1:14-17. While the '323 Patent does not provide an explicit definition of *ASIC*

² Hartsell uses "processor modules" to refer to modules 1001 and 1003, and "processing modules" to refer to implementations of the processor modules as, e.g., modules 1030a and 1030b, 1040a and 1040b, and 1050a and 1050b. For consistency, this Petition solely uses the term "processor modules" outside of directly quoted language.

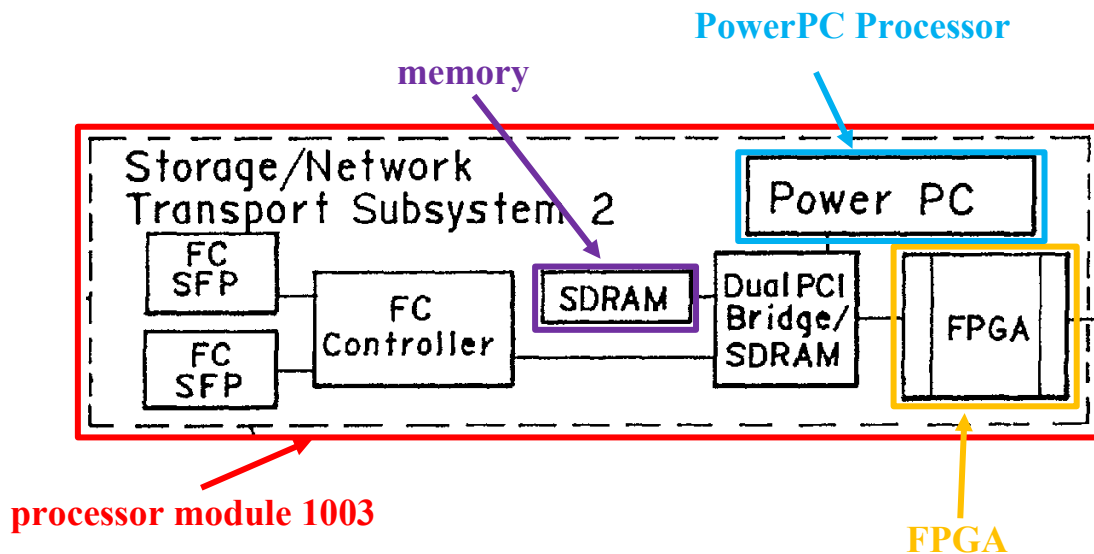
device, it consistently equates ASIC devices and FPGA devices. *E.g.*, Ex.1001, 5:32-36, 10:3-6, 16:26-29, 19:44-50, 21:6-12, 23:15-24, 25:26-32.

Hartsell's processor modules 1001 and 1003, as shown in Fig. 1, comprise (1) a field-programmable gate array ("FPGA"), connected to (2) a Pentium Chipset/Pentium III (or a PowerPC processor), and (3) memory.³ Figure 1C, below, provides examples of processor module 1001 and processor module 1003:

³ Hartsell describes processor module 1003 as also including various fibre channel components that are used "when the processor module 1003 is utilized as a storage processing engine 1040." Ex.1005, [0149]. Since these fibre channel components are not present in processor module 1001, it would have been obvious to a POSITA that the fibre channel components are not needed as part of processor module 1003 when processor module 1003 is used as a transport processing engine 1050. Ex.1003, ¶78.



Ex.1005, Fig. 1C (partial view, annotated); Ex.1003, ¶78



Ex.1005, Fig. 1C (partial view, annotated); Ex.1003, ¶78

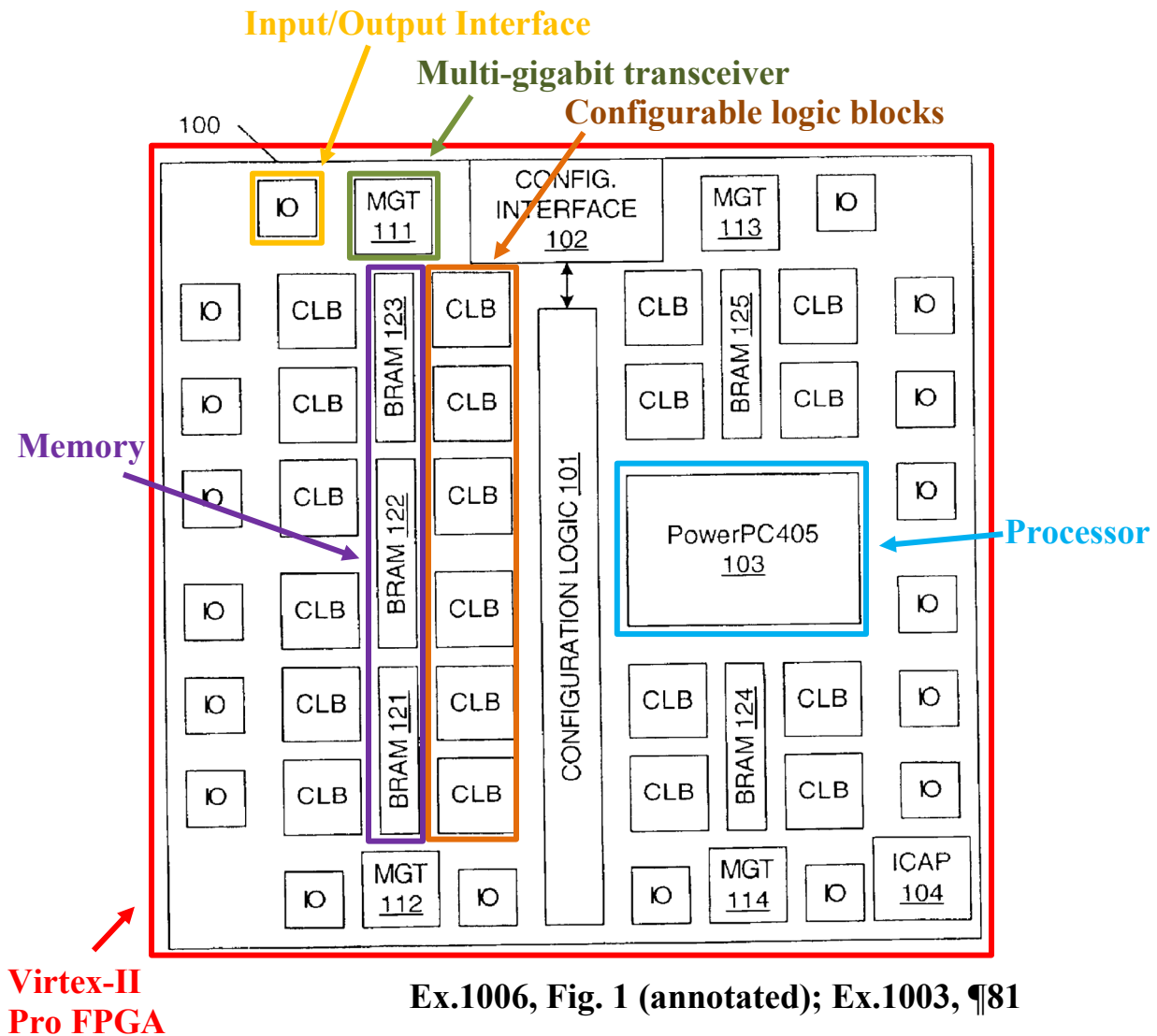
Hartsell discloses that each of the processor modules may use “any processor suitable for adapting to endpoint processing...such as...the PowerPC processor.” Ex.1005, [0055], [0072] (“In one embodiment transport engine 1050

may be a dedicated TCP/UDP processing module based on an INTEL PENTIUM III or MOTOROLA POWERPC 7450 based processor....”); Ex.1003, ¶79. The ’323 Patent similarly contemplates embodiments where PowerPC processors are embedded on an FPGA device (*ASIC device*), along with memory and additional programmable gates that can be configured to perform different tasks such as a data interface. Ex.1001, 1:33-50 (describing “system-level FPGAs with embedded Power PC” in the context of “current commercial products”), 10:22-35 (“FPGA devices 102, 104, 106, and 108 may be a Xilinx Virtex-II Pro® XC2VP50 FPGA device”); Ex.1003, ¶79.

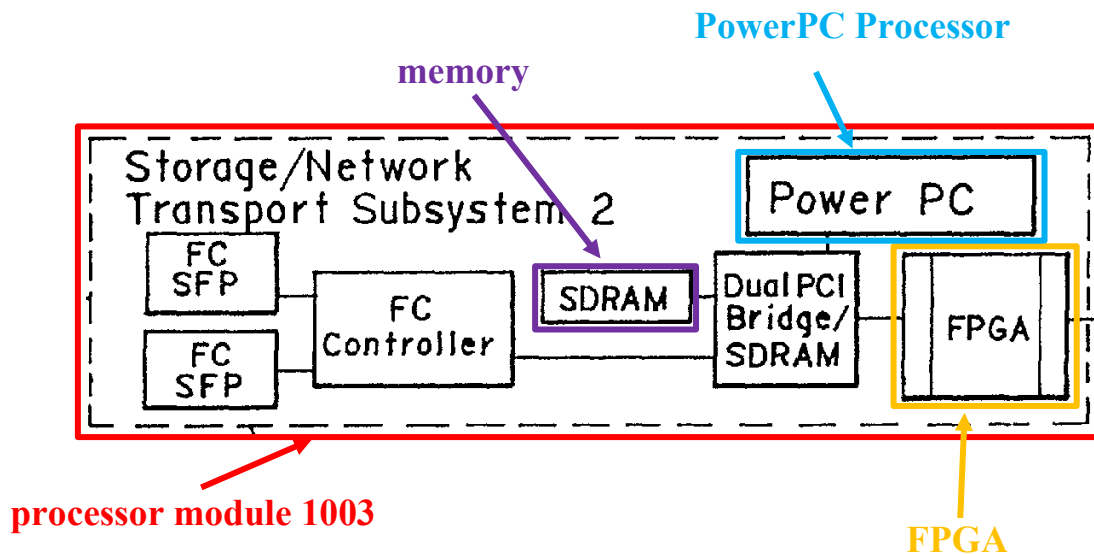
To the extent that Patent Owner argues that the claimed *ASIC devices* need to be implemented on a single integrated chip, well-known FPGA devices at the time of the ’323 Patent also include the components found in Hartsell’s processor modules 1001 and 1003, such as memory and a processor, incorporated into an integrated solution. For instance, the ’323 Patent points to Xilinx Virtex-II Pro FPGAs as an example of an ASIC device. Ex.1001, 10:3-6 (“[M]ultiple ASIC devices may be provided on a single circuit card, in this exemplary embodiment in the form of four FPGA devices”) 10:22-28 (“[E]ach of [the four] FPGA devices...may be a Xilinx Virtex-II Pro® XC2VP50 FPGA device”). Xilinx documentation confirms that the Virtex-II Pro FPGA family contains the same components contemplated by Hartsell for processor modules 1001 and 1003 in a

single FPGA device. *See* Ex.1010, 1-2 (describing the technical specifications of the Xilinx Virtex-II Pro FPGA family); Ex.1003, ¶80. The Virtex-II Pro FPGA family members include “user-configurable supporting circuitry,” an “on-chip processor,” and “on-chip memory.” Ex.1011, 17-18 (Virtex-II Pro FPGA “incorporate[s] both serial transceiver technology and a hard processor core,” e.g., a PowerPC Processor, “within a general-purpose FPGA device.”); Ex.1010, 1 (providing technical specifications for the ten members of the Virtex-II Pro family); *see also* Ex.1006, 1:14-31 (describing conventional FPGAs), 1:31-39 (describing Xilinx documentation relating to the Virtex-II Pro family in relation to conventional FPGAs); Ex.1012, 1-2, 947 (Internet Archive affidavit accompanying captures of Exhibit 1010 and Exhibit 1011).

For instance, Curd (Ex.1006) illustrates the major components of a Virtex-II Pro FPGA device, including input/output interfaces, multiple multi-gigabit transceivers, configurable logic blocks and configuration logic (together providing the device’s field-programmable functionality), and a PowerPC processor. Ex.1003, ¶81. These components are reflected in Figure 1, below:



The components substantially correspond to the same components described by Hartsell as being part of its processor modules 1001 and 1003, such as a PowerPC processor, memory, and input/output (I/O) interfaces, multi-gigabit transceivers, configurable logic blocks, and configuration logic (collectively forming an FPGA). Ex.1003, ¶82.



Ex.1005, Fig. 1C (partial view, annotated); Ex.1003, ¶82

In short, Curd confirms that the Xilinx Virtex-II Pro FPGA device was a commercially available product that included all of the components and functionality required by Hartsell's processor modules 1001 and 1003. Ex.1003, ¶83. Each component of Hartsell's processor modules 1001 and 1003 corresponds to functionality included in a Xilinx Virtex-II Pro FPGA device. Accordingly, it would have been obvious to a POSITA that to the extent the claimed *ASIC devices* need to be implemented on a single integrated chip, Hartsell's processor modules 1001 and 1003 would have been implementable as single integrated chip devices such as the known and commercially available Xilinx Virtex-II Pro FPGA devices. Ex.1003, ¶83. Further, by implementing Hartsell's processor modules as FPGA devices, the processor modules necessarily are *ASIC devices* because FPGAs are

ASIC devices, as confirmed by the '323 Patent and '323 File History. *See* Ex.1001, 2:45-50 (noting that FPGAs are examples of *ASIC devices*); Ex.1002, 44-46 (applicant arguing same during prosecution); Ex.1003, ¶83.

A POSITA would have been motivated to implement Hartsell's processor modules as single integrated chip FPGA devices, such as a Xilinx Virtex-II Pro implementation of Hartsell's processor modules, because such an implementation would lower the manufacturing cost (e.g., using an already-designed and -tested embedded processor on an FPGA device instead of creating a custom integration of a separate CPU such as Pentium III or PowerPC and a separate FPGA device), save circuit area, and thus improve production and operation efficiency. Ex.1011, 18 (“[U]sing a separate processor externally requires hundreds of additional interface pins, which degrades system performance and significantly increases FPGA I/O requirements and overall board costs.”), 17 (“cost savings com[e] from faster time-to-market, reduced printed circuit board (PCB) complexity, and lower component count”); Ex.1008, 175 (discussing cost advantages of Xilinx Virtex-II Pro FPGAs); Ex.1003, ¶84. Additionally, use of an off-the-shelf single chip integrated circuit FPGA, such as a Xilinx Virtex-II Pro FPGA device, would result in reduced complexity and faster time-to-market by employing an off-the-shelf component instead of designing, prototyping, testing, and manufacturing custom modules as originally suggested by Hartsell. Ex.1011, 17 (discussing Virtex-II Pro

FPGA technology providing costs savings from “faster time-to-market, reduced printed circuit board (PCB) complexity, and lower component count”); Ex.1003, ¶84.

The use of single integrated chip FPGA devices, such as Xilinx Virtex-II Pro FPGAs, to implement Hartsell’s content delivery system 1010 is also consistent with Hartsell’s discussion of using “modular” components. Ex.1003, ¶85. Hartsell discusses “modular” multi-task configuration of its content delivery system 1010 for easy customization of the system. Ex.1005, [0045], [0055]. Hartsell teaches the use of “modular processing engines,” each “provided with one or more discrete subsystem modules.” Ex.1005, [0045]. This modular configuration “allows the number and/or type of content delivery engines and processors to be selected or varied to fit the needs of a particular application.” Ex.1005, [0055]. Ex.1003, ¶85.

Thus, a POSITA would have been motivated to implement each “modular” processor module 1001 or 1003 of Hartsell using a single integrated chip FPGA device, such as a Xilinx Virtex-II Pro FPGA, such that each processing module is a single integrated circuit (e.g., a single semiconductor chip). *See* Ex.1006, Fig. 1; Ex.1003, ¶86. Doing so would support and further enhance the modular structure Hartsell intends to achieve. Each “modular” processing module integrated on a single FPGA device can be easily installed or replaced in the content delivery

system when the “number and/or type of content delivery engines and processors” varies to “fit the needs of a particular application.” Ex.1005, [0055]. Ex.1003, ¶86.

In addition, a POSITA would have been motivated to implement processor module 1001 or 1003 as a single integrated chip FPGA device, such as a Xilinx Virtex-II Pro FPGA, because such FPGAs supported superior circuit performance at the time of the '323 Patent. Ex.1010, 17-18; Ex.1003, ¶87. By implementing Hartsell's processor modules 1001 and 1003 as single integrated chip FPGA devices, such as Xilinx Virtex-II Pro FPGAs, Hartsell's content delivery system 1010 would achieve high transmission rates and compatibility of a variety of I/O technologies. Ex.1010, 2 (Virtex-II Pro devices support transmission rates of “622 Mbps to 3.125 Gbps per channel”), 4 (noting the advantages of Xilinx FPGAs “for customers who still need to support their differential or single-ended legacy bus architectures as they transition to serial architectures” with compatibility and support for “all the popular standards”). Such benefits would have motivated a POSITA to implement Hartsell's processor modules 1001 and 1003 as single integrated chip devices such as the known Xilinx Virtex-II Pro FPGA devices. Ex.1003, ¶87.

In addition, Hartsell's processor modules 1001 and 1003 (*ASIC devices*) are each dedicated to perform specific tasks. Content delivery system 1010 is configurable such that “any given processing engine of content delivery system

1010,” such as transport processing engine 1050 or network interface processing engine 1030, is “provided with multiple processing modules so as to enable parallel or redundant processing of data and/or communications.” Ex.1005, [0105]; Ex.1003, ¶88. These processor modules are application specific because they are dedicated and optimized for specific functions. Ex.1005, [0107] (noting that in some embodiments, processor modules are “specialized to specific applications”); Ex.1003, ¶88. For instance, “two or more **individual dedicated TCP/UDP processing modules** 1050a and 1050b,” shown in Fig. 1C as processor modules 1001 or 1003, “may be provided for transport processing engine 1050[.]” Ex.1005, [0105], [0053] (“content delivery system 1010 is capable of providing **multiple dedicated** and independent processing engines that are optimized for networking”); Ex.1003, ¶88.

Hartsell’s content delivery engines employ processor modules (each with their own processor and memory subsystems) to perform particular sub-tasks and operate independently. Ex.1005, [0055]. For instance, Hartsell’s transport processing engine off-loads tasks from other processing engines to handle application-specific tasks and to free up resources of other processing engines:

The transport processing engine 1050 may perform time out checks for each network connection, session management, data reordering and retransmission, data queuing and flow control,

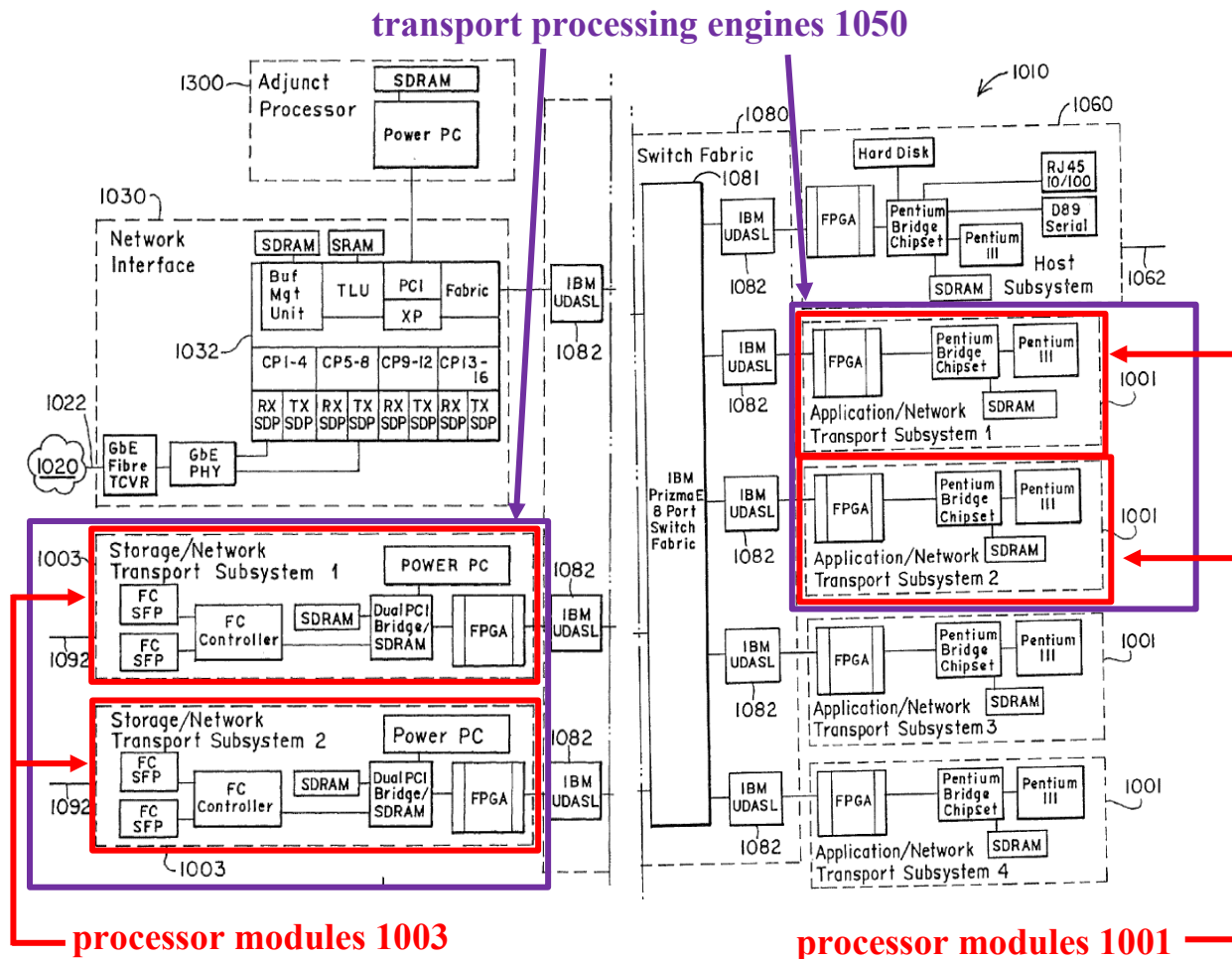
packet header generation, etc. off-loading these tasks from the application processing engine or the network interface processing engine. The transport processing engine 1050 may also handle error checking, likewise freeing up the resources of other processing engines.

Ex.1005, [0073]; *see also id.* [0135] (“Each engine may also be tailored in hardware and/or software to **perform specific content delivery task[s]**, thereby providing increasing content delivery speeds while requiring less system resources.”); Ex.1003, ¶89.

Accordingly, Hartsell’s processor modules 1001 and 1003, configured to operate as transport processing engines 1050 (and, alternatively, further configured to operate as network interface processing engines 1030), are application-specific devices that contain FPGAs (*ASIC devices*). Ex.1003, ¶90.

Second, Hartsell’s processor modules (*ASIC devices*) *each itself includes a packet router* because each processor module controls packet routing. Ex.1003, ¶91.

Hartsell explains that “[a]ny two modules of a given engine,” such as processor modules 1003 on the left-hand side in FIG. 1C’, “may communicate with separate modules of another engine or may communicate with the same module of another engine,” such as processor modules 1001 on the right-hand side in FIG. 1C”. Ex.1005, [0120]; Ex.1003, ¶92.



Ex.1005, Fig. 1C (combining Figs. 1C' and 1C'', annotated); Ex.1003, ¶92

A POSITA would have recognized that Hartsell's processor modules 1001 and 1003 would have operated as a *packet router* in the same way as the FPGAs described in the '323 Patent because the processor modules 1001 and 1003 are used to process packets and communicate packets to other processor modules 1001 and 1003. Ex.1003, ¶93. Indeed, Hartsell explains that its transport processing engines 1050 (which are implemented via multiple processor modules 1001 or 1003) “may perform time out checks for each network connection, session

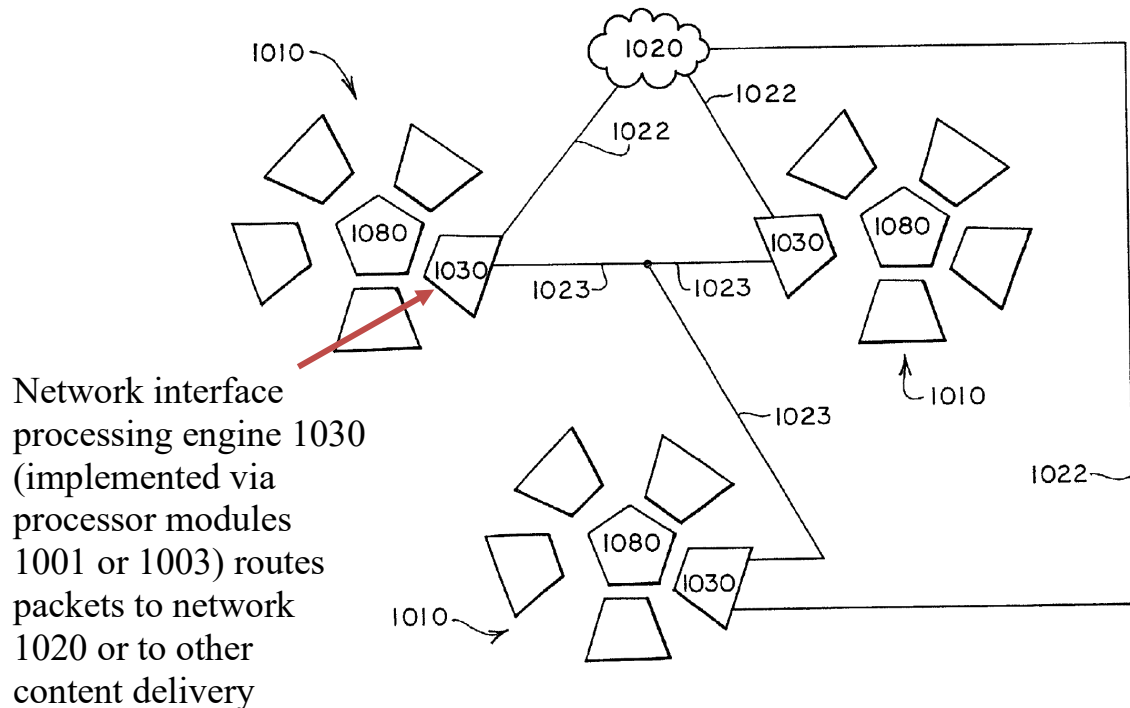
management, data reordering and retransmission, data queuing and flow control, packet header generation, etc.” Ex.1005, [0073]. Each processor module also includes an FPGA, and a POSITA would have configured the FPGAs of processor modules 1001 and 1003 to perform desired functionality, including performing routing functions, in light of Hartsell’s disclosure of the transfer of packets between engines in content delivery system 1010. Ex.1005, [0078] (discussing the transfer of packets between engines); Ex.1003, ¶93.

Hartsell further contemplates processing engine configurations that are “distributively interconnected across a network,” including configurations where processing engines are “physically remote” from one another. Ex.1005, [0275]; Ex.1003, ¶94. Data is communicated between Hartsell’s transport processing engines in the form of data packets. Ex.1005, [0072]-[0073], [0078] (discussing TCP/UDP processing and the transfer of packets “between the two engines”). “Routing of requests...may be controlled by transport and/or interface processing modules,” such as Hartsell’s processor modules 1001 and 1003. Ex.1005, [0107]. Each processor module performs the routing of requests in parallel with one or more additional processor modules. Ex.1005, [0105]; Ex.1003, ¶94. For example, Hartsell describes filtering requests, indicating that some processor modules decide whether to forward a request packet or to drop the request packet, for example, because the request cannot be fulfilled. Ex.1005, [0103] (“The network interface

engine may also be used to filter requests that are not supported....”), [0100], [0169] (“to filter out requests that the receiving system is not capable of processing”), [0190] (“...the request for content may be filtered at step 110 by, for example, one or more processing engines or modules...”).

Hartsell’s disclosure—with processor modules that comprise network interface and transport processing engines that control the routing of packetized data requests—renders obvious a *packet router* included within each processor module (*ASIC device*). As each processor module 1001 or 1003 is capable of routing and processing content requests (e.g., packets) independently, it would have been obvious for each transport processing module 1001 or 1003 to include a *packet router*. Ex.1003, ¶95; *see also* Ex.1005, [0123] (discussing routing content through transport processing engine 1050). For example, it would have been obvious for the processor (e.g., PowerPC) of each processor module 1001 or 1003 to act as a *packet router* because the processor module 1001 or 1003 operates to send packets to other processor modules 1001 or 1003, or even to a different system altogether. Ex.1003, ¶95. Hartsell illustrates in Figs. 1G and 1H, for example, that multiple systems 1010 can be coupled together and to a network 1020 via network interface processing engines 1030, which are implemented via processor modules 1001 or 1003. Ex.1005, [0151]. Hartsell describes this as a “cluster arrangement” of systems 1010. Ex.1005, [0112]. Hartsell also

contemplates that the network interface processing engine 1030 may be combined with the transport processing engine 1050. Ex.1005, [0084]; Ex.1003, ¶95.



Ex.1005, Fig. 1H (annotated); Ex.1003, ¶95

Alternatively, the incorporation of the network interface processing engine 1030 into the transport processing engine 1050 further renders obvious the claimed *packet router*. Ex.1005, [0084]. The “network interface engine 1030 may process[] all or some of the TCP/IP protocol stack.” Ex.1005, [0075]. The network interface engine 1030 receives TCP/IP packets and strips their header information, replacing it with an identifier or tag that is used to route the packet within Hartsell’s system. Ex.1005, [0066], [0080], [0126]; Ex.1003, ¶96.

The '323 Patent's disclosure confirms that Hartsell's processor module 1001 or 1003 would operate as a *packet router*. Ex.1003, ¶97. The '323 Patent explains that any routing scheme, including TCP/IP and Infiniband, would involve a *packet router*. Ex.1001, 22:49-23:8 (“[I]t will be understood that any other data packet configuration and routing scheme suitable for allowing a sender or source to determine the packet's destination within a reconfigurable communications infrastructure 1300 may be employed (e.g., TCP/IP, Fibrechannel, XAUI, Ethernet, Infiniband, Rapid I/O, etc.)”). Similarly, Hartsell teaches communications among the processor modules 1001 and 1003 may use of any interconnect protocol, such as Infiniband. Ex.1005, [0275]. A POSITA would have understood that the Infiniband protocol transmits data in the form of packets. Ex.1003, ¶97 (citing Ex.1013, Abstract (discussing switching Infiniband data packets); Ex.1014, Abstract (discussing converting ATM cells to Infiniband packets)).

Thus, the combination would result in processor modules 1001 or 1003 performing routing of Infiniband packets, which also renders obvious that each processor module 1001 or 1003 *includes a packet router*. Ex.1003, ¶98.

Therefore, Hartsell renders obvious this limitation.

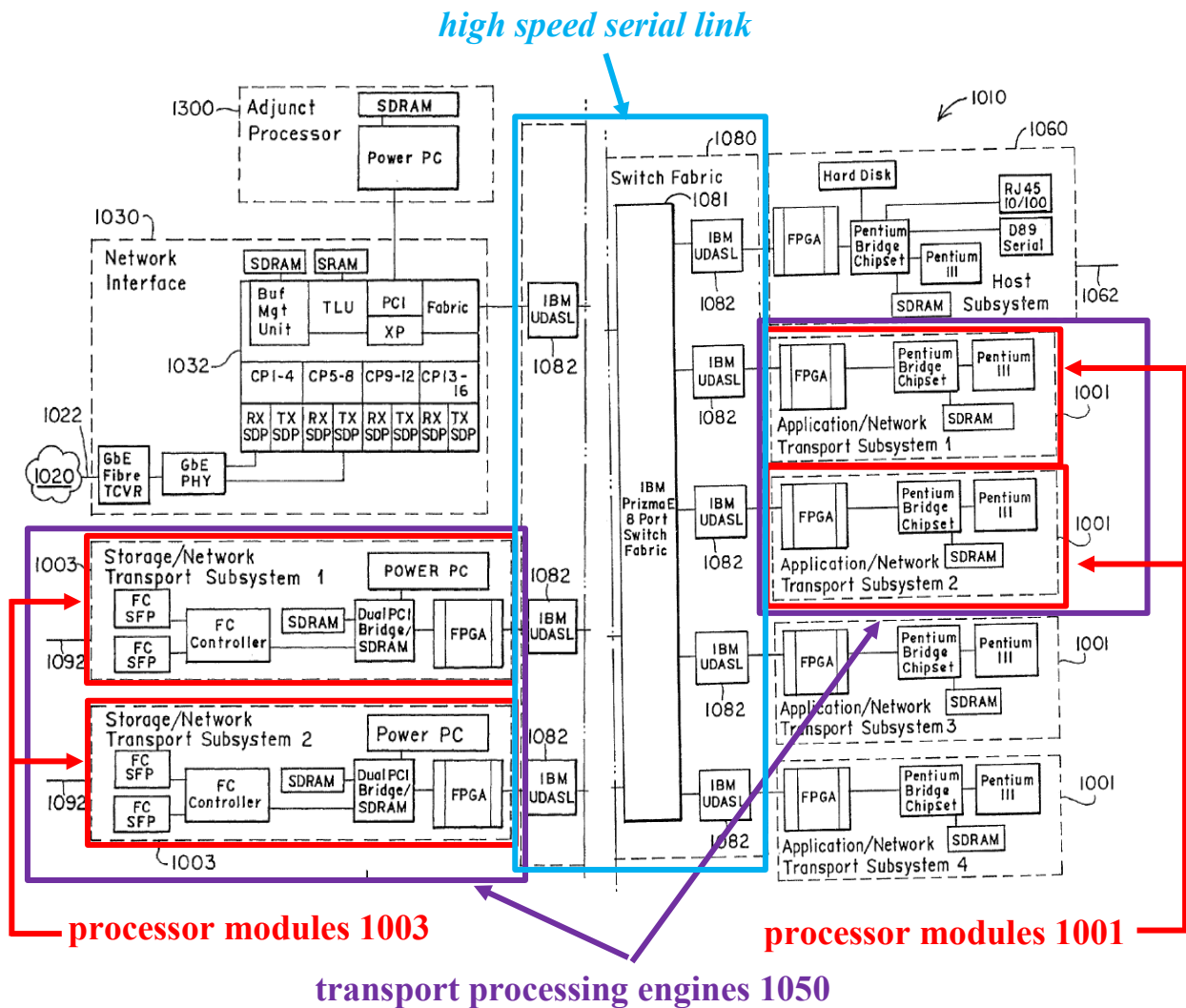
[27.3] said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a respective packet router of each of the ASIC devices of each other of said two or more signal processing circuits

First, as discussed in [27.1]-[27.2], Hartsell teaches that one transport processing module (such as processor module 1001 or 1003) in a transport processing engine is **communicatively coupled** to another transport processing module in another transport processing engine. Ex.1005, [0143]; Ex.1003, ¶100. A POSITA would have understood that these processor modules are *ASIC devices*. Ex.1003, ¶100. And each processor module includes a *packet router* for routing requests and data between the transport processing engines. *See supra*, [27.2]; Ex.1003, ¶100.

Second, Hartsell renders obvious that the processor modules (each of which comprises a *packet router*) are coupled via an *intervening high speed serial optical link*, as further detailed below. Ex.1003, ¶101.

Hartsell's processor modules are coupled to other processor modules by a node-to-node link in interconnect 1080. Ex.1005, [0058] ("distributive interconnection 1080 may be any...high speed interchange system[] such as a switch fabric"), [0144] ("the distributive interconnect 1080 may be a switch fabric based interconnect"); Ex.1003, ¶102. As shown in Fig. 1C, below, interconnect 1080 interconnects transport processing engines 1050 and their processor modules

1001 and 1003. *See* Ex.1005, [0058] (“a switch fabric establishes independent paths from node to node”), [0144] (“the switch fabric 1081 may be coupled to the individual processor modules through interface converter circuits 1082”); Ex.1003, ¶102.



Ex.1005, Fig. 1C (combining Figs. 1C' and 1C'', annotated); Ex.1003, ¶102

Interconnect 1080 includes node-to-node path links that connect one processing module to another processing module and transmit data bit-by-bit serially over “data aligned serial link interfaces.” Ex.1005, [0143]-[0144]; Ex.1003, ¶102. This node-to-node path link is a *high speed serial link* because interconnect 1080 is an “8x3.54 Gbps fabric” in eight port mode, and a “16x1.77 Gbps fabric” in sixteen port mode. Ex.1005, [0144]; Ex.1003, ¶102; *see also* Ex.1001, 6:2-7 (characterizing “high bandwidth interconnection mediums” as those transmitting data at or above “1 gigabit per second (Gbps)”), 20:60:67 (same).

Further, it would have been obvious to a POSITA to use a *serial optical link* as the node-to-node path link connecting one processor module to another. Ex.1003, ¶103. Hartsell teaches that its processing engines can be interconnected via “optical interconnect technology,” such as Infiniband. Ex.1005, [0275]; *see also supra*, [27.2]. Connecting Hartsell’s processor modules via “optical interconnect technology” renders obvious the claimed *intervening high speed serial optical link*.

Alternatively, to the extent the claimed *intervening high speed serial optical link* requires a single bidirectional link as described in embodiments of the ’323 Patent, it would have been obvious to implement interconnect 1080 as a bus. A POSITA would have been motivated to connect the processing engines in Hartsell’s content delivery system 1010—and thus each of Hartsell’s processor

modules 1001 and 1003—using a single bidirectional bus. Ex.1003, ¶104. Hartsell encourages such an implementation because it teaches that “distributive interconnection 1080 may be any multi-node I/O interconnection hardware or hardware/software system” including a “bus architecture.” Ex.1005, [0058]. Hartsell explains that “a ‘bus’ is any system bus that carries data in a manner that is visible to all nodes on the bus.” Ex.1005, [0058]. Thus, in a bus architecture, a single link (the shared bus) would be used for communications between any two processor modules. Skilled artisans were using bus architectures to facilitate communications between and among FPGAs prior to the priority date of the ’323 Patent. Ex.1003, ¶104 (citing Ex.1030, 628 (describing a “linear array of FPGA’s [] augmented with a global bus”)).

A POSITA would have coupled each of Hartsell’s processor modules 1001 and 1003 (*ASIC devices* containing FPGAs) using a bus because Hartsell provides a teaching, suggestion, or motivation to implement interconnect 1080 as a bus architecture. Ex.1005, [0058] (teaching that processing engines are interconnected by a “bus architecture”); Ex.1003, ¶105. Buses provide a single bidirectional link, such as is described in embodiments of the ’323 Patent. Ex.1003, ¶105 (citing Ex.1029, 1:54-2:4 (providing “an advanced bus structure” for bidirectional optical routing of information); Ex.1001, Fig. 13, 19:24-28 (describing a “high bandwidth interconnection medium 1350 to enable high bandwidth bi-directional

communications”)). A POSITA would have recognized that a bus architecture would have been capable of interconnecting Hartsell’s processor modules using “optical interconnect technology.” *See* Ex.1005, [0275]; Ex.1029, 2:33-41 (describing an “optical bus interface module” to facilitate device communication over fiber optic transmission lines); Ex.1003, ¶105. Bus architectures are easier to deploy, and present cost savings, over alternative architectures. Ex.1003, ¶105. And Hartsell confirms that a bus architecture is a “high speed interchange system[],” thus maintaining the high speed advantages of Hartsell’s switch fabric implementation discussed directly above. Ex.1005, [0058]; Ex.1003, ¶105.

A POSITA would have had a reasonable expectation of success in implementing Hartsell’s distributive interconnect 1080 as a bus architecture because, as explained above, such architectures were known in the art, and Hartsell intended for its content delivery systems to be implementable using bus architectures. Ex.1005, [0058]; Ex.1003, ¶106. Accordingly, it would have been obvious to a POSITA to implement content delivery system 1010 such that each processing engine and corresponding processor modules 1001 and 1003 were interconnected using a single bidirectional bus. Ex.1003, ¶106.

Third, Hartsell renders obvious that each of its processor modules (each comprising a *packet router*) would be coupled via an *intervening high speed serial*

optical link to another processor module through fabric interfaces (*first and second common interfaces*). Ex.1003, ¶107.

Hartsell describes an interface 34 located between interconnect 1080 and each processor module 1001 and 1003. Ex.1005, [0144] (“interface 34 provides an interface between the processor module bus and the UDASL switch interface converter circuit 1082 [within interconnect 1080]”), Fig.4; Ex.1003, ¶108.

Hartsell’s interface 34 for each processor module 1001 or 1003 renders obvious the *first and second common interfaces*. Ex.1003, ¶108. Alternatively, Hartsell’s UDASL switch interface converter circuit 1082⁴ may be considered part of each processor module’s *common interface* rather than part of the *high speed serial... link*. In view of Hartsell’s suggestion to modify interconnect 1080 (in either a switch fabric or bus implementation) to use optical communication technology, it would have been obvious to incorporate suitable optical transceiver functionality into interface 34, UDASL switch interface converter circuit 1082, or both. Ex.1003, ¶108.

Therefore, Hartsell renders obvious this limitation.

⁴ Hartsell’s UDASL switch interface converter circuit 1082 is similar to the PHY modules identified in Patent Owner’s infringement allegations as “*common interfaces*.” Petitioner’s analysis is consistent with those allegations.

[27.4] with no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits.

As discussed in [27.3], Hartsell renders obvious each processor module (ASIC device) connected to interconnect 1080 (*intervening high speed serial optical link*) via interface 34 (*common interface*), *with no other processing device intervening between*. Ex.1003, ¶110.

Hartsell teaches the processing engines “communicate with each other directly as peers.” Ex.1005, [0125]. Further, Hartsell depicts no other processing devices between the processor modules 1001 and 1003 and the interconnect 1080 in its switch fabric implementation. *See* Ex.1005, Figs. 1C', 1C"; *see also* Ex.1005, [0058] (“a switch fabric establishes **independent paths from node to node** and data is specifically addressed to a particular node on the switch fabric”); Ex.1003, ¶111.⁵ Similarly, no other processing devices would intervene in a bus

⁵ Patent Owner’s infringement allegations appear to take the position that the claim’s “*no other processing device intervening...*” limitation does not foreclose the presence of processing devices within the *high speed serial optical link*.

Petitioner’s analysis is consistent with those allegations. Additionally, Patent Owner took the position in a response to a motion to dismiss in a related parallel

implementation of interconnect 1080 because in such implementations, each processing engine or processor module 1001 and 1003 of Hartsell's content delivery system 1010 would be coupled to the bus via a common interface with no other processing devices between the respective common interfaces and the bus. Ex.1003, ¶111.⁶ Accordingly, in the architecture suggested by Hartsell, the processor modules are interconnected by optical communication links without any intermediary processing device. Ex.1003, ¶111.

Therefore, Hartsell renders obvious this limitation.

litigation that “under at least one plausible claim construction, a ‘fabric card’ may not be an intervening processing device.” Ex.1008 (*Lionra Techs. Ltd. v. Fortinet, Inc.*, 2:22-cv-00322-JPR-RSP, Dkt. 78 (E.D. Tex. Dec. 23, 2022)) at 6. Thus, under Patent Owner's own positions, Hartsell's interconnect meets the limitation that “*no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits.*”

⁶ This is in line with how Figures 13, 14, and 15 of the '323 Patent depict FPGA devices and signal processing circuits as being interconnected. Ex.1001, Figs. 13-15.

b) Claim 28

[28.1] The communications infrastructure of claim 27, wherein said interconnection further comprises a high bandwidth interconnection medium.⁷

Hartsell renders obvious that its *intervening high speed serial optical link* would comprise *a high bandwidth interconnection medium* (to the extent there are differences between the two terms). Ex.1003, ¶113.

As noted in limitation [27.3], Hartsell’s interconnect 1080 includes node-to-node path links that connect one processing module to another processing module and transmit data bit-by-bit serially over “data aligned serial link interfaces.” Ex.1005, [0143]-[0144]; Ex.1003, ¶114. Hartsell explains that interconnect 1080 is an “8x3.54 Gbps fabric” in eight port mode, and a “16x1.77 Gbps fabric” in

⁷ Claim 28 recites “said interconnection,” but claim 27 does not recite an “interconnection.” For the purposes of the present proceeding, Petitioner interprets the recited “interconnection” to refer to the “intervening high speed serial optical link” from claim 27. *See also* Ex.1002, 41 (amending claim 27 to remove “an interconnection comprising a high speed serial optical link” and to add “an intervening high speed serial optical link”). Petitioner reserves the right to raise potential 35 U.S.C. § 112 arguments in a forum where such arguments are available.

sixteen port mode. Ex.1005, [0144]. A POSITA would have understood that Hartsell’s interconnect 1080 includes a *high bandwidth interconnection medium* to facilitate its data transmission capabilities of at least 1.77 Gbps. Ex.1005, [0144]; Ex.1003, ¶114. This is confirmed by the ’323 Patent, which explains that “[e]xamples of suitable high bandwidth interconnection mediums include...any interconnection mediums...having a data transmission capability of greater than or equal to about 1 gigabit per second (Gbps).” Ex.1001, 6:2-7, 13:25-28 (describing an embodiment supporting “data transmission rates between 622 Mbps and 3.125 Gbps”); Ex.1003, ¶114.

Because Hartsell describes its interconnect 1080 as an “8x3.54 Gbps fabric” in eight port mode, and a “16x1.77 Gbps fabric” in sixteen port mode—each supporting a data transmission capability greater than 1 Gbps—Hartsell renders obvious this limitation. Ex.1005, [0144]; Ex.1001, 6:2-7; Ex.1003, ¶115.

c) Claim 31

[31.1] A method, comprising providing two or more separate signal processing circuits,

As discussed in [27.1], Hartsell provides a communications infrastructure comprising *two or more separate signal processing circuits*. See *supra*, [27.1]; Ex.1003, ¶116. And as discussed in further detail below in [31.5], Hartsell renders

obvious a method involving transferring data packets between the signal processing circuits. *See infra*, [31.5]; Ex.1003, ¶116. Accordingly, Hartsell renders obvious this limitation. Ex.1003, ¶116.

[31.2] each one of said two or more signal processing circuits including multiple ASIC devices that each itself includes a packet router,

See analysis at [27.2].

[31.3] said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a respective packet router of each of the ASIC devices of each other of said two or more signal processing circuits

See analysis at [27.3].

[31.4] with no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits;

See analysis at [27.4].

[31.5] selectively transferring at least one data packet from each said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits to each respective packet router of said at ASIC devices of each of the other of said two or more signal processing circuits through said first and second common interfaces and said intervening high speed serial optical link without routing said data through any other intervening processing device between each respective ASIC device and the high speed serial optical link.

As discussed in [27.3], the prior art renders obvious that data may be transmitted between one *packet router* in a processor module 1001 or 1003 (*ASIC device*) of a transport processing engine 1050 (*signal processing circuit*) to another

processor module 1001 or 1003. And as discussed in [27.2], a POSITA would have found it obvious for each of Hartsell's processor modules 1001 or 1003 to operate as (or to include) a *packet router* because in the combination, each transport processing module would route request packets to their intended destinations over peer-to-peer optical links available through interconnect 1080. Ex.1005, [0045] ("high speed distributive interconnect... that allows peer-to-peer communication between individual subsystem modules"), [0107] ("Routing of requests... may be controlled by transport and/or interface processing modules"), [0239]; Ex.1003, ¶120. Further, as discussed in [27.3], Hartsell's processor modules 1001 and 1003, configured as transport processing engines 1050, are coupled through a first interface 34 (*first common interface*), interconnect 1080 (*high bandwidth interconnection medium*), and a second interface 34 (*second common interface*). See Ex.1005, [0144], Figs. 1C, 4; Ex.1003, ¶120.

Further, Hartsell teaches *selectively transferring at least one data packet* by disclosing the data communicated is in the form of data packets. See *supra*, [27.2]. Hartsell discloses that transport processing engines 1050 (*signal processing circuits*) have routing functions to route data between processor modules. "Routing of requests...may be accomplished using a distributive interconnect and may be controlled by transport and/or interface processing modules." Ex.1005, [0107]. It would have been obvious to a POSITA that routing requests among processor

modules includes *selectively transferring at least one data packet*. Ex.1003, ¶121.

Hartsell further explains that “information management flow may advantageously occur between any two or more processing engines that may be present on a network and interconnected via a virtual distributed inter connect backplane.”

Ex.1005, [0276]; Ex.1003, ¶121.

Hartsell’s transport processing engine 1050 performs “network transport protocol sub-tasks, such as processing content requests received from network interface engine 1030.” Ex.1005, [0072]. A POSITA would have understood that the received requests would include packets, because network interface engine 1030 “process[es] high speed streams of network packets,” Ex.1005, [0066], requests are passed to network transport processing engine 1050, and transport processing engine 1050 performs “packet header generation” as part of its tasks. Ex.1005, [0072]-[0073]; *see also* Ex.1005, [0127] (“each processing engine” manipulates data packet headers by, e.g., setting priority levels), [0138] (processing engines reduce “the packet size transmitted across the distributed interconnect” through protocol layer manipulation); Ex.1003, ¶122.

Further, Hartsell discusses using Infiniband, as noted above. *See supra*, [27.2]-[27.3]; Ex.1005, [0231], [0275]. A POSITA would have understood that the Infiniband protocol transmits data in the form of packets. Ex.1003, ¶123 (citing Ex.1013; Ex.1014). Accordingly, a POSITA would have found it obvious for

Hartsell’s transport processing engine 1050 to *selectively transfer[] at least one data packet.*

Therefore, Hartsell renders obvious this limitation.

d) Claim 33

[33.1] The method of claim 31, wherein said interconnection further comprises a high band width interconnection medium.⁸

See analysis at [28.1].

D. Ground 2: The Combination of Hartsell and Hauck Renders Obvious Claims 27-28, 31, and 33

The ’323 Patent describes an exemplary embodiment in which “high-bandwidth packet routers” facilitate transferring packets “in point-to-point fashion.” Ex.1001, 11:56-66. To the extent that Patent Owner argues that the claims’ recitation of a “*packet router*” within each ASIC device implies that each

⁸ Claim 33 recites “said interconnection,” although parent claim 31 does not recite an “interconnection.” For the purposes of the present proceeding, Petitioner interprets the recited “interconnection” to refer to the “intervening high speed serial optical link” from claim 31. Petitioner reserves the right to raise potential 35 U.S.C. § 112 arguments in a forum where such arguments are available.

ASIC device has point-to-point interconnections to other ASIC devices (for example, as illustrated in the '323 Patent's Fig. 2), it would have been obvious to a POSITA to modify Hartsell's architecture to provide such direct, point-to-point interconnections between Hartsell's processing modules 1001 and 1003. Ex.1003, ¶126.

1. Reasons to combine Hartsell and Hauck

It would have been obvious to a POSITA to modify Hartsell's architecture to eliminate the need for switch fabric 1080 by providing more direct communications paths between pairs of processing modules 1001 and 1003. As discussed above, each processing module 1001 and 1003 includes an FPGA, and it was well-known to route data among and between FPGAs using data paths directly connecting the FPGAs. Ex.1003, ¶¶126, 48-49; *see, e.g.*, Ex.1031. Many multi-FPGA interconnection schemes were known in the art, including for example, "mesh" and "crossbar" interconnection architectures. Ex.1003, ¶126; Ex.1030, 626. It would have been obvious to a POSITA to try a "mesh" or "crossbar" interconnection architecture among the FPGAs of the processing modules because those were the "most common topologies" for interconnecting multiple FPGAs in a multi-FPGA system. Ex.1030, 626. Ex.1003, ¶126. A POSITA would have had an expectation of success in modifying Hartsell in this way because many two-dimensional and three-dimensional mesh-based systems had been built as early as

1998. Ex.1003, ¶126; Ex.1030, 626. Techniques for routing data between and among FPGAs in a mesh-based architecture had also long been known. Ex.1003, ¶126 (citing Ex.1030, 636 at [57]).

Additional reasons to combine teachings from each of the references are provided in the analysis below.

2. Claim Analysis

a) Claim 27

[27.1] A communications infrastructure, comprising two or more separate signal processing circuits,

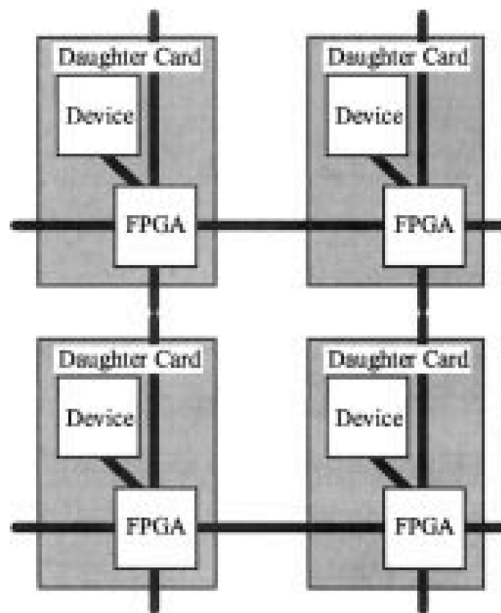
Hartsell renders obvious limitation [27.1]. *See* Section XI.C.1.a[27.1], above. Ex.1003, ¶129.

[27.2] each one of said two or more signal processing circuits including multiple ASIC devices that each itself includes a packet router,

Ground 2 relies on the same analysis and evidence as provided above in Ground 1 for limitation [27.2] regarding Hartsell's disclosure of *ASIC devices*. *See* Section XI.C.1.a[27.2], above. Ex.1003, ¶130.

Additionally, it would have been obvious to a POSITA to implement Hartsell's content delivery system 1010 such that the processor modules 1001 and 1003 (*ASIC devices*) would have each *include[d] a packet router* allowing for direct connection between each processor module, where such implementation

would have interconnected each processor module 1001 and 1003 in the same way as depicted in the figures of the '323 Patent. Ex.1003, ¶131. Such interconnections between the FPGAs of processor modules 1001 and 1003 would have been obvious and well-known to a POSITA by the priority date of the '323 Patent, as evidenced by Hauck. Ex.1003, ¶131. Hauck confirms the practice of directly connecting FPGA devices to route packets between the FPGAs was used “for both routing and rerouting of signals[.]” Ex.1030, 632, 633 (describing a system where FPGAs “are used for both routing and rerouting of signals”), Fig. 25(a).



Ex.1030, Fig. 25(a); Ex.1003, ¶131

Like Hartsell, Hauck describes the connection of devices, such as a processor, memory, or other necessary elements to implement a system, connected to the FPGAs depicted in Hauck’s Fig. 25(a), above, just as Hartsell’s processor

modules 1001 and 1003 include both an FPGA and other components including a processor and memory. Ex.1030, 632-633; Ex.1003, ¶132. Accordingly, it would have been obvious to modify Hartsell's content delivery system 1010 to directly interconnect Hartsell's processor modules 1001 and 1003, rather than having them connect through the switch fabric, because doing so would have been no more than applying a known technique (directly connecting FPGAs) to a known device (Hartsell's content delivery system 1010) ready for improvement to yield predictable results (directly connecting the FPGAs of each of Hartsell's processor modules 1001 and 1003 to route data between the processor modules). Ex.1003, ¶132. A POSITA would have had a reasonable expectation of success in making such modifications to Hartsell because, as noted above, the practice of directly connecting FPGAs such that FPGAs serve as packet routers to directly route data to other FPGAs was well-known in the art prior to the priority date of the '323 Patent. Ex.1003, ¶132.

And to the extent that each of Hartsell's processor modules 1001 and 1003 are implemented as single integrated chip FPGA devices, a POSITA would have recognized that each of the FPGA devices would be directly interconnected. As an example, Xilinx Virtex-II Pro FPGAs were known to have port modules capable of routing communications to other FPGAs. *See* Ex.1032, 1:40-43 (Xilinx patent FPGA with "port modules having configurable logic configured to process

communications for routing the communications”); Ex.1033, Abstract, [0004] (explaining that FPGAs are designed “with multi-gigabit serial transceivers that support a communications protocol...to enable communications of data between FPGAs at high speed”); Ex.1003, ¶133.

Thus, the modification would result in processor modules 1001 or 1003 performing routing of packets directly to other processor modules through the respective FPGAs, which renders obvious that each processor module 1001 or 1003 *includes a packet router*. Ex.1003, ¶134.

[27.3] said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a respective packet router of each of the ASIC devices of each other of said two or more signal processing circuits

First, as discussed in [27.1]-[27.2], Hartsell teaches that one transport processing module (such as processor module 1001 or 1003) in a transport processing engine is communicatively coupled to another transport processing module in another transport processing engine. Ex.1005, [0143]. A POSITA would have understood that these processor modules are *ASIC devices*. And each processor module includes a *packet router* for routing requests and data between the transport processing engines. *See supra*, [27.2]; Ex.1003, ¶135.

Second, Hartsell renders obvious that the processor modules (each of which comprises a *packet router*) are coupled via an *intervening high speed serial optical link*, as noted above in [27.2] and further detailed below. Ex.1003, ¶136.

In the modification described above in [27.2], Hartsell’s processor modules are directly coupled to other processor modules via the FPGA in each processor module. *See supra*, [27.2]; Ex.1003, ¶137. The practice of directly connecting FPGA devices to route packets between the FPGAs was used “for both routing and rerouting of signals[.]” Ex.1030, 632, 633 (describing a system where FPGAs “are used for both routing and rerouting of signals”), Fig. 25(a); Ex.1003, ¶137. This was also well-known to be implemented with single integrated chip FPGA devices, such as the Xilinx Virtex-II Pro FPGA family. *See* Ex.1020, 1:40-43 (Xilinx patent FPGA with “port modules having configurable logic configured to process communications for routing the communications”); Ex.1021, Abstract, [0004] (explaining that FPGAs are designed “with multi-gigabit serial transceivers that support a communications protocol...to enable communications of data between FPGAs at high speed”); Ex.1003, ¶137.

This node-to-node path link is a *high speed serial link* because interconnect 1080 is an “8x3.54 Gbps fabric” in eight port mode, and a “16x1.77 Gbps fabric” in sixteen port mode. Ex.1005, [0144]. In modifying Hartsell to use direct, FPGA-to-FPGA interconnects as suggested by Hauck, it would have been obvious to a

POSITA to maintain the speed and bandwidth of Hartsell's original communications capabilities, and thus to use interconnection technologies capable of communicating signals at least as fast as in Hartsell's original disclosure.

Ex.1003, ¶138. Accordingly, even in a modified architecture that includes point-to-point interconnections between processing modules 1001 and 1003, it would have been obvious for each point-to-point interconnection to be a *high speed serial link*. Ex.1003, ¶138.

Further, it would have been obvious to a POSITA to use a *serial optical link* as the node-to-node path link connecting one processor module to another. Hartsell teaches that its processing engines can be interconnected via “optical interconnect technology,” such as Infiniband. Ex.1005, [0275]; *see also supra*, [27.2]; Ex.1003, ¶139. Specifically, because Hartsell discloses that its processor modules use optical interconnect technology and optical protocols for packet transfer, in the modification to Hartsell, each processor module 1001 and 1003 would be connected to other processor modules 1001 and 1003 using optical interconnect technology. Connecting Hartsell's processor modules via “optical interconnect technology” renders obvious the claimed *intervening high speed serial optical link*. Ex.1003, ¶139.

Third, in the modification, Hartsell renders obvious that each of its processor modules (each comprising a *packet router*) would be coupled via an

intervening high speed serial optical link to another processor module through *first and second common interfaces* connected to the respective FPGAs of each processor module. Ex.1003, ¶140.

Hartsell describes an interface 34 located between interconnect 1080 and each processor module 1001 and 1003. Ex.1005, [0144] (“interface 34 provides an interface between the processor module bus and the UDASL switch interface converter circuit 1082 [within interconnect 1080]”), Fig.4. A POSITA would have recognized that by modifying Hartsell to directly connect processor modules 1001 and 1003 (as suggested by Hauck), Hartsell’s interface 34 for each processor module 1001 or 1003 would instead be used as *first and second common interfaces* to incorporate suitable optical transceiver functionality to transfer packets via an optical link between the respective processor modules. Ex.1003, ¶141.

Therefore, Hartsell and Hauck render obvious this limitation. Ex.1003, ¶142.

[27.4] with no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits.

Hartsell renders obvious limitation [27.4]. *See* Section XI.C.1.a[27.4], above. Ex.1003, ¶143.

b) Claim 28

[28.1] The communications infrastructure of claim 27, wherein said interconnection further comprises a high bandwidth interconnection medium.⁹

Ground 2 relies on the same analysis and evidence as provided above in Ground 1 for limitation [28.1]. The arguments and evidence discussed above with respect to Ground 1 are incorporated herein. *See* Section XI.C.1.a[28.1], above. Ex.1003, ¶144.

c) Claim 31

[31.1]-[31.4] (elements recited in claim 31)

As noted above in Ground 1, the analysis for elements [31.1]-[31.4] of claim 31 are substantially similar to elements [27.1]-[27.4] of claim 27. Thus, these elements are obvious for the same reasons discussed above for claim 27 in Ground 2. *See also* Section XI.C.1.a[31.1]-[31.4], above. Ex.1003, ¶145.

⁹ *See supra*, n.7.

[31.5] selectively transferring at least one data packet from each said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits to each respective packet router of said at ASIC devices of each of the other of said two or more signal processing circuits through said first and second common interfaces and said intervening high speed serial optical link without routing said data through any other intervening processing device between each respective ASIC device and the high speed serial optical link.

Ground 2 relies on the same analysis and evidence as provided above in Ground 1 for limitation [27.1]. The arguments and evidence discussed above with respect to Ground 1 are incorporated herein. *See* Section XI.C.1.a[31.5], above. Ex.1003, ¶146.

d) Claim 33

[33.1] The method of claim 31, wherein said interconnection further comprises a high band width interconnection medium.¹⁰

Ground 2 relies on the same analysis and evidence as provided above in Ground 1 for limitation [28.1], and thus for limitation [33.1]. The arguments and evidence discussed above with respect to Ground 1 are incorporated herein. *See* Sections XI.C.1.a[28.1] and XI.C.1.a[33.1], above. Ex.1003, ¶147.

¹¹ *See supra*, n.8.

E. Grounds 3 and 4: The Combination of Hartsell and Raj and the Combination of Hartsell, Hauck, and Raj Render Obvious Claims 27-28, 31, and 33

1. Reasons to combine Hartsell and Raj

Detailed analysis of the reasons to combine teachings from the prior art references is included in the claim analysis below.

2. Claim Analysis

The claim analysis for Grounds 3 and 4 rely on the same analysis and evidence as provided for Ground 1 (Hartsell alone) and Ground 2 (Hartsell with Hauck), respectively, except for where additional analysis is provided, as noted for respective limitations of the claims below. The additional analysis provided below applies for both Grounds 3 and 4.

a) Claim 27

[27.1] A communications infrastructure, comprising two or more separate signal processing circuits,

Hartsell renders obvious limitation [27.1]. *See* Section XI.C.1.a[27.1], above. Ex.1003, ¶150.

[27.2] each one of said two or more signal processing circuits including multiple ASIC devices that each itself includes a packet router,

Hartsell, alone or with Hauck, renders obvious limitation [27.2]. *See* Section XI.C.1.a[27.2], above, and Section XI.D.2.a[27.2], above. Ex.1003, ¶151.

[27.3] said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a respective packet router of each of the ASIC devices of each other of said two or more signal processing circuits

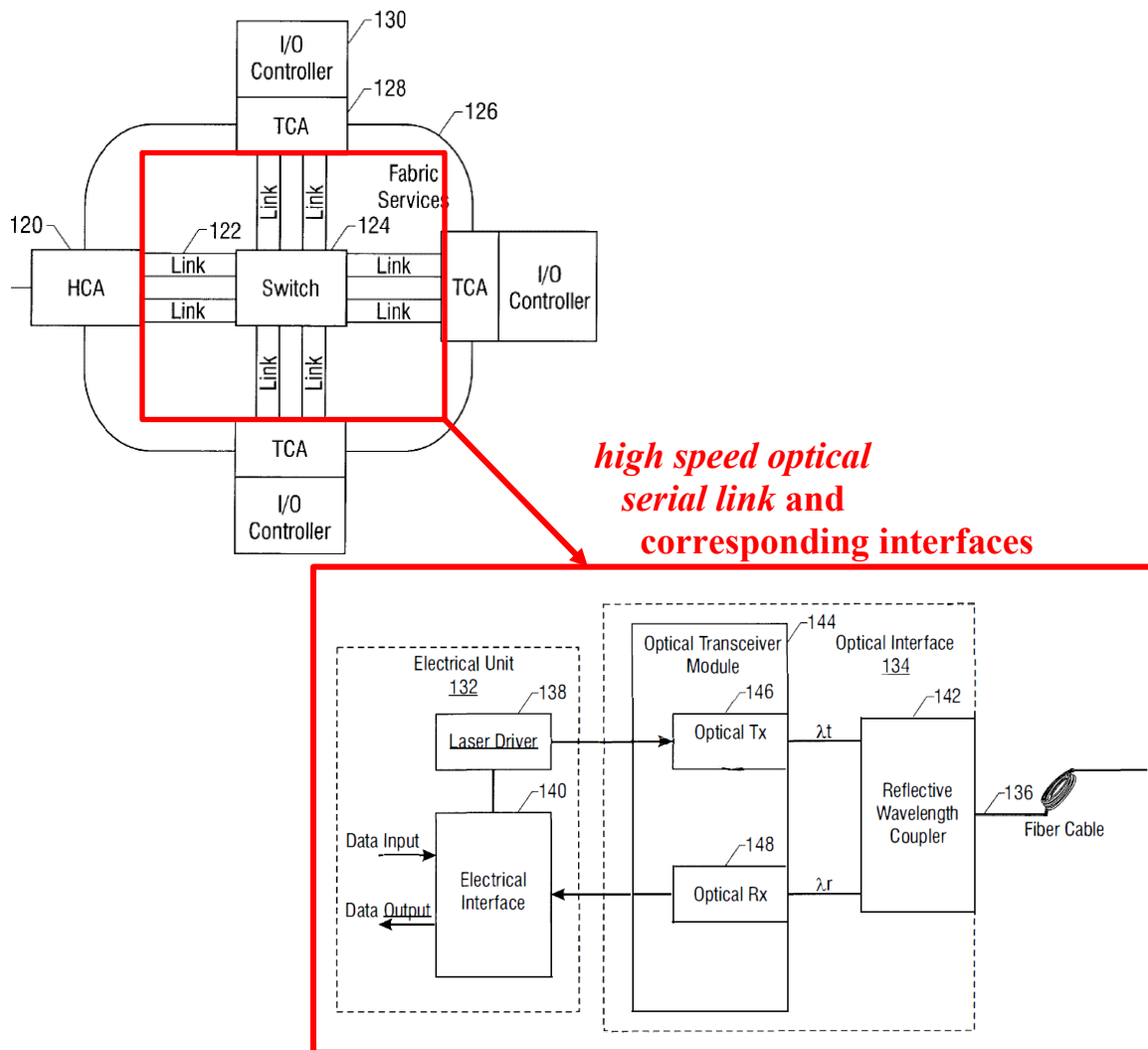
First, as discussed in [27.1]-[27.2], Hartsell teaches that one transport processing module (such as processor module 1001 or 1003) in a transport processing engine is communicatively coupled to another transport processing module in another transport processing engine (which may incorporate the functionality of network interface processing engines). Ex.1005, [0143]; Ex.1003, ¶152. A POSITA would have understood that these processor modules are *ASIC devices*. Ex.1003, ¶152. And each processor module includes a *packet router* for routing requests and data between the transport processing engines. *See supra*, [27.2]; Ex.1003, ¶152.

As discussed in Ground #1 for [27.3], Hartsell contemplates coupling processor modules via a “distributive interconnection 1080,” which operates as a “high speed interchange system[.]” Ex.1005, [0058]. Hartsell teaches that its processing engines can be interconnected via “optical interconnect technology,” such as Infiniband. Ex.1005, [0275]; *see also supra*, [27.2]. To the extent that Hartsell’s suggestion regarding the use of Infiniband and optical interconnect technology is insufficient by itself, a POSITA would have found it obvious to

consult other references for more information about using optical technologies such as Infiniband to provide optical interconnections between the processing modules. Ex.1003, ¶¶154-155. Raj provides such information, teaching that multiple circuit units can be interconnected via a switch built with *high speed serial optical links*. Ex.1007, 1:55-67; Ex.1003, ¶155.¹¹

Raj teaches a “server or other processor-based device” that includes input/output controllers coupled to one another via fabric services. Ex.1007, 1:50-55. Raj is described in the context of Infiniband, but its teachings are “applicable to optical links in general.” Ex.1007, 1:63-67; Ex.1003, ¶156. Raj’s Fig. 1, below, provides a depiction of the device’s fabric services, while Fig. 2 provides further detail of the configuration of the optical links and corresponding interfaces for the optical links:

¹¹ Petitioner presents ground 2 and the Raj reference in view of Patent Owner’s infringement allegations, which appear to take the position that the claim’s “*high speed serial optical link*” limitation does not foreclose the presence of an electrical unit. Petitioner’s analysis is consistent with those allegations.



Ex.1007, Fig. 1 (partial view, annotated), Fig. 2 (annotated); Ex.1003, ¶156

Raj's device-to-device optical serial link, depicted in Figs. 1 and 2 above as links 122 and switch 124, has an optical interface to communicate optical signals with electrical unit 132. Ex.1007, Abstract, 2:24-31; Ex.1003, ¶156. Further, it would have been obvious to incorporate Raj's electrical unit 132 and optical interface 134 into Hartsell's processing modules as part of each module's interface 34 ("*common interface*"), as discussed further below. Ex.1003, ¶156.

It would have been obvious to a POSITA to combine concepts from Hartsell's interconnect 1080 with Raj's optical switch 124 to interconnect multiple processor modules via optical links. Ex.1003, ¶157. A POSITA would have been motivated to combine features from Hartsell and Raj because Hartsell provides an explicit teaching to implement an optical serial link connection. Ex.1005, [0275] (separate processing engines may be interconnected using technologies such as **“optical interconnect technology** (e.g., in conjunction with optic/optic interface-based systems)"); Ex.1003, ¶157. Raj teaches the implementation of optical interconnections using optical serial links. Ex.1007, 1:64-65; Ex.1003, ¶157. Therefore, using Raj's optical serial link connection between processor modules would facilitate Hartsell's content delivery system to be compatible with an optical network environment, as suggested by Hartsell. Ex.1005, [0275]; Ex.1003, ¶157. The combination of Hartsell and Raj would achieve an optical interconnection and configuration for Hartsell's content delivery system, which would improve system data rates. Ex.1003, ¶157.

Further, a POSITA would have had a reasonable expectation of success in combining Raj's optical interconnection technology with Hartsell's interconnect 1080 because Hartsell teaches that its interconnect 1080 can be “any multi-node I/O interconnection hardware or hardware/software system” such as “a switch fabric or bus architecture.” Ex.1005, [0058]. Raj's optical switch 124 is a multi-

node I/O interconnection hardware as the switch 124 connects multiple I/O controllers 130. Ex.1007, 1:56-59; Ex.1003, ¶158. In addition, both Hartsell and Raj teach their interconnect technology can operate under the Infiniband specification, which was a well-known serial optical interconnection standard whose use was admitted to be within the POSITA skillset. Ex.1005, [0231], [0275]; Ex.1007, 1:65-67; Ex.1001, 11:2-9, 14:41-48, 21:12-16, 22:63-23:1; Ex.1003, ¶158. Therefore, it would have been obvious to implement Hartsell's interconnect 1080 using concepts from Raj's optical switch 124 and links 122, and a POSITA would have had a reasonable expectation of success in doing so. Ex.1003, ¶158.

In the resulting combination, each pair of Hartsell's processor modules would be connected via an optical serial link as taught by Raj, which renders obvious the claimed *intervening high speed serial optical link*. Ex.1003, ¶159.

Third, Hartsell in view of Raj renders obvious that each of Hartsell's processor modules (each comprising a *packet router*) would be coupled via an *intervening high speed serial optical link* to another processor module through fabric interfaces (*first and second common interfaces*). Ex.1003, ¶160.

Hartsell describes an interface 34 located between interconnect 1080 and each processor module 1001 and 1003. Ex.1005, [0144] ("interface 34 provides an interface between the processor module bus and the UDASL switch interface

converter circuit 1082 [within interconnect 1080]”), Fig.4; Ex.1003, ¶161.

However, Hartsell provides limited details for how interface 34 would operate when the interconnect 1080 uses optical communication technology such as Infiniband. Ex.1003, ¶161. Raj teaches an electro-optical interface that converts optical signals from the optical switch fabric to electrical signals. Ex.1007, 2:24-31. It would have been obvious to a POSITA to implement Hartsell’s interface 34 using optical communication components, such an electro-optical interface like that discussed in Raj. Ex.1003, ¶161.

A POSITA would have been motivated to combine the teachings because Hartsell describes using optical technology, and when implementing optical technology, an optical-to-electrical (and vice versa) interface would have been needed between the optical serial links and an electrical circuit unit such as the processor modules. Ex.1003, ¶162. Raj’s optical switch 124 has a similar need, as discussed immediately above, and Raj describes its implementation. Ex.1003, ¶162. By combining Raj’s optical-to-electrical interfaces (e.g., electrical interface 140 and laser driver 138) with Hartsell’s fabric interface 34, the combination would facilitate data transmission between Hartsell’s processor modules over an optical fabric (or optical bus interconnecting Hartsell’s processor modules, as discussed in further detail above in Ground 1). Ex.1003, ¶162. A POSITA would have had a reasonable expectation of success in combining Hartsell’s interface 34

with Raj's optical-to-electrical interfaces, because Hartsell itself suggests such a combination (Ex.1005, [0113]) and because such technology was well-known and standardized. *See* Ex.1007, 1:5-26 (describing known electro-optical interfaces, such as an Infiniband host channel adapter). Ex.1003, ¶162.

In the resulting combination, Hartsell's interface 34 for each processor module 1001 or 1003, implementing Raj's electrical interface 140 and laser driver 138 that converts electrical signals to optical signals, renders obvious the *first and second common interfaces*. Ex.1003, ¶163.

Therefore, the prior art renders obvious this limitation.

[27.4] with no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits.

As discussed in [27.3], the Hartsell-Raj combination renders obvious each processor module (*ASIC device*) connected to interconnect 1080, implementing Raj's optical serial link, (*intervening high speed serial optical link*) via interface 34, implementing Raj's electrical interface 140 and laser driver 138, (*common interface*). As discussed in [27.4] of Ground 1, Hartsell renders obvious processor modules coupled to an optical link without any intermediary processing device. Ex.1003, ¶¶165-166.

Similarly, Raj's Figs. 1 and 2 show no other processing device between the electrical circuits of the target channel adapters connected through the optical switch 124. *See* Ex.1007, Figs. 1, 2. Raj further teaches the "fiber may be utilized with a fabric switch 124 or a passive star network." Ex.1007, 3:5-6. Accordingly, a POSITA would have recognized that under Raj's network structure, circuits are interconnected by the switch fabric without any intermediary processing device. Ex.1003, ¶167. Alternatively, it would have been obvious for each of Hartsell's processor modules (*ASIC devices*) to have an optical link to each other processor module in a "passive star network" as suggested by Raj. Ex.1003, ¶167. Since such a network arrangement is described as "passive," it would have been obvious to a POSITA that the passive star network embodiment would not include any processing elements between the processor modules and the optical links. Ex.1003, ¶167.

Therefore, Hartsell in view of Raj renders obvious this limitation.

b) Claim 28

[28.1] The communications infrastructure of claim 27, wherein said interconnection further comprises a high bandwidth interconnection medium.¹²

Hartsell in combination with Raj renders obvious that its *intervening high speed serial optical link* would comprise a *high bandwidth interconnection medium* (to the extent there are differences between the two terms). Ex.1003, ¶169.

As discussed for [28.1] in Ground #1, Hartsell describes interconnect 1080 as a *high bandwidth interconnection* capable of multi-gigabit communications. *See supra*, Ground 1, [28.1].

Such multi-gigabit communication capabilities are retained in the combinations with Raj. Ex.1007, 1:63-64; Ex.1003, ¶170. Raj describes using optical communications technology in which “data rates may be in excess of 2.5 gigabits per second.” Ex.1007, 1:63-64. Thus, it would have been obvious to a POSITA for Hartsell’s interconnect 1080, when implemented using the optical communications technology of Raj, to support *high bandwidth* communications greater than or equal to at least 1 gigabit per second. Ex.1003, ¶¶170-172. Raj further describes transmitting data over fiber optic cables, such as “dispersion shifted fibers (DSF) or dispersion compensated fibers (DCF),” both of which

¹² *See supra*, n.7.

“support **high data rates** with low attenuation.” Ex.1007, 3:2-4. Such optical fibers were well-known as communications *medi[a]*. Ex.1003, ¶172.

In summary, the prior art describes transmitting data between processing modules via optical fibers at data rates in excess of 1 gigabit per second, which renders obvious “*high bandwidth interconnection medium*.” Ex.1003, ¶173.

c) Claim 31

[31.1] A method, comprising providing two or more separate signal processing circuits,

As discussed in [27.1], Hartsell provides a communications infrastructure comprising *two or more separate signal processing circuits*. *See supra*, [27.1]; Ex.1003, ¶174. And as discussed in further detail below in [31.5], Hartsell renders obvious a method involving transferring data packets between the signal processing circuits. *See infra*, [31.5]; Ex.1003, ¶174. Accordingly, Hartsell renders obvious this limitation. Ex.1003, ¶174.

[31.2] each one of said two or more signal processing circuits including multiple ASIC devices that each itself includes a packet router,

See analysis at [27.2].

[31.3] said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a respective packet router of each of the ASIC devices of each other of said two or more signal processing circuits

See analysis at [27.3].

[31.4] with no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits;

See analysis at [27.4].

[31.5] selectively transferring at least one data packet from each said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits to each respective packet router of said at ASIC devices of each of the other of said two or more signal processing circuits through said first and second common interfaces and said intervening high speed serial optical link without routing said data through any other intervening processing device between each respective ASIC device and the high speed serial optical link.

As discussed at [31.5] for Ground #1, Hartsell renders this limitation obvious by describing how its processor modules communicate with one another via data packets.

Further, Hartsell and Raj both discuss using Infiniband, as noted above. *See supra*, [27.2]-[27.3]; Ex.1005, [0231], [0275]; Ex.1007, 1:5-26, 1:65-67. A POSITA would have understood that the Infiniband protocol transmits data in the form of packets. Ex.1003, ¶178 (citing Ex.1013; Ex.1014). Accordingly, a

POSITA would have found it obvious for Hartsell's transport processing engine 1050, in the Hartsell-Raj combination, to *selectively transfer[] at least one data packet*.

Therefore, the prior art renders obvious this limitation.

d) Claim 33

*[33.1] The method of claim 31, wherein said interconnection further comprises a high band width interconnection medium.*¹³

See analysis at [28.1].

XII. DISCRETIONARY DENIAL IS INAPPROPRIATE

A. Discretionary Denial under 35 U.S.C. § 325(d) is Not Appropriate

Denial under § 325(d) is not warranted because the challenges presented in this petition are neither cumulative nor redundant to the prosecution of the '323 Patent. The Hartsell and Raj references were not cited or considered by the Examiner during prosecution of the '323 Patent.

In summary, the references in this Petition were neither relied upon during prosecution nor are cumulative of art relied upon during prosecution.

¹³ See *supra*, n.8.

B. Discretionary Denial under the *Fintiv* Factors is Not Appropriate

The Board balances six factors in considering denial under § 314. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential). These factors strongly favor institution. The district court case is in its very early stages. Patent Owner filed its complaint on August 8, 2022. Patent Owner provided its disclosure of asserted claims and infringement contentions on November 3, 2022. Ex.1018, 5. Invalidity contentions were due on February 10, 2023. Ex.1018, 4. Petitioner has since worked diligently to prepare this Petition, which is being filed well within the one-year timeframe allowed by Congress.

1. No Evidence Regarding a Stay

If an IPR is instituted, a stay of the co-pending litigation would be appropriate. However, given that a motion to stay has not yet been filed, the Board should not infer or attempt to predict the outcome if such a motion is later filed. *Sand Revolution II LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (June 16, 2020) (informative); *see also Dish Network L.L.C. v. Broadband iTV, Inc.*, IPR2020-01359, Paper 15 (Feb. 12, 2021) (“It would be improper to speculate, at this stage, what the Texas court might do regarding a motion to stay...”). Thus, this factor is neutral.

2. Parallel Proceeding Trial Date

Trial in the party's co-pending litigation is currently scheduled for May 20, 2024 (Ex.1018, 1), in line with the median time-to-trial for the Eastern District of Texas. *See* Ex.1016, 35 (showing the median time-to-trial in the Eastern District of Texas as 19 months); Director's June 21, 2022 Memorandum on Discretionary Denials (Ex.1019), 9 ("The PTAB will weigh this factor [factor 2] against exercising discretion to deny institution under Fintiv if the median time-to-trial is around the same time or after the projected statutory deadline for the PTAB's final written decision."). The Board's Final Written Decision is expected in December 2024.¹⁴

However, "scheduled trial dates are often subject to change." *In re Apple Inc.*, 979 F.3d 1332, 1344, n.5 (Fed. Cir. 2020); Ex.1019, 8 ("A court's scheduled trial date, therefore, is not by itself a good indicator of whether the district court trial will occur before the statutory deadline for a final written decision.").

Petitioner notes that eight other cases are scheduled for Jury selection on May 20, 2024—the same Jury Selection date as the co-pending litigation. Ex.1020 (listing

¹⁴ December 2024 is 18 months after June 2023, when Petitioner expects a Notice of Filing Date Accorded for this Petition.

all cases having Jury Selection scheduled for May 20, 2024, in front of Judge Gilstrap).

As such, this factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Grp.—Trucking LLC*, IPR2020-01393, Paper 24 (June 16, 2020) (panel granting institution on rehearing based on finding that uncertainty over district court’s trial date weighed against discretionary denial).

3. Investment in the Parallel Proceedings

The co-pending litigation is in its early stages, and the investment in it has been minimal. The parties have not exchanged proposed claim terms or constructions, and will not complete claim construction briefing until October 27, 2023. Ex.1018, 2. The *Markman* hearing is not scheduled until November 17, 2023. Ex.1018, 3. Fact discovery is in its nascent stages and is not set to close until December 8, 2023, and expert discovery is not set to close until February 5, 2024. Ex.1018, 3; *see PEAG LLC v. Varta Microbattery GMBH*, IPR2020-01214, Paper 8 at 17 (Jan. 6, 2021) (finding that since no claim construction hearing had yet been held and discovery was not completed, the little investment in the parallel proceeding weighed against discretionary denial).

Accordingly, the lack of investment in the parallel district court proceeding favors institution.

4. Overlapping Issues with the Parallel Proceeding

There is no overlap of prior art issues at this time. Instituting a proceeding will allow the Board to address the asserted prior art, and the issues will be narrowed in the co-pending litigation due to the estoppel provisions of 35 U.S.C. § 315(e)(2).

Additionally, if the Board institutes trial, Petitioner will cease asserting in the co-pending litigation the combination of references on which trial is instituted for the claims on which trial is instituted, to the extent Petitioner even asserts the same combination in the district court. *See Verizon v. Huawei*, IPR2020-01079, Paper 10 at 38 (finding a similar stipulation “mitigates the concern about overlapping issues” and weighs “against discretionary denial of the Petition”).

Accordingly, this factor weighs against discretionary denial.

5. Whether Petitioner is Defendant

Petitioner is a defendant in the litigation. Ex.1017. This is true of most Petitioners in IPR proceedings. While the *Fintiv* case indicates that a difference between the district court defendant and the petitioner may weigh against discretionary denial, nothing within the *Fintiv* case suggests that the same party. between the proceedings weighs in favor of discretionary denial. *See HP Inc. v. Slingshot Printing LLC*, IPR2020-01084, Paper 13 at 9 (having the “same parties

as parallel proceeding” makes factor 5 “neutral”). Accordingly, this factor is neutral and should not be a basis for denying institution.

6. Other Circumstances

As discussed in detail above, the prior art presented in this Petition renders the Challenged Claims unpatentable as obvious. Even if the Board determines that the other *Fintiv* factors favor a discretionary denial—which they do not—the Director’s *Fintiv* Guidance strongly supports institution of this challenge. *See CommScope Technologies LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 4-5 (PTAB Feb. 27, 2023) (precedential). Under the *Fintiv* Guidance, the Board “will not deny institution of an IPR or PGR under *Fintiv* [] when a petition presents compelling evidence of unpatentability.” EX1011, 9. The merits of Petitioner’s arguments are compelling because they lead to a strong conclusion that it is highly likely one or more claims are unpatentable by a preponderance of the evidence. For example, substantially all the claimed concepts are directly disclosed by Hartsell. The few claimed concepts for which additional prior art is alternatively cited are explicitly suggested by Hartsell (e.g., the use of an optical communication link). Additionally, Petitioner’s arguments are compelling because they present prior art in the same way that Patent Owner represents its claims in the parallel litigation. This factor weighs against discretionary denial.

As such, because the *Fintiv* factors are either neutral or weigh against discretionary denial, and because this Petition was filed well before the statutory bar date, institution should not be denied on discretionary factors.

C. Discretionary Denial under *General Plastic* is Not Appropriate

The '323 Patent has not been challenged in any prior IPR petition, so none of the *General Plastic* discretionary institution factors apply to this Petition. *See General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19, 16 (Sept. 6, 2016) (Section II.B.4.i. precedential).

XIII. CONCLUSION

Petitioner has established a reasonable likelihood that the Challenged Claims are unpatentable.

Respectfully submitted,

Dated: June 12, 2023
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XIV. MANDATORY NOTICES

Real Party-in-Interest

Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner certifies that the real party-in-interest is Cisco Systems, Inc.

Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), to the best knowledge of Petitioner, the '323 Patent is or was involved in the following cases:

Case Heading	Number	Court	Filed
<i>Lionra Techs. Ltd. v. Cisco Systems, Inc.</i>	2:22-cv-00305	EDTX	Aug. 8, 2022
<i>Lionra Techs. Ltd. v. Hewlett Packard Enterprise Co. et al.</i>	2:22-cv-00319	EDTX	Aug. 19, 2022
<i>Lionra Techs. Ltd. v. Fortinet, Inc.</i>	2:22-cv-00322	EDTX	Aug. 19, 2022
<i>Lionra Techs. Ltd. v. Palo Alto Networks, Inc.</i>	2:22-cv-00334	EDTX	Aug. 29, 2022

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Please address all correspondence in this proceeding to lead and back-up counsel. Petitioner consents to service in this proceeding by email at the addresses above.

XV. APPENDIX OF CHALLENGED CLAIMS

Claim 27

[27.1] A communications infrastructure, comprising two or more separate signal processing circuits,

[27.2] each one of said two or more signal processing circuits including multiple ASIC devices that each itself includes a packet router,

[27.3] said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a respective packet router of each of the ASIC devices of each other of said two or more signal processing circuits

[27.4] with no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits.

Claim 28

[28.1] The communications infrastructure of claim 27, wherein said interconnection further comprises a high bandwidth interconnection medium.

Claim 31

[31.1] A method, comprising providing two or more separate signal processing circuits,

[31.2] each one of said two or more signal processing circuits including multiple ASIC devices that each itself includes a packet router,

[31.3] said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a respective packet router of each of the ASIC devices of each other of said two or more signal processing circuits

[31.4] with no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits;

[31.5] selectively transferring at least one data packet from each said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits to each respective packet router of said at ASIC devices of each of the other of said two or more signal processing circuits through said first and second common interfaces and said intervening high speed serial optical link without routing said data through any other intervening processing device between each respective ASIC device and the high speed serial optical link.

Claim 33

[33.1] The method of claim 31, wherein said interconnection further comprises a high band width interconnection medium.

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner hereby certifies, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,644. Pursuant to 37 C.F.R. § 42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: June 12, 2023

/Theodore M. Foster/
Theodore M. Foster
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Registration No. 57,456

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, service was made on Patent Owner as detailed below.

Date of service June 12, 2023

Manner of service Federal Express

Documents served Petition for *Inter Partes* Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 7,921,323; Petitioner's Exhibit List; Exhibits 1001-1033

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