

Design of Flat-Panel Displays Based on Organic Light-Emitting Devices

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Abstract—We provide a systematic and quantitative analysis of the design of flat-panel displays (FPD's) based on organic light-emitting devices (OLED's). Key performance parameters are estimated for OLED-based displays; system issues, including addressing schemes and strategies required to achieve full-color displays, are treated quantitatively. Furthermore, addressing schemes for recently demonstrated, full-color high-resolution stacked OLED's are discussed. Our analysis shows that OLED technology is suitable for many FPD applications, and can provide performance superior to that achieved using alternative display technologies.

Index Terms—Active matrix, color, passive matrix, thin film.

NOMENCLATURE

A	Area of an organic light-emitting device (OLED).
C_{GS}	Gate-to-source capacitance of a field-effect transistor (FET).
C_{OX}	Insulator layer capacitance per unit area of a FET.
C_{pix}	Total holding capacitance of a pixel in an AM OLED display.
C_S	Storage capacitor in an AM OLED pixel.
d	Column drive signal duty cycle in an passive matrix (PM) OLED display.
D	Discrimination ratio.
D_c	Gap width between the column lines in a PM display.
D_r	Gap width between the row lines in a PM display.
E_a	Ambient illuminance.
$f(V)$	Current dependence on voltage followed by a forward biased OLED.
$f_{rev}(V)$	Current dependence on voltage followed by a reverse biased OLED.
F	Luminous flux emitted by an OLED.
H	Display height.
I	OLED drive current.
I	OLED luminous intensity.
I_D	FET drain current.
J	OLED drive current density.
l	FET channel width.

L	Instantaneous luminance of an OLED.
L_d	Average brightness of a display.
L	Excess optical loss resulting from a full-color strategy.
m	Power-law in the OLED I - V dependence.
M	Number of rows of a display.
n_a	Refractive index of the OLED EL material.
N	Number of columns of a display.
N_g	Number of gray levels of a display.
P	Optical power emitted by an OLED.
r_a	Aperture ratio.
R_e	Effective resistance of an OLED under low forward voltages.
R_{rev}	Effective resistance of a reverse biased OLED.
R_{sq}	Sheet resistance of the continuous top contact of an AM OLED array.
R_{sqc}	Column-line sheet resistance in a PM OLED display.
R_{sqr}	Row-line sheet resistance in a PM OLED display.
T_f	Frame time.
V	OLED drive voltage.
V_c	Column-line voltage drop in a PM OLED display.
V_{DS}	Drain-to-source voltage of a FET.
V_g	Ground-line voltage drop in an AM OLED display.
V_G	Gate potential of a FET.
V_{GS}	Gate-to-source voltage of a FET.
V_{on}	OLED turn-on voltage.
V_r	Row-line voltage drop in a PM OLED display.
V_T	FET threshold voltage.
$ V_0 $	Top contact voltage drop in an AM OLED display.
$V(\lambda)$	Relative spectral luminous efficiency function for photopic vision.
w	FET channel width.
W	Display width.
W_c	Column-line width in a PM OLED display.
W_r	Row-line width in a PM OLED display.
ΔP	Power penalty.
χ	Fraction of recombinations that result in singlet excitons.
η	OLED quantum efficiency.
η_e	Fraction of emitted photons that can escape an OLED.
η_E	OLED energy conversion efficiency.

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η_F	EL material fluorescent efficiency.
η_L	OLED luminous efficiency.
η_r	Relative efficiency for a full-color strategy.
η_{re}	Fraction of electrons and holes that recombine in the emissive layer of an OLED.
μ_{FET}	FET channel field-effect mobility.

I. INTRODUCTION

THE RAPID progress recently made in organic light-emitting devices (OLED's) creates great potential for developing lightweight high-resolution full-color flat-panel displays (FPD's) [1], [2]. The recently demonstrated advantages of OLED's include high brightness, high efficiency, and low cost [1]–[5]. Furthermore, unique properties of organic electroluminescent (EL) and charge transport materials may lead to novel applications such as head up [6], [7], flexible, roll up, ultralightweight [8], [10], [11], and high-resolution [12], [13] displays. Several publications [2]–[5] have reviewed the status of organic EL technology, examined its performance and manufacturing advantages over alternative technologies, and speculated on its possible evolution. A systematic and quantitative study on the design and limitations of OLED-based FPD's, however, has to our knowledge not been reported.

Starting with an analysis of a single OLED, in this paper we report a systematic study of the design of OLED-based FPD's. This paper is organized as follows. In Section II, the photometry and efficiency of a single OLED is addressed, and methods to improve the contrast of an OLED-based display are analyzed and compared. In Section III, addressing schemes for monochromatic displays are quantitatively studied and compared, and their limits and suitable applications are discussed. In Section IV, different methods to achieve full color are discussed and compared, and the drive schemes for a novel approach toward full color—the stacked OLED configuration [13]—are proposed. This paper focuses on high-performance small-molecule OLED's, although similar analyses can be used to examine the performance of displays based on polymer OLED's.

II. ANALYSIS OF THE SINGLE OLED

The structure of a conventional OLED [14] is shown in Fig. 1(a), with several variations provided in [4]. Electrons and holes are correspondingly injected from the cathode and anode and migrate through the electron and hole transport layers. Electroluminescence is generated by radiative recombination of these carriers near the interface between the two transport layers. The device current versus voltage (I – V) characteristics, which are well described in previous work [15], can be approximated as follows: At lower voltages ($V < V_{on}$), $I = V/R_e$, indicating ohmic behavior; whereas at higher operating voltages ($V > V_{on}$), $I = KV^{m+1}$ with $m \sim 6$ –10, suggestive of trap-limited conduction characteristic of small-molecule OLED's [15]. Here, V_{on} is the turn-on voltage defined as the voltage at which the currents due to ohmic and trap-limited conduction [15] are equal; R_e is the effective resistance of the OLED at low voltages; and K is a proportionality constant. Fig. 1(b) shows a second OLED

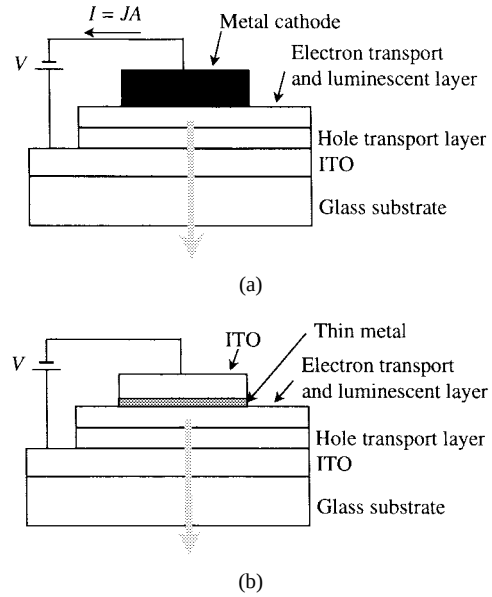


Fig. 1. OLED structures. (a) A conventional heterostructure OLED. (b) A transparent OLED, or TOLED.

structure [6], [7], [9], [10] to be considered in this study—a transparent OLED (or TOLED) that has been demonstrated using the unique property that many organic EL materials are transparent to their own emission due to the red shift of their EL spectra from their absorption bands [15]. A very thin metal film (~ 100 Å) combined with an ITO cap is used as the transparent, electron-injecting cathode. The TOLED's are 60%–90% transparent in the visible spectral region and emit light from both bottom and top device surfaces at quantum efficiencies approaching 1% when turned on [6], [10].

A. Photometry and Efficiency

To describe the emissive properties of an OLED, here we briefly define the radiometric and photometric quantities relevant to this study. Reference [16] provides a detailed discussion on radiometry and photometry. The radiant intensity of a light source in a given direction is the sum of the power contained in all the rays emitted in that direction by the entire source. The SI unit of the radiant intensity is W/sr. The radiant flux of a source is simply the total radiant power emitted from the source. Luminous flux, measured in lumens (lm), is the photometric equivalent of the radiant flux. The lumen is the power-like unit of brightness-sensation-producing ability [16]. Luminous intensity, equivalent to radiant intensity, is defined as the total number of lumens from a source emitted in a given direction. The unit of luminous intensity is therefore lm/sr, which has been renamed the candela (cd). The luminance of a specific segment of a source in a specific direction is defined as the luminous intensity emitted from that segment divided by the area of the segment's projection in that direction. The SI unit of luminance is cd/m^2 . Directly related to the human sensation of brightness, this quantity is often referred to as “brightness.” In this work, we use the word “luminance” in a more physical sense, and “brightness” in a more sensational sense. For example, for a fast pulsed source,

we talk about its *instantaneous* “luminance” and its *average*, *perceived* “brightness.”

Consider an OLED with an emissive area A , driven by a voltage V and a current density J , emitting an optical power P , at a quantum efficiency η . The luminous intensity, $I(\theta)$, in the absence of microcavity effects [17] has the same angular distribution [18] as the radiant intensity:

$$I(\theta) = \frac{I(0) \cos \theta}{\sqrt{1 - \left(\frac{1}{n_a}\right)^2 \sin^2 \theta}} \quad (1)$$

where θ is the angle between the viewing direction and the substrate normal, and n_a is the refractive index of the light-emitting material. Thus, the luminance in direction θ is

$$L(\theta) = \frac{I(\theta)}{A \cos \theta} = \frac{I(0)/A}{\sqrt{1 - \left(\frac{1}{n_a}\right)^2 \sin^2 \theta}}. \quad (2)$$

For $n_a = 1.7$, which is typical for many organic EL materials such as tris-(8-hydroxyquinoline) aluminum (Alq_3) [19], $L(\theta)$ increases monotonically from $L(0) = I(0)/A$ to $L(90^\circ) = 1.24I(0)/A$. Hence, the viewing cone of an OLED extends over the entire forward hemisphere.

The total luminous flux emitted by the OLED is

$$F = \int_{\text{half space}} I(\theta) d\Omega \equiv \pi C_n L(0) A \quad (3)$$

where $C_n \equiv 2n_a^2(1 - \sqrt{1 - 1/n_a^2})$. Assuming that the normalized emission power spectrum of the OLED is $\phi(\lambda)$, where $\int_0^\infty \phi(\lambda) d\lambda = 1$, the luminous flux F , and optical power P are related via

$$F = \left[683 \int_{\lambda_1}^{\lambda_2} V(\lambda) \phi(\lambda) d\lambda \right] P \equiv C_V P \quad (4)$$

where $\lambda_1 = 380$ nm, $\lambda_2 = 780$ nm, and $V(\lambda)$ is the relative spectral luminous efficiency function for photopic vision [16]. The emitted optical power is related to the drive current density via

$$P = \frac{\eta J A}{\frac{q}{hc} \int_0^\infty \lambda \phi(\lambda) d\lambda} \equiv \frac{\eta J A}{C_E} \quad (5)$$

where h is Planck's constant, c is the speed of light, and q is the electron charge. Using (3)–(5), we obtain

$$J = \frac{C_n C_E \pi L(0)}{C_V \eta}. \quad (6)$$

The constants C_n , C_E , and C_V depend on the refractive index or the emission spectrum of the EL material. For an OLED using Alq_3 as the emissive material, $C_n = 1.1$, $C_V = 427$ lm/W, and $C_E = 0.44$ V⁻¹. Equation (6) gives the drive current density required to achieve a given luminance. The current density versus luminance curves are shown for different η in Fig. 2 for undoped Alq_3 -based OLED's. A luminance of 100 cd/m² is usually considered sufficient for video displays (at least 35 cd/m² is required by ANSI standards

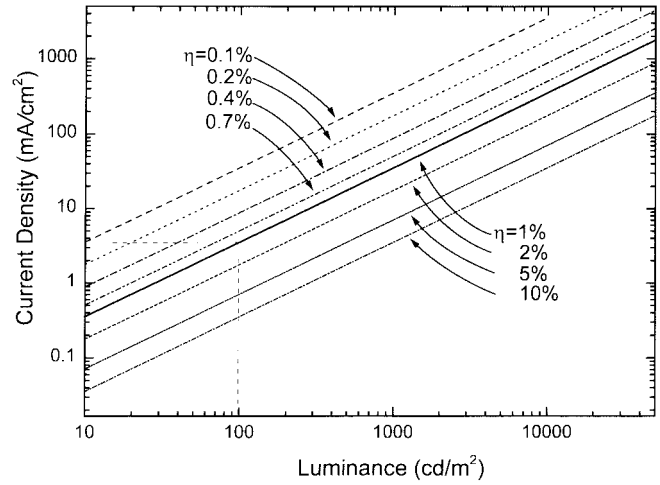


Fig. 2. Current density versus luminance curves for nondoped Alq_3 -based OLED's. The parameter η is the quantum efficiency of the OLED's.

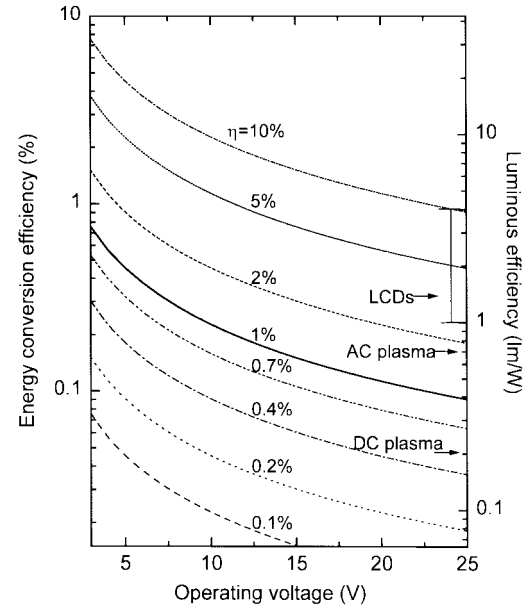


Fig. 3. Energy conversion efficiency and luminous efficiency as functions of OLED drive voltage. Also shown are the values of luminous efficiencies for other FPD technologies.

[20], corresponding to a drive current density of only 3.6 mA/cm² for $\eta = 1\%$, which is typical of undoped Alq_3 -based devices.

The energy conversion efficiency is $\eta_E = P/JAV = \eta/C_E V$, and the luminous efficiency is $\eta_L = F/JAV = \eta/[(C_E/C_V)V] = C_V \eta_E$. Fig. 3 shows the energy conversion and luminous efficiencies versus operating voltage for Alq_3 -based OLED's with η as a parameter. For such devices at a drive voltage $V = 10$ V, a quantum efficiency of 1.0% is equivalent to a luminous efficiency of 1.0 lm/W, which is higher than that achieved with plasma displays, as shown in Fig. 3. (Here, 0.2 lm/W is typical for dc and 0.7 lm/W for ac plasma displays) [21]. Although the fluorescent backlights for liquid crystal displays (LCD's) have an efficiency of 15–30 lm/W [4], the overall luminous efficiency of LCD's is about 1–3 lm/W, since the polarizing optics block 85%–90% of the

light [5] and the nonunity aperture ratio (defined as the ratio of the emissive area to the total pixel area) of active matrix LCD's (AMLCD's) leads to further loss [4].

To compare the efficiency of OLED's to alternative technologies, a discussion of the fundamentally attainable OLED quantum efficiency is useful. The maximum external quantum efficiency of an OLED can be expressed as $\eta = \eta_F \chi \eta_{re} \eta_e$, where η_F is the fluorescent quantum efficiency of the light-emitting material, χ is the fraction of recombinations that result in singlet excitons, η_{re} is the fraction of electrons and holes that recombine in the emissive layer, and η_e is the fraction of photons that can escape the device [4]. For Alq_3 , $\eta_F = (30 \pm 5)\%$ [19], typical of electron transporting EL materials. The OLED quantum efficiency, however, can be increased by doping the electron transport layer with a high-fluorescent (near unity) efficiency dye [22], [23]. A widely accepted hypothesis for the fraction of singlets [4] is $\chi = 1/4$ due to the relative spin degeneracy of singlets and triplets. We note that χ may deviate in the case of doped systems. Further, η_{re} can be near unity if unipolar current is completely blocked. The waveguiding in the device layers limits η_e to $\sim 1/(2n_a^2)$, which for typical EL materials such as Alq_3 , gives $\eta_e \cong 17\%$. This fraction, along with χ , limits the quantum efficiency of an OLED on a conventional planar substrate to below 5%. The fraction η_e , however, can be improved by using a shaped glass substrate, where each OLED is grown on a raised mesa [18]. Hence, the rays which would otherwise be waveguided are reflected into the forward direction by the sidewalls of the mesa. This substrate geometry has been demonstrated to increase the OLED external efficiency by at least a factor of 2. Another advantage of the shaped substrate is that it permits a 100% aperture ratio if interconnections are placed on or above the side wall surfaces [18]. Using these numbers, the best case quantum efficiency of an OLED is $\eta \cong 1 \times 0.25 \times 1 \times 0.34 = 8.5\%$.

To obtain a general prospect of the efficiency of state-of-the-art OLED's, typical recent values of η and η_L at a given voltage, V , for OLED's based on various materials are listed in Table I, along with corresponding emission colors. The listed efficiency and voltage values correspond to video luminance. High-quantum efficiency has already been achieved for all the primary colors. The relatively low η_L for red and blue OLED's is due to the low sensitivity of the eye, i.e., $V(\lambda)$ is small in those spectral regions (e.g., $V(480 \text{ nm}) = 0.139$ and $V(650 \text{ nm}) = 0.107$).

The total OLED power consumption required for a display to achieve a given luminance is $P_i = C_n \pi L_d A_P / \eta_L$, where A_P is the panel area, and L_d is the average display brightness which may be different from the instantaneous pixel luminance, $L(0)$, due to drive schemes as discussed in the next section. Fig. 4 shows P_i required to achieve a 100 cd/m^2 luminance versus the display panel diagonal dimension for OLED panels with various η_L . In this calculation, the refractive index of the EL material is assumed to be $n_a = 1.7$ (corresponding to $C_n = 1.1$), which is typical for most small-molecule organic EL materials. For $\eta_L = 1 \text{ lm/W}$, the total OLED power consumption required to achieve a 100 cd/m^2 luminance for a 17-in diagonal FPD is only 31 W. As shown in

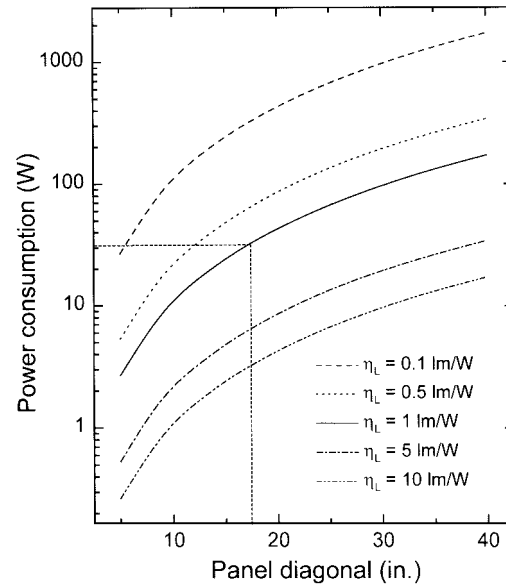


Fig. 4. Total OLED power consumption required to achieve a 100 cd/m^2 brightness versus the display panel diagonal for Alq_3 -based OLED's. The aspect ratio is assumed to be 3:4.

TABLE I
TYPICAL VALUES OF CIE COORDINATES, QUANTUM EFFICIENCY,
AND LUMINOUS EFFICIENCY AT A GIVEN OPERATING
VOLTAGE FOR OLED'S BASED ON VARIOUS MATERIALS

EL Material	EL color	CIE coordinates	η	η_L at operating voltage V	Reference
Un-doped Alq_3	Green	$x = 0.216$ $y = 0.376$	1%	1 lm/W^* @ 10 V	22, 24
Quinacridone in Alq_3	Green		$\sim 4.8\%^*$	12 lm/W @ $\sim 5 \text{ V}$	24
Perylene in BAlq	Blue	$x = 0.163$ $y = 0.194$	1.2%	0.56 lm/W @ 10 V	3
DSA amine in DPVBi	Blue		2.4%	6 lm/W @ $\sim 5 \text{ V}$	25
Alq_3 :OPh	Blue	$x = 0.20$ $y = 0.32$	0.49	0.3 lm/W @ 10 V	9
DCJT in Alq_3	Red	$x = 0.616$ $y = 0.381$	2.5%	1.3 lm/W @ 9 V	3
TPP in Alq_3	Red	$x = 0.68$ $y = 0.32$	0.11%	0.01 lm/W^* @ 15 V	13, 26
DCM in Alq_3	red	$x = 0.64$ $y = 0.36$	0.1	0.01 lm/W^* @ 10 V	27

* Calculated from data supplied by original work.

Table I, OLED's with a luminous efficiency $> 10 \text{ lm/W}$ have already been demonstrated by doping the EL active layer [23], making the OLED superior to alternative technologies such as liquid crystal and plasma displays.

B. Contrast

The high reflectance of the metal alloy cathode of an OLED leads to a low-pixel contrast ratio (PCR) in high-ambient illuminance. Here, we quantify the PCR by defining the discrimination ratio as the ratio of the brightness of an "on" pixel to that of an "off" pixel [28]. The brightness of an "off" OLED is taken to be solely due to the reflection of the ambient illuminance, E_a , which is assumed to have a uniform angular distribution. The "off" pixel brightness is, therefore, $L_{\text{off}} = RE_a/2\pi$, where R is the reflectance of the pixel measured from the substrate side. The "on" pixel

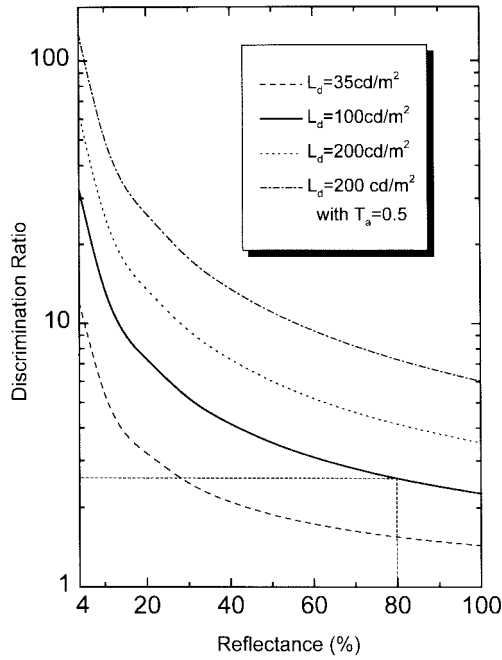


Fig. 5. Discrimination ratio versus OLED reflectance curves under a 500 lux ambient illuminance.

brightness is $L_{\text{on}} = L_d + L_{\text{off}}$. The discrimination ratio is, therefore, $D = 1 + (2\pi L_d / RE_a)$, which is plotted in Fig. 5 as a function of R under $E_a = 500$ lux (ANSI standard) [20] for different display brightnesses. For $L_d = 100 \text{ cd/m}^2$ and $R = 80\%$, $D = 2.6$. Discrimination ratios >5 can only be achieved with a display brightness $>200 \text{ cd/m}^2$ for high-reflectance pixels under this ambient lighting condition. To increase D , the reflection of ambient light must be suppressed.

A circular polarizer (CP) can be placed in front of the display to achieve high-discrimination ratios. Although the quarter-wave plate in the CP is wavelength dependent, the reflected ambient light can be sufficiently attenuated if the quarter-wave plate is centered near $\lambda = 555 \text{ nm}$, where $V(\lambda)$ is maximum. This is due to the broad spectral width of the CP blocking band, coupled with the insensitivity of the eye to the wavelengths in the tails of $V(\lambda)$. A zeroth-order quarter-wave plate is desirable to obtain a broad blocking band for the CP [29]. To analyze the improvement in D for this and the following schemes, we assume that the front surface of the display is antireflection (AR) coated, and thus we can neglect Fresnel reflections at this surface. Here, the front of the display is the polarizer surface facing the viewer. Assuming a uniform spectral distribution for the ambient illuminance, a zeroth-order quarter-wave plate centered at $\lambda = 555 \text{ nm}$, and a 100% efficiency for the CP, the luminance due to reflected ambient light is found to be attenuated by a factor of 71, while the emitted light is only attenuated by a factor of 2. Hence, for a display with $L_d = 200 \text{ cd/m}^2$ (corresponding to a 100 cd/m^2 perceived brightness) and $R = 80\%$ under a 500 lux ambient illuminance, D is increased to 113.

To quantify the energy loss of a particular contrast-enhancing, addressing, or full-color scheme, we define the power penalty (ΔP) resulting from the scheme as the increase in electrical power required to achieve the same

brightness which would be achieved without employing the enhancement scheme. The power penalty of the CP scheme is $\Delta P = 2^{m+2/m+1} \approx 3 \text{ dB}$, where $m+1$ is the power law exponent in the I - V dependence. Although D is significantly improved by the CP, a problem of this scheme is that the phase retardation of the quarter-wave plate and the contrast of the linear polarizer depends on the viewing angle. Polarizers of any type reduce the useful viewing angle of a display to 45° from the normal [28]. Hence, the use of CP's is only suitable for displays with a limited viewing angle. Another problem is cost and complexity: The quarter-wave plate and the linear polarizer must be aligned. In addition, the fabrication of zeroth-order wave plates is complicated, resulting in higher cost for this already complex scheme. The use of multiple-order quarter-wave plates (with a phase retardation $2n\pi + \pi/2$, where the integer $n \neq 0$) will reduce the blocking bandwidth and increase the viewing angle sensitivity of the CP.

An alternative scheme to increase the discrimination ratio employs an absorber with an optical transmittance, T_a , placed in front of the display. In this case, $D = 1 + (2\pi L_d / T_a RE_a)$, since the background light passes through the absorber twice while the emitted light passes through only once. However, the display luminance is decreased to $T_a L_d$, leading to a power penalty of $\Delta P = T_a^{-(m+2/m+1)}$. If $T_a = 0.5$, then $L_d = 200 \text{ cd/m}^2$ is required to achieve a 1 cd/m^2 perceived brightness. In this case, the discrimination ratio increases to 7.3 for $R = 80\%$ at a power penalty of $\Delta P = 2^{m+2/m+1} \approx 3 \text{ dB}$. The D - R curve for this case is also shown in Fig. 5.

Finally, a high-contrast display can also be realized using TOLED's [6] with an absorbing background. Most of the energy of the incident ambient light is transmitted through the TOLED's and absorbed, while the backward propagating EL is also absorbed, leading to a power penalty of $2^{m+2/m+1}$. In this case, $D = 13.6$ for $L_d = 100 \text{ cd/m}^2$ if a 10% residual reflectance resulting from the semitransparent cathode [6] [see Fig. 1(b)] is assumed. Hence, this simple scheme provides sufficient improvement in D at the same power penalty as the other schemes, without encountering problems of viewing angle dependence and increased cost arising from inclusion of expensive optics and filters in the display.

III. ADDRESSING SCHEMES FOR MONOCHROMATIC DISPLAYS

A display is an array of independently controllable pixels, the number of which depends on its dimension and resolution required by a particular application. Very large pixel counts are encountered in high-information content displays. For example, an NTSC standard TV screen requires 1.5×10^5 pixels. The addressing of a large number of pixels in an array is an important issue in the display technology. Among the five addressing schemes used in electronic displays [28], direct addressing and matrix addressing are suitable for OLED-based systems. The direct addressing scheme, where each pixel is connected to an individual driver, can only be used for discrete indicators and simple alphanumeric displays with few characters. In this case, complex character patterns can be realized using shadow masks. By comparison, inorganic LED alphanumeric displays are expensive to fabricate because

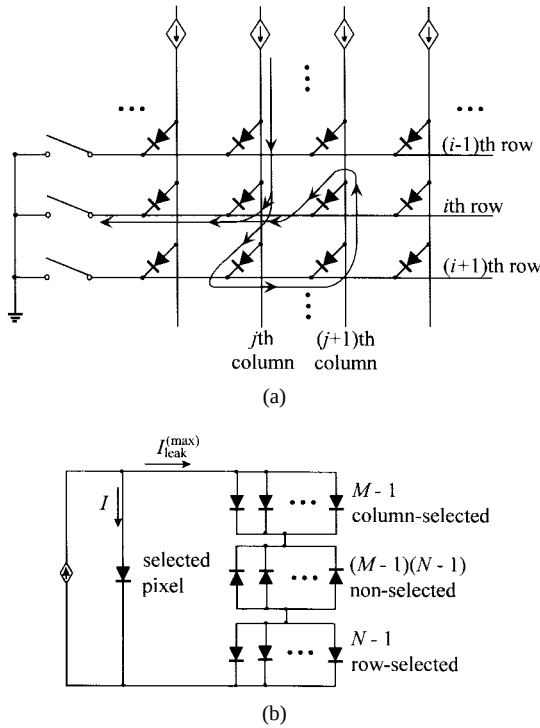


Fig. 6. (a) The circuit diagram of a PM OLED array. An OLED is represented by a diode. (b) The equivalent circuit of a PM OLED array when only one pixel is selected.

of the many individual diodes required to make up a single character, each with its own contacts and leads [30].

In a matrix addressed display, pixels are organized in rows and columns, and each pixel is electrically connected between one row lead, and one column lead. The addressing schemes where active electronic components are added to the pixels are called active matrix (AM) addressing; while those without extra active components in the pixels are termed passive matrix (PM) addressing. Matrix addressed OLED arrays can enable the realization of high-information content, large-area FPD's.

A. Passive Matrix Addressing

A passive matrix OLED (PM OLED) array consists of two sets of electrically isolated leads (rows and columns) arranged orthogonally with an OLED at each intersection, as shown in Fig. 6(a). An electronic switch is employed to address each of the rows. To achieve gray levels, the column drivers must be current sources since the pixel luminance is proportional to the drive current, and the I - V characteristics of the OLED's are highly nonlinear as discussed in Section II.

Such a monochromatic, PM OLED display prototype has recently been demonstrated [23]. Here, we quantitatively study an N (columns) $\times$ M (rows) PM array of identical OLED pixels, with W_r wide rows separated by gaps of width D_r , and W_c wide columns separated by gaps of width D_c . The aperture ratio of this display is $r_a = W_r W_c / [(W_r + D_r)(W_c + D_c)]$. Unintentional direct coupling occurs when pixels in different rows are simultaneously addressed. For example, when pixel (i, j) (the pixel at the intersection of the i th row and j th column) and pixel (i', j') are simultaneously addressed, pixels (i, j') and (i', j) are unintentionally selected. Therefore, the

array must be addressed pixel-at-a-time or row-at-a-time to prevent direct coupling. The row-at-a-time mode is chosen to maximize the pixel duty factor (defined as the percent of the total time each pixel is driven into the "on" state by the column signal). The pixel duty factor of such a row-scanned array is $1/M$. Fig. 6(a) shows that a large number of pixels are unintentionally reverse biased when a pixel is addressed. Here, reverse bias is defined as applying a negative voltage to the ITO anode with respect to the metal cathode. For example, when pixel (i, j) is addressed, in the circuit branch containing pixels $(i, j+1)$, $(i+1, j+1)$, and $(i+1, j)$, pixel $(i+1, j+1)$ is reverse biased [see Fig. 6(a)]. Hence, an addressed pixel must be driven with a pulsed current at a duty cycle, d , to avoid catastrophic, irreversible breakdown (or shorting) caused by long term reverse bias on the nonselected pixels. To achieve an average display luminance of L_d , the pixels must, therefore, be driven to an instantaneous luminance of:

$$L(0) = M L_d / (r_a d). \quad (7)$$

This requirement, which may limit the number of rows in a display, must be considered in the design. The only published, experimental data on OLED maximum *instantaneous* luminance, to our knowledge, were reported by Nakamura *et al.* [31] and Hosokawa *et al.* [25]. Nakamura *et al.* reported [31] an instantaneous luminance of 10^4 cd/m² for a blue-emitting OLED, which enables a 50-row PM display if $d = 50\%$ and $r_a = 100\%$. The same group later demonstrated [25] a pulse emission of 5×10^4 cd/m², enabling 250-line PM addressing under these same conditions. Two reviews [32], [33] state that luminance of over 10^5 cd/m² has been reported without referring to the original work. Even such a high-maximum luminance limits the display row number to 500 for $d = 50\%$ or ~ 1000 for $d \approx 100\%$. Besides limiting the number of rows, the high-instantaneous luminance requirement also lowers the OLED power conversion efficiency η_E by increasing the drive voltage.

As discussed above, leakage currents flow through unintentionally formed circuit branches comprising reverse-biased OLED's when a pixel is addressed. The total leakage current drawn from a column driver through all the similar branches depends on the brightness profile of the addressed row. Two extreme cases are considered: 1) all the pixels in the selected row are driven to the same brightness and 2) one pixel, (i, j) , in the addressed row is driven to full brightness (by a current I , corresponding to a voltage V), with all others turned off. In case 1), the voltages across all the pixels in the addressed row are equal, and thus the voltage drops across the remaining pixels are zero. The total leakage current through other pixels is, therefore, also zero. In case 2), the array is represented by an equivalent circuit [28] shown in Fig. 6(b). For convenience, we refer to the pixels in the addressed row except pixel (i, j) itself as "row-selected pixels;" the pixels in the j th column except pixel (i, j) itself as "column-selected pixels;" and all others as "nonselected pixels." When driven by a current I , the voltage V across pixel (i, j) is also applied to the branch composed of the row-selected, nonselected, and column-selected pixels, forcing a leakage current, $I_{leak}^{(max)}$, through this branch. In the

intermediate cases (where the pixels in the addressed row are driven to different brightnesses), the leakage current extracted from each column driver is less than $I_{\text{leak}}^{(\text{max})}$, since less voltage is dropped along the leakage current paths as compared to case (2). Hence, the leakage current extracted from each column driver ranges from zero to $I_{\text{leak}}^{(\text{max})}$, depending on the brightness profile of the selected row. Assuming the current source provides a fixed current for a given pixel brightness, the current I actually flowing through an addressed pixel depends on the leakage current. The criterion $I_{\text{leak}}^{(\text{max})} \ll I$, which limits the array size as discussed below, must be met, not only to lower the display parasitic drive power penalty caused by the leakage, but also to achieve good brightness control. For a display with N_g gray levels, the condition $I_{\text{leak}}^{(\text{max})} \leq I_{\text{max}}/N_g = I_{\text{min}}$ should be satisfied, where I_{max} and I_{min} are drive currents corresponding to the full brightness and the lowest nonzero gray level, respectively.

Since the leakage current paths in a PM OLED array follow the reverse-biased pixels, a quantitative leakage current analysis calls for knowledge of OLED I - V characteristics under reverse bias. However, no quantitative and systematic study on this subject has thus far been reported to our knowledge. Hence, we briefly discuss the OLED reverse biased I - V behavior measured in our laboratory by comparing the reverse and forward currents at voltages of same magnitudes, $|V|$, but opposite polarity. A more complete study of the reverse-biased I - V characteristics will be published elsewhere. The rectification ratio, defined as the ratio of currents corresponding to same magnitudes of forward and reverse voltage, is between ~ 1 – 10^2 (depending on the voltage) for OLED's using 4,4'-bis[N -(1-naphthyl)- N -phenyl-amino]biphenyl (α -NPD) or N,N' -diphenyl- N,N' -bis(methylphenyl)1-1'-biphenyl-4,4'-diamine (TPD) as the hole transport material, Alq₃ as the electron transport and EL material, and Mg-Ag alloy as the cathode material [34]. In our laboratory, we found [34] that the insertion of an additional hole injection layer, e.g., copper phthalocyanine (CuPc) between the anode and hole transport layer, improves the rectification ratios at most operational voltages ($|V| > V_{\text{on}}$) to $\geq 10^3$. The reverse biased I - V behavior at lower voltages, however, are of more importance in the analysis of leakage current here, since the total voltage V is divided between the row-selected, nonselected, and column-selected pixels [see Fig. 6(b)]. We also found [34] that for both OLED structures discussed above, the reverse biased I - V dependence at lower voltages follows an ohmic behavior, i.e., $I = V/R_{\text{rev}}$, where $R_{\text{rev}} \sim R_e$.

We assume that the reverse biased I - V behavior of an OLED follows $I_{\text{rev}} = f_{\text{rev}}(V_{\text{rev}})$, where the reverse current, I_{rev} , and reverse voltage, V_{rev} , are taken as positive values. Hence, $I_{\text{leak}}^{(\text{max})}$ can be found by solving

$$I_{\text{leak}}^{(\text{max})} = (N-1)f(V_1) \quad (8)$$

$$I_{\text{leak}}^{(\text{max})} = (M-1)(N-1)f_{\text{rev}}(V_2) \quad (9)$$

$$I_{\text{leak}}^{(\text{max})} = (M-1)f(V_3) \quad (10)$$

$$V_1 + V_2 + V_3 = V \quad (11)$$

where V_1 , V_2 , and V_3 are the voltages across the column selected, nonselected, and row selected pixels, respectively, and

$$f(V) = \begin{cases} V/R_e, & V < V_{\text{on}} \\ KV^{m+1}, & V > V_{\text{on}} \end{cases}$$

represents the forward bias I - V characteristics.

Since $f_{\text{rev}}(V)$ depends on the OLED structure and $f(V)$ behaves differently in the low- and high-voltage regimes, the solving of (8)–(11) involves a large number of different cases. Here we only discuss two special cases. In the case of lower brightness where the drive voltage V across the addressed pixel is sufficiently low such that V_1 , V_2 , and V_3 are less than V_{on} , each column- or row-selected OLED in Fig. 6(b) can be effectively represented by a resistor, R_e . Assuming $M \gg 1$ and $N \gg 1$, V_2 is negligibly small compared to V_1 and V_3 . With these simplifying assumptions, we have

$$V_1 = \frac{N-1}{M+N-2} V \quad (12)$$

and

$$I_{\text{leak}}^{(\text{max})} = \frac{(M-1)(N-1)}{M+N-2} \cdot \frac{V}{R_e}. \quad (13)$$

Assuming $N > M$, the above analysis is valid if $V_1 < V_{\text{on}}$, i.e., if $V < V_{\text{on}}(M+N-2)/(N-1)$ is satisfied. In this case, if the drive voltage across the addressed pixel is sufficiently low, small OLED rectification ratios do not appreciably increase the leakage current. Thus, it is the strong nonlinearity in the OLED forward biased I - V behavior that allows for the efficient operation of a PM OLED array in this case. For large M and N , the condition $I_{\text{leak}}^{(\text{max})} \leq I_{\text{min}}$ becomes

$$I_{\text{min}} \geq \frac{MN}{M+N} \cdot \frac{V(I_{\text{min}})}{R_e} \quad (14)$$

where $V(I_{\text{min}})$ is the drive voltage corresponding to the current I_{min} .

In a PM addressed display, the instantaneous pixel luminance required to achieve a given average display brightness L_d is proportional to the number of rows, M , as discussed previously. Hence, for large M , a large current and a correspondingly high voltage are required to drive the pixel to a sufficient brightness. If very high-instantaneous pixel luminance is required, the condition $V < V_{\text{on}}(M+N-2)/(N-1)$ can not be satisfied, giving rise to the second case we consider here. Assuming high-rectification ratios (larger than M and N) for the OLED's, V_1 , and V_3 are clamped at V_{on} , with the extra voltage dropped across the nonselected pixels. The leakage current in this case is, therefore,

$$I_{\text{leak}}^{(\text{max})} = (M-1)(N-1)f_{\text{rev}}(V-2V_{\text{on}}). \quad (15)$$

For large pixel numbers, $I_{\text{leak}}^{(\text{max})} \cong MNf_{\text{rev}}(V-2V_{\text{on}})$. Hence, for high-rectification ratio OLED's, the condition that $I_{\text{leak}}^{(\text{max})} \leq I_{\text{max}}/N_g$ becomes

$$f(V)/f_{\text{rev}}(V-2V_{\text{on}}) \leq MNN_g. \quad (16)$$

Assuming the turn-on voltage is $V_{\text{on}} = 3.5$ V and the OLED's operate at $V = 10$ V, the ratio $f(V)/f_{\text{rev}}(V-2V_{\text{on}})$

is $\sim 10^5$, limiting the pixel number $N \times M$ to $\sim (84 \times 72) = 6048$ for a display with $N_g = 16$ gray levels. A 512×384 display with 64 gray levels is possible with the ratio $f(V)/f_{\text{rev}}(V - 2V_{\text{on}})$ increased to $\sim 10^7$.

In short, when designing an PM OLED display, the leakage current should be examined as follows: For a given display logical size (number of rows and columns) and physical layout, first determine the pixel instantaneous luminances required by the highest and lowest brightnesses using (7). Then use (6) to find the corresponding device current densities J , which determines the drive voltages, V . Finally, $I_{\text{leak}}^{(\text{max})}$ is found for both the highest and lowest gray levels by solving (8)–(11), following the criterion that $I_{\text{leak}}^{(\text{max})} \leq I_{\text{max}}/N_g = I_{\text{min}}$.

Currents flowing through the row and column lines, along with the finite resistance of these lines, give rise to the row-line and column-line voltage drops, which may limit the operation of a PM OLED array. Assuming that all the pixels in an addressed row are driven to full brightness, L_d , by a current density, J , the voltage drop on a row line is $V_r = JW_c R_{\text{sq}} [Nl_e + N(N-1)(W_c + D_c)/2]$, where R_{sq} is the sheet resistance of the row line, and l_e is the lead length between the panel edge and the first pixel at the array edge. For large N ,

$$V_r \cong JW^2 R_{\text{sq}}/2 = \frac{C_n C_E \pi}{C_V \eta} \cdot \frac{L_d}{r_a d} \cdot MW^2 R_{\text{sq}}/2 \quad (17)$$

where $W = N(W_c + D_c)$ is the width of the array. The voltage drop along a column line is

$$V_c = JW_r H R_{\text{sqc}} = \frac{C_n C_e \pi}{C_V \eta} \cdot \frac{L_d}{r_a d} \cdot \frac{W_r}{W_r + D_r} \cdot H^2 R_{\text{sqc}} \quad (18)$$

where H and R_{sqc} are height of the array and sheet resistance of the column lines, respectively. Since $V_r \propto MW^2$ while $V_c \propto H^2$, metal cathode lines are used as row lines due to their low resistance.

Fig. 7 shows the row-line voltage drop versus the array width for $L_d = 100 \text{ cd/m}^2$, $r_a = 80\%$ and $d = 50\%$, in the case that both ends of the row line are connected to the drive circuit. Hence, V_r is equal to half the value given by (17). The row-line sheet resistance, $R_{\text{sq}} = 0.03 \text{ } \Omega/\square$, corresponding to a 1000-Å-thick Mg–Ag cathode with a 5000-Å-thick Ag cap, is typical for top metal contacts, while $R_{\text{sq}} = 4 \text{ } \Omega/\square$ is the sheet resistance for a 100-Å-thick Mg–Ag semitransparent cathode with an ITO cap for TOLED's. To decrease row-line voltage of a PM TOLED array, metal wires parallel to the rows can be predeposited on the substrate, necessitating photolithographic patterning of the organic layers and the row electrode. Assuming $W_r = W_c = 100 \text{ } \mu\text{m}$, Fig. 7 also shows the row-line voltage of a PM TOLED array with 150 Ω/cm (10 μm wide, 1000-Å-thick Ag) predeposited row wires at the same conditions as above.

The power penalty (ΔP) incurred by passive matrix addressing due to the row-line voltage drop is negligible since the power consumption on an addressed row line due to the current through each pixel is negligibly small. Fig. 8 shows V_c and ΔP versus the array height for $L_d = 100 \text{ cd/m}^2$, $r_a = 80\%$, $d = 50\%$, $W_r/(W_r + D_r) = 0.9$, and $R_{\text{sqc}} = 20 \text{ } \Omega/\square$, where both ends of the column line are once again

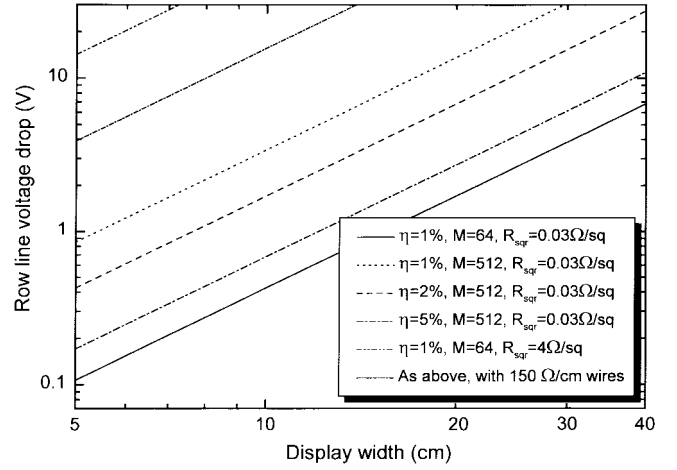


Fig. 7. Row-line voltage drop versus display width curves for PM OLED displays with an aperture ratio $r_a = 80\%$ driven to a brightness $L_d = 100 \text{ cd/m}^2$ by column signals with a duty cycle $d = 50\%$. Row drive circuits are assumed to be placed on two, opposite sides of the display.

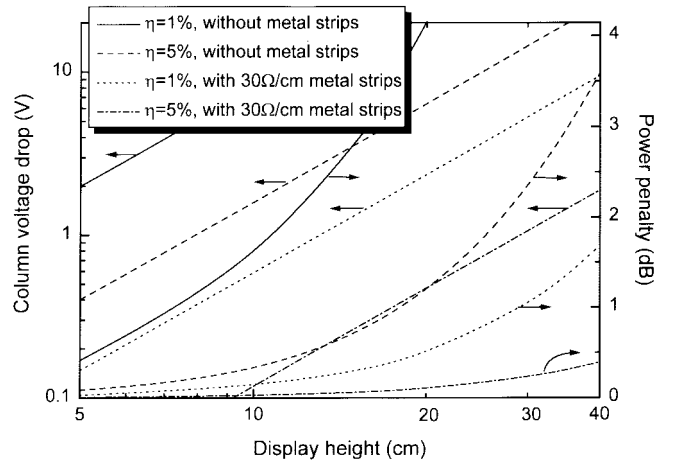


Fig. 8. Column voltage drop and the resulting power penalty versus display height for PM OLED displays with an aperture ratio $r_a = 80\%$ driven to a brightness $L_d = 100 \text{ cd/m}^2$ by column signals with a duty cycle $d = 50\%$. Column drive circuits are assumed to be placed on the two opposite sides of the display.

connected to the drive circuit, thereby halving V_c from the value given by (18). The power penalty, $\Delta P = 1 + V_c/(2V)$, due to the column voltage drop is also shown in Fig. 8 for an operating voltage $V = 10 \text{ V}$. Metal strips, which may reduce the aperture ratio, can be added along side of the ITO column lines to improve the column-line conductance for large arrays. Assuming $W_r = W_c = 100 \text{ } \mu\text{m}$ and $D_r = 10 \text{ } \mu\text{m}$, a calculation of V_c is shown in Fig. 8 for the case where 150 Ω/cm metal strips are used. The row-line and column-line voltage drops can be easily suppressed to a few volts for displays with width and height of $\sim 40 \text{ cm}$, and the power penalty is below 3 dB for most cases. Using a shaped substrate [18], the near 100% aperture ratio is unaffected by the use of wider metal strips.

Finally, we examine the time response of a PM OLED array. The EL response time of small-molecule OLED's has been found to be $< 1 \text{ } \mu\text{s}$ [25], [31], [35], sufficient for most pulse driven arrays. The electronic time response of an addressed

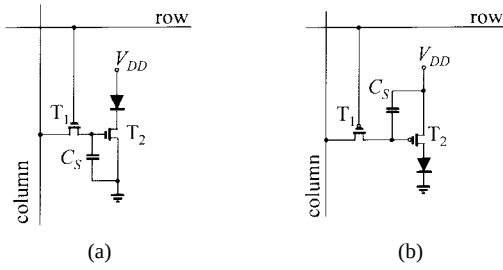


Fig. 9. Pixel circuit designs for AM OLED displays. (a) Using n-channel FET's. Organic inverted light-emitting devices, or OILED's are required in this scheme. (b) Using p-channel FET's.

pixel is estimated as follows. An OLED can be represented by a parallel connected resistance and capacitance. The equivalent resistance of a $100 \mu\text{m} \times 100 \mu\text{m}$ OLED pixel is $\sim 10^8 \Omega$, much higher than the output resistance r of the column drivers. When the condition $I_{\text{leak}}^{(\text{max})} \ll I$ is satisfied, the circuit branch composed of row-selected, nonselected, and column-selected pixels can be ignored when estimating the time constant [see Fig. 6(b)]. The equivalent capacitance C for the pixel is estimated to be $\sim 10^{-12}$ F, using $C = \epsilon A/z$, where $\epsilon \approx 10^{-13}$ F/cm is the permittivity of the organic materials, and $z \approx 1000 \text{ \AA}$ is the total thickness of the organic layers. Hence, the time constant of the addressed pixel is $\tau = rC \approx 0.6$ ns, assuming a driver output impedance $r = 600 \Omega$. Therefore, the OLED time response is not a limiting factor in the design of PM OLED displays.

In summary, PM OLED arrays have the merits of simple concept and fabrication, moderate power penalty, and fast time response. Nevertheless, their size is limited by: 1) the high-instantaneous pixel luminance required to achieve a given average display brightness due to the very low-pixel duty factor, limiting the number of rows to below ~ 1000 ; 2) the leakage current through the nonselected pixels, limiting the MNN_g product to below $\sim 10^7$ (corresponding to a 512×384 display with 64 gray levels); and 3) the voltage drops across the column and row lines, limiting the display dimension to below ~ 40 cm in width and height (or ~ 17 -in diagonal). Due to these limits, AM addressing is necessary for high-information content, large-area FPD's.

B. Active Matrix Addressing

In the active matrix addressing scheme, an electronic switch is placed at each pixel, providing the means to retain video information on a storage capacitor during a complete frame time. In the case of AM OLED displays, an additional active component is needed to provide the OLED drive current at each pixel. These active components can be field-effect transistors (FET's), such as crystalline Si metal-oxide-semiconductor field-effect transistors (MOSFET's) or thin-film transistors (TFT's), depending on the application. Here, the channel material for TFT's may be polycrystalline CdSe or Si of various crystallinity ranging from polycrystalline Si (poly-Si) to amorphous Si (*a*-Si). Poly-Si and *a*-Si TFT's have been used in AMLCD's, while CdSe TFT's are seldom used due to fundamental problems such as difficulties to deposit stoichiometric thin films, and lack of a highly insulating

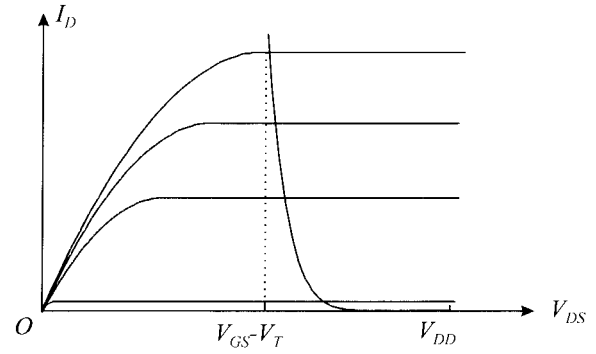


Fig. 10. The I_D - V_{DS} characteristics of n-channel FET's along with the load line resulting from the OLED I - V characteristics.

native oxide [36]. In addition, organic TFT's represent an emerging and promising technology for display applications. For example, a pentacene-based organic TFT has recently been demonstrated [37] with a field-effect mobility of $1.5 \text{ cm}^2/\text{Vs}$ and an on-off ratio of 10^8 , superior to the performance of *a*-Si TFT's.

A pixel design for an AM OLED display using n-channel FET's is shown in Fig. 9(a). When a row is selected, the column signal is written via the accessing transistor T_1 to the gate of the drive transistor T_2 . The written voltage V_{G2} is thereby retained for a complete frame time T_f . Transistor T_2 operates in the saturation regime, where the OLED drive current I is controlled by the gate-to-source voltage V_{GS2} and has little dependence on the source-to-drain voltage, V_{DS2} . The dc-voltage source V_{DD} may be replaced with a pulsed voltage source to achieve ac operation, which has been shown [38] to improve OLED lifetime.

This particular design can not be implemented using OLED's deposited in a conventional sequence, since the metal cathode must be the first layer to be deposited on the TFT backplane. This problem is solved by using top-emitting inverted OLED's [39], [40]. A polymeric, top-emitting, inverted OLED has been previously demonstrated [39], and a small molecule organic inverted light-emitting device (OILED) has also recently been reported [40]. The layers in a small-molecule-based OILED are deposited in the following sequence: a bottom metal cathode, an electron transport and EL layer, a hole transport layer, a protection layer, and finally, an ITO top anode. The top ITO is deposited using a very low-power room-temperature RF magnetron sputtering process, and the protection layer, composed of CuPc or 3,4,9,10-perylene-tetracarboxylic dianhydride (PTCDA), is employed to protect the underlying organic materials from bombardment damage in the sputtering process.

In an alternative configuration where the OLED and T_2 are integrated as has been demonstrated [41] with a polymer OLED integrated with an *a*-Si, n-channel TFT, the OLED is placed between the source of T_2 and ground. This configuration is easy to implement since it uses OLED's deposited in the conventional sequence with the metal cathode being the last (top) layer. The circuit shown in Fig. 9(a) is preferable, however, since in this case $V_{G2} = V_{GS2}$ directly controls the OLED current.

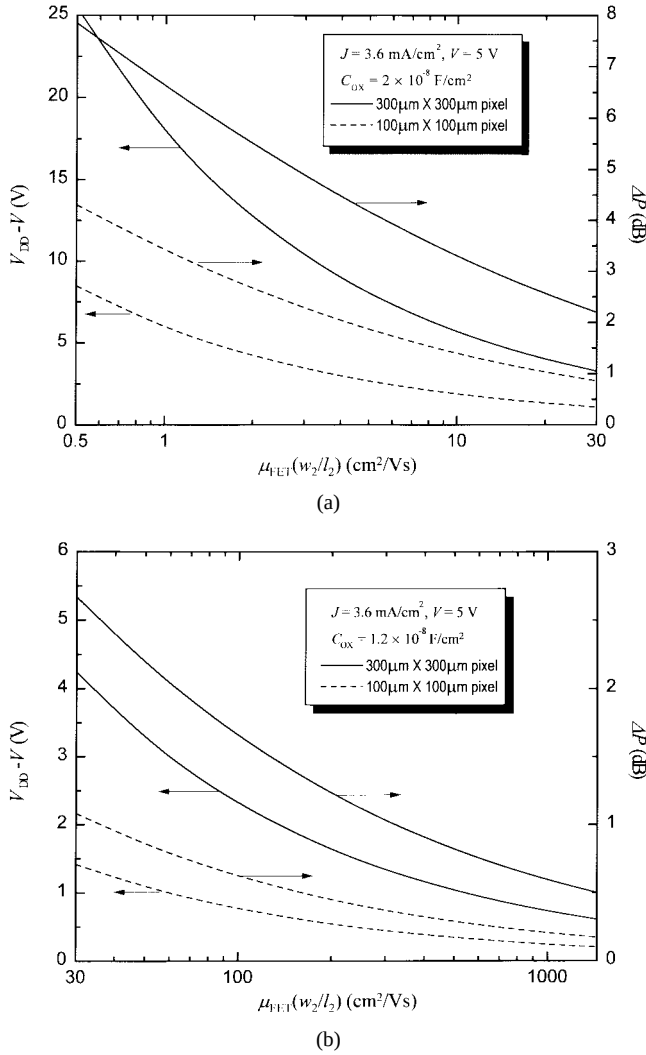


Fig. 11. Voltage drop on the drive transistor $V_{DD} - V$ and power penalty as functions of the $\mu_{FET}(w_2/l_2)$ product for (a) a -Si TFT's or organic TFT's, and (b) poly-Si TFT's or crystalline Si FET's.

The pixel circuit can also be implemented with p-channel FET's as shown in Fig. 9(b). Although this eliminates the need for OLED's, the performance of p-channel FET's is typically lower than that of n-channel FET's made from the same material, and only n-channel TFT's has thus far been realized using a -Si. Since the pixel circuit in Fig. 9(b) can be similarly analyzed to that in Fig. 9(a), the following discussion only focuses on the example circuit using n-channel FET's.

The I_D - V_{DS} characteristics of an n-channel FET are shown schematically in Fig. 10, along with the load line resulting from the OLED I - V characteristics. The knees in the I_D - V_{DS} curves between the linear and saturation regimes are at $V_{DS} = V_{GS} - V_T$, and the saturation currents are $I_D = \mu_{FET}C_{OX}(w/l)(V_{GS} - V_T)^2$, where μ_{FET} , C_{OX} , w , l , and V_T are the field-effect mobility, insulator layer capacitance per unit area, channel width, channel length, and threshold voltage of the FET, respectively [42]. The criterion for T_2 to operate in the saturation regime is $V_{GS2} - V_T \leq V_{DD} - V$, i.e.,

$$V_{DD} \geq V + \sqrt{\frac{2JA}{\mu_{FET}C_{OX}(w_2/l_2)}} \quad (19)$$

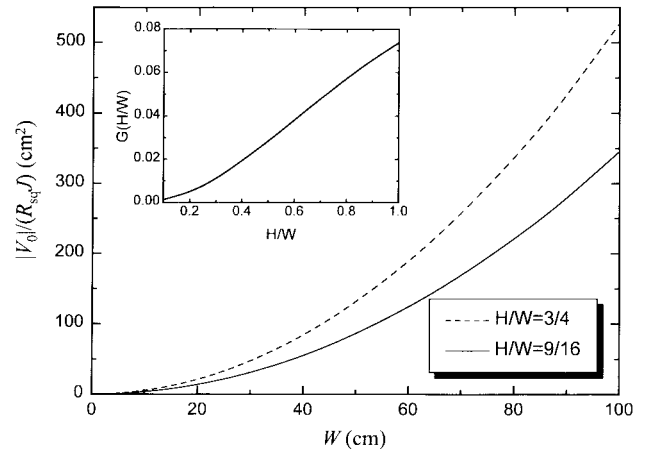


Fig. 12. Voltage drop $|V_0|$ from the edges to the center of the nonpatterned contact of an AM OLED display as a function of the display width, W . The voltage drop is normalized to $|V_0|/(R_{sq}J)$, where R_{sq} is the sheet resistance of the contact and J is the OLED current density. Inset: The function $G(H/W)$, where H is the display height.

TABLE II
FIELD-EFFECT MOBILITY AND ON-OFF RATIO
FOR TFT'S BASED ON VARIOUS MATERIALS

Channel material	Field effect mobility (cm ² /Vs)	on-off ratio
a -Si	0.6 ~ 1	10^7
n-type poly-Si	50 ~ 400	10^6
p-type poly-Si	15 ~ 70	10^6
pentacene	1.5	10^8

where JA is the OLED drive current required to achieve full brightness, and V is the corresponding OLED voltage. A low V_{DD} is desirable to achieve low-panel power consumption and to make the technology suitable for portable, battery-powered applications. The power penalty due to the introduction of T_2 is $\Delta P = V/V_{DD}$. For a pixel driven to full brightness, $\Delta P = 1 + \sqrt{(2JA/\mu_{FET}C_{OX}(w_2/l_2))/V}$. The channel width of T_2 , i.e., w_2 , is limited by the pixel dimension, l_2 is limited by short channel effects, C_{OX} is determined by the insulator layer thickness and material properties, and μ_{FET} depends on the channel material.

The voltage drop on the drive transistor $V_{DD} - V$ and power penalty ΔP are plotted versus $\mu_{FET}(w_2/l_2)$ in Fig. 11(a) for a -Si TFT's, and in Fig. 11(b) for poly-Si TFT's or crystalline Si FET's. Typical values of μ_{FET} for TFT's based on various channel materials are listed in Table II. In the case of a -Si TFT's, $V_{DD} - V$ is only a few volts, and $\Delta P < 3$ dB for high- w/l ratios as shown in Fig. 12(a). Further, $V_{DD} - V$ and ΔP are even lower for poly-Si TFT's or crystalline Si FET's with their significantly higher field mobility, μ_{FET} . Fig. 11(a) also applies to organic TFT's with comparable performance.

The analysis of T_1 is similar to that of the accessing transistor in AMLCD's [43], [44]. Assume that the gate potential of T_1 is $V_{G1} = V_H$ when a row is addressed, and the voltage on the column line is V_{sig} . At the end of the storage capacitor charging period, the pixel capacitance, C_{pix} (the sum of the storage capacitance C_S and the gate-to-source capacitance C_{GS2} of T_2), stores charge $C_{pix}V_{sig}$,

while the gate-to-source capacitance of T_1 , C_{GS1} stores charge $C_{GS1}(V_{\text{sig}} - V_H)$. When V_{G1} is brought to zero, the charge stored on C_{pix} and C_{GS1} will be redistributed. During the retention period, the output of T_1 is, therefore, $V_{G2} = V_{\text{sig}}[1 - C_{GS1}/(C_{GS1} + C_{\text{pix}}) \cdot (V_H/V_{\text{sig}})]$ [43]. To have $V_{G2} - V_{\text{sig}}$ during this period, it is important that $C_{\text{pix}} \gg C_{GS1}$, therefore necessitating a separate storage capacitance. Even with a large C_S , $V_{G2} < V_{\text{sig}}$ during the retention period. To eliminate this difference, C_S can be connected to the previous row instead of ground, and a compensation voltage [44] $V_{\text{comp}} = -(C_{GS1}/C_S)V_H$, can be applied to the nonselected rows.

The required on-off ratio of T_1 is estimated as follows: to charge C_S to a voltage V_{G2} within the addressing time, the on current, I_{on} , must satisfy

$$I_{\text{on}} \geq \frac{C_{\text{pix}} V_{G2\text{max}}}{T_f/M} \quad (20)$$

where $V_{G2\text{max}}$ is the maximum of V_{G2} corresponding to full brightness. To retain V_{G2} for a full frame time, the off current, I_{off} , must satisfy:

$$I_{\text{off}} \leq \frac{C_{\text{pix}} \Delta V_{G2}}{ST_f} \quad (21)$$

where ΔV_{G2} is the change in V_{G2} when the pixel brightness is changed by one gray-level increment, and S is a safety margin coefficient [43], which ensures sufficient engineering margin for proper display operation by accounting for the variation in performance between pixels. Since the pixel brightness is $L \propto (V_{G2} - V_T)^2$, the number of gray levels is

$$N_g = \frac{L_{\text{max}}}{\Delta L} = \frac{V_{G2\text{max}} - V_T}{2\Delta V_{G2}} \quad (22)$$

where L_{max} is the display full brightness, and ΔL is the brightness step for one gray scale. From (20)–(22), we obtain

$$\frac{I_{\text{on}}}{I_{\text{off}}} \geq 2SMN_g \cdot \frac{V_{G2\text{max}}}{V_{G2\text{max}} - V_T} \approx 2SMN_g. \quad (23)$$

If $M = 1024$, $N_g = 256$, and $S = 3$, then $I_{\text{on}}/I_{\text{off}} \leq 8 \times 10^5$. At room temperature, $I_{\text{on}}/I_{\text{off}} \sim 10^7$ for *a*-Si TFT's, and $I_{\text{on}}/I_{\text{off}} \sim 10^6$ for poly-Si TFT's, as listed in Table II. Therefore, both types of TFT's satisfy the on-off ratio requirement. Even higher on-off ratio ($\sim 10^8$) has recently been demonstrated using an organic TFT based on pentacene [37].

The field-effect mobility of the accessing transistor required by AM addressing of OLED displays is estimated as follows. Since T_1 operates in the linear regime, then

$$\frac{\partial I_{D1}}{\partial V_{DS1}} = \mu_{\text{FET}} \frac{w_1}{l_1} C_{\text{OX}}(V_{GS1} - V_T). \quad (24)$$

In order to charge C_S within the addressing time window, we require that

$$5 \left(\frac{\partial I_{D1}}{\partial V_{DS1}} \right)^{-1} C_{\text{pix}} \leq \frac{T_f}{M}. \quad (25)$$

From (24) and (25), we obtain

$$\mu_{\text{FET}} \frac{w_1}{l_1} \leq \frac{5MC_{\text{pix}}}{T_f C_{\text{OX}}(V_{GS1} - V_T)}. \quad (26)$$

If $C_{\text{pix}} = 1$ pF, $T_f = 16$ ms, $C_{\text{OX}} = 2 \times 10^{-8}$ F/cm², and $V_{GS1} - V_T = 5$ V, then $\mu_{\text{FET}}(w_1/l_1) \geq 3$ cm²/Vs is required for $M = 1000$. This requirement is readily fulfilled by *a*-Si TFT's with moderate w/l ratios, and all poly-Si TFT's. The recently demonstrated high-performance organic TFT [37] can also fulfill this requirement with a w/l ratio of only 3.

In an AM OLED array, the bottom contacts connected to the TFT's are patterned, while the top contact forms a continuous sheet shared by all pixels in the array. Unlike LCD pixels, the OLED's draw current, leading to a voltage drop on the nonpatterned, top contact. For an array of dimension W (width) $\times H$ (height), with a current density J through each pixel, and assuming the array edges are at the same potential, the voltage drop from the edges to the center of the display is

$$|V_0| = JR_{\text{sq}} W^2 \left[\frac{1}{8} - \frac{4}{\pi^3} \cdot \sum_{n=1}^{\infty} \frac{(-1)^{n+1}}{(2n-1)^3 \cosh(2n-1)(\pi H/W)} \right] \\ \equiv JR_{\text{sq}} W^2 \cdot G\left(\frac{H}{W}\right) \quad (27)$$

where R_{sq} is the sheet resistance of the top contact. Fig. 12 shows $|V_0|/(JR_{\text{sq}})$ versus W for $H/W = 3/4$ and $H/W = 9/16$, which are standard aspect ratios for video displays. The function $G(H/W)$ is plotted in the inset. For an AM OLED array using p-channel FET's as switches and a metal cathode for the top contact, $|V_0|$ is negligibly small ($|V_0| = 57$ mV for $J = 3.6$ mA/cm², $R_{\text{sq}} = 0.03$ $\Omega/\square$, $W = 100$ cm, and $H/W = 3/4$). For arrays using n-channel FET's and OLED's with a continuous ITO sheet as the shared anode, however, $|V_0|$ is high for large arrays due to the high-sheet resistance of the ITO thin-film sputter deposited by low-power RT processes [6]. For example, if $J = 3.6$ mA/cm² and $R_{\text{sq}} = 300$ $\Omega/\square$ (for a 400-Å-thick ITO sputter deposited at a 5-W RF power and room temperature [6]), then $|V_0| = 90$ V for $W = 40$ cm and $H/W = 3/4$. $|V_0|$ can be decreased by depositing a thin (~ 100 -Å) metal (e.g., Al) cap on the ITO anode without appreciably lowering the anode transparency, or by depositing a metal grid on the ITO anode in the gaps between the pixels. A 3- $\Omega/\square$ top contact composed of a high-sheet resistance ITO thin-film capped with a 80-Å-thick Al layer, leads to a voltage drop of only 0.9 V for the same conditions as above. Here, Al is chosen because of its good adhesion to ITO.

The analysis of the voltage drop on the ground line of an addressed row [see Fig. 9(a)] is similar to that of the row-line voltage drop in PM OLED arrays. Assuming the line is grounded at both sides of the panel, the voltage drop on the ground line is $V_g = (1/4) J \cdot (\rho/t) \cdot (H/M/b) \cdot W^2$, where J is the current density through the OLED, ρ is the resistivity of the ground line, and t and b are its thickness and width, respectively. If $J = 3.6$ mA/cm², $\rho = 3$ $\mu\Omega\cdot\text{cm}$, $t = 2000$ Å, $(H/M)/b = 10$, then $V_g = 1.2$ V for $W = 100$ cm. Hence, the ground-line voltage drop is not a limiting factor for the active matrix display size. The same conclusion applies to the power line voltage drop in AM OLED displays using p-channel FET's as shown in Fig. 9(b).

The resistance of an addressed row line, the gate-to-drain capacitance of T_1 of all the pixels in the addressed row, and the crossover capacitance between the addressed row line and all the column lines give rise to row-line delay [45], which may also limit the AM OLED array size. The row-line delay becomes a limiting factor for *a*-Si TFT backplanes due to the commonly used inverted, staggered TFT structures [45]. A scaling analysis [45] on *a*-Si TFT-LCD's pointed out that 40-in HDTV's would be possible with 300-nm-thick Cu gates. When this analysis is applied to AM OLED displays, the size limit is even less tight, since in this case the row-line and column-line widths will not necessarily be decreased with increasing resolution to maintain a given display aperture ratio. Unlike light-subtracting, back lit LCD's, the efficiency of an OLED display is not affected by the aperture ratio. Furthermore, a very high-aperture ratio can be obtained with top-emitting OLED's, independent of how much area is occupied by the transistors and interconnection lines.

The above analysis shows the potential to build large-area high-information-content AM-addressed OLED displays using currently available TFT technology. Although the use of a transistor backplane increases the display cost, the deposition of OLED's for monochromatic AM OLED displays is straightforward since only the bottom contact needs to be patterned. Column and row drive circuits can be positioned at the edges of the panel to reduce cost and interconnection failure. In spite of the absence of load transistors, fully integrated drivers based on *a*-Si TFT's have been demonstrated [46].

IV. FULL-COLOR DISPLAYS

A. Approaches to Full Color

OLED's emitting in red (R), green (G), and blue (B) spectral regions with sufficiently high efficiency are readily obtainable [12], and a color gamut similar to that of a CRT can be produced with emission spectral bandwidths of 75–100 nm [3]. The CIE (Commission Internationale de l'Eclairage) chromaticity coordinates, along with the quantum and luminous efficiencies are listed in Table I for recently reported, typical R, G, and B OLED's. An acceptable technology for producing full-color OLED displays, however, to our knowledge has not yet been reported in the literature. Fig. 13 shows five potential strategies [12] for making such full-color displays: 1) side-by-side patterning of R, G, and B OLED's; 2) absorptive filtering of white OLED's; 3) microcavity filtered OLED's; 4) fluorescent down-conversion of blue-emitting OLED's; and 5) color-tunable OLED's. These strategies were compared in previous work [12], which focused on the architecture of the full-color OLED itself. In this section, these strategies are quantitatively compared along with their drive schemes. For comparison, we define the relative efficiency, η_r , of a strategy as the ratio of the optical power of an element in a full-color pixel to that emitted by a discrete, monochromatic OLED. Hence, the power penalty for a particular strategy is $\Delta P = 1/\eta_r$, and the excess optical loss due to the full-color mechanism is $L = 1 - \eta_r$.

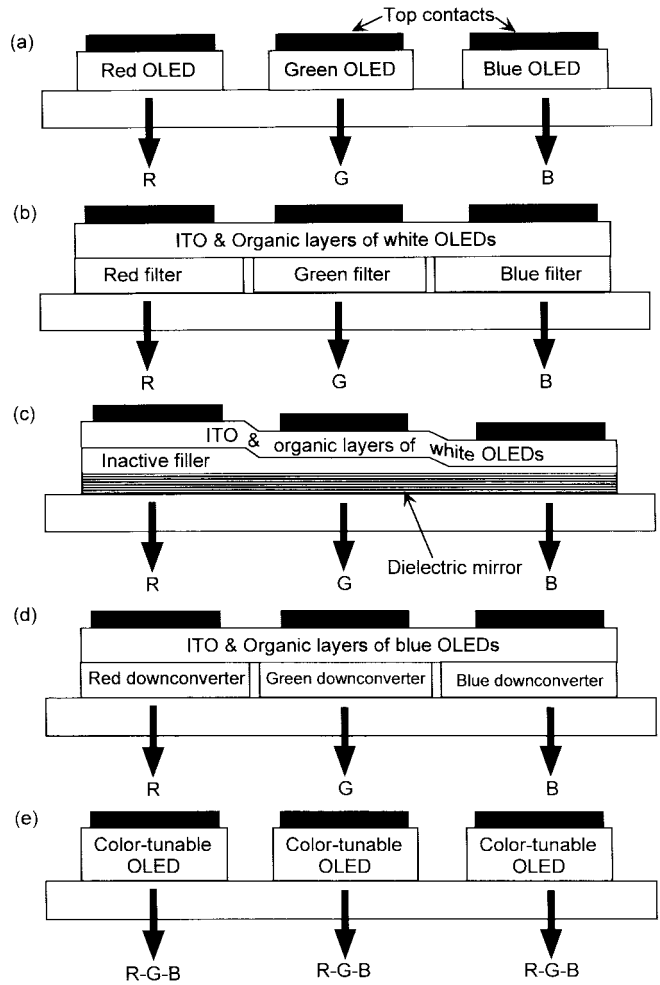


Fig. 13. Schematic diagram of the five strategies for achieving full-color displays based on OLED's. (a) Side-by-side patterning of R, G, and B OLED's. (b) Filtering of white light-emitting OLED's by color passband filters. (c) Microcavity filtering of broad-band OLED's. (d) Downconversion of blue light to generate green and red light. (e) Color tunable OLED's.

As shown in Fig. 13(a), strategy (1) uses side-by-side R, G, and B OLED's to make a compound, full-color pixel. This strategy is conceptually simple and involves no extra power penalty. The difficulty is the need for separate growth and patterning of red-, green-, and blue-emitting organic EL materials [12], [47].

In strategy (2), white OLED's can be made using materials with very broad emission spectra [48], or using two or more sequentially deposited, light-emitting layers [49]–[51]. This emission is then filtered using absorptive filter arrays such as those employed in color LCD technology. The OLED's may be grown on top of a prepatterned filter array¹² for bottom-emitting architectures as shown in Fig. 13(b); or may also be deposited on a separate glass plate and then aligned with the filter plate (which may serve as the lid for encapsulation as well) for top emission. The drawback of this strategy is the high loss of emitted power. There is a tradeoff between relative efficiency and color saturation if a broad emission spectrum OLED is used. Therefore, a white OLED with an emission spectrum composed of discrete R, G, and B bands is preferred. Assuming that discrete R, G, and B emission bands are covered

by ideal, 80% transmissive square pass band filters, and that the emitted energy is equally distributed among the R, G, and B emission peaks, the relative efficiency is $\eta_r = 27\%$, corresponding to a loss of $L = 73\%$.

In strategy (3) [see Fig. 13(c)], a white OLED is filtered by a microcavity, which is composed of a dielectric quarter wavelength stack as the bottom mirror, the metal contact as the top mirror, and an inactive material as a filler layer to adjust the cavity thickness [47]. Since the principal effect of the microcavity is to redistribute the optical energy, the overall efficiency of the color pixel is not necessarily decreased by the filtering. However, full-color displays based on microcavity filtered OLED's will be limited to those applications which do not require a large viewing angle due to the pronounced direction dependence of the resonance wavelength. The change in emission color for angles $>15^\circ$ can be quite severe [47]. By employing a modified cavity OLED, a $\pm 45^\circ$ viewing angle can be achieved [47].

A full-color pixel can also be implemented using a single blue OLED to pump wavelength down-converters, which efficiently absorb blue light and reemit the energy as green or red light [12], [25], [31], [53]. As for the filters in strategy (2), the down-converter array can either be predeposited on the substrate in the case of bottom emission as shown in Fig. 13(d), or deposited on a separate glass plate for a top-emitting OLED display. The former configuration requires planarization after the deposition of the down-converter array which must be sufficiently thick to absorb all the emitted light; the latter requires precise and potentially costly alignment of the two plates. In an example of this strategy [25], organic fluorescent materials are patterned to form the down-converter array. A down-converter size of $80 \times 250 \mu\text{m}^2$ has been achieved using a photolithographic process. The relative efficiencies of the green and red down-converters are $\eta_{rG} = \eta_G \lambda_B / \lambda_G$ and $\eta_{rR} = \eta_R \lambda_B / \lambda_R$, respectively, where η_G and η_R are their respective quantum efficiencies, λ_G and λ_R are the peak emission wavelengths of the green and red converters, and λ_B is the peak wavelength of the blue OLED. If $\lambda_B = 480 \text{ nm}$, $\lambda_G = 550 \text{ nm}$, $\lambda_R = 650 \text{ nm}$ and $\eta_G = \eta_R = 70\%$, then $\eta_{rG} = 61\%$ and $\eta_{rR} = 52\%$. The corresponding losses are $L_G = 39\%$ and $L_R = 48\%$ for the G and R subpixels, respectively. A potential problem of this strategy is "color bleeding," i.e., the unintentional pumping of down-converters by ambient light or waveguided radiation in the substrate [12].

In strategy (5), an array of continuously color-tunable OLED's removes the requirement that at least three subpixels be used to make a single, full-color pixel [12]. As shown in Fig. 13(e), this results in a threefold improvement in resolution and display fill-factor as compared to the other four strategies. Color-tunable OLED's have been demonstrated with both polymeric [54]–[57] and molecular [58]–[61] materials. Color variation is achieved by voltage and/or polarity tuning. The only molecular OLED capable of three color tuning [61] to our knowledge takes advantage of both voltage and polarity tunability. Brightness control can be obtained by varying the duty cycle of a pulsed drive current, while the amplitude and polarity are used to control the color. This complicates both the display drive circuit and the video data processing.

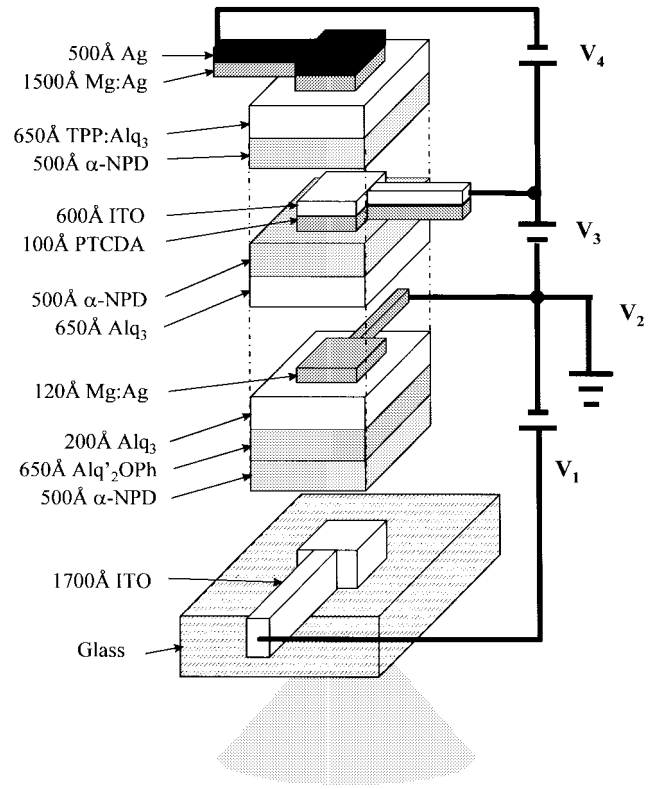


Fig. 14. Schematic cross section of a three-color SOLED (see [13]).

Furthermore, all these color-tunable emitters [58]–[61] have very low efficiency and/or require high-drive voltage. Hence, the color variable devices based on the polarity- and/or voltage-tuning are still far from practical display applications.

A novel pixel configuration, where independent red-, green-, and blue-emitting TOLED's are vertically stacked, allows for full, independent tunability of color and brightness [13]. A three-color stacked OLED (SOLED), as shown in Fig. 14, has been recently demonstrated to possess sufficiently high performance for display applications [13]. A transparent OLED is used as the middle element, sharing the thin, semitransparent metal cathode of the bottom element. In this device, an absorptive protection layer is deposited prior to the ITO anode, which is shared by the top element. The relative efficiency and addressing schemes of SOLED-based full-color displays will be discussed in detail in the following subsection.

B. Addressing Schemes

The addressing schemes (both AM and PM) for an N (columns) $\times$ M (rows) full-color display implemented with strategies (1)–(4) are identical to those used for a $3N \times M$ monochromatic display. The following discussion will therefore focus on the addressing of SOLED arrays, with comparison to the various strategies described in the preceding subsection.

A PM SOLED array can be constructed as shown in Fig. 15(a). Here, two addressing lines are used for each row: the common cathode of the bottom and middle devices r_1 , and the top cathode r_2 . Further, there are two drive lines for each column: the bottom anode c_1 , and the common anode of the

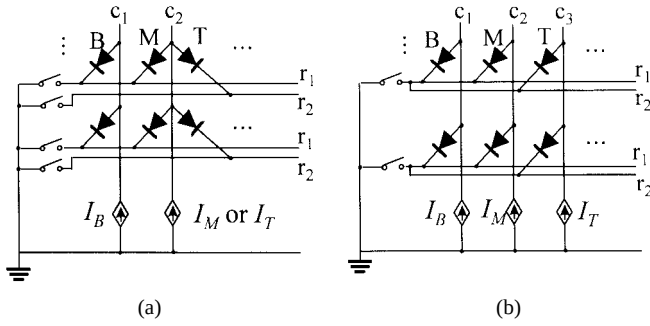


Fig. 15. The schematic illustration of PM SOLED arrays. B, M, and T indicate the bottom, middle, and top elements. (a) Implemented without and (b) with an inserted insulating layer.

middle and top devices c_2 . The addressing time of each row is divided between r_1 and r_2 . This array is equivalent to a PM array with $2M$ rows and $2N$ (for r_1) or N (for r_2) pixels in the intervening rows, resulting in a pixel duty factor of $1/(2M)$. To avoid decreasing the duty factor, an alternative PM addressing scheme employs an insulating layer inserted between the top and middle devices to electrically isolate these two elements in the stack. In practice, this necessitates two growths of ITO contacts separated by an insulator layer. The reflection from the many interfaces in a SOLED has been found to lead to microcavity effects [13], which affect the emission spectra of the stacked devices. The insertion of an optically transparent insulating layer provides one more degree of freedom to adjust the cavity length and hence to tune the emission into the appropriate sectors of the chromaticity chart. In this design, there are three column lines to provide full color for each column. These are anodes c_1, c_2 , and c_3 of the bottom, middle, and top devices, respectively. The two row lines r_1 and r_2 are connected to each other at the edge of the display. This scheme, as shown in Fig. 15(b), is equivalent to a $3N \times M$ pixel PM array. In both cases, the row-line and column-line voltage drops, power penalty and leakage current can be calculated using the methods described in Section III-A.

Active matrix addressing of a SOLED display can be implemented as shown in Fig. 16, where both n- and p-channel transistors are required. Transistors T_1 and T_4 control the currents through the bottom and middle devices (i.e., I_B and I_T), respectively. The current through the middle device I_M is controlled by T_2 and T_3 , giving currents $I_M + I_B$ and $I_M + I_B$, respectively. Since each OLED is connected to two drive transistors, the voltage drops on two transistors must be considered when V_{DD} is chosen. While this design avoids the need for the insertion of an insulating layer in the stack, it has several disadvantages: Eight transistors and four column signals are needed for each pixel, and the current through the middle device can not be independently controlled. Data processing is complicated in that the two column signals correspond to $I_B + I_M$ and $I_M + I_T$. Furthermore, every electrode must be patterned, which eliminates an important advantage of AM addressing.

To avoid these disadvantages, an insulating layer inserted between the top and middle devices is once again necessary. A design using only six p-channel transistors and three column signals is shown in Fig. 17. The analysis of an $N \times M$ AM

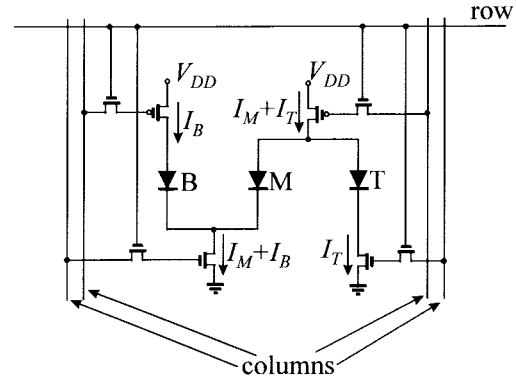


Fig. 16. A full-color AM OLED display pixel design based on the SOLED structure shown in Fig. 14.

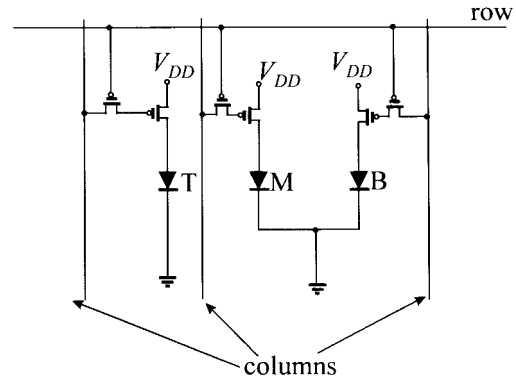


Fig. 17. A full-color AM OLED display pixel implemented using p-channel transistors and a SOLED with an insulating layer inserted between the top and middle elements.

SOLED display is similar to that of a $3N \times M$ monochromatic display described above. Since p-channel transistors are needed, α -Si TFT's can not be used in this scheme.

The above described addressing schemes are compatible with the SOLED structure shown in Fig. 14, which may have a transparent, insulating layer between the middle and bottom elements. Optical losses in this structure, caused by the absorption by the thin metal cathode and the protection layer [13], [40] are calculated using a simplified model employed in previous work [12]. We assume that each element in the stack emits equally toward the top cathode and the transparent substrate. The thin metal cathode and the protection layer have optical transmission coefficients T_C and T_P respectively. For simplicity, we ignore reflections from the thin metal cathode, assuming that light not transmitted through the thin cathode is absorbed. By summing the light emitted in both the upward and downward directions from each element in the stack, we obtain $\eta_{bt} = (1 + T_C^2 T_P^2)/2$, $\eta_{rM} = (1 + T_P^2)T_C/2$, and $\eta_{rT} = T_C T_P$. Fig. 18 shows these relative efficiencies, and the corresponding optical losses, L_B, L_M , and L_T , versus the thin metal cathode transmission for different values of T_P . For typical values of $T_P = 80\%$ [40] and $T_C = 70\%$ [6], the losses are: $L_B = 33\%$, $L_M = 43\%$, $L_T = 44\%$. To lower the optical loss, a highly transparent, hole transporting material is desired for the protection layer. If the protection layer is fully transparent, $L_B = 25\%$, $L_M = 30\%$, $L_T = 30\%$ for $T_C =$

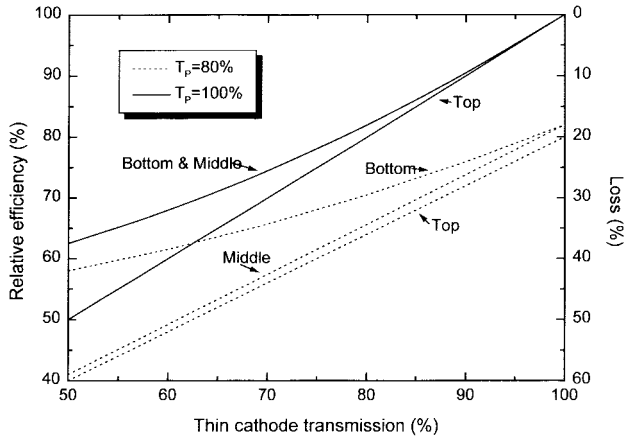


Fig. 18. The relative efficiency and optical loss versus thin metal optical transmission curves with the protection layer transparency, T_P , as a parameter for the SOLED structure in Fig. 14, or the modified structure with an inserted transparent insulating layer.

70%. For $T_C = 80\%$, this values are $L_B = 18\%$, $L_M = 20\%$, $L_T = 20\%$. In either case, the losses are considerably less than encountered in strategies (2)–(4). To increase the aperture ratio, the SOLED shown in Fig. 14 may be made top-emitting using a transparent top cathode. The relative efficiencies for this case can be found using the same model.

Active matrix addressing can also be implemented with n-channel TFT's using a modified (top-emitting) SOLED structure shown in Fig. 19(a), with the corresponding pixel drive circuit shown in Fig. 19(b). Here, the bottom element is an OLED, with its ITO anode shared by the middle element. The insulating layer is inserted between the thin cathodes of the middle and top elements. The top element is again an OLED, necessitating one more protection layer. As in the p-channel transistor scheme, independent control of each device is achieved, and the analysis of such an $N \times M$ array is again the same as that of a $3N \times M$ monochromatic display. The relative efficiencies for the bottom, middle, and top devices are $\eta_{rB} = T_C^2 T_P^2$, $\eta_{rM} = (1 + T_P^2) T_C^2 T_P / 2$, and $\eta_{rT} = (1 + T_P^2 T_C^4) T_P / 2$, respectively. For 70% transparent thin cathodes, $L_B = 69\%$, $L_M = 68\%$, $L_T = 54\%$ if $T_P = 80\%$; and $L_B = 51\%$, $L_M = 51\%$, $L_T = 38\%$ if $T_P = 100\%$. The optical losses of this device configuration are therefore higher than those of the inverse structure, since there are two protection layers and two thin metal cathodes in the stack. Nevertheless, the losses here are still lower than for strategy (2), and comparable with those in strategy (4) if an improved, highly transparent, hole transporting material is used for the protection layers. This modified device configuration, along with the n-channel transistor drive scheme, allows for the use of low-cost α -Si TFT's in the AM addressing of SOLED arrays.

C. Comparison

Among the five strategies to achieve full-color OLED displays, strategy (1), with no extra optical loss, is a good candidate if a high-definition low-cost patterning process for organic thin films is established. The high-optical loss ($>70\%$) makes strategy (2) less attractive than the other methods.

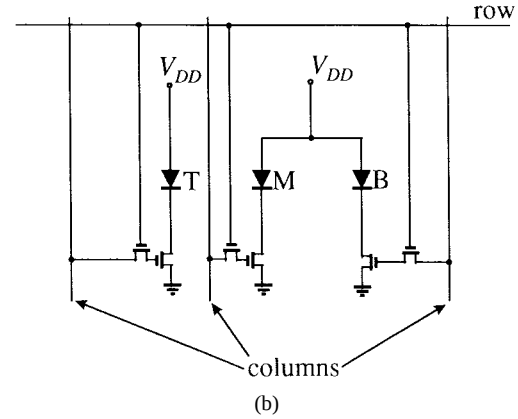
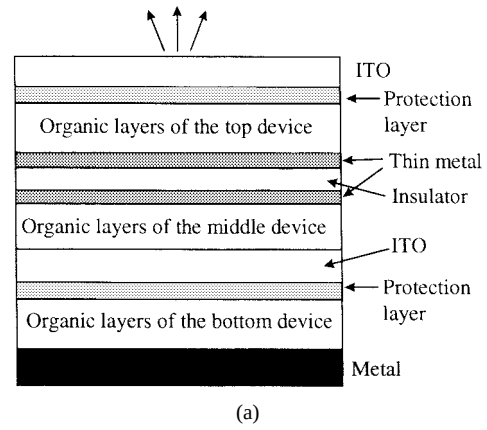


Fig. 19. An AM SOLED display pixel implemented using n-channel transistors with an insulating layer inserted between the top and middle SOLED elements. (a) Device structure. (b) Pixel drive circuit.

However, it may be used before other techniques become mature, since filter arrays widely used in LCD's can be readily transplanted for use in OLED displays. Strategy (3) is limited by the small viewing angle, although extra loss may be avoidable. Using high-quantum efficiency ($\sim 70\%$) photoluminescent materials which can be patterned at a high definition for the down-converters, strategy (4), with moderate losses (40%–50% for R and G subpixels), is also a good candidate. Strategy (5) has the unique advantage that leads to a threefold increase in resolution. A SOLED array, with its pixel structure as demonstrated in previous work, or modified to provide for independent contacting of all three elements in the stack, can be addressed with either the PM or AM scheme. With moderate optical loss (superior strategy (4) in some cases), the unique threefold improvement in resolution, and relative ease in patterning, this strategy represents an excellent approach to achieving very high-resolution full-color FPD's.

V. SUMMARY

In this paper, we systematically and quantitatively analyzed the performance of OLED-based FPD's. Displays based on currently available OLED technology can meet current ANSI standards for luminance and contrast in video displays. OLED displays are superior to LCD's in terms of viewing angle and brightness, and their luminous efficiency (including the power penalty resulting from addressing and full-color mechanisms)

is comparable with, or better than those of other FPD technologies. Both AM and PM addressing can be used to address an OLED display. The limits in both logical size (numbers of rows and columns) and physical size (display dimensions) are analyzed for PM OLED arrays. Due to these limits, AM addressing is needed for large size and high-information content (larger than 17-in diagonal with more than 500 rows and 64 gray levels). Currently available *a*-Si and poly-Si TFT performance satisfies the requirements of AM OLED displays. High-performance organic TFT's have been demonstrated, creating the potential for developing "all-organic," flexible active matrix displays. Strategies to achieve full color were compared. With no extra loss, side-by-side patterning of R, G, and B OLED's is a good candidate if a high-definition low-cost patterning process is established; down-conversion of blue OLED's, with the potential problem of "color bleeding," has moderate loss along with a moderate fabrication complexity. A novel approach toward full-color displays, the stacked OLED, or SOLED, has moderate loss and the potential to achieve the highest possible resolution. Vacuum-deposited OLED's have potential applications ranging from monochromatic alphanumeric displays to high-resolution full-color video displays if major difficulties such as relatively short operational lifetime are overcome. Furthermore, unique properties of organic thin films such as transparency, flexibility, and simplicity of film deposition, which are unobtainable using inorganic semiconductor materials, can potentially lead to novel display applications and configurations in the near future.

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- G. Gu**, photograph and biography not available at the time of publication.
- Stephen R. Forrest** (M'83–SM'88–F'91), for photograph and biography, see this issue, p. 2.