SD Specifications
Part 1
Physical Layer
Simplified Specification

Version 4.10

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SD Group

Panasonic Corporation
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Toshiba Corporation

Technical Committee
SD Card Association

CONFIDENTIAL

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SD Card Association
2400 Camino Ramon, Suite 375
San Ramon, CA 94583 USA
Telephone: +1 (925) 275-6615,
Fax: +1 (925) 886-4870
E-mail: office@sdcard.org

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Conventions Used in This Document

Naming Conventions

- Some terms are capitalized to distinguish their definition from their common English meaning. Words not capitalized have their common English meaning.

Numbers and Number Bases

- Hexadecimal numbers are written with a lower case "h" suffix, e.g., FFFFh and 80h.
- Binary numbers are written with a lower case "b" suffix (e.g., 10b).
- Binary numbers larger than four digits are written with a space dividing each group of four digits, as in 1000 0101 0010b.
- All other numbers are decimal.

Key Words

- May: Indicates flexibility of choice with no implied recommendation or requirement.
- Shall: Indicates a mandatory requirement. Designers shall implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification.
- Should: Indicates a strong recommendation but not a mandatory requirement. Designers should give strong consideration to such recommendations, but there is still a choice in implementation.

Application Notes

Some sections of this document provide guidance to the host implementers as follows:

> Application Note:
> This is an example of an application note.

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1. General Description

SD Memory Card is a memory card that is specifically designed to meet the security, capacity, performance, and environment requirements inherent in newly emerging audio and video consumer electronic devices. The SD Memory Card will include a content protection mechanism that complies with the security of the SDMI standard and will be faster and capable of higher Memory capacity. The SD Memory Card security system uses mutual authentication and a "new cipher algorithm" to protect against illegal usage of the card content. A Non-secure access to the user's own content is also available.

SD memory cards may also support a second security system based on commonly used standards, such as ISO-7816, which can be used to interface the SD memory card into public networks and other systems supporting mobile e-commerce and digital signature applications.

In addition to the SD Memory Card, there is the SD I/O (SDIO) Card. The SDIO Card specification is defined in a separate specification named: "SDIO Card Specification" that can be obtained from the SD Association. The SDIO Specification defines an SD card that may contain interfaces between various I/O units and an SD Host. The SDIO card may contain memory storage capability as well as its I/O functionality. The Memory portion of SDIO card shall be fully compatible to the given Physical Layer Specification. The SDIO card is based on and compatible with the SD Memory card. This compatibility includes mechanical, electrical, power, signalling, and software. The intent of the SD I/O card is to provide high-speed data I/O with low power consumption for mobile electronic devices. A primary goal is that an I/O card inserted into a non-SDIO aware host will cause no physical damage or disruption of that device or its software. In this case, the I/O card should simply be ignored. Once inserted into an SDIO aware host, the detection of the card will be via the normal means described in the given Physical Layer Specification with some extensions that are described in the SDIO Specification.

The SD Memory Card communication is based on an advanced 9-pin interface (Clock, Command, 4xData and 3xPower lines) designed to operate in at maximum operating frequency of 50 MHz and low voltage range. The communication protocol is defined as a part of this specification.

The SD Specifications are divided into several documents. The SD Specifications documentation structure is given in Figure 1-1.

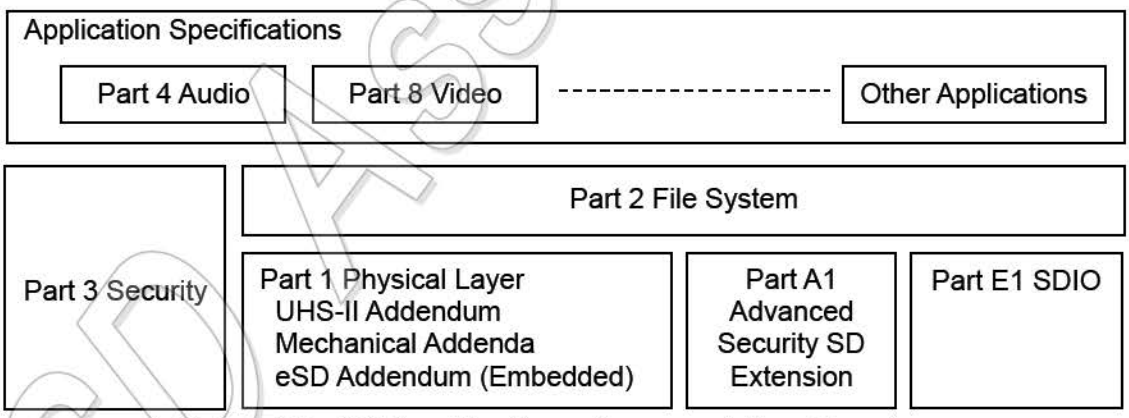


Figure 1-1: SD Specifications Documentation Structure

- **Audio Specification:**
  This specification, along with other application specifications, describes the specification of a specific application (in this case - Audio Application) and the requirements to implement it.

- **File System Specification:**
  The specification describes the specification of the file format structure of the data saved in the SD Memory Card (in User Area and Protected Area).

SD Association

- **Security Specification:**
  The specification describes the content protection mechanism and the application-specific commands that support it.

- **Physical Layer Specification (this document):**
  The specification describes the physical interface and the command protocol used by the SD Memory Card. The purpose of the Physical Layer specification is to define the SD Memory Card, its environment, and handling.
  The document is divided into several portions. Chapter 3 gives a general overview of the system concepts. The common SD Memory Card characteristics are described in Chapter 4. As this description defines an overall set of card properties, we recommend using the product documentation in parallel. The card registers are described in Chapter 5.
  Chapter 6 defines the electrical parameters of the SD Memory Card's hardware interface.

  Mechanical Specification described in Chapter 8 in Version 2.00 is moved to the Standard Size Mechanical Addendum.
  There are three mechanical addenda depend on form factors.
  (1) Standard Size Mechanical Addendum
  (2) miniSD Mechanical Addendum
  (3) microSD Mechanical Addendum

  UHS-II Interface Specification is defined by the UHS-II Addendum.
  Un-removable memory device for embedded application is defined by the eSD Addendum.

  As used in this document, "shall" or "will" denote a mandatory provision of the standard. "Should" denotes a provision that is recommended but is not mandatory. "May" denotes a feature, which may or may not be present–at the option of the implementer–and whose presence does not preclude compliance.

- **Mc-EX Interface Specification:** (This section was added in version 1.10)
  Part A1 of the SD memory card specification (Refer to Figure 1-1) serves as an extension to the SD card Physical Layer Specification and provides all of the definitions required to transfer the Mobile Commerce Extension (Mc-EX) command packets from the Mc-EX host to the Mc-EX enabled SD memory card, and vice versa.

- **SDIO Specification**
  SDIO card and embedded SDIO are specified based on the Physical Layer Specification and modifications and extensions are described in the Part E1 SDIO Specification.

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2. System Features

- Targeted for portable and stationary applications
- Capacity of Memory
  (1) Standard Capacity SD Memory Card (SDSC): Up to and including 2 GB
  (2) High Capacity SD Memory Card (SDHC): More than 2GB and up to and including 32GB
  (3) Extended Capacity SD Memory Card (SDXC): More than 32GB and up to and including 2TB
- Voltage range:
  High Voltage SD Memory Card – Operating voltage range: 2.7-3.6 V
  UHS-II SD Memory Card – Operating voltage range VDD1: 2.7-3.6 V, VDD2: 1.70-1.95V
- Designed for read-only and read/write cards.
- Bus Speed Mode (using 4 parallel data lines)
  (1) Default Speed mode: 3.3V signaling, Frequency up to 25 MHz, up to 12.5 MB/sec
  (2) High Speed mode: 3.3V signaling, Frequency up to 50 MHz, up to 25 MB/sec
  (3) SDR12: UHS-I 1.8V signaling, Frequency up to 25 MHz, up to 12.5MB/sec
  (4) SDR25: UHS-I 1.8V signaling, Frequency up to 50 MHz, up to 25MB/sec
  (5) SDR50: UHS-I 1.8V signaling, Frequency up to 100 MHz, up to 50MB/sec
  (6) SDR104: UHS-I 1.8V signaling, Frequency up to 208 MHz, up to 104MB/sec
  (7) DDR50: UHS-I 1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec
  (8) UHS156: UHS-II RCLK Frequency Range 26MHz - 52MHz, up to 1.56Gbps per lane.
- Switch function command supports Bus Speed Mode, Command System, Drive Strength, and future functions
- Correction of memory field errors
- Card removal during read operation will never harm the content
- Content Protection Mechanism - Complies with highest security of SDMI standard.
- Password Protection of cards (CMD42 - LOCK_UNLOCK)
- Write Protect feature using mechanical switch
- Built-in write protection features (permanent and temporary)
- Card Detection (Insertion/Removal)
- Application specific commands
- Comfortable erase mechanism

SD Association

- Protocol attributes of the communication channel:

SD Memory Card Communication Channel
Six-wire communication channel (clock, command, 4 data lines)
Error-protected data transfer
Single or Multiple block oriented data transfer

- SD Memory Card Form-factor
  There are three Part 1 mechanical addenda as follows:
  Standard Size SD Memory Card: Specified in "Part 1 Standard Size SD Card Addendum"
  miniSD Memory Card: Specified in "Part 1 miniSD Card Addendum"
  microSD Memory Card: Specified in "Part 1 microSD Card Addendum"

- Standard Size SD Memory Card thickness is defined as both 2.1 mm (normal) and 1.4 mm (Thin SD Memory Card).

SD Association

3. SD Memory Card System Concept

Description here is a blank in the Simplified Specification.

3.1 Read-Write Property

In terms of read-write property, two types of SD Memory Cards are defined:

- Read/Write (RW) cards (Flash, One Time Programmable - OTP, Multiple Time Programmable - MTP). These cards are typically sold as blank (empty) media and are used for mass data storage, end user video, audio or digital image recording
- Read Only Memory (ROM) cards. These cards are manufactured with fixed data content. They are typically used as a distribution media for software, audio, video etc.

3.2 Supply Voltage

In terms of operating supply voltage, two types of SD Memory Cards are defined:

- High Voltage SD Memory Cards that can operate the voltage range of 2.7-3.6 V.
- UHS-II SD Memory Card that can operate the voltage ranges VDD1: 2.7-3.6 V, VDD2: 1.70-1.95V

3.3 Card Capacity

3.3.1 User Area and Protected Area

SD Memory Card has two accessible independent areas: User Area and Protected Area. User Area is main memory area and Protected Area can be accessed by the authentication defined by the Part 3 Security Specification. Card Capacity means the sum of User Area Capacity and Protected Area Capacity.

3.3.2 Card Capacity Classification

In terms of card capacity, three types of SD Memory Cards are defined:

- Standard Capacity SD Memory Card (SDSC) supports capacity up to and including 2 G bytes (2^{31} bytes). All versions of the Physical Layer Specifications define the Standard Capacity SD Memory Card.
- High Capacity SD Memory Card (SDHC) supports capacity more than 2 G bytes (2^{31} bytes) up to 32 G bytes and is defined from the Physical Layer Specification Version 2.00.
- Extended Capacity SD Memory Card (SDXC) supports more than 32 G bytes (2^{35} bytes) up to 2TB.

Note:

1. The Part 1 Physical Layer Specification Version 3.00 or later and Part 2 File System Specification Version 3.00 or later allow Standard Capacity SD Memory Cards to have capacity up to and including 2 GB, High Capacity SD Memory Cards to have capacity up to and including 32 GB and Extended Capacity SD Memory Card to have capacity up to 2 TB.
2. Hosts that can access (read and/or write) SD Memory Cards with a capacity greater than 2 GB and up to and including 32 GB, shall also be able to access SD Memory Cards with a capacity of 2 GB or less.
3. Hosts that can access (read and/or write) SD Memory Cards with a capacity greater than 32 GB and up to 2 TB, shall also be able to access SD Memory Cards with a capacity of 32 GB or less.

3.4 Speed Class

Five Speed Classes are defined and indicate minimum performance of the cards

- Class 0 - These class cards do not specify performance. It includes all the legacy cards prior to the Physical Layer Specification Version 2.00, regardless of its performance

SD Association

- Class 2 is more than or equal to 2 MB/sec performance (Default Speed Mode)
- Class 4 is more than or equal to 4 MB/sec performance (Default Speed Mode)
- Class 6 is more than or equal to 6 MB/sec performance (Default Speed Mode)
- Class 10 is more than or equal to 10 MB/sec performance (High Speed Mode)

High and Extended Capacity SD Memory Cards shall support Speed Class Specification and have performance more than or equal to Class 2.

Note that the unit of performance [MB/sec] indicates 1000x1000 [Byte/sec] while the unit of data size [MB] indicates 1024x1024 [Byte]. This is because the maximum SD Bus speed is specified by the maximum SD clock frequency (25 [MB/sec] = 25000000 [Byte/sec] at 50 MHz) and data size is based on memory boundary (power of 2).

3.5 Bus Topology

This section is a blank in the Simplified Specification

SD Association

3.6 Bus Protocol

3.6.1 SD Bus Protocol

Communication over the SD bus is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit.

- **Command**: a command is a token that starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- **Response**: a response is a token that is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- **Data**: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

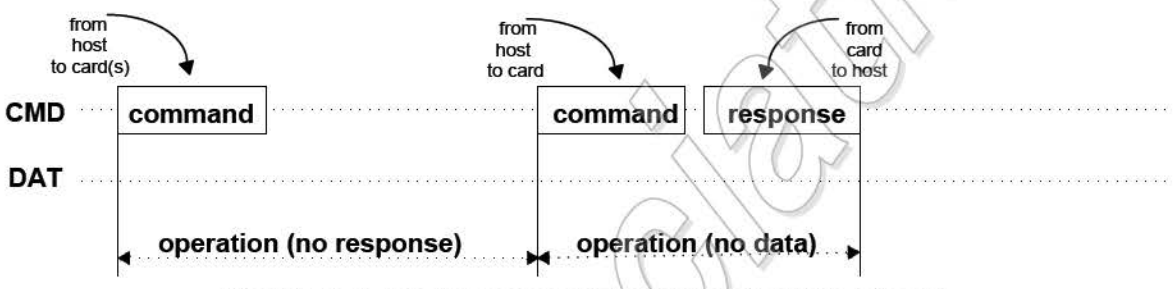


Figure 3-4: "no response" and "no data" Operations

Card addressing is implemented using a session address, assigned to the card during the initialization phase. The structure of commands, responses and data blocks is described in Chapter 4. The basic transaction on the SD bus is the command/response transaction (refer to Figure 3-4). This type of bus transaction transfers their information directly within the command or response structure. In addition, some operations have a data token.

Data transfers to/from the SD Memory Card are done in blocks. Data blocks are always succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines.

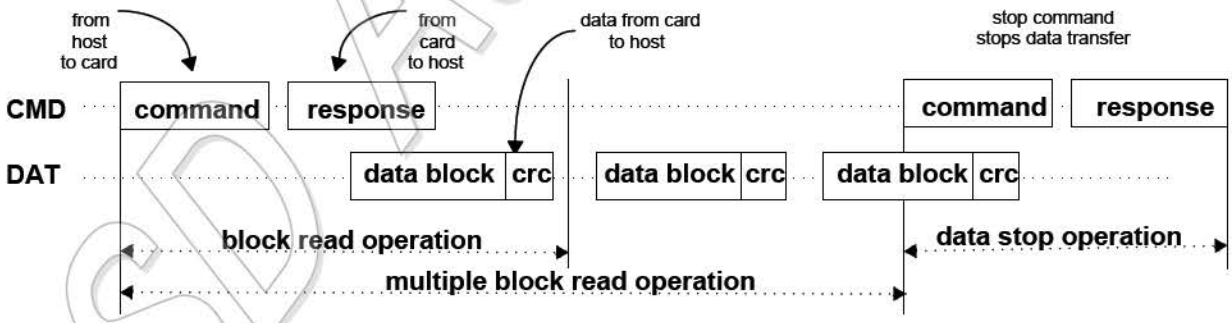


Figure 3-5: (Multiple) Block Read Operation

The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line (see Figure 3-6) regardless of the number of data lines used for transferring the data.

SD Association

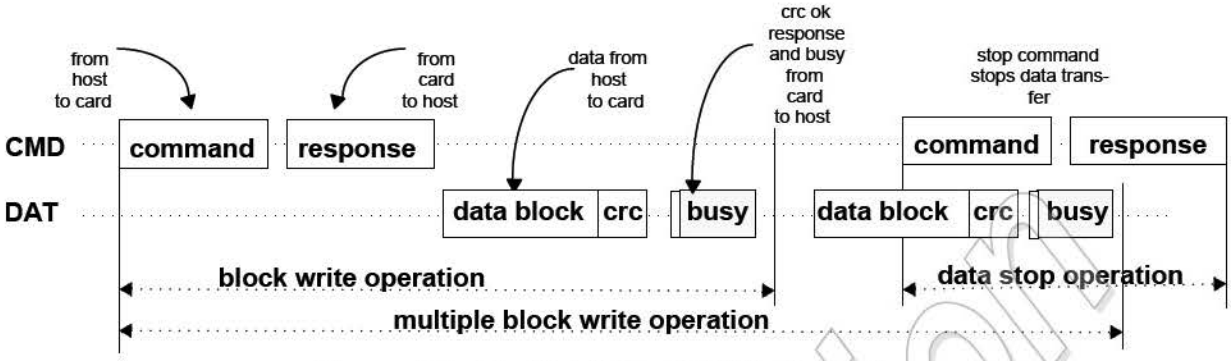


Figure 3-6: (Multiple) Block Write Operation

Command tokens have the following coding scheme:

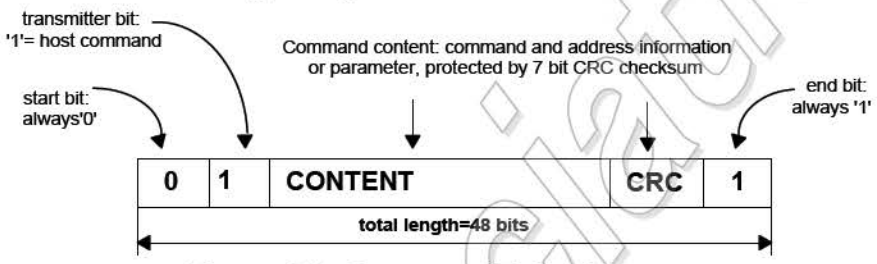


Figure 3-7: Command Token Format

Each command token is preceded by a start bit (0) and succeeded by an end bit (1). The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected and the operation may be repeated.

Response tokens have one of four coding schemes, depending on their content. The token length is either 48 or 136 bits. The detailed commands and response definition is given in Chapter 4.7. The CRC protection algorithm for block data is a 16-bit CCITT polynomial. All allowed CRC types are described in Chapter 4.5.

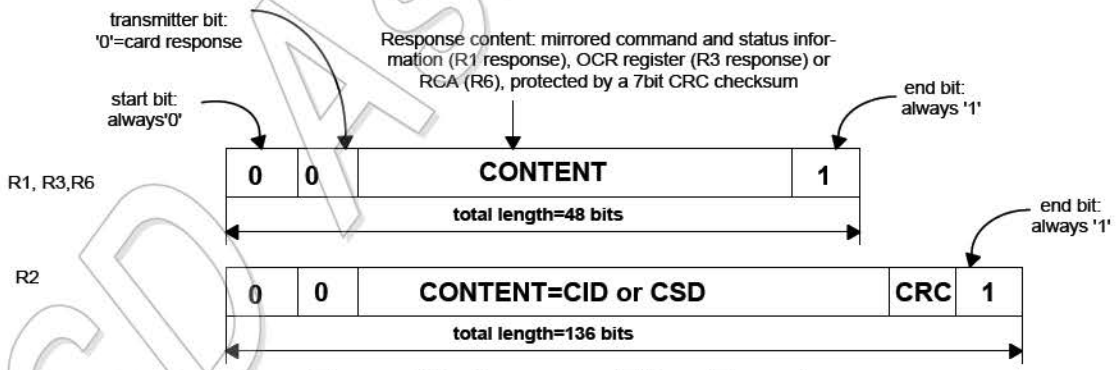


Figure 3-8: Response Token Format

In the CMD line the Most Significant Bit (MSB) is transmitted first, the Least Significant Bit (LSB) is the last.

When the wide bus option is used, the data is transferred 4 bits at a time (refer to Figure 3-10). Start and end bits, as well as the CRC bits, are transmitted for every one of the DAT lines. CRC bits are calculated and checked for every DAT line individually. The CRC status response and Busy indication will be sent by the card to the host on DAT0 only (DAT1-DAT3 during that period are don't care).

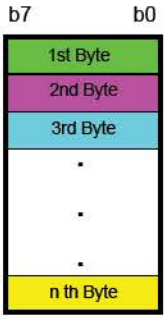
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There are two types of Data packet format for the SD card.

(1) Usual data (8-bit width): The usual data (8-bit width) are sent in LSB (Least Significant Byte) first, MSB (Most Significant Byte) last sequence. But in the individual byte, it is MSB (Most Significant Bit) first, LSB (Least Significant Bit) last.

(2) Wide width data (SD Memory Register): The wide width data is shifted from the MSB bit.

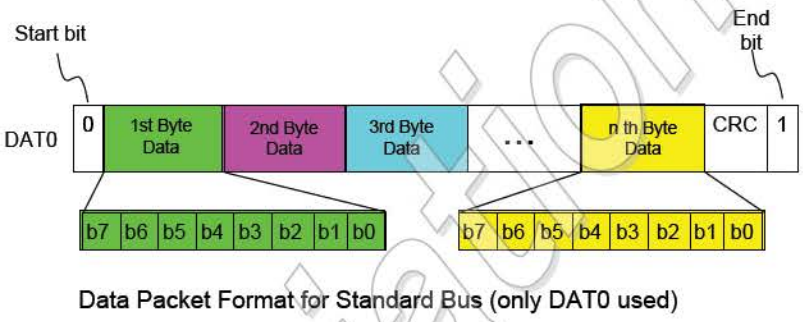
1. Data Packet Format for Usual Data (8-bit width)



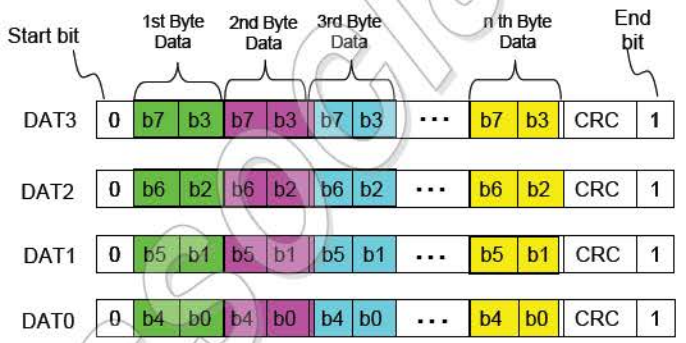
8bit width Data

Ex

[SDIO]
CMD53
[SD memory]
CMD17, CMD18,
CMD24, CMD25,
ACMD18, ACMD25,
etc



Data Packet Format for Standard Bus (only DAT0 used)



Data Packet Format for Wide Bus (all four lines used)

Figure 3-9: Data Packet Format - Usual Data

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2. Data Packet Format for Wide Width Data (Ex. ACMD13)

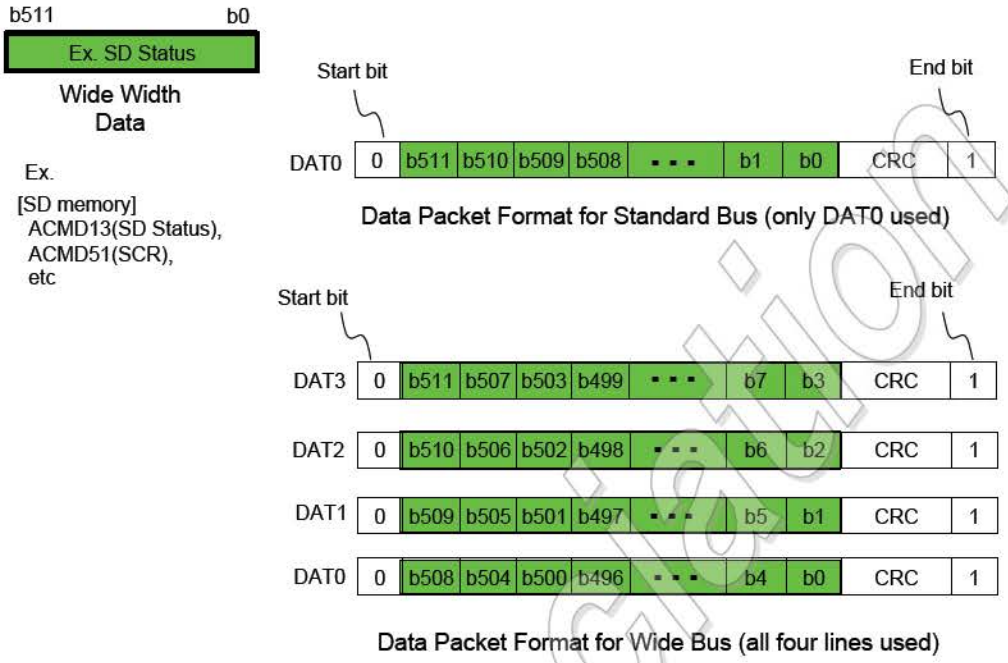


Figure 3-10: Data Packet Format - Wide Width Data

3.6.2 SPI Bus Protocol

Details of the SPI Bus protocol are described in Chapter 7.

3.6.3 UHS-II Bus Protocol

UHS-II Bus protocol is defined in the UHS-II Addendum.

SD Association

3.7 SD Memory Card–Pins and Registers

3.7.1 SD Bus Pin Assignment

The SD Memory Card has the form factor 24 mm x 32 mm x 2.1 mm or 24 mm x 32 mm x 1.4 mm.

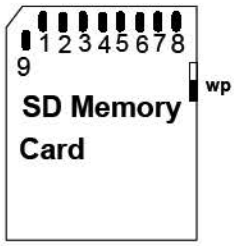


Figure 3-11: SD Memory Card Shape and Interface (Top View)

Figure 3-11 shows the general shape of Standard Size and interface contacts of the SD Memory Card. The detailed physical dimensions and mechanical description are given in Part 1 Mechanical Addenda. Table 3-1 defines the card contacts:

Pin #	SD Mode			SPI Mode		
	Name	**Type**[1]	**Description**	**Name**	**Type**[1]	**Description**
1	CD/DAT3[2]	I/O/PP[3]	Card Detect/ Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
2	CMD	I/O/PP	Command/Response	DI	I	Data In
3	VSS1	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1[4]	I/O/PP	Data Line [Bit 1]	RSV		
9	DAT2[5]	I/O/PP	Data Line [Bit 2]	RSV		

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command
4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

Table 3-1: SD Memory Card Pad Assignment

SD Association

Each card has a set of information registers (see also Chapter 5 in the Physical Layer Specification):

Name	Width	Description
CID	128	Card identification number; card individual number for identification (See 5.2). **Mandatory**.
RCA[1]	16	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization (See 5.4). **Mandatory**.
DSR	16	Driver Stage Register; to configure the card's output drivers (See 5.5). **Optional.**
CSD	128	Card Specific Data; information about the card operation conditions (See 5.3). **Mandatory**
SCR	64	SD Configuration Register; information about the SD Memory Card's Special Features capabilities (See 5.6). **Mandatory**
OCR	32	Operation conditions register (See 5.1). **Mandatory.**
SSR	512	SD Status; information about the card proprietary features (See 4.10.2). **Mandatory**
CSR	32	Card Status; information about the card status (See 4.10.1). **Mandatory**

(1) RCA register is not used (available) in SPI mode

Table 3-2: SD Memory Card Registers

The host may reset the cards by switching the power supply off and on again. Each card shall have its own power-on detection circuitry that puts the card into a defined state after the power-on. No explicit reset signal is necessary. The cards can also be reset by sending the GO_IDLE (CMD0) command.

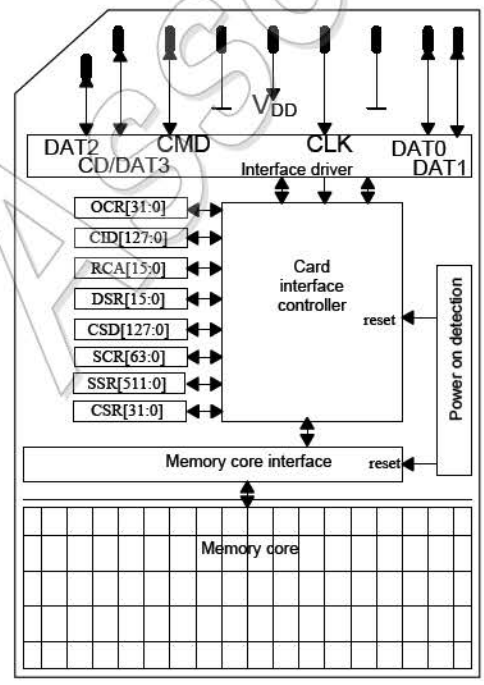


Figure 3-12: SD Memory Card Architecture

SD Association

3.7.2 UHS-II Pin Assignment

UHS-II Card shape is the same as SD Cards and UHS-II Interface is assigned to pads on the second row.

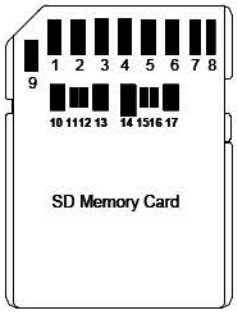


Figure 3-13 : UHS-II Card Shape and Interface (Top View)

Figure 3-13 shows the shape of Standard Size and interface contacts of the UHS-II SD Memory Card. The detailed physical dimensions and mechanical description are given in Part 1 Mechanical Addenda. Table 3-3 defines the contacts for UHS-II. SD bus contacts 7 and 8 Pins are used for RCLK. The first row contacts in non UHS-II mode are equivalent to Table 3-1. Regarding PHY I/O Type, refer to the UHS-II Addendum for more details.

Pin #	Name	Type	Description
4	VDD1	Supply voltage	2.7V to 3.6V
7	RCLK+	Differential Signaling: Input	Clock Input
8	RCLK-	Differential Signaling: Input	Clock Input
10	VSS3	Ground	
11	D0+	Differential Signaling: Input (FD) / Bidirectional (HD)	Input in default
12	D0-	Differential Signaling: Input (FD) / Bidirectional (HD)	Input in default
13	VSS4	Ground	
14	VDD2	Supply Voltage 2	1.70V to 1.95V
15	D1-	Differential Signaling: Output (FD) / Bidirectional (HD)	Output in default
16	D1+	Differential Signaling: Output (FD) / Bidirectional (HD)	Output in default
17	VSS5	Ground	

Table 3-3 : UHS-II Interface Pad Assignment

UHS-II Card shall not drive unused lines of SD I/F in UHS-II mode. (CLK, CMD and DAT[3:2]. DAT[2] may be used as interrupt line in case of UHS-II SDIO Card. In this case, card controls DAT[2] level.)
Host shall not leave these unused lines floating, but keep them at a defined high or low level. How to keep line level is dependent on host implementation. For example, use pull-up resistor or host drives the lines to low level without providing pull-up voltage. As DAT[1:0] are used for providing RCLK, individual line control is required to use pull-up method for CMD and DAT[3:2]. CLK (without pull-up resistor) should be driven to low.
In case of entering hibernate mode, unused lines shall be set to low before turning off VDD1.

SD Association

3.8 ROM Card

ROM Card is defined as read only memory which meets following requirements. A permanent or temporary write protected writable SD memory card does not belong to this category.

3.8.1 Register Setting Requirements

Table 3-4 shows register setting requirements for ROM Card.

Register	Field	Value	Comment
SD Status	SD_CARD_TYPE	0001h	SD ROM Card
CSD	CCC bit 4	0	Class4 block write
	CCC bit 5	0	Class5 erase
	CCC bit 6	0	Class6 write protection
	CCC bit 7	0 or 1	Class7 lock card
	PERM_WRITE_PROT	1	Permanent Write Protect
SCR	SD_SECURITY	0 or 2 or 3	Security is optional.

Table 3-4 : Register Setting Requirements for ROM Card

3.8.2 Unsupported Commands

The ROM Card shall treat following commands as unsupported and illegal command.

CMD24, CMD25, CMD27, CMD28, CMD29, CMD30, CMD32, CMD33, CMD38

3.8.3 Optional Commands

The ROM Card can support following commands as optional command.

CMD42, security commands

- If CMD42 is not supported, bit 7 of CCC shall be set to 0. CMD42 is treated as illegal command.
- When ROM card supports CMD42, "Unlocking the card" and "Locking the card" functions shall be supported by presetting the password. LOCK_UNLOCK_FAILED is indicated when receiving the other unsupported functions of CMD42.
- If security is not supported, SD_SECURITY shall be set to 0. The security commands are treated as illegal command.
- ROM card does not support write and erase to the protected area. Refer to the Part 3 Security Specification about security command support of ROM card.

3.8.4 WP Switch

A full-size ROM card does not have WP Switch.

SD Association

3.9 Ultra High Speed Phase I (UHS-I) Card

UHS-I provides up to 104MB/sec performance on 4-bit SD bus with the single end driver interface. Card form factor is the same and existing connector can be used.

3.9.1 UHS-I Card Operation Modes

- DS - Default Speed up to 25MHz 3.3V signaling
- HS - High Speed up to 50MHz 3.3V signaling
- SDR12 - SDR up to 25MHz 1.8V signaling
- SDR25 - SDR up to 50MHz 1.8V signaling
- SDR50 - SDR up to 100MHz 1.8V signaling
- SDR104 - SDR up to 208MHz 1.8V signaling
- DDR50 - DDR up to 50MHz 1.8V signaling

Note: 1.8V signal timings are different from those of 3.3V.

3.9.2 UHS-I Card Types

UHS-I supports two card Types:

- UHS50
- UHS104

UHS-I is not applied to SDSC card but can be applied to SDHC and SDXC card.

Figure 3-14 and Figure 3-15 show UHS-I supported modes.
DDR50 is mandatory for microSD form factor and optional for Standard size SD form factor

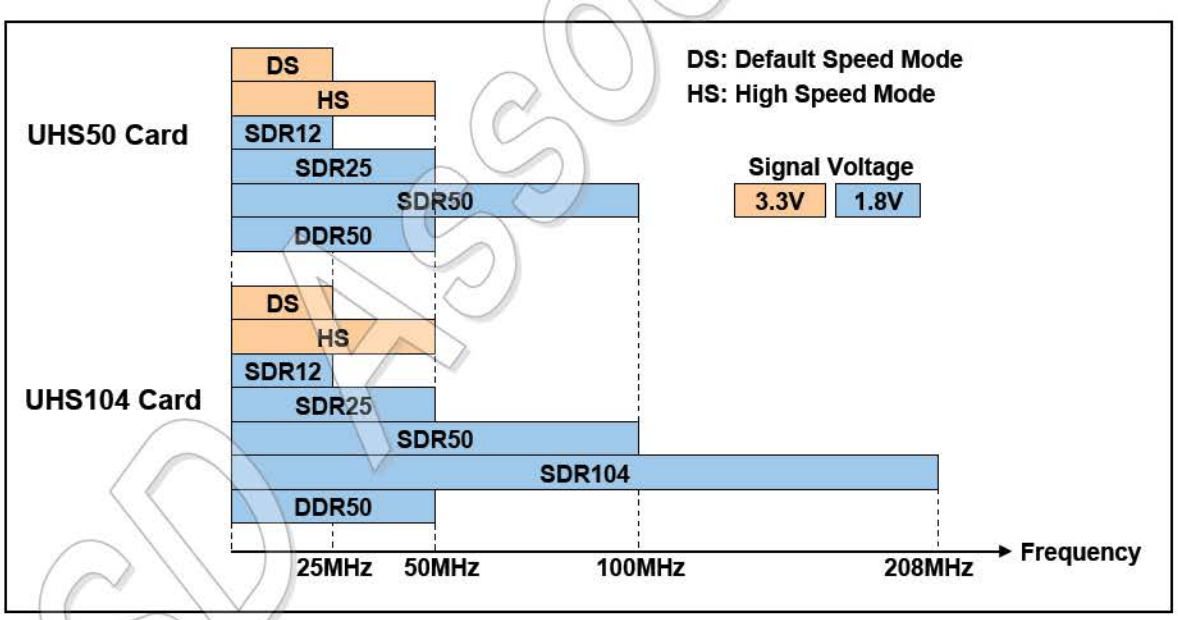


Figure 3-14 : UHS-I Card Type Modes of Operation versus Frequency Range

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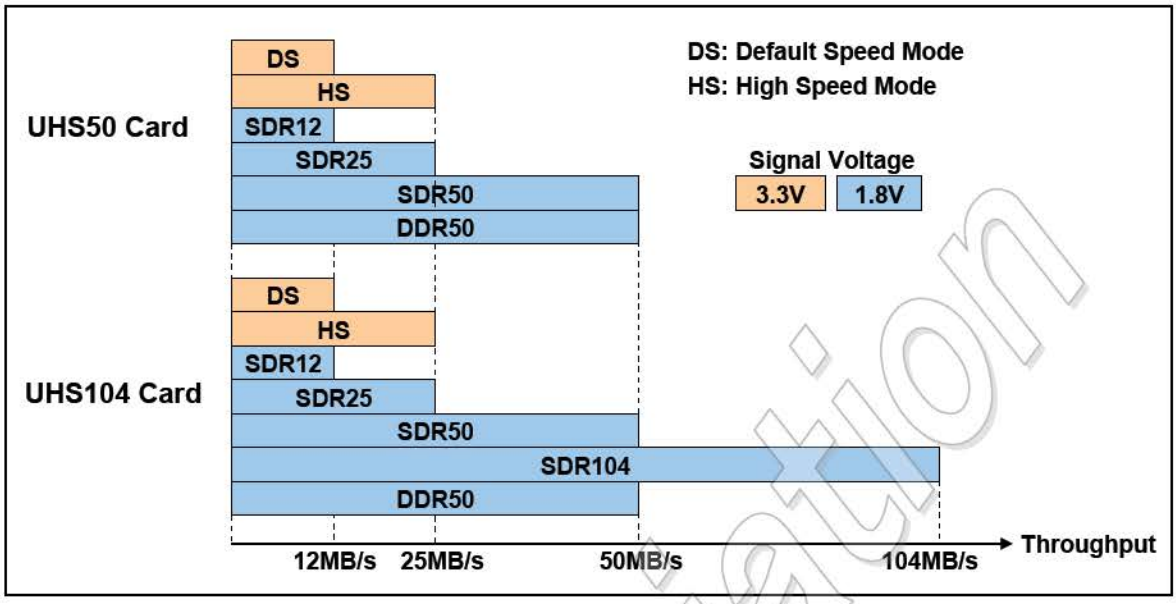


Figure 3-15 : UHS-I Card Type Modes of Operation versus Throughput

3.9.3 UHS-I Host and Card Combination

Host may use SDR50, DDR50 and SDR104 modes with either UHS50 Card or UHS104 Card.
Table 3-5 shows usable UHS performance depends on the combination of host and card. UHS-I for removable card is presumed that one card is connected to a SD bus. Maximum performance of up to 104MB/s is possible only if host supports SDR104 mode and card is UHS104 Card (supports SDR104 mode). If card is a UHS50 Card or if host doesn't support SDR104 mode, performance is limited to 50MB/s (SDR104 mode cannot be used).
Host may use DDR50 mode with UHS50 Card and UHS104 Card in microSD form factors.

Host types:

SDR-FD – SDR signaling, fixed-delay (can't use tuning)
SDR-VD – SDR signaling, variable-delay (can use tuning)
DDR – DDR signaling

Host type / Card type	HOST-SDR-FD (SDR, fixed-delay)	HOST-SDR-VD (SDR, variable-delay)	HOST-DDR (DDR)
UHS50 card microSD	SDR50 ≤ 100MHz	SDR50 ≤ 100MHz + tuning	DDR50 ≤ 50MHz
UHS104 card microSD	SDR50 ≤ 100MHz	SDR104 ≤ 208MHz + tuning	DDR50 ≤ 50MHz
UHS50 card Full-size SD	SDR50 ≤ 100MHz	SDR50 ≤ 100MHz + tuning	Optional
UHS104 card Full-size SD	SDR50 ≤ 100MHz	SDR104 ≤ 208MHz + tuning	Optional

Table 3-5 : UHS-I Host and Card Combinations

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3.9.4 UHS-I Bus Speed Modes Selection Sequence

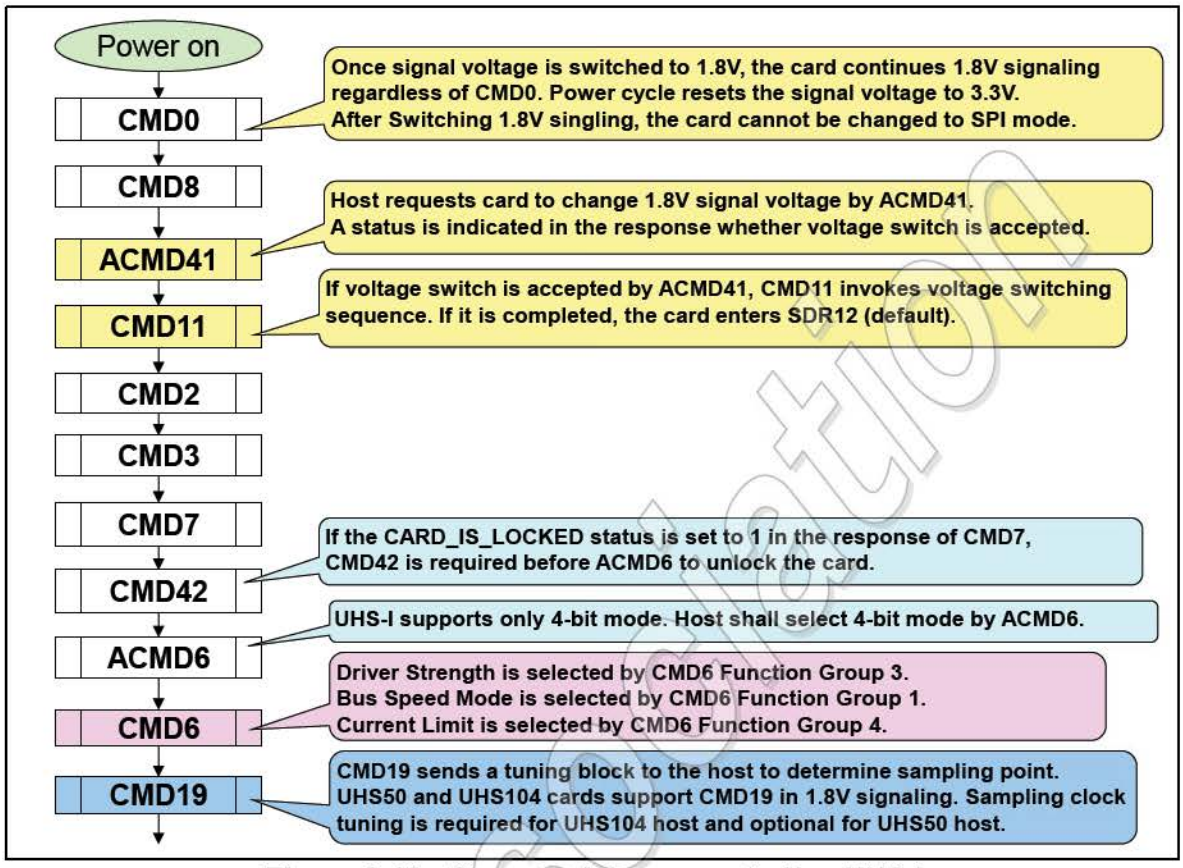


Figure 3-16 : Command Sequence to Use UHS-I

Figure 3-16 shows command sequence to use a UHS-I. After power cycle, card is in 3.3V signaling mode. The first CMD0 selects the bus mode; SD mode or SPI mode. 1.8V signaling mode can be entered only in SD mode. Once the card enters 1.8V signaling mode, the card cannot be switched to SPI mode or 3.3V signaling without power cycle. If the card receives CMD0, card returns to Idle state but still work with SDR12 timing. UHS-I is provided in SD mode but not in SPI mode.

As higher bus speed requires low level signaling, UHS-I adopts 1.8V signaling level for SDR50, DDR50 and SDR104 modes. Still card is supplied with 3.3V by the host and 1.8V signaling level for SDCLK, CMD and DAT[3:0] lines is converted from 3.3V power line. To avoid voltage mismatch between host and card, signaling level is changed by voltage switch sequence at the initialization. The host and card communicate using ACMD41 whether host and card support 1.8V signaling mode. Support of 1.8V signaling both host and card means UHS-I can be used. CMD11 invokes the voltage switch sequence. The card enters UHS-I mode and card input and output timings are changed (SDR12 in default) when the voltage switch sequence is completed successfully. (Refer to Section 4.2.4 for more detail.)

Only 4-bit bus mode is supported in UHS-I except CMD42. If the card is locked, host needs to unlock the card by CMD42 in 1-bit mode and then needs to issue ACMD6 to change 4-bit bus mode. Operating in 1-bit mode is not assured.

Host can choose suitable output driver strength by CMD6 Function Group 3.

Host can choose one of UHS-I modes by CMD6 Function Group 1. Each UHS-I mode is specified by the maximum frequency, sampling edges (rising-only or both) and maximum Power consumption for compatibility with existing cards. Host can choose one of UHS-I mode depending on capability of generating SDCLK frequency and capacity of power supply host supported.

CMD19 can be executed in transfer state of 1.8V signaling mode while the card is unlocked. The other case, CMD19 is treated as illegal command.

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3.9.5 UHS-I System Block Diagram

This section is a blank in the Simplified Specification.

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3.9.6 Summary of Bus Speed Mode for UHS-I Card

Table 3-6 shows the card requirements regarding Bus Speed modes selected by CMD6 function group 1. The maximum frequency and the maximum power are determined by CMD6.

Bus Speed Mode[*1]	Max. Bus Speed [MB/s]	Max. Clock Frequency [MHz]	Signal Voltage [V]	Max. Power[*2] [W]		
				SDSC[*3]	SDHC[*4]	SDXC[*5]
SDR104	104	208	1.8	-	2.88[*6]	2.88[*6]
SDR50	50	100	1.8	-	1.44	1.44
DDR50	50	50	1.8	-	1.44	1.44
SDR25	25	50	1.8	-	0.72	0.72
SDR12	12.5	25	1.8	-	0.36	0.36/0.54[*7]
High Speed	25	50	3.3	0.72	0.72	0.72
Default Speed	12.5	25	3.3	0.36	0.36	0.36/0.54[*7]

*1: The card supports a UHS-I mode shall support all lower UHS-I modes.
*2: Host may control power by the Power Limit function in CMD6 (Refer to Section 4.3.10.3).
*3: SDSC stands for SD Standard Capacity Memory Card and
*4: SDHC stands for SD High Capacity Memory Card.
*5: SDXC stands for SD Extended Capacity Memory Card.
*6: The actual maximum current may vary from the limit described in this table. It is limited by the Mechanical Addenda in the sections that define the thermal profile of the device and the connector profile.
*7: Host may select either maximum power by XPC in ACMD41 (Refer to Section 4.2.3.1). In SPI mode, XPC is not supported and the power shall be up to 0.36W (100mA at 3.6V on VDD1).

Table 3-6 : Bus Speed Modes of UHS-I Card

DS - Default Speed up to 25MHz 3.3V signaling
HS - High Speed up to 50MHz 3.3V signaling
SDR12 - SDR up to 25MHz 1.8V signaling
SDR25 - SDR up to 50MHz 1.8V signaling
SDR50 - SDR up to 100MHz 1.8V signaling
SDR104 - SDR up to 208MHz 1.8V signaling
DDR50 - DDR up to 50MHz 1.8V signaling

Table 3-7 clarifies option / mandatory of bus speed mode for each card capacity type.

Card Classification		DS	HS	SDR50	SDR104	DDR50
SDSC		M	O	N/A	N/A	N/A
SDHC	Non UHS-I	M	O	N/A	N/A	N/A
	UHS50	M	M	M	N/A	O (Standard SD) M (microSD)
	UHS104	M	M	M	M	O (Standard SD) M (microSD)
SDXC	Non UHS-I	M	O	N/A	N/A	N/A
	UHS50	M	M	M	N/A	O (Standard SD) M (microSD)
	UHS104	M	M	M	M	O (Standard SD) M (microSD)

M: Mandatory, O: Optional, N/A: Not Available

Table 3-7 : Bus Speed Mode Option / Mandatory

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3.10 Ultra High Speed Phase II (UHS-II) Card

3.10.1 UHS-II Card Operation Modes

SD Bus Interface Modes

- DS - Default Speed up to 25MHz 3.3V signaling
- HS - High Speed up to 50MHz 3.3V signaling
- SDR12 - SDR up to 25MHz 1.8V signaling
- SDR25 - SDR up to 50MHz 1.8V signaling
- SDR50 - SDR up to 100MHz 1.8V signaling
- SDR104 - SDR up to 208MHz 1.8V signaling (Optional)
- DDR50 - DDR up to 50MHz 1.8V signaling (Optional for Standard Size Card)

UHS-II Interface Modes

- FD156 - Full Duplex mode up to 156MB/s at 52MHz in Range B
- HD312 - Half Duplex with 2 Lanes mode up to 312MB/s at 52MHz in Range B (Optional)

3.10.2 UHS-II Card Type

UHS-II supports one card Type

The performance of UHS-II card is indicated based on in Full Duplex mode because HD312 is optional.

- UHS156: UHS-II Card with data rate up to 1.56Gbps in FD156 mode and up to 312Gbps in HD312 mode (Optional).

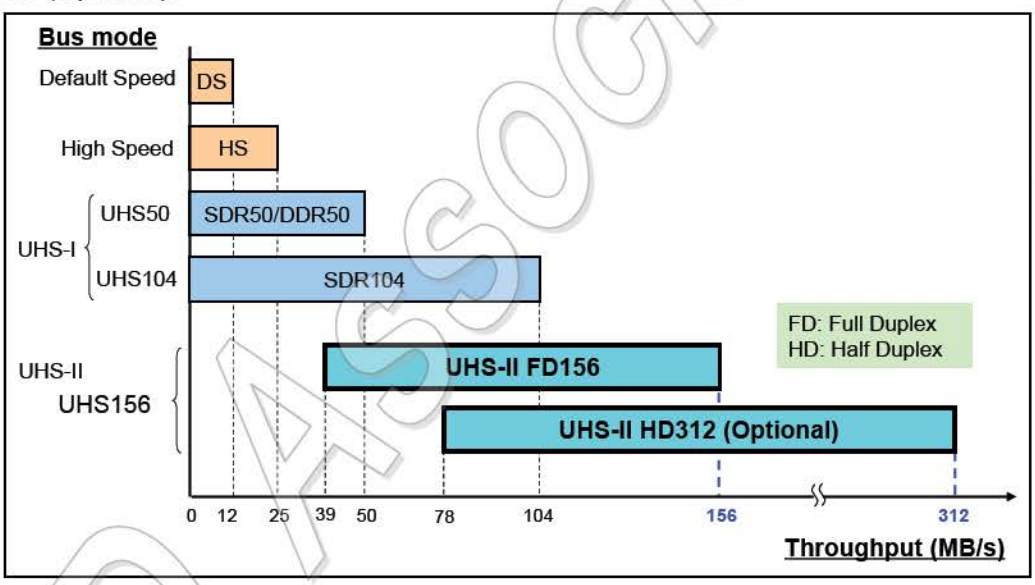


Figure 3-18 : Throughput of UHS156 UHS-II Card

3.10.3 UHS-II Host and Card Combination

Host type / Card type	UHS-II FD156 only	UHS-II HD312 supported
UHS156 (HD312 not supported)	up to 1.56Gbps	up to 1.56Gbps
UHS156 (HD312 supported)	up to 1.56Gbps	up to 3.12Gbps

Note: HD312 cannot be used in Ring Topology

Table 3-8 : UHS-II Host and Card Combinations

SD Association

3.10.4 UHS-II Interface Selection Sequence

UHS-II supported host shall support Legacy SD Bus Interface (I/F) and UHS-II I/F. Removable UHS-II card slot shall be connected to both I/Fs. Then UHS-II card may be initialized not only in UHS-II mode but also in SD Bus I/F mode.

Figure 3-19 shows how to select UHS-II mode. After power up, SD bus I/F and UHS-II I/F of UHS-II card are enabled. UHS-II supported host provides RCLK and STB.L to D0 lane. Host waits D1 lane to change EIDL to STB.L. If STB.L is detected on D1 lane, host starts UHS-II initialization. If D1 lane is not changed to STB.L by 200us timeout, host should initialize the card in SD Bus I/F mode. As 200us for STB.L detection is defined as per card, host needs to determine total timeout value that depends on UHS-II bus topology of a system.

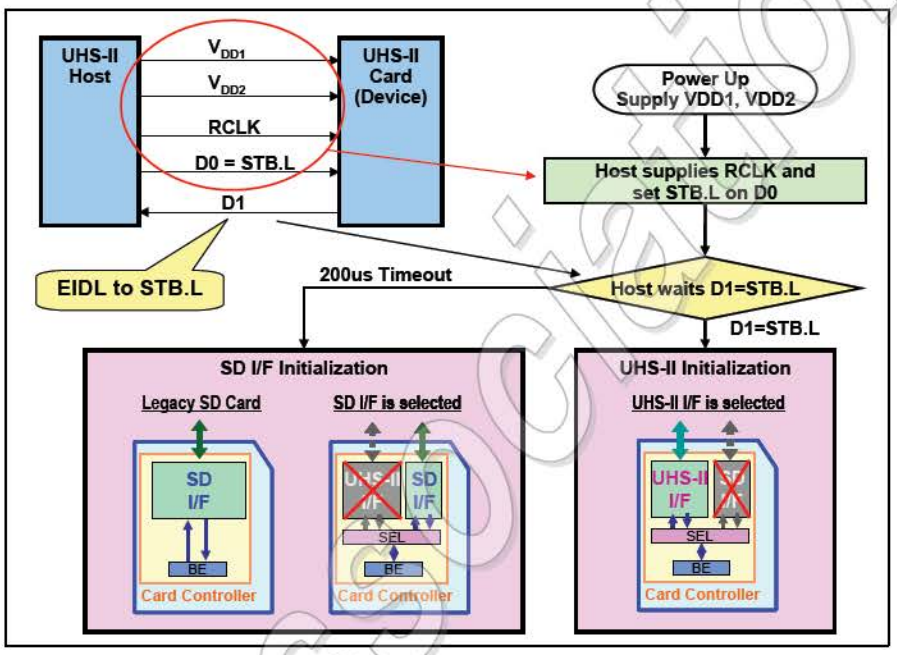


Figure 3-19 : UHS-II Interface Detection

Figure 3-20 shows abstract of UHS-II Initialization sequence. The first step is PHY initialization. PLL is activated and synchronized. Before completing PHY Initialization period, SD Bus I/F is disabled. The second step is Device Initialization. Backend functions of devices are initialized. The third step is Enumeration. 4-bit unique Device ID is assigned to each device to be able to select one of devices by a Device ID. The fourth step is Configuration. UHS-II register is set to be able to use UHS-II devices in optimized bus sequence. The fifth step is SD-TRAN Initialization. UHS-II emulates SD Commands by the SD-TRAN. SD-TRAN Initialization is equivalent to SD Bus Initialization but host issues SD Commands in UHS-II packets. UHS-II card accepts most SD commands except some specific commands. Refer to Section 4.7.5 about the difference of SD command definition in UHS-II. If CMD0 is received, the UHS-II card re-starts from SD-TRAN initialization.

Figure 3-21 shows SD Bus I/F Initialization sequence for UHS-II Card. UHS-II card shall disable UHS-II Interface before execution of ACMD41 is completed. If VDD2 is provided during SD Interface initialization of UHS-II Card, host shall continue to provide VDD2. VDD2 may be off by power cycle with VDD1 before starting SD Interface initialization. On detecting non UHS-II card, host may turn off VDD2 anytime.

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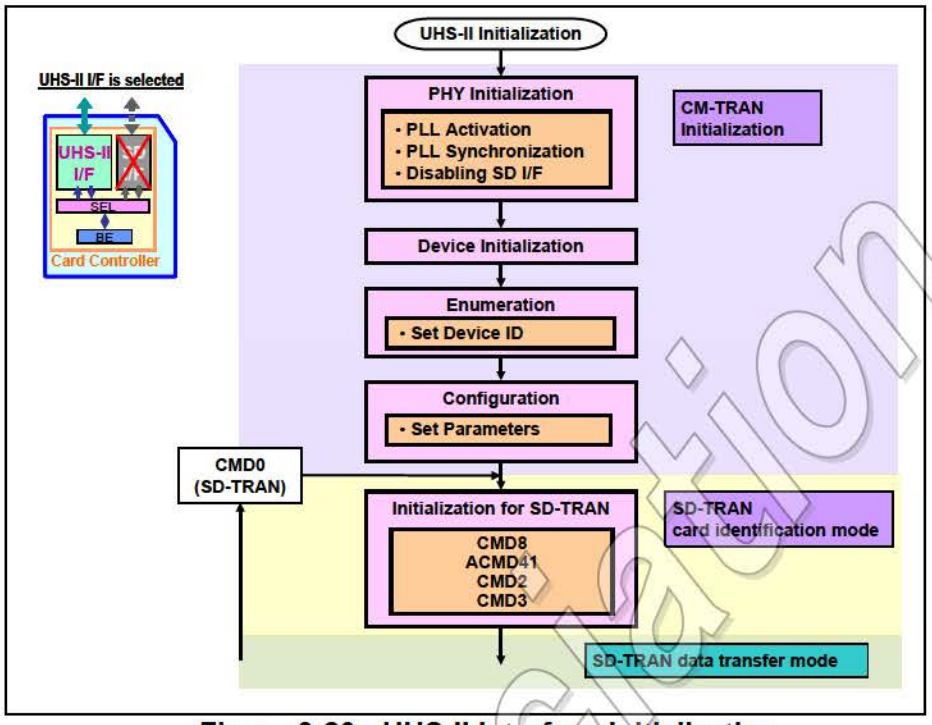


Figure 3-20 : UHS-II Interface Initialization

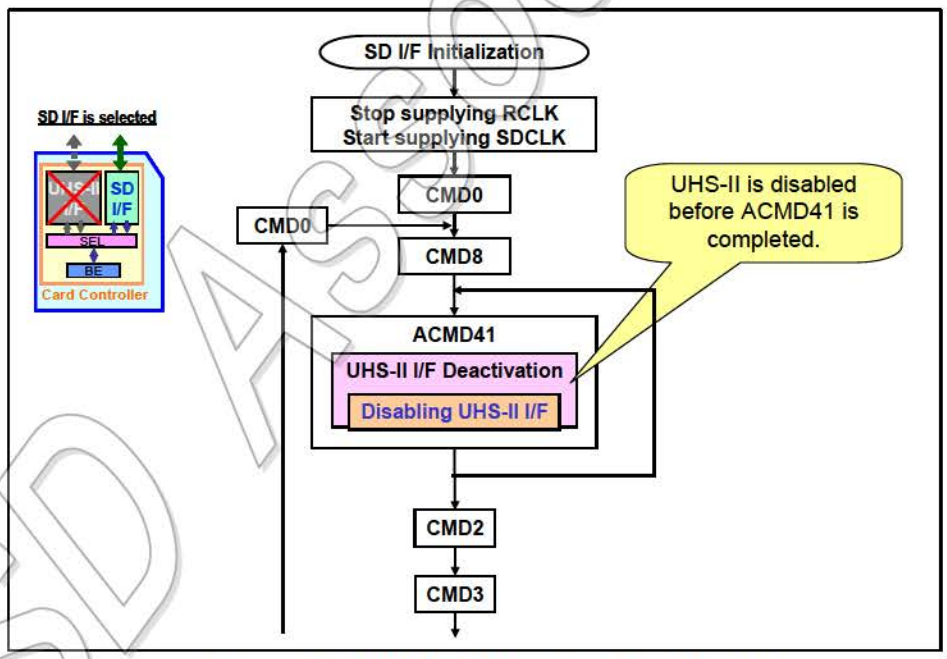


Figure 3-21 : UHS-II Interface Deactivation

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3.10.5 Summary of Bus Speed Mode for UHS-II Card

Bus Speed Mode*1	Max. Bus Speed	Max. Clock Frequency	Signal Voltage	Max. Power*2 [W]			
	[MB/s]	[MHz]	[V]	SDSC*3	SDHC*4	SDXC*5	
HD312	312	52	0.4	-	2.88*6	2.88*6	UHS-II I/F*8
FD156	156	52	0.4	-	2.88*6	2.88*6	
SDR104	104	208	1.8	-	2.88*6	2.88*6	SD Bus I/F
SDR50	50	100	1.8	-	1.44	1.44	
DDR50	50	50	1.8	-	1.44	1.44	
SDR25	25	50	1.8	-	0.72	0.72	
SDR12	12.5	25	1.8	-	0.36	0.36/0.54*7	
High Speed	25	50	3.3	0.72	0.72	0.72	
Default Speed	12.5	25	3.3	0.36	0.36	0.36/0.54*7	

*1: The card supports a UHS-I mode shall support all lower UHS-I modes.
*2: Host may control card power by the Power Limit Function of CMD6
*3: SDSC stands for SD Standard Capacity Memory Card.
*4: SDHC stands for SD High Capacity Memory Card.
*5: SDXC stands for SD Extended Capacity Memory Card.
*6: The actual maximum current may vary from the limit described in this table. It is limited by the Mechanical Addenda in the sections that define the thermal profile of the device and the connector profile.
*7: Host may select either card power by XPC in ACMD41.
In SPI mode, XPC is not supported and the power shall be up to 0.36W (3.6V 100mA).
*8: Minimum power requirement of host in UHS-II mode is 0.72W and it is applied from PHY Initialization.

Table 3-9 : Bus Speed Modes of UHS-II Card

Table 3-10 shows Card Types and Supported Bus Speed Modes.
It is recommended that UHS-II hosts implement the UHS-I mode (at least SDR50) to provide backward compatibility with UHS-I cards.

Card Classification		SPI	DS	HS	SDR50	SDR104	DDR50	FD156	HD312
SDSC		M	M	O	N/A	N/A	N/A	N/A	N/A
SDHC	Non UHS	M	M	O	N/A	N/A	N/A	N/A	N/A
	UHS50	M	M	M	M	N/A	O (Standard SD) M (microSD)	N/A	N/A
	UHS104	M	M	M	M	M	O (Standard SD) M (microSD)	N/A	N/A
	UHS156	M	M	M	M	O	O (Standard SD) M (microSD)	M	O
SDXC	Non UHS	M	M	O	N/A	N/A	N/A	N/A	N/A
	UHS50	M	M	M	M	N/A	O (Standard SD) M (microSD)	N/A	N/A
	UHS104	M	M	M	M	M	O (Standard SD) M (microSD)	N/A	N/A
	UHS156	M	M	M	M	O	O (Standard SD) M (microSD)	M	O

Table 3-10 : Bus Speed Mode Option / Mandatory

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4. SD Memory Card Functional Description

4.1 General

All communication between host and cards is controlled by the host (master). The host sends commands of two types: broadcast and addressed (point-to-point) commands.

- **Broadcast commands**
  Broadcast commands are intended for all cards. Some of these commands require a response.
- **Addressed (point-to-point) commands**
  The addressed commands are sent to the addressed card and cause a response from this card.
  A general overview of the command flow is shown in Figure 4-1 for card identification mode and in Figure 4-13 for data transfer mode. The commands are listed in the command tables (Table 4-22-Table 4-31). The dependencies between current state, received command, and following state are listed in Table 4-34. In the following sections, the various card operation modes will be described first. Afterwards, the restrictions for controlling the clock signal are defined. All SD Memory Card commands, along with the corresponding responses, state transitions, error conditions and timings are presented in the succeeding sections.
  Two operation modes are defined for the SD Memory Card system (host and cards):
- **Card identification mode**
  The host will be in card identification mode after reset and while it is looking for new cards on the bus. Cards will be in this mode after reset until the SEND_RCA command (CMD3) is received.
- **Data transfer mode**
  Cards will enter data transfer mode after their RCA is first published. The host will enter data transfer mode after identifying all the cards on the bus.

The following table shows the dependencies between operation modes and card states. Each state in the SD Memory Card state diagram (see Figure 4-1) is associated with one operation mode:

Card state	Operation mode
Inactive State	inactive
Idle State	card identification mode
Ready State	
Identification State	
Stand-by State	data transfer mode
Transfer State	
Sending-data State	
Receive-data State	
Programming State	
Disconnect State	

Table 4-1: Overview of Card States vs. Operation Modes

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4.2 Card Identification Mode

While in card identification mode the host resets all the cards that are in card identification mode, validates operation voltage range, identifies cards and asks them to publish Relative Card Address (RCA). This operation is done to each card separately on its own CMD line. All data communication in the Card Identification Mode uses the command line (CMD) only.

During the card identification process, the card shall operate in the SD clock frequency of the identification clock rate f_{OD}.

4.2.1 Card Reset

In SD Mode, the command GO_IDLE_STATE (CMD0) is the software reset command and sets each card into *Idle State* regardless of the current card state. Cards in *Inactive State* are not affected by this command.

After power-on by the host, all cards are in *Idle State*, including the cards that have been in *Inactive State* before.

After power-on or CMD0, all cards' CMD lines are in input mode, waiting for start bit of the next command. The cards are initialized with a default relative card address (RCA=0x0000) and with a default driver strength with 400KHz clock frequency. In case of 3.3V signaling, default driver strength is specified by the Driver Stage Register (DSR) if supported and selected highest driving current capability. In case of 1.8V signaling, default driver strength is specified by type B driver.

In UHS-II Mode, RCA is not cleared to 0x0000 by CMD0 and kept its Device ID, which is determined by Enumeration.

4.2.2 Operating Condition Validation

At the start of communication between the host and the card, the host may not know the card supported voltage and the card may not know whether it supports the current supplied voltage. The host issues a reset command (CMD0) with a specified voltage while assuming it may be supported by the card. To verify the voltage, a following new command (CMD8) is defined in the Physical Layer Specification Version 2.00.

SEND_IF_COND (CMD8) is used to verify SD Memory Card interface operating condition. The card checks the validity of operating condition by analyzing the argument of CMD8 and the host checks the validity by analyzing the response of CMD8 (See Chapter 4.3.13). The supplied voltage is indicated by VHS field in the argument. The card assumes the voltage specified in VHS as the current supplied voltage. Only 1-bit of VHS shall be set to 1 at any given time. Both CRC and check pattern are used for the host to check validity of communication between the host and the card.

If the card can operate on the supplied voltage, the response echoes back the supply voltage and the check pattern that were set in the command argument.

If the card cannot operate on the supplied voltage, it returns no response and stays in idle state. It is mandatory to issue CMD8 prior to first ACMD41 to initialize SDHC or SDXC Card (See Figure 4-1). Receipt of CMD8 makes the cards realize that the host supports the Physical Layer Version 2.00 or later and the card can enable new functions.

SD_SEND_OP_COND (ACMD41) is designed to provide SD Memory Card hosts with a mechanism to identify and reject cards which do not match the V_{DD} range desired by the host. This is accomplished by the host sending the required V_{DD} voltage window as the operand of this command (See Chapter 5.1). Cards which cannot perform data transfer in the specified range shall discard themselves from further bus operations and go into *Inactive State*. The levels in the OCR register shall be defined accordingly (See Chapter 5.1). Note that ACMD41 is application specific command; therefore APP_CMD (CMD55) shall always precede ACMD41. The RCA to be used for CMD55 in *idle_state* shall be the card's default RCA = 0x0000.

After the host issues a reset command (CMD0) to reset the card, the host shall issue CMD8 prior to ACMD41 to re-initialize the SD Memory card.

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Figure 4-1 shows State Diagram of card Identification mode for SD I/F. In case of UHS-II mode, refer to SD-TRAN Section of the UHS-II Addendum.

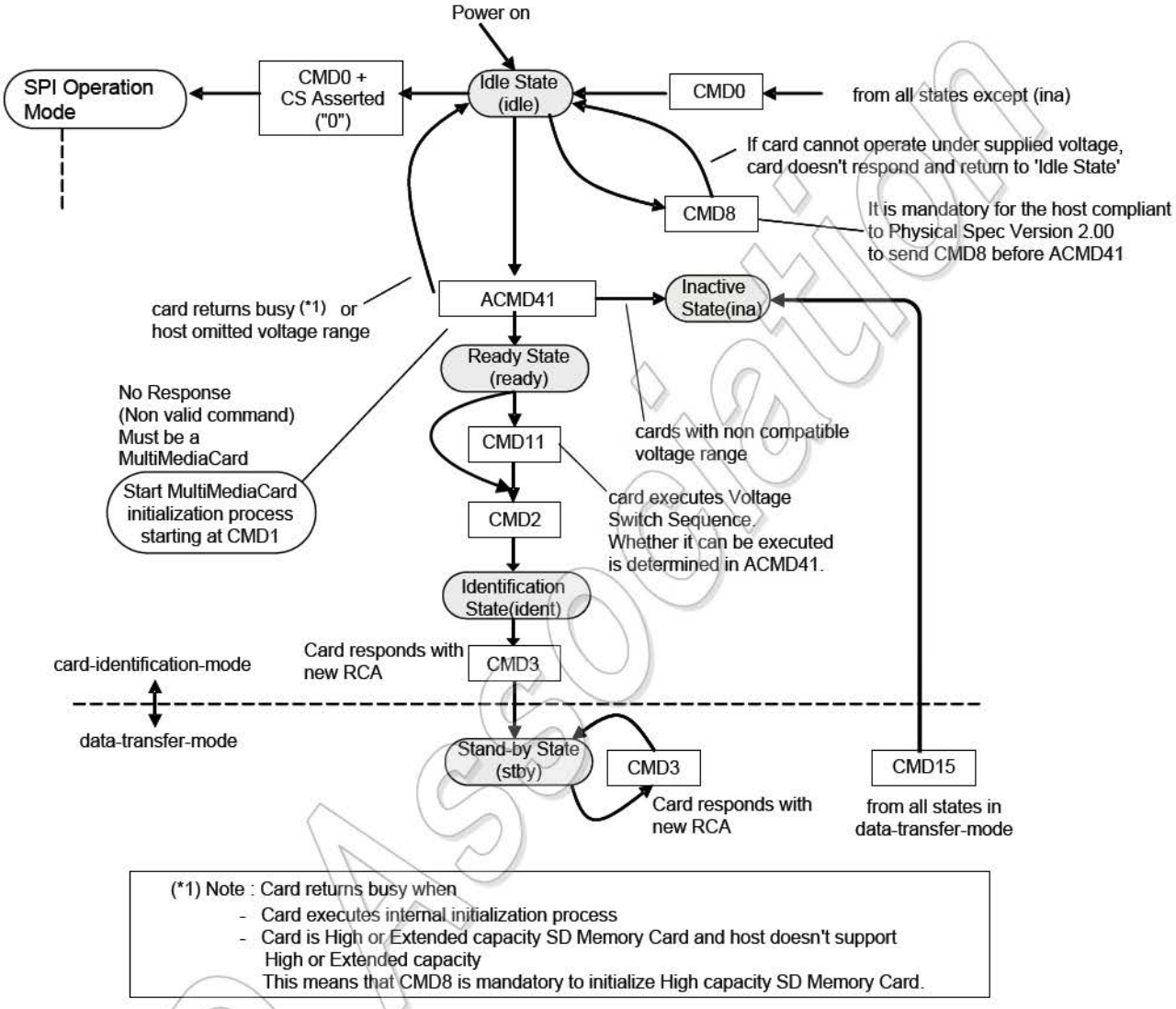


Figure 4-1: SD Memory Card State Diagram (card identification mode)

By setting the OCR to zero in the argument of ACMD41, the host can query each card and determine the common voltage range before sending out-of-range cards into the *Inactive State* (query mode). This query should be used if the host is able to select a common voltage range or if a notification to the application of non-usable cards in the stack is desired. The card does not start initialization and ignores HCS in the argument (refer to Section 4.2.3) if ACMD41 is issued as a query. Afterwards, the host may choose a voltage for operation and reissue ACMD41 with this condition, sending incompatible cards into the *Inactive State*.

During the initialization procedure, the host is not allowed to change the operating voltage range. Refer to the power up sequence as described in Chapter 6.4.

4.2.3 Card Initialization and Identification Process

After the bus is activated the host starts card initialization and identification process (See Figure 4-2). The initialization process starts with SD_SEND_OP_COND (ACMD41) by setting its operational conditions and the HCS bit in the OCR. The HCS (Host Capacity Support) bit set to 1 indicates that the host supports SDHC or SDXC Card. The HCS (Host Capacity Support) bit set to 0 indicates that the host supports neither SDHC nor SDXC Card.

Receiving of CMD8 expands the ACMD41 function; HCS in the argument and CCS (Card Capacity Status) in the response. HCS is ignored by cards, which didn't respond to CMD8. However the host should set HCS to 0 if the card returns no response to CMD8. Standard Capacity SD Memory Card ignores HCS. If HCS is set to 0, SDHC and SDXC Cards never return ready status (keep busy bit to 0).

The busy bit in the OCR is used by the card to inform the host whether initialization of ACMD41 is completed. Setting the busy bit to 0 indicates that the card is still initializing. Setting the busy bit to 1 indicates completion of initialization. Card initialization shall be completed within 1 second from the first ACMD41. The host repeatedly issues ACMD41 for at least 1 second or until the busy bit are set to 1.

The card checks the operational conditions and the HCS bit in the OCR only at the first ACMD41 with setting voltage window in the argument. While repeating ACMD41, the host shall not issue another command except CMD0.

If the card responds to CMD8, the response of ACMD41 includes the CCS field information. CCS is valid when the card returns ready (the busy bit is set to 1). CCS=0 means that the card is SDSC. CCS=1 means that the card is SDHC or SDXC.

The host performs the same initialization sequence to all of the new cards in the system. Incompatible cards are sent into *Inactive State*. The host then issues the command ALL_SEND_CID (CMD2), to each card to get its unique card identification (CID) number. Card that is unidentified (i.e. which is in *Ready State*) sends its CID number as the response (on the CMD line). After the CID was sent by the card it goes into *Identification State*. Thereafter, the host issues CMD3 (SEND_RELATIVE_ADDR) asks the card to publish a new relative card address (RCA), which is shorter than CID and which is used to address the card in the future data transfer mode. Once the RCA is received the card state changes to the *Stand-by State*. At this point, if the host wants to assign another RCA number, it can ask the card to publish a new number by sending another CMD3 command to the card. The last published RCA is the actual RCA number of the card.

The host repeats the identification process, i.e. the cycles with CMD2 and CMD3 for each card in the system.

Initialization of SDXC is identical to SDHC. User area capacity of SDXC card is specified by C_SIZE and it shall be more than or equal to 32GB.

Figure 4-2 shows Card Initialization and Identification for SD I/F. In case of UHS-II mode, refer to SD-TRAN Section of the UHS-II Addendum.

Application Notes:
The host shall set ACMD41 timeout more than 1 second to abort repeat of issuing ACMD41 when the card does not indicate ready. The timeout count starts from the first ACMD41 which is set voltage window in the argument.

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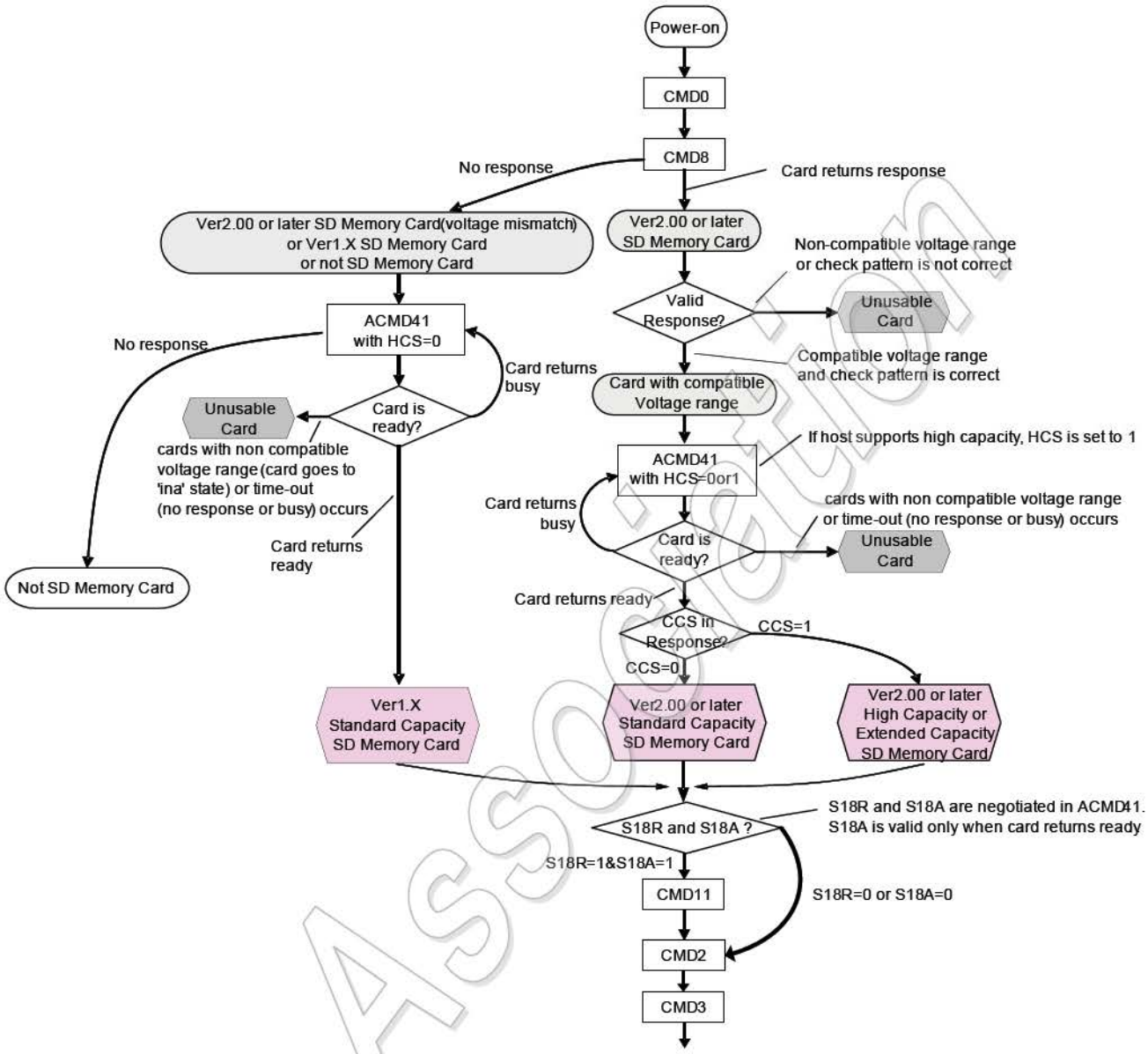


Figure 4-2: Card Initialization and Identification Flow (SD mode)

SD Association

4.2.3.1 Initialization Command (ACMD41)

Followings are general rules of the argument of ACMD41:

(1) If the voltage window field (bit 23-0) in the argument is set to zero, it is called "inquiry CMD41" that does not start initialization and is use for getting OCR. The inquiry ACMD41 shall ignore the other field (bit 31-24) in the argument.

(2) If the voltage window field (bit 23-0) in the argument is set to non-zero at the first time, it is called "first ACMD41" that starts initialization. The other field (bit 31-24) in the argument is effective.

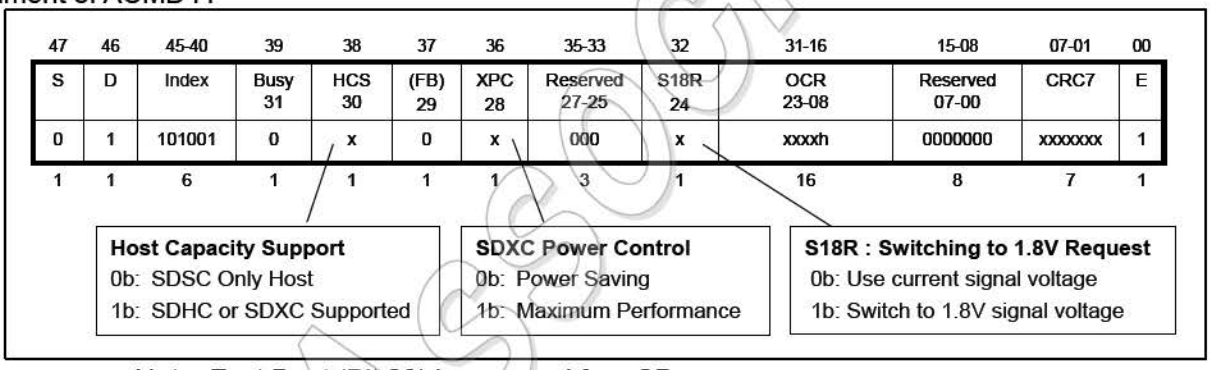
(3) The argument of following ACMD41 shall be the same as that of the first ACMD41.

Figure 4-3 shows argument format and Figure 4-4 shows response format. Two new fields are added to the argument of ACMD41.

If a SDXC Card is initialized with XPC=0, the card is operating at up to 0.36W (100mA at 3.6V on VDD1) in Default Speed or SDR12, and if the card does not support Speed Class, Class 0 is indicated in SD Status. If a SDXC Card is initialized with XPC=1, the card is operating at up to 0.54W (150mA at 3.6V on VDD1) in Default Speed or SDR12, and the card supports Speed Class. Re-initialization is required to change XPC selection.

UHS-I supported host sets S18R=1 in the argument of ACMD41 to request the card to switch 1.8V signaling level. UHS-I card respond with S18A=1 in the response of ACMD41 (if in 3.3V signaling mode) and then host can issue voltage switch command. Once voltage switch is performed, UHS-I card indicates S18A=0 to keep current signal voltage. In UHS-II mode, the card always indicates S18A=0.

(1) Argument of ACMD41



Note: Fast Boot (Bit 29) is reserved for eSD.

Figure 4-3 : Argument of ACMD41

(2) Response of ACMD41 (R3)

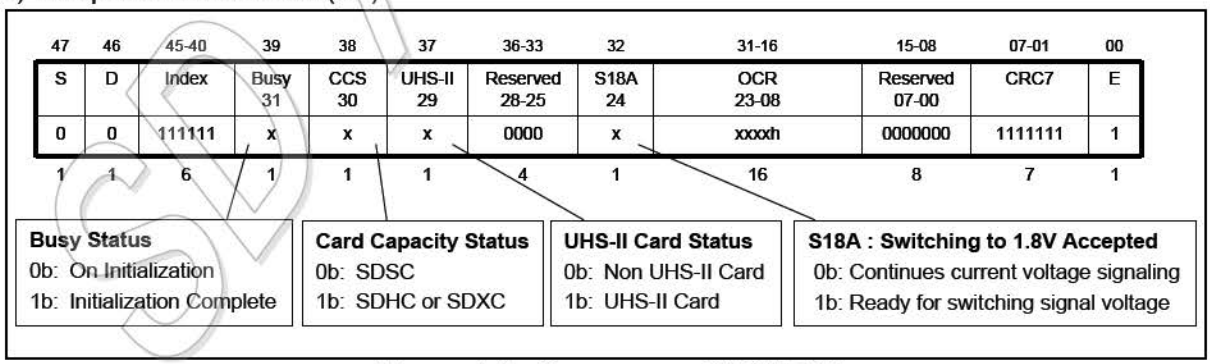


Figure 4-4 : Response of ACMD41

CCS (Bit 30), UHS-II (Bit 29) and S18A (Bit 24) are valid when Busy (Bit 31) is set to 1.

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4.2.4 Bus Signal Voltage Switch Sequence

4.2.4.1 Initialization Sequence for UHS-I

Figure 4-5 shows sequence of commands to perform voltage switch and Figure 4-6 shows initialization flow chart for UHS-I hosts. Red and yellow boxes are new procedure to initialize UHS-I card.

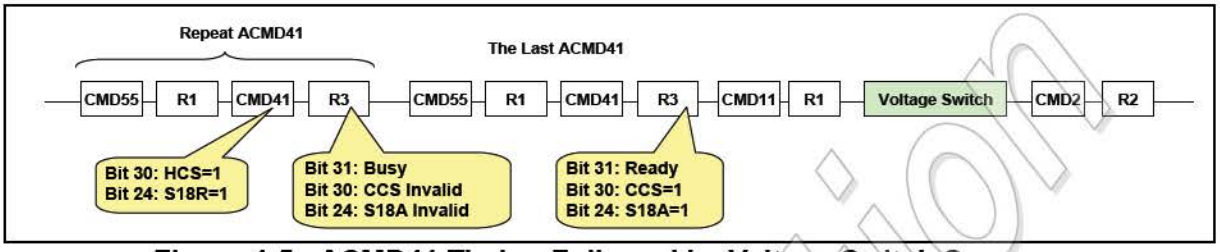


Figure 4-5 : ACMD41 Timing Followed by Voltage Switch Sequence

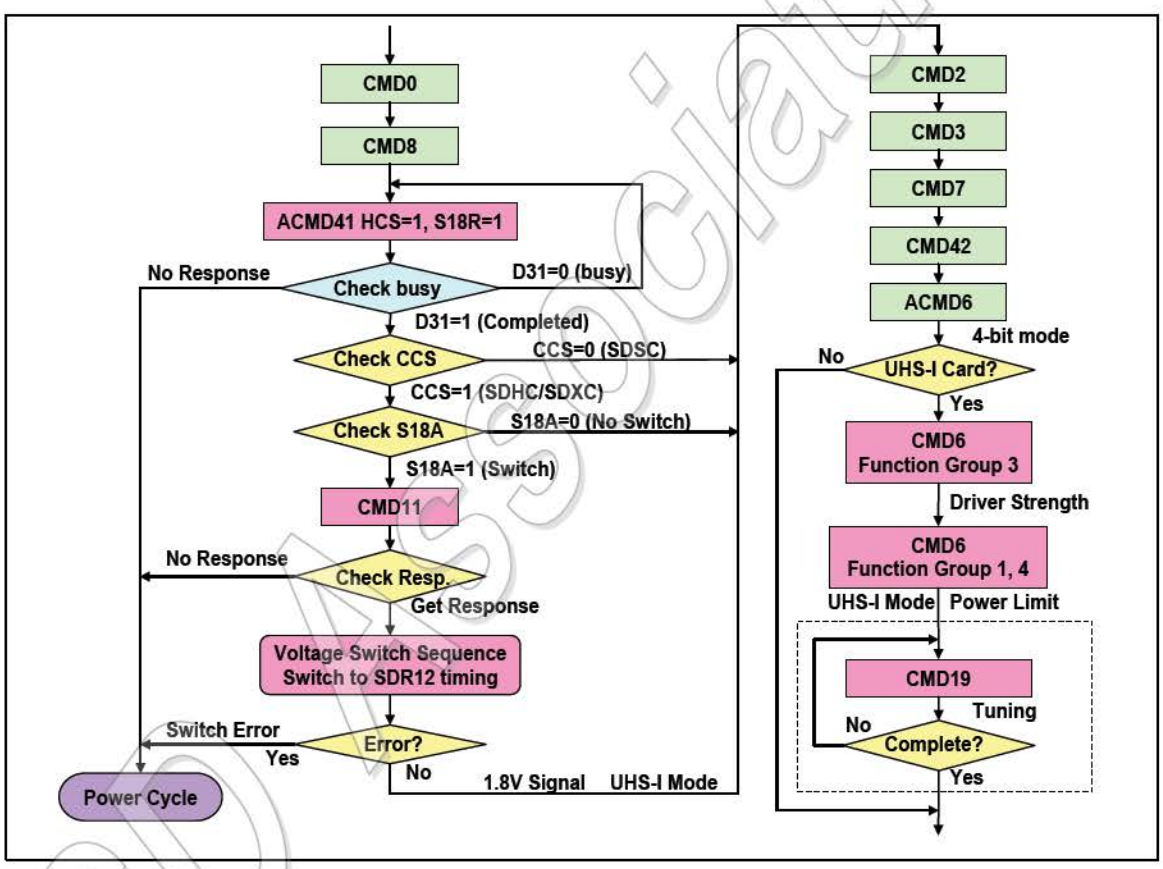


Figure 4-6 : UHS-I Host Initialization Flow Chart

When signaling level is 3.3V, host repeats to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready. The argument (HCS and S18R) of the first ACMD41 is effective but the all following ACMD41 should be issued with the same argument. If Bit 31 indicates ready, host needs to check CCS and S18A. The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use current signaling level. S18A=1 means that voltage switch is allowed and host issues CMD11 to invoke voltage switch sequence. By receiving CMD11, the card returns R1 response and start voltage switch sequence. No response of CMD11 means that S18A was 0 and therefore host should not have sent CMD11. Completion of voltage switch sequence is checked by high level of DAT[3:0]. Any bit of DAT[3:0] can be checked depends on ability of the host.

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When entering tran state, CARD_IS_LOCKED status in the R1 response should be checked (it is indicated in the response of CMD7). If the card is locked, CMD42 is required to unlock the card. If the card is unlocked, CMD42 can be skipped.
In case of UHS-I card, appropriate driver strength is selected by CMD6 Function Group 3 and one of UHS-I modes is selected by CMD6 Function Group 1.
In SDR50 and SDR104 modes, if tuning of sampling point is required, CMD19 is repeatedly issued until tuning is completed.

4.2.4.2 Timing to Switch Signal Voltage

This section is a blank in the Simplified Specification.

4.2.4.3 Timing of Voltage Switch Error Detection

This section is a blank in the Simplified Specification.

4.2.4.4 Voltage Switch Command

Figure 4-9 shows Voltage Switch Command (CMD11) definition. CMD11 can be executed in ready state and doesn't change the state. Even if the card is locked, CMD11 can be executed. Returning R1 type response means the card starts voltage switch sequence. If the host detects no response, power cycle should be executed.
There are four cases that the card indicates no response to CMD11.

(1) The card does not support voltage switch.
(2) The card supports voltage switch but ACMD41 is received with S18R=0.
(3) The card receives CMD11 not in ready state.
(4) Signaling level is already switched to 1.8V.

For all above cases, CMD11 is treated as an illegal command.

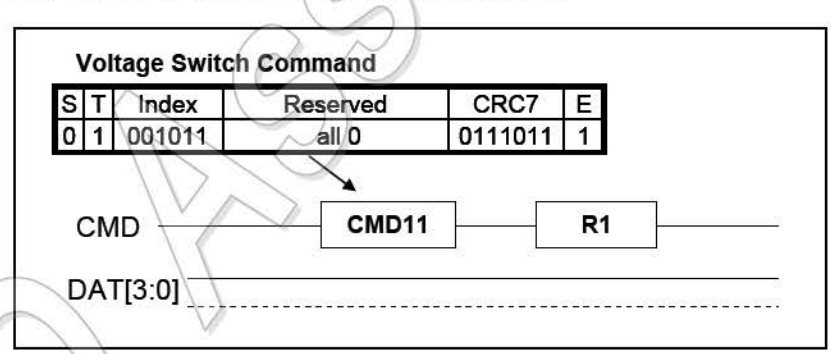


Figure 4-9 : Voltage Switch Command

4.2.4.5 Tuning Command

A known data block ("Tuning block") can be used to tune sampling point for tuning required hosts. The tuning capability of sampling point is mandatory for HOST-SDR-VD and optional for HOST-SDR-FD. This procedure gives the system optimal timing for each specific host and card combination and compensates for static delays in the timing budget including process, voltage and different PCB loads and skews.

CMD19 is defined for Send Tuning Block Command. R1 type response is defined. CMD19 can be executed in transfer state of 1.8V signaling mode while the card is unlocked. The other case, CMD19 is treated as illegal command. Data block, carried by DAT[3:0], contains a pattern for tuning sampling position to receive data on the CMD and DAT[3:0] line. The block length of CMD19 is fixed and CMD16

is not required.

The tuning command (CMD19) follows the timing of the single block read command as described in Figure 4-10.

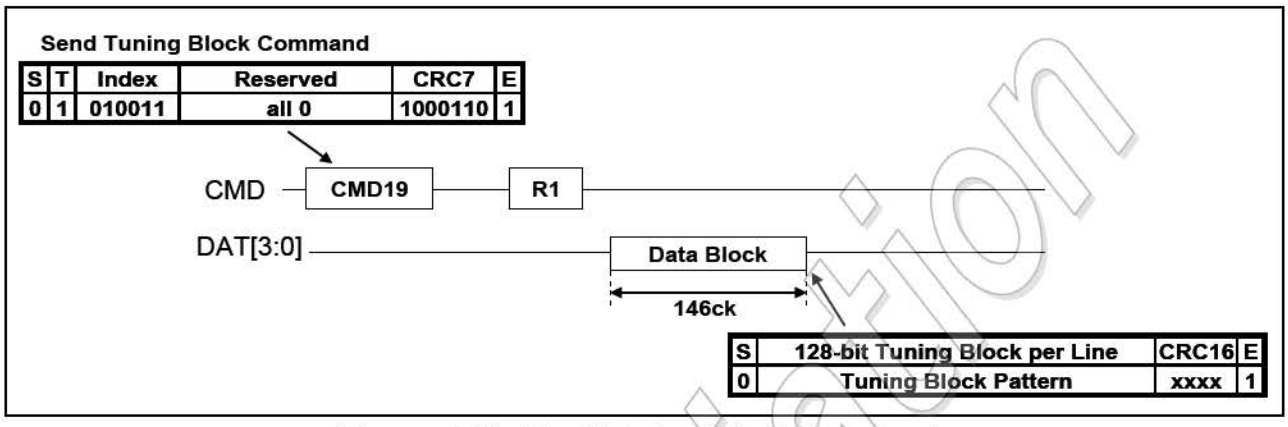


Figure 4-10 : Send Tuning Block Command

This sequence is defined as multiple, consecutive executions of CMD19 that are sent from the host and responded by the card, without any other command mixed between them.
The card shall complete a sequence of 40 times CMD19 executions in no more than 150ms. The tuning process is normally shorter than 40 executions of CMD19, and therefore should be shorter than 150ms.
The sequence period definition does not include any host processing time. If host needs time to process CMD19 between executions, the sequence may be longer by this amount of time.

FF0FFF00	FFCCC3CC	C33CCCFF	FEFFFEEF
FFDFFFDD	FFFBFFFB	BFFF7FFF	77F7BDEF
FFF0FFF0	0FFCCC3C	CC33CCCF	FFEFFFEE
FFFDFFFD	DFFFBFFF	BBFFF7FF	F77F7BDE

Table 4-3 : Tuning Block Pattern

A part of this section is not described.

4.2.4.6 An Example of UHS-I System Block Diagram

This section is a blank in the Simplified Specification.

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4.3 Data Transfer Mode

Until the end of Card Identification Mode the host shall remain at f_{OD} frequency because some cards may have operating frequency restrictions during the card identification mode. In Data Transfer Mode the host may operate the card in f_{PP} frequency range. The host issues SEND_CSD (CMD9) to obtain the Card Specific Data (CSD register), e.g. block length, card storage capacity, etc.

The broadcast command SET_DSR (CMD4) configures the driver stages of all identified cards. It programs their DSR registers corresponding to the application bus layout (length) and the number of cards on the bus and the data transfer frequency. The clock rate is also switched from f_{OD} to f_{PP} at that point. SET_DSR command is an option for the card and the host.

CMD7 is used to select one card and put it into the *Transfer State*. Only one card can be in the *Transfer State* at a given time. If a previously selected card is in the *Transfer State* its connection with the host is released and it will move back to the *Stand-by State*. When CMD7 is issued with the reserved relative card address "0x0000", all cards are put back to *Stand-by State* (Note that it is the responsibility of the Host to reserve the RCA=0 for card de-selection - refer to Table 4-22, CMD7.

SD Memory Card State Diagram in UHS-II is defined by the UHS-II Addendum.

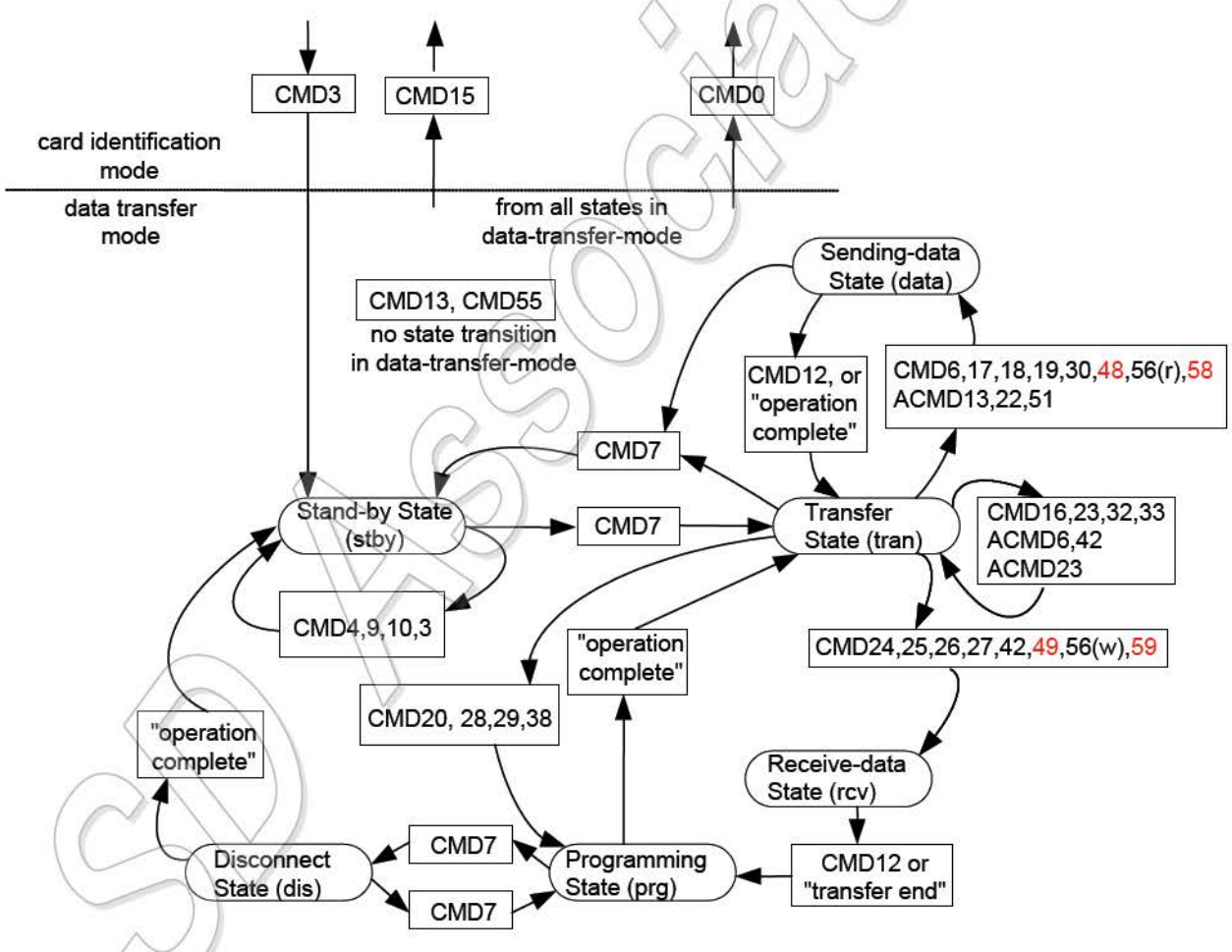


Figure 4-13: SD Memory Card State Diagram (data transfer mode)

This may be used before identifying new cards without resetting other already registered cards. Cards which already have an RCA do not respond to identification commands (ACMD41, CMD2, see Chapter 4.2.3) in this state. CMD48, CMD49, CMD58 and CMD59 are also available in UHS-II mode.

Important Note: The card de-selection is done if certain card gets CMD7 with un-matched RCA. That happens automatically if selection is done to another card and the CMD lines are common. So, in SD Memory Card system it will be the responsibility of the host either to work with common CMD line (after initialization is done) - in that case the card de-selection will be done automatically or if the CMD lines are separate then the host shall be aware to the necessity to de-select cards.
All data communication in the Data Transfer Mode is point-to point between the host and the selected card (using addressed commands). All addressed commands get acknowledged by a response on the CMD line.

The relationship between the various data transfer modes is summarized below.

- All data read commands can be aborted any time by the stop command (CMD12). The data transfer will terminate and the card will return to the *Transfer State.* The read commands are such as block read (CMD17), multiple block read (CMD18), send write protect (CMD30), send SCR (ACMD51) and general command in read mode (CMD56). (Refer to Figure 4-13 for more details.)
- All data write commands can be aborted any time by the stop command (CMD12). The write commands shall be stopped prior to deselecting the card by CMD7. The write commands are such as block write (CMD24 and CMD25), program CSD (CMD27), lock/unlock command (CMD42) and general command in write mode (CMD56). (Refer to Figure 4-13 for more details.)
- As soon as the data transfer is completed, the card will exit the data write state and move either to the *Programming State* (transfer is successful) or *Transfer State* (transfer failed).
- If a block write operation is stopped and the block length and CRC of the last block are valid, the data will be programmed.
- The card may provide buffering for block write. This means that the next block can be sent to the card while the previous is being programmed.
  If all write buffers are full, and as long as the card is in *Programming State* (see SD Memory Card state diagram Figure 4-13), the DAT0 line will be kept low (BUSY).
- There is no buffering option for write CSD, write protection and erase. This means that while the card is busy servicing any one of these commands, no other data transfer commands will be accepted. DAT0 line will be kept low as long as the card is busy and in the *Programming State*. Actually if the CMD and DAT0 lines of the cards are kept separated and the host keep the busy DAT0 line disconnected from the other DAT0 lines (of the other cards) the host may access the other cards while the card is in busy.
- Parameter set commands are *not* allowed while card is programming.
  Parameter set commands are: set block length (CMD16), erase block start (CMD32) and erase block end (CMD33).
- Read commands are *not* allowed while card is programming.
- Moving another card from *Stand-by* to *Transfer State* (using CMD7) will not terminate erase and programming operations. The card will switch to the *Disconnect State* and will release the DAT line.
- A card can be reselected while in the *Disconnect State*, using CMD7. In this case the card will move to the *Programming State* and reactivate the busy indication.
- Resetting a card (using CMD0 or CMD15) will terminate any pending or active programming operation. This may destroy the data contents on the card. It is the host's responsibility to prevent this.
- CMD34-37, CMD50 and CMD57 are reserved for SD command system expansion. State transitions for these commands are defined in each command system specification.

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4.3.1 Wide Bus Selection/Deselection

Wide Bus (4 bit bus width) operation mode may be selected/deselected using ACMD6. The default bus width after power up or GO_IDLE (CMD0) is 1 bit bus width.
In order to change the bus width two conditions shall be met:
a) The card is in '*tran state*'.
b) The card is not locked

A locked card will responds to ACMD6 as illegal command.

4.3.2 2 GByte Card

To make 2GByte card, the Maximum Block Length (READ_BL_LEN=WRITE_BL_LEN) shall be set to 1024 bytes. However, the Block Length, set by CMD16, shall be up to 512 bytes to keep consistency with 512 bytes Maximum Block Length cards (Less than and equal 2GByte cards).

4.3.3 Data Read

The DAT bus line level is high by the pull-up when no data is transmitted. A transmitted data block consists of start bits (1 or 4 bits LOW), followed by a continuous data stream. The data stream contains the payload data (and error correction bits if an off-card ECC is used). The data stream ends with end bits (1 or 4 bits HIGH). The data transmission is synchronous to the clock signal. The payload for block oriented data transfer is protected by 1 or 4 bits CRC check sum (See Chapter 0).
The Read operation from SD Memory Card may be interrupted by turning the power off. The SD Memory Card ensures that data is not destroyed during all the conditions except write or erase operations issued by the host even in the event of sudden shut down or removal.
Read command is rejected if BLOCK_LEN_ERROR or ADDRESS_ERROR occurred and no data transfer is performed.

- **Block Read**

Block read is block oriented data transfer. The basic unit of data transfer is a block whose maximum size is always 512 bytes. Smaller blocks whose starting and ending address are entirely contained within 512 bytes boundary may be transmitted.
Block Length set by CMD16 can be set up to 512 bytes regardless of READ_BL_LEN.
A CRC is appended to the end of each block ensuring data transfer integrity. CMD17 (READ_SINGLE_BLOCK) initiates a block read and after completing the transfer, the card returns to the *Transfer State*. CMD18 (READ_MULTIPLE_BLOCK) starts a transfer of several consecutive blocks. Blocks will be continuously transferred until a STOP_TRANSMISSION command (CMD12) is issued. The stop command has an execution delay due to the serial command transmission. The data transfer stops after the end bit of the stop command.
When the last block of user area is read using CMD18, the host should ignore OUT_OF_RANGE error that may occur even the sequence is correct.
If the host uses partial blocks whose accumulated length is not block aligned and block misalignment is not allowed, the card shall detect a block misalignment at the beginning of the first misaligned block, set the ADDRESS_ERROR error bit in the status register, abort transmission and wait in the *Data State* for a stop command.

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Table 4-4 defines the card behavior when a partial block accesses is enabled.
If the misaligned block is the first data block of the command (i.e. ADDRESS_ERROR was reported in the actual response to the command), then no data is transferred and the card remains in the TRAN state.

CSD value			Current Blocklen *1	Read CMD Start Address
Max block size READ_BL_LEN	Misalign	Partial		
512Bytes	0 (Disable)	1 (Enable)	1- 512 bytes	Any address is accepted. *2
1kBytes	0 (Disable)	1 (Enable)	1- 512 bytes	Any address is accepted. *2
2kBytes	0 (Disable)	1 (Enable)	1- 512 bytes	Any address is accepted. *2

*1: "Current Blocklen" size is set or changed by CMD16. If value is less than or equal 512 bytes (There are no relations with Misalign and Partial option), it is set with no error.
*2: When the Blocklen size data range crosses 512 bytes block boundary, card outputs the data until the 512 bytes block boundary" and then the data becomes invalid and CRC error also may occur. The card will send "ADDRESS_ERROR" on the next command response. Host should issue CMD12 to recover.

Table 4-4: Read Command Blocklen

4.3.4 Data Write

The data transfer format is similar to the data read format. For block oriented write data transfer, the CRC check bits are added to each data block. The card performs 1 or 4 bits CRC parity check (See Chapter 4.5) for each received data block prior to the write operation. By this mechanism, writing of erroneously transferred data can be prevented.
Write command is rejected if BLOCK_LEN_ERROR or ADDRESS_ERROR occurred and no data transfer is performed.

- **Block Write**

During block write (CMD24 - 27, 42, 56(w)) one or more blocks of data are transferred from the host to the card with 1 or 4 bits CRC appended to the end of each block by the host. A card supporting block write shall be required that Block Length set by CMD16 shall be 512 bytes regardless of WRITE_BL_LEN is set to 1k or 2k bytes.
Table 4-5 defines the card behavior when partial block accesses is disabled (WRITE_BL_PARTIAL = 0).

CSD value			Current Blocklen *1	Write CMD Start Address
Max block size WRITE_BL_LEN	Misalign	Partial		
512Bytes	0 (Disable)	0 (Disable)	512 bytes *2	n * 512 bytes *3 (n: Integer)
1kBytes	0 (Disable)	0 (Disable)	512 bytes *2	n * 512 bytes *3 (n: Integer)
2kBytes	0 (Disable)	0 (Disable)	512 bytes *2	n * 512 bytes *3 (n: Integer)

*1: "Current Blocklen" size is set or changed by CMD16. If value is less than 512 bytes (there are no relations with Misalign and Partial option), it is set with no error. And then "Current Blocklen" size is tested when write command execution.
*2: If the current Blocklen is other than this value, the card indicates "BLOCK_LEN_ERROR" on the Write command response.
*3: If start address is other than this value, the card will send "ADDRESS_ERROR" on the Write command response.

Table 4-5: Write Command Blocklen

If WRITE_BL_PARTIAL is allowed (=1) then smaller blocks, up to resolution of one byte, can be used as well. If the CRC fails, the card shall indicate the failure on the DAT line (see below); the transferred data will be discarded and not be written, and all further transmitted blocks (in multiple block write

mode) will be ignored.
Multiple block write command shall be used rather than continuous single write command to make faster write operation.
If the host uses partial blocks whose accumulated length is not block aligned and block misalignment is not allowed (CSD parameter WRITE_BLK_MISALIGN is not set), the card shall detect the block misalignment error and abort programming before the beginning of the first misaligned block. The card shall set the ADDRESS_ERROR error bit in the status register, and while ignoring all further data transfer, wait in the *Receive-data-State* for a stop command.
Note that the first data block is misaligned for write command (i.e. ADDRESS_ERROR is reported in the actual response of the write command), the card remains in tran state and no data is programmed.
The write operation shall also be aborted if the host tries to write over a write protected area. In this case, however, the card shall set the WP_VIOLATION bit.
Programming of the CSD register does not require a previous block length setting. The transferred data is also CRC protected. If a part of the CSD register is stored in ROM, then this unchangeable part shall match the corresponding part of the receive buffer. If this match fails, then the card will report an error and not change any register contents.
Some cards may require long and unpredictable times to write a block of data. After receiving a block of data and completing the CRC check, the card will begin writing and hold the DAT0 line low if its write buffer is full and unable to accept new data from a new WRITE_BLOCK command. The host may poll the status of the card with a SEND_STATUS command (CMD13) at any time, and the card will respond with its status. The status bit READY_FOR_DATA indicates whether the card can accept new data or whether the write process is still in progress). The host may deselect the card by issuing CMD7 (to select a different card) which will displace the card into the *Disconnect State* and release the DAT line without interrupting the write operation. When reselecting the card, it will reactivate busy indication by pulling DAT to low if programming is still in progress and the write buffer is unavailable. Actually, the host may perform simultaneous write operation to several cards with inter-leaving process. The interleaving process can be done by accessing each card separately while other cards are in busy. This process can be done by proper CMD and DAT0-3 line manipulations (disconnection of busy cards).

- **Pre-erased Setting prior to a Multiple Block Write Operation**

Setting a number of write blocks to be pre-erased (ACMD23) will make a following Multiple Block Write operation faster compared to the same operation without preceding ACMD23. The host will use this command to define how many number of write blocks are going to be send in the next write operation. If the host will terminate the write operation (Using stop transmission) before all the data blocks sent to the card the content of the remaining write blocks is undefined(can be either erased or still have the old data). If the host will send more number of write blocks than defined in ACMD23 the card will erase block one by one(as new data is received). This number will be reset to the default (=1) value after Multiple Blocks Write operation.
It is recommended using this command preceding CMD25, some of the cards will be faster for Multiple Write Blocks operation. Note that the host should send ACMD23 just before WRITE command if the host wants to use the pre-erased feature. If not, pre-erase-count might be cleared automatically when another commands (ex: Security Application Commands) are executed.

- **Send Number of Written Blocks**

Systems that use Pipeline mechanism for data buffers management are, in some cases, unable to determine which block was the last to be well written to the flash if an error occurs in the middle of a Multiple Blocks Write operation. The card will respond to ACMD22 with the number of well written blocks.

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4.3.5 Erase

It is desirable to erase many write blocks simultaneously in order to enhance the data throughput. Identification of these write blocks is accomplished with the ERASE_WR_BLK_START (CMD32), ERASE_WR_BLK_END (CMD33) commands.

The host should adhere to the following command sequence: ERASE_WR_BLK_START, ERASE_WR_BLK_END and ERASE (CMD38).

If an erase (CMD38) or address setting (CMD32, 33) command is received out of sequence, the card shall set the ERASE_SEQ_ERROR bit in the status register and reset the whole sequence.

If an out of sequence command (except SEND_STATUS) is received, the card shall set the ERASE_RESET status bit in the status register, reset the erase sequence and execute the last command.

If the erase range includes write protected sectors, they shall be left intact and only the non-protected sectors shall be erased. The WP_ERASE_SKIP status bit in the status register shall be set.

The address field in the address setting commands is a write block address in byte units. The card will ignore all LSB's below the WRITE_BL_LEN (see CSD) size.

As described above for block write, the card will indicate that an erase is in progress by holding DAT0 low. The actual erase time may be quite long, and the host may issue CMD7 to deselect the card or perform card disconnection, as described in the Block Write section, above.

The data at the card after an erase operation is either '0' or '1', depends on the card vendor.

The SCR register bit DATA_STAT_AFTER_ERASE (bit 55) defines whether it is '0' or '1'.

4.3.6 Write Protect Management

Three write protect methods are supported in the SD Memory Card as follows:

- Mechanical write protect switch (Host responsibility only)
- Card internal write protect (Card's responsibility)
- Password protection card lock operation.

- **Mechanical Write Protect Switch**

A mechanical sliding tablet on the side of the card (refer to the Part 1 Standard Size SD Card Mechanical Addendum) will be used by the user to indicate that a given card is write protected or not. If the sliding tablet is positioned in such a way that the window is open it means that the card is write protected. If the window is close the card is not write-protected.

A proper, matched, switch on the socket side will indicate to the host that the card is write-protected or not. It is the responsibility of the host to protect the card. The position of the write protect switch is unknown to the internal circuitry of the card.

- **Card's Internal Write Protection (Optional)**

This section is a blank in the Simplified Specification.

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4.3.7 Card Lock/Unlock Operation

4.3.7.1 General

The password protection feature enables the host to lock a card while providing a password, which later will be used for unlocking the card. The password and its size are kept in a 128-bit PWD and 8-bit PWD_LEN registers, respectively. These registers are non-volatile so that a power cycle will not erase them.

Locked cards respond to (and execute) all commands in the "basic" command class (class 0), ACMD41, CMD16 and "lock card" command class. Thus, the host is allowed to reset, initialize, select, query for status, etc., but not to access data on the card. If the password was previously set (the value of PWD_LEN is not 0), the card will be locked automatically after power on.

Similar to the existing CSD register write commands, the lock/unlock command is available in "transfer state" only. This means that it does not include an address argument and the card shall be selected before using it.

The card lock/unlock command has the structure and bus transaction type of a regular single block write command. The transferred data block includes all the required information of the command (password setting mode, PWD itself, card lock/unlock etc.). Table 4-6 describes the structure of the command data block. Note that the host compliant to the Physical Specification Version 2.00 or later shall set reserved bits (Bit7-4) to 0 when issuing CMD42.

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Reserved (shall be set to 0)				ERASE	LOCK_ UNLOCK	CLR_ PWD	SET_ PWD
1	PWDS_LEN							
2	Password data							
...								
PWDS_LEN + 1								

Table 4-6: Lock Card Data Structure

- **ERASE:** 1 Defines Forced Erase Operation. In byte 0, bit 3 will be set to 1 (all other bits shall be 0). All other bytes of this command will be ignored by the card.
- **LOCK/UNLOCK**: 1 = Locks the card. 0 = Unlock the card (note that it is valid to set this bit together with SET_PWD but it is not allowed to set it together with CLR_PWD).
- **CLR_PWD**: 1 = Clears PWD.
- **SET_PWD**: 1 = Set new password to PWD
- **PWDS_LEN**: Defines the following password(s) length (in bytes). In case of a password change, this field includes the total password lengths of old and new passwords. The password length is up to 16 bytes. In case of a password change, the total length of the old password and the new password can be up to 32 bytes.
- **Password data:** In case of setting a new password, it contains the new password. In case of a password change, it contains the old password followed by the new password.

The data block size shall be defined by the host before it sends the card lock/unlock command. The block length shall be set to greater than or equal to the required data structure of the lock/unlock command. In the following explanation, changing block size by CMD16 is not a mandatory requirement for the lock/unlock command.

Since block length shall always be even in DDR50 mode, the block length for CMD42 shall always be rounded up to an even size. If CMD16 is used prior to CMD42 to set the block length, it shall always specify an even length.

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The following paragraphs define the various lock/unlock command sequences:

- **Setting the Password**
  - Select a card (CMD7), if not previously selected.
  - Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bits password size (in bytes), and the number of bytes of the new password. In the case that a password *replacement* is done, then the block size shall consider that both passwords-the old and the new one-are sent with the command.
  - Send the Card Lock/Unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode (SET_PWD), the length (PWDS_LEN) and the password itself. In the case that a password *replacement* is done, then the length value (PWDS_LEN) shall include both passwords (the old and the new one) and the password data field shall include the old password (currently used) followed by the new password. Note that the card shall handle the calculation of the new password length internally by subtracting the old password length from PWDS_LEN field.
  - In the case that the sent old password is not correct (not equal in size and content), then the LOCK_UNLOCK_FAILED error bit will be set in the status register and the old password does not change. In the case that the sent old password is correct (equal in size and content), then the given new password and its size will be saved in the PWD and PWD_LEN registers, respectively.

Note that the password length register (PWD_LEN) indicates if a password is currently set. When it equals 0, there is no password set. If the value of PWD_LEN is not equal to zero, the card will lock itself after power up. It is possible to lock the card immediately in the current power session by setting the LOCK/UNLOCK bit (while setting the password) or sending an additional command for card lock.

- **Reset the Password:**
  - Select a card (CMD7), if not previously selected.
  - Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.
  - Send the card lock/unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode CLR_PWD, the length (PWDS_LEN), and the password itself. If the PWD and PWD_LEN content match the sent password and its size, then the content of the PWD register is cleared and PWD_LEN is set to 0. If the password is not correct, then the LOCK_UNLOCK_FAILED error bit will be set in the status register.

- **Locking the Card:**
  - Select a card (CMD7), if not previously selected.
  - Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.
  - Send the card lock/unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode LOCK, the length (PWDS_LEN) and the password itself.

If the PWD content is equal to the sent password, then the card will be locked and the card-locked status bit will be set in the status register. If the password is not correct, then the LOCK_UNLOCK_FAILED error bit will be set in the status register.
Note that it is possible to set the password and to lock the card in the same sequence. In such a case, the host shall perform all the required steps for setting the password (as described above) including the bit LOCK set while the new password command is sent.
If the password was previously set (PWD_LEN is not 0), then the card will be locked automatically after

power on reset.
An attempt to lock a locked card or to lock a card that does not have a password will fail and the LOCK_UNLOCK_FAILED error bit will be set in the status register, unless it was done during a password definition or change operations.

- **Unlocking the Card:**
  - Select a card (CMD7), if not previously selected.
  - Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.
  - Send the card lock/unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode UNLOCK, the length (PWDS_LEN) and the password itself.

If the PWD content is equal to the sent password, then the card will be unlocked and the card-locked status bit will be cleared in the status register. If the password is not correct, then the LOCK_UNLOCK_FAILED error bit will be set in the status register.
Note that unlocking is done only for the current power session. As long as the PWD is not cleared, the card will be locked automatically on the next power up. The only way to unlock the card is by clearing the password.
An attempt to unlock an unlocked card will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register, unless it was done during a password definition or change operation.

4.3.7.2 Parameter and the Result of CMD42

The block length shall be greater than or equal to the required data structure of CMD42; otherwise, the result of CMD42 is undefined and the card may be in the unexpected locked state. Table 4-7 clarifies the behavior of CMD42. The reserved bits in the parameter (bit7-4) of CMD42 shall be don't care. In the case that CMD42 requires the password, it is assumed that the old password and the new password are set correctly; otherwise the card indicates an error regardless of Table 4-7. If the password length is 0 or greater than 128 bits, the card indicates an error. If errors occur during execution of CMD42, the LOCK_UNLOCK_FAILED (Bit24 of Card Status) shall be set to 1 regardless of Table 4-7. The CARD_IS_LOCKED (Bit25 of Card Status) in the response of CMD42 shall be the same as Current Card State in Table 4-7. In the field of Card Status, 0 to 1 means the card changes to Locked and 1 to 0 means the card changes to Unlocked after execution of CMD42. It can be seen in the response of CMD13 after the CMD42. The LOCK_UNLOCK_FAILED (Bit24 of Card Status) as the result of CMD42 can be seen in the response of either CMD42 or the following CMD13.

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CMD42 Parameter in the data
Bit3: ERASE
Bit2: LOCK_UNLOCK
Bit1: CLR_PWD
Bit0: SET_PWD

Related bits in the Card Status
Bit25: CARD_IS_LOCKED
Bit24: LOCK_UNLOCK_FAILED

CMD42 Parameter				Current Card State	PWD_LEN and PWD	Result of the Function	Card Status	
Bit3	Bit2	Bit1	Bit0				Bit25	Bit24
After Power On					Exist	The card is locked	1	0
					Cleared	The card is unlocked	0	0
1	0	0	0	Locked	Exist	Force Erase (Refer to Table 4-8)	Table 4-8	
1	0	0	0	Unlocked	Exist	Error	0	1
1	0	0	0	Unlocked	Cleared	Error	0	1
0	1	0	0	Locked	Exist	Error	1	1
0	1	0	0	Unlocked	Exist	Lock the card	0 to 1	0
0	1	0	0	Unlocked	Cleared	Error	0	1
0	1	0	1	Locked	Exist	Replace password and the card is still locked	1	0
0	1	0	1	Unlocked	Exist	Replace password and the card is locked	0 to 1	0
0	1	0	1	Unlocked	Cleared	Set Password and lock the card	0 to 1	0
0	0	1	0	Locked	Exist	Clear PWD_LEN and PWD and the card is unlocked	1 to 0	0
0	0	1	0	Unlocked	Exist	Clear PWD_LEN and PWD	0	0
0	0	1	0	Unlocked	Cleared	Error (Note *4 Refer to Table 4-10)	0	1
0	0	0	1	Locked	Exist	Replace password and the card is unlocked	1 to 0	0
0	0	0	1	Unlocked	Exist	Replace password and the card is unlocked	0	0
0	0	0	1	Unlocked	Cleared	Set password and the card is still unlocked	0	0
0	0	0	0	Locked	Exist	Unlock the card	1 to 0	0
0	0	0	0	Unlocked	Exist	Error	0	1
0	0	0	0	Unlocked	Cleared	Error	0	1
Other combinations				Don't care	Don't care	Error (Note *1 Refer to Table 4-10)	0 or 1	1

Table 4-7: Lock Unlock Function (Basic Sequence for CMD42)

Application Note:
To replace password, the host should consider following cases. When PWD_LEN and password data exist, the card assumes old and new passwords are set in the data structure. When PWD_LEN and PWD are cleared, the card assumes only new password is set in the data structure. In this case, the host shall not set old password in the data structure; otherwise, unexpected password is set.

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4.3.7.3 Forcing Erase

In the case that the user forgot the password (the PWD content) it is possible to erase all the card data content along with the PWD content. This operation is called *Forced Erase*.

- Select a card (CMD7), if not previously selected already.
- Define the block length (CMD16) to 1 byte (8-bit card lock/unlock command). Send the card lock/unlock command with the appropriate data block of one byte on the data line including the 16 bit CRC. The data block shall indicate the mode ERASE (the ERASE bit shall be the only bit set).

If the ERASE bit is not the only bit set in the data field, the LOCK_UNLOCK_FAILED error bit will be set in the status register and the erase request is rejected. If the command was accepted, then ALL THE CARD CONTENT WILL BE ERASED including the PWD and PWD_LEN register content and the locked card will be unlocked. An attempt to force erase on an unlocked card will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register.

4.3.7.3.1 Force Erase Function to the Locked Card

Table 4-8 clarifies the relation between force erase and Write Protection. The force erase does not erase the secure area. The card shall keep its locked state during the erase execution and change to the unlocked state after the erase of all user area is completed. Similarly, the card shall keep Temporary and Group Write Protection during the erase execution and clear Write Protection after the erase of all user area is completed. In the case of an erase error occurs, the card can continue force erase if the data of error sectors are destroyed.

Write Protections
PWP: Permanent Write Protect (CSD Bit13)
TWP: Temporary Write Protect (CSD Bit12)
GWP: Group Write Protect (CMD28, CMD29, CMD30)

CMD42 Parameter				PWP	TWP GWP	Result of the Function	Card Status	
Bit3	Bit2	Bit1	Bit0				Bit25	Bit24
1	0	0	0	Yes	don't care	Error (Note *2 Refer to Table 4-10)	1	1
1	0	0	0	No	Yes	Execute force erase and clear Temporary Write Protect and Group Write Protect. (Note *3 Refer to Table 4-10)	1 to 0	0
1	0	0	0	No	No	Execute force erase.	1 to 0	0

Table 4-8: Force Erase Function to the Locked Card (Relation to the Write Protects)

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4.3.7.4 Relation Between ACMD6 and Lock/Unlock State

ACMD6 is rejected when the card is locked and bus width can be changed only when the card is unlocked. Table 4-9 shows the relation between ACMD6 and the Lock/Unlock state.

Card State	Bus Mode	Result of the Function
Unlocked	1-bit mode	ACMD6 is accepted
Locked	1-bit mode	ACMD6 is rejected and still in 1-bit mode
Unlocked	4-bit mode	ACMD6 is accepted
Locked	4-bit mode	ACMD6 is rejected and still in 4-bit mode. CMD0 change to 1-bit mode

Table 4-9: Relation between ACMD6 and the Lock/Unlock State

Application Note:
After power on (in 1-bit mode), if the card is locked, the SD mode host shall issue CMD42 in 1-bit mode. If the card is locked in 4-bit mode, the SD mode host shall issue CMD42 in 4-bit mode.

4.3.7.5 Commands Accepted for Locked Card

The locked card shall accept commands listed below and return response with setting CARD_IS_LOCKED.

1) Basic class (0)
2) Lock card class (7)
3) CMD16
4) ACMD41
5) ACMD42

All other commands including security commands are treated as illegal commands.
Note: CMD11 (Class 0) and CMD40 (Class 7) are new commands accepted in the locked card state. CMD40 is reserved for Security Specification.

Application Note:
After power on, the host can recognize the card lock/unlock state by the CARD_IS_LOCKED in the response of CMD7 or CMD13.

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4.3.7.6 Two Types of Lock/Unlock Card

There are two types of lock/unlock function-supported cards. The Type 1 is the earlier version of SD Memory Card and the Type 2 is defined in the Physical Layer Specification Version 1.10 and higher. Table 4-10 shows the difference between these types of cards. The SD memory cards that support Lock/Unlock and comply with Version 1.01, can take either Type 1 or Type 2. The SD Memory Cards that support Lock/Unlock and comply with Version 1.10 and higher, shall take Type 2.

Notes	Type 1 Card (Earlier Version)	Type 2 Card (New Version)
*1 in Table 4-7	Treat CMD42 Parameter=0011b as 0001b. Treat CMD42 Parameter=0111b as 0101b. Treat CMD42 Parameter=0110b as 0010b. Results of other combinations are Error.	All results are Error
*2 in Table 4-8	Execute force erase and set Permanent Write Protect. If force erase is completed, the CARD_IS_LOCKED is changed from 1 to 0. A priority is given to force erase from Permanent Write Protect.	The result is Error A priority is given to Permanent Write Protect from force erase.
*3 in Table 4-8	Execute force erase but Temporary Write Protect and Group Write Protect are not cleared. It should be cleared by the host.	Execute force erase and clear Temporary Write Protect and Group Write Protect.
*4 in Table 4-7	CMD42 Parameter=0010 and CMD42 Parameter=0110 The result is no error. Card status Bit24 will be 0	The result is Error. Card status Bit24 will be 1

Table 4-10: Version Difference of Lock/Unlock Functions

Application Note:
The host can use both types of cards without checking the difference by taking account of the following points.

(1) The host should not set the parameters of CMD42 that return an error listed in Table 4-7. (For *1)
(2) The host should not issue a force erase command if the Permanent Write Protect is set to 1, otherwise the Type 1 card can no longer be used even if the user remembers the password. (For *2)
(3) After the force erase, if the Temporary Write Protect is not cleared, the host should clear it. (For *3)

4.3.8 Content Protection

This section is a blank in the Simplified Specification.

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4.3.9 Application-Specific Commands

4.3.9.1 Application-Specific Command – APP_CMD (CMD55)

This command, when received by the card, causes the card to interpret the following command as an application-specific command, ACMD. The ACMD provides command extension, has the same structure as that of regular commands and it may have the same CMD number. The card recognizes it as ACMD by the fact that it appears after APP_CMD.
When an ACMD is not defined, the card treats it as regular command. If, as an example, a card has a definition for ACMD13 but not for ACMD7, then, command 13 after APP_CMD is interpreted as the non-regular CMD13 but command 7 after APP_CMD is interpreted as the regular CMD7. In order to use one of the ACMD's, the host should be:

(1) When sending APP_CMD, the response has the APP_CMD bit set signaling to the host that ACMD is now expected.
(2) ACMD55 does not exist. If multiple CMD55 are issued continuously, APP_CMD bit in each response is set to 1. The command issued immediately after the last CMD55 shall be interpreted as ACMD. When more than one command (except CMD55) is issued directly after CMD55, the first command is interpreted as ACMD and the following commands are interpreted as regular commands
(3) If a defined ACMD is send and it is legal, the response has the APP_CMD bit set, indicating that the accepted command is interpreted as ACMD.
(4) If an undefined ACMD is sent and it is legal, the response has the APP_CMD bit cleared, indicating that the accepted command is interpreted as normal CMD.
(5) If a defined or undefined ACMD is sent and it is illegal, then it is handled as an illegal command. Illegal Command Error is indicated in the next R1/R6 response and host should ignore APP_CMD status in the response. Next command is handled as normal command.

Host shall not use undefined ACMDs as regular commands even if the specification defines it.
The following ACMD numbers are reserved for the SD Memory Card proprietary applications and shall not be used by any SD Memory Card manufacturer:
ACMD6, ACMD13, ACMD17-26, ACMD38-49, ACMD51.

In above explanation, commands defined in the detailed command description section are "defined" commands but not defined in the section are "Undefined" commands (Section 4.7.4 or Section 7.3.1.3 depends on bus mode). "Legal" means that a defined or undefined command is accepted at the current state and "Illegal" means that a defined or undefined command is not accepted at the current state.

Exception in ACMD41

- The response of ACMD41 does not have APP_CMD status. Sending the response of CMD41 in idle state means the card is accepted as legal ACMD41.
- As APP_CMD status is defined as "clear by read", APP_CMD status, which is set by ACMD41, may be indicated in the response of next CMD11 or CMD3. However, as ACMD11 and ACMD3 are not defined, it is not necessary to set APP_CMD status.
- Host should ignore APP_CMD status in the response of CMD11 and CMD3.

4.3.9.2 General Command - GEN_CMD (CMD56)

This section is a blank in the Simplified Specification.

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4.3.10 Switch Function Command

4.3.10.1 General

Switch function command (CMD6) is used to switch or expand memory card functions. Currently four function groups are defined:

(1) Access Mode:
Selection of SD bus interface speed modes.
(2) Command System:
A specific function can be extended and controlled by a set of shared commands.
(3) Driver Strength
Selection of suitable output driver strength in UHS-I modes depends on host environment.
(4) Power Limit
Selection to limit the maximum power depends on host power supply capability and heat release capability. Current Limit is re-defined as Power Limit to account for the two power supply voltages on UHS II cards.

This was introduced in the Physical Layer Specification Version 1.10. Therefore, cards that are compatible with earlier versions of the spec do not support it. The host should check the "SD_SPEC" field in the SCR register to identify what version of the spec the card complies with before using CMD6. It is also possible to check support of CMD6 by bit10 of CCC in CSD. It is mandatory for an SD memory card of Version 1.10 and higher to support CMD6.

CMD6 is valid under the "Transfer State". Once selected, via the switch command, all functions only return to the default function after a power cycle, CMD6 (Mode 1 operation with Function 0 in each function group) or CMD0. Executing a power cycle or issuing CMD0 will cause the card to reset to the "idle" state and all the functions to switch back to the default function.

As a response to CMD6, the SD Memory Card will send R1 response on the CMD line and 512 bits of status on the DAT lines. From the SD bus transaction point of view, this is a standard single block read transaction and the time out value of this command is 100 ms, the same as in read command. If CRC error occurs on the status data, the host should issue a power cycle.
CMD6 function switching period is within 8 clocks after the end bit of status data. When CMD6 changes the bus behavior (i.e. access mode), the host is allowed to use the new functions (increase/decrease CLK frequency beyond the current max CLK frequency), at least 8 clocks after at the end of the switch command transaction (see Figure 4-14).

In response to CMD0, the switching period is within 8 clocks after the end bit of CMD0. When CMD6 has changed the bus behavior (i.e. access mode) the host is allowed to start the initialization process, at least 8 clocks after at the CMD0.

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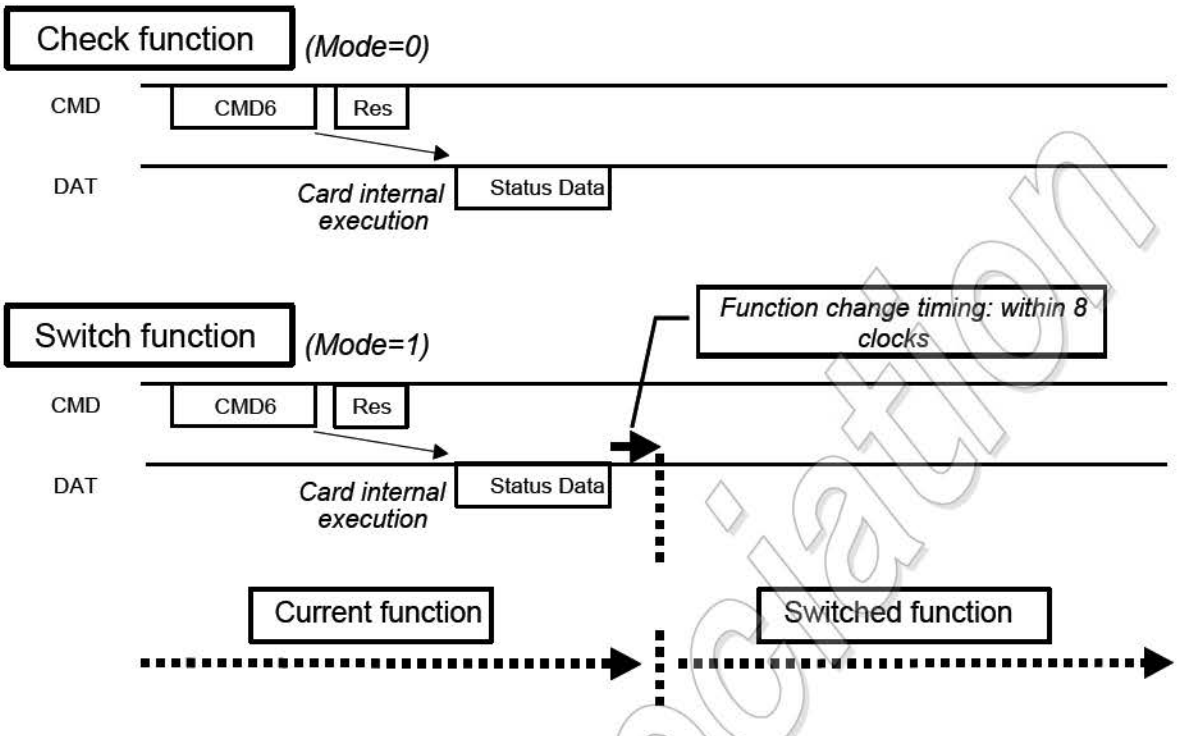


Figure 4-14: Use of Switch Command

CMD6 supports six function groups, and each function group supports sixteen branches (functions). Only one function can be chosen and active in a given function group. Function 0 in each function group is the default function (compatible with Spec. 1.01).

CMD6 can be used in two modes:

- Mode 0 (Check function) is used to query if the card supports a specific function or functions.
- Mode 1 (set function) is used to switch the functionality of the card.

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4.3.10.2 Mode 0 Operation - Check Function

CMD6 mode 0 is used to query which functions the card supports, and to identify the maximum current/power consumption of the card under the selected functions.
Refer to Table 4-31: Switch function commands (class 10) for the argument definition of CMD6.

A query is done by setting the argument field of the command, as follows:

- Set the Mode bit to 0
- Select only one function in each function group. Selection of default function is done by setting the function to 0x0. Select a specific function by using appropriate values from Table 4-11. Selecting 0xF will keep the current function that has been selected for the function group.
- When the function in query is ready, the card returns the inquired function number, if busy, the card returns the current function number (See Table 4-15).

In response to a query, the switch function will return the following 3 statuses (see Table 4-13):

- The functions that are supported by each of the function groups
- The function that the card will switch to in each of the function groups. This value is identical to the provided argument if the host made a valid selection or 0xF if the selected function was invalid.
- Maximum current/power consumption under the selected functions. If one of the selected functions was wrong, the return value will be 0.

4.3.10.3 Mode 1 Operation - Set Function

CMD6 mode 1 is used to switch the functionality of the card.

Switching to a new functionality is done by:

- Setting the Mode bit to 1
- Selecting only one function in each function group. Selection of default function is done by setting the function to 0x0. It is recommended to specify 0xF (no influence) for all selected functions, except for functions that need to be changed. Selecting 0xF will keep the current function for the function group.
- When a function cannot be switched because it is busy, the card returns the current function number (not returns 0xF), the other functions in the other groups may still be switched.

In response to a set function, the switch function will return the following 3 statuses:

- The functions that are supported by each of the function groups
- The function that is the result of the switch command. In case of invalid selection of one function or more, all set values are ignored and no change will be done (identical to the case where the host selects 0xF for all functions groups). The response to an invalid selection of function will be 0xF.
- Maximum current/power consumption under the selected functions. If one of the selected functions was wrong, the return value will be 0.

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Arg. Slice	[23:20]	[19:16]	[15:12]	[11:8]	[7:4]	[3:0]
Group No.	6	5	4	3	2	1
Function name	reserved	reserved	Power Limit*3	Driver Strength	Command system	Access mode*1
0x0	Default*2		Default*2 0.72W	Default*2 Type B	Default*2	Default*2 / SDR12
0x1	Reserved	Reserved	1.44W	Type A	For eC	High-Speed / SDR25
0x2	Reserved	Reserved	2.16W	Type C	Reserved	SDR50
0x3	Reserved	Reserved	2.88W	Type D	OTP	SDR104
0x4	Reserved	Reserved	1.80W	Reserved	ASSD	DDR50
0x5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x9	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0xA	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0xB	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0xC	Reserved	Reserved	Reserved	Reserved	(eSD)	Reserved
0xD	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0xE	Reserved	Reserved	Reserved	Reserved	Vendor specific	Reserved
0xF	No influence					

Note1: Bus Speed Mode is alias of Access Mode.
Note2: "Default" of Function 0 means that a function of just after the card initialized.
Note3: Notes for Power Limit
(1) Function 2 and 3 may be used only for embedded devices.
(2) Allowed power consumption for removable cards shall be up to 1.80W, even though the Power Limit is set to 2.16W or 2.88W.

Table 4-11: Available Functions of CMD6

Function Group 1 is defined as Bus Speed Mode switch. If the card is initialized in 3.3V signal level, Default Speed and High Speed are assigned to function 0 and 1. Then support bits of function 2 to 4 (SDR50, SDR104 and DDR50) are set to 0. If the card is initialized in 1.8V signal level, SDR and DDR modes are assigned from function 0 to function 4.

Function Group 2 is defined for Command System extension. CMD34-37, CMD50 and CMD57 are reserved for SD command system. OTP and ASSD are added. Refer to Part A1 Advanced Security Extension (McEX), Part 1 OTP Addendum and Part A3 ASSD Core Specification for more detail.

Function Group 3 is defined as driver strength selection for UHS-I modes. This switch is effective in 1.8V signaling mode.

Function Group 4 is defined as Power Limit switch for total card power consumable. This field is set

according to host power supply capability.
For SDIO Combo Cards, refer to SDIO specification to set the total card power consumable.

The Power Limit is defined in accordance with the Mechanical Addenda that define thermal requirements as a function of total card power consumption.

This Function Group is used for any bus mode including UHS-I and UHS-II modes. The default value of the Power Limit is 0.72W (minimum setting). In Legacy SD and UHS-I cards that have only VDD1 and not VDD2, this translates to 200mA at 3.6V.
In UHS-I mode, after selecting one of SDR50, SDR104 or DDR50 mode by Function Group 1, host needs to change the Power Limit to enable the card to operate in higher performance. In UHS-II mode, the host needs to change the Power Limit after finishing initialization to enable the card to operate in higher performance. Total card power is the sum of VDD1 and VDD2 power consumption.

In the other cases which may consume power by some function operations, such functions should have a function enable method (it will be defined in each Function Specification). After setting Power Limit, functions should be enabled by the function initialization. In case a function is not provided with enough power, it will fail initialization and the function is disabled by the card. If a function does not have a function enable method, the function shall work in 0.72W.
Power restriction described in Table 3-6, Table 3-9.

Function 0-F	F0	F1	F2	F3	F4	F5-FE	FF
Non UHS Mode	1	X	X	X	X	0 0	1
UHS Mode	1	1	1	1	1	0 0	1

Note 1: Same values are assigned to all X's: either 0 or 1.
Note 2: For Card compliant to Ver3.0x, all X are equal to 0 in Non UHS Mode and the support bit for F4 is set to 0 in UHS Mode.

For example, in UHS-I card, when the maximum power of a card is 1.08W (300mA at 3.6V on VDD1), the card operates at up to 0.72W (200mA at 3.6V on VDD1) when the Current Limit is set to 0.72W and up to 1.08W when Power Limit is set to 1.44W, 1.80W (and when Function 3 is selected).

Function Group 4 Power Limit	Max. Allowed Power (VDD1 and VDD2)	Max. Current of VDD1	Max. Current of VDD2
Function 0	0.72W	200mA	200mA
Function 1	1.44W	400mA	200mA
Function 2	2.16W	600mA	Note 6
Function 3	2.88W	800mA	Note 6
Function 4	1.80W	400mA	200mA

Note 1: Max. Allowed Power is defined as total of VDD1 and VDD2 power per card at the maximum voltage: 3.6V for VDD1 and 1.95V for VDD2.
Note 2: UHS-I Card is up to 1.44W even if one of Function 2, 3 or 4 is selected. 1.80W is defined for UHS-II mode.
Note 3: Function 2 and 3 cannot be used in UHS-II mode.
Note 4: UHS Host should support power supply capability of 400mA for VDD1 and 200mA for VDD2. VDD1 only Host should set to Function 0 or 1.
Note 5: Host needs to support VDD2 to use UHS-II or NFC supported cards.
Note 6: Max. Current of VDD2 for embedded device will be provided by device vendor.

Table 4-12 : Power Limit and Current Limit of VDD1 and VDD2

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Application Notes:
Default setting is 0.72W. In this mode, UHS-I and UHS-II card may not provide the maximum performance. The Speed Grade performance is defined at 1.44W mode. The maximum performance of the card is available when setting of this field covers the maximum current (power) of the card that can be read by CMD6 mode 0.
Host determines setting of this field by the host power supply capability to the card, heat release capability of host and the maximum current of a connector. Refer to the Mechanical Addenda for more details.

The followings are requirements in UHS-II mode,

(1) Function Group 1 and 3 are not used.
(2) Support of Function Group 2 is optional.
(3) Support of Function Group 4 is mandatory.

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4.3.10.4 Switch Function Status

The switch function status is the returned data block that contains function and current consumption information. The block length is predefined to 512 bits and the use of SET_BLK_LEN command is not necessary. Table 4-13 describes the status data structure.

The status bits of the response contain the information of the function group. Maximum current consumption will be used only for the new function added through this command. In this case, VDD_R_CURR_MIN, VDD_W_CURR_MIN, VDD_R_CURR_MAX and VDD_W_CURR_MAX values in the CSD register provides the current consumption when all card functions are set to the default state and can be used by spec 1.01 compatible hosts.

<table>
<tr><th>Bits</th><th>Description</th><th>Width</th></tr>
<tr><td>511:496</td><td>Maximum Current/Power Consumption
This field indicates total current/power consumption of the card including enabled functions selected by the Function Selection ([399:376] bits) dependent on selected Bus Speed Mode.
The host should check the maximum current consumption by mode 0 operation and verify that it can supply the necessary current/power before executing mode 1 operation.
Especially in UHS-I or UHS-II mode, this field is related to Current Limit / Power Limit setting. CMD6 mode 0 indicates the maximum current/power of a selected bus speed mode regardless of the setting of Current Limit / Power Limit. CMD6 mode 1 indicates the maximum current/power of a selected bus speed mode depending on the setting of Current Limit.

Definition for SD I/F Mode
<table>
<tr><th>Value</th><th>Maximum Current(Power) Consumption at 3.6V</th></tr>
<tr><td>0</td><td>Error</td></tr>
<tr><td>1</td><td>1mA (3.6mW)</td></tr>
<tr><td>2</td><td>2mA (7.2mW)</td></tr>
<tr><td>3</td><td>3mA (10.8mW)</td></tr>
<tr><td>.....</td><td>.....</td></tr>
<tr><td>65,535</td><td>65,535mA (235926mW)</td></tr>
</table>
The voltage to calculate current consumption is defined at 3.6V.
Maximum current consumption is average over 1second.

Definition for UHS-II Mode
For UHS-II Card, this field is defined as Maximum Power Consumption. Total maximum power consumption of V_{DD1} and V_{DD2} is indicated. The definition of Power Consumption in this field is equivalent to Current Consumption at 3.6V. Refer to Current Limit / Power Limit in Section 4.3.10.3 about the relation between power and current of VDD1 and VDD2.
<table>
<tr><th>Value</th><th>Maximum Power Consumption</th></tr>
<tr><td>0</td><td>Error</td></tr>
<tr><td>1</td><td>3.6mW (= 1mA x 3.6V)</td></tr>
<tr><td>2</td><td>7.2mW (= 2mA x 3.6V)</td></tr>
<tr><td>3</td><td>10.8mW (= 3mA x 3.6V)</td></tr>
<tr><td>.....</td><td>.....</td></tr>
<tr><td>65,535</td><td>235926mW</td></tr>
</table>
</td><td>16</td></tr>
</table>

SD Association

Bits	Description	Width
495:480	**Support Bits of Functions in Function Group 6** Each bit corresponds to a function. Function 15 and 0 are always enabled. If a bit 480+i is set, function i is supported (i = Function 15 to 0)	16
479:464	**Support Bits of Functions in Function Group 5** Each bit corresponds to a function. Function 15 and 0 are always enabled. If a bit 464+i is set, function i is supported (i = Function 15 to 0)	16
463:448	**Support Bits of Functions in Function Group 4** Each bit corresponds to a function. Function 15 and 0 are always enabled. If a bit 448+i is set, function i is supported (i = Function 15 to 0)	16
447:432	**Support Bits of Functions in Function Group 3** Each bit corresponds to a function. Function 15 and 0 are always enabled. If a bit 432+i is set, function i is supported (i = Function 15 to 0)	16
431:416	**Support Bits of Functions in Function Group 2** Each bit corresponds to a function. Function 15 and 0 are always enabled. If a bit 416+i is set, function i is supported (i = Function 15 to 0)	16
415:400	**Support Bits of Functions in Function Group 1** Each bit corresponds to a function. Function 15 and 0 are always enabled. If a bit 400+i is set, function i is supported (i = Function 15 to 0)	16
399:396	**Function Selection of Function Group 6** mode 0 - The function which can be switched in function group 6. mode 1 - The function which is result of the switch command, in function group 6. 0xF shows function set error with the argument.	4
395:392	**Function Selection of Function Group 5** mode 0 - The function which can be switched in function group 5. mode 1 - The function which is result of the switch command, in function group 5. 0xF shows function set error with the argument.	4
391:388	**Function Selection of Function Group 4** mode 0 - The function which can be switched in function group 4. mode 1 - The function which is result of the switch command, in function group 4. 0xF shows function set error with the argument.	4
387:384	**Function Selection of Function Group 3** mode 0 - The function which can be switched in function group 3. mode 1 - The function which is result of the switch command, in function group 3. 0xF shows function set error with the argument.	4
383:380	**Function Selection of Function Group 2** mode 0 - The function which can be switched in function group 2. mode 1 - The function which is result of the switch command, in function group 2. 0xF shows function set error with the argument.	4
379:376	**Function Selection of Function Group 1** mode 0 - The function which can be switched in function group 1. mode 1 - The function which is result of the switch command, in function group 1. 0xF shows function set error with the argument.	4
375:368	**Data Structure Version** 00h – bits 511:376 are defined 01h – bits 511:272 are defined 02h-FFh – reserved	8
367:352	**Reserved for Busy Status of functions in group 6** If bit [i] is set, function [i] is busy. This field can be read in mode 0 and mode 1	16
351:336	**Reserved for Busy Status of functions in group 5** If bit [i] is set, function [i] is busy. This field can be read in mode 0 and mode 1	16

SD Association

Bits	Description	Width
335:320	**Reserved for Busy Status of functions in group 4** If bit [i] is set, function [i] is busy. This field can be read in mode 0 and mode 1	16
319:304	**Reserved for Busy Status of functions in group 3** If bit [i] is set, function [i] is busy. This field can be read in mode 0 and mode 1	16
303:288	**Busy Status of functions in group 2** If bit [i] is set, function [i] is busy. This field can be read in mode 0 and mode 1	16
287:272	**Reserved for Busy Status of functions in group 1** If bit [i] is set, function [i] is busy. This field can be read in mode 0 and mode 1	16
271:0	Reserved (All '0')	272

Table 4-13: Status Data Structure

4.3.10.4.1 Busy Status Indication for Functions

Each bit [367-272] shows the busy status of corresponding functions; 0 indicates ready and 1 indicates busy. While the status is busy, the host should not change the corresponding function. Switch command mode 1 can be applied only to ready functions.

If the function failed to be switched in mode 1 operation and returns the current function number in the response, the function is considered busy. The mode 1 operation may affect the behavior of a function. The mode 0 operations should be used to check the busy status of a function because it does not affect its behavior, especially, for function group 2 as defined below.

Function Group 2															
303	302	301	300	299	298	297	296	295	294	293	292	291	290	289	288
0	VS	0	0	0	0	0	0	0	0	0	ASSD	0	0	eC	0

Note: 0: Ready 1: Busy

Figure 4-15: Busy Status of 'Command System'

4.3.10.4.2 Data Structure Version

Data Structure Version indicates effective bit fields of the Switch Function Status. The cards can set either 00h or 01h. When this field is set to 01, busy status indication is effective.

Data Structure Version	Fields of Status Data Structure
00h	511:376 are defined
01h	511:272 are defined
02h-FFh	Reserved

Table 4-14: Data Structure Version

4.3.10.4.3 Function Table of Switch Command

Table 4-15, Table 4-16 and Table 4-17 shows possible combinations of the function switch.

"Argument" indicates 4-bit code specified in the argument of switch command (bits 23-0). **"Busy Status"** indicates the function is busy as defined below.

"Status Code" indicates 4-bit code in the Status Data Structure, bits 399-376.

SD Association

Argument	Busy Status	Status Code	Comment
0	Don't Care	0	Status indicates a default function, which is always supported.
Supported function	Ready	=Arg.	Status indicates that the function specified in the argument is supported and can be switched.
	Busy	Current Selected	Status indicates that the function specified in the argument is supported but cannot be switched because the function is busy.
Not Supported function	Don't Care	Fh	Status indicates that the function specified in the argument is not supported.
Fh	Don't Care	Current Selected	Status indicates current selected function

Table 4-15: Status Code of Mode 0 to Supported Function Group

Argument	Busy Status	Status Code	Comment
0	Don't Care	0	Default function can always be switched.
Supported function	Ready	=Arg.	Status indicates the same function number as specified in the argument, which means successful function change.
	Busy	Current Selected	Switch function is canceled and status indicates current selected function.
Not Supported function	Don't Care	Fh	If one of the function groups indicates an error code (Fh), switch requests to all switch functions are canceled and the rest of the data in the Status Data Structure should be ignored.
Fh	Don't Care	Current Selected	Status indicates current selected function

Table 4-16: Status Code of Mode 1 to Supported Function Group

Argument	Busy Status	Status Code	Comment
0	Don't Care	0	Status always indicates 0.
Eh-1h	Don't Care	Fh	Status always indicates Fh.
Fh	Don't Care	0	Status always indicates 0.

Table 4-17: Status Code of Mode 0 and 1 to Unsupported Function Group

SD Association

4.3.10.5 Relationship between CMD6 Data and Other Commands

This section is a blank in the Simplified Specification.

4.3.10.6 Switch Function Flow Example

This section is a blank in the Simplified Specification.

4.3.10.7 Example of Checking

This section is a blank in the Simplified Specification.

4.3.10.8 Example of Switching

This section is a blank in the Simplified Specification.

SD Association

4.3.11 High-Speed Mode (25 MB/sec interface speed)

Although the Rev 1.01 SD memory card supports up to 12.5 MB/sec interface speed, the speed of 25 MB/sec is necessary to support increasing performance needs of the host and because memory size continues to grow.

To achieve the 25 MB/sec interface speed, the clock rate is increased to 50 MHz and CLK/CMD/DAT signal timing and circuit conditions are reconsidered and changed from the Physical Layer Specification Version 1.01.

After power up, the SD memory card is in the default speed mode, and by using Switch Function command (CMD6), the Version 1.10 and higher SD memory card can be placed in High-Speed mode. The High-Speed function is a function in the access mode group (see Table 4-11). Supporting High-Speed mode is optional.

Because it is not possible to control two cards or more in the case that each of them has a different timing mode (Default and High-Speed mode) and in order to satisfy severe timing, the host shall drive only one card. CLK/CMD/DAT signal shall be connected in 1-to-1 between the host and the card.

4.3.12 Command System

SD commands CMD34-37, CMD50, and CMD57 are reserved for SD command system expansion via the switch command. Switching between the various functions of the command system function group, will change the interpretation and associated bus transaction (i.e. command without data transfer, single block read, multiple block write, etc.) of these commands. Supporting Command system is optional

- When the "standard command set" (default function 0x0) is selected, these commands will not be recognized by the card and will be considered as illegal commands (as defined in the Physical Layer Specification Version 1.01)
- When the "vendor specific" (function 0xE) is selected, the behaviors of these commands are vendor specific. They are not defined by this standard and may change for different card vendors.
- When the "mobile e-commerce" (function 0x1) is selected, the behavior of these commands is governed by the SD Specifications Part A1: Mobile Commerce Extension Specification.

When either of these extensions is used, special care should be given to proper selection of the command set function; otherwise, the host command may be interpreted incorrectly.

All other commands of the SD memory card (not reserved for the switch commands) are always available and will be executed as defined in this document regardless of the currently selected commands set.

SD Association

4.3.13 Send Interface Condition Command (CMD8)

CMD8 (Send Interface Condition Command) is defined to initialize SD Memory Cards compliant to the Physical Layer Specification Version 2.00 or later. CMD8 is valid when the card is in Idle state. This command has two functions.

- Voltage check:
  Checks whether the card can operate on the host supply voltage.
- Enabling expansion of existing command and response:
  Reviving CMD8 enables to expand new functionality to some existing commands by redefining previously reserved bits. ACMD41 was expanded to support initialization of SDHC Card and the expansion is also applied to SDXC Card.

Table 4-18 shows the format of CMD8.

Bit position	47	46	[45:40]	[39:20]	[19:16]	[15:8]	[7:1]	0
Width (bits)	1	1	6	20	4	8	7	1
Value	'0'	'1'	'001000'	'00000h'	x	x	x	'1'
Description	Start bit	Transmission bit	Command index	Reserved bits	Voltage supplied (VHS)	Check pattern	CRC7	End bit

Voltage Supplied	Value Definition
0000b	Not Defined
0001b	2.7-3.6V
0010b	Reserved for Low Voltage Range
0100b	Reserved
1000b	Reserved
Others	Not Defined

Table 4-18: Format of CMD8

When the card is in Idle state, the host shall issue CMD8 before ACMD41. In the argument, 'voltage supplied' is set to the host supply voltage and 'check pattern' is set to any 8-bit pattern.
The card checks whether it can operate on the host's supply voltage. The card that accepted the supplied voltage returns R7 response. In the response, the card echoes back both the voltage range and check pattern set in the argument. If the card does not support the host supply voltage, it shall not return response and stays in Idle state.

A part of this section is not described.

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4.3.14 Command Functional Difference in Card Capacity Types

CCS in the response of ACMD41 determines card capacity types: CCS=0 is SDSC and CCS=1 is SDHC or SDXC.

Memory access commands include block read commands (CMD17, CMD18), block write commands (CMD24, CMD25), and block erase commands (CMD32, CMD33).

Following are the functional differences of memory access commands between SDSC and SDHC, SDXC:

- Command Argument
  SDHC and SDXC use the 32-bit argument of memory access commands as block address format. Block length is fixed to 512 bytes regardless CMD16,
  SDSC uses the 32-bit argument of memory access commands as byte address format. Block length is determined by CMD16,
  i.e.:
  (a) Argument 0001h is byte address 0001h in the SDSC and 0001h block in SDHC and SDXC
  (b) Argument 0200h is byte address 0200h in the SDSC and 0200h block in SDHC and SDXC
- Partial Access and Misalign Access
  SDHC and SDXC disable Partial access and Misalign access (crossing physical block boundary) as the block address is used. Access is only granted based on block addressing.
- Set Block Length
  SDHC and SDXC use 512-byte fixed block length for memory access commands regardless of the block length set by CMD16. The setting of the block length does not affect the memory access commands. CMD42 is not classified as a memory access command. The data block size shall be specified by CMD16 and the block length can be set up to 512 bytes. Setting block length larger than 512 bytes sets the BLOCK_LEN_ERROR error bit regardless of the card capacity.
- Write Protected Group
  SDHC and SDXC do not support write-protected groups. Issuing CMD28, CMD29 and CMD30 generates the ILLEGAL_COMMAND error.

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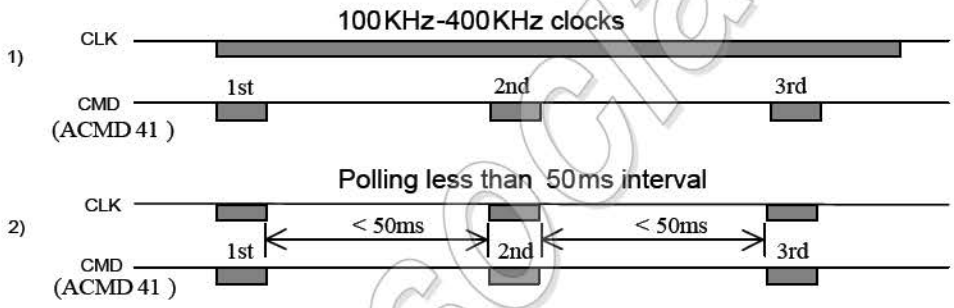
4.4 Clock Control

The SD Memory Card bus clock signal can be used by the host to change the cards to energy saving mode or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to lower the clock frequency or shut it down. For example, in the case that a host with 512 Bytes of data buffer would like to transfer data to a card with 1 KByte write blocks. So, to preserve a continuous data transfer, from the card's point of view, the clock to the card shall be stopped after the first 512 Bytes. Then the host will fill its internal buffer with another 512 Bytes. After the second half of the write block is ready in the host, it will continue the data transfer to the card by re-starting the clock supply. In such a way, the card does not recognize any interruptions in the data transfer.

There are a few restrictions the host shall consider:

- The bus frequency can be changed at any time (under the restrictions of maximum data transfer frequency and the identification frequency defined by the specification document).
- An exemption to the above is ACMD41 (SD_APP_OP_COND). After issuing the command ACMD41, the following 1) or 2) procedures shall be done by the host until the card becomes ready.
  1) Issue continuous clock in the frequency range of 100 KHz-400 KHz.

If the host wants to stop the clock, poll busy bit by ACMD41 command at less than 50 ms intervals.



- It is an obvious requirement that the clock shall be running for the card to output data or response tokens. After the last SD Memory Card bus transaction, the host is required, to provide **8 (eight)** clock cycles for the card to complete the operation before shutting down the clock. Following is a list of the various bus transactions:
  - •A command with no response. 8 clocks after the host command end bit.
  - •A command with response. 8 clocks after the card response end bit.
  - •A read data transaction. 8 clocks after the end bit of the last data block.
  - •A write data transaction. 8 clocks after the CRC status token.
- The host is allowed to shut down the clock of a "busy" card. The card will complete the programming operation regardless of the host clock. However, the host shall provide a clock edge for the card to turn off its busy signal. Without a clock edge, the card (unless previously disconnected by a deselect command -CMD7) will force the DAT line down forever.

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4.5 Cyclic Redundancy Code (CRC)

The CRC is intended to protect SD Memory Card commands, responses, and data transfer against transmission errors on the SD Memory Card bus. One CRC is generated for every command and checked for every response on the CMD line. For data blocks, one CRC per transferred block is generated. The CRC is generated and checked as described in the following.

- **CRC7**

The CRC7 check is used for all commands, for all responses except type R3, and for the CSD and CID registers. The CRC7 is a 7-bit value and is computed as follows:

Generator polynomial: $G(x) = x^7 + x^3 + 1$.

$M(x) = (\text{first bit}) * x^n + (\text{second bit}) * x^{n-1} + ... + (\text{last bit}) * x^0$

$CRC[6...0] = \text{Remainder } [(M(x) * x^7)/G(x)]$

The first bit is the most left bit of the corresponding bit string (of the command, response, CID or CSD). The degree *n* of the polynomial is the number of CRC protected bits decreased by one. The number of bits to be protected is 40 for commands and responses (n = 39), and 120 for the CSD and CID (n = 119).

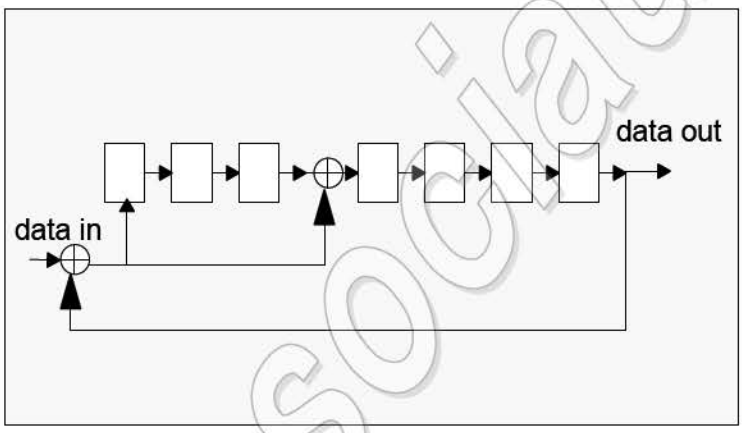


Figure 4-20: CRC7 Generator/Checker

- **CRC7 Examples**

The CRC section of the command/response is bolded.

CMD0 (Argument=0) --> 01 000000 00000000000000000000000000000000 "**1001010**" 1
CMD17 (Argument=0) --> 01 010001 00000000000000000000000000000000 "**0101010**" 1
Response of CMD17 --> 00 010001 00000000000000000000100100000000 "**0110011**" 1

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- **CRC16**

In the case of one DAT line usage, the CRC16 is used for payload protection in block transfer mode. The CRC check sum is a 16-bit value and is computed as follows:

Generator polynomial $G(x) = x^{16} + x^{12} + x^5 + 1$

$M(x) = (\text{first bit}) * x^n + (\text{second bit}) * x^{n-1} + \ldots + (\text{last bit}) * x^0$

$CRC[15...0] = \text{Remainder } [(M(x) * x^{16})/G(x)]$

The first bit is the first data bit of the corresponding block. The degree *n* of the polynomial denotes the number of bits of the data block decreased by one (e.g. n = 4095 for a block length of 512 bytes). The generator polynomial G(x) is a standard CCITT polynomial. The code has a minimal distance d=4 and is used for a payload length of up to 2048 Bytes (n <= 16383).

The same CRC16 method shall be used in single DAT line mode and in wide bus mode.

In wide bus mode, the CRC16 is done on each line separately.

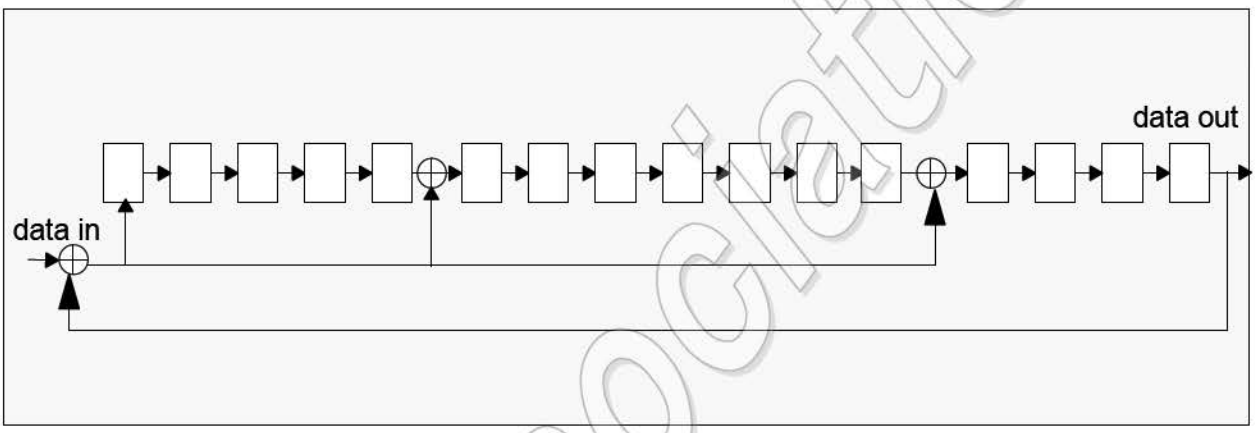


Figure 4-21: CRC16 Generator/Checker

- **CRC16 Example**

512 bytes with 0xFF data --> CRC16 = 0x7FA1

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4.6 Error Conditions

4.6.1 CRC and Illegal Command

All commands are protected by CRC (cyclic redundancy check) bits. If the addressed card's CRC check fails, the card does not respond and the command is not executed. The card does not change its state, and COM_CRC_ERROR bit is set in the status register.

Similarly, if an illegal command has been received, a card shall not change its state, shall not response and shall set the ILLEGAL_COMMAND error bit in the status register. Only the non-erroneous state branches are shown in the state diagrams (see Figure 4-1 and Figure 4-13).

Table 4-34 contains a complete state transition description.

There are different kinds of illegal commands:

- Commands that belong to classes not supported by the card (e.g. write commands in read only cards).
- Commands not allowed in the current state (e.g. CMD2 in Transfer State).
- Commands that are not defined (e.g. CMD5).

4.6.2 Read, Write and Erase Timeout Conditions

A card shall complete the command within the time period defined as follows or give up and return an error message. If the host does not get any response with the given timeout it should assume that the card is not going to respond and try to recover (e.g. reset the card, power cycle, reject, etc.).

4.6.2.1 Read

For a Standard Capacity SD Memory Card, the times after which a timeout condition for read operations occurs are (card independent) **either 100 times longer** than the typical access times for these operations given below **or 100 ms (the lower of the two)**. The read access time is defined as the sum of the two times given by the CSD parameters TAAC and NSAC (see Chapter 5.3). In the case of a single read operation, these card parameters define the typical delay between the end bit of the read command and the start bit of the data block. In the case of a multiple-read operation, they also define the typical delay between the end bit of a data block and the start bit of next data block.

A High Capacity SD Memory Card and Extended Capacity SD Memory Card indicate TAAC and NSAC as fixed values. The host should use 100 ms timeout (minimum) for single and multiple read operations rather than using TAAC and NSAC.

4.6.2.2 Write

For a Standard Capacity SD Memory Card, the times after which a timeout condition for write operations occurs are (card independent) **either 100 times longer** than the typical program times for these operations given below **or 250 ms (the lower of the two).** The R2W_FACTOR field in the CSD is used to calculate the typical block program time obtained by multiplying the read access time by this factor. It applies to all write commands (e.g. SET(CLR)_WRITE_PROTECT, PROGRAM_CSD and the block write commands). High Capacity SD Memory Card and Extended Capacity SD Memory Card indicate R2W_FACTOR as a fixed value.

In case of High Capacity SD Memory Card, maximum length of busy is defined as 250ms for all write operation.

While the card should try to maintain that busy indication of write operation does not exceed 250ms in the case of SDXC card, if the card is not possible to maintain operations with 250ms busy, the card can indicate write busy up to 500ms including single and multiple block write in the following scenarios:

a) The last busy in any write operation up to 500ms including single and multiple block write.
b) When multiple block write is stopped by CMD12, the busy from the response of CMD12 is up to 500ms.
c) When multiple block write is stopped by CMD23, the busy after the last data block is up to 500ms.

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d) Busy indication at block gap in multiple block write is up to 250ms except a following case. When the card executes consecutive two blocks write (2*512Bytes) and it spans across the physical block boundary, the busy after the each block can be indicated up to 500ms.

Especially regardless of the above definition, a speed class writing mode specified by CMD20 shall keep write busy up to 250ms in any case until the end of speed class write is indicated.

There are two types of busies in a multiple block write operation.
(1) Write busy at block gap (without CMD12) is maximum 250ms
(2) Write busy after CMD12 is maximum 250ms (500ms for SDXC)

If CMD12 is issued during a multiple block write operation's busy period, the host timeout counter is reset and the 250ms (500ms for SDXC) timeout period is measured from the response of CMD12.

In UHS-II mode, data is transferred by the unit of Data Burst. Data Burst consists of one or multiple data blocks and is determined depends on capability of host and card. Busy is not indicated after every block but indicated after every Data Burst. The maximum busy length after Data Burst is defined as 1 second. Refer to UHS-II Addendum about Data Burst for more details.

Application Notes:
The host should use a fixed timeout for write operations rather than using a timeout calculated from the R2W_FACTOR parameter.
It is strongly recommended for hosts to implement more than 500ms timeout value even if the card indicates the 250ms maximum busy length.
Even if the card supports Speed Class, any multiple block write operation may indicate a busy period of up to a maximum of 250ms. The sum of the busy periods over an AU is limited by Speed Class.
In UHS-II mode, refer to the UHS-II Addendum about host timeout setting.

4.6.2.3 Erase

If the card supports parameters for erase timeout calculation in the SD Status, the host should use them to determine erase timeout (see Chapter 4.10.2). If the card does not support these parameters, erase timeout can be estimated by block write delay.
The duration of an erase command can be estimated by the number of write blocks (WRITE_BL) to be erased multiplied by 250 ms.

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4.7 Commands

SD Commands applicable to UHS-II are defined in the UHS-II Addendum.

4.7.1 Command Types

There are four kinds of commands defined to control the SD Memory Card:

- Broadcast commands (bc), no response - The broadcast feature is only if all the CMD lines are connected together in the host. If they are separated, then each card will accept it separately in its turn.
- Broadcast commands with response (bcr)
  response from all cards simultaneously - Since there is no Open Drain mode in SD Memory Card, this type of command shall be used only if all the CMD lines are separated - the command will be accepted and responded by every card separately.
- Addressed (point-to-point) commands (ac)
  no data transfer on DAT
- Addressed (point-to-point) data transfer commands (adtc)
  data transfer on DAT

All commands and responses are sent over the CMD line of the SD Memory Card. The command transmission always starts with the left bit of the bit string corresponding to the command codeword.

4.7.2 Command Format

All commands have a fixed code length of 48 bits.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'1'	x	x	x	'1'
Description	Start bit	Transmission bit	Command index	Argument	CRC7	End bit

Table 4-20: Command Format

A command always starts with a start bit (always 0), followed by the bit indicating the direction of transmission (host = 1). The next 6 bits indicate the index of the command, this value being interpreted as a binary coded number (between 0 and 63). Some commands need an argument (e.g. an address), which is coded by 32 bits. A value denoted by 'x' in the table above indicates this variable is dependent on the command. All commands are protected by a CRC (see Chapter 4.5 for the definition of CRC7). Every command codeword is terminated by the end bit (always 1). All commands and their arguments are listed in Table 4-22 to Table 4-32.

4.7.3 Command Classes

The command set of the SD Memory Card system is divided into several classes (See Table 4-21). Each class supports a set of card functionalities.
Table 4-21 determines the setting of CCC from the card supported commands. A CCC bit, which corresponds to a supported command number, is set to 1. A class in CCC includes mandatory commands is always set to 1. Cards with specific functions may need to support some optional commands. For example, Combo Card shall support CMD5.

Class 0, 2, 4, 5 and 8 are mandatory and shall be supported by all SD Memory Cards. Class 7 except CMD40 is mandatory for SDHC and SDXC. The other classes are optional. The supported Card Command Classes (CCC) are coded as a parameter in the card specific data (CSD) register of each card, providing the host with information on how to access the card.
If different types of commands are assigned to a Command Class (Class 7, Class 8 and Class 11), which command supported can be determined by referring command support information in SCR register.

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Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	**class description**	**basic**	**reserved**	**block read**	**reserved**	**block write**	**erase**	**write protection**	**lock card**	**application specific**	**I/O mode**	**switch**	**extension**
CMD0	Mandatory	+											
CMD2	Mandatory	+											
CMD3	Mandatory	+											
CMD4	Mandatory	+											
CMD5	Optional										+		
CMD6[2]	Mandatory											+	
CMD7	Mandatory	+											
CMD8[3]	Mandatory	+											
CMD9	Mandatory	+											
CMD10	Mandatory	+											
CMD11[5]	Optional	+											
CMD12	Mandatory	+											
CMD13	Mandatory	+											
CMD15	Mandatory	+											
CMD16	Mandatory			+		+			+				
CMD17	Mandatory			+									
CMD18	Mandatory			+									
CMD19[5]	Optional			+									
CMD20[6]	Optional			+		+							
CMD21	Optional												+
CMD23[7]	Optional			+		+							
CMD24[1]	Mandatory					+							
CMD25[1]	Mandatory					+							
CMD27[1]	Mandatory					+							
CMD28	Optional							+					
CMD29	Optional							+					
CMD30	Optional							+					
CMD32[1]	Mandatory						+						
CMD33[1]	Mandatory						+						
CMD34-37[2]	Optional											+	
CMD38[1]	Mandatory						+						
CMD40	Optional								+				
CMD42[4]	(Note 4)								+				
CMD48	Optional												+
CMD49	Optional												+
CMD50[2]	Optional											+	

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Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	class description	basic	reserved	block read	reserved	block write	erase	write protection	lock card	application specific	I/O mode	switch	extension
CMD52	Optional										+		
CMD53	Optional										+		
CMD55	Mandatory									+			
CMD56	Mandatory									+			
CMD57[2]	Optional											+	
CMD58	Optional												+
CMD59	Optional												+
ACMD6	Mandatory									+			
ACMD13	Mandatory									+			
ACMD14	Optional									+			
ACMD15	Optional									+			
ACMD16	Optional									+			
ACMD22[1]	Mandatory									+			
ACMD23[1]	Mandatory									+			
ACMD28	Optional									+			
ACMD41	Mandatory									+			
ACMD42	Mandatory									+			
ACMD51	Mandatory									+			

Note (1): The commands related write and erase are mandatory only for the Writable types of Cards.
Note (2): This command was defined in version 1.10
Note (3): This command is newly defined in version 2.00
Note (4): This command is optional in Version 1.01 and 1.10 and mandatory from Version 2.00
Note (5): Mandatory for UHS-I supported Card
Note (6): Not supported by SDSC. Optional for SDHC and Mandatory for SDXC.
Note (7): Not supported by SDSC. Mandatory for UHS104 card.

Table 4-21: Card Command Classes (CCCs) in SD Mode

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4.7.4 Detailed Command Description

The following tables describe in detail all SD Memory Card bus commands. The responses R1-R3, R6 are defined in Chapter 4.9. The registers CID, CSD and DSR are described in Chapter 5. The card shall ignore stuff bits and reserved bits in an argument.

CMD INDEX	type	argument	resp	abbreviation	command description
CMD0	bc	[31:0] stuff bits	-	GO_IDLE_STATE	Resets all cards to idle state
CMD1	reserved				
CMD2	bcr	[31:0] stuff bits	R2	ALL_SEND_CID	Asks any card to send the CID numbers on the CMD line (any card that is connected to the host will respond)
CMD3	bcr	[31:0] stuff bits	R6	SEND_RELATIVE_ ADDR	Ask the card to publish a new relative address (RCA)
CMD4	bc	[31:16] DSR [15:0] stuff bits	-	SET_DSR	Programs the DSR of all cards
CMD5	reserved for I/O cards (refer to the "SDIO Card Specification")				
CMD7	ac	[31:16] RCA [15:0] stuff bits	R1b (only from the selecte d card)	SELECT/DESELECT_ CARD	Command toggles a card between the stand-by and transfer states or between the programming and disconnect states. In both cases, the card is selected by its own relative address and gets deselected by any other address; address 0 deselects all. In the case that the RCA equals 0, then the host may do one of the following: - Use other RCA number to perform card de-selection. - Re-send CMD3 to change its RCA number to other than 0 and then use CMD7 with RCA=0 for card de-selection.
CMD8	bcr	[31:12]reserved bits [11:8]supply voltage(VHS) [7:0]check pattern	R7	SEND_IF_COND	Sends SD Memory Card interface condition, which includes host supply voltage information and asks the card whether card supports voltage. Reserved bits shall be set to '0'.
CMD9	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CSD	Addressed card sends its card-specific data (CSD) on the CMD line.
CMD10	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CID	Addressed card sends its card identification (CID) on CMD the line.
CMD11	ac	[31:0] reserved bits (all 0)	R1	VOLTAGE_SWITCH	Switch to 1.8V bus signaling level.
CMD12	ac	[31:0] stuff bits	R1b	STOP_ TRANSMISSION	Forces the card to stop transmission
CMD13	ac	[31:16] RCA [15:0] stuff bits	R1	SEND_STATUS	Addressed card sends its status register.
CMD14	reserved				

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CMD INDEX	type	argument	resp	abbreviation	command description
CMD15	ac	[31:16] RCA [15:0] reserved bits	-	GO_INACTIVE_ STATE	Sends an addressed card into the *Inactive State*. This command is used when the host explicitly wants to deactivate a card. Reserved bits shall be set to '0'.

Table 4-22: Basic Commands (class 0)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	In the case of a Standard Capacity SD Memory Card, this command sets the block length (in bytes) for all following block commands (read, write, lock). Default block length is fixed to 512 Bytes. Set length is valid for memory access commands only if partial block read operation are allowed in CSD. In the case of SDHC and SDXC Cards, block length set by CMD16 command does not affect memory read and write commands. Always 512 Bytes fixed block length is used. This command is effective for LOCK_UNLOCK command. In both cases, if block length is set larger than 512Bytes, the card sets the BLOCK_LEN_ERROR bit. In DDR50 mode, data is sampled on both edges of the clock. Therefore, block length shall always be even.
CMD17	adtc	[31:0] data address[2]	R1	READ_SINGLE_ BLOCK	In the case of a Standard Capacity SD Memory Card, this command, this command reads a block of the size selected by the SET_BLOCKLEN command.[1] In case of SDHC and SDXC Cards, block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command.
CMD18	adtc	[31:0] data address[2]	R1	READ_MULTIPLE_ BLOCK	Continuously transfers data blocks from card to host until interrupted by a STOP_TRANSMISSION command. Block length is specified the same as READ_SINGLE_BLOCK command.
CMD19	adtc	[31:0] reserved bits (all 0)	R1	SEND_TUNING_ BLOCK	64 bytes tuning pattern is sent for SDR50 and SDR104.
CMD20	ac	[31:28]Speed Class Control [27:0]Reserved (all-0)	R1b	SPEED_CLASS_CON TROL	Speed Class control command. Refer to Section 4.13.2.8.

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CMD INDEX	type	argument	resp	abbreviation	command description
CMD22	reserved				
CMD23	ac	[31:0] Block Count	R1	SET_BLOCK_COUNT	Specify block count for CMD18 and CMD25.

1) The data transferred shall not cross a physical block boundary unless READ_BLK_MISALIGN is set in the CSD.
2) SDSC Card (CCS=0) uses byte unit address and SDHC and SDXC Cards (CCS=1) use block unit address (512 Bytes unit).

Table 4-23: Block-Oriented Read Commands (class 2)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	See description in Table 4-23
CMD20	ac	[31:28]Speed Class Control [27:0]Reserved (all-0)	R1b	SPEED_CLASS_CONTROL	Speed Class control command. Refer to Section 4.13.2.8.
CMD23	ac	[31:0] Block Count	R1	SET_BLOCK_COUNT	Specify block count for CMD18 and CMD25.
CMD24	adtc	[31:0] data address[2]	R1	WRITE_BLOCK	In case of SDSC Card, block length is set by the SET_BLOCKLEN command1. In case of SDHC and SDXC Cards, block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command.
CMD25	adtc	[31:0] data address[2]	R1	WRITE_MULTIPLE_BLOCK	Continuously writes blocks of data until a STOP_TRANSMISSION follows. Block length is specified the same as WRITE_BLOCK command.
CMD26	Reserved For Manufacturer				
CMD27	adtc	[31:0] stuff bits	R1	PROGRAM_CSD	Programming of the programmable bits of the CSD.

1) The data transferred shall not cross a physical block boundary unless WRITE_BLK_MISALIGN is set in the CSD. In the case that write partial blocks is not supported, then the block length=default block length (given in CSD).
2) SDSC Card (CCS=0) uses byte unit address and SDHC and SDXC Cards (CCS=1) use block unit address (512 bytes unit).

Table 4-24: Block-Oriented Write Commands (class 4)

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CMD INDEX	type	argument	resp	abbreviation	command description
CMD28	ac	[31:0] data address[2]	R1b	SET_WRITE_PROT	If the card has write protection features, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE). SDHC and SDXC Cards do not support this command.
CMD29	ac	[31:0] data address[2]	R1b	CLR_WRITE_PROT	If the card provides write protection features, this command clears the write protection bit of the addressed group. SDHC and SDXC Cards do not support this command.
CMD30	adtc	[31:0] write protect data address[2]	R1	SEND_WRITE_ PROT	If the card provides write protection features, this command asks the card to send the status of the write protection bits.[1] SDHC and SDXC Cards do not support this command.
CMD31	reserved				

1) 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data line. The last (least significant) bit of the protection bits corresponds to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding write protection bits shall be set to 0.
2) Data address is in byte units in a Standard Capacity SD Memory Card.

Table 4-25: Block Oriented Write Protection Commands (class 6)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD32	ac	[31:0] data address[1]	R1	ERASE_WR_BLK_ START	Sets the address of the first write block to be erased.
CMD33	ac	[31:0] data address[1]	R1	ERASE_WR_BLK_END	Sets the address of the last write block of the continuous range to be erased.
CMD38	ac	[31:0] stuff bits	R1b	ERASE	Erases all previously selected write blocks.
CMD39	reserved				
CMD41	reserved				

1) SDSC Card (CCS=0) uses byte unit address and SDHC and SDXC Cards (CCS=1) use block unit address (512 bytes unit).
2) CMD40 is moved to Table 4-27 (Class 7).

Table 4-26: Erase Commands (class 5)

CMD INDEX	type	argument	resp	abbreviation	command description

CMD INDEX	type	argument	resp	abbreviation	command description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	See description in Table 4-23
CMD40	adtc	Defined by DPS Spec.	R1	Defined by DPS Spec.	Single block read type. Available even if card is locked.
CMD42	adtc	[31:0] Reserved bits (Set all 0)	R1	LOCK_UNLOCK	Used to set/reset the password or lock/unlock the card. The size of the data block is set by the SET_BLOCK_LEN command. Reserved bits in the argument and in Lock Card Data Structure shall be set to 0.
CMD43-47 CMD51	reserved				

Table 4-27: Lock Card (class 7)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD55	ac	[31:16] RCA [15:0] stuff bits	R1	APP_CMD	Indicates to the card that the next command is an application specific command rather than a standard command
CMD56	adtc	[31:1] stuff bits. [0]: RD/WR	R1	GEN_CMD	Used either to transfer a data block to the card or to get a data block from the card for general purpose/application specific commands. In case of a SDSC Card, block length is set by the SET_BLOCK_LEN command. In case of SDHC and SDXC Cards, block length is fixed to 512 bytes. The host sets RD/WR=1 for reading data from the card and sets to 0 for writing data to the card.
CMD60-63	reserved for manufacturer				

Table 4-28: Application-Specific Commands (class 8)

All the application-specific commands (given in Table 4-28) are supported if Class 8 is allowed (mandatory in SD Memory Card).

CMD INDEX	type	argument	resp	abbreviation	command description
CMD52-54	Commands for SDIO (refer to the "SDIO Card Specification")				

Table 4-29: I/O Mode Commands (class 9)

All future reserved commands shall have a codeword length of 48 bits, as well as their responses (if there are any).

The following table describes all the application-specific commands supported/reserved by the SD Memory Card. All the following ACMDs shall be preceded with APP_CMD command (CMD55).

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ACMD INDEX	type	argument	resp	abbreviation	command description
ACMD1-5	Reserved				
ACMD6	ac	[31:2] stuff bits [1:0]bus width	R1	SET_BUS_WIDTH	Defines the data bus width ('00'=1bit or '10'=4 bits bus) to be used for data transfer. The allowed data bus widths are given in SCR register.
ACMD7-12	Reserved				
ACMD13	adtc	[31:0] stuff bits	R1	SD_STATUS	Send the SD Status. The status fields are given in Table 4-43.
ACMD14-16	Reserved for DPS Specification				
ACMD17	Reserved				
ACMD18	Reserved for SD security applications[1]				
ACMD19-21	Reserved				
ACMD22	adtc	[31:0] stuff bits	R1	SEND_NUM_WR_ BLOCKS	Send the number of the written (without errors) write blocks. Responds with 32bit+CRC data block. If WRITE_BL_PARTIAL='0', the unit of ACMD22 is always 512 byte. If WRITE_BL_PARTIAL='1', the unit of ACMD22 is a block length which was used when the write command was executed.
ACMD23	ac	[31:23] stuff bits [22:0]Number of blocks	R1	SET_WR_BLK_ ERASE_COUNT	Set the number of write blocks to be pre-erased before writing (to be used for faster Multiple Block WR command). "1"=default (one wr block)[2].
ACMD24	Reserved				
ACMD25	Reserved for SD security applications[1]				
ACMD26	Reserved for SD security applications[1]				
ACMD27	Shall not use this command				
ACMD28	Reserved for DPS Specification				
ACMD29	Reserved				
ACMD30-35	Reserved for Security Specification				
ACMD36-37	Reserved				
ACMD38	Reserved for SD security applications[1]				
ACMD39-40	Reserved				

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ACMD INDEX	type	argument	resp	abbreviation	command description
ACMD41	bcr	[31]reserved bit [30]HCS(OCR[30]) [29]reserved for eSD [28]XPC [27:25]reserved bits [24]S18R [23:0] V_{DD} Voltage Window(OCR[23:0])	R3	SD_SEND_OP_COND	Sends host capacity support information (HCS) and asks the accessed card to send its operating condition register (OCR) content in the response on the CMD line. HCS is effective when card receives SEND_IF_COND command. Sends request to switch to 1.8V signaling (S18R). Reserved bit shall be set to '0'. CCS bit is assigned to OCR[30]. XPC controls the maximum power in the default speed mode of SDXC card. XPC=0 means 0.36W (100mA at 3.6V on VDD1) (max.) but speed class is not supported. XPC=1 means 0.54W (150mA at 3.6V on VDD1) (max.) and speed class is supported.
ACMD42	ac	[31:1] stuff bits [0]set_cd	R1	SET_CLR_CARD_DETECT	Connect[1]/Disconnect[0] the 50 KOhm pull-up resistor on CD/DAT3 (pin 1) of the card.
ACMD43-49	--	--	--	--	Reserved for SD security applications[1]
ACMD51	adtc	[31:0] stuff bits	R1	SEND_SCR	Reads the SD Configuration Register (SCR).
ACMD52-54	Reserved for Security Specification				
ACMD55	Not exist				Equivalent to CMD55. Refer to Section 4.3.9.1.
ACMD56-59	Reserved for Security Specification				

1) Refer to the "Part3 Security Specification" for a detailed explanation about the SD Security Features
2) Command STOP_TRAN (CMD12) shall be used to stop the transmission in Write Multiple Block whether or not the pre-erase (ACMD23) feature is used.

Table 4-30: Application Specific Commands used/reserved by SD Memory Card

Table 4-31 was added in version 1.10.

CMD INDEX	type	argument	resp	abbreviation	command description
CMD6	adtc	[31] Mode 0:Check function 1:Switch function [30:24] reserved (All '0') [23:20] reserved for function group 6 (0h or Fh) [19:16] reserved for function group 5 (0h or Fh) [15:12] function group 4 for Power Limit [11:8] function group 3 for Drive Strength [7:4] function group 2 for Command System [3:0] function group 1 for Access Mode	R1	SWITCH_FUNC	Checks switch-able function (mode 0) and switch card function (mode 1). See Chapter 4.3.10.
CMD34 CMD35	Reserved for each command system set by switch function command (CMD6). Detailed definition is referred to each command system specification.				

CMD INDEX	type	argument	resp	abbreviation	command description
CMD36					
CMD37					
CMD50					
CMD57					

Table 4-31: Switch Function Commands (class 10)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD21	Reserved for DPS Specification				
CMD48	adtc	[31]MIO 0:Memory, 1:I/O [30:27] FNO [26] Reserved (=0) [25:9] ADDR [8:0] LEN	R1	READ_EXTR_SINGLE	Single block read type. Refer to Section 5.7.2.1.
CMD49	adtc	[31]MIO 0:Memory, 1:I/O [30:27] FNO [26] MW [25:9] ADDR [8:0] LEN/MASK	R1	WRITE_EXTR_SINGLE	Single block write type. Refer to Section 5.7.2.2.
CMD58	adtc	[31]MIO 0:Memory, 1:I/O [30:27] FNO [26] BUS 0:512B, 1:32KB [25:9] ADDR [8:0] BUC	R1	READ_EXTR_MULTI	Multi-block read type. Refer to Section 5.7.2.4.
CMD59	adtc	[31]MIO 0:Memory, 1:I/O [30:27] FNO [26] BUS 0:512B, 1:32KB [25:9] ADDR [8:0] BUC	R1	WRITE_EXTR_MULTI	Multi-block write type. Refer to Section 5.7.2.5.

Note: CCC bit 11 is set to 1 when any command of class 11 is supported. Supporting of these commands is indicated in SCR register.

Table 4-32: Function Extension Commands (class 11)

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4.7.5 Difference of SD Commands Definition in UHS-II

Table 4-33 shows the difference of SD commands definition when the card is in UHS-II mode.
SD-TRAN driver of host should manage the difference of SD commands functions. Not supported commands should not issue to UHS-II card. CMD13 shall not be issued during data transfer. Normally, data transfer should be stopped by setting TLEN instead of using CMD12. CMD23 and CMD55 functions are included in UHS-II packet functions.

Command	Description
CMD0	Terminate SD transaction and reset SD-TRAN state.
CMD3	Returns Device ID in the response instead of RCA
CMD4	Illegal
CMD6	Function Group 1 and 3 are not used.
CMD7	Device ID is set to the argument instead of RCA
CMD13	Device operation is up to implementation during data transfer (e.g. CTS).
CMD11	Illegal
CMD12	Normally, TLEN (data length) in UHS-II packet is used to stop data transfer. CMD12 should be used to abort an operation when illegal situation occurs.
CMD15	Illegal
CMD19	Illegal
CMD23	Not Affected. TLEN in UHS-II packet is used to specify data length.
CMD55	Not Affected. ACMD is set by APP field in UHS-II packet.
ACMD6	Illegal
ACMD42	Illegal

(1) Not Affected means that the command is not executed in any card state, and response is returned (response type is up to implementation).
(2) Illegal means that card returns response with NACK=1.
(3) As SDHC/SDXC Cards do not support CMD28, 29 and 30, these commands are also illegal in UHS-II mode.

Table 4-33 : Difference of SD Commands Definition in UHS-II

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4.8 Card State Transition Table

Table 4-34 defines the card state transitions depend on the received command. State name in the table is the next state after the command is executed. "-" indicated that the command is treated as illegal command. In addition, whether a command is executable depends on command class (CCC).

	Current State									
	idle	**ready**	**ident**	**stby**	**tran**	**data**	**rcv**	**prg**	**dis**	**ina**
"Operation Complete"	-	-	-	-	-	tran	-	tran	stby	-
class 0										
CMD0	idle	idle	idle	idle	idle	idle	idle	idle	idle	-
CMD2	-	ident	-	-	-	-	-	-	-	-
CMD3	-	-	stby	stby	-	-	-	-	-	-
CMD4	-	-	-	stby	-	-	-	-	-	-
CMD7, card is addressed	-	-	-	tran	-	-	-	-	prg	-
CMD7, card is not addressed	-	-	-	stby	stby	stby	-	dis	-	-
CMD8	idle	-	-	-	-	-	-	-	-	-
CMD9	-	-	-	stby	-	-	-	-	-	-
CMD10	-	-	-	stby	-	-	-	-	-	-
CMD11	-	ready	-	-	-	-	-	-	-	-
CMD12	-	-	-	-	-	tran	prg	-	-	-
CMD13	-	-	-	stby	tran	data	rcv	prg	dis	-
CMD15	-	-	-	ina	ina	ina	ina	ina	ina	-
class 2										
CMD16	-	-	-	-	tran	-	-	-	-	-
CMD17	-	-	-	-	data	-	-	-	-	-
CMD18	-	-	-	-	data	-	-	-	-	-
CMD19	-	-	-	-	data	-	-	-	-	-
CMD20	-	-	-	-	prg	-	-	-	-	-
CMD23	-	-	-	-	tran	-	-	-	-	-
class 4										
CMD16	-	-	-	-	tran	-	-	-	-	-
CMD20	-	-	-	-	prg	-	-	-	-	-
CMD23	-	-	-	-	tran	-	-	-	-	-
CMD24	-	-	-	-	rcv	-	-	-	-	-
CMD25	-	-	-	-	rcv	-	-	-	-	-
CMD27	-	-	-	-	rcv	-	-	-	-	-
class 6										
CMD28	-	-	-	-	prg	-	-	-	-	-
CMD29	-	-	-	-	prg	-	-	-	-	-
CMD30	-	-	-	-	data	-	-	-	-	-
class 5										
CMD32	-	-	-	-	tran	-	-	-	-	-
CMD33	-	-	-	-	tran	-	-	-	-	-
CMD38	-	-	-	-	prg	-	-	-	-	-

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	Current State									
	idle	**ready**	**ident**	**stby**	**tran**	**data**	**rcv**	**prg**	**dis**	**ina**
class 7										
CMD40	-	-	-	-	data	-	-	-	-	-
CMD42	-	-	-	-	rcv	-	-	-	-	-
class 8										
CMD55	idle	-	-	stby	tran	data	rcv	prg	dis	-
CMD56; RD/WR = 0	-	-	-	-	rcv	-	-	-	-	-
CMD56; RD/WR = 1	-	-	-	-	data	-	-	-	-	-
ACMD6	-	-	-	-	tran	-	-	-	-	-
ACMD13	-	-	-	-	data	-	-	-	-	-
ACMD14-16	Refer to DPS Specification									
ACMD22	-	-	-	-	data	-	-	-	-	-
ACMD23	-	-	-	-	tran	-	-	-	-	-
ACMD28	Refer to DPS Specification									
ACMD18,25,26,38, 43,44,45,46,47,48,49	Refer to the "Part3 Security Specification" for information about the SD Security Features									
ACMD41, OCR check is OK and card is not busy	ready	-	-	-	-	-	-	-	-	-
ACMD41, OCR check is OK and card is busy[2]	idle	-	-	-	-	-	-	-	-	-
ACMD41, OCR check fails	ina	-	-	-	-	-	-	-	-	-
ACMD41, query mode	idle	-	-	-	-	-	-	-	-	-
ACMD42	-	-	-	-	tran	-	-	-	-	-
ACMD51	-	-	-	-	data	-	-	-	-	-
class 9										
CMD52-CMD54	Refer to the "SDIO Card Specification"									
class 10[1]										
CMD6	-	-	-	-	data	-	-	-	-	-
CMD34-37,50,57	Refer to each command system specification									
class 11										
CMD21	Refer to DPS Specification									
CMD48	-	-	-	-	data	-	-	-	-	-
CMD49	-	-	-	-	rcv	-	-	-	-	-
CMD58	-	-	-	-	data	-	-	-	-	-
CMD59	-	-	-	-	rcv	-	-	-	-	-
CMD41,CMD43-47	reserved									
CMD60...CMD63	reserved for manufacturer									

Note (1): Class 10 commands were defined in Version 1.10.
Note (2): Card returns busy in case of following.
- Card executes internal initialization process
- When HCS in the argument is set to 0 to SDHC or SDXC Card.

Table 4-34: Card State Transition Table

The state transitions of the SD Memory Card application-specific commands are given under Class 8, above.

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4.9 Responses

All responses are sent via the command line CMD. The response transmission always starts with the left bit of the bit string corresponding to the response codeword. The code length depends on the response type.

A response always starts with a start bit (always 0), followed by the bit indicating the direction of transmission (card = 0). A value denoted by 'x' in the tables below indicates a variable entry. All responses except the type R3 (see below) are protected by a CRC (see Chapter 4.5 for the definition of CRC7). Every command codeword is terminated by the end bit (always 1).

There are five types of responses for the SD Memory Card. The SDIO Card supports additional response types named R4 and R5. Refer to SDIO Card Spec for detailed information on the SDIO commands and responses. Their formats are defined as follows:

4.9.1 R1 (normal response command):

Code length is 48 bits. The bits 45:40 indicate the index of the command to be responded to, this value being interpreted as a binary coded number (between 0 and 63). The status of the card is coded in 32 bits. Note that if a data transfer to the card is involved, then a busy signal may appear on the data line after the transmission of each block of data. The host shall check for busy after data block transmission. The card status is described in Chapter 4.10.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	x	x	x	'1'
Description	start bit	transmission bit	command index	card status	CRC7	end bit

Table 4-35: Response R1

4.9.2 R1b

R1b is identical to R1 with an optional busy signal transmitted on the data line. The card may become busy after receiving these commands based on its state prior to the command reception. The Host shall check for busy at the response.

4.9.3 R2 (CID, CSD register)

Code length is 136 bits. The contents of the CID register are sent as a response to the commands CMD2 and CMD10. The contents of the CSD register are sent as a response to CMD9. Only the bits [127...1] of the CID and CSD are transferred, the reserved bit [0] of these registers is replaced by the end bit of the response.

Bit position	135	134	[133:128]	[127:1]	0
Width (bits)	1	1	6	127	1
Value	'0'	'0'	'111111'	x	'1'
Description	start bit	transmission bit	reserved	CID or CSD register incl. internal CRC7	end bit

Table 4-36: Response R2

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4.9.4 R3 (OCR register)

Code length is 48 bits. The contents of the OCR register are sent as a response to ACMD41.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'111111'	x	'1111111'	'1'
Description	start bit	transmission bit	reserved	OCR register	reserved	end bit

Table 4-37: Response R3

4.9.5 R6 (Published RCA response)

Code length is 48 bit. The bits 45:40 indicate the index of the command to be responded to - in that case, it will be '000011' (together with bit 5 in the status bits it means = CMD3). The 16 MSB bits of the argument field are used for the Published RCA number.

Bit position	47	46	[45:40]	[39:8] Argument field		[7:1]	0
Width (bits)	1	1	6	16	16	7	1
Value	'0'	'0'	x	x	x	x	'1'
Description	start bit	transmission bit	command index ('000011')	New published RCA [31:16] of the card	[15:0] card status bits: 23,22,19,12:0 (see Table 4-41)	CRC7	end bit

Table 4-38: Response R6

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4.9.6 R7 (Card interface condition)

Code length is 48 bits. The card supported voltage information of 3.3V range power pin is sent by the response of CMD8. Bits 19-16 indicate the voltage range that the card supports. The card that accepted the supplied voltage returns R7 response. In the response, the card echoes back both the voltage range and check pattern set in the argument.

Bit position	47	46	[45:40]	[39:20]	[19:16]	[15:8]	[7:1]	0
Width (bits)	1	1	6	20	4	8	7	1
Value	'0'	'0'	'001000'	'00000h'	x	x	x	'1'
Description	Start bit	Transmission bit	Command index	Reserved bits	Voltage accepted	Echo-back of check pattern	CRC 7	End bit

Table 4-39: Response R7

Table 4-40 shows the format of 'voltage accepted' in R7.

Voltage accepted	Value Definition
0000b	Not Defined
0001b	2.7-3.6V
0010b	Reserved for Low Voltage Range
0100b	Reserved
1000b	Reserved
Others	Not Defined

Table 4-40: Voltage Accepted in R7

SD Association

4.10 Two Status Information of SD Memory Card

The SD Memory Card supports two status fields as follows:
- '*Card Status*': Error and state information of a executed command, indicated in the response
- *'SD Status*': Extended status field of 512 bits that supports special features of the SD Memory Card and future Application-Specific features.

4.10.1 Card Status

The response format R1 contains a 32-bit field named *card status*. This field is intended to transmit the card's status information (which may be stored in a local status register) to the host. If not specified otherwise, the status entries are always related to the previous issued command.
Table 4-41 defines the different entries of the status. Unused reserved bits shall be set to 0. The type and clear condition fields in the table are abbreviated as follows:

- Type:
  •E: Error bit.
  •S: Status bit.
  •R: Detected and set for the actual command response.
  •X: Detected and set during command execution. The host can get the status by issuing a command with R1 response.

- Clear Condition:
  •A: According to the card current state.
  •B: Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).
  •C: Clear by read.

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Bits	Identifier	Type	Value	Description	Clear Condition
31	OUT_OF_RANGE	E R X	'0'= no error '1'= error	The command's argument was out of the allowed range for this card.	C
30	ADDRESS_ERROR	E R X	'0'= no error '1'= error	A misaligned address which did not match the block length was used in the command.	C
29	BLOCK_LEN_ERROR	E R X	'0'= no error '1'= error	The transferred block length is not allowed for this card, or the number of transferred bytes does not match the block length.	C
28	ERASE_SEQ_ERROR	E R	'0'= no error '1'= error	An error in the sequence of erase commands occurred.	C
27	ERASE_PARAM	E R X	'0'= no error '1'= error	An invalid selection of write-blocks for erase occurred.	C
26	WP_VIOLATION	E R X	'0'= not protected '1'= protected	Set when the host attempts to write to a protected block or to the temporary or permanent write protected card.	C
25	CARD_IS_LOCKED	S X	'0' = card unlocked '1' = card locked	When set, signals that the card is locked by the host	A
24	LOCK_UNLOCK_FAILED	E R X	'0' = no error '1' = error	Set when a sequence or password error has been detected in lock/unlock card command.	C
23	COM_CRC_ERROR	E R	'0'= no error '1'= error	The CRC check of the previous command failed.	B
22	ILLEGAL_COMMAND	E R	'0'= no error '1'= error	Command not legal for the card state	B
21	CARD_ECC_FAILED	E R X	'0'= success '1'= failure	Card internal ECC was applied but failed to correct the data.	C
20	CC_ERROR	E R X	'0'= no error '1'= error	Internal card controller error	C
19	ERROR	E R X	'0'= no error '1'= error	A general or an unknown error occurred during the operation.	C
18	reserved				
17	reserved for DEFERRED_RESPONSE (Refer to eSD Addendum)				
16	CSD_OVERWRITE	E R X	'0'= no error '1'= error	Can be either one of the following errors: - The read only section of the CSD does not match the card content. - An attempt to reverse the copy (set as original) or permanent WP (unprotected) bits was made.	C
15	WP_ERASE_SKIP	E R X	'0'= not protected '1'= protected	"Set when only partial address space was erased due to existing write protected blocks or the temporary or permanent write protected card was erased.	C

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Bits	Identifier	Type	Value	Description	Clear Condition
14	CARD_ECC_DISABLED	S X	'0'= enabled '1'= disabled	The command has been executed without using the internal ECC.	A
13	ERASE_RESET	S R	'0'= cleared '1'= set	An erase sequence was cleared before executing because an out of erase sequence command was received	C
12:9	CURRENT_STATE	S X	0 = idle 1 = ready 2 = ident 3 = stby 4 = tran 5 = data 6 = rcv 7 = prg 8 = dis 9-14 = reserved 15 = reserved for I/O mode	The state of the card when receiving the command. If the command execution causes a state change, it will be visible to the host in the response to the next command. The four bits are interpreted as a binary coded number between 0 and 15.	B
8	READY_FOR_DATA	S X	'0'= not ready '1'= ready	Corresponds to buffer empty signaling on the bus	A
7:6					
5	APP_CMD	S R	'0' = Disabled '1' = Enabled	The card will expect ACMD, or an indication that the command has been interpreted as ACMD	C
4	reserved for SD I/O Card				
3	AKE_SEQ_ERROR (SD Memory Card app. spec.)	E R	'0' = no error '1' = error	Error in the sequence of the authentication process	C
2	reserved for application specific commands				
1, 0	reserved for manufacturer test mode				

Table 4-41: Card Status

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For each command responded by R1 response, following table defines the affected bits in the status field. An 'x' means the error/status bit may be set in the response to the respective command.

CMD Number	Response Format Card Status Bit Number																					
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12:9	8	5
3[1]									x	x			x							x		
6[2]	x						x		x	x	x	x	x							x		
7					x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	
11							x		x	x			x							x		
12	x	x				x	x		x	x	x	x	x					x		x		
13	x	x			x	x	x	x	x	x	x	x	x			x	x	x		x	x	
16			x		x	x	x	x	x	x	x	x	x			x	x	x	x	x		
17	x	x			x	x	x	x	x	x	x	x	x			x	x	x	x	x		
18	x	x			x	x	x	x	x	x	x	x	x			x	x	x	x	x		
19	x	x			x	x	x	x	x	x	x	x	x			x	x	x	x	x		
20	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	
23	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x		
24	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	
25	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	
26					x	x	x	x	x	x	x	x	x			x	x	x	x	x		
27					x	x	x	x	x	x	x	x	x			x	x	x	x	x		
28	x				x	x	x	x	x	x	x	x	x			x	x	x	x	x		
29	x				x	x	x	x	x	x	x	x	x			x	x	x	x	x		
30	x				x	x	x	x	x	x	x	x	x			x	x	x	x	x		
32	x			x	x	x	x	x	x	x	x	x	x			x	x	x	x	x		
33	x			x	x	x	x	x	x	x	x	x	x			x	x	x	x	x		
38				x	x	x	x	x	x	x	x	x	x			x	x	x	x	x		
42					x	x	x	x	x	x	x	x	x			x	x	x	x	x		
48	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	
49	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	
55					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x
56					x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x
58	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	
59	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	
ACMD6	x				x	x	x	x	x	x	x	x	x			x	x	x	x	x		x
ACMD13					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x
ACMD22					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x
ACMD23					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x
ACMD42					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x
ACMD51					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x

(1) The response to CMD3 is R6 that includes only bits 23, 22, 19 and 12:9 out of the Card Status
(2) This command was defined in version 1.10

Table 4-42: Card Status Field/Command - Cross Reference

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4.10.2 SD Status

The SD Status contains status bits that are related to the SD Memory Card proprietary features and may be used for future application-specific usage. The size of the SD Status is one data block of 512 bit. The content of this register is transmitted to the Host over the DAT bus along with a 16-bit CRC. The SD Status is sent to the host over the DAT bus as a response to ACMD13 (CMD55 followed with CMD13). ACMD13 can be sent to a card only in '*tran_state*' (card is selected). The SD Status structure is described in below. Unused reserved bits shall be set to 0.

The same abbreviation for 'type' and 'clear condition' were used as for the Card Status above.

Bits	Identifier	Type	Value	Description	Clear
511:510	DAT_BUS_WIDTH	S R	'00'= 1 (default) '01'= reserved '10'= 4 bit width '11'= reserved	Shows the currently defined data bus width that was defined by SET_BUS_WIDTH command	A
509	SECURED_MODE	S R	'0'= Not in the mode '1'= In Secured Mode	Card is in Secured Mode of operation (refer to the "Part 3 Security Specification").	A
508:502	Reserved for Security Functions (Refer to Part 3 Security Specification)				
501:496	reserved				
495:480	SD_CARD_TYPE	SR	'00xxh'= SD Memory Cards as defined by this document ('x'=don't care). The following cards are currently defined: '0000h'= Regular SD RD/WR Card. '0001h'= SD ROM Card '0002h'=OTP	In the future, the 8 LSBs will be used to define different variations of an SD Memory Card (Each bit will define different SD Types). The 8 MSBs will be used to define SD Cards that do not comply with the Physical Layer Specification.	A
479:448	SIZE_OF_PROTECTED_AREA	SR	Size of protected area	(See below)	A
447:440	SPEED_CLASS	SR	Speed Class of the card	(See below)	A
439:432	PERFORMANCE_MOVE	SR	Performance of move indicated by 1 [MB/s] step.	(See below)	A
431:428	AU_SIZE	SR	Size of AU	(See below)	A
427:424	reserved				
423:408	ERASE_SIZE	SR	Number of AUs to be erased at a time	(See below)	A
407:402	ERASE_TIMEOUT	SR	Timeout value for erasing areas specified by UNIT_OF_ERASE_AU	(See below)	A
401:400	ERASE_OFFSET	SR	Fixed offset value added to erase time.	(See below)	A
399:396	UHS_SPEED_GRADE	SR	Speed Grade for UHS mode	(See below)	A
395:392	UHS_AU_SIZE	SR	Size of AU for UHS mode	(See below)	A
391:312	reserved				
311:0	reserved for manufacturer				

Table 4-43: SD Status

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- **SIZE_OF_PROTECTED_AREA**

Setting this field differs between SDSC and SDHC/SDXC.
In case of SDSC Card, the capacity of protected area is calculated as follows:
Protected Area = SIZE_OF_PROTECTED_AREA_* MULT * BLOCK_LEN.
SIZE_OF_PROTECTED_AREA is specified by the unit in MULT*BLOCK_LEN.

In case of SDHC and SDXC Cards, the capacity of protected area is calculated as follows:
Protected Area = SIZE_OF_PROTECTED_AREA
SIZE_OF_PROTECTED_AREA is specified by the unit in byte.

- **SPEED_CLASS**

This 8-bit field indicates the Speed Class. Classes lower than indicated by this field are also effective. For example, Class 10 is indicated, host should consider Class 2 to 6 is also effective.

SPEED_CLASS	Value Definition
00h	Class 0
01h	Class 2
02h	Class 4
03h	Class 6
04h	Class 10
05h – FFh	Reserved

Table 4-44: Speed Class Code Field

Application Note:
If a Class value indicated in SD Status (including reserved value) is larger than that of host supported, the host should read as any Class can be used with the card.

- **PERFORMANCE_MOVE**

This 8-bit field indicates Pm and the value can be set by 1 [MB/sec] step. If the card does not move used RUs, Pm should be considered as infinity. Setting to FFh means infinity. The minimum value of Pm is defined by in Table 4-45. Pm is defined for Class 2 to 6 in Default Speed Mode. When host uses Class 10, Pm indicated in SD Status shall be ignored and treated as 0.

PERFORMANCE_MOVE	Value Definition
00h	Sequential Write
01h	1 [MB/sec]
02h	2 [MB/sec]
.....	.....
FEh	254 [MB/sec]
FFh	Infinity

Table 4-45: Performance Move Field

SD Association