Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout

B.Doyle, B.Boyanov, S.Datta, M. Doczy, S.Hareland, B. Jin, J.Kavalieros, T. Linton*, R.Rios* & R.Chau
Components Research, TCAD*, Logic Technology Development, Intel Corporation, Hillsboro, OR 97124

I. Abstract

Tri-Gate fully-depleted CMOS transistors have been fabricated with various body dimensions. These experimental results and 3-D simulations are used to explore the design space for full depletion, as well as layout issues for the Tri-Gate architecture, down to 30nm gate lengths. It is found not only that the Tri-Gate body dimensions are flexible and relaxed compared to single-gate or double-gate devices, but that the corner plays a fundamental role in determining the device I-V characteristics. The corner device not only turns on at lower voltages due to the proximity of two adjacent gates, but the DIBL of this part of the device is much smaller than the rest of the transistor. The shape of the subthreshold I-V characteristics and the degree of DIBL control, as well as the early device turn-on are also greatly affected by the degree of body corner rounding. Examination of layout issues shows that the fin-doubling approach from using a spacer printing technique results in an increase in drive current of 1.2 times that of a planar device for a given width, though the shape of the allowed Tri-Gate fins has certain restrictions.

II. Introduction

One of the fundamental issues facing scaling of CMOS transistors is the ability to control the transistor leakage current (Ioff), while at the same time maintaining high drive current (Ion) [1]. Figure 1 shows a representative sampling of the trend of Ioff with gate length for bulk devices [2]. It can be seen that, irrespective of whether the transistors are in production (i.e. well controlled) or not, the same monotonic increase in Ioff with shrinking gate length is maintained.

One solution to this is to go to a fully-depleted design [3], where the sub-threshold slope (S/S) approaches the theoretical value of 60 mV/dec. FinFET double-gate transistors have been offered for future transistor design [4], but, while this device offers excellent short channel effect (SCE) control, the vertical nature of the device and the difficulties in fabricating such a device suggest that the Tri-Gate might be the next transistor design.

In this paper, we explore the issues facing the transistor design and layout of such devices at gate lengths of 30nm and below, both from the experimental and simulation viewpoints.

III. Tri-Gate Fabrication & Device Characteristics

Tri-Gate transistors down to 30nm were fabricated in the following manner. To get body widths of the same approx. size as the polysilicon gate, the body was first fabricated by treating it in a similar manner to polysilicon, using aggressive poly-silicon lithography and etch techniques to get body thicknesses equal to gate lengths. The body was then doped to obtain acceptable threshold voltages (Vt) using conventional boron implants. No halo implants were used for setting Vt, nor were there any angled implants used anywhere in the process. This is in contrast to Double-Gate (DG), and this is possible since the Tri-Gate very much resembles bulk transistor from the processing point-of-view. However, to get the right Vt's, it was found necessary to protect the Tri-Gate bodies from boron outdiffusion into the surrounding oxide by an N2O oxidation before gate definition. The gate stack included polysilicon gates, and a conventional physical oxide thickness of 15 Angstroms. Raised source/drains were used to reduce parasitic resistances [2], and the transistor was silicided using nickel.

CMOS Tri-Gate transistors were fabricated down to 30nm. Figures 2 and 3 show examples of CMOS devices at Lg=60nm. Fig. 4 shows the cross-section of the nMOS device in Figs 2 & 3. This device has body dimensions of H_{Si}=36nm and W_{Si}=55nm, The NMOS device had a subthreshold slope (S/S) = 68 mV/decade, DIBL=41mV/V, Ion=1.14mA/mm and Ioff=70nA/mm at Vcc= 1.3V. The PMOS device showed S/S=69.5 mV/decade, DIBL= 48mV/V, Ion=520mA/mm and Ioff = 24nA/mm at Vcc=1.3V

IV. Tri-Gate Simulations and Layout

One of the advantages of the Tri-Gate structure is the flexibility of the body. Figure 5 shows that between the extremes of Double-Gate (Fig.5 a) and Single-Gate (Fig.5 e), the Tri-Gate can have a multitude of shapes (Fig. 5 b-d). Figure 6 shows the width-to-height ratio needed to maintain the body in full depletion for single gate (SG) and DG devices, and the experimental and 3-D simulation calibrated to the experimental, for the 60nm Lg device. The simulation and experimental data shows that the body dimensions are more relaxed, and that the device has full depletion with excellent short channel control at body values greater than SG (H_{Si}) or DG (W_{Si}) devices require. The same is true at Lg=30nm (Fig. 7).

To understand this more fully, 3-D simulations were undertaken using DESSIS [5]. Both Lg=60nm (H_{Si}=60nm and W_{Si}=60nm) and Lg=30nm (H_{Si}=30nm and W_{Si}=30nm) showed full depletion at these body sizes. Fig. 8 shows the simulated Id-Vg characteristics of the Lg=30nm device. Splitting this simulation into corner and non-corner components (Fig. 9), it can be seen that the corner turns on earlier than the body. The presence of the immediately-adjacent gates (e.g. g1/g2 or g2/g3 in Fig. 5) are responsible for the lower Vt of the corner device, as well as the smaller DIBL compared to the non-corner device. This is further shown in Figure 10, where the corner device is seen to provide most of the total transistor current, until Vg=0.4-0.5V. The corner effect can also be seen from the electron density curves of Figure 11, where at Vg=0.4V, Vd=1V, the corner regions have the highest electron density. Thus the full transistor depends intimately on the corner. If the body is too wide, the full device shows a hump in log Id-Vg resulting in lower Ion.

To further explore the corner effect, simulations were performed on devices whose corner shape was changed. This is shown in Figure 12, where R represents the radius of curvature of the corner. It can be seen that the sharper the corner, the greater the early turn-on effect of the corner device and the smaller the DIBL. By R=20nm, the Vt of the corner device has shifted by almost 200mV.

Thus the best design involves keeping the body width small, at the same time rounding the Tri-Gate body corners to ensure that the corner device does not turn on too early. There are further constraints however to the design of the body, and this is related to layout. Tri-Gate body shape can vary, from FinFET-like to single-gate-like (Fig 13). In order to attain maximum perimeter width in a given layout area, spacer lithography is needed (Fig. 14) [2,7]. While the H_{is} is unlimited using this technique, W_{Si} is governed by the need to form gaps between the spacers (Fig. 14). Figure 15 shows the amount of drive current enhancement over planar devices, achieved in a given layout area. For litho printing, the fin width cannot drop below 30nm due to litho limitations at this node. This gives a drive current of 0.6 times the planar device. For spacer printing, the minimum width has no limits, but the maximum width is fixed at 50nm, due to the need to define the spacers themselves (Fig. 14). The gain in Ion is always greater than for a planar device, and at 30nm dimensions, the Ion is 120% that of a planar device.

V. Conclusions

Tri-Gate CMOS transistors have been fabricated, as well as simulated down to Lg=30nm to explore the fabrication and design space at these dimensions. Full depletion is achieved with relaxed body dimensions over other fully-depleted transistor structures. It is found that the corner of the body plays an dominant role in the sub-threshold behavior. Furthermore, corner rounding is found to affect greatly the threshold voltage of the devices, as well as the sub-threshold characteristics. It is also shown that layout play an important part in the shape of the Tri-Gate body. It is concluded that in an optimized Tri-Gate device, particular attention will have to be paid to the device body edges.

VI. References

[1] ITRS 2001, PIDS section, Table 2a.
[2] B.Doyle et al. Intel Technology Journal, vol 6(2), V, pp.1-9 (2001)
[3] R.Chau et al, IEDM 2000, pp. 45-48.
[4] H-S. P. Wong et al, IEDM Technical Digest, pp. 407 -410, 1998
[5] R. Chau et al., SSDM, pp. 68-69, 2002
[6] "DESSIS", ISE TCAD Release 7.0 Manual, Volume 4A, Part 12.
[7] C-M Hu et al, IEEE Trans El Dev.,Vol. 49, pp. 436-441, 2002

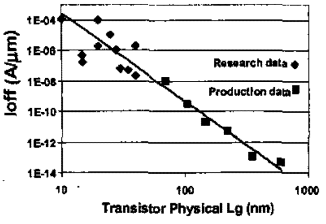

Figure 1. Increase in off-current with decreasing gate length for conventional planar transistors.

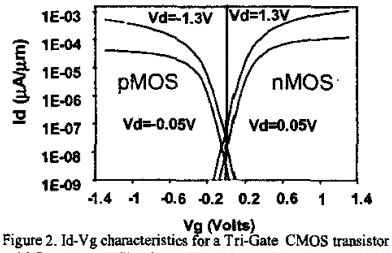

Figure 2. Id-Vg characteristics for a Tri-Gate CMOS transistor with Lg=60nm, WSi=55nm, HSi =36nm at Vcc=0.05V and 1.3V.

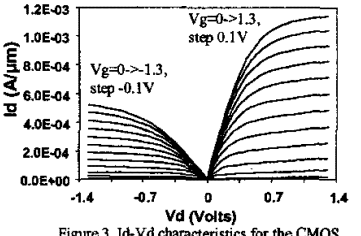

Figure 3. Id-Vd characteristics for the CMOS Tri-Gate transistor of Figure 2.

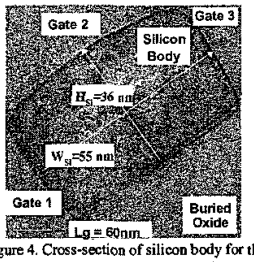

Figure 4. Cross-section of silicon body for the nMOS Tri-Gate Transistor of Figs 2 & 3.

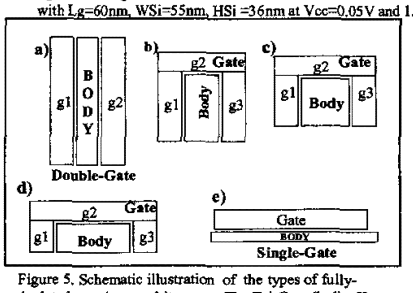

Figure 5. Schematic illustration of the types of fully-depleted transistor architectures. The Tri-Gate (b-d) offers flexibility in silicon body geometry.

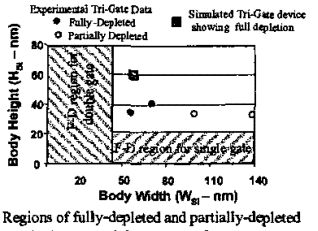

Figure 6. Regions of fully-depleted and partially-depleted behavior for Single gate and double-gate @Lg=60nm.Tri-Gate body shows more relaxed body dimensions than either.

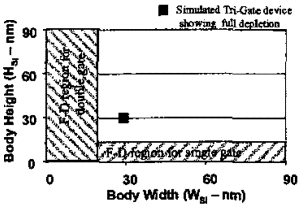

Figure 7. Regions of fully depleted and partially depleted behavior for s ingle gate and double-gate @Lg=30nm.Tri-Gate body shows more relaxed body dimensions than either.

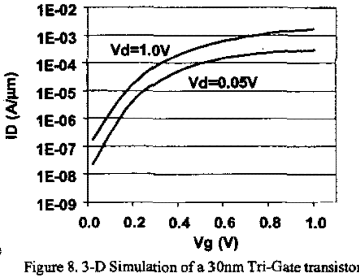

Figure 8. 3-D Simulation of a 30nm Tri-Gate transistor.

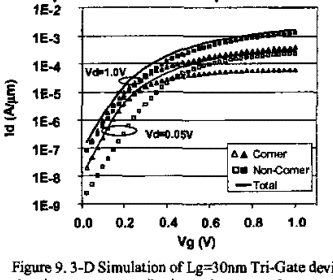

Figure 9. 3-D Simulation of Lg=30nm Tri-Gate device, showing current contributions of corner and non-corner regions.

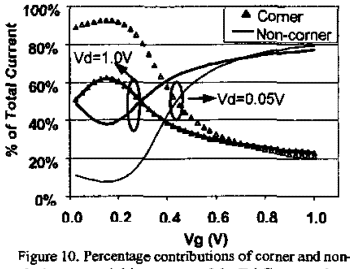

Figure 10. Percentage contributions of corner and non-corner devices to total drive current of the Tri-Gate transistor.

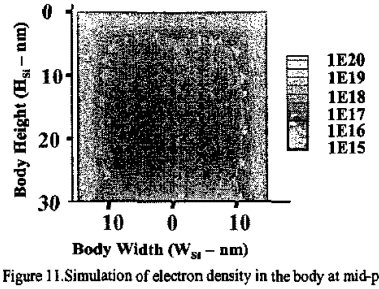

Figure 11.Simulation of electron density in the body at mid-point between source and drain, for Vd=1V, Vg=0.4.

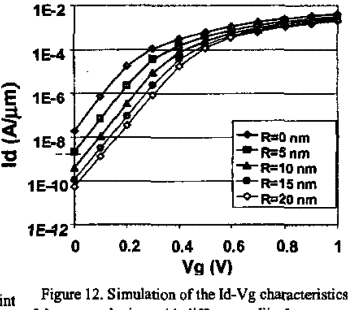

Figure 12. Simulation of the Id-Vg characteristics of the corner device, with different radii of curvature and Lg=30nm.

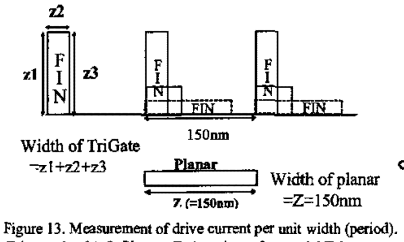

Figure 13. Measurement of drive current per unit width (period). Trigate:z1+z2+z3. Planar : Z. A variety of potential Tri-Gate dimensions is also shown, each of which would have different perimeter width per unit period

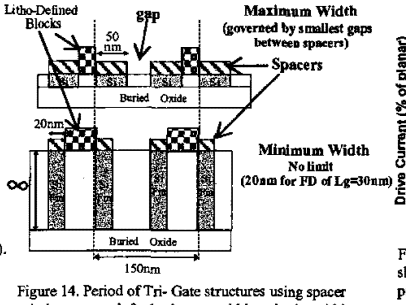

Figure 14. Period of Tri- Gate structures using spacer printing approach for both max. width and min. width dimensions to maintain full depletion

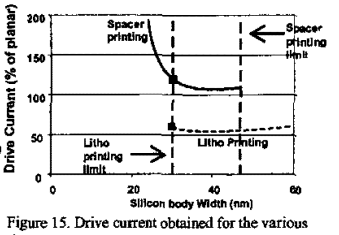

Figure 15. Drive current obtained for the various shapes of fully-depleted silicon fin for both litho printing and spacer printing. The silicon height is adjusted to maintain full depletion.