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Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond

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Abstract. One of the greatest challenges for future CMOS generations is to limit the series resistance of source/drain junctions and their contacts to a small fraction of the channel 'on' resistance. This challenge is caused by structural changes in transistor design as well as fundamental limitations of silicon as a semiconductor. It is anticipated that junctions that rely solely on ion-implantation combined with an advanced annealing technique will not meet our expectations beyond the 45 nm node. Fundamentally different processes and new materials are needed to meet the future requirements. Starting with the 90 nm technology node, we have already begun to see examples of departures from the conventional junction formation methods. A good example is Intel's 90 nm technology process featuring recessed $\text{Si}_{1-x}\text{Ge}_x$ source/drain junctions incorporated to address the series resistance concerns and to introduce uniaxial strain into the channel for enhanced mobility. It is predicted that within a few years the conventional planar MOSFET will be replaced with one of the so-called "non-classical" transistor structures, which include the fully-depleted SOI, FINFET and various structures proposed for enhanced carrier mobility via strain engineering. Unfortunately, these structures bring their own source/drain integration challenges requiring further innovations in materials and processes. This paper presents an overview of the key source/drain challenges with emphasis on MOSFET series resistance. Potential solutions to these challenges with emphasis on applications of $\text{Si}_{1-x}\text{Ge}_x$ in source/drain engineering will be discussed in reference to various transistor structures currently considered as potential candidates for future CMOS generations.

Keywords: CMOS, source/drain junctions, series resistance

PACS: 85.30.Tv, 85.30.Kk, 85.40.Ls, 85.30.De

INTRODUCTION

The planar MOSFET structure, which has survived continued scaling for more than two decades is beginning to show its short-comings as the CMOS integrated circuit industry approaches the 45 nm technology node. Shown in Figure 1 is the planar MOSFET in two different configurations: *extension* and *elevated contact* structures as they are referred to in the International Technology Roadmap for Semiconductors (ITRS)[1]. Continuous scaling of the MOSFET dimensions has brought the extension and contact junction depths indistinguishably close to each other. In the extension structure, the thickness of the silicide contact has to be scaled with the junction depth in order to keep the defective silicide/silicon interface sufficiently away from the junction depletion region. Unfortunately, the silicide forms by consuming the underlying junction and its thickness cannot be scaled indefinitely due to agglomeration. The elevated contact structure provides a sacrificial silicon layer to consumption and allowing a thicker silicide contact. Figure 2 shows the predicted junction depth for different CMOS technology nodes. It can be seen that beyond 60 nm, the extension structure is abandoned for the elevated contact structure. ITRS also predicts that around

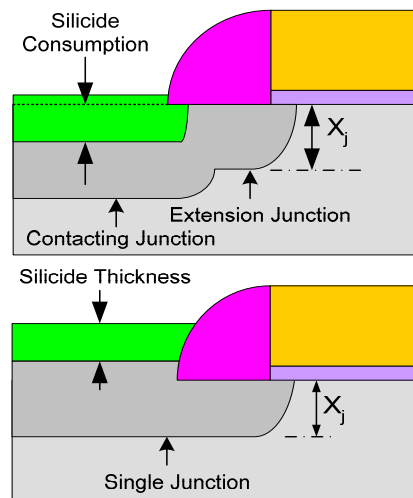


FIGURE 1. Extension and Elevated Contact Structures

45 nm, a fully depleted structure will be adopted with the junction depth approaching 5 nm toward the end of the roadmap.

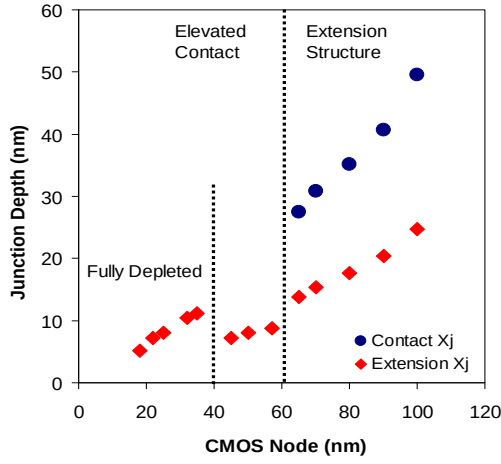


FIGURE 2. Junction Depth of the extension and contact junctions as a function of the DRAM half pitch.

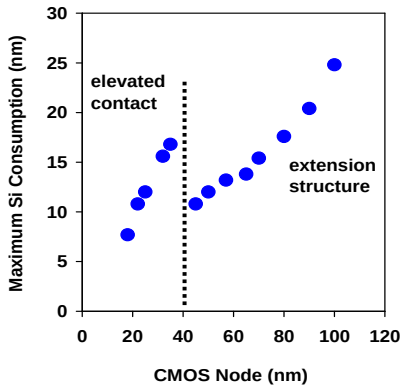


FIGURE 3. Maximum allowable silicon consumption in *extension* and *elevated-contact* structures plotted as a function of DRAM half pitch.

Figure 3 shows the maximum allowable Si consumption for different technology nodes. The discontinuity at 45 nm is due to the sacrificial layer provided by the elevated contact structure allowing a thicker silicide. A typical elevated contact layer is formed by selective Si epitaxy over the source/drain regions. There are key manufacturing challenges associated with this process. First, excellent selectivity is required to avoid spurious nucleation on insulators resulting in electrical shorts. Second, the doping density at the metal-semiconductor interface must be sufficiently high to achieve an excellent ohmic contact. If the selectively deposited material is in-situ doped, this can be achieved regardless of the silicide or Si thickness. Finally, the elevated contact must be free of defects, which is not a simple task when the silicon layer is grown on a heavily doped extension junction [2, 3].

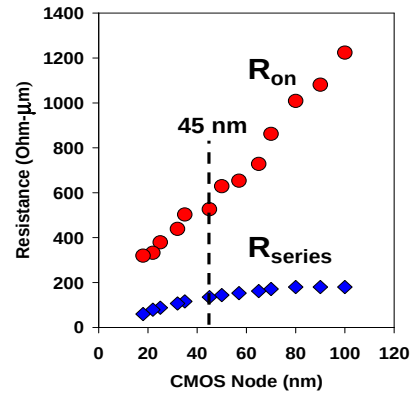


FIGURE 4. Channel resistance and maximum allowable series resistance as a function of DRAM half pitch.

MOSFET SERIES RESISTANCE

A grand challenge for future CMOS technology nodes is to form ultra-shallow source/drain junctions with a parasitic series resistance limited to a small fraction of the channel 'on' resistance. Figure 4 shows the channel resistance and the maximum allowable source/drain resistance for different technology generations. The leading three contributors to the source/drain series resistance are the bulk resistance of the extension and contacting junctions under the sidewall spacer, the overlap resistance, which includes the accumulation and spreading resistances and the contact resistance of the silicide-silicon interface[4]. To reduce the bulk resistance, we need junction formation methods that can provide high levels of dopant activation such that the junction depth - sheet resistance product can be kept at a small value. The overlap resistance is determined by the maximum doping level under the spacer, extension lateral abruptness and the width of the sidewall spacer. While reducing the lateral abruptness can reduce the overlap resistance, it can also increase the *off* current, which must be carefully weighed in optimizing the junction formation method[5].

Contact Resistance

With continued scaling of the MOSFET, the contact resistance has become a major contributor to the series resistance. To lower the contact the resistance, we need a small Schottky barrier height at the interface and a sufficiently high doping level under the metal contact. The contact resistivity, ρ_c of a metal-semiconductor contact can be expressed as

$$\rho_c = K \exp \left[\frac{\phi_B}{\sqrt{N}} \right] \quad (1)$$

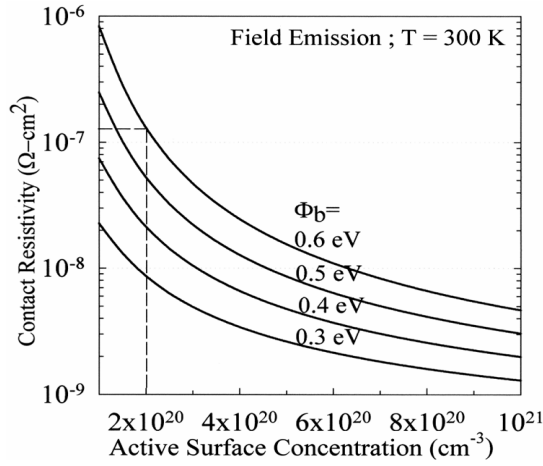


FIGURE 5. Dependence of contact resistivity on doping concentration under the contact and metal-semiconductor barrier height.

where K is a constant determined by the semiconductor, ϕ_B is the barrier height and N is the doping density under the metal contact. This dependence can be observed in Figure 5, which shows the contact resistivity plotted as a function of the doping concentration for different barrier heights. The barrier height is largely determined by pinning of the Fermi level at a fixed energy level within the semiconductor forbidden gap with little dependence on the metal work function. The doping level is usually determined by the solid solubility level of the dopant in Si. Assuming Fermi level pinning near the midgap and a maximum doping level of $2 \times 10^{20} \text{ cm}^{-3}$ (typical for boron) a contact resistivity of $10^{-7} \Omega - \text{cm}^2$ is obtained as shown in Figure 5, which is the current state-of-art for silicon with implanted junctions and silicided contacts.

Shown in Figure ?? is the maximum allowable contact resistivity for different technology generations from ITRS. It can be seen that both NMOS and PMOS devices will require a contact resistivity under $10^{-7} \Omega - \text{cm}^2$ beyond 45 nm. The discontinuity in the curves is due to the reduced channel resistance with the dual gate structure and the desire to keep the series resistance at the same percentage level. It is important to realize that the curves in 6 were obtained assuming that the series resistance is entirely determined by the contact resistance ignoring the contributions from extension and overlap resistances. Since we know that this is not true, the curves in Figure 6 only serve as an upper bound, the actual contact resistivity must be lower.

Since the maximum doping level under the contact is determined by the solid solubility of the dopant in Si, there is not much we can do to increase the active carrier concentration unless a non-equilibrium technique is

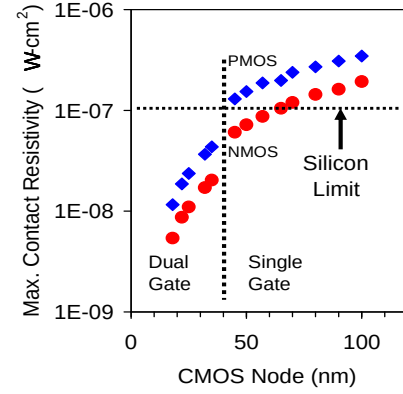


FIGURE 6. Maximum allowable contact resistivity assuming the entire series resistance is due to contact resistance.

employed in junction formation. Another possibility is to reduce the barrier height by using two different metals with work-functions near the conduction and valence band edges of Si. Unfortunately, pinning of the Fermi level makes the barrier height more or less independent of the metal work function severely limiting our flexibility in choosing new contact materials. A potential solution is Fermi level depinning by passivating the surface states. In a recent article, Tao et al. used a monolayer of selenium to achieve the ideal barrier heights expected for Al and Cr on n-type Si [6]. More work is needed on this topic before the dual-metal approach can be considered as a viable approach.

SILICON-GERMANIUM SOURCE/DRAIN TECHNOLOGY

Another approach is to use a semiconductor with a smaller bandgap than Si under the contact metal assuming that the Fermi level pinning will always be present. A suitable material is $\text{Si}_{1-x}\text{Ge}_x$, which can be grown selectively at temperatures as low as 500 °C. While the material can be doped by ion-implantation, in-situ doping offers high boron incorporation without the need for a high-temperature activation anneal. An example is presented in Figure 7, which shows the atomic boron profile obtained by secondary ion mass spectroscopy from an in-situ doped $\text{Si}_{1-x}\text{Ge}_x$ layer grown by ultrahigh vacuum rapid thermal chemical vapor deposition. The details of the deposition conditions can be found in earlier publications from our laboratory [7, 8]. It can be seen that the boron concentration in the $\text{Si}_{1-x}\text{Ge}_x$ layer is more than 10^{21} cm^{-3} . What makes this result valuable is the fact that boron activation in $\text{Si}_{1-x}\text{Ge}_x$ is also higher, which is demonstrated in Figure 8 comparing

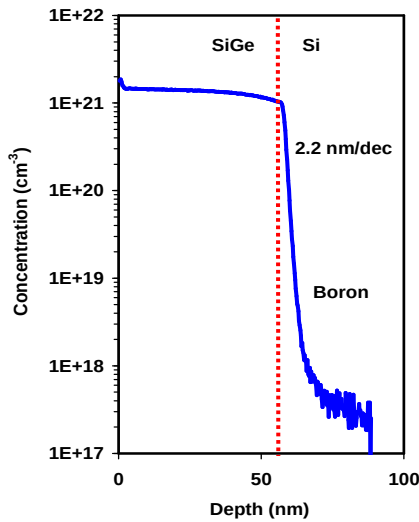


FIGURE 7. Boron profile obtained from an in-situ doped $\text{Si}_{1-x}\text{Ge}_x$ film grown by UHV-RTCVD

boron in Si and $\text{Si}_{0.55}\text{Ge}_{0.45}$. Secondary Ion Mass Spectroscopy was used to measure the atomic boron concentration in Si. Hall Effect was used to measure the active doping concentration in both Si and $\text{Si}_{1-x}\text{Ge}_x$. A Hall scattering factor of unity was assumed. It can be seen that while the boron concentration increases with the diborane flow, the active doping concentration in Si saturates at a level under $2 \times 10^{20} \text{ cm}^{-3}$. On the other hand, in $\text{Si}_{0.55}\text{Ge}_{0.45}$, the doping concentration continues to increase with the diborane flow reaching a maximum concentration of $7 \times 10^{20} \text{ cm}^{-3}$.

Another important feature in Figure 7 is the abruptness of the boron profile, which is helpful in reducing the overlap resistance. The growth temperature of 500°C is too low for any boron diffusion, resulting in a very abrupt junction. The value shown in Figure 7 has not been corrected for the SIMS cascading effect, nevertheless, it is still an excellent number satisfying extension lateral abruptness requirements down to 45 nm in ITRS [1].

High boron activation, smaller bandgap and the ability to reduce boron diffusion formed the basis for the $\text{Si}_{1-x}\text{Ge}_x$ source/drain technology[7], which involved etching the source/drain areas to a desired depth followed by selective deposition of an in-situ doped $\text{Si}_{1-x}\text{Ge}_x$ layer. In this approach, the junction is formed solely by the in-situ doped $\text{Si}_{1-x}\text{Ge}_x$ layer. Because a subsequent high-temperature step is not used, the abruptness of the original profile is preserved, hence, the recess depth determines the junction depth. A key challenge with this approach is to protect the gate dielectric during the source/drain etch and the $\text{Si}_{1-x}\text{Ge}_x$ deposition. A simpler integration approach is to form the

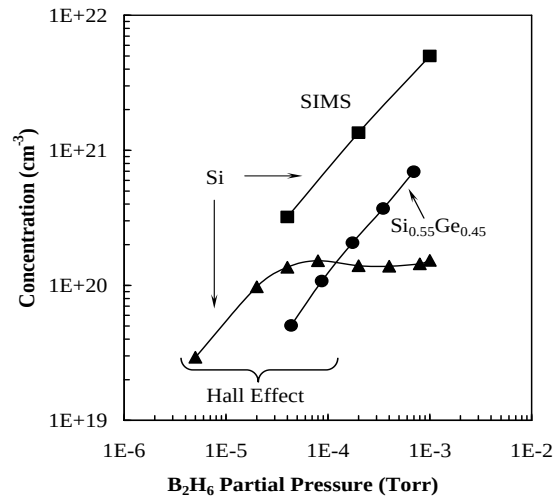


FIGURE 8. Atomic boron concentration obtained in Si by SIMS and the hole density obtained in Si and $\text{Si}_{1-x}\text{Ge}_x$ by Hall Effect measurements.

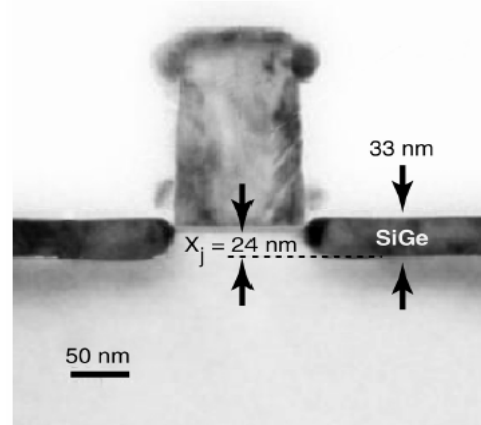


FIGURE 9. P-channel MOSFET with $\text{Si}_{1-x}\text{Ge}_x$ source/drain junctions.

extension by out-diffusion of dopant atoms from the doped $\text{Si}_{1-x}\text{Ge}_x$ layer. Another approach is to form the extension junction by ion-implantation and use the $\text{Si}_{1-x}\text{Ge}_x$ layer as the contacting junction to reduce the contact resistance. First MOSFETs using $\text{Si}_{1-x}\text{Ge}_x$ in recessed source/drain regions were fabricated in a joint work by Motorola and NCSU[8]. Shown in Figure 9 is a cross-sectional transmission electron micrograph of the MOSFETs from this study.

Self-Aligned Nickel Germanosilicide Contacts

If $\text{Si}_{1-x}\text{Ge}_x$ is used as the source/drain material, there is a need to identify a contact material equivalent to silicides used to form self-aligned contacts to junctions formed in silicon. Fortunately, $\text{Si}_{1-x}\text{Ge}_x$ alloys also react with the popular silicide elements to form low-resistivity germanosilicides, which can be formed self-aligned to the exposed $\text{Si}_{1-x}\text{Ge}_x$ areas[9]. There are however important challenges associated with germanosilicides. It has been shown that at elevated temperatures Ge atoms in all germanosilicides show the tendency to segregate at the grain boundaries to form Ge rich $\text{Si}_{1-x}\text{Ge}_x$ grains [9, 10, 11, 12]. This leads to a rough interface, leaky junctions and a very high-sheet resistance, which sets the upper-bound for subsequent process temperatures.

Our recent work in this laboratory focused on nickel germanosilicide ($\text{NiSi}_{1-x}\text{Ge}_x$) contacts to boron and phosphorus doped $\text{Si}_{1-x}\text{Ge}_x$ alloys [9]. There are several important reasons for choosing Ni as the germanosilicide element: NiSi has a resistivity comparable to that of TiSi_2 and CoSi_2 , it forms at lower temperatures with less silicon consumption and there are no known adverse narrow line effects. Finally, both Ni silicide and germanide have the same crystalline structure with very similar lattice constants; therefore, the materials are miscible with the potential to form a ternary germanosilicide phase. Finally, NiSi is already used in IC manufacturing, hence, there already exists a knowledge base for Ni.

The results from this study have shown that high quality $\text{NiSi}_{1-x}\text{Ge}_x$ contacts can be formed on both boron and phosphorus doped $\text{Si}_{1-x}\text{Ge}_x$ alloys, however, Ge out-diffusion from the germanosilicide grains limit the maximum processing temperature to approximately 450°C . We have also shown that by inserting a thin Pt layer between Ni and $\text{Si}_{1-x}\text{Ge}_x$, the thermal stability of the germanosilicide can be significantly improved[9]. The resulting germanosilicide maintains a low resistivity and a smooth interface at elevated temperatures. Figure 10 shows a cross-sectional TEM micrograph from a sample annealed at 600°C . Using the approach or by keeping the maximum temperature below 450°C , $\text{Si}_{1-x}\text{Ge}_x$ junctions with excellent reverse leakage behavior and a minimum contact resistivity of $\sim 10^{-8} \Omega - \text{cm}^2$ can be formed[8].

Contact Resistivity

Figure 11 shows the measured contact resistivity values as a function of the B_2H_6 partial pressure for contacts formed on Si and $\text{Si}_{1-x}\text{Ge}_x$ with two different Ge levels of 42% and 51%. The boron concentration was

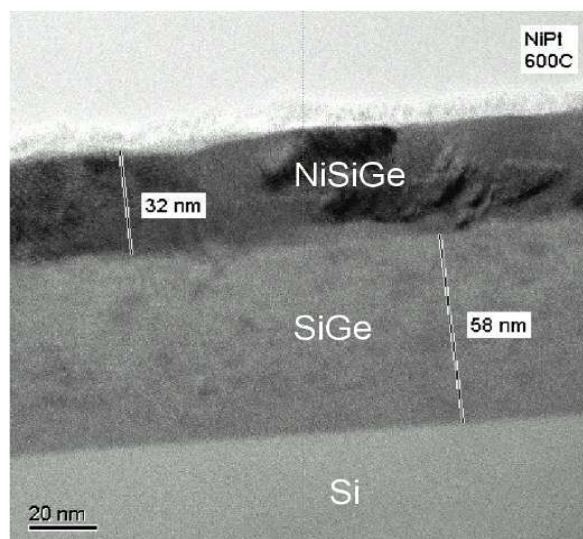


FIGURE 10. Cross-sectional TEM micrograph of a germanosilicide formed with Ni(15nm) and Pt(1.5nm) on boron doped $\text{Si}_{1-x}\text{Ge}_x$ and annealed at 600°C

also varied in a wide range by changing the B_2H_6 flow rate during growth. One can refer to Figure 8 to correlate the B_2H_6 flow to boron concentration. The lower doping levels were included in this study only to verify the trend since they are far below the levels we expect to have in state-of-the-art source/drain junctions. The starting Ni thickness was 10 nm and the $\text{NiSi}_{1-x}\text{Ge}_x$ and NiSi contacts were both formed at 400°C to obtain a smooth interface. It can be seen that there exists a significant drop in contact resistivity when $\text{Si}_{1-x}\text{Ge}_x$ is used. For both materials, the contact resistivity is reduced by increasing the active doping level. Increasing the Ge concentration from 42 to 51 % further drops the contact resistivity except for the highest doping concentration, which might be related to changes in the band structure due to very high levels of boron [7]. The key conclusion from Figure 11 is that by using $\text{Si}_{1-x}\text{Ge}_x$, a minimum contact resistivity of $2 \times 10^{-8} \Omega - \text{cm}^2$ is obtained, which satisfies the contact resistivity requirements for future CMOS technology nodes near the end of the ITRS roadmap [1]. In comparison, the best contact resistivity obtained for the NiSi/Si interface was about 3×10^{-7} , which is in agreement with the theoretical predictions [7].

Schottky Barrier Height

It is necessary to understand the parameters influencing the $\text{Si}_{1-x}\text{Ge}_x$ bandgap. This is especially true for very high boron levels used in this work, which can

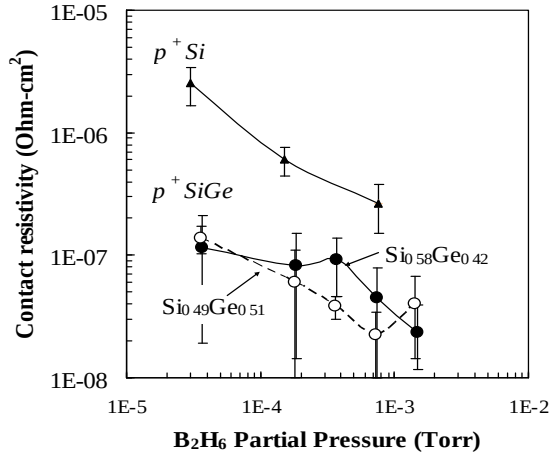


FIGURE 11. The experimentally obtained contact resistivity values obtained with two different Ge percentages plotted as a function of the B_2H_6 partial pressure.

affect the bandgap via strain compensation, which was proposed as a potential mechanism to explain enhanced boron activation in $Si_{1-x}Ge_x$ in earlier work from this laboratory [7].

Metal-Semiconductor diodes were fabricated to measure the Schottky barrier height, ϕ_B , between the $NiSi_{1-x}Ge_x$ contacts and lightly boron doped $Si_{1-x}Ge_x$ layers via I-V measurements. Lightly doped $Si_{1-x}Ge_x$ layers were used to obtain rectifying instead of ohmic contacts. The barrier height was determined from [13]

$$\phi_B = \frac{kT}{q} \ln \left(\frac{A^* T^2}{J_s} \right) \quad (2)$$

where J_s is the reverse saturation current density, A^* is Richardson's constant, k is Boltzmann's constant and T is the ambient temperature. According to this equation, ϕ_B can be determined if J_s is measured and if A^* is known. In the literature, it is commonly assumed that A^* is linearly dependent on the Ge content [14]. Since A^* is available for Si and Ge, extrapolation can be used to obtain an estimate for any Ge concentration. In this work, we used A^* values of $40.8 \text{ A/cm}^2 \text{ K}^2$ and $79.2 \text{ A/cm}^2 \text{ K}^2$ for pure p-type Si and Ge respectively [14, 15, 16].

Figure 12 shows the measured barrier height values for four different Ge concentrations. The bandgap of relaxed $Si_{1-x}Ge_x$ is also plotted for reference. Since the $Si_{1-x}Ge_x$ layers are sufficiently thick ($\sim 100 \text{ nm}$) and lightly doped they are relaxed. The data indicates $\phi_B \cong 0.5 \text{ eV}$ within the range of Ge concentrations considered in this experiment. This value is lower than $\phi_B \cong 0.61 \text{ eV}$ reported by Saha et al. for $NiSiGe$ formed on relaxed $Si_{0.75}Ge_{0.25}$ at 300°C [17]. In an earlier study,

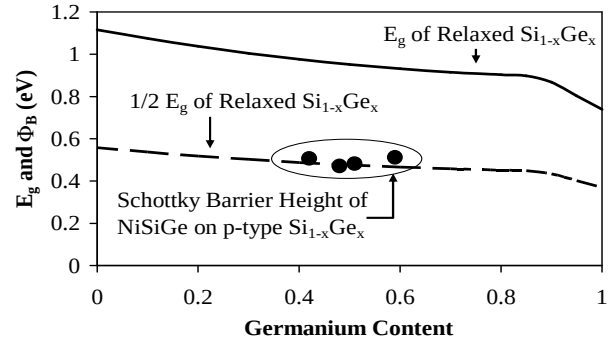


FIGURE 12. Barrier height measured at the $NiSi_{1-x}Ge_x / Si_{1-x}Ge_x$ interface.

Aubry et al. showed for W contacts formed on p-type $Si_{1-x}Ge_x$ that pinning occurred at a fixed position relative to the conduction band and the barrier height decreased with the decreasing $Si_{1-x}Ge_x$ bandgap [18]. It is difficult to arrive at a similar conclusion based on the data shown in Figure 12, which may also be interpreted as $\phi_B \cong 1/2 E_g$. In either case, we expect to have a smaller barrier height due to the smaller bandgap of $Si_{1-x}Ge_x$.

Silicon-Germanium Bandgap

The $Si_{1-x}Ge_x$ bandgap can play an important role in determining the barrier height as discussed in the previous section. In our case, this is an especially interesting question because heavy boron doping can modify the $Si_{1-x}Ge_x$ bandgap. We have measured the bandgap of $Si_{1-x}Ge_x$ layers with varying boron doping levels ranging from medium to high doping levels. Three different Ge levels of 45, 60 and 73 % were employed. PN junction diodes were fabricated by depositing in-situ boron doped $Si_{1-x}Ge_x$ layers on n-type Si. For the bandgap measurement, a method outlined in detail by Palmer was employed [19]. In this method, the built-in potential, V_{bi} of a diode is determined from its reverse bias depletion region capacitance, C , according to

$$\frac{1}{C^2} = \frac{2}{A^2 q \epsilon_{Si} N_D} (V_{bi} - V_D) \quad (3)$$

where V_D is the applied voltage, A is the junction area, ϵ_{Si} is the dielectric permittivity of Si, q is the electronic charge and N_D is the doping level in the n-type substrate. The valance band off-set, ΔE_v is then determined from

$$\Delta E_v \cong \epsilon_{g,Si} - \Delta \epsilon_{n,Si} - \Delta \epsilon_{p,SiGe} - qV_{bi} \quad (4)$$

where $\epsilon_{g,Si}$ is the Si bandgap, $\Delta \epsilon_{n,Si}$ is the separation between the conduction band and the Fermi level in n-type Si and $\Delta \epsilon_{p,SiGe}$ is the separation between the valence

band and the Fermi level in p-type $\text{Si}_{1-x}\text{Ge}_x$. Finally, the $\text{Si}_{1-x}\text{Ge}_x$ bandgap is determined from

$$\varepsilon_{g,\text{SiGe}} = \varepsilon_{\text{Si}} - \Delta\varepsilon_c - \Delta\varepsilon_v \quad (5)$$

assuming that the conduction band off-set, $\Delta\varepsilon_c$ between Si and $\text{Si}_{1-x}\text{Ge}_x$ is negligibly small.

In this study, $\Delta\varepsilon_{p,\text{SiGe}}$ in equation 4 was determined using a model proposed by Matutinovic-Kristelj [20] and the result is shown in Figure 13 for the Ge and B concentrations considered in this study. As shown, in heavily boron doped $\text{Si}_{1-x}\text{Ge}_x$, the Fermi level can have a significant penetration into the valence band. Shown in Figure 14 is the valence band offset calculated using the above model as a function of the doping level in $\text{Si}_{1-x}\text{Ge}_x$. The doping level was determined from Hall Effect measurements. The data is surprisingly well behaved and free of scatter. It is known that the Hall scattering factor can vary with both Ge and B concentrations. An average Hall scattering factor of 0.5 was used since the reported values are within 0.3 - 0.75 for Ge concentrations up to 40% and boron levels below 10^{20} cm^{-3} [21, 22].

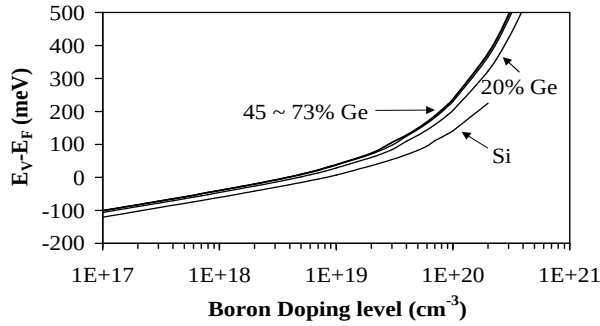


FIGURE 13. The position of the Fermi level with respect to the valence band edge calculated using the theoretical model in [20] as a function of the doping level determined from the Hall Effect measurements.

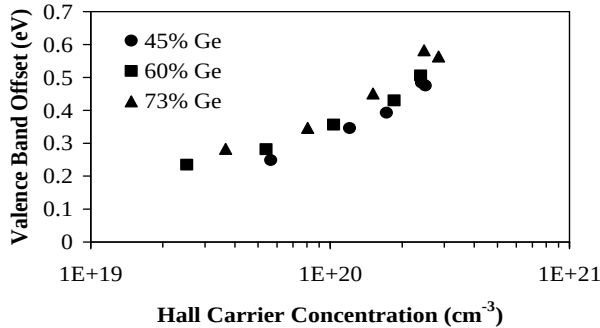


FIGURE 14. Valence band offset as a function of doping density calculated according to Eq. 4 and the model results in Figure 13

The calculations shown in Figure 14 should be corrected for second order effects. First, it is important

to note that at very high boron levels (i.e. several percent) the strain compensation is likely to change the $\text{Si}_{1-x}\text{Ge}_x$ bandgap and the band alignment. While this phenomenon has not been modelled yet, similar effects have been observed and modelled for carbon in $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ alloys [23, 24]. Because B and C atoms are comparable in size, a similar behavior should be expected for SiGeB. It has been shown that the band alignment in $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ /Si heterostructures stays $\text{Si}_{1-x}\text{Ge}_x$ -like since carbon incorporation is entirely accommodated in the valence band. It was found that the valence band off-set decreases by 20 - 26 meV/% for carbon concentrations in the range of 0 to 1.3%. The reduction is about 37 meV/% for higher carbon concentrations in the range of 1.3% to 2.5%. If we assume a similar effect with boron, a reduction of ~ 60 meV should be expected in the valence band off-set for concentrations less than 2% ($\sim 10^{21} \text{ cm}^{-3}$).

Another important impact of heavy boron doping on the band structure is bandgap narrowing, which has been reported for both Si and $\text{Si}_{1-x}\text{Ge}_x$ [25]. At a boron doping level of 10^{20} cm^{-3} , the silicon band gap is reduced more than 200 meV, which is a significant fraction of the silicon bandgap. For $\text{Si}_{1-x}\text{Ge}_x$, the bandgap narrowing is smaller for the same doping level, and it decreases slightly at higher Ge levels. As such, heavy boron doping has two effects on the $\text{Si}_{1-x}\text{Ge}_x$ bandgap: While strain compensation tends to increase the bandgap, heavy doping can cause bandgap narrowing. If we assume that the heavily doped $\text{Si}_{1-x}\text{Ge}_x$ alloys used in this study have about the same amount of bandgap narrowing as the $\text{Si}_{0.7}\text{Ge}_{0.3}$ films in [25], we can estimate the bandgap reduction to be at least around 160 meV. At the same time, if we assume that the strain compensation effect of boron is comparable to that of carbon, we estimate an increase of 100 meV in the bandgap.

The resulting valence band off-set including the corrections for the second order effects is plotted in Figure 15 as a function of the Ge concentration. Also shown is the theoretically predicted position of the valence band edge in fully relaxed $\text{Si}_{1-x}\text{Ge}_x$ and undoped, strained $\text{Si}_{1-x}\text{Ge}_x$ [26]. The combined effects of bandgap narrowing and strain compensation can be visualized by shifting the straight line for undoped strained $\text{Si}_{1-x}\text{Ge}_x$ upward by 100 meV. It can be seen in Figure 15 that majority of the data points are between the two extremes: fully relaxed undoped $\text{Si}_{1-x}\text{Ge}_x$ and heavily boron doped $\text{Si}_{1-x}\text{Ge}_x$ with bandgap narrowing and strain compensation. The data is suggestive of a good agreement between the experimental results and the analysis presented above. At low boron doping levels, $\text{Si}_{1-x}\text{Ge}_x$ films with high Ge concentrations can relax resulting in a bandgap close to that of Si. For films with about 45% Ge and higher boron doping, the valence band offset is around 0.45 eV yielding a $\text{Si}_{1-x}\text{Ge}_x$ bandgap of approximately

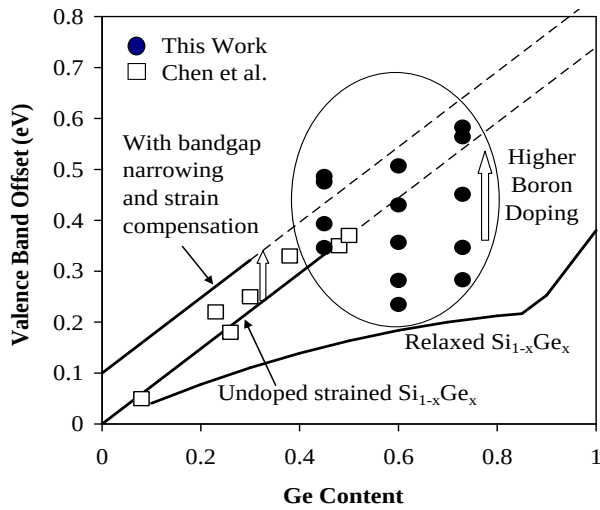


FIGURE 15. The valence band offset shown as a function of the Ge content. Solid circles are from this study and open squares for lower Ge concentrations are from [26].

0.67 eV. According to the above analysis, we estimate the $\text{Si}_{1-x}\text{Ge}_x$ bandgap to vary from 0.96 eV (fully relaxed $\text{Si}_{1-x}\text{Ge}_x$) with low boron doping levels to 0.68 eV (heavily doped strained $\text{Si}_{1-x}\text{Ge}_x$) with high boron doping levels. If we assume that Fermi level is pinning occurring at a fixed energy level relative to the conduction band, we expect a barrier height change of approximately 0.3 eV, which is significant according to eqn. 1. From Figure 5, one can see that an order magnitude improvement in contact resistivity can be obtained by a 0.3 eV reduction in barrier height for the same doping level.

LOCAL STRAIN

Another important advantage of using $\text{Si}_{1-x}\text{Ge}_x$ in the source/drain areas has recently been demonstrated by S. Thompson and his colleagues at Intel corporation [27]. They have shown that the $\text{Si}_{1-x}\text{Ge}_x$ junctions could be used to induce uniaxial compressive strain in the channel regions of small geometry MOSFETs to achieve mobility enhancement. This of course requires that the channel is narrow such that compressive strain can extend throughout the entire channel. It is claimed that the performance gain achieved with uniaxial strain is larger than that possible with conventional biaxial tensile strain and it can be maintained at high electric fields. Figure 16 shows the preferred type and direction of uniaxial channel strain to achieve enhanced carrier mobility in p-channel and n-channel transistors. It can be seen that for p-channel devices, compressive stress is needed along the longitudinal direction. On the other hand, for n-channel tran-

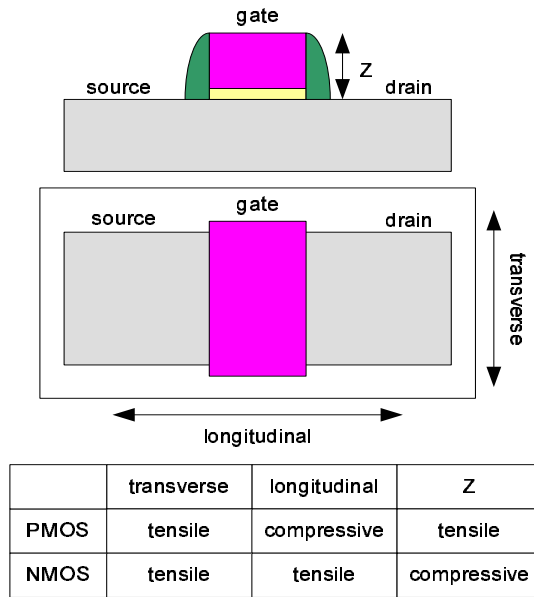


FIGURE 16. Type of the local strain needed by p-channel and n-channel transistors in different directions.

sistors, the stress must be tensile, which implies that the $\text{Si}_{1-x}\text{Ge}_x$ junctions cannot be used for mobility enhancement. As an alternative solution, Intel researchers chose to use a Si_3N_4 capping layer to introduce tensile strain in the channel.

Previous work from this laboratory has shown that low-resistivity $\text{NiSi}_{1-x}\text{Ge}_x$ contacts can also be formed on phosphorus doped $\text{Si}_{1-x}\text{Ge}_x$ alloys. A pressing question for future technology nodes is then to weigh the performance improvement due to reduced contact resistance against enhanced channel mobility. It is also possible to consider using the nitride gap with $\text{Si}_{1-x}\text{Ge}_x$ in the source/drain regions.

Many factors affect the channel strain including the channel length, channel width, Ge concentration, boron doping and $\text{Si}_{1-x}\text{Ge}_x$ depth. A curious question is the extendability of this approach to future CMOS nodes, since the recess depth and the $\text{Si}_{1-x}\text{Ge}_x$ thickness are to be scaled with the junction depth. Another question is the defects that form at the relaxed $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ interface and their location relative to the Si channel and the junction depletion region. The defects can play an important role in relaxing the lattice strain as well as serving as generation sites resulting in excessive junction leakage. More work is necessary to understand the impact of these parameters on mobility enhancement and source/drain quality. Finally, the contact metal can also have an impact on the channel strain. For instance, NiSi results in tensile strain, which can shadow the compressive strain obtained

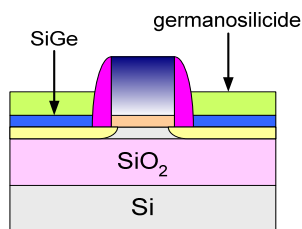


FIGURE 17. Ultrathin SOI MOSFET with elevated $\text{Si}_{1-x}\text{Ge}_x$ contacts.

from $\text{Si}_{1-x}\text{Ge}_x$. This may require the $\text{Si}_{1-x}\text{Ge}_x$ thickness to be considerably more than the recess depth to keep the channel sufficiently away from the contact metal.

SILICON-ON-INSULATOR MOSFETS

MOSFETs with ultrathin silicon-on-insulator (SOI) channels promise important advantages for future technology nodes. Different integration schemes are currently being considered including those that combine advantages of SOI with the enhanced mobility of strained silicon channels. A particularly interesting approach involves the transfer of an ultrathin strained silicon layer on a $\text{Si}_{1-x}\text{Ge}_x$ buffer to a handle wafer by wafer bonding [28].

The source/drain challenges of the bulk MOSFET are present for the ultrathin SOI structures as well. Additionally, we have the challenge of forming the junctions in an ultrathin Si layer with reliable, low-resistivity contacts. The primary challenge is that unless the junctions are elevated by selective epitaxy of a sacrificial Si or $\text{Si}_{1-x}\text{Ge}_x$ layer, the silicide contact has to consume the entire Si layer. Unfortunately, this limits the silicide/silicon contact area to the cross-sectional area of the channel significantly increasing the contact resistance. By using a sacrificial layer, the original contact area can be preserved. If $\text{Si}_{1-x}\text{Ge}_x$ is used to elevate the junctions as shown in Figure 17, it can also provide enhanced dopant activation and a small barrier height to achieve a smaller contact resistance, which is again a critical challenge for this structure. It is also possible to consider using an in-situ doped $\text{Si}_{1-x}\text{Ge}_x$ layer as a diffusion source to form the extension junctions. Finally, it is plausible that the elevated $\text{Si}_{1-x}\text{Ge}_x$ junctions can induce compressive stress in the channel region.

FINFET

Another promising structure for future technology generations is the FINFET, which can be used in double or

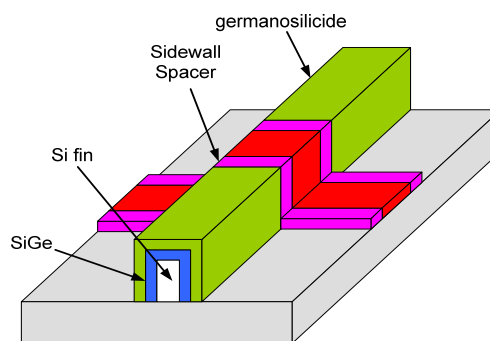


FIGURE 18. FINFET with elevated $\text{Si}_{1-x}\text{Ge}_x$ source/drain junctions

tri-gate configurations [29]. While the FINFET has the potential to boost the current drive, the source/drain parasitic resistance, which can severely limit its performance should be addressed. FINFET source/drain integration suffers from the same problem mentioned in the previous section for the ultrathin body MOSFET. Basically, the Si fin is so thin that formation of a silicide contact consumes the entire fin reducing the contact area to the cross-sectional area of the fin. The logical solution to this problem is to increase the thickness of the fin by selective deposition of a sacrificial layer. The resulting structure can be viewed as an elevated source/drain FINFET. This approach was implemented in a recent study at IBM using selective Si epitaxy [30]. It should also be possible to use $\text{Si}_{1-x}\text{Ge}_x$ instead of Si to lower the contact resistance and possibly to introduce compressive strain into the Si channel as discussed in the previous section.

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