

Scalability of the $\text{Si}_{1-x}\text{Ge}_x$ Source/Drain Technology for the 45-nm Technology Node and Beyond

Geert Eneman, Peter Verheyen, Rita Rooyackers, Faran Nouri, *Senior Member, IEEE*, Lori Washington, Robert Schreutelkamp, Victor Moroz, Lee Smith, *Member, IEEE*, An De Keersgieter, Malgorzata Jurczak, and Kristin De Meyer, *Senior Member, IEEE*

Abstract—The authors present a study on the layout dependence of the silicon-germanium source/drain ($\text{Si}_{1-x}\text{Ge}_x$ S/D) technology. Experimental results on $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors with various active-area sizes and polylengths are combined with stress simulations. Two technologically important configurations are investigated: the nested transistor, where a polygate is surrounded by other gates, and isolated transistors, where the active area is completely surrounded by isolation oxide. The channel stress, caused by epitaxial $\text{Si}_{1-x}\text{Ge}_x$ is reduced substantially when the active area is decreased from a large size towards typical values for advanced CMOS technology nodes. Nested transistors with longer gate lengths are more sensitive towards layout scaling than shorter gates. Increasing recess depth and germanium concentration gives larger channel stress, but does not change layout sensitivity. Increased lateral etching leads to higher stress, as well as to reduced layout sensitivity. In small-size transistors, there exists an optimal recess depth, beyond which the stress in the channel will not increase further. For isolated transistor structures, the interaction between $\text{Si}_{1-x}\text{Ge}_x$ and the isolating oxide can even lead to stress reduction when the recess depth is increased. When technology advances, active-area dimensions will be scaled together with gate lengths and widths. For typical sizes of advanced silicon CMOS $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors, simulations indicate that the channel stress can be maintained in future technology nodes.

Index Terms—MOSFET, SiGe, strained-silicon.

I. INTRODUCTION

ADVANCED silicon MOSFET technology relies heavily on the use of strained-silicon to boost the performance of both nMOS and pMOS transistors [1]–[14], since mechanical stress in a strained-silicon channel can significantly improve the conduction properties of holes and electrons inside the inversion layer. One of the most successful techniques for pMOS performance enhancement is the silicon-germanium

source/drain ($\text{Si}_{1-x}\text{Ge}_x$ S/D) transistor, where the silicon of the S/D regions is etched, and epitaxially refilled with $\text{Si}_{1-x}\text{Ge}_x$. Typical Ge concentrations lie around 20%. The lattice mismatch between $\text{Si}_{1-x}\text{Ge}_x$ and silicon creates a large stress inside the transistor channel. Previous studies indicate that this stress translates linearly into mobility increase, while for large stress values, the stress-mobility relation even becomes super-linear [15], [16]. Moreover, $\text{Si}_{1-x}\text{Ge}_x$ S/D reduces the S/D resistance substantially [5], [13], [17]. This combined effect gives large performance improvements for pMOS transistors [1], [9], [13], [14].

The performance of $\text{Si}_{1-x}\text{Ge}_x$ S/D pMOSFETs is mostly measured on single transistors, i.e., isolated structures with a large active area. When the $\text{Si}_{1-x}\text{Ge}_x$ S/D technique is used in advanced silicon technologies, however, the active-area size will be significantly smaller than on single transistors, which may reduce the stress in the channel [2], [7], [18]. In this paper, the impact of active-area dimensions, channel length, S/D recess depth, germanium concentration, and $\text{Si}_{1-x}\text{Ge}_x$ -to-channel distance on the stress introduced inside the channel is investigated using experimental results on state-of-the-art $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors, combined with stress simulations.

II. EXPERIMENTAL CONDITIONS

PMOS transistors were fabricated with standard CMOS processing conditions, including a 1.4-nm equivalent oxide thickness (EOT) SiON gate dielectric and 100-nm polysilicon gate. Transistors with a gate length down to 45 nm were obtained. After highly doped drain (HDD) implants and activation anneal, the S/D areas were etched back by either 70 or 120 nm, and epitaxially refilled up to 40 nm above the original level with B-doped $\text{Si}_{0.8}\text{Ge}_{0.2}$, reaching B levels up to $1 \times 10^{20} \text{ cm}^{-3}$. The etch and regrowth parameters were tuned to be independent of the active-area sizes under consideration (Fig. 1). Standard nickel silicidation and Cu backend concluded the processing [7], [9]. The $\text{Si}_{1-x}\text{Ge}_x$ S/D performance improvement of large-active-area transistors with 120-nm recess is 65% at $I_{\text{OFF}} = 10^{-7} \text{ A}/\mu\text{m}$, as compared to reference transistors (Fig. 2). For 70-nm recess, the $I_{\text{ON}}/I_{\text{OFF}}$ improvement was found to be 40%.

To investigate the scalability of the $\text{Si}_{1-x}\text{Ge}_x$ S/D technology, dedicated transistor structures have been analyzed, which will be termed “isolated” and “nested” transistors further on. The isolated structure [Fig. 3(a)] is a transistor surrounded by

Manuscript received February 28, 2006; revised April 19, 2006. The review of this paper was arranged by Editor C. Y. Lu.

G. Eneman is with the Interuniversity Microelectronics Center (IMEC), 3001 Leuven, Belgium. He is also with the Electrical Engineering Department (ESAT), Integrated System (INSYS) division of Katholieke Universiteit Leuven (KUL), Belgium and Fund for Scientific Research, Flanders, Belgium.

P. Verheyen, R. Rooyackers, A. De Keersgieter, and M. Jurczak are with the Interuniversity Microelectronics Center (IMEC), 3001 Leuven, Belgium.

F. Nouri, L. Washington, and R. Schreutelkamp are with the Applied Materials, Sunnyvale, CA 94086 USA.

V. Moroz and L. Smith are with Synopsys, Mountain View, CA 94043 USA.

K. De Meyer is with Interuniversity Microelectronics Center (IMEC), 3001 Leuven, Belgium. She is also with the Electrical Engineering Department (ESAT), Integrated System (INSYS) division of Katholieke Universiteit Leuven (KUL), 3001 Leuven, Belgium.

Digital Object Identifier 10.1109/TED.2006.876390

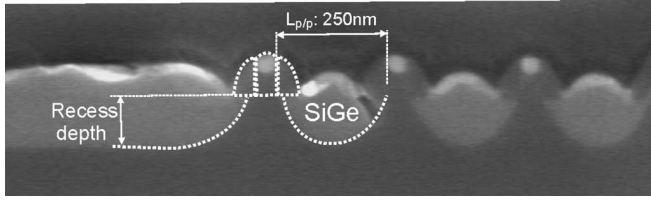


Fig. 1. Cross section SEM image of a $\text{Si}_{1-x}\text{Ge}_x$ S/D transistor structure with an etch depth of 120 nm. The recess etch was optimized to be independent of layout dimensions. At $L_{p/p} = 250$ nm, a small decrease in etch depth can be measured. The smallest dimension that is electrically evaluated is considerably larger ($L_{p/p} = 500$ nm).

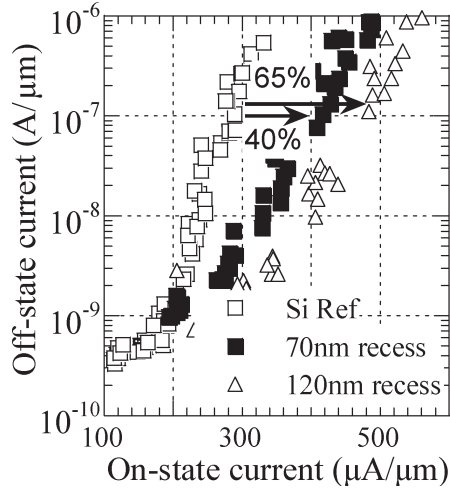


Fig. 2. I_{ON}/I_{OFF} plot ($|V_{dd}| = 1$ V) of $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors with 120-nm recess, 70-nm recess, and coprocessed reference transistors. Wide transistors were measured ($W = 10$ μm) with large-active-area dimensions ($L_{s/d} = 10$ μm).

shallow trench isolation (STI), where the S/D length $L_{s/d}$ is varied. In the nested transistor structure [Fig. 3(b)], the gate is surrounded by identical gates. In this case, the poly-to-poly length $L_{p/p}$ is varied. All measured isolated and nested transistors in this paper have a width of 10 μm . $L_{s/d}$ and $L_{p/p}$ vary between 10 μm and 500 nm. In advanced CMOS technologies, however, the specifications for the minimal $L_{s/d}$ and $L_{p/p}$ are considerably smaller than 500 nm. Typical values for the minimal $L_{s/d}$ and $L_{p/p}$ in the 45-nm technology node are 150 and 100 nm, respectively. To estimate the effectiveness of the $\text{Si}_{1-x}\text{Ge}_x$ S/D technology at these small feature sizes, Taurus-Process stress-simulations of $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors have been done [19]. This allows to extrapolate the experimental results to active-area sizes that are used in advanced chip design.

III. RESULTS

A. Experimental Results

On short-channel length transistors, mobility extraction is a nontrivial task. Different techniques to extract mobility on short channel lengths exist, but are hampered by metrology issues and the assumptions made by the technique. Therefore, the maximum linear transconductance is preferred in this case

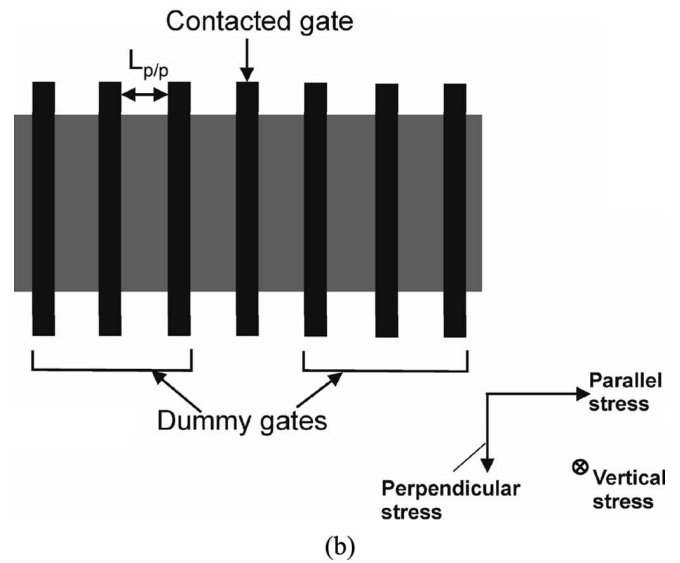
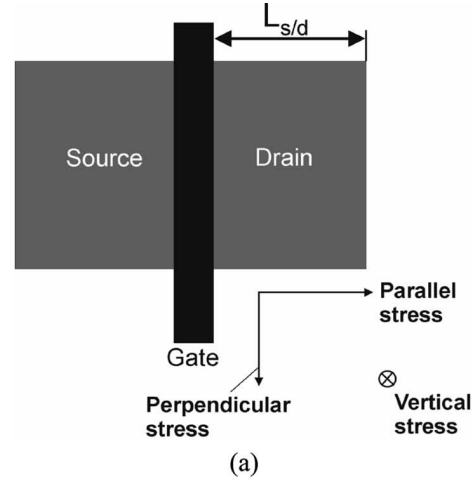


Fig. 3. Top-view drawing of the transistors of this experiment: (a) isolated structure and (b) nested transistor structure. The directions of the parallel, vertical and perpendicular stresses are indicated.

as a parameter to experimentally verify the effect of active-area scaling on $\text{Si}_{1-x}\text{Ge}_x$ S/D improvements in an easy way. It should be noted that the thermal budget of the $\text{Si}_{1-x}\text{Ge}_x$ S/D epiprocess may slightly alter the doping profiles, leading to other effective gate lengths as compared to reference devices. As a consequence, the absolute values of the g_m improvements in Figs. 4 and 6 should be interpreted with care. However, these L_{eff} variations will not affect the behavior of the performance versus active-area size. The g_m improvement for a certain active-area length is measured versus that of silicon reference transistors with the same active-area length. This is done to compensate for active-area-dependent variations other than $\text{Si}_{1-x}\text{Ge}_x$ S/D stress, such as polylength variations for small $L_{p/p}$ s in the case of nested transistors.

Part of the g_m improvement of the $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors should be attributed to a reduced series resistance. The dR/dL method was used to estimate the series resistance and a first-order model was employed to calculate the effect of series resistance on the transconductance. We estimate that less than 20% of the transconductance improvement is caused

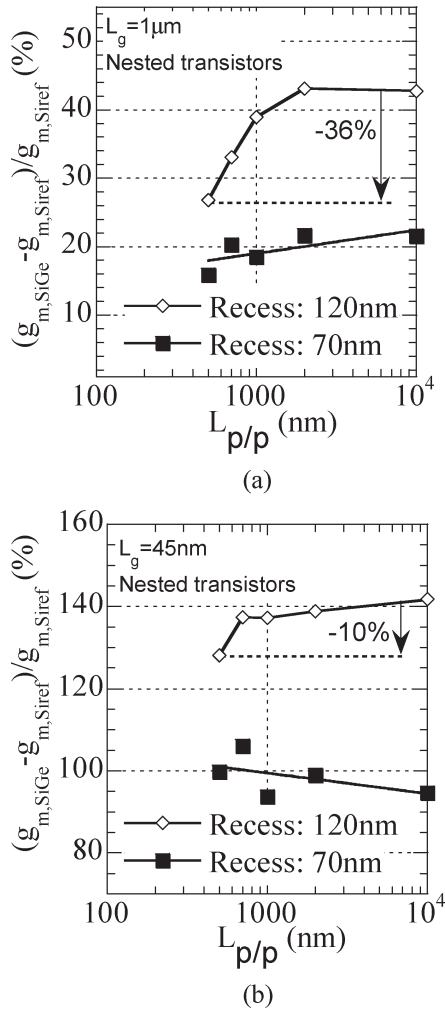


Fig. 4. Maximum transconductance improvement ($|V_D| = 100$ mV) of $\text{Si}_{1-x}\text{Ge}_x$ S/D nested transistors, over reference transistors with the same mask length and $L_{p/p}$, versus poly-to-poly length. (a) Transistors with a gate length of $1 \mu\text{m}$. (b) Transistors with a gate length of 45 nm. The arrow indicates the relative reduction of the g_m improvement with respect to long active-area devices for transistors with 120-nm recess.

by series-resistance changes for a polylength of 45 nm. For a $1\text{-}\mu\text{m}$ polylength, the effect of series resistance on g_m is much smaller, and is estimated to be below 2%. This shows that the transconductance improvements in Figs. 4 and 6 are mainly caused by mechanical stress effects. Therefore, the g_m improvement as a function of $L_{s/d}$ or $L_{p/p}$ is useful to study active-area scaling of $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors.

A transistor with a large active area has a large amount of epitaxial $\text{Si}_{1-x}\text{Ge}_x$ stressor in the source and drain areas. The compressive parallel stress created in the channel, combined with the effect of a reduced S/D resistance leads to an improved g_m for $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors. For a channel length of $1 \mu\text{m}$, nested $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors with an $L_{p/p}$ of $10\text{-}\mu\text{m}$ and 120-nm recess show more than 40% higher g_m than transistors without $\text{Si}_{1-x}\text{Ge}_x$ S/D [Fig. 4(a)]. For 70-nm recess, the improvement over transistors without $\text{Si}_{1-x}\text{Ge}_x$ S/D is around 20% [Fig. 4(a)]. Scaling the channel length brings the $\text{Si}_{1-x}\text{Ge}_x$ stressor closer together, which increases the stress. Therefore, the improvement is much larger for short channels [Fig. 4(b)].

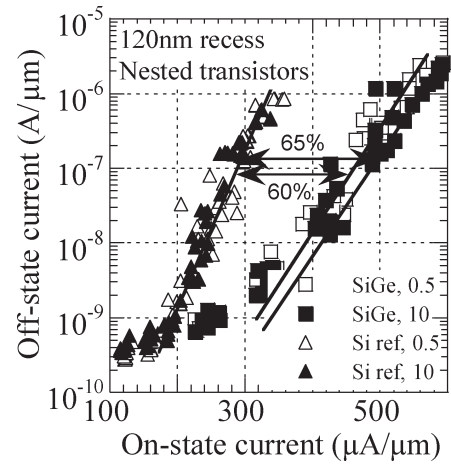


Fig. 5. $I_{\text{ON}}/I_{\text{OFF}}$ plot ($|V_{\text{dd}}| = 1$ V) of $\text{Si}_{1-x}\text{Ge}_x$ S/D and reference nested transistor structures with an $L_{p/p}$ of $10 \mu\text{m}$ and 500 nm . Transistor width is $10 \mu\text{m}$.

Scaling down the poly-to-poly length in nested transistors decreases the relative amount of $\text{Si}_{1-x}\text{Ge}_x$ stressor material, and therefore the stress decreases for smaller $L_{p/p}$ s. For long channel lengths [Fig. 4(a)], reducing the poly-to-poly lengths from $10 \mu\text{m}$ to 500 nm results in a transconductance improvement decrease from 42% to 27% for the largest recess depth, which means that 36% of the long active-area improvement is lost at $L_{p/p} = 500 \text{ nm}$. The trend line is not clear for the shallower recess depth. For short channel lengths, the behavior is qualitatively the same, although less reduction is seen [Fig. 4(b)]: For 120-nm recess, only 10% of the improvement is lost when $L_{p/p}$ scales from $10 \mu\text{m}$ to 500 nm . Fig. 5 shows the $I_{\text{ON}}/I_{\text{OFF}}$ performance for nested $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors with 120-nm recess and nested reference transistors for two poly-to-poly lengths. The effect of scaling $L_{p/p}$ from $10 \mu\text{m}$ to 500 nm results in a saturation I_{ON} improvement reduction by 5% at $I_{\text{OFF}} = 1 \times 10^{-7} \text{ A}/\mu\text{m}$.

Isolated transistors with an $L_{s/d}$ of $10 \mu\text{m}$ show about the same g_m increase over transistors without $\text{Si}_{1-x}\text{Ge}_x$ as nested transistors with a large active area [Fig. 6(a) and (b)]. Reducing the active-area length in isolated transistors has a much more pronounced effect than in nested transistors. For long channel lengths [Fig. 6(a)], scaling $L_{s/d}$ from $10 \mu\text{m}$ to 500 nm reduces the transconductance gain from 43% to 19% for 120-nm recess, and from 22% to 10% for 70-nm recess. This is a reduction of the performance gain by more than 50% in both cases. As in nested transistors, the transconductance loss is less severe for a shorter channel length [Fig. 6(b)], but is still 25% for the deepest recess etch and 13% for the shallower etch. The $I_{\text{ON}}/I_{\text{OFF}}$ performance gain for isolated $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors with 120-nm recess reduces by 10% when $L_{s/d}$ is reduced to 500 nm (Fig. 7).

In summary, reducing the active-area dimension $L_{p/p}$ or $L_{s/d}$ leads to a decrease of the performance in $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors. This decrease is worse for longer channel lengths. Isolated structures seem to be more sensitive to layout variations than nested structures. $I_{\text{ON}}/I_{\text{OFF}}$ performance decreases when scaling the active-area lengths from $10 \mu\text{m}$ to 500 nm . To estimate the effectiveness of the $\text{Si}_{1-x}\text{Ge}_x$ S/D technology

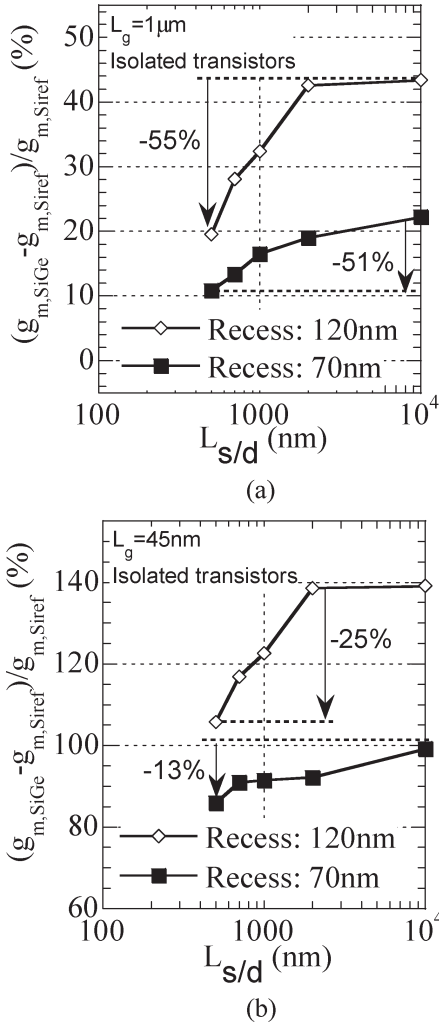


Fig. 6. Maximum transconductance improvement ($|V_{dd}| = 100$ mV) of $Si_{1-x}Ge_x$ S/D isolated transistors, over reference transistors with the same mask length and $L_{s/d}$, versus S/D length. (a) Transistors with a gate length of $1 \mu m$. (b) Transistors with a gate length of 45 nm. The arrow indicates the relative reduction of the g_m improvement with respect to long active-area devices.

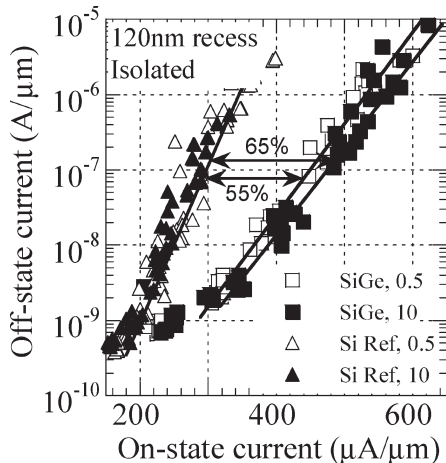


Fig. 7. I_{ON}/I_{OFF} plot ($|V_{dd}| = 1$ V) of $Si_{1-x}Ge_x$ S/D and reference isolated transistor structures with an $L_{s/d}$ of $10 \mu m$ and 500 nm. Transistor width is $10 \mu m$.

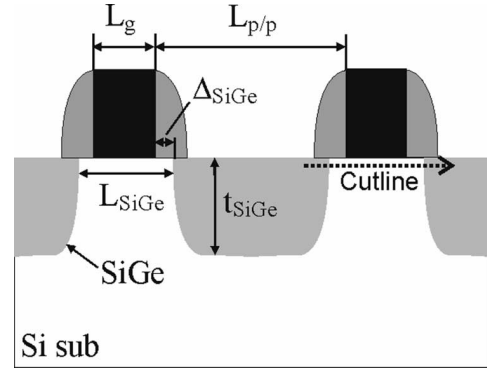


Fig. 8. Schematic cross section of a nested $Si_{1-x}Ge_x$ S/D transistor structure.

for structures with very small active-area dimensions, stress simulations are used and are shown in the next sections.

B. Simulation of Layout Sensitivity in Nested Transistors

Stress simulations have been performed using the Taurus-Process software from Synopsys [19]. The simulations have been done for industry standard (100)/ $\langle 110 \rangle$ transistors, with 100-nm polyheight and 30-nm-wide nitride spacers. Epitaxial $Si_{1-x}Ge_x$ S/D deposition was simulated with 20-nm overgrowth above the original Si surface. Two-dimensional (2-D) simulations have been performed to simulate the effect of $L_{p/p}$ and $L_{s/d}$ with a plane-strain boundary condition in the perpendicular direction (see Fig. 3), making the results valid for wide transistors. Epitaxial $Si_{1-x}Ge_x$ in S/D regions causes a large compressive stress parallel in the channel. The vertical and perpendicular stress (directions shown in Fig. 3) are tensile and compressive, respectively, and are typically less than 30% of the parallel stress in absolute value. Therefore, the parallel stress will be the main focus of this paper. For long channel lengths, the parallel stress varies along the transistor channel, resulting in a higher compressive stress at the edges of the channel and a lower stress level at the channel center. At which channel position the stress is most important for the conduction improvement is a nontrivial question, and will be dependent on transistor sizes, as well as on applied voltages. Therefore, we focus on parallel stress that is averaged along the transistor channel.

In nested transistors, important parameters that determine the amount of stress introduced in the channel by $Si_{1-x}Ge_x$ S/D are the germanium concentration, the poly-to-poly length $L_{p/p}$, the etch depth t_{SiGe} , and the $Si_{1-x}Ge_x$ separation L_{SiGe} , as shown in Fig. 8. L_{SiGe} scales with the gate length L_g

$$L_{SiGe} = L_g + 2\Delta_{SiGe} \quad (1)$$

Δ_{SiGe} is the $Si_{1-x}Ge_x$ -to-channel distance. It is dependent on the S/D-etch conditions and spacer width. It does not depend on L_g .

When the poly-to-poly length of a nested transistor is increased for a fixed gate length, the relative amount of $Si_{1-x}Ge_x$ stressor increases, which will lead to a higher channel stress. The maximum stress will be obtained for infinite $L_{p/p}$. On the other side, when $L_{p/p}$ decreases to zero, the stress will

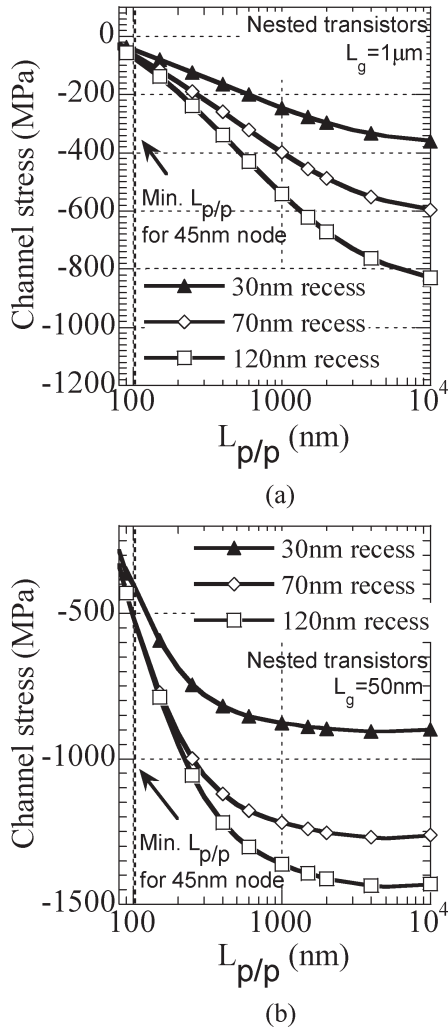


Fig. 9. Simulated channel stress versus $L_{p/p}$ in nested $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors with (a) a channel length of $1 \mu\text{m}$ and (b) a channel length of 50 nm . Simulations are valid for wide transistors. The stresses are averaged over the transistor channel. Δ_{SiGe} is equal to 25 nm and the S/D germanium concentration is 20%.

decrease accordingly, since the amount of $\text{Si}_{1-x}\text{Ge}_x$ to induce stress will diminish. This can be seen when the channel stress in nested transistors is plotted versus $L_{p/p}$ (Fig. 9). Negative stress values indicate compressive stress, positive stress values are tensile. In the case of a long channel length [Fig. 9(a)], the average channel stress decreases to zero when the poly-to-poly length is scaled down, while stress saturation starts only for $L_{p/p}$ s above $5 \mu\text{m}$. Reducing the recess depth decreases the stress in the channel, but leads to similar layout sensitivity: when $L_{p/p}$ reduces from $10 \mu\text{m}$ to 100 nm , the stress reduction is around 90% for every recess depth. For short gate lengths [Fig. 9(b)], the stress inside the channel is much larger than for long gate lengths. Moreover, the stress saturates in this case at a much shorter distance, around an $L_{p/p}$ of 500 nm , indicating that transistors with a short channel length are less sensitive to layout variations. When $L_{p/p}$ decreases from $10 \mu\text{m}$ to 100 nm , the stress reduction is 65% for 120-nm recess depth and 55% for 30-nm recess.

The measurement results of Fig. 4(a) and (b) were obtained on nested structures with a minimal $L_{p/p}$ of 500 nm . For

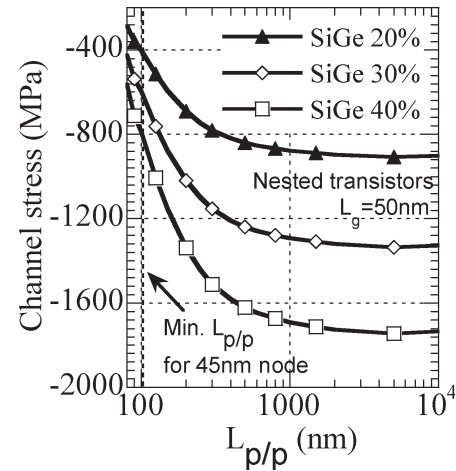


Fig. 10. Simulated channel stress versus $L_{p/p}$ in nested $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors with a recess depth of 30 nm for different $\text{Si}_{1-x}\text{Ge}_x$ S/D germanium concentrations. The stresses are averaged over the transistor channel. Δ_{SiGe} is equal to 25 nm .

an $L_{p/p}$ decrease from $10 \mu\text{m}$ to 500 nm , the stress simulations (Fig. 9) predict 35% reduction in parallel stress for $L_{\text{gate}} = 1 \mu\text{m}$ and 120-nm-recess depth [Fig. 9(a)]. For $L_{\text{gate}} = 50 \text{ nm}$, a stress reduction of 12% is predicted [Fig. 9(b)]. These values are in good qualitative agreement with the relative g_m reductions that are measured experimentally [36% and 10%, Fig. 4(a) and (b)].

Deeper S/D recess and shorter gate lengths will increase the stress created in the nested transistor channel, as shown in Fig. 9(a) and (b). Moreover, shorter gate lengths will decrease the layout sensitivity. In CMOS technology, however, the minimal gate length will be fixed for a given technology node. Increasing the S/D recess etch depth, on the other hand, can cause increased bulk leakage [9]. Leakage control is expected to limit the maximum $\text{Si}_{1-x}\text{Ge}_x$ recess depth more and more in next technology nodes, by requiring that the S/D recess is shallower than the depth of the HDD junction. There exist, however, other options to increase the channel stress further than scaling the gate length and increasing recess depth. One of these options is to use higher germanium concentrations in the S/D area. It is shown in Fig. 10 that a higher channel stress can be obtained when the $\text{Si}_{1-x}\text{Ge}_x$ S/D concentration is increased to 30% or 40%. The layout dependence, however, does not change: About 55% stress reduction occurs for all germanium concentrations when $L_{p/p}$ is scaled from $10 \mu\text{m}$ to 100 nm . The maximum germanium concentration to be used is limited by the defects generated in the layers, and the maximum leakage that can be allowed.

Another option to create higher stress is to decrease Δ_{SiGe} from (1) by decreasing the spacer width or increasing the isotropy of the S/D etch. In this way, the $\text{Si}_{1-x}\text{Ge}_x$ S/D separation L_{SiGe} can be scaled even when the polylength is fixed. Bringing the $\text{Si}_{1-x}\text{Ge}_x$ closer together leads to higher stress (Fig. 11), as well as to a reduced sensitivity: While the stress decrease is 55% for an L_{SiGe} of 100 nm when $L_{p/p}$ is scaled from $10 \mu\text{m}$ to 100 nm , this reduction is only 30% for an L_{SiGe} of 50 nm . Decreasing Δ_{SiGe} requires a good control over the etch conditions to keep leakage and yield acceptable.

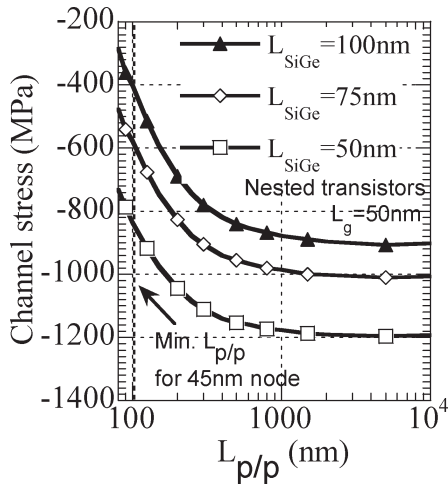


Fig. 11. Simulated channel stress versus $L_{p/p}$ in nested $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors with a recess depth of 30 nm for different $\text{Si}_{1-x}\text{Ge}_x$ separations L_{SiGe} (see Fig. 8). The stresses are averaged over the transistor channel. L_g is equal to 50 nm and the S/D germanium concentration is 20%.

C. Simulation of Layout Sensitivity in Isolated Transistors

To simulate the isolated transistor structure, a 350-nm-deep STI with high-density plasma oxide deposition at 700 °C was included in the simulation flow. The STI oxide introduces around 250 MPa extra compressive stress in the channel direction for $L_{s/d} = 150$ nm and a gate length of 50 nm. Due to the higher complexity of the isolated structure, S/D lengths were limited to a maximum of 1 μm in the stress simulations. The channel stress is shown as a function of $L_{s/d}$ in Fig. 12 for $L_g = 1 \mu\text{m}$ and $L_g = 50$ nm. Whereas in nested transistors, a deeper recess etch always gives a higher channel stress, this is not the case for isolated structures. This difference can be explained by the impact of the STI oxide in isolated structures. Silicon dioxide is much softer than silicon and has a Young's modulus that is about three times smaller than that of crystalline silicon. Therefore, the presence of the STI oxide close to the transistor will allow for much more stress relaxation of the $\text{Si}_{1-x}\text{Ge}_x$ stressor, which will lead to a lower channel stress than in a nested structure. The highest stress field in isolated transistors can be found at the bottom of the $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer, where the $\text{Si}_{1-x}\text{Ge}_x$ is bound to the much stiffer silicon substrate (Fig. 13). Reducing the recess depth will bring this high-stress region closer to the channel, and will lead to a higher channel stress. This effect is expected to be more pronounced for short S/D lengths, where the STI oxide is much closer to the channel. Fig. 12(b) illustrates this effect. A recess depth of 30 nm gives higher stress levels than 120- or 70-nm recess for $L_{s/d}$ s below 300 and 200 nm, respectively. Contrary to nested transistors, isolated structures show dependence of layout sensitivity on recess depth: Scaling $L_{s/d}$ from 1 μm to 150 nm reduces the stress for the deepest recess etch by 50% and 60% for $L_g = 1 \mu\text{m}$ and 50 nm, respectively, while the reduction is only 25% and 34% (same considered gate lengths) for 30-nm-recess depth. In conclusion, a shallower recess etch is less sensitive towards layout variations, and can give higher channel stresses than deeper recess etches, depending on the recess etch conditions.

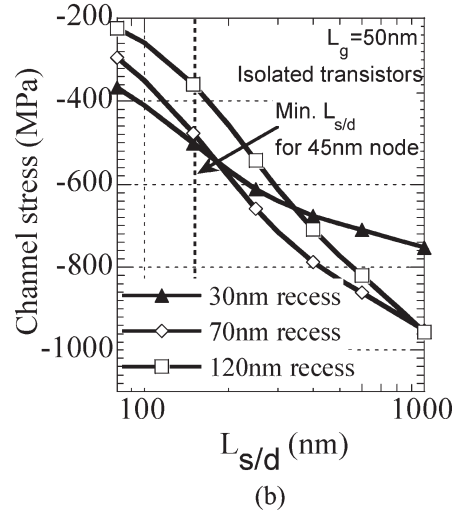
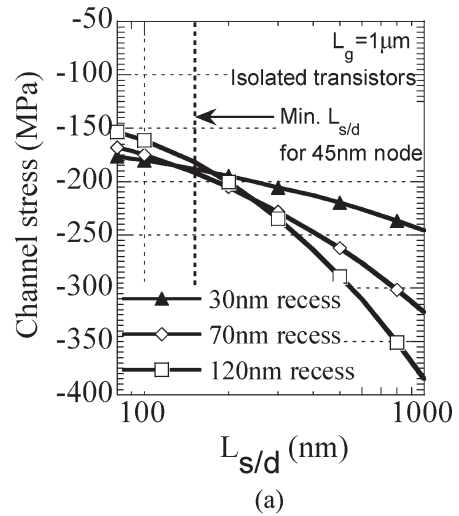


Fig. 12. Simulated channel stress versus $L_{s/d}$ in isolated $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors with (a) a channel length of 1 μm and (b) a channel length of 50 nm. Simulations are valid for wide transistors. The stresses are averaged over the transistor channel. Δ_{SiGe} is equal to 25 nm and the S/D germanium concentration is 20%.

Transistors with a small active area have a different stress sensitivity towards recess depth than those with a large active area, as is shown in Fig. 14(a) and (b). In large structures, etching deeper than 60 nm will increase channel stress further, especially in nested structures. However, when $L_{p/p}$ is decreased to 100 nm in nested transistors, etching deeper than 60 nm does not give extra stress [Fig. 14(a)]. Isolated structures with a small $L_{s/d}$ even show a maximum stress versus recess depth [Fig. 14(b)]. It seems that both for small nested and isolated structures an optimal etch depth exists, around 60 and 40 nm, respectively, beyond which no further stress improvement is obtained.

In the last two sections, we focused on the scaling of active-area lengths. Device widths will also be scaled in the next CMOS technologies. Narrow transistors have less $\text{Si}_{1-x}\text{Ge}_x$ material than wide structures, and the presence of the STI oxide on the transistor sides allows for further relaxation of the $\text{Si}_{1-x}\text{Ge}_x$. Therefore, the channel stress is expected to be lower for narrow transistors. To simulate the width effect,

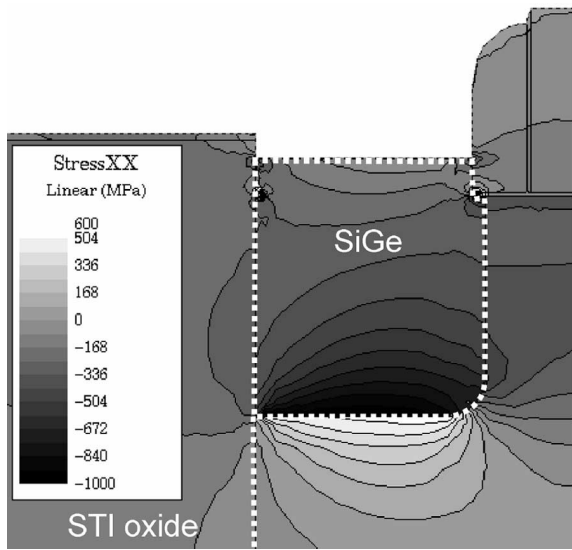


Fig. 13. Lateral stress contours of a $\text{Si}_{1-x}\text{Ge}_x$ S/D isolated transistor. $L_{s/d}$ is 150 nm, etch depth is 120 nm. At the bottom of the $\text{Si}_{1-x}\text{Ge}_x$ S/D region, the connection with the silicon substrate creates a large stress field. Higher in the epitaxial layer, where the $\text{Si}_{1-x}\text{Ge}_x$ is clamped between the silicon substrate and the isolation oxide, the stress values are much lower.

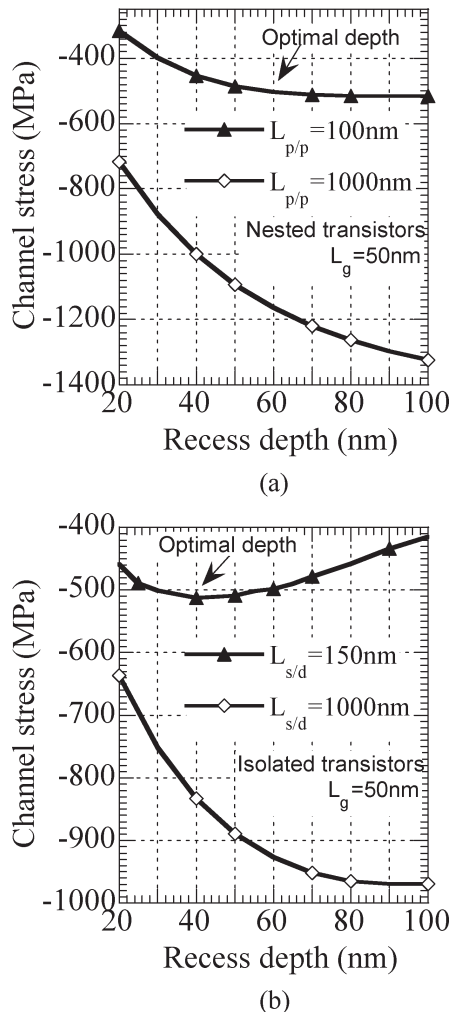


Fig. 14. Simulated channel stress as a function of recess depth for (a) nested and (b) isolated transistors. The stresses are averaged over the transistor channel. Δ_{SiGe} is equal to 25 nm and the S/D germanium concentration is 20%.

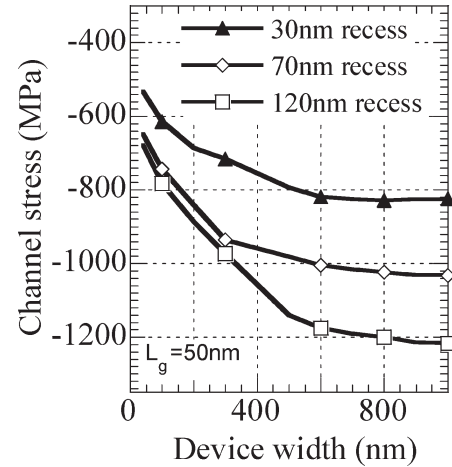


Fig. 15. Simulated channel stress versus device width in $\text{Si}_{1-x}\text{Ge}_x$ S/D transistors. Simulations were done for nested transistors with a large $L_{p/p}$. The stresses are averaged over the transistor channel. Δ_{SiGe} is equal to 25 nm and the S/D germanium concentration is 20%.

the three-dimensional (3-D) simulator capabilities of Taurus-Process were used. An example of the simulated width effect is shown in Fig. 15 for $L_g = 50$ nm. When the device width is scaled to 100 nm, the channel stress is reduced by more than 25% for all etch depths.

D. Is the $\text{Si}_{1-x}\text{Ge}_x$ S/D Technology Scalable?

The simulations done in the previous sections indicate that the stress introduced by $\text{Si}_{1-x}\text{Ge}_x$ S/D will depend nonlinearly on active-area length and width, as well as on etch depth and gate length. Until now, we focused on the separate variation of these parameters. When technology advances, the parameters discussed in the previous sections (L_g , $L_{p/p}$, $L_{s/d}$, and W) will be scaled in conjunction. As demonstrated in the previous sections, decreasing the active-area length and width reduces the channel stress, since the amount of $\text{Si}_{1-x}\text{Ge}_x$ stressor material is reduced. Decreasing the gate length, however, will bring the $\text{Si}_{1-x}\text{Ge}_x$ stressor regions closer together, which leads to an increase in stress. Therefore, the question rises whether $\text{Si}_{1-x}\text{Ge}_x$ channel stress will increase or not when all these dimensions are scaled down in the next technology nodes.

To estimate this, 3-D simulations have been performed on nested transistors, with typical dimensions for the 45-, 32-, and 22-nm technology node [20]. The parameters varied are shown in Table I. The results of these simulations are shown in Figs. 16 and 17. The stress along the channel (dotted line of Fig. 8) is shown in Fig. 16. At the edge of the silicon region, the stresses are larger for the technology with the largest $L_{p/p}$. In the center of the channel, however, the technology with the shortest gate length shows the highest stress. The stress averaged across the channel is shown in Fig. 17. Our simulations indicate that the stress inside the channel can be maintained and even increased slightly when the $\text{Si}_{1-x}\text{Ge}_x$ S/D technology is scaled according to the specifications given by the International Technology Roadmap for Semiconductors (ITRS) roadmap [20].

TABLE I
TECHNOLOGY PARAMETERS FOR THE 45-, 32-, AND 22-nm
TECHNOLOGY NODE

	$L_g(\text{nm})$	$L_{p/p}(\text{nm})$	$L_{\text{SiGe}}(\text{nm})$	$t_{\text{SiGe}}(\text{nm})$	$W(\text{nm})$
45nm node	18	100	50	60	100
32nm node	13	70	35	50	70
22nm node	9	50	24	45	50

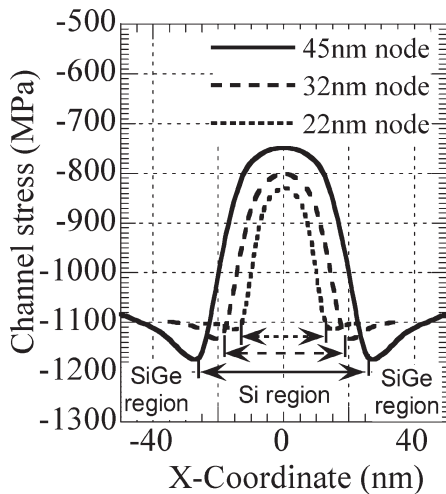


Fig. 16. Stress along the channel in nested transistors of the 45-, 32-, and 22-nm technology node (cutline shown in Fig. 8). Stresses shown are averaged along the width of the channel. The stress variation along the width is small (Variation < 50 MPa). X-coordinate 0 corresponds to the center of the channel. The S/D germanium concentration used was 20%.

IV. CONCLUSION

P-type transistor performance can be improved significantly when the S/D regions are recessed and epitaxially refilled with $\text{Si}_{1-x}\text{Ge}_x$. Saturation current improvements of 65% are measured on isolated transistors with short channel lengths and a large active area. The $\text{Si}_{1-x}\text{Ge}_x$ S/D technology is based on local stress creation, which makes the stress created by this technique dependent on active-area dimensions. Therefore, the performance that is measured on transistors with a large active area will give a serious overestimation when extrapolated to transistors in an actual design, i.e., with a small active-area length and width. Although the layout sensitivity of the $\text{Si}_{1-x}\text{Ge}_x$ S/D technology decreases for shorter channel lengths and lower recess depths in nested structures, the stress overestimation is large (> 30%) when $L_{p/p}$ is scaled to 100 nm, even for transistors with 50-nm gate length and a recess depth of only 30 nm. This will give serious additional challenges for the development of circuit modeling tools.

For a given technology node, several options exist to increase channel stress further: increasing recess depth and germanium concentration of the $\text{Si}_{1-x}\text{Ge}_x$ S/D allows for higher stress, but does not improve sensitivity. Decreasing the $\text{Si}_{1-x}\text{Ge}_x$ -to-channel distance will not only lead to higher stress, but also

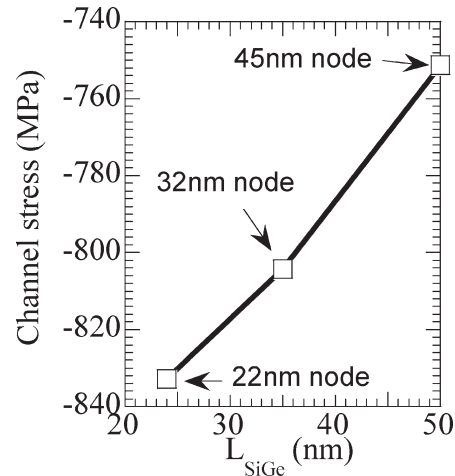


Fig. 17. Average channel stresses in $\text{Si}_{1-x}\text{Ge}_x$ S/D nested transistors of the 45-, 32-, and 22-nm technology node, showing an increase in stress when going to more advanced technologies. The value shown is the average stress in the silicon channel, measured 1 nm under the SiO_2 oxide. The S/D germanium concentration used was 20%.

to a reduced layout sensitivity. These options come at a price, however: increasing the recess depth may increase junction leakage when the recess is deeper than the HDD junction. Increasing the germanium concentration requires improved control of the epitaxial growth and subsequent processing to keep the amount of crystallographic defects acceptable. Finally, bringing the $\text{Si}_{1-x}\text{Ge}_x$ layer too close to the channel may cause problems with gate and OFF-state leakage. Etch and epitaxial growth conditions need to be controlled very well in this case to keep leakage and yield acceptable.

When a transistor is surrounded by isolation oxide (isolated transistors), the interaction between the $\text{Si}_{1-x}\text{Ge}_x$ stressor and the isolation oxide will lead to stress relaxation in the channel. This may lead to smaller channel stress for a deeper recess etch, dependent on active-area dimensions and etch shape.

For scaled nested and isolated transistors, there exists an optimal recess depth, beyond which the stress introduced will not increase further. This optimal recess depth decreases for shorter channel lengths.

Advanced technologies will feature decreasing active-area sizes, as well as shorter gate lengths. The question rises whether channel stress can be maintained in scaled technologies that feature epitaxial $\text{Si}_{1-x}\text{Ge}_x$ in the source and drain regions. Using typical values for transistor dimensions, according to CMOS technology nodes of the ITRS roadmap, stress simulations indicate that the $\text{Si}_{1-x}\text{Ge}_x$ S/D channel stress can be maintained and even increased for the next technology nodes.

REFERENCES

- [1] P. Ranade, T. Ghani, K. Kuhn, K. Mistry, S. Pae, L. Shifren, M. Stettler, K. Tone, S. Tyagi, and M. Bohr, "High performance 35 nm L_{gate} CMOS transistors featuring NiSi metal gate (FUSI), uniaxial strained silicon channels and 1.2 nm gate oxide," in *IEDM Tech. Dig.*, 2005, pp. 227–230.
- [2] A. Oishi, O. Fujii, T. Yokoyama, K. Ota, T. Sanuki, H. Inokuma, K. Eda, T. Idaka, H. Miyajima, S. Iwasa, H. Yamasaki, K. Oouchi, K. Matsuo, H. Nagano, T. Komoda, Y. Okayama, T. Matsumoto, K. Fukasaku, T. Shimizu, K. Miyano, T. Suzuki, K. Yahashi, A. Horiuchi, Y. Takegawa, K. Saki, S. Mori, K. Ohno, I. Mizushima,

- M. Saito, M. Iwai, S. Yamada, N. Nagashima, and F. Matsuoka, "High performance CMOSFET technology for 45 nm generation and scalability of stress-induced mobility enhancement technique," in *IEDM Tech. Dig.*, 2005, pp. 239–242.
- [3] M. Horstmann, A. Wei, T. Kammler, J. Höntschel, H. Bierstedt, T. Feudel, K. Froberg, M. Gerhardt, A. Hellmich, K. Hempel, J. Hohage, P. Javorka, J. Klais, G. Koerner, M. Lenski, A. Neu, R. Otterbach, P. Press, C. Reichel, M. Trentsch, B. Trui, H. Salz, M. Schaller, H. Engelmann, O. Herzog, H. Ruelke, P. Hübner, R. Stephan, D. Greenlaw, M. Raab, and N. Kepler, "Integration and optimization of embedded—SiGe, compressive and tensile stressed liner films, and stress memorization in advanced SOI CMOS technologies," in *IEDM Tech. Dig.*, 2005, pp. 243–246.
- [4] Z. Luo, Y. Chong, J. Kim, N. Rovedo, B. Greene, S. Panda, T. Sato, J. Holt, D. Chidambarrao, J. Li, R. Davis, A. Madan, A. Turansky, O. Gluschenkov, R. Lindsay, A. Ajmera, J. Lee, S. Mishra, R. Amos, D. Schepis, H. Ng, and K. Rim, "Design of high performance PFETs with strained Si channel and laser anneal," in *IEDM Tech. Dig.*, 2005, pp. 495–498.
- [5] P. Verheyen, G. Eneman, R. Rooyackers, R. Loo, L. Eeckhout, D. Rondas, F. Leys, J. Snow, D. Shamiryan, M. Demand, T. Y. Hoffmann, M. Goodwin, H. Fujimoto, C. Ravit, B.-C. Lee, M. Caymax, K. De Meyer, P. Absil, M. Jurczak, and S. Biesemans, "Demonstration of recessed SiGe S/D and inserted metal gate on HfO_2 for high performance pMOSFETs," in *IEDM Tech. Dig.*, 2005, pp. 907–910.
- [6] T. Ueno, H. Ree, S. Lee, H. Lee, D. Shin, Y. Jin, S. Maeda, and N. Lee, "Dramatically enhanced performance of recessed SiGe source-drain PMOS by in-situ etch and regrowth technique (INSERT)," in *VLSI Symp. Tech. Dig.*, 2005, pp. 24–25.
- [7] G. Eneman, P. Verheyen, R. Rooyackers, F. Nouri, L. Washington, R. Degraeve, B. Kaczer, V. Moroz, A. De Keersgieter, R. Schreutelkamp, M. Kawaguchi, Y. Kim, A. Samoilov, L. Smith, P. P. Absil, K. De Meyer, M. Jurczak, and S. Biesemans, "Layout impact on the performance of a locally strained PMOSFET," in *VLSI Symp. Tech. Dig.*, 2005, pp. 22–23.
- [8] S. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key differences for process-induced uniaxial vs. substrate-induced biaxial stresses Si and Ge channel MOSFETs," in *IEDM Tech. Dig.*, 2004, pp. 225–228.
- [9] F. Nouri, P. Verheyen, L. Washington, V. Moroz, I. De Wolf, M. Kawaguchi, S. Biesemans, R. Schreutelkamp, Y. Kim, M. Shen, X. Xu, R. Rooyackers, M. Jurczak, G. Eneman, K. De Meyer, L. Smith, D. Pramanik, H. Forstner, S. Thirupapuliyur, and G. Higashi, "A systematic study of trade-offs in engineering a locally strained pMOSFET," in *IEDM Tech. Dig.*, 2004, pp. 1055–1058.
- [10] H. Irie, K. Kita, K. Kyuno, and A. Toriumi, "In-plane mobility anisotropy and universality under uni-axial strains in n- and p-MOS inversion layers on (100), (110), and (111) Si," in *IEDM Tech. Dig.*, 2004, pp. 213–216.
- [11] S. Pidín, T. Mori, K. Inoue, S. Fukuta, N. Itoh, E. Mutoh, K. Okoshi, R. Nakamura, K. Kobayashi, K. Kawamura, T. Saiki, S. Fukuyama, S. Satoh, M. Kase, and K. Hashimoto, "A novel strained enhanced CMOS architecture using selectively deposited high tensile and high compressive silicon nitride films," in *IEDM Tech. Dig.*, 2004, pp. 213–216.
- [12] J. Cai, K. Kim, A. Bryant, K. Jenkins, C. Ouyang, D. Singh, Z. Ren, K. Lee, H. Yin, J. Hergenrother, T. Kanarsky, A. Kumar, X. Wang, S. Bedell, A. Reznicek, H. Hovel, D. Sadana, D. Uriarte, R. Mitchell, J. Ott, D. Mocuta, P. O'Meal, A. Mocuta, E. Leobandung, R. Miller, W. Haensch, and M. Leong, "Performance comparison and channel length scaling of strained Si FETs on SiGe-on-Insulator (SGOI)," in *IEDM Tech. Dig.*, 2004, pp. 165–168.
- [13] P. R. Chidambaram, B. A. Smith, L. H. Hall, H. Bu, S. Chakravarthi, Y. Kim, A. V. Samoilov, A. T. Kim, P. J. Jones, R. B. Irwin, M. J. Kim, A. L. P. Rotondaro, C. F. Machala, and D. T. Grider, "35% drive current improvement from recessed-SiGe drain extensions on 37 nm gate length PMOS," in *VLSI Symp. Tech. Dig.*, 2004, pp. 48–49.
- [14] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors," in *IEDM Tech. Dig.*, 2003, pp. 978–980.
- [15] L. Smith, V. Moroz, G. Eneman, P. Verheyen, F. Nouri, L. Washington, M. Jurczak, O. Penzin, D. Pramanik, and K. De Meyer, "Exploring the limits of stress-enhanced hole mobility," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 652–654, Sep. 2005.
- [16] L. Washington, F. Nouri, S. Thirupapuliyur, G. Eneman, P. Verheyen, V. Moroz, L. Smith, X. Xu, S. Kawaguchi, T. Huang, K. Ahmed, M. Balseanu, L. Xia, M. Shen, Y. Kim, A. Samoilov, R. Rooyackers, K. De Meyer, and R. Schreutelkamp, "PMOSFET with 200% enhancement induced by multiple stressors," *IEEE Electron Device Lett.*, submitted for publication.
- [17] M. Öztürk, J. Liu, and H. Mo, "Low resistivity nickel germanosilicide contacts to ultra-shallow $\text{Si}_{1-x}\text{Ge}_x$ source/drain junctions for nanoscale CMOS," in *IEDM Tech. Dig.*, 2003, pp. 497–500.
- [18] V. Moroz, G. Eneman, P. Verheyen, F. Nouri, L. Washington, L. Smith, M. Jurczak, and D. Pramanik, "The impact of layout on stress-enhanced PMOS performance," in *Proc. SISPAD*, 2005, pp. 143–146.
- [19] *Taurus TSUPREM*, *Taurus Process Reference Manual*, Oct. 2005. Version X-2005.10.
- [20] ITRS Roadmap for Semiconductors, ITRS 2005 Edition, Process Integration, Devices and Structures, *High Performance Logic Technology Requirements*. [Online]. Available: <http://public.itrs.net/>



Geert Eneman was born in Turnhout, Belgium, in 1979. He received the B.S. and M.S. degrees in electrical engineering from the Katholieke Universiteit Leuven (KUL), Leuven, Belgium, in 1999 and 2002, respectively. He is currently working toward the Ph.D. degree on the topic of strained-silicon transistors, at the Electrical Engineering Department (ESAT), Integrated System (INSYS) division of the KUL, Belgium.

He is a Researcher in the CMOS Device Research Department, Interuniversity Microelectronics Center, Leuven. Since 2002, he has been a Research Assistant of the Fund for Scientific Research, Flanders, Belgium. His current research interests include the technology, device integration, characterization, and modeling of strained-silicon transistors.



Peter Verheyen received the M.S. and Ph.D degree in electrical engineering from the Katholieke Universiteit Leuven (KUL), Belgium, in 1996 and 2003, respectively.

He did his doctoral research in the Interuniversity Microelectronics Center (IMEC), Leuven, Belgium where he is currently employed as a member of the Silicon Process and Device Technology (SPDT)/CMOS Device Research group. He is doing research on the effect of strain on device performance, from a processing and electrical characterization point of view.



Rita Rooyackers received the B.S. degree in industrial chemistry at the Rega Institute, Leuven, Belgium, in 1975, and followed the basics of very large scale integration (VLSI) processing of the postgraduate education program in Microelectronics Engineering (PMMS) at the Katholieke Universiteit Leuven (KUL).

From 1976 until 1984, she was working at the Electrical Engineering Department (ESAT) laboratory of the KUL in silicon technology development. In 1984, she joined the newly established research center Interuniversity Microelectronics Center, Leuven. She is currently with the Silicon Process and Device Technology (SPDT) division in the group Device Implementation Program (DIP), working in the field on deep submicrometer technology development and process integration of CMOS devices and finFETs. She is the coauthor of about 60 publications in those fields.



Faran Nouri (SM'00) received the M.S. degree in electrical engineering from the University of Colorado, Boulder, in 1984.

She is the Director of the Applications Development Center for the Frontend Products at Applied Materials. She has authored or coauthored over 50 technical papers and has been awarded eight patents.

Ms. Nouri has served as Cochair of the hot-carrier committee of International Reliability Physics Symposium (IRPS), has been a member of International Technology Roadmap for Semiconductors (ITRS) committees, and has served as a member of the technical committee for the very large scale integration (VLSI) Symposium. She is the Cochair of the Transistor Scaling Symposium at Materials Research Society (MRS) 2006.



Lori Washington received the B.S. and M.S. degrees in materials science from Stanford University, Stanford, CA.

She is currently a senior member of technical staff with Applied Materials, Sunnyvale, CA, where she works on Si- and SiGe-based epitaxy and the integration of SiGe into CMOS devices.



Robert Schreutelkamp received the Ph.D. degree in physics from University of Utrecht, The Netherlands, in 1991 and the MBA degree from Vlerick Management School, Belgium, in 2005.

He is a Technology Manager with Applied Materials, responsible for R&D activities at Interuniversity Microelectronics Center, Leuven, Belgium.



Victor Moroz received the Ph.D. degree in semiconductor physics from the University of Nizhny Novgorod, Russia, in 1992.

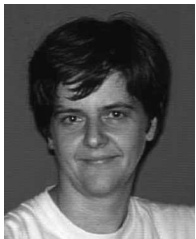
His professional career revolves around technology computer-aided design (TCAD) and includes silicon process integration in the industry, teaching undergraduate and graduate students, and for the last ten years, developing process simulation and design for manufacturability tools at the Technology Modeling Associates and the TCAD department at Synopsys. Several facets of this activity are reflected

in his more than 50 technical papers and more than 10 patents.



Lee Smith (M'89) received the B.S. degree from University of Florida, Gainesville, in 1989, and the Ph.D. degree from Stanford University, Stanford, CA, in 1997, all in physics.

In 1998, he joined the Technology Computer-Aided Design (TCAD) Department at Synopsys, Inc. as an R&D Engineer developing models and algorithms for numerical device simulation. He is currently a Staff R&D Engineer in the TCAD design for manufacturability Solutions Group at Synopsys engaged in model development for simulating advanced CMOS devices and addressing issues related to DFM.



An De Keersgieter received the M.S. degree in physics from the University of Ghent, Ghent, Belgium, in 1984.

In 1985, she joined Interuniversity Microelectronics Center (IMEC), Leuven, working on process modeling. She has been involved in modeling and simulation work for several European projects such as STORM, ADEQUAT, ACE, HUNT, ARTEMIS, and NANOCMOS. Currently, she is mainly focussing on process and device simulation and calibration of 65-nm and smaller CMOS technologies.

Among fields of interest are strain-engineering and multigate devices. She is a member of the CMOS Device Research Department, IMEC, Device Implementation Projects. She is also responsible for support of technology computer-aided design (TCAD) tools used at IMEC.

Ms. De Keersgieter has been a member of scientific committee for European Solid-State Device Research Conference (ESSDERC) conferences, since 2005 and 2006.



Malgorzata Jurczak received the M.Sc. and the Ph.D. degrees from the Warsaw University of Technology (WUT), Warsaw, Poland, in 1991 and 1997, respectively, both in electrical engineering.

In 1991, she joined WUT where she worked on modeling of MOS silicon-on-insulator (SOI) devices. In 1994, she was with National Microelectronics Research Centre (NMRC), Cork, Ireland, and with Kyung Hee University, Seoul, Korea, in 1997. In 1998, she joined CNET Grenoble, France Telecom. She was involved in development of 0.18 and

0.12 μm CMOS process and alternative approaches for sub-0.1- μm CMOS. In 2000, she joined Interuniversity Microelectronics Center (IMEC), Belgium, Leuven, Belgium. In 2000 to 2003, she was the IMEC Coordinator of the JDP program with Philips on device process integration for 90- and 65-nm CMOS. From 2003, she has been the Group Leader of the Device Implementation Projects in the CMOS department. She is also a project manager of IMEC Industrial Affiliated Program on FINFET devices. She has participated into several European projects: ACE, ULTRA, MEDEA, HUNT. She was the project coordinator of the European IST ARTEMIS project. Currently she is in the Technical Advisory Committee of the IST Integrated project Nano-CMOS. She holds 15 French and American patents, and authored and coauthored more than 60 papers. Since 2002 and 2003, she has been a member of scientific committees of International Electron Devices Meeting (IEDM) and, in 2000, 2004, and 2005, European Solid-State Device Research Conference (ESSDERC) conferences.

Dr. Jurczak received the Best Paper Award at the ESSDERC Conference in 2000 and the Paul Rappaport Award for the best paper published in IEEE TRANSACTIONS ON ELECTRON DEVICES in 2000.



Kristin De Meyer (S'73-M'85-SM'00) received the degree in electrical engineering and the Ph.D. degree from the Katholieke Universiteit Leuven (KU Leuven), Leuven, Belgium, in 1974 and 1979, respectively.

From November 1979 to November 1980, she was granted an IBM World Trade Postdoctoral Fellowship and was with the IBM Thomas J. Watson Research Centre, Yorktown Heights, NY, working on the development of electrically alterable read-only memory using Si-rich oxides. At the end of 1980, she

returned to the KU Leuven as a Senior Research Assistant and from October 1982 as a Research Associate of the National Fund for Scientific Research (NFWO). With the foundation of the Interuniversity Microelectronics Center (IMEC), her activities moved from the KU Leuven to the IMEC, where she initially remained as a Research Associate of the NFWO. Since October 1989, she has been a regular employee of the IMEC. From 1985 to 1992, she was the Head of the Group on Process and Device Modelling and Simulation, working on process optimization techniques, parameter extraction, analytical and numerical device modeling, and computational physics. The Statistical Process Control Activities (SPC) were also monitored through her group. From January 1993 to December 2002, she was in charge of deep-submicrometer MOS technology and exploratory field-effect devices. From January 2003, she became the Strategic Coordinator of Doctoral Research in the IMEC. Since October 1986, she has been a part-time Professor at the KU Leuven. She has authored or coauthored more than 250 publications.

Dr. De Meyer was the coordinator for the IMEC in the ESPRIT 962 EVEREST, STORM, NOVA, ULTRA, VAHMOS2000 (prime), FASEM, and ULIS projects, in the IST SIGMUND (prime) and SATURN (SOI) projects, and currently in the Maie Curie EST EDITH project. She was also involved in the ESPRIT ACCESS program, ADEQUAT, ACE, and IST HUNT. She has also managed the HCM-SUSTAIN network on deep-submicrometer silicon technology with 21 partners from academia and research institutes. She is currently the Editor of the IEEE ELECTRON DEVICE LETTERS and a Member of the International Technology Roadmap for Semiconductors (ITRS) working groups on Process Integration, Devices and Structures (PIDS) and Emerging Research Devices (ERD). She has organized summer courses, the SISPAD 1998, and the ULIS 2004 workshop.