

Applications of Epitaxy for Semiconductor Technology

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The role of epi in CMOS as one of the key performance enhancing element for both bulk-Si and SOI technologies is well established. This review discusses e-SiGe, e-Si:C, and raised source drain epi research for 15 nm and beyond nodes. Impact of proposed device design change from “doped body” to “undoped body” will be examined. Finally, growth options for strained SiGe (> 50%) on Si without a graded buffer layer have been studied to fabricate short channel pFETs. Challenges and opportunities for epi in the context of future generation CMOS are discussed.

CMOS Scaling

Despite formidable power density, lithography challenges, and escalating development cost CMOS scaling continues to follow Moore’s law (Figure 1). However, current CMOS scaling is driven by density scaling rather than density/performance scaling because of increased power dissipation. This is particularly true in this new era of multi-core architecture for computing. The ultimate goal of scaling which is to lower the cost per function per successive CMOS generation is being achieved nevertheless despite performance limitations.

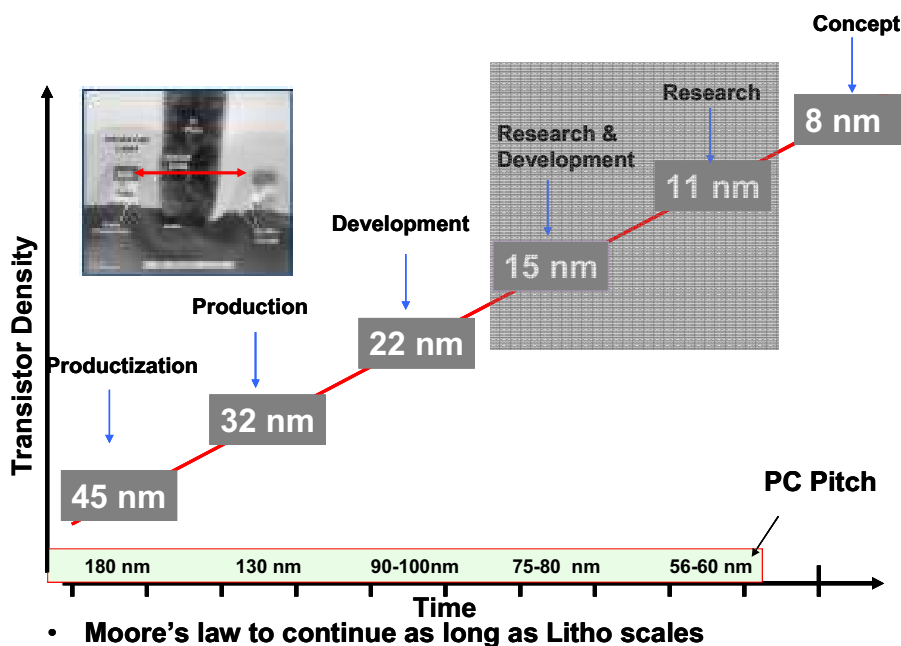


Figure 1. CMOS technology roadmap to 8 nm node.

Over the last few nodes, doubling of device density has been achieved by lining up all device gates in one direction only, i.e., by reducing the device pitch along one axis (to fit one gate, spacers and contacts) by 30%, and reducing the device width along the other axis by 30% as well. Figure 1 inset shows a modern device in a tight pitch surrounding (1). The requirement to fit the device and the contact in an ever shrinking pitch is a firm one, since in the absence of such a capability, a significant motivation behind the Moore's Law will disappear.

As the device pitch scales below 100 nm, it is estimated that 25-30% of the pitch will be consumed by the device channel, and the rest will be consumed by spacers and contacts (Figure 2). The channel length scaling that slowed during the 90 - 45 nm era has to be picked up again as we move to the 32 nm and beyond nodes. Channel length of < 20 nm will be required for 15 nm and beyond nodes.

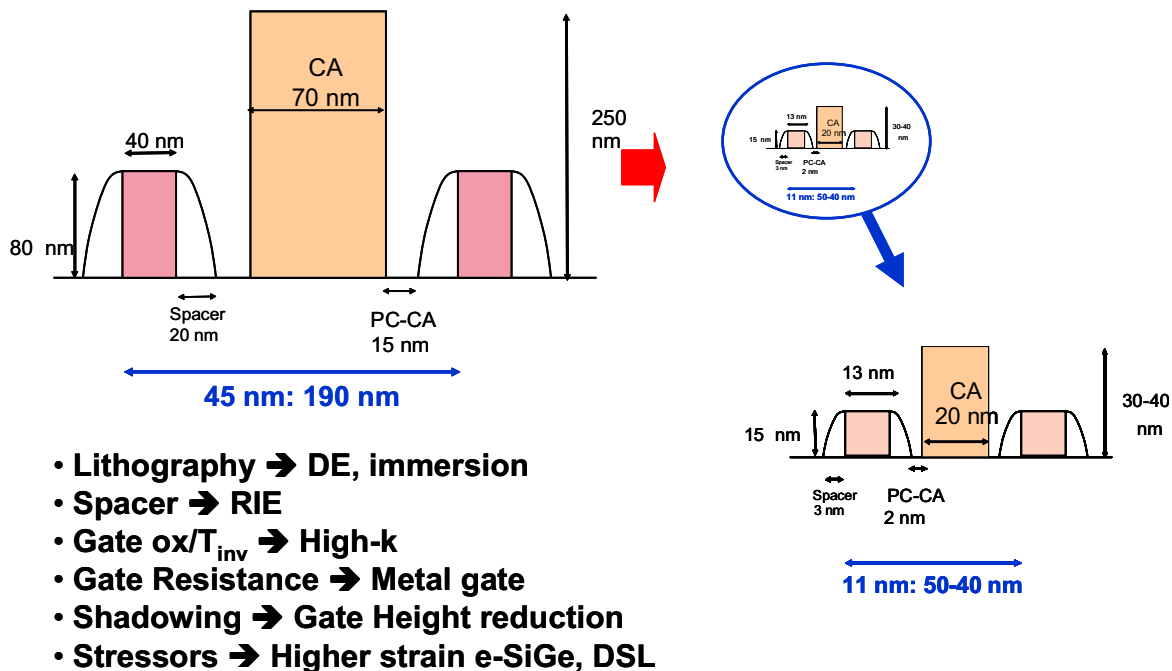


Figure 2. Gate to gate pitch for 65 nm and 15 nm devices: (a) and (b) to scale, (c) magnified view of (b) (from Ref 1)

Figure 2 also lists various challenges arising from lithography, spacers, gate oxide, gate resistance, gate shadowing during ion implantation, and stressor implementation, and how these challenges are expected to be addressed in 22 nm and beyond CMOS nodes.

Device Design for 22 nm & Beyond CMOS

It is remarkable conventional device design with doped channel (“doped body”) has successfully been applied since the inception of CMOS, and has now been extended down to 22 nm CMOS node on both bulk-Si and partially depleted (PD) SOI albeit with challenges (Figure 3). This trend is likely to continue to at least 15 nm node. Key performance enhancing elements will include advanced lithography (for density scaling), p and n channel strain via e-SiGe, and e-Si:C, respectively, shallow but highly doped extensions (via epi or ion implantation or a combination of both epi and ion implantation), low contact resistance contacts and silicides, high-k/metal gate, and low-k dielectrics. Further scaling beyond 15 nm using conventional device design (i.e., with doped body) may lead to degraded device performance (lower I_{on} and higher I_{off} due to increased short channel effects) particularly for low power (LP) applications. “Counter-scaling”, i.e., device drive current degradation, has been shown to occur at L_{gate} of ~ 30 nm in bulk technology (2) due to ever increasing halo doping causing GIDL, high junction leakage, and increased device variability. To counteract this degradation trend device design based on “body control” or “undoped body” is being explored (3).

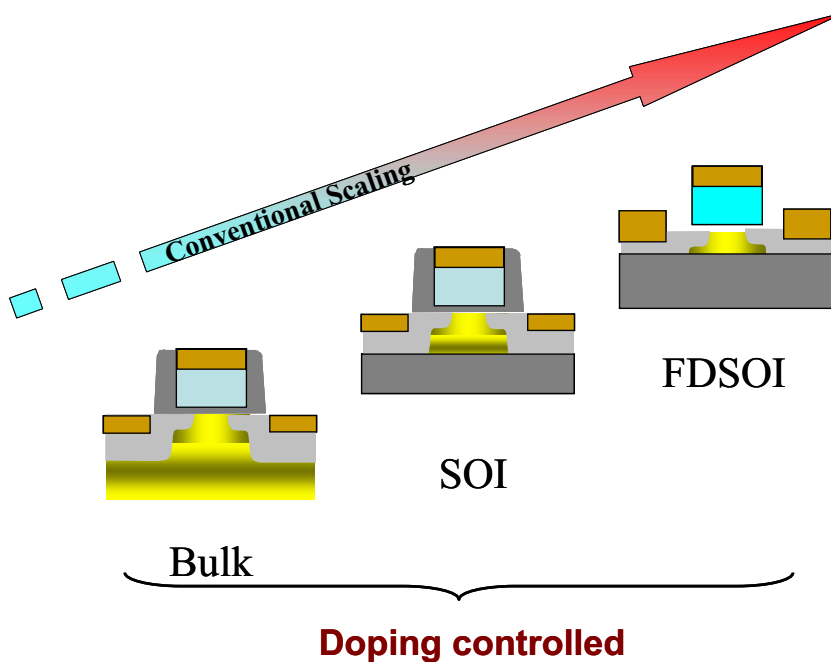


Figure 3. Evolution of “doped-body” device design (from Ref 3)

Three device design options are being considered for “undoped body”: (i) extra-thin SOI (ETSOI), (ii) FinFET, and (iii) tri-gate. Figure 4 below shows the design for the ETSOI option. Design rules for body and BOX thickness, and their relationship to L_{min} to achieve desired device electrostatics are illustrated below.

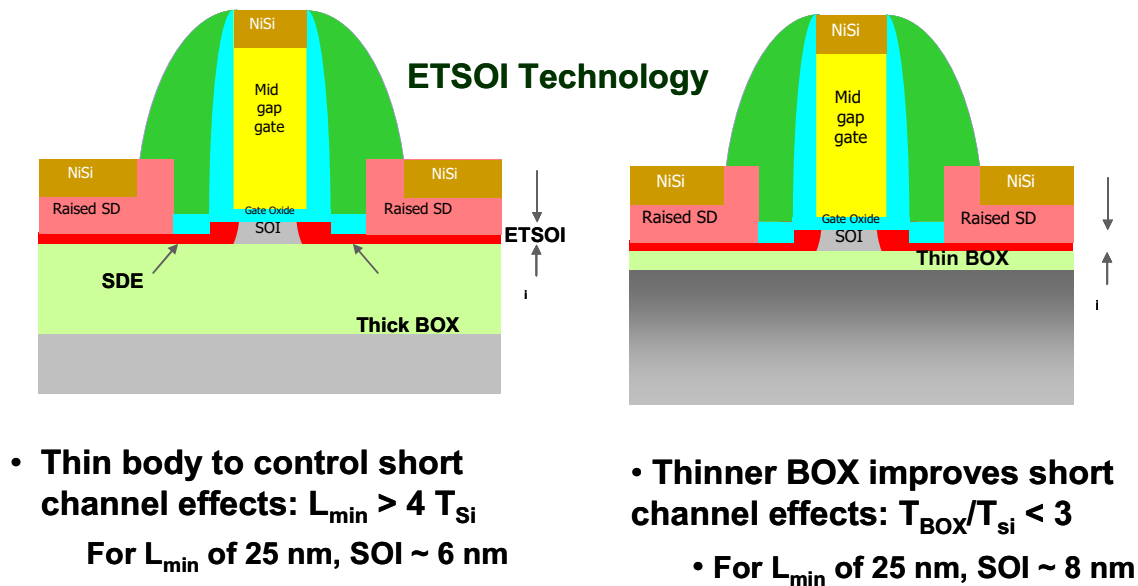


Figure 4. “Undoped-body” device design using ETSOI technology (from Ref 3)

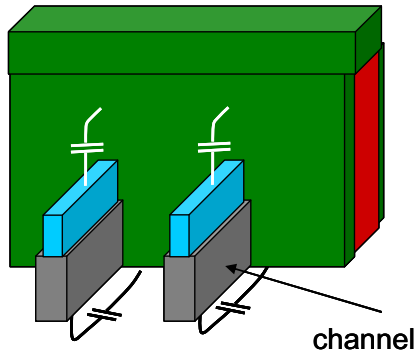
Figure 5 shows FinFET and Trigate options for body-controlled MOSFETs (3). These are three dimensional devices with the conducting channel wrapped around a thin silicon "fin", which forms the body of the device. The dimensions of the fin determine the effective channel length of the device. There are several advantages in using this device architecture: (i) short channel effects (i.e., improved DIBL) are controlled by the thickness of its thin body instead of channel doping which in turn reduces random dopant fluctuations, (ii) improved mobility due to lower vertical field and less coulombic scattering, (iii) improved subthreshold slope, (iv) low parasitic capacitance, and (v) performance boost for pFETs on 110 surfaces of a fin (4). The disadvantages include: (i) fundamental 3D C_{gs} penalty from the fringing fields between the gate and the bottom of source/drain (C_{tb}), (ii) $R_{\text{parasitic}}$ which has several components, such as the body extension resistance, the spreading resistance from the thin body channel to the epi S/D regions, silicide contact resistance. From practical point of view, 3D structures have serious integration challenges including control of fin thickness, epitaxial growth on source drain region, conformal doping, and silicidation etc.

Trigate transistors employ a single gate stacked on top of two vertical gates allowing for essentially three times the surface area for electrons to travel (Figure 5). Tri-gate transistors have been shown to reduce leakage and consume far less power than current transistors. The term tri-gate is sometimes used generically to denote any multigate FET

with three effective gates or channels. Pros and cons of tri-gate transistors are expected to be similar to those described for FinFETs.

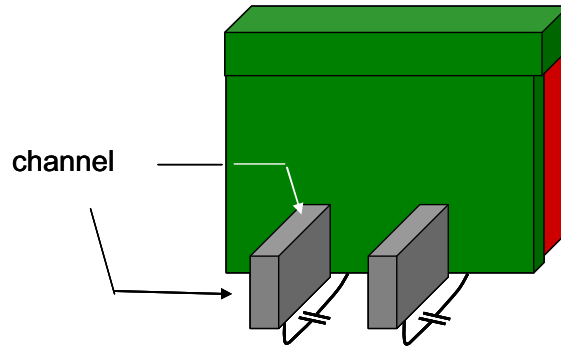
FinFETs: higher C_{fringe}

- no top or bottom conduction



Trigate: Lower C_{fringe}

- no bottom conduction



- FinFET less demanding on vertical etches due to a protective dielectric cap

Figure 5. “Undoped-body” device design using FinFET and Trigate options (from Ref 3).

Channel & Source-Drain Engineering by Epi

Current CMOS technology is serving two widely different application platforms: 1. high performance computing (HPC), and 2. low power consumer electronics. Table 1 below compares requirements for the two applications.

Table 1.

	High Performance	Low Power
Junction leakage	100 nA/ μm	1-100 pA/ μm
Metal levels	13-14	< 10
Stressors	e-SiGe, e-Si:C, liners	None or minimal
Chip dimensions	Up to 5 cm ²	1-2 cm ²
Applications	Computing: main frame, servers, video games, graphic chips	Consumer electronics
Cost	High	Low

CMOS technology addressing HPC does require various advanced processes including high-k/metal gate, and strain engineering. Successful implementation of e-SiGe for strained p-FETs is well established. However, disproportionate reduction in device area per generation with respect to gate length, requires increased strain in the e-SiGe to compensate for the lost volume due to non-scaled gate length.. For example, Ge concentration has increased steadily from < 20% in 90 nm pFETs to > 35% in 32 nm pFETs, and this trend is expected to continue to future nodes. e-SiGe proximity to the pFET channel is another effective knob to maximize strain in the channel (Fig 6) (5). It is critical that e-SiGe be pseudomorphic at growth temperature and remain fully strained during subsequent processing temperatures which could exceed 900°C. Basically, this implies that future CMOS will contain e-SiGe which is thermodynamically unstable. From practical point of view, thermal management of metastable e-SiGe layers during post-epi processing will govern defectivity in e-SiGe. In particular, any halo, extension or source-drain implant in conjunction with annealing which facilitates strain relaxation of

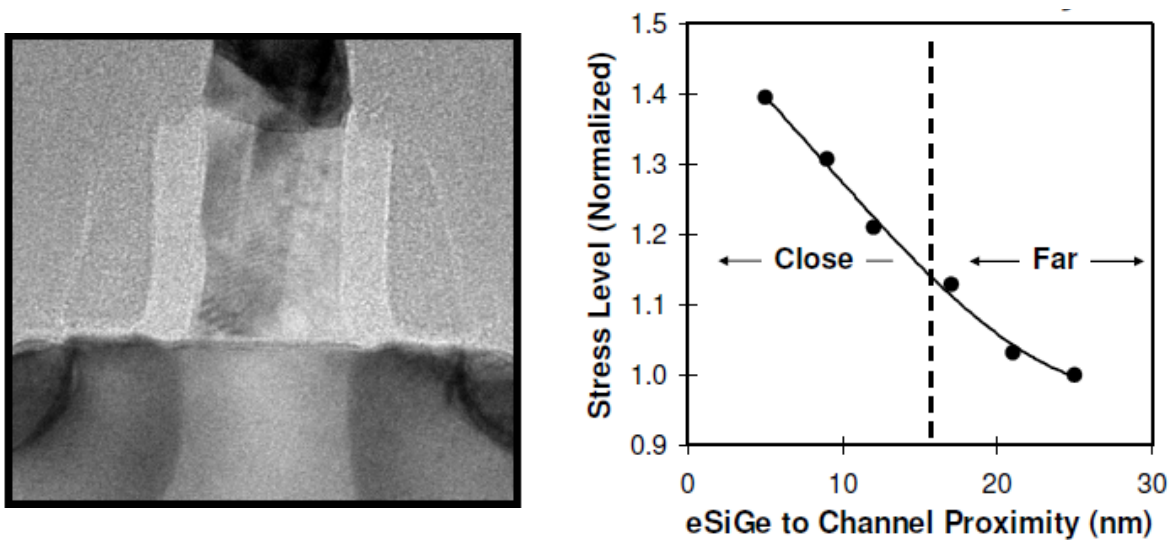


Figure 6. **a.** e-Si Ge in advanced pFETs and **b.** its strain as a function of channel proximity (from Ref 5)

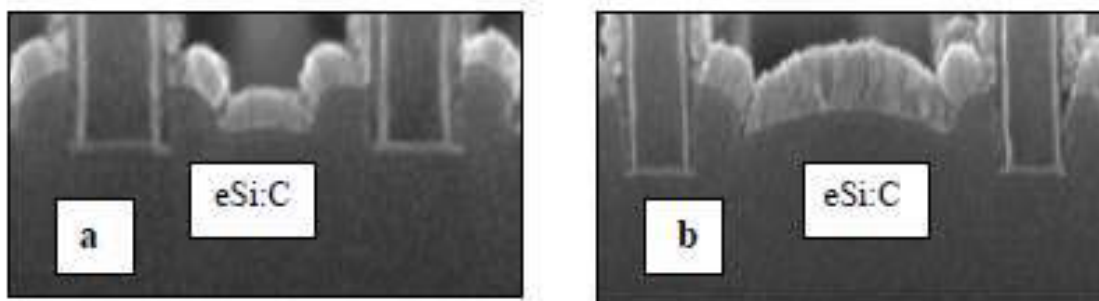


Figure 7. e-Si:C implementation in advanced nFETs: (a) narrow gate pitch, and (b) wide gate pitch (from Ref 6)

these highly metastable materials will no longer be practical. Current epi effort is therefore aimed at in situ boron doped SiGe (mid 10^{20} cm^{-3}). Similarly, equivalent thermodynamic scenario for nFET is expected to occur once e-Si:C process is implemented to strain nFET channels. Again, the emphasis is on achieving in situ phosphorus doped e-Si:C to avoid relaxation via ion implantation/annealing. Figures 6 and 7 show e-SiGe (5) and e-Si:C (6) implementation in advanced CMOS nodes.

CMOS technology addressing low-power application, on the other hand, either may not utilize strain enhancement via e-SiGe and e-Si:C, or such options may not be suitable for the low-power device design such as that with ETSOI (7) and FinFETs devices (4). Epi requirements in these cases are dominated by reduction in external series resistance due to extremely thin extension layers ($< 2 \text{ nm}$). Therefore, raised source drain (RSD) Si epi with high in situ boron and phosphorus doping ($> 4 \times 10^{20} \text{ cm}^{-3}$) for pFETs and nFETs, respectively, is required. In addition, there may be geometrical requirements to minimize C_{ov} such as that shown for ETSOI in Figure 8.

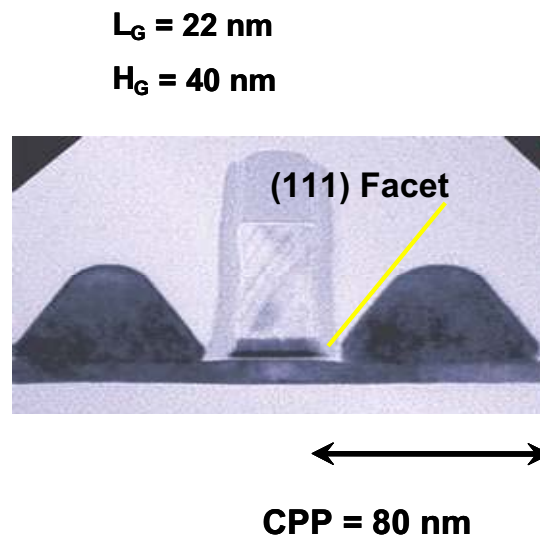


Figure 8. Faceted growth of raised source-drain Si on ETSOI (Ref 7)

High Mobility SiGe and Ge Channels for pFETs

The best hole mobility material has been shown to be uniaxially strained Ge (Figure 9) (8). By fabricating short channel SiGe, relaxed Ge and strained Ge channel devices with scaled high- κ /metal gate stacks, three main advantages are demonstrated: *i*) more aggressive T_{inv} scaling of the gate dielectric due to lower temperature processing, *ii*) band gap engineering to allow better control of threshold voltage and possibly *iii*) lower external resistance due to the higher B activation in these materials.

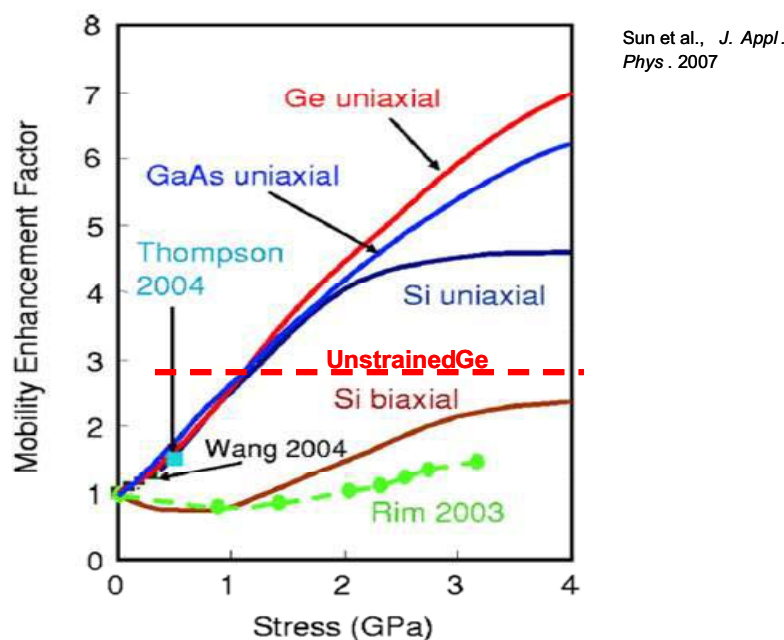


Figure 9. Comparison of mobility enhancement in strained Si, Ge and GaAs (from Ref 8)

We now describe methods to grow Ge on Si, followed by fabrication of pFETs on strained Ge.

Growth of Ge on Bulk-Si and SOI: To reduce large ($\sim 4\%$) misfit strain for Ge epitaxial growth on Si, a relaxed SiGe template with Ge concentration in the range of 20-40% is used on Si or SOI followed by growth of strained Ge. Figure 10 shows XTEM results from the growth of highly strained, thin Ge layers on high-quality 300 mm GBLs with nominally 20% Ge (9).

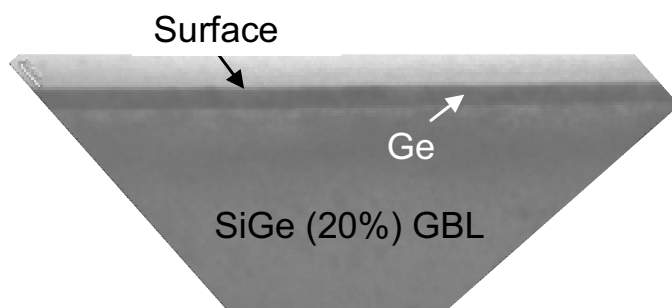


Figure.10. XTEM showing planar strained Ge growth on SiGe GBL (from Ref 9)

Similar results for s-Ge growth has been obtained on relaxed SGOI substrates (Figure not shown)

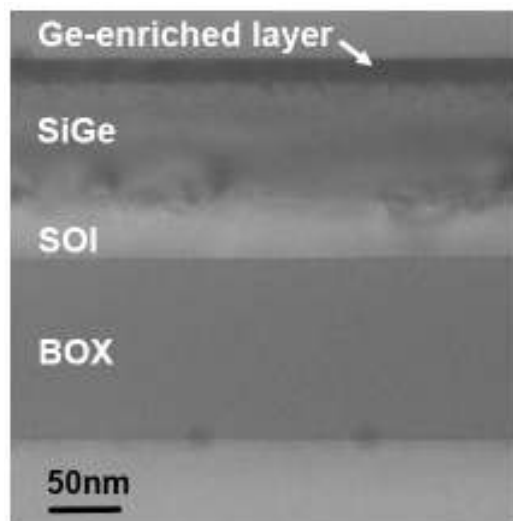
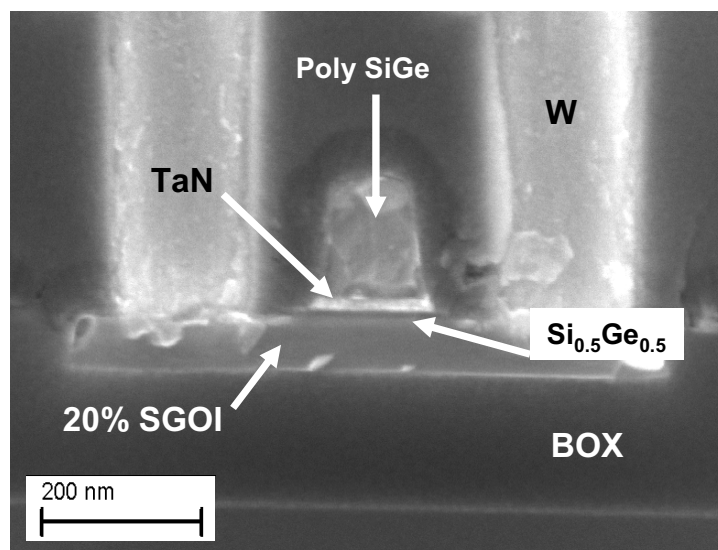


Figure 11. Ge growth on SOI via a SiGe buffer layer (from Ref 9)

Another approach to obtain high Ge content in the surface region is to oxidize a pseudomorphic SiGe layer with 20-30% Ge at $> 900^{\circ}\text{C}$ as shown in Figure 11..

Short channel ($\sim 0.1 \mu\text{m}$) pFETs with Ge concentration varying from 50 – 100% were fabricated using structures of both Figs 10 (with a SGOI substrate) and 11. Figure 12 shows cross-sectional SEM of a fully integrated pFET using a strained $\text{Si}_{0.5}\text{Ge}_{0.5}$ channel.



Bedell et al., ECS 2009

Figure 12. XSEM of a fully finished s-Ge pFET (from Ref 10)

I-V characteristics from devices shown in Fig 12 were obtained for control Si, $\text{Si}_{0.5}\text{Ge}_{0.5}$, and Ge and are shown in Figure 13. These results show that I_{on} in these devices increases only linearly with increasing Ge content due to increased carrier mobility, but the off-state leakage (I_{off}) increases exponentially rendering these devices unusable for low-power CMOS application (Figure 13). Use of Ge is nevertheless appealing for a variety of optoelectronic applications as well as multi-junction solar cells. Research on Ge growth on Si should continue to integrate above described applications on Si.

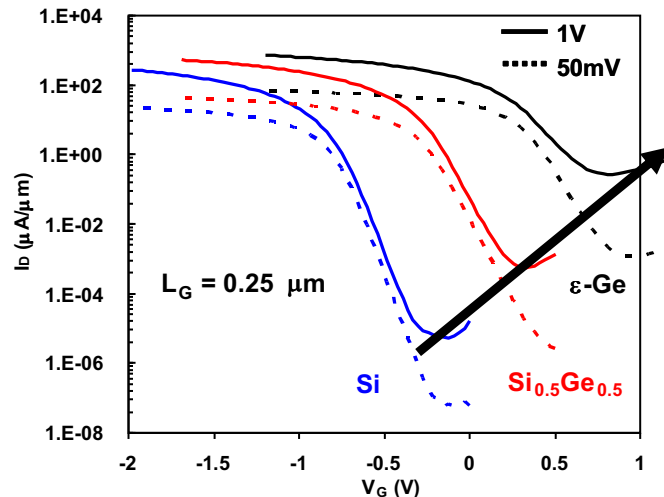


Figure 13. I_d - V_g characteristics of s -SiGe, and s -Ge pFETs along with a Si pFET. Exponential increase in I_{off} with increasing Ge% is evident (from Ref 10).

Summary of Epi Options for Si CMOS

Table 2 below summarizes various epi options in progress for current and future CMOS.

CMOS Elements	Epi Process	Substrate		Growth/Doping
		Bulk-Si/SOI	ETSOI/3D	
Source/Drain Engineering	RSD: Si, SiGe	Yes	Yes	Conventional selective, In situ B & P
	e-SiGe (>1% strain)	Yes	No	Conventional selective, In situ B
	e-Si:C (> 0.2% strain)	Yes	No	Growth/etch, In situ P
Channel Engineering	c-SiGe (>20%)	Yes	??	Selective, undoped
	c-Ge	Yes	??	Selective, undoped

Future Epi Applications and Challenges

Although epi will unquestionably remain integral part of CMOS technology, it will face challenges both from fundamental and manufacturing points of view. At the fundamental level, high strain epi processes will inherently be metastable and subsequent process induced defect control will be paramount to epi's success with CMOS. This will force growth temperatures for epi to remain $< 650\text{ }^{\circ}\text{C}$. At such growth temperatures, throughput of e-SiGe or e-Si:C is likely to suffer. Additionally, selective epitaxial growth will increasingly utilize growth/etch sequence rather than conventional chlorine based selective growth. This latter process may result in deteriorated loading and micro-loading effects. These challenges although formidable are not unsurmountable.

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