

Gate Oxide Reliability of Poly-Si and Poly-SiGe CMOS devices

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CIP-GEGEVENS KONINKLIJKE BIBLIOTHEEK, DEN HAAG

Title : Gate Oxide Reliability of Poly-Si and Poly-SiGe CMOS devices

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ISBN : 90-365-1391-X

Keywords : IC-Technology, Semiconductors, Gate Oxide Reliability, Silicon-Germanium, Stress-Induced Leakage Current(SILC), Gate Oxide Breakdown, Light Emission

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This research was financially supported by the Dutch Foundation for Fundamental Research on Matter (FOM).

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Chapter 1

Introduction

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.

I believe that such a large circuit can be built on a single wafer."

Gordon E. Moore (1965) [1]

1.1 Introduction

The down-scaling of CMOS device dimensions has been the main stimulation for the continuing growth of the microelectronics industry over the past two decades. This trend of steady down-scaling was first formulated by Gordon E. Moore and is better known as Moore's law [1]. In 1965 G. Moore published a semi-log plot of the number of components on a silicon chip versus the date of first availability. The result was a straight line representing almost a doubling per year. In the later years, the rate relaxed somewhat to a doubling every 18 months. This is still the rate of today and it is expected to prevail for some time.

Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) have been around quite some time now. The main success of these silicon based devices is, apart from the possibility to reduce their dimensions down to almost nanometer scale dimensions, the stable high quality silicon-silicon dioxide interface and their ability to interconnect millions to billions of devices on a single chip to form an integrated circuit (IC). The basic concept of the MOSFET and its operation was already formulated almost seventy years ago [2], even before the experimental discovery of the bipolar junction transistor on December 16, 1947 by J. Bardeen, W. H. Brattain and W. Shockley [3, 4] for which they later received the Nobel

Price. However, it was not until 1960 that the first silicon MOSFET was actually realized by Kahng and Atalla [5]. Ironically enough, the main reason for the rather late realization of a functioning MOSFET was that at those days it was very hard to realize an interface between a dielectric layer and a semiconductor which was of very high quality, a requirement for proper MOSFET action.

Today, after many generations of scaling the smallest feature in CMOS devices, that is the gate oxide thickness, is approaching atomic dimensions and fundamental limits imposed by quantum mechanics as off-state leakage current close in on technology. Tunneling currents larger than 1 A/cm^2 are predicted for SiO_2 dielectric layers of 1.5-2 nm thickness. Also the reliability of the gate oxide is becoming a major problem. If the scaling trend continues as predicted by the International Technology Roadmap for Semiconductors (ITRS) [6](see Table 1.1), SiO_2 may not be able to meet future reliability requirements under (normal) operation conditions [7].

Year of First Shipment Technology Node	1997 250 nm	1999 180 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm
Eq. Oxide thickness [nm]	4-5	3-4	2-3	1.5-2	<1.5	<1.0
Maximum Field [MV/cm]	4-5	5	5	>5	>5	>5
Supply (gate) voltage [V]	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6

Table 1.1: Equivalent gate oxide thickness, electrical field and largest allowable gate voltage corresponding to the indicated year of first manufacture and technology generation. Data taken from the International Technology Roadmap for Semiconductors (1998 Update version) [6].

A fundamental understanding of the degradation mechanism of ultra-thin SiO_2 layers is therefore of great importance to allow accurate predictions of the reliability for future MOS devices under device operation conditions. Early in the next century state-of-the-art MOSFETs will have 1-2 nm gate oxide thickness and will work at supply voltages of 1 V. The reliability of these devices is becoming a major issue. This creates some interesting research challenges to be solved in the near future. Some of them will be addressed in this thesis.

"Fortunately there is still some margin left in today's devices for perhaps a few generations, but how much longer can CMOS scaling continue?"

1.2 Oxide degradation, reliability and lifetime

SiO_2 is still beyond any doubt one of the key factors in the success of CMOS-technology. The main reason for this is that for the reliable production of large-scale integrated circuits(ICs) it is necessarily to produce by compatible tech-

nologies both a semiconductor and an insulator that have superb electrical and mechanical properties. In fact, SiO_2 is a very good insulator with a very large bandgap of around $\mathcal{E}_g=8\text{-}9$ eV [8, 9] and it can be grown very easily and well-controlled on a Si-substrate.

The properties of the oxide-silicon system are fundamental to the performance of integrated-circuit devices and knowledge about these properties has been around for quite a long time now. At present, SiO_2 layers as thin as 1.5 nm can already be made and are used as a gate dielectric in a fully functioning MOSFET with a gate length of 0.1 μm [10, 11]. This also displays some of the most powerful properties of SiO_2 , namely its scalability and process integration capabilities. Nevertheless SiO_2 is not perfect and still suffers from some degradation. Aggressive down-scaling of the gate oxide thickness for future MOS devices however requires that, among other concerns, the gate oxide can still meet requirements for reliability. A fundamental understanding of the degradation mechanism of SiO_2 is therefore of great importance to allow accurate predictions of the reliability for future MOS devices at device operation conditions.

Gate oxide reliability has always been a major issue in determining the feasibility of MOS devices. Especially the reliability of ultra-thin gate dielectrics ($t_{ox} < 5$ nm) is of increasing concern because of the significant direct tunneling currents flowing during normal device operation. The exponentially increase in tunnel current with decreasing oxide thickness will increase the standby power and seriously degrade the gate oxide reliability at operation conditions if the gate voltage is not simultaneously reduced sufficiently. This direct tunneling (DT) current poses a serious problem onto the further down-scaling of the gate oxide thickness for sub-100 nm feature-size technologies. If the scaling trend continues, SiO_2 may not be able to meet future reliability requirements [7, 6]. This means that another material with higher reliability and lower standby tunneling current will be needed ¹.

Ultra-thin gate oxide reliability is therefore a major research topic, but in spite of the large amount of knowledge already gathered on this subject a number of issues are still not resolved. Gate oxide reliability was studied mainly for n-doped polycrystalline silicon (poly-Si) gate material up till now. With the down-scaling of the gate oxide thickness below 10 nm, p^+ poly-Si gate electrodes have been proposed for deep sub-micron gates to replace n^+ poly-Si gates. The main reason for this is that n^+ gate p-channel devices need an additional p-type implantation in the Si-substrate for threshold voltage adjustment. When a voltage is applied between the source and drain it is observed that the minimum in potential barrier is no longer at the surface indicating a buried channel operation [12]. However, p^+ gate p-channel devices do not require an additional implant for threshold

¹To overcome this problem, the Semiconductor Industry Association (SIA) mentions high- ϵ dielectrics like Ta_2O_5 as a possible candidate to replace SiO_2 in sub-100nm feature-size technologies, which should enter production around the year 2006 (1997 version) [6].

voltage adjustment and thus remains a surface channel device.

Surface channel pMOSFETs with p^+ poly-Si gate have several advantages over conventional n^+ poly-Si gate buried-channel pMOSFETs, such as reduced short-channel effects and improved turn-off characteristics [12]. Therefore, for CMOS devices with ultra-thin gate oxides, p^+ gates have been proposed for p-channel MOSFETs to convert the buried channel operation to surface channel operation.

The degradation of p^+ gate devices with ultra-thin gate oxides is therefore also a major concern. However, before studying the degradation of p^+ gate devices it may be instructive to recall the most important models for explanation of oxide degradation as reported in literature and to review the different stages in the breakdown process.

1.3 Physical mechanisms of oxide degradation

In literature, many models have been suggested in order to explain the physical mechanism of oxide degradation under electrical stress conditions. A common assumption in all these models is that if some parameter reaches a critical value it triggers the breakdown of the oxide. The three most prevailing models reported in literature are :

1. *Electric Oxide Field model*

According to this thermodynamic model [13, 14, 15, 16], the electric field itself induces sufficient damage in the oxide due to local field enhancement to cause electron trap generation. Since this model is solely based on the applied electrical field, it means that the electron flux does not influence the oxide degradation at all. This model is therefore commonly referred to as the E_{ox} -model. It has however been observed by Degraeve *et al.* [17] that both the electron fluence and the electric field determines the oxide breakdown. It was shown that electron trap generation is identical for all stress fields and that the electric field merely acts as an acceleration factor for the degradation process. This strongly suggests that the breakdown process is current driven, which means that the time-to-failure data should show a $1/E_{ox}$ dependence due to Fowler-Nordheim (FN) current conduction. This is known as the $1/E_{ox}$ model and will be explained next. However it should be noted that there are also reports which indicate that the E_{ox} -model gives a better fit to long-term and low-field data than the $1/E_{ox}$ model [18, 19]. These data suggests strongly that it is field, not current, which causes the time-dependent degradation of the oxide.

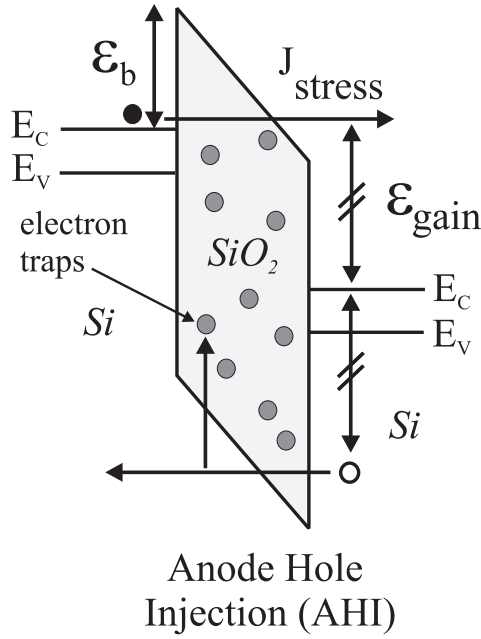


Figure 1.1: Schematic representation of Anode Hole Injection (AHI) model.

2. Anode Hole Injection model (AHI)

In the Anode Hole Injection model (AHI) [20, 21, 22, 23, 24] the injected electrons gain kinetic energy as they travel through the conduction band of the SiO_2 layer. Upon reaching the anode these high-energetic electrons release part of their energy as they fall back to the conduction band in the anode. Thereby having a probability of creating a *hot-hole* which can tunnel back into the oxide (see Fig. 1.1). These holes are suspected to damage the oxide layer, i.e. creating electron traps and will eventually trigger the breakdown process as soon as a critical hole fluence is reached. This model is commonly referred to as the $1/E_{ox}$ model, since the time-to-failure data should show a $1/E_{ox}$ dependence due to Fowler-Nordheim (FN) current conduction. This model assumes that trap generation is directly linked to hole generation, since holes are needed to create traps in the oxide. Indeed, a unique relationship between hole fluence and electron trap generation is found, independent of stress field and oxide thickness [17]. Furthermore, it was demonstrated that breakdown in thin oxide layers occurs as soon as a critical density of (neutral) electron traps in the oxide is reached.

According to Schuegraf *et al.* [22] the AHI model proves to be valid for a large thickness range varying between 2.5 nm and at least 13 nm and can predict Q_{bd} and t_{bd} behavior for low oxide voltages down to 2.4 V.

However, DiMaria *et al.* [25, 26, 27] observed that anode hole injection is important, but only for gate voltages larger than $V_g \approx 7.6$ V. They observed a threshold energy for trap creation of about 2.3 eV with respect to the bottom of the oxide conduction band, while they stated that for anode hole injection a threshold energy of at least 5 eV is needed. So they concluded that degradation of the gate oxide is not related to *hot-holes* but to hydrogen-induced defects, as will be explained in the next model.

3. Hydrogen-release model

This model is very similar to the AHI injection model. According to the hydrogen release model oxide degradation is due to H^+ instead of holes [28, 29, 26]. A large amount of hydrogen is present at the interface, since passivation of the Si/SiO₂ interface defects with hydrogen is performed in standard CMOS-processing. In this model the energy of the high-energetic electrons is released by releasing hydrogen from the Si/SiO₂ interface. When the H^+ enters the oxide it is believed to create damage. This is supported by experimental evidence. DiMaria *et al.* [26, 30, 31] demonstrated that SiO₂ degrades in a similar manner when exposed to H^+ . From these studies it was also concluded that the generation of neutral oxide traps in thin oxides is the dominant cause of oxide degradation and will eventually lead to oxide breakdown. So electron trap creation can be observed as soon as the electron energy exceeds 2 eV with respect to the bottom of the oxide conduction band. However, it has been observed that in the direct tunneling(DT) regime, where the electrons do not enter the oxide conduction band, defect generation still occurs.

The E_{ox} versus $1/E_{ox}$ controversy has continued for many years now, since both models can fit the time-to-failure data rather well over the measured (limited) field ranges. Although the latter two models are the most prevailing ones in explaining the degradation of the oxide, no model has been proven to be unambiguously correct up until now.

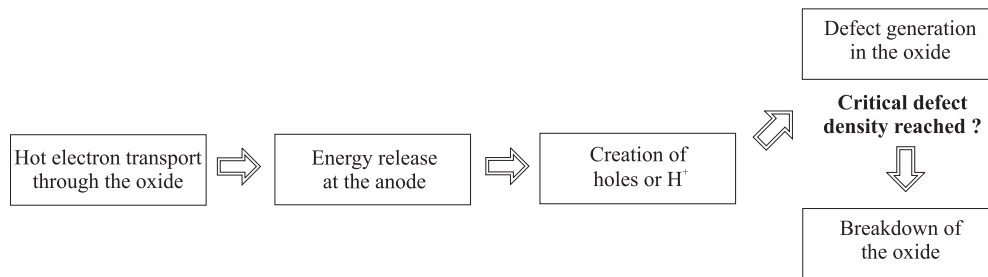


Figure 1.2: Schematic illustration of gate oxide breakdown due to positive species (holes or H^+).

Nevertheless, from the models above it can be concluded that the degradation mechanism of the oxide is most likely related to positive species as is illustrated in Fig. 1.2 and that breakdown occurs as soon as a critical neutral electron trap density $D_{ot,crit}$ is reached.

1.4 Problem definition: Basic principles

In the previous section it was stated that oxide degradation proceeds with the generation of neutral electron traps in the bulk of the oxide. In this section the different stages of oxide degradation as a function of the density of generated electron traps in (ultra-)thin gate oxides is briefly evaluated. Up until a few years ago the focus was mostly on the occurrence of defect-related i.e. *extrinsic* breakdown, while *intrinsic* breakdown never posed any real reliability problem. However, with the further down-scaling of the oxide thickness to only a few nanometers, intrinsic related breakdown has become a major reliability problem. Since this intrinsic related breakdown eventually limits the scaling of the gate oxide thickness for future generation MOS devices it seems natural to investigate its properties in more detail. First however a brief overview of the different stages of oxide degradation is given.

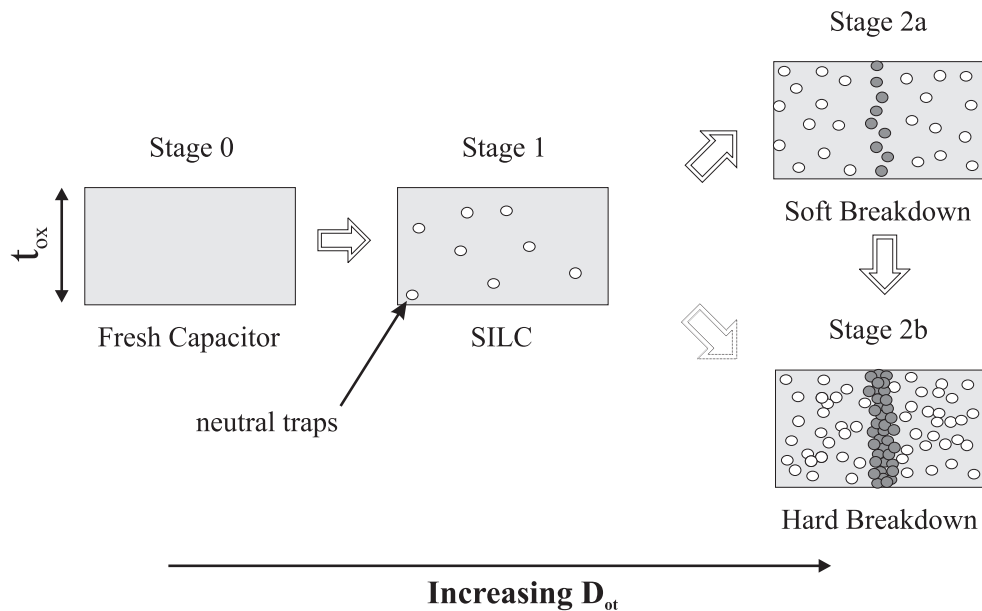


Figure 1.3: Schematic illustration of oxide degradation. Roughly 3 stages can be distinguished, which are 1) SILC, 2a) soft breakdown and 2b) (hard) breakdown.

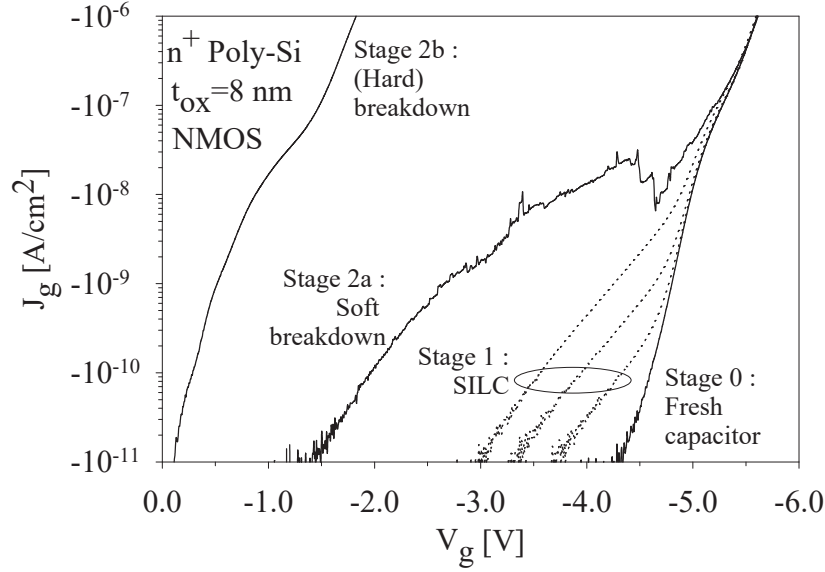


Figure 1.4: J_g - V_g measurements of n^+ poly-Si NMOS capacitors on 8 nm gate oxide thickness showing the different stages of oxide degradation, which are 1) SILC, 2a) soft breakdown and 2b) (hard) breakdown.

Electrical stressing the oxide leads to continuous degradation of its insulating properties. Roughly 3 different stages of oxide degradation can be distinguished, which are depicted in Fig. 1.3.

The occurrence of these stages depend on the density of (neutral) electron traps present in the bulk of the oxide D_{ot} . The current-voltage(I-V) characteristics which belong to each of these stages are displayed in Fig. 1.4.

- **Stage 1: Stress-Induced Leakage Current(SILC)**

In sub-10 nm oxides high field stressing of the oxide generates a low field leakage current, which is referred to as Stress-Induced Leakage Current(SILC). Stress-Induced Leakage Current or SILC is the increase in low-level leakage through thin silicon dioxide(SiO_2) layers after the oxide has been subject to high electrical-field stressing. This phenomenon was first observed in the early eighties by Maserjian *et al.* [32] and will be treated in more detail in chapter 3.

- **Stage 2a: Soft breakdown(SB)**

At a higher amount of neutral traps in the oxide, Soft-Breakdown(SB) may occur. Soft, quasi, early, non-destructive breakdown or B-mode SILC is the sudden increase in gate current density at low fields on top of the SILC current to extremely high current levels. It was first observed by Lee *et al.* [33]. This sudden increase in gate current is accompanied by an increase in gate signal noise. Soft breakdown is (only) observed when the power dissipation after breakdown is limited as happens for instance in ultra-thin oxides and small area MOS capacitors [34, 35]. An important difference between SILC and soft breakdown(SB) is that the conduction mechanism of SILC is uniform, i.e. it occurs over the whole capacitor area, while SB conduction occurs at a localized area.

The question however whether soft breakdown corresponds to a real oxide failure is still to be resolved [36]. For ultra-thin oxides it has been reported that the (soft)breakdown of such oxides is difficult to detect, since the post breakdown I-V characteristics are not significantly different from the initial I-V characteristics. The conduction mechanism after breakdown is therefore an important issue and will be treated in more detail in chapter 5.

- **Stage 2b: (Hard) breakdown(HB)**

Further stressing of the gate oxide will eventually lead to termination of the oxide degradation by the occurrence of breakdown of the oxide. This is the final stage of oxide breakdown, where thermal run-away effects lead to a complete loss of insulating properties of the oxide. Hard breakdown occurs if the power dissipation during breakdown is high enough to locally melt the oxide over a small volume centered around the point of breakdown. So hard breakdown is often observed in large area MOS capacitors and thick oxides. It is believed that breakdown is characterized by a maximum amount of electron traps in the gate oxide $D_{ot,crit}$, which is known as the critical defect density at breakdown [17, 7].

Oxide breakdown can be characterized by two parameters, the amount of time which is stressed before the device breaks down and the amount of charge fluence which passed through it. The first is the time-to-breakdown t_{db} and the second the charge-to-breakdown Q_{bd} .

The definition of time-to-breakdown is straightforward, while the charge-

to-breakdown is defined by Eq. 1.1 as [37, 38] :

$$Q_{bd} = \int_0^{t_{bd}} J_g(t) dt \quad (1.1)$$

The charge-to-breakdown is a well-known and widely-used tool to evaluate the gate oxide reliability of MOS structures and study the influence of processing conditions on the Q_{bd} , such as anneal temperature, gate materials and gate implants. The Q_{bd} can be related to the electron trap density D_{ot} , where Q_{bd} is reached as soon as $D_{ot}=D_{ot,crit}$. This implies that the density of neutral traps present in the bulk of the oxide D_{ot} and the generation rate of them ($P_g=\Delta D_{ot}/\Delta Q_{inj}$) are important parameters for gate oxide reliability.

After breakdown a link of electron traps is formed in the gate oxide which connects the gate with the substrate. The post (hard) breakdown I-V characteristics of carefully designed MOS capacitors are studied in chapter 5 as well.

1.5 Research objectives

In this thesis the conduction mechanism, oxide degradation and breakdown of (ultra-)thin gate oxides with n^+ and p^+ gates, which are subject to electrical stress are studied. The aim is to obtain a better fundamental knowledge about oxide degradation and breakdown in both p^+ and n^+ gate devices, which can eventually be used to accurately predict the reliability of CMOS devices with ultra-thin gate oxides at operation conditions.

Recently a larger tunnel barrier height and a different conduction mechanism for gate injection ($-V_g$) have been proposed for p^+ -poly gate devices [39, 40, 41]. This might have a large impact on the reliability of future CMOS devices with p^+ gates. However a complete understanding is still not available. The research objectives of this thesis can essentially be split up into four parts.

First the conduction (I-V), degradation mechanism (SILC) and time-to-breakdown t_{bd} of (ultra-)thin gate oxides is investigated. P^+ and n^+ -gates with poly silicon (poly-Si) and poly Silicon-Germanium (poly-Si_{0.7}Ge_{0.3}) are used to study the influence of gate workfunction on gate current and SILC current. Poly-SiGe is chosen since it allows modification of the workfunction of the gate for p^+ gate devices. Moreover, it is fully compatible with (poly-)Si technology.

Fig. 1.5 displays the energy band diagram of Si, SiGe and Ge. From Fig. 1.5 it can be observed that Si($\chi=4.05$ eV) and Ge($\chi=4.00$ eV) have comparable electron affinity χ . However, the bandgap of Ge($\mathcal{E}_g=0.66$ eV) is much smaller

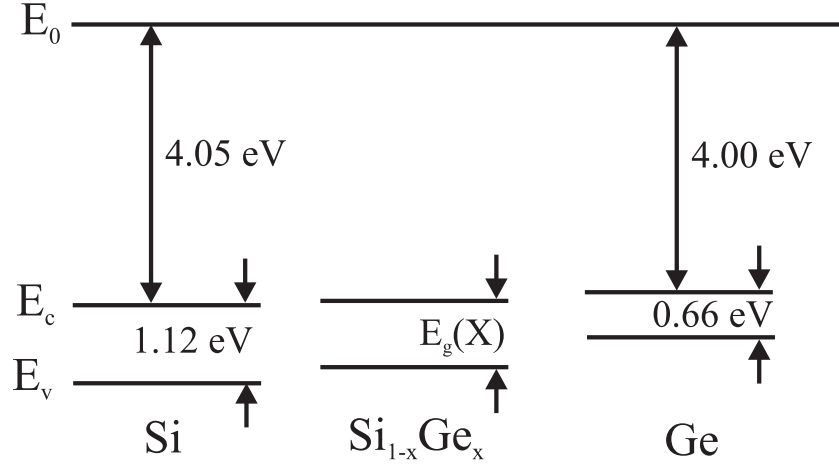


Figure 1.5: Energy band diagram of Si, SiGe and Ge. It can be observed that the bandgap of SiGe can be tuned by changing the Ge fraction.

than Si ($\mathcal{E}_g=1.12$ eV). This allows modification of the valence band edge position of the gate by varying the Ge fraction x in poly-Si_{1-x}Ge_x gate devices and therefore influence the gate workfunction for p⁺ gate devices. This workfunction engineering by exploiting the difference in valence band edge can in principle be applied for all Ge contents. Moreover, poly-Si_{1-x}Ge_x is a promising alternative to poly-Si as a gate material due to its process compatibility and favorable electrical properties, such as higher dopant activation, lower sheet resistance, superior hole mobility and tunable work function [42, 43, 44, 45, 46, 47]. However the gate oxide reliability of poly-SiGe gate devices has not been studied in detail yet.

The impact of gate current and gate workfunction on the reliability of the gate oxide is also briefly investigated. The physical models for oxide degradation presented in the previous section will be critically reviewed based on our findings.

Next, the post-breakdown I-V characteristics of n⁺ poly-Si NMOS gate devices are studied. The I-V characteristics after breakdown can give important information of the breakdown process, which will eventually lead to a better understanding of the degradation mechanism leading to (catastrophic) breakdown.

Finally, light emission measurements are performed on the post breakdown I-V characteristics of n⁺ poly-Si NMOS gate devices. These light emission measurements may also reveal important information about the physical properties of the link formed after breakdown.

1.6 Outline of this thesis

In this thesis the oxide degradation mechanisms of CMOS devices with (ultra)-thin gate oxides is studied. The conduction mechanism, oxide degradation and breakdown of (ultra-)thin gate oxides with n^+ and p^+ poly-Si and poly-SiGe gates have been studied.

The outline of this thesis and main conclusions of every chapter are given in more detail below.

Chapter 2

In this chapter the C-V and I-V characteristics of NMOS and PMOS capacitors are studied. P^+ and n^+ -gates with poly silicon(poly-Si) and poly Silicon-Germanium(poly-Si_{0.7}Ge_{0.3}) were used to study the influence of gate workfunction on gate current. C- V_g measurements on p^+ gate devices show a shift of the flatband voltage from $V_{fb}=0.82$ V(poly-Si) to $V_{fb}=0.60$ V(poly-SiGe) which is caused by a shift in the valence band position of the gate. For p^+ gate devices the J_g - E_{ox} characteristics depend on gate material and gate bias polarity. The onset of conduction at $-V_g$ occurs at a significantly higher oxide field than for $+V_g$ condition. A new model based on Minority Carrier Tunneling(MCT) from the gate is proposed for the J_g - E_{ox} characteristics of p^+ gate devices under gate injection conditions ($-V_g$). Furthermore, high frequency (10 kHz) C- V_g curves of p^+ poly-Si gate devices on 4.8 nm oxide thickness show no sharp onset of gate inversion in the p^+ poly-Si gate at $-V_g$. This is most likely caused by carrier tunneling out of the gate which occurs at a higher rate than that of carrier generation under MCT injection conditions. For very thin oxides ($t_{ox} < 4$ nm) another contribution to the I-V characteristics at $-V_g$ is observed. Carrier separation measurements indicate that a hole current is flowing from the source/drain to the gate in the low voltage regime. This current is presumably due to holes which can tunnel (via traps) from the hole inversion layer in the substrate to the gate. Furthermore, this hole current increases strongly with decreasing oxide thickness and can be important for the degradation and reliability of ultra-thin oxides.

Chapter 3

In this chapter the Stress-Induced Leakage Current(SILC) characteristics of NMOS and PMOS capacitors are studied. P^+ and n^+ -gates with poly silicon(poly-Si) and poly Silicon-Germanium(poly-Si_{0.7}Ge_{0.3}) were used to study the influence of gate workfunction on the SILC current. For n^+ gate devices, symmetric SILC with gate bias polarity is observed. No significant difference in SILC characteristics between the n^+ poly-SiGe and poly-Si reference devices is observed. For p^+ -poly gate devices, asymmetric SILC (gate bias polarity) and reduced SILC

for p^+ poly-Si_{0.7}Ge_{0.3} is observed. The stress injection bias polarity dependence of p^+ gate devices is also studied. It is found that the amount of traps generated per unit of injected charge is approximately 10 times higher for injection of stress from the gate compared to substrate injection of stress. For very thin oxides ($t_{ox} < 4$ nm) the SILC current at $-V_g$ and at low voltages is dominated by hole tunneling from the substrate to the gate. This current is interpreted as trap assisted hole tunneling (HTAT). The effect of fluorine(F) on the SILC characteristics of n^+ poly-Si gate devices has also been studied. A small amount of F suppresses the generation of new oxide traps under high field electron injection, which leads to reduced SILC. At excessive F doses an increase of SILC is observed. Finally, a two-step tunneling model was developed to evaluate the SILC current under FN, MCT and VBT injection conditions. It is shown that this model successfully describes the experimental I-V characteristics for both n^+ and p^+ poly gate devices under substrate as well as gate injection conditions.

Chapter 4

In this chapter results are presented of the time-to-breakdown (t_{bd}) of both n^+ and p^+ poly-Si gate devices on ultra-thin gate oxides ($t_{ox} < 5$ nm). For the 2.5 nm oxides (n^+ poly-Si gate) a decrease in t_{bd} of nearly 4 orders of magnitude is observed when the ambient temperature is increased from 25°C to 200°C. Also a weak gate bias polarity dependence is observed with respect to time-to-breakdown if t_{bd} is plotted as a function of the gate voltage V_g . For p^+ -poly Si gate devices an increase of t_{bd} with increasing gate anneal RTA temperature, i.e. increasing active gate doping, is observed, which is most likely related to a decrease in tunneling current during stress at a fixed gate voltage. This indicates that both the total energy release at the anode and the electron fluence are important parameters for t_{bd} of ultra-thin oxides. It appears that constant voltage stress (CVS) is also preferable for p^+ -poly gate devices on sub-5 nm gate oxides.

Chapter 5

In this chapter results are presented of the post-breakdown electrical characteristics of n^+ poly-Si MOS capacitors with 8 nm and 10 nm thick oxides. The dependence of the post breakdown I-V characteristics on capacitor area, substrate doping and breakdown power were evaluated. Depending on gate and substrate doping polarity, different post breakdown characteristics were observed. For n^+ -poly/oxide/ n^+ -substrate MOS capacitors the post breakdown characteristics resemble that of a resistance. The value of the resistance is determined by the filament cross-section formed through the emission of energy stored in the MOS capacitor before breakdown. For n^+ -poly/oxide/p-substrate MOS capacitors the I-V characteristics after high power breakdown resemble that of a nanometer size diode with a high I_{on}/I_{off} ratio. The breakdown voltage of these diodes is high due to the gate action. For low power breakdown the diodes become

"non-ideal" and their "non-ideality" depends strongly on stress current. The conduction mechanism after low power breakdown is still not well understood. The I-V characteristics of these devices were also measured at variable temperature to study the dominant conduction processes after breakdown. At very low power dissipation soft-breakdown may occur. This shows that soft-breakdown does not only occur in sub-5 nm oxides, but can also be enforced in 8 nm gate oxide thickness structures if the total energy during breakdown is limited.

Chapter 6

In this chapter results are presented of the spectrally resolved absolute measurements of the electroluminescence of silicon nanometer-scale diode-antifuses. The emission spectrum of the diode-antifuses is measured in the energy range of 1.4 - 2.8 eV at different forward and reverse currents. The dependence of the emission intensity on the current was evaluated to study the dominant emission processes. Previously proposed mechanisms for avalanche emission from conventional silicon p-n junctions are discussed in order to understand the origin of the emission. With the diode-antifuses biased in reverse breakdown, we measured (after correction for absorption and interference in the poly-Si layer) a nearly wavelength-independent emission extending from UV to IR corresponding with an average electron temperature between $T_e=5000-6000$ K. This agrees with previous data of conventional avalanche p-n junctions. For the forward biased condition the spectrum reflects the silicon band structure due to emission from electron-hole recombinations. A lattice temperature at the emission site of about $T_L=400$ K was estimated. Finally, the stability of the diode-antifuses has been tested. Results indicate that the diode-antifuse is basically a high quality device. The external power efficiency has been calculated to be $PE=2.0 \cdot 10^{-6}\%$ in the energy range of 1.4 - 2.8 eV. The optical power per unit area is rather high and can reach values up to $0.1-10$ W/cm². Furthermore, due to its nanometer-scale dimensions, very high electrical fields and current densities are possible at low power consumption. This makes the diode-antifuse an excellent candidate for emitter elements in Si-based optical interconnect schemes and for optical sensors and actuator systems.

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