Low Temperature (≤ 800°C) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70 nm CMOS

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ABSTRACT

We present a novel, low-temperature source/drain junction and contact formation technology applicable to sub-70 nm CMOS. In this process, in-situ boron doped SiGe is selectively deposited at 500 °C in the source/drain windows recessed to the desired junction depth. The technology meets the NTRS roadmap requirements for (i) junction depth/sheet resistance (< 100 Ω/sq. for 30 nm junctions), (ii) ultra-low resistivity contacts (1.5 x 10^{-8} Ω-cm^2), (iii) excellent reverse leakage characteristics (less than 1% of the I_{OFF} budget), (iv) perfect box-shaped lateral abruptness and (v) *thermal* integration compatibility with high-k gate dielectrics using the conventional (gate-last) CMOS process flow.

INTRODUCTION

Conventional implanted junctions fall severely short of the future R_{SH}-X_J requirements (1). They are also very limited in terms of achievable contact resistivity and lateral abruptness, which are crucial to minimize the MOSFET series resistance and short channel effects (2). For sub-70 nm CMOS technology nodes, novel junction and contact formation technologies that provide above-equilibrium dopant activation, near-perfect box-shaped profiles, and ultra-low resistivity contacts (< 5 x 10^{-8} Ω-cm^2) are required. Lastly, it is highly desirable to have a junction technology, which allows for easy integration with high-k/metal gate stacks using the conventional CMOS flow without the need for adoption of costly replacement-gate processes that would be required with high-temperature (> 800°C) junction techniques.

JUNCTION-CONTACT FORMATION & CHARACTERIZATION

In the proposed technology, junctions are formed by selective deposition of heavily boron-doped SiGe alloys in the S/D areas recessed by isotropic etching to the desired junction depth (Fig. 1). The junction recess can be achieved using an isotropic Si etch process (like a SF_6 plasma etch).

The films are selectively deposited (Fig. 2) by rapid thermal chemical vapor deposition (RTCVD) at 500 °C using disilane (Si_2H_6), germane (GeH_4) and diborane (B_2H_6) as the precursors. Owing to the low deposition temperature, the deposited junctions are perfectly abrupt.

Above-equilibrium dopant activation is achieved in the deposited layers by the strain compensation effect [(3), (4)] of substitutionally incorporated boron in SiGe. The smaller substitutional boron atoms relieve the compressive strain induced in the lattice mismatched SiGe film. This results in incorporation of percent levels (Fig. 3 and 4) of substitutional (and thus, active) boron in the SiGe matrix. In addition, the strain compensation results in high quality SiGe film growth. Also, since enhanced activation is achieved *in-situ* during the film deposition, a subsequent junction activation anneal is precluded. Ge concentrations as high as 75% were investigated to reduce the band-gap under the contact metal for low-contact resistivity.

Fig. 5 and 6 show Hall effect measurement data for as-deposited and annealed $Si_{0.27}Ge_{0.73}$ films. Corresponding SIMS profiles are shown in Fig. 7. The sheet resistance of 30 nm films is less than 100 Ω/sq. Annealing was seen to result in no degradation in R_{SH} or anomalous enhanced diffusion. A compilation of best-case R_{SH}-X_J data reported using various techniques (Fig. 8) contrasted against the 35-70 nm CMOS design windows shows that the SiGe process comfortably satisfies the end-of-roadmap R_{SH}-X_J requirements. In this technique, the junction depth for as-deposited and low-temperature annealed cases is determined solely by the recess etch depth. Thus, R_{SH} extends along an equi-resistivity line over the entire X_J range.

Comparison of statistical leakage data (@ -1 V) obtained for as-deposited and annealed $Si_{0.27}Ge_{0.73}$ and $Si_{0.55}Ge_{0.45}$ junctions (Fig. 9) with very conservative estimates of maximum allowable junction leakage for high performance and low power designs shows that the junction leakages fall well within the acceptable range. The maximum allowable leakage limits for each design were obtained by allowing only 1 % of the total I_{OFF} for the junction leakage and by using the appropriate areal and peripheral leakage components for a nominal device layout. The diborane partial pressure corresponds to chemical concentrations in the range of ~ 2 x 10^{20} to ~ 1 x 10^{22} cm^{-3}.

Temperature dependence of reverse leakage current for the as-deposited and annealed junctions are shown in Fig. 10 & 11. Over the entire projected range of device operation (@ -1 V, 25-100 °C) the leakage current is generation-dominated. At higher temperatures, the leakage shifts into a diffusion-dominated current for the annealed junctions. In order to determine the dominant leakage mechanisms for the as-deposited heterojunction, the I-V characteristics of the SiGe-Si heterojunction were derived. Using the energy-band

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diagram for a strained (p^+)SiGe/(n)Si hetero-junction (Fig. 12) and assuming the thermionic emission theory for a schottky barrier diode,

$$J \approx J_0\left(1-\frac{V}{V_{bi}}\right)\left[\exp\left(\frac{qV}{kT}\right)-1\right] \qquad (1)$$

where,

$$J_0 = \left(\frac{qA^*TV_{bi}}{k}\right)\exp\left(-\frac{qV_{bi}}{kT}\right) \qquad (2)$$

This yields a temperature dependent reverse leakage with a slope of –7701 K. Comparing the temperature dependence of these I-V characteristics with those of the heterojunction at -1 V (Fig. 13), a diffusion-dominated leakage mechanism is confirmed at higher temperatures. At higher biases (≥ 4 V), for both types of junctions, the mechanism shifts into band-to-band tunneling (substrate doping ~ 2 x10^{18} cm^{-3}).

The junction abruptness was determined using the reverse-bias C-V method (Fig. 14). The abruptness factor (m) - junction abruptness correlation was quantified using PISCES simulations to extract the abruptness factors for junctions with known abruptness values (Fig. 15). Comparing the locus of all extracted abruptness factors against this correlation, all as-deposited and 800 °C annealed junctions fall within 3 nm/decade.

Six-terminal kelvin structures (Fig. 16) were used to characterize the contact resistance (R_C) and contact resistivity (ρ_C). Contact formation was achieved by sputter-deposition of tungsten and subsequent annealing @ 700 °C, 30s. The resulting contacts were ohmic (Fig. 17). Fig. 18 plots ρ_C as a function of diborane partial pressure and %Ge. These values are *uncorrected* for 2-D current flow associated with kelvin structures and hence represent an upper bound. Contact resistivities as low as 1.5 x 10^{-8} Ω-cm^2 were achieved, satisfying the 35-nm technology node requirements. The 45 %Ge gave the lowest ρ_C owing to the reduced band-gap of strained $Si_{1-x-y}Ge_xB_y$ films. Strained growth is expected, based on the dramatic increase in the critical thickness (Fig. 19) of (boron-doped) SiGe films with percent levels of boron incorporation.

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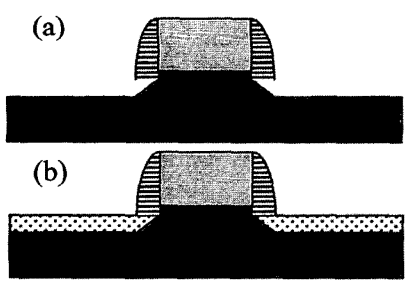


Figure 1: (a) Isotropic Si etch to define (extension) junction recess, (b) selective SiGe deposition @ 500 °C to form refilled junctions.

Figure 2: SEM image illustrating selectivity of SiGe deposition with respect to thermal oxide.

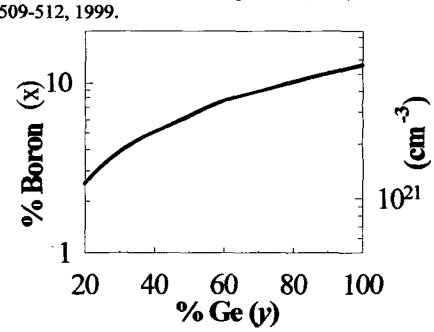


Figure 3: %B (cm^{-3}) versus %Ge for zero misfit in $Si_{1-x-y}Ge_xB_y$ with respect to Si.

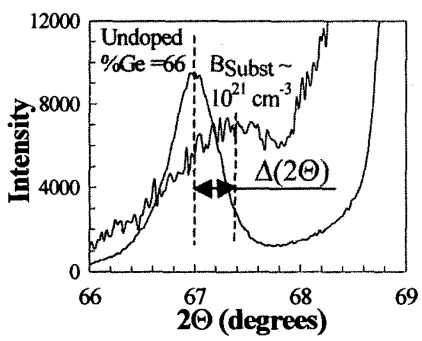
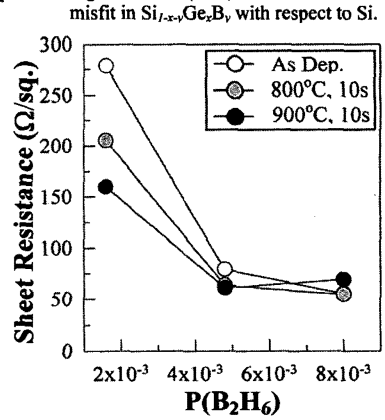


Figure 4: Angular shift between (400) peaks of XRD profiles of undoped and doped (10^{21} cm^{-3}) films with the same Si:Ge ratio (34:66), indicating the strain compensation effect.

Figure 5: Sheet Resistance of as-deposited & annealed $Si_{0.27}Ge_{0.73}$ films vs. diborane partial pressure.



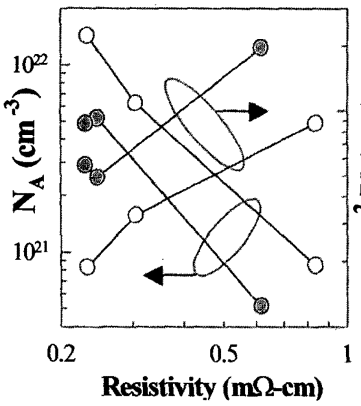


Figure 6: Carrier Density and Hall Mobility of as-deposited (White) and 800 °C, 10s annealed (Gray) $Si_{0.27}Ge_{0.73}$ films.

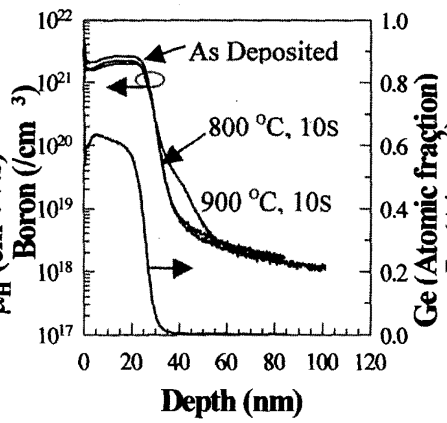


Figure 7: Boron & Ge SIMS profiles of as-deposited and annealed $Si_{0.27}Ge_{0.73}$ films.

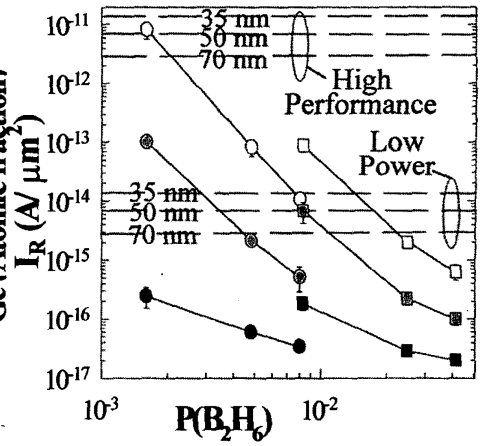


Figure 9: Statistical Reverse Leakage Data for SiGe Alloys. LEGEND: Circle – $Si_{0.27}Ge_{0.73}$, Square – $Si_{0.55}Ge_{0.45}$, White– As deposited, Gray – 800°C, 10s, Black – 900°C, 10s.

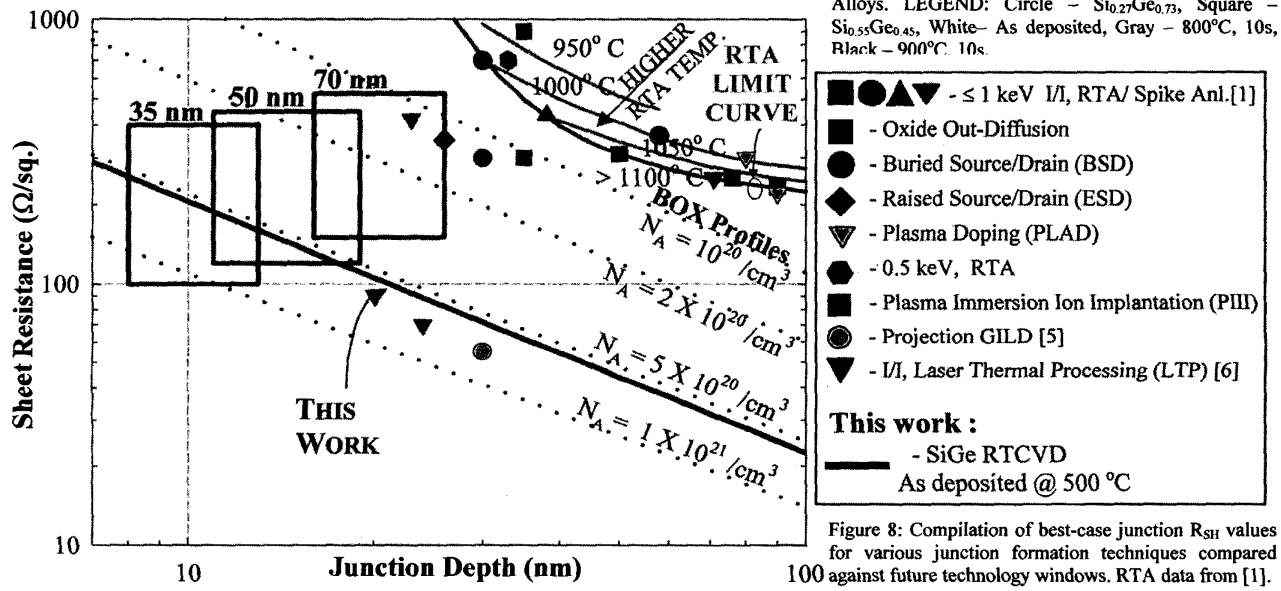


Figure 8: Compilation of best-case junction R_{SH} values for various junction formation techniques compared against future technology windows. RTA data from [1].

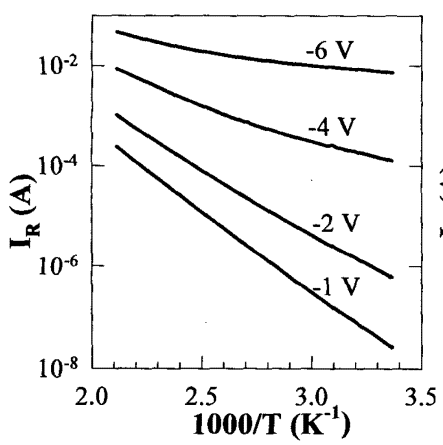


Figure 10: Temperature Dependence of Reverse Leakage Current for as-deposited $Si_{0.55}Ge_{0.45}$ junctions.

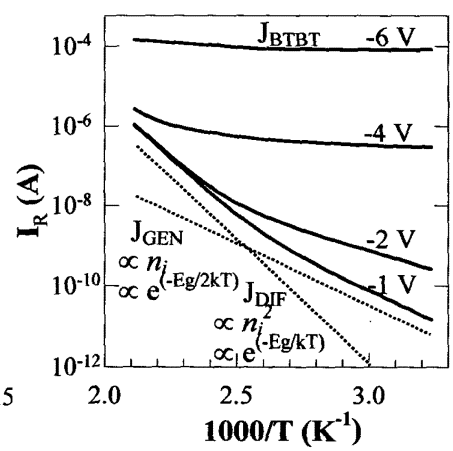


Figure 11: Temperature Dependence of Reverse Leakage Current for 900 °C, 10s annealed $Si_{0.55}Ge_{0.45}$ junctions.

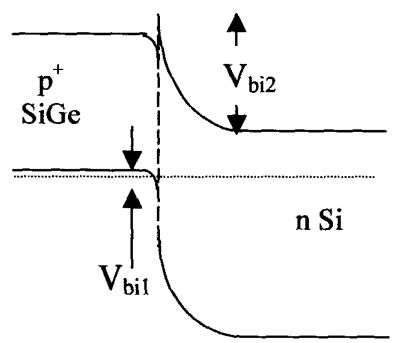


Figure 12: Band diagram of strained (p+)SiGe/(n)Si at thermal equilibrium.

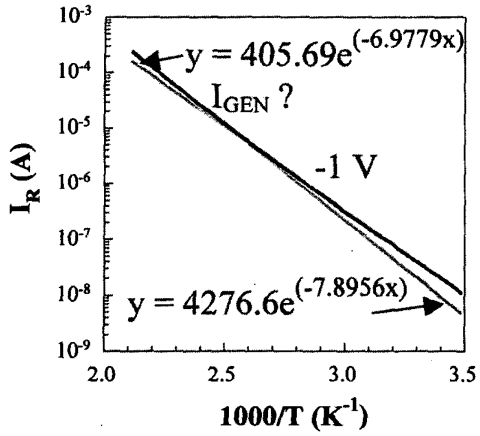


Figure 13: Temperature Dependence of Reverse Leakage Current for as-deposited $Si_{0.55}Ge_{0.45}$ junctions at –1 V. The I-V modeling yielded a I_R-T slope of 7701 K, closely matching the slope observed at high temperatures (-7895.6 K).

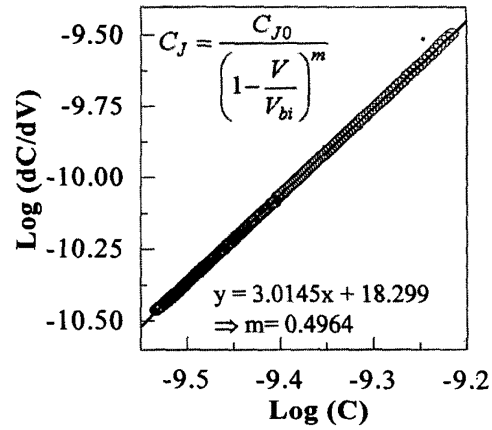


Figure 14: Junction Abruptness Extraction from reverse-bias C-V measurements.

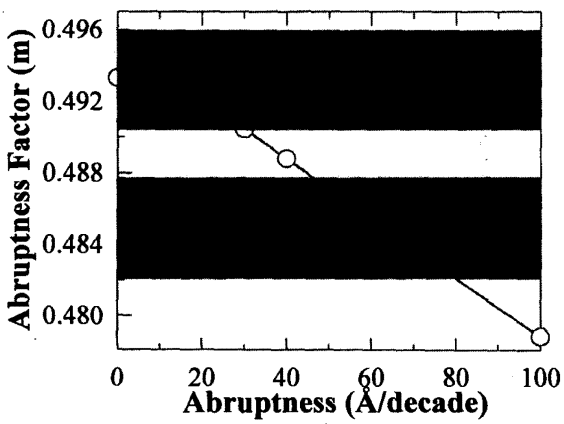


Figure 15: PISCES-extracted Abruptness factor-junction abruptness correlation compared against locus of all measured junction abruptness factors.

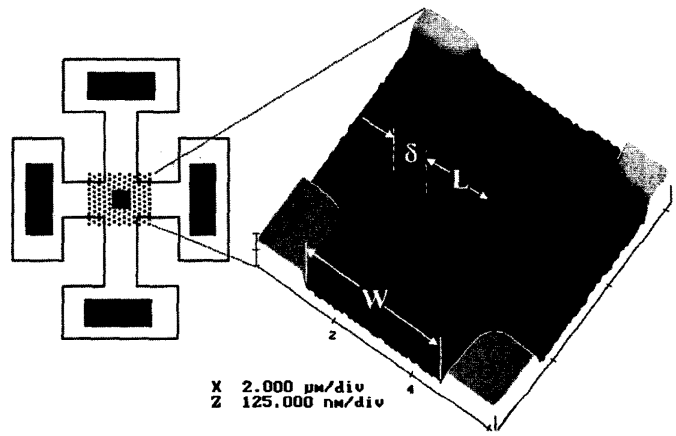


Figure 16: AFM image of 6-Terminal Kelvin Structure immediately prior to contact metal deposition.
L = 0.7, 1.0 & 1.5 µm; δ = 0.7 & 1.0 µm.

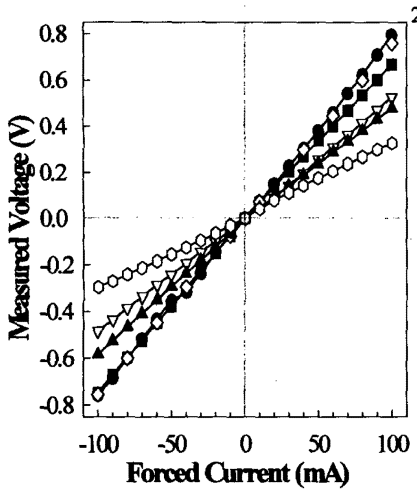


Figure 17: I-V indicating Ohmic SiGe-W(SiGe) Contacts.

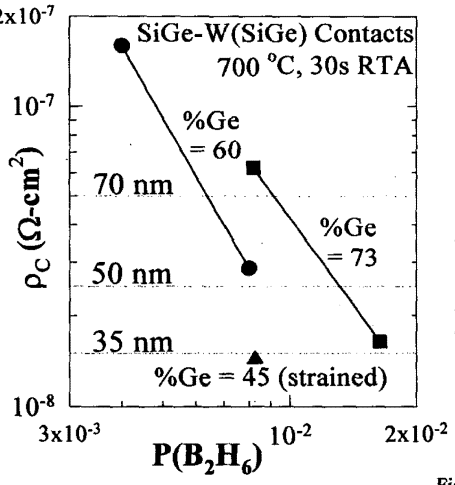


Figure 18: Uncorrected Specific Contact Resistivity of SiGe-W(SiGe) contacts vs %Ge & diborane partial pressure.

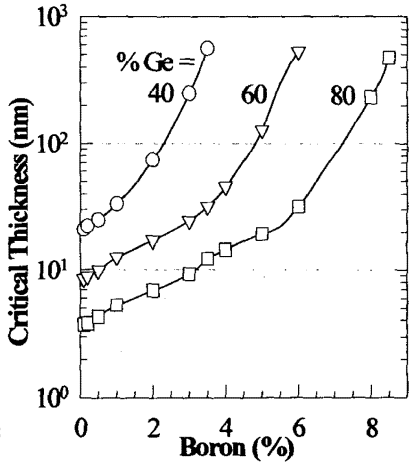


Figure 19: Calculations of critical thickness as a function of %Ge & %B in a SiGeB alloy, based on equivalent %misfit of a SiGe alloy.