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Lin et al.

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(54) **METHOD FOR FABRICATING A FINFET DEVICE**

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(22) Filed: **Nov. 9, 2012**

(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation of application No. 12/703,918, filed on Feb. 11, 2010, now Pat. No. 8,310,013.

(51) **Int. Cl.**
H01L 21/336 (2006.01)

(52) **U.S. Cl.**
USPC **438/198**

(58) **Field of Classification Search**
USPC 438/198
See application file for complete search history.

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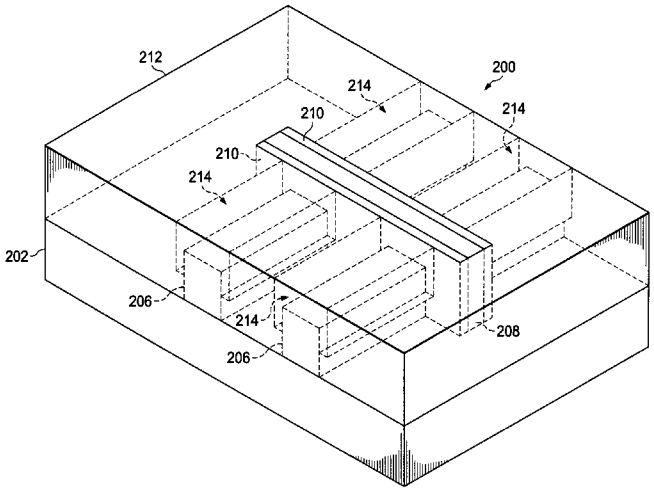
(57) **ABSTRACT**

A FinFET device and method for fabricating a FinFET device is disclosed. An exemplary method includes forming a fin structure on a semiconductor substrate and forming a gate structure on the fin structure. A capping layer is then formed over the semiconductor substrate, fin structure, and gate structure. The capping layer is patterned to form an opening exposing a second portion of the fin structure. An epitaxial layer is grown in the opening and on the second portion of the fin structure. At least one of a source region and a drain region is provided in the epitaxial layer. The method may continue to remove the capping layer.

20 Claims, 18 Drawing Sheets



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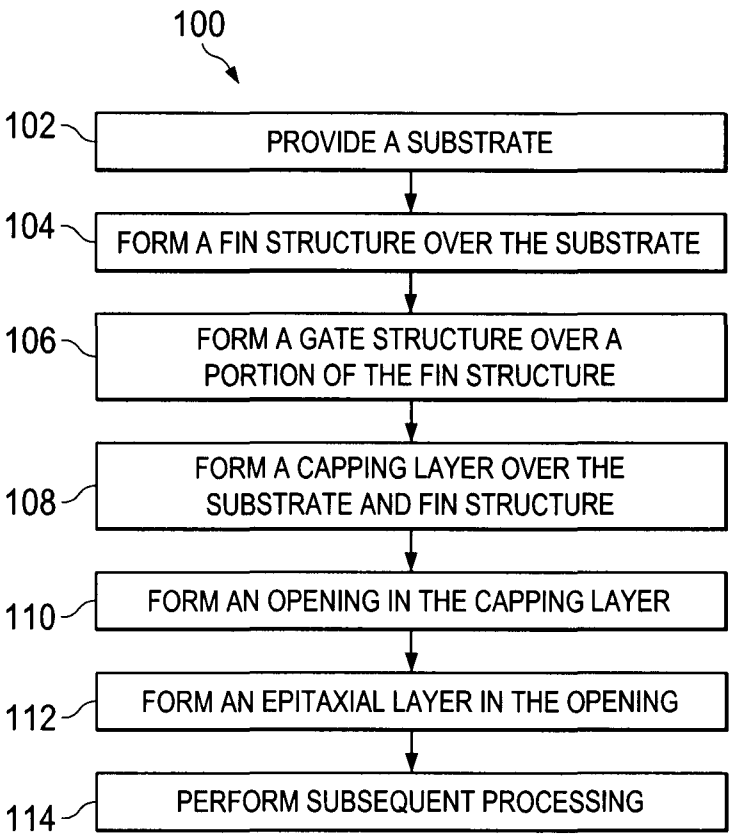
100
102
PROVIDE A SUBSTRATE
104
FORM A FIN STRUCTURE OVER THE SUBSTRATE
106
FORM A GATE STRUCTURE OVER A PORTION OF THE FIN STRUCTURE
108
FORM A CAPPING LAYER OVER THE SUBSTRATE AND FIN STRUCTURE
110
FORM AN OPENING IN THE CAPPING LAYER
112
FORM AN EPITAXIAL LAYER IN THE OPENING
114
PERFORM SUBSEQUENT PROCESSING

Fig. 1

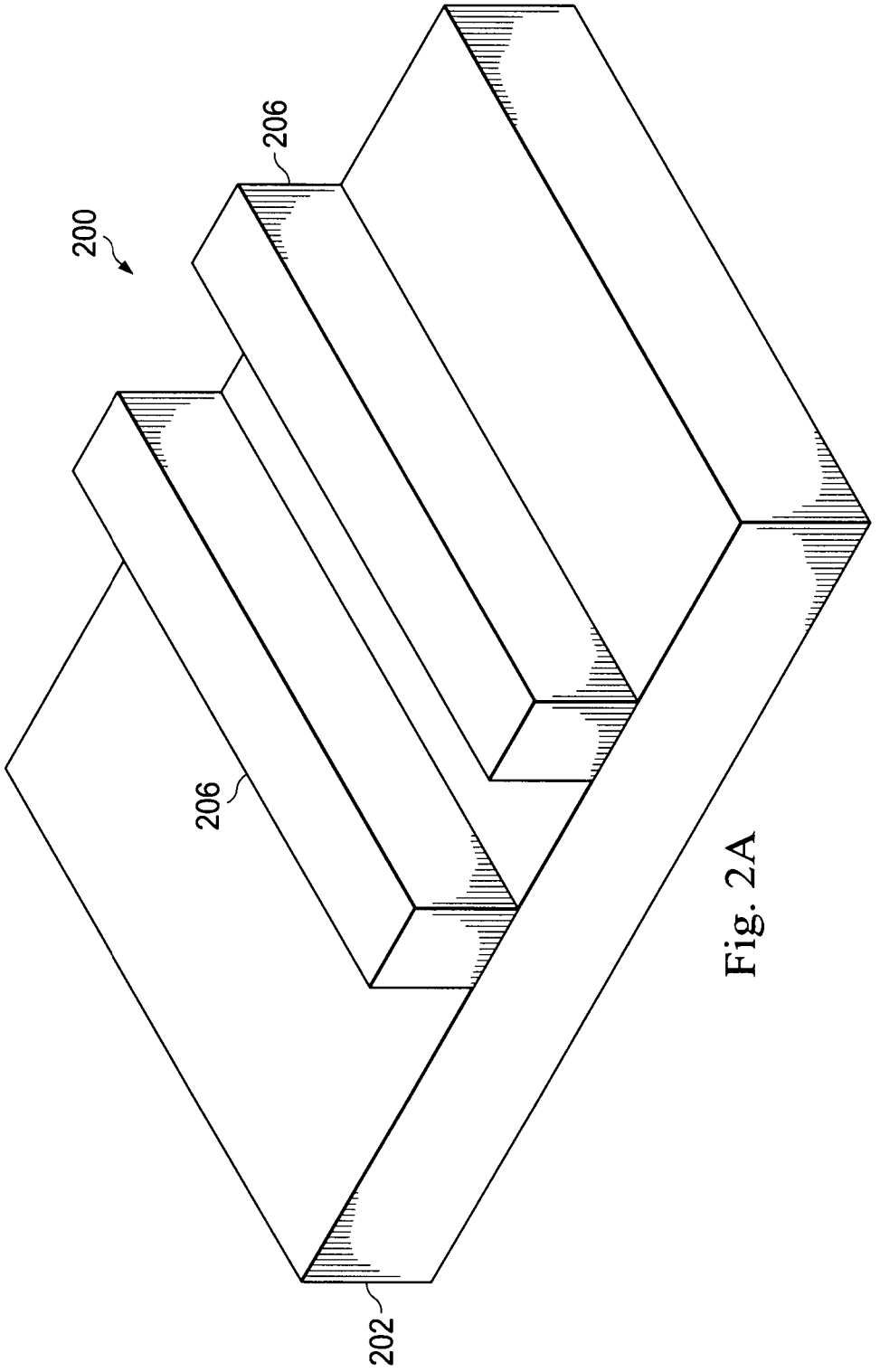

Fig. 2A

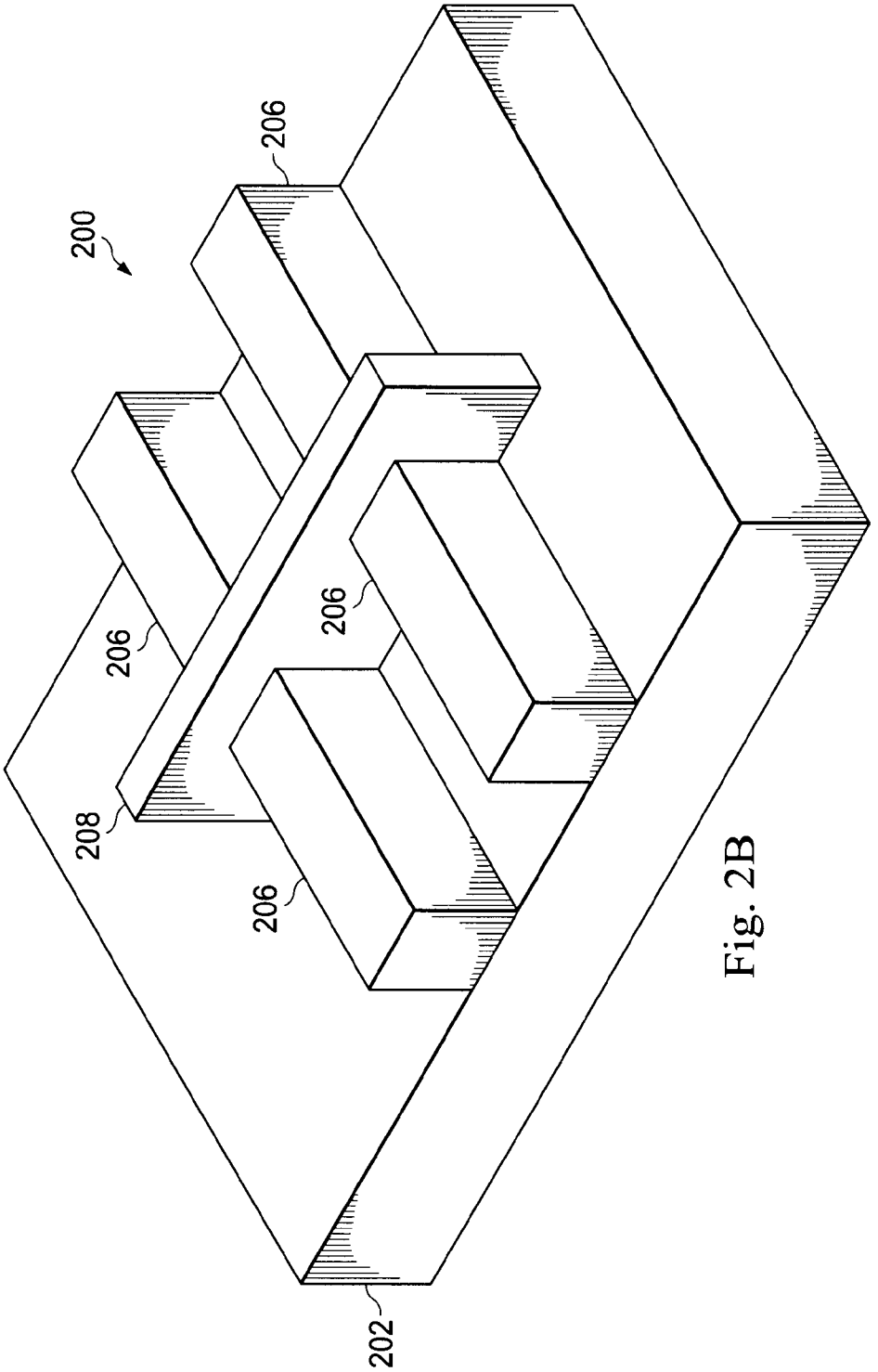

Fig. 2B

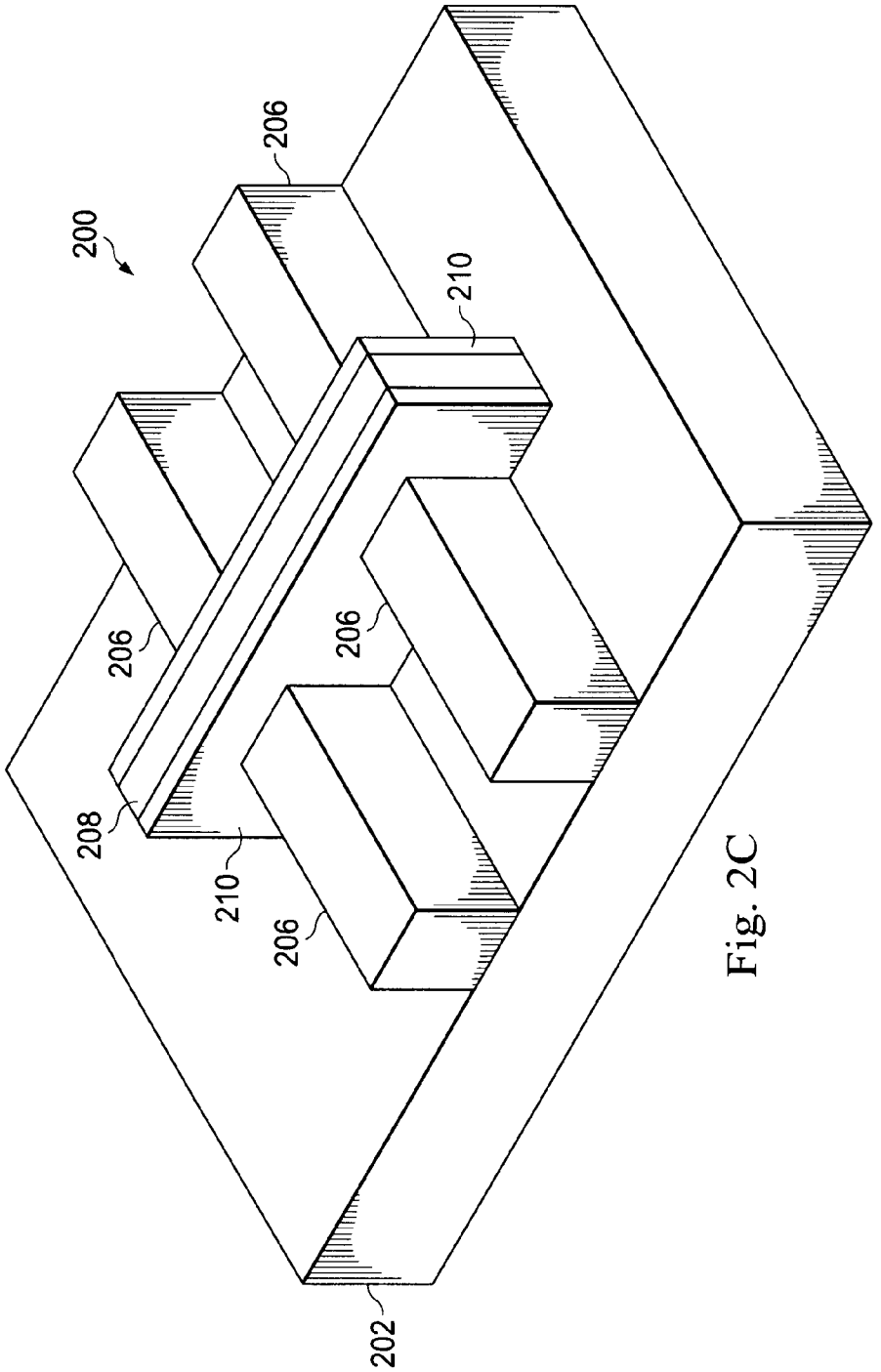

Fig. 2C

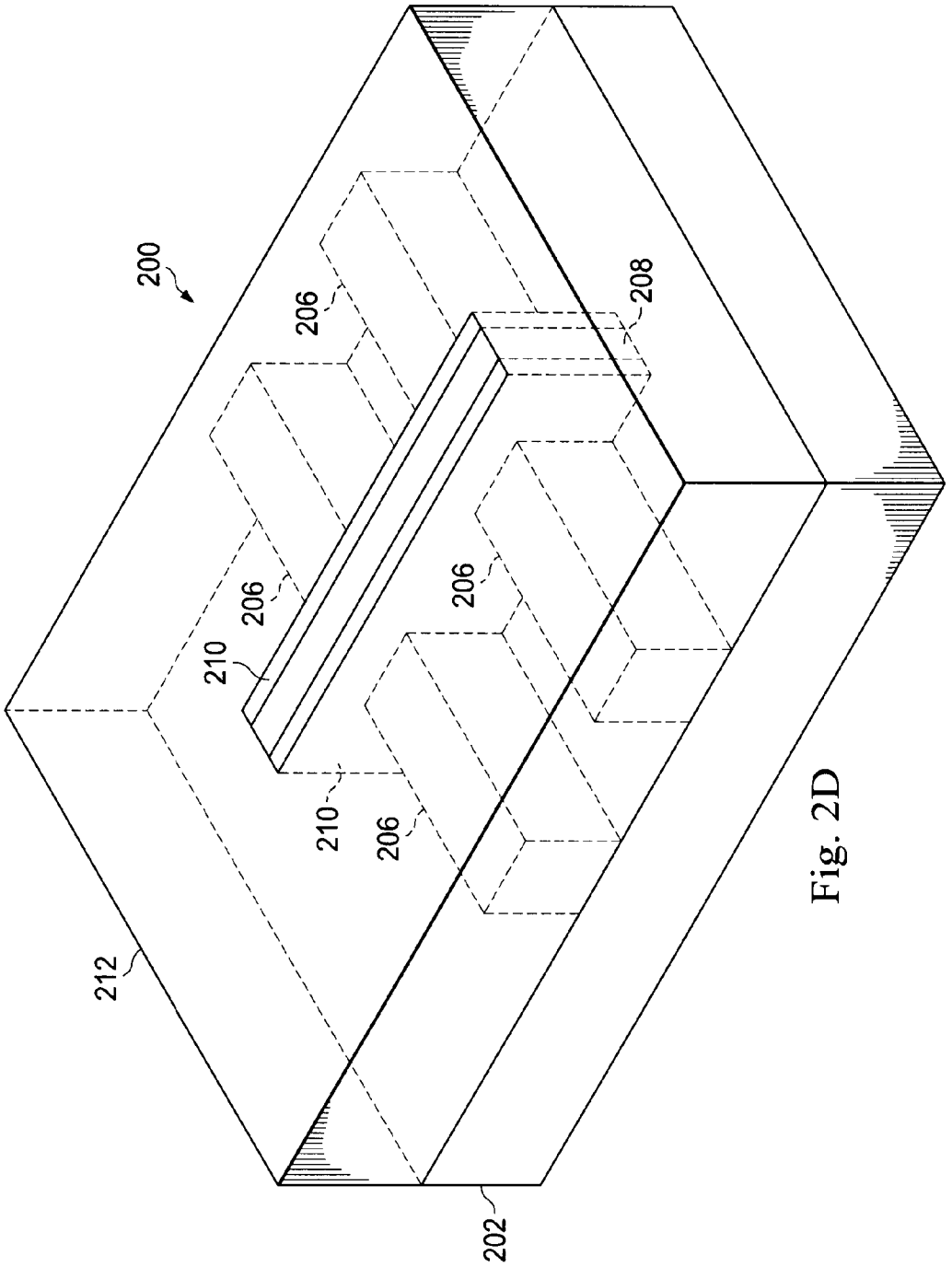

Fig. 2D

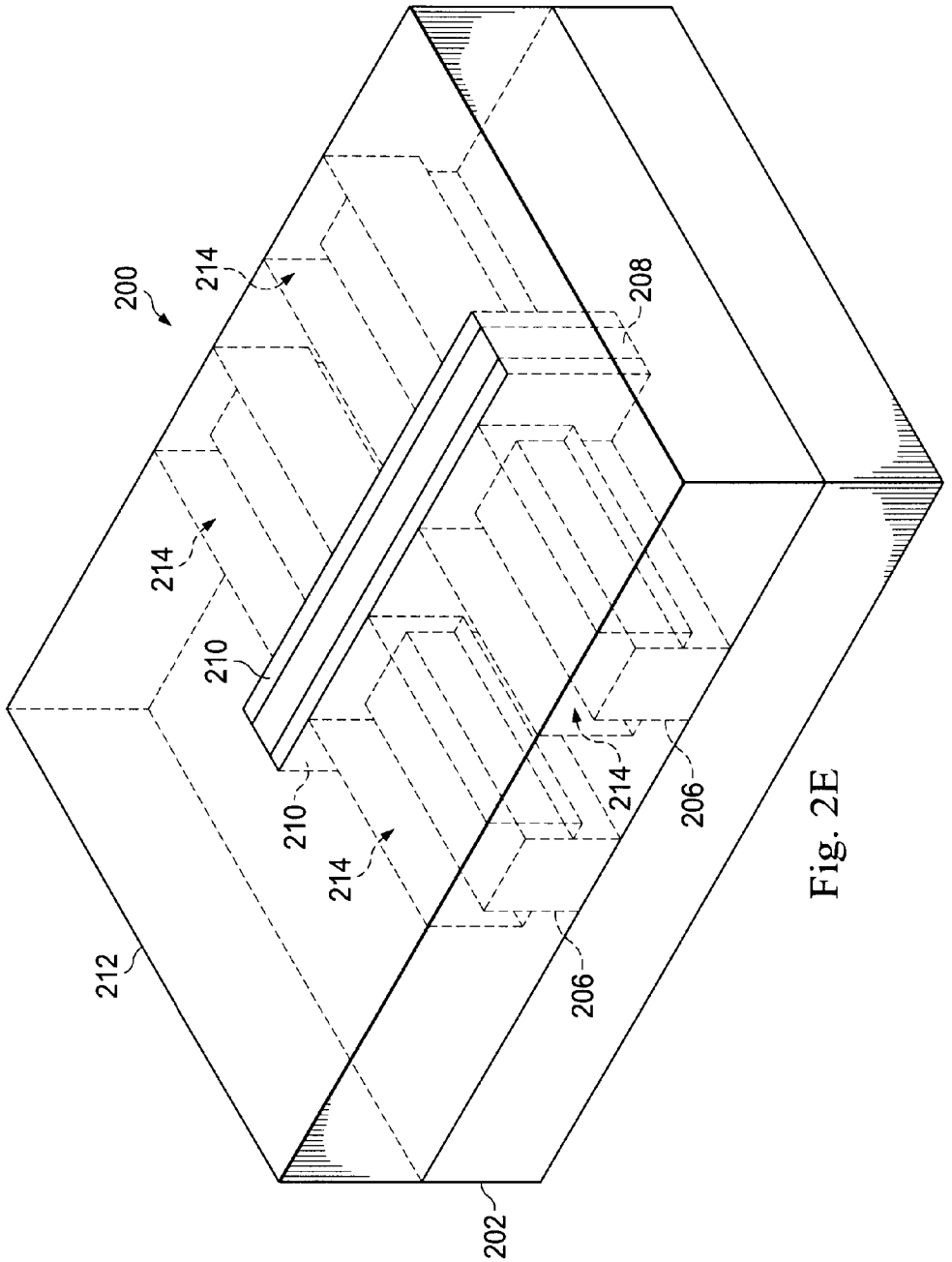

Fig. 2E

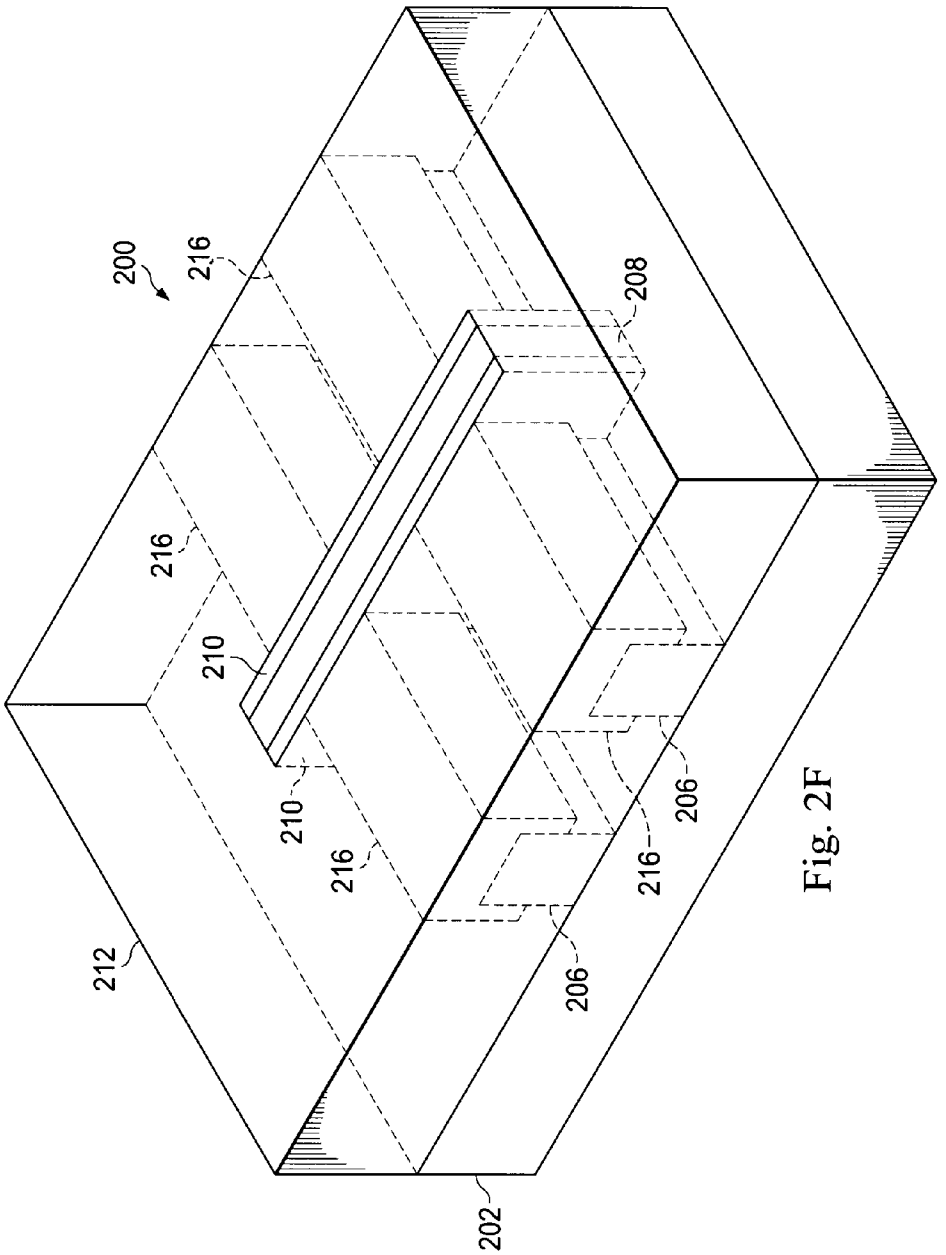

Fig. 2F

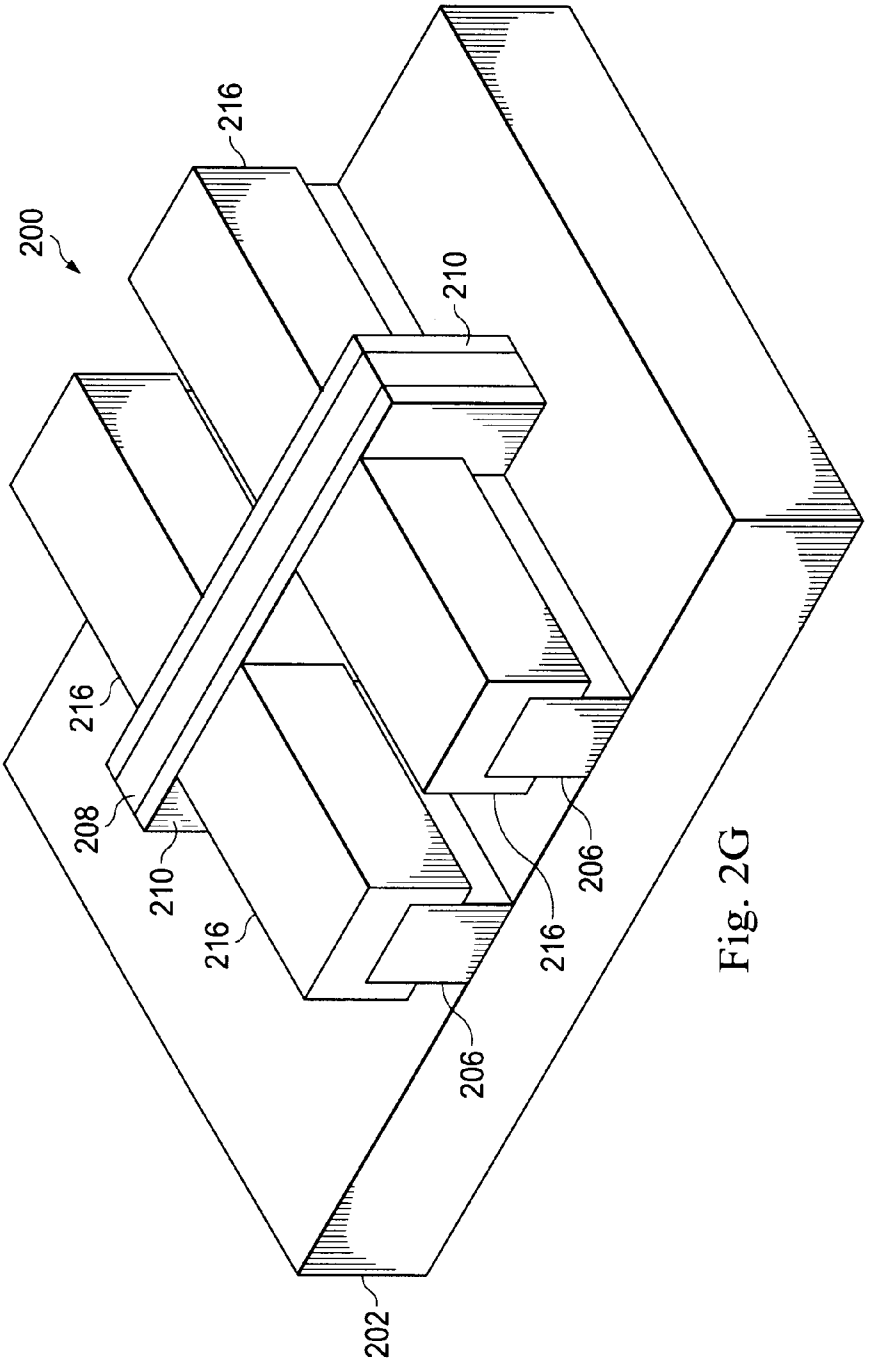

Fig. 2G

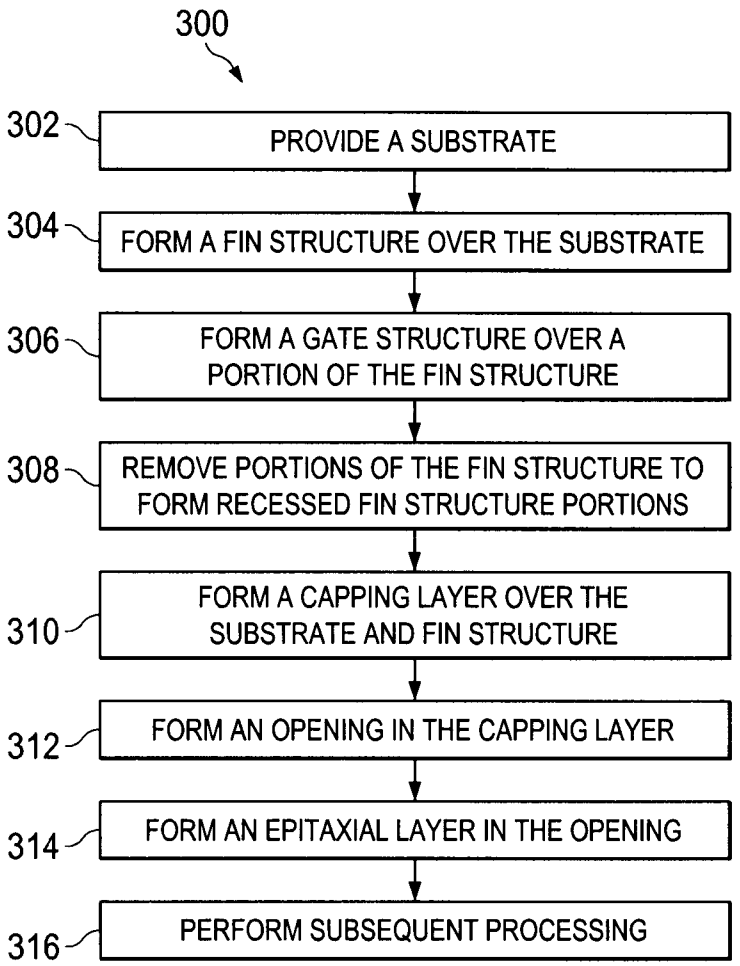
300
302
PROVIDE A SUBSTRATE
304
FORM A FIN STRUCTURE OVER THE SUBSTRATE
306
FORM A GATE STRUCTURE OVER A PORTION OF THE FIN STRUCTURE
308
REMOVE PORTIONS OF THE FIN STRUCTURE TO FORM RECESSED FIN STRUCTURE PORTIONS
310
FORM A CAPPING LAYER OVER THE SUBSTRATE AND FIN STRUCTURE
312
FORM AN OPENING IN THE CAPPING LAYER
314
FORM AN EPITAXIAL LAYER IN THE OPENING
316
PERFORM SUBSEQUENT PROCESSING

Fig. 3

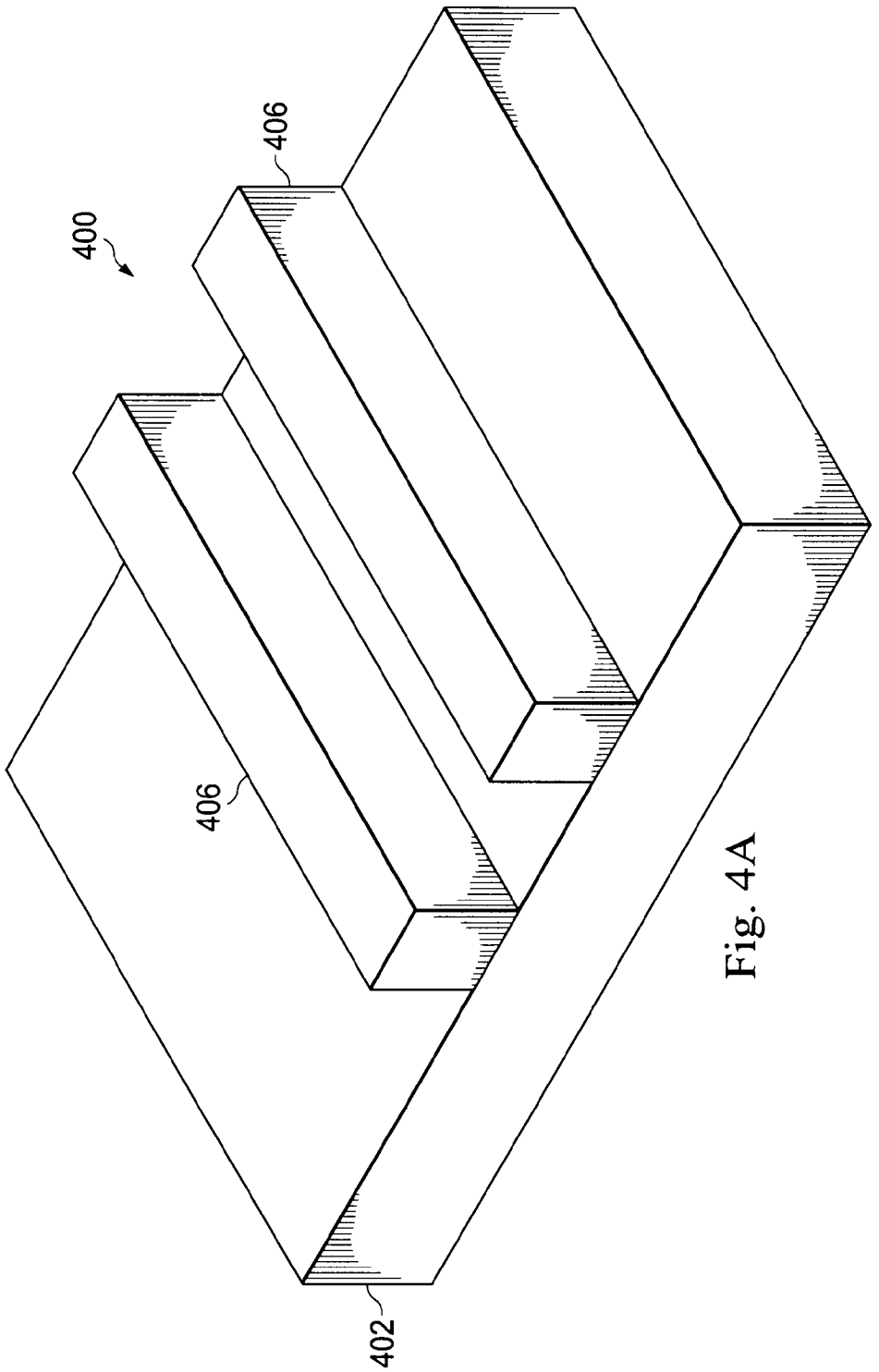

Fig. 4A

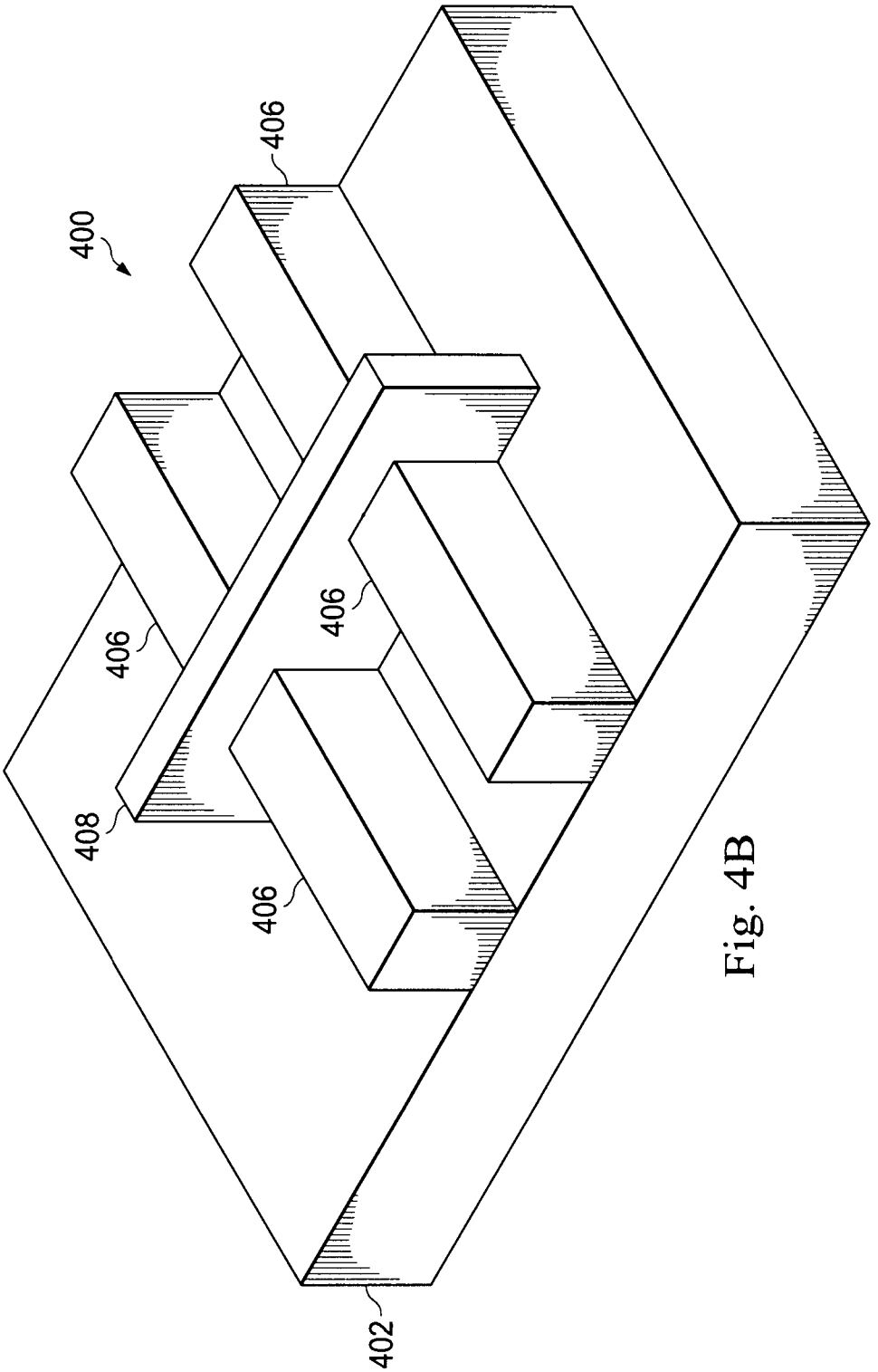

Fig. 4B

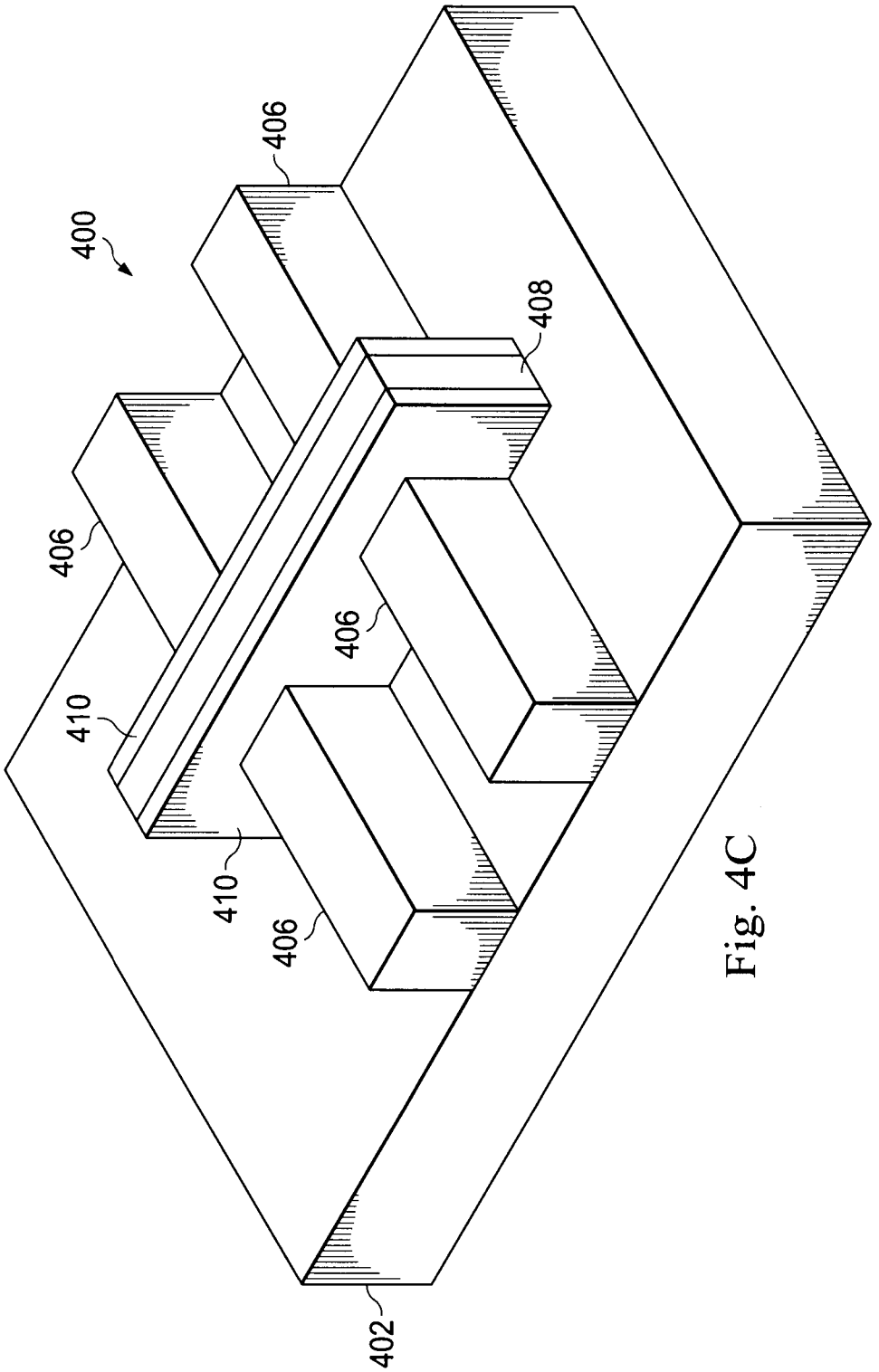

Fig. 4C

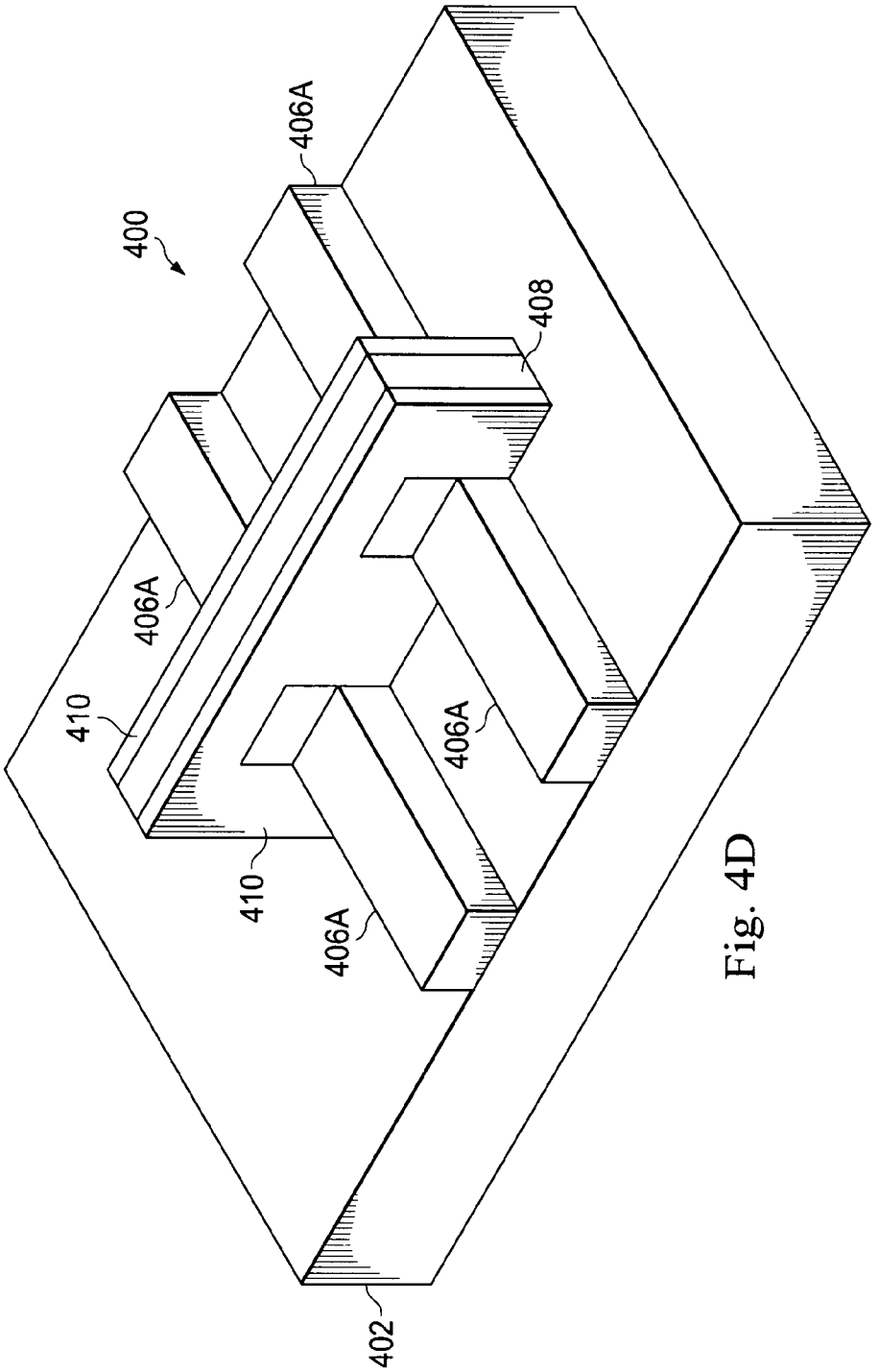

Fig. 4D

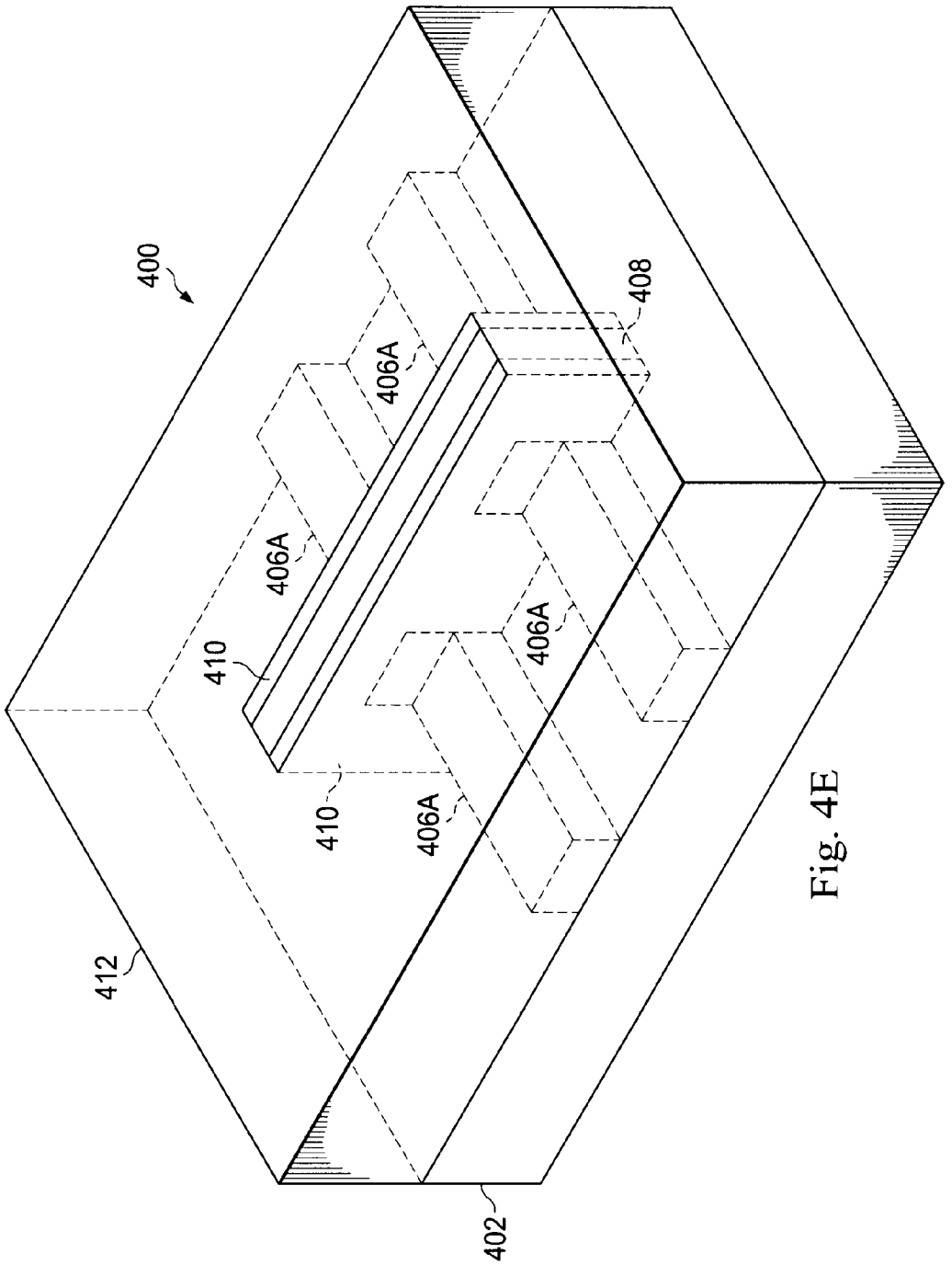

Fig. 4E

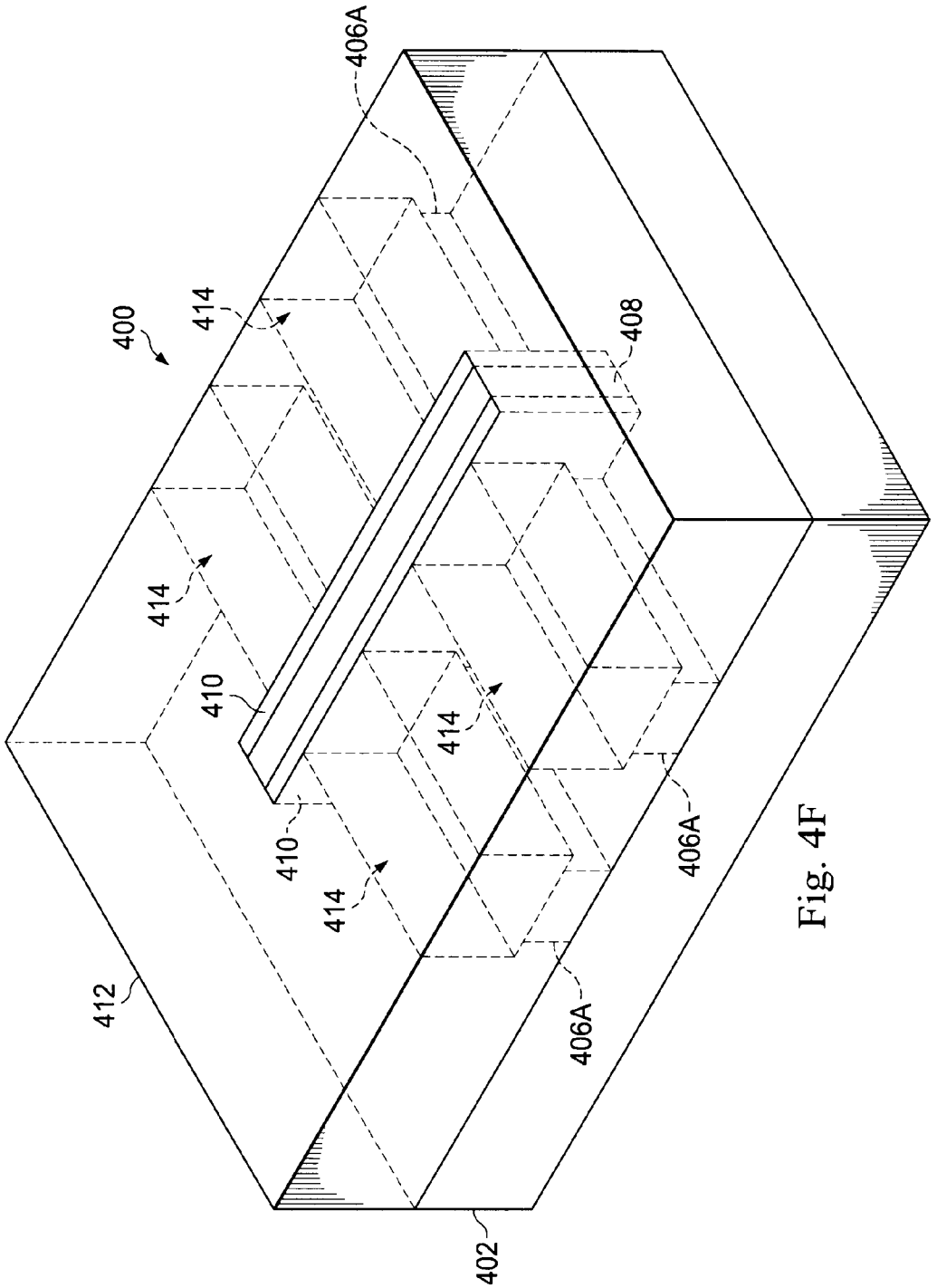

Fig. 4F

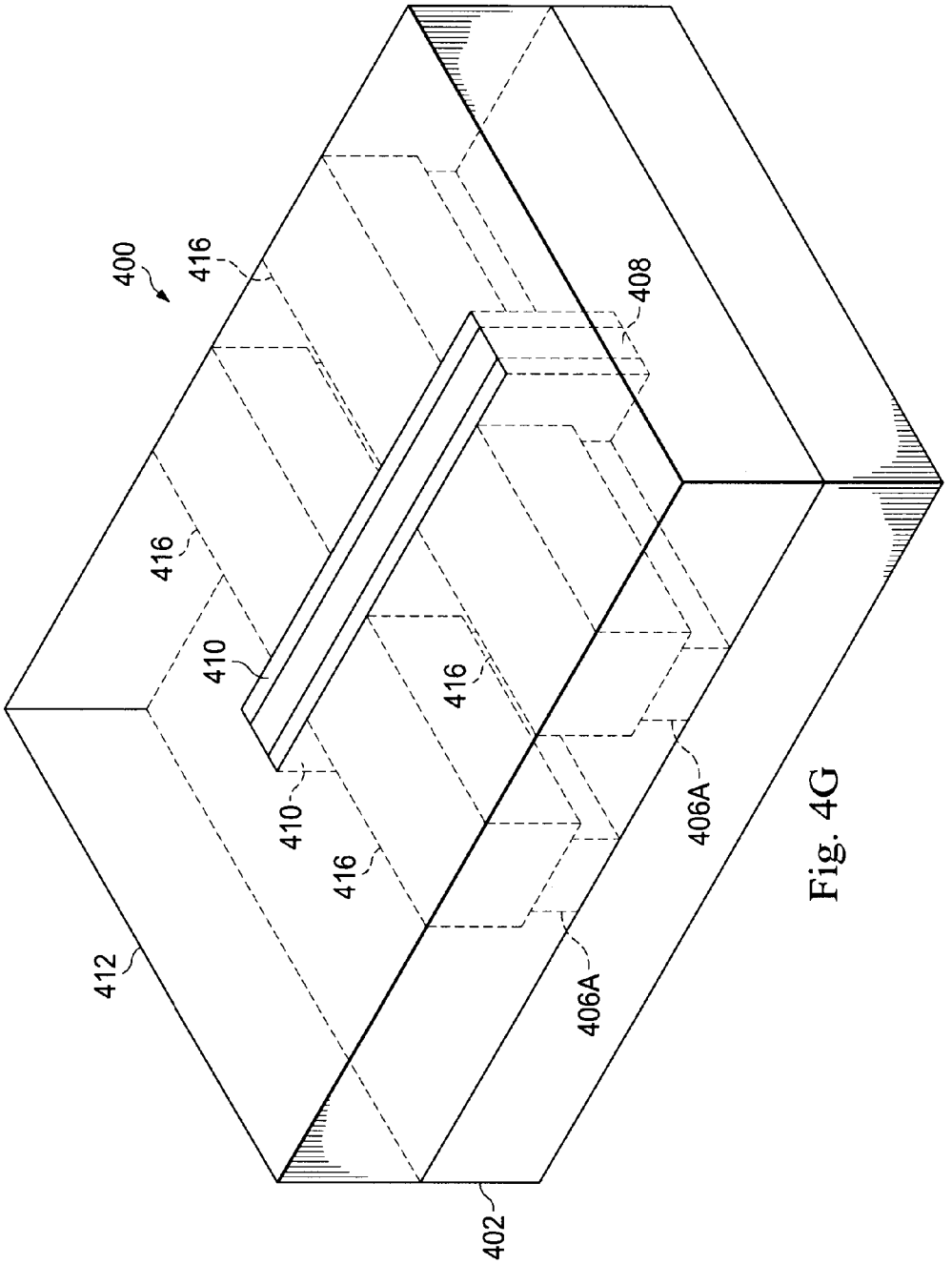

Fig. 4G

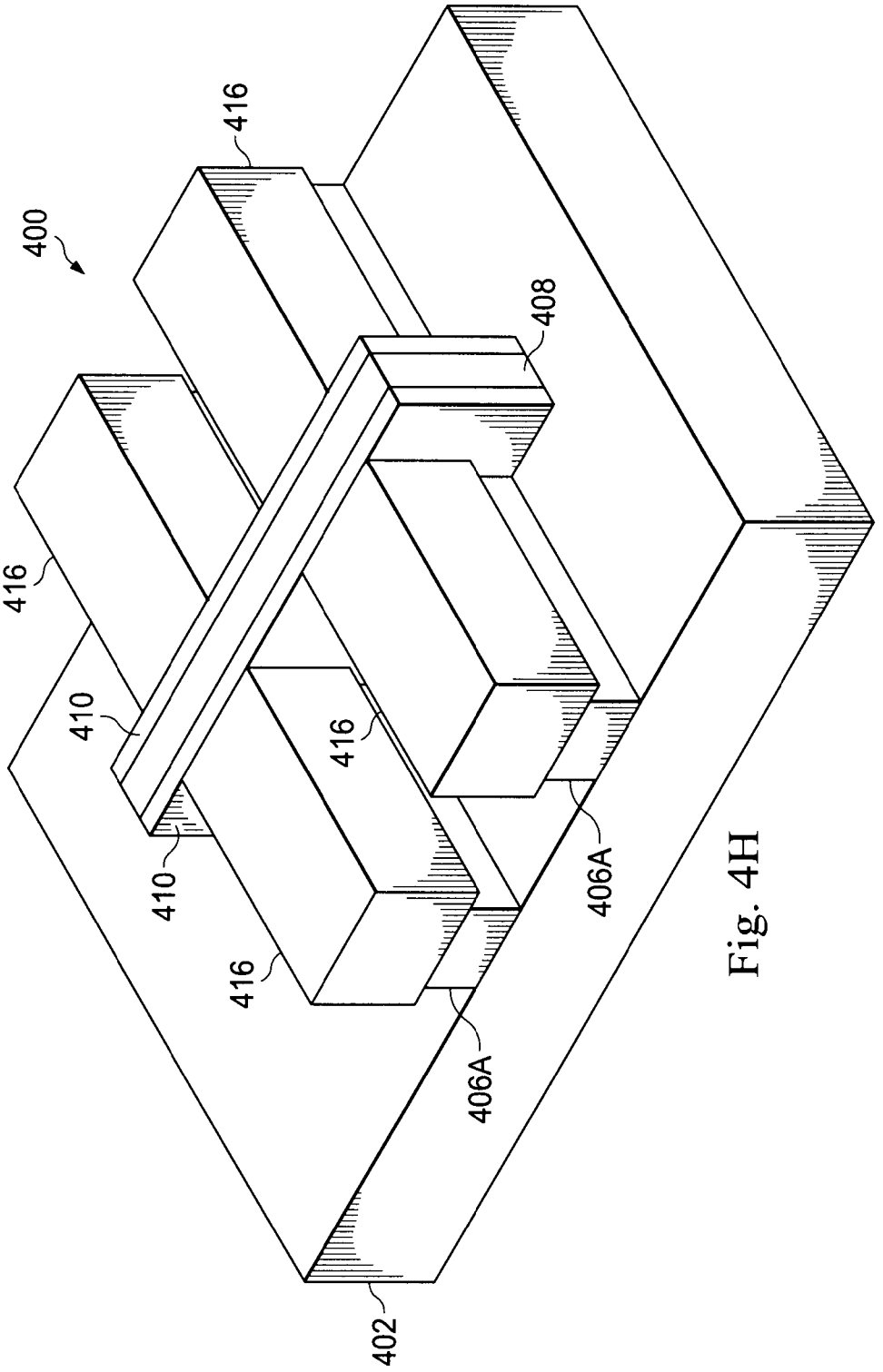

Fig. 4H

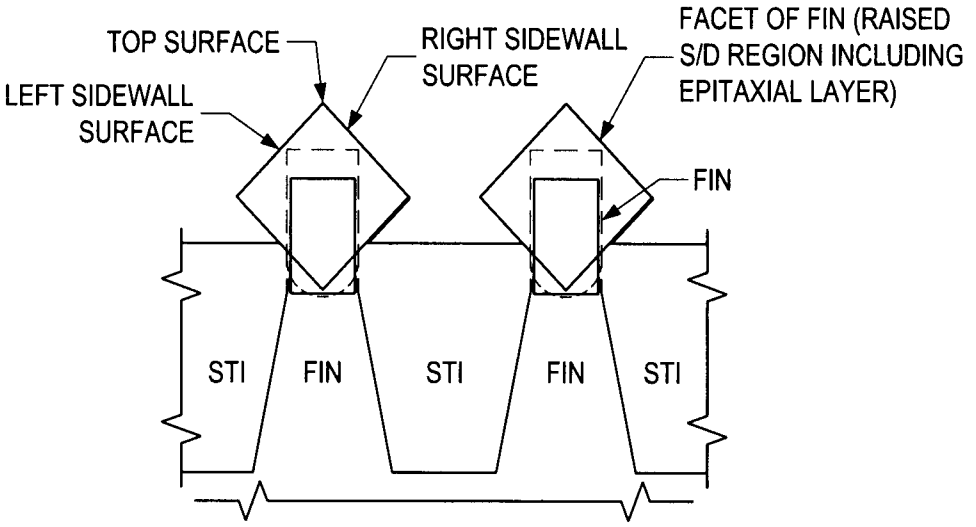
TOP SURFACE
RIGHT SIDEWALL SURFACE
FACET OF FIN (RAISED S/D REGION INCLUDING EPITAXIAL LAYER)
LEFT SIDEWALL SURFACE
FIN
STI
FIN
STI
FIN
STI

Fig. 5A

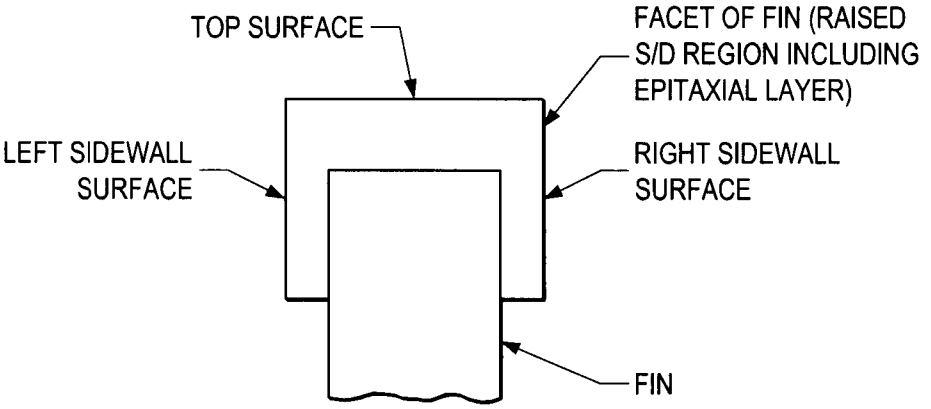
TOP SURFACE
FACET OF FIN (RAISED S/D REGION INCLUDING EPITAXIAL LAYER)
LEFT SIDEWALL SURFACE
RIGHT SIDEWALL SURFACE
FIN

Fig. 5B

METHOD FOR FABRICATING A FINFET DEVICE

PRIORITY DATA

This application is a continuation application of Ser. No. 12/703,918, filed on Feb. 11, 2010, entitled "Method For Fabricating A Finfet Device," the entire disclosure of which is incorporated herein by reference.

BACKGROUND

As the semiconductor industry has progressed into nanometer technology process nodes in pursuit of higher device density, higher performance, and lower costs, challenges from both fabrication and design issues have resulted in the development of three dimensional designs, such as a fin-like field effect transistor (FinFET). A typical FinFET is fabricated with a thin "fin" (or fin structure) extending from a substrate, for example, etched into a silicon layer of the substrate. The channel of the FET is formed in this vertical fin. A gate is provided over (e.g., wrapping) the fin. It is beneficial to have a gate on both sides of the channel allowing gate control of the channel from both sides. Further advantages of FinFET devices include reducing the short channel effect and higher current flow.

As device structures become more dense, there have been problems associated with fabrication of FinFET devices. For example, conventional FinFET device fabrication methods are unable to provide varied profiles, such as a square profile, of facets (e.g., Si or SiGe facets) of the fin structure. Simply changing various process settings has proved incapable of significantly improving the ability to fabricate varied profiles. The facet profile affects a contact salicidation area, which in conventional FinFET devices may be smaller than desirable, resulting in higher than desirable salicide contact resistance, and thus poor device performance. Further, in conventional FinFET device fabrication methods, a fin structure height is limited by a fin structure width, for example, because of faceting. As devices become smaller, the fin structure height limitation further exacerbates the shrinking contact salicidation area issue. Accordingly, an improved FinFET device and improved method for fabricating a FinFET device is desired.

SUMMARY

The present disclosure provides for many different embodiments. An exemplary FinFET device can include a substrate of a crystalline semiconductor material having a top surface of a first crystal plane orientation; a fin structure of the crystalline semiconductor material overlying the substrate; a gate structure over a portion of the fin structure; an epitaxy layer over another portion of the fin structure, the epitaxy layer having a surface having a second crystal plane orientation, wherein the epitaxy layer and underlying fin structure include a source and drain region, the source region being separated from the drain region by the gate structure; and a channel defined in the fin structure from the source region to the drain region, and aligned in a direction parallel to both the surface of the epitaxy layer and the top surface of the substrate.

Another exemplary FinFET device fabricated by the methods described herein can include a substrate including a fin structure, wherein the substrate is crystalline silicon and has a top surface with a first crystallographic plane orientation; a gate structure disposed on a portion of the fin structure, the gate structure traversing the fin structure; an epitaxy layer formed over another portion of the fin structure, wherein the epitaxy layer has first, second, and third surfaces, the first surface being parallel to the top surface of the substrate, and the second and third surfaces being perpendicular to the first surface and having a second crystallographic plane orientation; and a source and drain region in the epitaxy layer that defines a channel in the fin structure from the source region to the drain region, the channel being aligned in a direction defined by an intersection line between the first surface and the second surface.

Yet another exemplary FinFET device includes a semiconductor substrate having a fin structure disposed thereover, the fin structure having a top surface parallel to a top surface of the semiconductor substrate, the top surfaces having a (001) crystal plane orientation; a gate structure traversing the fin structure, the gate structure separating a source region and a drain region of the fin structure, wherein the source and drain region define a channel therebetween and aligned in a <110> direction; and the source and drain region including an epitaxial layer having a top surface and two sidewall surfaces, wherein the top surface has a (001) crystal plane orientation, and the two sidewall surfaces can have a (110) crystal plane orientation.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** is a flow chart of a method for fabricating an integrated circuit device according to aspects of the present disclosure; and

FIGS. **2**A-**2**G are various cross-sectional views of embodiments of an integrated circuit device during various fabrication stages according to the method of FIG. **1**.

FIG. **3** is a flow chart of a method for fabricating an integrated circuit device according to aspects of the present disclosure; and

FIGS. **4**A-**4**H are various cross-sectional views of embodiments of an integrated circuit device during various fabrication stages according to the method of FIG. **3**.

FIGS. **5**A-**5**B illustrate various cross-sectional views along a channel of a fin structure according to one or more embodiments.

DETAILED DESCRIPTION

The present disclosure relates generally to semiconductor devices, and more particularly, to a FinFET device and methods of fabricating a FinFET device (e.g., element or portion of a device/element).

It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In

addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

With reference to FIGS. **1**, **2**A-**2**G, **3**, and **4**A-**4**H, methods **100**, **300** and semiconductor devices **200**, **400** are collectively described below. The semiconductor devices **200**, **400** illustrate a FinFET device (e.g., transistor) or any portion thereof (e.g., a fin). As employed in the present disclosure, the term FinFET device refers to any fin-based, multi-gate transistor. The FinFET devices **200**, **400** may be included in a microprocessor, memory cell, and/or other integrated circuit devices. It is understood that additional steps can be provided before, during, and after the methods **100**, **300**, and some of the steps described below can be replaced or eliminated, for additional embodiments of the methods. It is further understood that additional features can be added in the semiconductor devices **200**, **400**, and some of the features described below can be replaced or eliminated, for additional embodiments of the semiconductor devices **200**, **400**.

FIG. **1** illustrates a flow chart of an embodiment of the method **100** to fabricate the FinFET device **200**. Referring to FIGS. **1** and **2**A, at block **102**, a substrate (wafer) **202** is provided. The substrate **202** comprises silicon in a crystalline structure. The substrate **202** comprises any suitable crystallographic orientation (e.g., a (100), (110), or (111) crystallographic orientation). The substrate **202** may further include a notch aligned along any suitable direction (e.g., a <110> or <100> direction). In the present embodiment, the substrate **202** includes a top surface having a (001) crystalline (plane) orientation. In another embodiment, the substrate **202** includes a (001) crystallographic (plane) orientation with a notch aligned in a <110> direction. Alternatively, the substrate **202** comprises other suitable elementary semiconductors, such as germanium in crystal; a compound semiconductor, such as silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; or combinations thereof. Alternatively, the substrate **202** includes a silicon-on-insulator (SOI) substrate. The SOI substrate can be fabricated using separation by implantation of oxygen (SIMOX), wafer bonding, and/or other suitable methods. The substrate **202** may include isolation regions, various doped regions, other suitable features, and/or combinations thereof.

At block **104**, a fin structure **206** is formed over the substrate **202**. The exemplary fin structure **206** comprises one or more fins. The fins comprise any suitable material, for example, the fin structure **206** comprises one or more silicon fins (Si-fin). As illustrated in FIG. **2**A, the fin structure **206** exhibits a rectangular shape with a top surface that is parallel to a top surface of the substrate **202**. Accordingly, the top surface of the fin structure **206** may have a (001) crystallographic plane orientation, similar to the substrate **202**. The rectangular-shaped fin structure **206** can also include a right and left sidewall surfaces perpendicular to the top surfaces of the fin structure **206** and/or substrate **202**.

The fin structure **206** is formed by any suitable process including various deposition, photolithography, and/or etching processes. An exemplary photolithography process may include forming a photoresist layer (resist) overlying the substrate (e.g., on a silicon layer), exposing the resist to a pattern, performing a post-exposure bake process, and developing the resist to form a masking element including the resist. The masking element may then be used to etch the fin structure into the silicon layer. The fin structure may be etched using reactive ion etching (RIE) processes and/or other suitable processes. In an example, the fin structure **206** may be formed, for example, by etching a layer of silicon on the substrate. The layer of silicon may be a silicon layer of a SOI substrate (e.g., overlying an insulator layer). The fin structure **206** may further include a capping layer disposed on the fins. The capping layer may include a silicon capping layer. It is understood that multiple parallel fin structures may be formed in a similar manner.

Alternatively, the fin structure **206** is formed by a double-patterning lithography (DPL) process. DPL is a method of constructing a pattern on a substrate by dividing the pattern into two interleaved patterns. DPL allows enhanced feature (e.g., fin) density. Various DPL methodologies may be used including double exposure (e.g., using two mask sets), forming spacers adjacent features and removing the features to provide a pattern of spacers, resist freezing, and/or other suitable processes.

Referring to FIGS. **1** and **2**B, at block **106**, a gate structure **208** is formed over a portion of the fin structure **206**. The gate structure **208** traverses the fin structure **206**. In the present embodiment, the gate structure **208** is formed over a central portion of the fin structure **206**. The gate structure **208** includes one or more material layers, such as interfacial layers, capping layers, diffusion/barrier layers, dielectric layers, electrode layers, conductive layers, other suitable layers, and/or combinations thereof. For example, the gate structure **208** may include a gate dielectric layer and a gate electrode. The gate dielectric layer comprises a dielectric material, such as silicon oxide, silicon nitride, high-k dielectric material, other suitable dielectric material, and/or combinations thereof. Examples of high-k dielectric material include HfO_2, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, zirconium oxide, aluminum oxide, hafnium dioxide-alumina (HfO_2—Al_2O_3) alloy, other suitable high-k dielectric materials, and/or combinations thereof. The gate electrode includes any suitable material, such as polysilicon, aluminum, copper, titanium, tantalum, tungsten, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, metal alloys, other suitable materials, and/or combinations thereof.

The gate structure **208** is formed by any suitable process. For example, the gate structure **208** is formed by a procedure including deposition, photolithography patterning, and etching processes. The deposition processes include chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), high density plasma CVD (HDPCVD), metal organic CVD (MOCVD), remote plasma CVD (RPCVD), plasma enhanced CVD (PECVD), low-pressure CVD (LPCVD), atomic layer CVD (ALCVD), atmospheric pressure CVD (APCVD), plating, other suitable methods, and/or combinations thereof. The photolithography patterning processes include photoresist coating (e.g., spin-on coating), soft baking, mask aligning, exposure, post-exposure baking, developing the photoresist, rinsing, drying (e.g., hard baking), other suitable processes, and/or combinations thereof. Alternatively, the photolithography exposing process is implemented or replaced by other proper methods such as maskless photolithography, electron-beam writing, and ion-beam writing. The etching processes include dry etching, wet etching, and/or other etching methods (e.g., reactive ion etching).

The gate structure **208** may further include spacers **210** as illustrated in FIG. **2**C. The spacers **210** are formed by any suitable process to any suitable thickness. The spacers **210**, which are positioned on each side of the gate structure **208**, may comprise a nitride material (e.g., silicon nitride). In various examples, the spacers **210** comprise a dielectric mate-

rial, such as silicon nitride, silicon carbide, silicon oxynitride, other suitable materials, and/or combinations thereof.

Various doped regions, such as source and drain (S/D) regions, can be formed in the fin structure **206**. The S/D regions can include lightly doped S/D regions (LDD regions) and/or heavily doped S/D regions (HDD regions). The gate structure **208** traversing the fin structure **206** can separate the various doped regions. For example, the gate structure **208** can separate a source region and a drain region of the fin structure **206**. The doping species may depend on the type of device being fabricated, such as an NMOS or PMOS device. The doping species include p-type dopants, such as boron or BF_2; n-type dopants, such as phosphorus or arsenic; and/or combinations thereof. The S/D regions may comprise various doping profiles. The doped regions may be formed by implantation processes, diffusion process, and/or other suitable processes. One or more annealing processes may be performed to activate the S/D regions. The annealing processes comprise rapid thermal annealing (RTA), laser annealing processes, and/or other suitable annealing processes.

Conventional processing of the FinFET device **200** would continue with performing a selective epitaxial growth/deposition process to form raised source/drain regions comprising epitaxially grown silicon (Si) or silicon germanium (SiGe), which can also be referred to as facets of the fin structure (e.g., Si and SiGe facets). It has been observed that conventional facets of the fin structure, such as the Si and SiGe facets, are unable to exhibit a rectangular profile following conventional processing. More particularly, it has been observed that epitaxially growing Si and SiGe facets cannot form a rectangular profile on a silicon substrate having a (001) crystallographic orientation with a notch aligned in a <110> direction. For example, FIG. **5**A is a cross-sectional view of a fin structure along a channel of the fin structure, where the facets of the fin structure exhibit a diamond shaped profile, which often occurs in conventional processing. When the facets are grown on a silicon substrate having a (001) crystallographic plane orientation, the diamond shaped profile of FIG. **5**A may have a top (first) surface with a (001) crystal plane and right/left (second/third) sidewall surfaces with a (111) crystal plane. In other words, the substrate, channel, and facet each have a different crystallographic orientation (e.g., wafer (001)/channel (110)/facet (111)). Because conventional facets naturally grow in a diamond shape, fin structure height is limited by fin structure width. This adversely decreases an area available for later performed salicidation to form salicide contact areas, which also contributes to increased contact resistance. Improving the profile of the facets is difficult by varying process settings.

Accordingly, an improved method for providing improved facet profile control is desired. The present disclosure proposes utilizing a damascene process to form the facets of the fin structure, i.e., the raised source/drain regions of the FinFET device. The damascene process can be utilized to form unique and/or arbitrary profiles of the fin structure including the facets. For example, FIG. **5**B is a cross-sectional view of a fin structure along a channel of the fin structure, where the fin structure including the facets of the fin structure exhibit a rectangular-shaped profile. The damascene process disclosed herein can utilize a capping layer that is patterned to define a desired facet profile. The capping layer can provide improved profile control (for example, by providing the ability to form facets having a rectangular profile, particularly Si and SiGe facets grown on a silicon substrate having a (001) crystallographic orientation) and increase/expand a salicidation area, which can reduce salicide contact resistance. The capping layer also eliminates fin structure height limitations, even as fin structure widths decrease. Unique facet profiles and/or arbitrary facet profiles are possible by forming epitaxial layers in an etched profile of the capping layer, forming defined facets (source/drain regions). It is understood that different embodiments may have different advantages, and that no particular advantage is necessarily required of any embodiment.

Referring to FIGS. **1** and **2**D, at block **108**, a capping layer is formed over the substrate and fin structure. In the present embodiment, a capping layer **212** is formed over the substrate **202**, fin structure **206**, and gate structure **208** (including spacers **210**). The capping layer **212** comprises any suitable material. An exemplary capping layer **212** is an oxide capping layer, such as silicon oxide or silicon oxynitride (SiON). Alternatively, the capping layer **212** includes other suitable materials, such as silicon nitride, SiC, SiOC, spin-on glass (SOG), a low-k film, tetraethylorthosilicate (TEOS) formed oxide, plasma enhanced CVD oxide (PE-oxide), high-aspect-ratio-process (HARP) formed oxide, or other suitable material. The capping layer **212** is formed by any suitable deposition process. Subsequently, one or more chemical mechanical polishing (CMP) processes are performed to planarize the capping layer **212** as illustrated in FIG. **2**D. For example, the CMP process is performed until a portion of the gate structure **208** and spacers **210** are reached (which may expose a top portion of the gate structure **208** and spacers **210**).

Referring to FIGS. **1** and **2**E, at block **110**, an opening is formed in the capping layer to define source and drain regions for the FinFET device **200**. The source and drain regions may alternatively be referred to as facet portions of the fin structure **206**, and thus, the opening in the capping layer defines a facet profile. For example, opening **214** is formed in the capping layer **212** by a combination of photolithography and etching processes. The opening **214** (comprising one or more openings in the present embodiment) defines source and drain (S/D) regions (or facet profiles) for the FinFET device **200**. Thus, the capping layer **212** may be patterned to define various S/D (or facet) profiles. The opening **214** also exposes portions of the fin structure **206**. The capping layer **212** may exhibit a different etching selectivity than the fin structure **206**, such that etching of the capping layer **212** does not modify a profile of the fin structure **206** or damage the fin structure **206** (e.g., the fin structure **206** exhibits a higher etching resistance than the capping layer **212**).

The photolithography patterning processes include photoresist coating (e.g., spin-on coating), soft baking, mask aligning, exposure, post-exposure baking, developing the photoresist, rinsing, drying (e.g., hard baking), other suitable processes, and/or combinations thereof. Alternatively, the photolithography exposing process is implemented or replaced by other proper methods such as maskless photolithography, electron-beam writing, and ion-beam writing. The etching processes include dry etching, wet etching, and/or other etching methods (e.g., reactive ion etching).

At block **112**, raised source and drain regions are formed. For example, the opening **214** is filled with an epitaxial layer **216**, which forms epitaxial layer **216** on the exposed portions of the fin structure **206** (e.g., source and drain regions of the fin structure **206**) as illustrated in FIG. **2**F. The epitaxial layer **216** is grown in regions by one or more epitaxy (epi) processes where the capping layer **212** has been removed (e.g., in the present embodiment, within the opening **214** over portions of the fin structure **206**). The epitaxy processes include CVD deposition techniques (e.g., vapor-phase epitaxy (VPE) and/or ultra-high vacuum CVD (UHV-CVD)), molecular beam epitaxy, and/or other suitable processes. The epitaxy process may use gaseous and/or liquid precursors, which

interact with the composition of the fin structure **206** (e.g., silicon). In the present embodiment, the epitaxial layer **216** comprises silicon (Si) (i.e., Si epi layer **216**), formed by a silicon epitaxial deposition process. Alternatively, the epitaxial layer **216** comprises silicon germanium (SiGe) (i.e., SiGe epi layer). The epitaxial layer **216** may be a doped epi layer, which may be doped during its deposition (growth) by adding impurities to the source material of the epitaxy process or subsequent to its deposition growth process by an ion implantation process. For example, a silicon epi layer may be doped with phosphorous (to form a Si:P epi layer). The doped epitaxial layer may have a gradient doping profile. Subsequently, a CMP process may be performed to planarize the epitaxial layer **216**. It is understood that, in some examples, prior to forming the raised S/D regions, S/D regions of the fin structure **206**, such as LDD and/or HDD S/D regions, may be formed in the openings.

As illustrated in FIGS. **2**F and **2**G, when considering a sectional view of the FinFET device **200** taken along the channel of the device, the epitaxial layer **216** and/or fin structure **206** have a rectangular profile. The rectangular profile is similar to the profile illustrated by the cross-section of a fin structure having a raised source/drain region in FIG. **5**B. The raised S/D regions (and/or epitaxial layer **216**) have a top (first) surface, a right (second) sidewall surface, and a left (third) sidewall surface. The top surface of the raised S/D region is parallel to the top surface of the fin structure, and the right/left sidewall surfaces of the raised S/D region are perpendicular to the top surface of the raised S/D region. Furthermore, the top surface of the raised S/D regions and the top surface of the fin structure are parallel with the top surface of the substrate as well. Particularly, the top surface of the substrate has a first crystalline plane orientation, the second sidewall surface (the third sidewall surface as well) has a second crystalline plane orientation different from the first crystalline plane orientation. The channel is aligned in a direction parallel to both the top surface of the substrate and the second sidewall surface of the epitaxy layer. Stating differently, the channel is aligned in a direction defined by an intersection line between the first surface and the second surface.

In the present example, where the substrate **202** and/or fin structure **206** have a (001) crystallographic plane orientation, to achieve the rectangular profile, the top surface of the raised S/D region has a (001) crystal plane orientation and the left/right sidewall surfaces have a (110) crystal plane orientation. In other words, the channel and facet have the same crystallographic plane orientation, which is different from the crystallographic plane orientation of the substrate (e.g., wafer (001)/channel (110)/facet (110)).

At block **114**, subsequent processing may be performed. Referring to FIG. **2**G, the capping layer **212** is removed by any suitable process. The method **100** may continue to fabricate other features of the FinFET device **200**, including for example, forming contacts, interconnect structures, and/or other suitable features and processes. The FinFET device **200** exhibits expanded salicidation areas, such that the later formed contacts exhibit reduced salicide contact resistance. The expanded salicidation areas are achieved by the method **100** providing the ability to vary the profile of the source and drain regions, particularly providing a square profile.

FIG. **3** illustrates a flow chart of an embodiment of the method **300** to fabricate the FinFET device **400**. Referring to FIGS. **3** and **4**A, at block **302**, a substrate (wafer) **402** is provided. The substrate **402** comprises silicon in a crystalline structure. The substrate **402** comprises any suitable crystallographic orientation (e.g., a (100), (110), or (111) crystallographic orientation). The substrate **402** may further include a notch aligned along any suitable direction (e.g., a <110> or <100> direction). In one embodiment, the substrate **402** includes a top surface having a (001) crystalline plane orientation. In the present embodiment, the substrate **402** comprises a (001) crystallographic orientation with a notch aligned in a <110> direction. Alternatively, the substrate **402** comprises other suitable elementary semiconductors, such as germanium in crystal; a compound semiconductor, such as silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; or combinations thereof. Alternatively, the substrate **402** includes a silicon-on-insulator (SOI) substrate. The SOI substrate can be fabricated using separation by implantation of oxygen (SIMOX), wafer bonding, and/or other suitable methods. The substrate **402** may include isolation regions, various doped regions, other suitable features, and/or combinations thereof.

At block **304**, a fin structure **406** is formed over the substrate **402**. The exemplary fin structure **406** comprises one or more fins. The fins comprise any suitable material, for example, the fin structure **406** comprises one or more silicon fins (Si-fin). As illustrated in FIG. **4**A, the fin structure **406** exhibits a rectangular shape with a top surface that is parallel to a top surface of the substrate **402**. Accordingly, the top surface of the fin structure **406** may have a (001) crystallographic plane orientation, similar to the substrate **402**. The rectangular-shaped fin structure **406** can also include a right and left sidewall surfaces perpendicular to the top surfaces of the fin structure **406** and/or substrate **402**.

The fin structure **406** is formed by any suitable process including various deposition, photolithography, and/or etching processes. An exemplary photolithography process may include forming a photoresist layer (resist) overlying the substrate (e.g., on a silicon layer), exposing the resist to a pattern, performing a post-exposure bake process, and developing the resist to form a masking element including the resist. The masking element may then be used to etch the fin structure into the silicon layer. The fin structure may be etched using reactive ion etching (RIE) processes and/or other suitable processes. In an example, the fin structure **406** may be formed, for example, by etching a layer of silicon on the substrate. The layer of silicon may be a silicon layer of a SOI substrate (e.g., overlying an insulator layer). The fin structure **406** may further include a capping layer disposed on the fins. The capping layer may include a silicon capping layer. It is understood that multiple parallel fin structures may be formed in a similar manner.

Alternatively, the fin structure **406** is formed by a double-patterning lithography (DPL) process. DPL is a method of constructing a pattern on a substrate by dividing the pattern into two interleaved patterns. DPL allows enhanced feature (e.g., fin) density. Various DPL methodologies may be used including double exposure (e.g., using two mask sets), forming spacers adjacent features and removing the features to provide a pattern of spacers, resist freezing, and/or other suitable processes.

Referring to FIGS. **3** and **4**B, at block **306**, a gate structure **408** is formed over a portion of the fin structure **406**. The gate structure **408** traverses the fin structure **406**. In the present embodiment, the gate structure **408** is formed over a central portion of the fin structure **406**. The gate structure **408** includes one or more material layers, such as interfacial layers, capping layers, diffusion/barrier layers, dielectric layers, electrode layers, conductive layers, other suitable layers, and/or combinations thereof. For example, the gate structure **408** may include a gate dielectric layer and a gate electrode. The

gate dielectric layer comprises a dielectric material, such as silicon oxide, silicon nitride, high-k dielectric material, other suitable dielectric material, and/or combinations thereof. Examples of high-k dielectric materials include HfO_2, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, zirconium oxide, aluminum oxide, hafnium dioxide-alumina (HfO_2—Al_2O_3) alloy, other suitable high-k dielectric materials, and/or combinations thereof. The gate electrode includes any suitable material, such as polysilicon, aluminum, copper, titanium, tantalum, tungsten, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, metal alloys, other suitable materials, and/or combinations thereof.

The gate structure **408** is formed by any suitable process. For example, the gate structure **408** is formed by a procedure including deposition, photolithography patterning, and etching processes. The deposition processes include chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), high density plasma CVD (HDPCVD), metal organic CVD (MOCVD), remote plasma CVD (RPCVD), plasma enhanced CVD (PECVD), low-pressure CVD (LPCVD), atomic layer CVD (ALCVD), atmospheric pressure CVD (APCVD), plating, other suitable methods, and/or combinations thereof The photolithography patterning processes include photoresist coating (e.g., spin-on coating), soft baking, mask aligning, exposure, post-exposure baking, developing the photoresist, rinsing, drying (e.g., hard baking), other suitable processes, and/or combinations thereof. Alternatively, the photolithography exposing process is implemented or replaced by other proper methods such as maskless photolithography, electron-beam writing, and ion-beam writing. The etching processes include dry etching, wet etching, and/or other etching methods (e.g., reactive ion etching).

The gate structure **408** may further include spacers **410** as illustrated in FIG. **4**C. The spacers **410** are formed by any suitable process to any suitable thickness. The spacers **410**, which are positioned on each side of the gate structure **408**, may comprise a nitride material (e.g., silicon nitride). In various examples, the spacers **410** comprise a dielectric material, such as silicon nitride, silicon carbide, silicon oxynitride, other suitable materials, and/or combinations thereof.

Various doped regions, such as source and drain (S/D) regions, can be formed in the fin structure **406**. The S/D regions can include lightly doped S/D regions (LDD regions) and/or heavily doped S/D regions (HDD regions). The gate structure **408** traversing the fin structure **406** can separate the various doped regions. For example, the gate structure **408** can separate a source region and a drain region of the fin structure **406**. The doping species may depend on the type of device being fabricated, such as an NMOS or PMOS device. The doping species include p-type dopants, such as boron or BF_2; n-type dopants, such as phosphorus or arsenic; and/or combinations thereof The S/D regions may comprise various doping profiles. The doped regions may be formed by implantation processes, diffusion process, and/or other suitable processes. One or more annealing processes may be performed to activate the S/D regions. The annealing processes comprise rapid thermal annealing (RTA), laser annealing processes, and/or other suitable annealing processes.

In the present example, at block **308**, recessed fin structure portions are formed. As illustrated in FIG. **4**D, portions of the fin structure **406** are removed to form recessed fin structure portions **406**A. The portions of the fin structure **406** are removed by any suitable process, including patterning and etching processes as described herein.

As noted above, conventional processing of the FinFET device **400** would continue with performing a selective epitaxial growth/deposition process to form raised source/drain regions comprising epitaxially grown silicon (Si) or silicon germanium (SiGe), which can also be referred to as facets of the fin structure (e.g., Si and SiGe facets). It has been observed that conventional facets of the fin structure, such as the Si and SiGe facets, are unable to exhibit a rectangular profile following conventional processing. More particularly, it has been observed that epitaxially growing Si and SiGe facets cannot form a rectangular profile on a silicon substrate having a (001) crystallographic orientation with a notch aligned in a <110> direction. For example, FIG. **5**A is a cross-sectional view of a fin structure along a channel of the fin structure, where the facets of the fin structure exhibit a diamond shaped profile, which often occurs in conventional processing. When the facets are grown on a silicon substrate having a (001) crystallographic plane orientation, the diamond shaped profile of FIG. **5**A may have a top (first) surface with a (001) crystal plane and right/left (second/third) sidewall surfaces with a (111) crystal plane. In other words, the substrate, channel, and facet each have a different crystallographic orientation (e.g., wafer (001)/channel (110)/facet (111)).

Because conventional facets naturally grow in a diamond shape, fin structure height is limited by fin structure width. This adversely decreases an area available for later performed salicidation to form salicide contact areas, which also contributes to increased contact resistance. Improving the profile of the facets is difficult by varying process settings. Accordingly, an improved method for providing improved facet profile control is desired. The present disclosure proposes utilizing a damascene process to form the facets of the fin structure, i.e., the raised source/drain regions of the FinFET device. The damascene process can be utilized to form unique and/or arbitrary profiles of the fin structure including the facets. For example, FIG. **5**B is a cross-sectional view of a fin structure along a channel of the fin structure, where the fin structure including the facets of the fin structure exhibit a rectangular-shaped profile.

Referring to FIGS. **3** and **4**E, at block **310**, a capping layer is formed over the substrate and fin structure. In the present embodiment, a capping layer **412** is formed over the substrate **402**, fin structure **406** (including recessed fin structure portions **406**A), and gate structure **408** (including spacers **410**). The capping layer **412** comprises any suitable material. An exemplary capping layer **412** is an oxide capping layer, such as silicon oxide or silicon oxynitride (SiON). Alternatively, the capping layer **412** includes other suitable materials, such as silicon nitride, SiC, SiOC, spin-on glass (SOG), a low-k film, tetraethylorthosilicate (TEOS) formed oxide, plasma enhanced CVD oxide (PE-oxide), high-aspect-ratio-process (HARP) formed oxide, or other suitable material. The capping layer **412** is formed by any suitable deposition process. Subsequently, one or more chemical mechanical polishing (CMP) processes are performed to planarize the capping layer **412** as illustrated in FIG. **4**E. For example, the CMP process is performed until a portion of the gate structure **408** and spacers **410** are reached (which may expose a top portion of the gate structure **408** and spacers **410**).

Referring to FIGS. **3** and **4**G, at block **312**, an opening is formed in the capping layer to define source and drain regions for the FinFET device **400**. The source and drain regions may alternatively be referred to as facet portions of the fin structure **406**, and thus, the opening in the capping layer defines a facet profile. For example, opening **414** is formed in the capping layer **412** by a combination of photolithography and etching

processes. The opening **414** (comprising one or more openings in the present embodiment) defines source and drain (S/D) regions for the FinFET device **400**. Thus, the capping layer **412** may be patterned to define various S/D profiles. The opening **414** also exposes portions of the fin structure **406** (here, the recessed portions of the fin structure **406**A are exposed). The capping layer **412** may exhibit a different etching selectivity than the fin structure **406**, such that etching of the capping layer **412** does not modify a profile of the fin structure **406** or damage the fin structure **406** (e.g., the fin structure **406** exhibits a higher etching resistance than the capping layer **412**).

The photolithography patterning processes include photoresist coating (e.g., spin-on coating), soft baking, mask aligning, exposure, post-exposure baking, developing the photoresist, rinsing, drying (e.g., hard baking), other suitable processes, and/or combinations thereof. Alternatively, the photolithography exposing process is implemented or replaced by other proper methods such as maskless photolithography, electron-beam writing, and ion-beam writing. The etching processes include dry etching, wet etching, and/or other etching methods (e.g., reactive ion etching).

At block **314**, raised source and drain regions are formed. For example, the opening **414** is filled with an epitaxial layer **416**, which forms epitaxial layer **416** on the exposed portions of the fin structure **406** (i.e., recessed portions of the fin structure **406**A, which may include S/D regions, such as those formed by an implantation process) as illustrated in FIG. **4**G. The epitaxial layer **416** is grown in regions by one or more epitaxy or epitaxial (epi) processes where the capping layer **412** has been removed (e.g., in the present embodiment, within the opening **414** over portions of the fin structure **406**). The epitaxy processes include CVD deposition techniques (e.g., vapor-phase epitaxy (VPE) and/or ultra-high vacuum CVD (UHV-CVD)), molecular beam epitaxy, and/or other suitable processes. The epitaxy process may use gaseous and/or liquid precursors, which interact with the composition of the fin structure **406** (e.g., silicon). In the present embodiment, the epitaxial layer **416** comprises silicon germanium (SiGe) (i.e., SiGe epi layer **416**), formed by a silicon germanium epitaxial deposition process. Alternatively, the epitaxial layer **416** comprises silicon (Si) (i.e., Si epi layer). The epitaxial layer **416** may be a doped epi layer, which may be doped during its deposition (growth) by adding impurities to the source material of the epitaxy process or subsequent to its deposition growth process by an ion implantation process. The doped epitaxial layer may have a gradient doping profile. For example, a silicon epi layer may be doped with phosphorous (to form a Si:P epi layer). Subsequently, a CMP process may be performed to planarize the epitaxial layer **416**. It is understood that, in some examples, prior to forming the raised S/D regions, S/D regions of the fin structure **406**, such as LDD and/or HDD S/D regions, may be formed in the openings, using the capping layer **412** as a mask.

As illustrated in FIGS. **4**G and **4**H, when considering a sectional view of the FinFET device **400** taken along the channel of the device, the epitaxial layer **416** and/or fin structure **206** have a rectangular profile. The rectangular profile is similar to the profile illustrated by the cross-section of a fin structure having a raised source/drain region in FIG. **5**B. The raised S/D regions (and/or epitaxial layer **416**) have a top (first) surface, a right (second) sidewall surface, and a left (third) sidewall surface. The top surface of the raised S/D region is parallel to the top surface of the fin structure, and the right/left sidewall surfaces of the raised S/D region are perpendicular to the top surface of the raised S/D region. Furthermore, the top surface of the raised S/D regions and the top surface of the fin structure are parallel with the top surface of the substrate as well. Particularly, the top surface of the substrate has a first crystalline plane orientation, the second sidewall surface (the third sidewall surface as well) has a second crystalline plane orientation different from the first crystalline plane orientation. The channel is aligned in a direction parallel to both the top surface of the substrate and the second sidewall surface of the epitaxy layer. Stating differently, the channel is aligned in a direction defined by an intersection line between the first surface and the second surface.

In the present example, where the substrate **402** and/or fin structure **406** have a (001) crystallographic plane orientation, to achieve the rectangular profile, the top surface of the raised S/D region has a (001) crystal plane orientation and the left/right sidewall surfaces have a (110) crystal plane orientation. In other words, the channel and facet have the same crystallographic plane orientation, which is different from the crystallographic plane orientation of the substrate (e.g., wafer (001)/channel (110)/facet (110)).

At block **316**, subsequent processing may be performed. Referring to FIG. **4**H, the capping layer **412** is removed by any suitable process. The method **100** may continue to fabricate other features of the FinFET device **400**, including for example, forming contacts, interconnect structures, and/or other suitable features and processes. The FinFET device **400** exhibits expanded salicidation areas, such that the later formed contacts exhibit reduced salicide contact resistance. The expanded salicidation areas are achieved by the method **300** providing the ability to vary the profile of the source and drain regions, particularly providing a square profile.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method for fabricating a FinFET device comprising:

forming a fin structure on a semiconductor substrate;

forming a gate structure, wherein the gate structure overlies a first portion of the fin structure;

forming a capping layer over the semiconductor substrate, fin structure, and gate structure;

patterning the capping layer to form an opening, wherein the opening exposes a second portion of the fin structure; and

growing an epitaxial layer in the opening and on the second portion of the fin structure, wherein the epitaxial layer includes at least one of a source region and a drain region associated with the gate structure.

2. The method of claim **1**, wherein the forming the capping layer includes depositing an oxide capping layer.

3. The method of claim **1**, further comprising:

removing the capping layer after growing the epitaxial layer.

4. The method of claim **1**, wherein the patterning the capping layer to form the opening includes removing a portion of the capping layer to define a profile of the source and drain regions.

5. The method of claim 1, wherein the growing the epitaxial layer in the opening comprises forming a source and a drain each having a square profile.

6. The method of claim 1, wherein the patterning the capping layer to form the opening includes performing at least one photolithography process and at least one etch process.

7. The method of claim 1, wherein the growing the epitaxial layer in the opening includes performing a selective epitaxy growth process to form at least one of a silicon layer and a silicon germanium layer.

8. The method of claim 1, further comprising:

prior to forming the capping layer, forming a recessed region in the second portion of the fin structure.

9. The method of claim 1, further comprising:

performing a first chemical mechanical polishing process on the capping layer.

10. The method of claim 9, further comprising:

performing a second chemical mechanical polishing process on the grown epitaxial layer.

11. A method for fabricating a FinFET device comprising:

forming a fin structure on a substrate;

forming a gate structure on a first region of the fin structure;

removing a second region of the fin structure to form a recessed portion of the fin structure;

forming a capping layer over the first and second regions of the fin structure;

patterning the capping layer to form an opening that defines a source and drain region associated with the gate structure, wherein the opening exposes the recessed portion of the fin structure;

growing an epitaxial layer on the exposed recessed portion of the fin structure in the opening of the capping layer; and

removing the capping layer after growing the epitaxial layer.

12. The method of claim 11, wherein the providing the substrate including the fin structure includes providing a silicon substrate having a (001) crystallographic orientation.

13. The method of claim 11, wherein the growing the epitaxial layer on the exposed recessed portion of the fin structure comprises forming a source and a drain having a square profile.

14. The method of claim 11, wherein the growing the epitaxial layer on the exposed recessed portion of the fin structure comprises forming a raised source and a raised drain.

15. The method of claim 11, further comprising:

performing an ion implantation process on the epitaxial layer.

16. A method of fabricating a FinFET device comprising:

providing a substrate of a crystalline semiconductor material having a top surface of a first crystal plane orientation;

forming a fin structure of the crystalline semiconductor material overlying the substrate;

forming a gate structure over a first portion of the fin structure;

growing an epitaxy layer over a second portion of the fin structure adjacent the first portion, wherein a surface of the epitaxy layer substantially perpendicular to the top surface has a second crystal plane orientation, the second crystal plane orientation different than the first crystal plane orientation; and

forming a channel region in the fin structure, wherein the channel region is aligned in a direction parallel to both the surface of the epitaxy layer and the top surface of the substrate.

17. The method of claim 16, wherein the growing the epitaxy layer includes performing a damascene process that includes:

forming a capping layer over the substrate, the fin structure, and the gate structure;

patterning the capping layer to form an opening, wherein the opening exposes the second portion of the fin structure;

growing the epitaxy layer in the opening on the exposed second portion of the fin structure; and

removing the capping layer.

18. The method of claim 16, wherein the growing the epitaxy layer includes performing a damascene process that includes:

removing a third portion of the fin structure overlying the second portion of the fin structure, to form a recessed portion of the fin structure;

forming a capping layer over the substrate, fin structure, and gate structure;

patterning the capping layer to form an opening, wherein the opening exposes the recessed portion of the fin structure;

growing the epitaxy layer in the opening on the exposed recessed portion of the fin structure; and

removing the capping layer.

19. The method of claim 16, wherein growing the epitaxy layer further includes performing an implantation process.

20. The method of claim 16, wherein a region in which the growing of the epitaxy layer is performed is defined by a sacrificial capping layer.

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