# A Logic Nanotechnology Featuring Strained-Silicon

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***Abstract*—Strained-silicon (Si) is incorporated into a leading edge 90-nm logic technology [1]. Strained-Si increases saturated n-type and p-type metal–oxide–semiconductor field-effect transistors (MOSFETs) drive currents by 10 and 25%, respectively. The process flow consists of selective epitaxial $Si_{1-x}Ge_x$ in the source/drain regions to create longitudinal uniaxial compressive strain in the p-type MOSEFT. A tensile Si nitride-capping layer is used to introduce tensile uniaxial strain into the n-type MOSFET and enhance electron mobility. Unlike past strained-Si work, 1) the amount of strain for the n-type and p-type MOSFET can be controlled independently on the same wafer and 2) the hole mobility enhancement in this letter is present at large vertical electric fields, thus, making this flow useful for nanoscale transistors in advanced logic technologies.**

***Index Terms*—CMOS, metal–oxide–semiconductor field-effect transistors (MOSFET), strained-silicon (Si).**

## I. Introduction

STRAINED-SILICON (Si) using a novel low cost process flow is introduced. Unlike the traditional approach where biaxial strain is applied into the channel from the bottom using strained-Si on relaxed $Si_{1-x}Ge_x$ [2]–[4], in this letter, uniaxial strain is introduced from the side using $Si_{1-x}Ge_x$ (p-type MOSFET) and a nitride capping film with a large tensile stress (n-type MOSFET). Transmission electron micrographs (TEMs) of MOSFETs are shown in Fig. 1. Strained-Si mobility enhancement is well-known and has found many applications in mechanical sensors. However, until recently [1], there has been no published literature on incorporating either biaxial or uniaxial strained Si into a commercial CMOS microprocessor logic technology. In this letter, we compare and contrast biaxial and uniaxial strained-Si MOSFETs and describe the uniaxial strained-Si process flow used in a 90-nm logic technology. We focus only on the hole mobility enhancement with strain since the conduction band splitting and mobility enhancement with a tensile nitride-capping layer [5], [6] is similar to the biaxial strained-Si case [2]–[4].

## II. Uniaxial Strained–Si

Biaxial strained Si has received substantial attention over the past few years [2]–[4]. Little attention, however, has been paid to unixial strained-Si. While biaxial tensile stress has potential technological importance to CMOS logic technologies since

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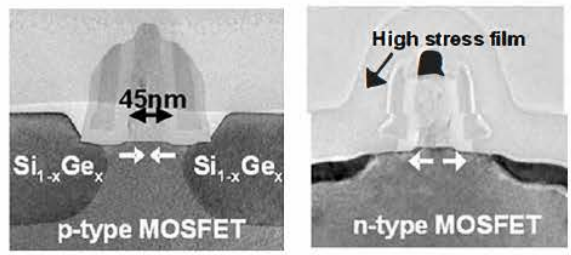


Fig. 1. TEM micrographs of 45-nm p-type and n-type MOSFET.

it introduces advantageous strain for both n type and p type MOSFET, it has not been introduced to fabricate commercial CMOS microprocessor due to integration challenges, process complexity, and cost. Furthermore, most PMOS, biaxially stressed Si demonstrates near-zero hole mobility improvement at large vertical electric fields [2] where commercial MOSFETs operate. Uniaxially stressed PMOS, however, does not suffer from this performance problem (as will be shown). However, the use of unixial stress for CMOS logic is not without its own complexities.

The difficulty in using uniaxial mechanical stress to improve the performance arises since it has been difficult to improve both n-type and p-type MOSFETs simultaneously. In this letter, compressive uniaxial strain is introduced into the p-type MOSFET by inserting an Si recess etch and selective epitaxial $Si_{1-x}Ge_x$ ($x = 0.17$) deposition post-spacer formation into a standard logic technology process flow. The mismatch in the $Si_{1-x}Ge_x$ to Si lattice causes the p type MOSFET to be under compres sive strain. The use of $Si_{1-x}Ge_x$ in the source/drain area for the purpose of higher boron activation was first proposed by Ozturk [7], however, for small devices the near completely biaxial strained-SiGe in the source/drain (if not completely strained due to the lack of misfits in Fig. 1) creates significant uniaxial compression in the channel as confirmed by three-dimensional finite-element analysis. Longitudinal uniaxial tensile strain is introduced into the n-type MOSFET by an Si nitride-capping layer [5], [6]. There are several techniques to neutralize the capping layer strain on the PMOS device, one is the use of a Ge implant, and masking layer [6]. Thus, for the first time, a process flow has been developed that allows the strain to be targeted independently for n- and p-type MOSFETs (by adjusting capping films stress for n-type and Ge source/drain concentration for p-type). The unique advantage of this uniaxial strained-Si process flow is that on the same wafer, compressive strain is introduced into the p-type and tensile strain in the n-type MOSFETs to improve ***both*** the electron and hole mobility. Furthermore, by confining

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the $Si_{1-x}Ge_x$ to the source/drain and introducing it late in the process flow, the integration challenges are simpler than the biaxial approach and MOSFET self-heating is unchanged.

## III. Experimental Results and Discussion

In this letter, we investigate large mobility enhancement in the small-strain regime using uniaxial stress since the integration of low strain into a CMOS logic technology creates less defects and requires less alteration of the technology midsection thermal cycles to avoid strain relaxation. In this small-strain regime, the piezoresistance varies linearly with strain (1% nonlinearity at 250 MPa) [8] and the piezoresistance coefficients can be used as a guide as to which strain maximizes the mobility enhancement.

We now use the piezoresistance coefficients to quantify strained-Si mobility enhancement. In this discussion, we assume industry-standard Si wafers with (001) surface and wafer notch on the [110] axis. Since uniaxial process-induced strain is generally applied either parallel (longitudinal) or perpendicular (transverse) to the direction of MOSFET current flow, we choose this coordinate system versus one aligned to the ⟨100⟩ axes. The effect of mechanical stress on the mobility can then be expressed as follows:

$$\frac{\Delta\mu}{\mu} \approx \left|\pi_{\parallel}\sigma_{\parallel} + \pi_{\perp}\sigma_{\perp}\right| \quad (1)$$

where the subscripts $\parallel$ and $\perp$ refer to the directions parallel and transverse to the current flow in the plane of the MOSFETs, $\Delta\mu/\mu$ is the fractional change in mobility, $\sigma_{\parallel}$ and $\sigma_{\perp}$ are the longitudinal and transverse stresses, and $\pi_{\parallel}$ and $\pi_{\perp}$ are the piezoresistance coefficients expressed in $Pa^{-1}$. $\pi_{\parallel}$ and $\pi_{\perp}$ can be expressed in terms of the three fundamental cubic piezoresistance coefficients $\pi_{11}$, $\pi_{12}$, and $\pi_{44}$.

The longitudinal and transverse piezoresistance coefficients for the standard layouts are given in Table I. For simplicity, we use the bulk values for $\pi_{11}$, $\pi_{12}$, and $\pi_{44}$ first measured 50 years ago by Smith [9], though technically piezoresistance coefficients should take into account the two-dimensional (2-D) nature of transport in MOSFETs and depend on temperature and doping [10]. Using the bulk coefficients, $\pi_{\parallel}$ and $\pi_{\perp}$ are calculated in Table I. We find the bulk coefficients quantitatively predict strained-Si experimental data in this work consistent with past work [11]. From Table I, the large positive value $\pi_{\parallel}$ for p-type MOSFETs with ⟨110⟩ channel orientation shows significantly less strain in needed for enhanced hole mobility when introduced with longitudinal compression versus in-plane biaxial strain. This is quantified by evaluating (1) and using

$$\gamma = \frac{\text{stress}}{\text{strain}} = \frac{\sigma_{\parallel}}{\frac{\Delta l}{l}} \quad (2)$$

where $\gamma$ is the Youngs modulus, and $(\Delta l/l)$ is the strain. The evaluation shows only 0.2% lattice displacement is required for a 30% mobility gain versus the biaxial case where > 1% displacement is required.

In this letter, the uniaxial strain increases the hole mobility for the 45-nm gate length transistor by 50% as shown in Fig. 2. The mobility for the short-channel device is extracted from the improvement in the linear current using $I_D = k(V_{GS}-V_T)(V_{DS}-I_D R_{SD})(V_{DS} = 50\ \text{mV})$ where $R_{SD}$ is measured independently and is also improved due to the Ge in the source/drain [7]. The field dependence of the mobility is also extracted using conventional techniques on a long-channel transistor [4] (where $R_{SD}$ is negligible) to validate the field dependence is correct. The key observation is that for this strained-Si flow, the hole mobility enhancement is present at a large vertical field (Fig. 2). This result is consistent with other uniaxial strained-Si where the mobility enhancement is also observed at a high field: mechanical wafer bending [12] and nitride capping layer [5], [6].

Why the hole mobility enhancement for uniaxial strain is present at high fields can be inferred from references [13]–[14]. Fig. 3 summarizes what is known about the hole band structure for unstrained- and strained-Si. The valance bands are plotted

TABLE I
Longitudinal and Transverse Piezoresistance Coefficients Evaluated for Standard Layout and Wafer Orientation (Units of $10^{-12}$ $cm^2$ $dyne^{-1}$)

| | <100> | | <110> | |
|---|---|---|---|---|
| Polarity | $\pi_{\parallel}$ | $\pi_{\perp}$ | $\pi_{\parallel}$ | $\pi_{\perp}$ |
| N or P | $\pi_{11}$ | $\pi_{12}$ | $(\pi_{11}+\pi_{12}+\pi_{44})/2$ | $(\pi_{11}+\pi_{12}-\pi_{44})/2$ |
| N-type | -102 | 53.4 | -31.6 | -17.6 |
| P type | 6.6 | -1.1 | 71.8 | 66.3 |

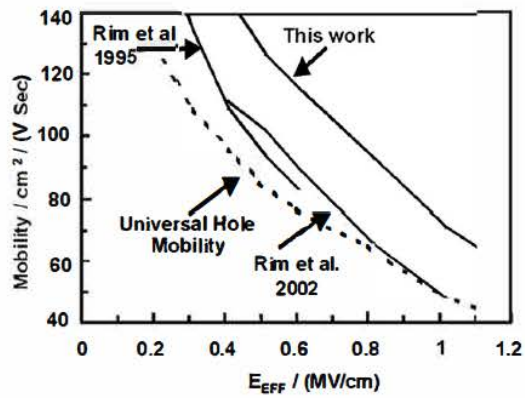


Fig. 2. Hole mobility for uniaxial strained Si introduced $Si_{1-x}Ge_x$ in the source/drain.

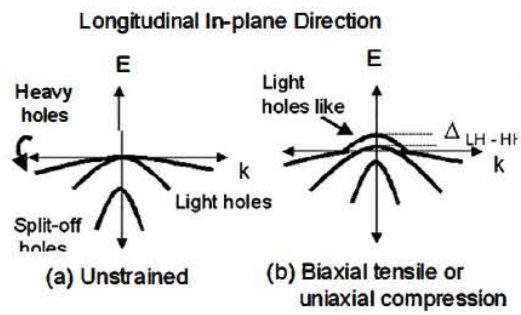


Fig. 3. Simplified hole valance band structure for longitudinal in plane direction. (a) Unstrained and (b) strained-Si.

for the in-plane direction of the MOSFET channel. Both uniaxial and biaxial strain can be used to lift the degeneracy in the valance band and cause the bands to not only shift, but to change shape as shown in Fig. 3. For both biaxial tensile and uniaxial compressive stress, a key component of the enhanced mobility results from the lowest energy subband having a low conductivity effective mass because it is "light hole like" [13]–[15]. This strain-induced formation of low in plane effective mass (high mobility) was first calculated by Bir and Pikus ([15, pp. 313–315, Figs. 30 and 31]) in 1958 in which a "dimple" at $k = 0$ is formed by the light hole band dropping in energy. To explain the field dependence of the mobility in biaxial tensile strain, Fischetti [15] recently showed the reduction in hole mobility enhancement with vertical field results from the quantization associated with the confining surface potential of the MOSFET [15]. The surface potential decreases the separation between the light and heavy hole-like bands ($\Delta_{\mathrm{lh-hh}}$ see Fig. 3). This decreased separation with surface potential does not occur for uniaxial strained-Si as seen in the mobility data and confirmed by internal band calculations.

## IV. Conclusion

In this letter, we describe a strained-Si process flow that allowing the strain to be targeted independently for n- and p-type MOSFETs (by adjusting capping films stress for n type and Ge source/drain concentration p-type). The uniaxial strained-Si p-type MOSFET is shown to have significant advantages over biaxial strain since 1) it has a much larger mobility enhancement for a given strain and 2) the mobility enhancement is present at large vertical fields.

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