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【Purport】

Submit it to the Commissioner of the Korean Intellectual Property Office as above.

【Official Fee】

【Application Fee】	0 page 38,000 won
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【Abstract】

【Summary】

The present invention relates to a semiconductor device having a low resistance contact. According to an embodiment of the present invention, the semiconductor device comprises: a P-type field effect transistor and an N-type field effect transistor respectively formed on first and second active regions of a substrate The first and the second contact pad layer including the Si epitaxial layer and the SiGe epitaxial layer which successively is laminated on the source / drain regions of N type MOSFET and P-type field effect transistor and an interlayer insulating film which is formed on the P-type and N-type field effect transistors and includes a first contact hole which has a first bottom surface to expose the SiGe epitaxial layer of the first contact pad layer and a second contact hole which has a second bottom surface to expose the Si epitaxial layer by penetrating the SiGe epitaxial layer of the second contact pad layer. The second metal silicide layer which may not contain the Ge formed on the first metal silicide layer and the second bottom surface containing the Ge formed on the first bottom surface and contact plugs which are formed on the first and second metal silicide layers and bury the first and second contact holes.

【Representative Drawing】

Drawing1f

【Description of the Invention】

【Title of Invention】

SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME

【The Detailed Description of the Invention】

【Technical Field】

【0001】 The present invention relates to a semiconductor device and a method for manufacturing the same, and more particularly, to a field effect transistor having a low resistance contact and a method for manufacturing the same.

【Background Technique】

【0002】 Electronic devices such as computers, cellular phones, and digital cameras require active devices for logic implementation. As the active device, a complementary MOS transistor (or CMOS transistor) having low power driving and high linear characteristics is widely used.

【0003】 In recent years, the design rule of a semiconductor device has been narrowed due to the light, thin, and small size of an electronic product, and accordingly, the contact area of the source/drain regions of the CMOS transistor has also been gradually reduced. Since the reduction of the contact area increases the contact resistance, the improvement of the contact resistance is an important issue in the high integration of CMOS transistors.

【0004】 The CMOS transistor includes a P-channel MOSFET and an N-channel MOSFET connected in series with each other. In order to provide a low resistance contact to such a CMOS transistor, it is necessary to form a contact having a low Schottky barrier on the P-channel MOSFET and the N-channel MOSFET. Conventionally, the different work function is in P channel MOSFET and N channel MOSFETA technique for reducing the Schottky barrier of a contact by forming each of the metal silicide layers has been

proposed.

【0005】However, in order to form different types of metal silicide layers on the P-channel MOSFET and the N-channel MOSFET, the silicide layer of the P-channel MOSFET and the silicide layer of the N-channel MOSFET were formed through separate processes. For example, first, in order to form a PtSi film, which is a metal silicide film having a high work function, on a P-channel MOSFET, a mask film is formed to completely block an N-channel MOSFET region. Thereafter, the PtSi layer is formed in the P-channel MOSFET region. Next, in order to form an ErSi film, which is a metal silicide film having a low work function, on the N-channel MOSFET, the mask film blocking the N-channel MOSFET region needs to be removed to expose the N-channel MOSFET region.

【0006】As described above, the process of forming the mask layer for forming the silicide layer having different metal elements in the P-channel MOSFET region and the N-channel MOSFET region and selectively blocking any one region therefor involves an additional photolithography process and an etching process, and thus there is a problem in that the process is complicated and the cost is increased.

【Content of Invention】

【Problem to solve】

【0007】Accordingly, the technical problem to be solved by the present invention is to provide a semiconductor device capable of reducing contact resistance with respect to both a P channel MOSFET and an N channel MOSFET by forming silicide layers having different compositions between a source/drain region and a contact plug through a simple manufacturing method.

【0008】In addition, another object of the present invention is to provide a

method of manufacturing a semiconductor device capable of manufacturing a semiconductor device having the above advantages without a blocking process.

【Solution to the Problem】

【0009】The semiconductor device according to an embodiment of the present invention comprises: a substrate including first and second active regions The respective formed P-type field effect transistor on first and second active area and N type field effect transistor The first and the second contact pad layer including the Si epitaxial layer and the SiGe epitaxial layer which successively is laminated on the source / drain regions of N type MOSFET and P-type field effect transistor and an interlayer insulating film which is formed on the P-type and N-type field effect transistors and includes a first contact hole which has a first bottom surface to expose the SiGe epitaxial layer of the first contact pad layer and a second contact hole which has a second bottom surface to expose the Si epitaxial layer by penetrating the SiGe epitaxial layer of the second contact pad layer. It is formed in the first metal silicide layer and the second bottom surface containing the Ge formed in the first bottom surfaceThe second metal silicide layer which may not contain Ge and contact plugs formed on the first and second metal silicide layers to bury the first and second contact holes.

【0010】The semiconductor device may further include a diffusion barrier layer between the sidewall of the second contact hole and the metal silicide layer. In addition, at least one of the first and second contact pad layers may be grown in a direction parallel to the main surface of the substrate to be extended onto a partial region of the device isolation layer defining the first and second active regions.

【0011】The semiconductor device according to another embodiment of the

present invention for achieving the technical problem includes a substrate including first and second active regions The respective formed P-type field effect transistor on first and second active area and N type field effect transistor The respective first contact pad layer included and the second contact pad layer the SiGe epitaxial layer and the Si epitaxial layer laminated on the source / drain regions of N type field effect transistor and P-type field effect transistor according to order and an interlayer insulating film which is formed on the P-type and N-type field effect transistors and includes a first contact hole having a first bottom surface which penetrates the Si epitaxial layer of the first contact pad layer and exposes the SiGe epitaxial layer and a second contact hole having a second bottom surface which exposes the Si epitaxial layer of the second contact pad layer. And the second metal silicide layer which contain does not the Ge formed in the first metal silicide layer containing the Ge formed in the first bottom surface and the second bottom surface and contact plugs formed on the first and second metal silicide layers to bury the first and second contact holes.

【0012】At least a portion of the SiGe epitaxial layer of the first contact pad layer may be buried in the first active region. In addition, at least one of the first and second contact pad layers may be grown in a direction parallel to the main surface of the substrate to be extended onto a partial region of the device isolation layer defining the first and second active regions.

【0013】The semiconductor device according to another embodiment of the present invention for achieving the technical problem includes a substrate including first and second active regions The respective formed P-type field effect transistor on first and second active area and N type field effect transistor The respective first included and the second contact pad layer the Si epitaxial layer and the Ge atomic layer successively laminated on the source / drain regions of N type MOSFET and P-type field effect transistor

The inter-layer insulating film which is formed on P-type and N type field effect transistors and includes the second contact hole having the second bottom surface exposing the Si epitaxial layer through the Ge atomic layer of the second contact pad layer and the first contact hole having the first bottom surface exposing the Ge atomic layer of the first contact pad layer The second metal silicide layer which may not contain Ge formed in the bottom surface of the first metal silicide layer and the second contact hole containing Ge formed in the first bottom surface of the first contact hole and contact plugs formed on the first and second metal silicide layers to bury the first and second contact holes.

【0014】According to another aspect of the present invention, there is provided a method of manufacturing a semiconductor device, the method including forming a first active region for a P-type field effect transistor and a second active region for an N-type field effect transistor on a substrate said first bowThe step of forming the first gate stack on the nature domain The step of forming the second gate stack on the second active area The step of at the same time, forming first and second epitaxial bilayers including the Si epitaxial layer on the second active area except for the first active region except for the first gate stack and the second gate stack and SiGe epitaxial layer The step forming the inter-layer insulating film covering first and second gate stacks and top of epitaxial double layers The step forming the first contact hole having the first bottom surface exposing the SiGe epitaxial layer of the first epitaxial double layer within the inter-layer insulating film The step forming the second contact hole having the second bottom surface exposing the Si epitaxial layer within the inter-layer insulating film through the SiGe epitaxial layer of the second epitaxial double layer Step of at the same time, forming the first metal silicide layer containing Ge in the first bottom surface and the second metal silicide

layer which contain may not Ge in the second bottom surface and forming contact plugs which bury the first and second contact holes on the first and second silicide layers.

【0015】According to another aspect of the present disclosure, there is provided a method of manufacturing a semiconductor device, the method including forming a first active region for a P-type field effect transistor and a second active region for an N-type field effect transistor on a substrate The step of forming the first gate stack on the first active region The step of forming the second gate stack on the second active area sequence units on the first active region except for the first gate stack and the second active region except for the second gate stack, respectivelyThe step of at the same time, forming first and second epitaxial bilayers including the SiGe epitaxial layer and Si epitaxial layer The step forming the inter-layer insulating film covering first and second gate stacks and top of epitaxial double layers The step forming the first contact hole having the first bottom surface exposing the Si epitaxial layer within the inter-layer insulating film through the Si epitaxial layer of the first epitaxial double layer The step forming the second contact hole having the second bottom surface exposing the Si epitaxial layer of the second epitaxial double layer within the inter-layer insulating film Step of at the same time, forming the first metal silicide layer containing Ge in the first bottom surface and the second metal silicide layer which contain may not Ge in the second bottom surface and a step of forming contact plugs burying the first and second contact holes on the first and second silicide layers.

【Effect】

【0016】A semiconductor device according to embodiments of the present invention can provide a semiconductor device having a low resistance contact by lowering the height of a Schottky barrier of a contact region by

providing silicide layers of different compositions to a P-type field effect transistor and an N-type field effect transistor.

【0017】 In addition, the method for manufacturing a semiconductor device according to embodiments of the present invention can provide a semiconductor device having a low resistance contact without a photolithography and etching process by omitting a blocking process by forming a silicide layer having a low Schottky barrier through an interlayer insulating layer and a contact hole formed in the interlayer insulating layer.

【Detailed Description for the Implementation of the Invention】

【0018】 Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings.

【0019】 Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present invention to those skilled in the art. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present disclosure to those skilled in the art.

【0020】 It will be understood that when an layer is referred to as being "on" another layer, it can be directly on the other layer or intervening layers may also be present. In the drawings, the thickness or size of each layer is exaggerated for convenience and clarity of description, and the same reference numerals refer to the same elements in the drawings. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

【0021】 The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a," "an," and "the" are

intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

【0022】 It will be understood that, although the terms first, second, etc. may be used herein to describe various members, components, regions, layers and/or sections, these members, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one member, component, region, layer or section from another region, layer or section. Accordingly, a first member, component, region, layer, or section to be described below may refer to a second member, component, region, layer, or section without departing from the teachings of the present disclosure.

【0023】 As disclosed herein, a field effect transistor may be used interchangeably with a channel MOSFET, a MOSFET, and a MISFET. In addition, although the disclosed embodiments relate to a field effect transistor having a flat channel, this is exemplary, and it will be understood by those skilled in the art that a MOS transistor having a fin-shaped or recessed channel is also included in the present invention.

【0024】 Hereinafter, embodiments of the present invention will be described with reference to the drawings schematically showing ideal embodiments of the present invention. In the drawings, variations of the illustrated shape can be expected, for example, depending on manufacturing techniques and/or tolerances. Accordingly, embodiments of the present invention should not be construed as being limited to the particular shape of the regions shown herein, but should include, for example, changes in shape resulting from

manufacturing.

【0025】 1A to 1F are cross-sectional views illustrating a method of manufacturing a semiconductor device 100 according to an embodiment of the present invention.

【0026】 Referring to FIG. 1A, a P-type field effect transistor 50A is formed on a substrate 10.The second active area in which the first active region and N type field effect transistor (50B) are formed is included. The substrate 10 is a substrate capable of a known semiconductor device manufacturing process, and may be, for example, a silicon single crystal substrate, a silicon-on-insulator (Silicon-On-Insulator; SOI) or silicon-on-sapphire (Silicon-On-Saphire; The substrate may be an SOS substrate.

【0027】 the first active region and the second active area of the substrate(10) is the shallow trench isolation (shallow trench isolation STI) may be defined by the device isolation layer 11. The substrate 10 may include an N well and a P well in the first and second active regions, respectively. Alternatively, when a substrate of a specific conductivity type is used, any one well may be replaced. For example, the P-type substrate 10 may be used to form only N wells in the first active region of the substrate 10. Alternatively, the reverse case is also possible.

【0028】 The first and the second gate stack (20A, 20B) are formed respectively on the first active region and the second active area. The gate stacks 20A and 20B may be formed by sequentially forming the gate insulating layer 21, the gate conductive layers 22a and 22b, and the capping layer 23 for protecting the gate insulating layer 21, the gate conductive layers 22a and 22b, and patterning the gate insulating layer 21, the gate conductive layers 22a and 22b, and the capping layer 23 on the first and second active regions.

【0029】 The gate insulating layer 21 may be a silicon oxide layer. However, this is exemplary, and the present invention is not limited thereto. For

example, the gate insulating layer 21 may include a high-k thin film having a dielectric constant greater than that of the silicon oxide layer, for example, a silicon nitride layer (SiNx), a tantalum oxide layer (TaOx), a hafnium oxide layer (HfOx), an aluminum oxide layer (AlOx), and a zinc oxide layer (ZnOx).

【0030】The gate conductive films (22a, 22b) are, for example, highly doped polysilicon films, tungstenIt may be a metal film such as ten, nickel, molybdenum, cobalt, or the like, a metal silicide film, or a combination thereof, for example, a stacked film of a highly doped polysilicon film and a nickel cobalt silicide film. In some embodiments, the gate conductive layers 22a and 22b in the first and second gate stacks 20A and 20B may be formed of materials having different work functions. For example, the gate conductive layer 22a of the first gate stack 20A may be formed of a metal silicide layer, and the gate conductive layer 22b of the second gate stack 20B may be formed of a metal layer. The capping layer 23 may be silicon nitride or silicon oxide.

【0031】In some embodiments, the gate stacks (20A, 20B) are used as an ion implantation mask film to suppress the hot carrier effect occurring in the drain region of the transistors (50A, 50B). LDD) regions 31a and 31b, a shallow source/drain-extension-region; SDE; 31a, 31b) can be further formed.

【0032】The gate spacer film(24) is formed in the sidewall of the gate stack (20A, 20B). The gate spacer layer 24 may be formed of silicon nitride. Thereafter, a high-concentration ion implantation process may be performed in the first active region and the second active region using the gate stacks 20A and 20B and the spacer layer 24 as mask layers to form high-concentration source/drain regions 32a and 32b.

【0033】Next, a Si epitaxial layer 41L is simultaneously formed on the exposed source/drain regions 32a and 32b of the first and second active regions.

Subsequently, a SiGe epitaxial layer 42L is simultaneously formed on the Si epitaxial layer 41L on the first and second active regions. SiThe thickness of the epitaxial layer 41L may be in a range of 10 Å to 500 Å. The thickness of the SiGe epitaxial layer 42L may be in a range of 30 Å to 500 Å. The Ge molarity of the SiGe epitaxial layer 42L is in the range of 3% to 50%.

【0034】 The Si epitaxial layer 41L and the SiGe epitaxial layer 42L may be formed using a selective epitaxial growth method. For example, the Si epitaxial layer 41L includes SiH_4,Si_2H_4,Si_2H_6or SiH_2Cl_2A silicon-containing gas such as may be produced by chemical vapor deposition at about 700˚C. Similarly, the SiGe epitaxial layer 42L includes SiH_4,Si_2H_4,Si_2H_6or SiH_2Cl_2GeH in the silicon containing gas including etc_4Alternatively, a Ge-containing gas such as GeH is mixed to grow a SiGe crystal film on the Si epitaxial layer 41L. However, this is exemplary, and the present invention is not limited thereto. For example, the Si epitaxial layer 41L and the SiGe epitaxial layer 42L may also be formed by a molecular beam epitaxy method.

【0035】 In some embodiments, the Si epitaxial layer 41L and the SiGe epitaxial layer 42L may be grown not only in a direction perpendicular to the corresponding active region but also in a direction parallel to the main surface of the substrate 10 to extend onto a partial region of the adjacent device isolation layer 11. The extended epitaxial layers 41L and 42L may secure a photolithography process margin for forming a contact plug and may further reduce contact resistance due to the increased upper surface area.

【0036】 Thereafter, in order that the conductivity is given to the epitaxial double layer (40E1) on the first active region and the second active region, the ion implantation mask film (not shown) is formed and the ion injection process is proceedIt can be performed. For example, a Group 3 element, for example, boron (B), may be doped into the epitaxial double layer 40E1 on the

first active region, and a Group 5 element, for example, phosphorus (P) or arsenic (As), may be doped into the double layer 40E1 on the second active region.

【0037】 Alternatively, as will be described with reference to FIGS. 1B and 1C, an ion implantation process may be performed on the contact pad layer 40PA on the first active region exposed after the first contact hole HA is formed, and an ion implantation process may be performed on the contact pad layer 40PB on the second active region exposed after the second contact hole HB is formed.

【0038】 Referring to FIG. 1B, an interlayer insulating layer 60 is formed to cover upper portions of the P-type and N-type field effect transistors 50A and 50B and the epitaxial double layers 40E1. The interlayer insulating layer 60 may be a silicon oxide layer, a phosphosilicate glass (PSG) layer, or a borophosphosilicate glass (BPSG) layer. Alternatively, the interlayer insulating layer 60 may be a doped CVD glass layer that is a low dielectric constant material. However, these are merely exemplary, and the present invention is not limited thereto.

【0039】 Thereafter, any one of the first active region and the second active region, for example, as shown, a first contact hole HA disposed on the first active region may be first formed. In order to form the first contact hole HA, a mask layer M1 is formed on the interlayer insulating layer 60 to expose a region where the first contact hole HA is to be formed by a photolithography process. Thereafter, a first contact hole HA may be formed in the interlayer insulating layer 60 using a plasma dry etching process. The first contact the etch depth of the first contact hole (HA) is controlledThe bottom surface of the hole HA exposes the SiGe epitaxial layer 42L. Thereby, the contact pad layer 40PA for the P-type field effect transistor 50A is completed.

【0040】 Referring to FIG. 1C, a photolithography process may be performed

on the interlayer insulating layer 60 to form a mask layer M2 exposing a region where the second contact hole HB is formed. Thereafter, a second contact hole HB is formed in the interlayer insulating layer 60 using a plasma dry etching process. The etching depth of the second contact hole HB is adjusted so that the bottom surface of the second contact hole HB penetrates the SiGe epitaxial layer 42L′ to expose the underlying Si epitaxial layer 41L. Thereby, the contact pad layer 40PB for the N-type field effect transistor 50B is completed.

【0041】 The etching process of the second contact hole HB may be continuously performed on the interlayer insulating layer 60 and the SiGe epitaxial layer 42L using the same etching gas. In some embodiments, the interlayer insulating layer 60 and the SiGe epitaxial layer 42L may be discontinuously etched using different etching gases in consideration of an etching selectivity.

【0042】 Referring to FIG. 1D, a diffusion barrier 65 may be formed to cover the exposed portion of the SiGe epitaxial layer 42L′ exposed on the sidewall of the second contact hole HB. The diffusion barrier 65 is formed to prevent a silicidation reaction between the exposed SiGe epitaxial layer 42L′ and a barrier metal layer (70 in FIG. 1E), which will be described later.

【0043】 As shown in FIG. 1D, the diffusion barrier layer 65 may be a spacer layer formed on the sidewall of the second contact hole HB. The thickness of the spacer layer has the range of 20 Å to 500 Å. The spacer layer may have, for example, an etch selectivity with respect to the interlayer insulating layer 60.It can be formed into the silicon nitride film had. For example, after the mask layer M3 exposing the second contact hole HB is formed, a silicon nitride layer having a predetermined thickness may be formed in the second contact hole HB. Thereafter, an etch-back process may be performed using the selectivity of the interlayer insulating layer 60 and the silicon nitride layer

to form a diffusion barrier layer 65 in the form of a spacer layer covering the sidewall of the second contact hole HB. However, the inventive concept is not limited thereto, and the diffusion barrier layer 65 may be formed on both the sidewalls of the first contact hole HA and the second contact hole HB without forming the mask layer M3.

【0044】 Referring to FIG. 1E, a barrier metal layer having a predetermined thickness may be formed in the first and second contact holes HA and HB. 70) is formed. The barrier metal layer 70 may be formed by a blanket deposition process without a mask layer.

【0045】 The chemical vapor deposition capable of the film formation which the barrier metal layer(70) uniforms (conformal) or the atomic layer deposition (atomic layer deposition; ALD) may be used. In addition, the barrier metal layer 70 may be formed by physical vapor deposition such as sputtering. The barrier metal layer 70 may be formed of at least one of Ti, Ni, Co, Pd, and Pt, or an alloy thereof. The barrier metal layer 70 may have a thickness of about 10 Å to about 400 Å.

【0046】 After the barrier metal layer 70 is formed, silicide films 80A and 80B are formed between the barrier metal layer 70 and the exposed SiGe epitaxial layer 42L and Si epitaxial layer 41L, respectively, through heat treatment at a relatively low temperature, for example, about 300˚ C. to 650˚ C. In some embodiments, the barrier metal layer (70) not participating in the silicidation reaction is subjected to a suitable etching processThus, the silicide films 80A and 80B may remain locally only on the bottom surfaces of the first and second contact holes HA and HB.

【0047】 As a result, silicide layers 80A and 80B having different compositions are formed in the first contact hole HA and the second contact hole HB. That is, the silicide film 80A in the first contact hole HA is formed of M (Si) containing Ge by the SiGe epitaxial layer 42L.$_{1-y}$Ge$_y$The silicide film 80B in the

second contact hole HB may be an MSi film formed by the exposed Si epitaxial layer 41L.

【0048】As shown in FIG. 1F, a contact plug 90 filling the first and second contact holes HA and HB is formed on the silicide layers 80A and 80B. The contact plug 90 may be formed of tungsten (W), aluminum (Al), copper (Cu), molybdenum (Mo), titanium (Ti), tantalum (Ta), ruthenium (Ru), tungsten (W), or an alloy thereof. However, this is merely an example, and the present invention is not limited thereto. For example, the contact plug 90 may be a conductive nitride of the metals illustrated above. Thereafter, a circuit for supplying power connected to the contact plug and a metal wiring process may be performed to complete the semiconductor device 100. The semiconductor device 100 may be, for example, a P-type MOSFET of a peripheral circuit region of a dynamic random access memory (DRAM) and an N-type MOSFET of the peripheral circuit region and a memory cell region.

【0049】in the first active region and the silicide film (80A, 80B) contacting the contact plug(90) in the second active area everyone lowers the Schottky barrier height of the contact area and the sheet resistance is reducedIt turns on. In particular, in the first active region where the P-type field effect transistor 50A is formed, Si having higher reactivity than Ge preferentially reacts during the silicidation reaction of the SiGe epitaxial layer 42L and the barrier metal layer 70. As a result, the Ge concentration increases at the interface between the SiGe epitaxial layer 42L and the barrier metal layer 70. As the concentration of Ge increases, the band gap of the contact region may decrease. Since the reduction of the band gap reduces the height of the Schottky barrier, the contact resistance of the P-type field effect transistor 50A may be rapidly reduced.

【0050】According to the above-described embodiment, by simultaneously forming the epitaxial double layer 40E1 having the same structure with

respect to the P-type field effect transistor 50A and the N-type field effect transistor 50B and adjusting the depth of the contact holes HA and HB exposing the epitaxial double layer 40E1 in the interlayer insulating film 60, the silicide films 80A and 80B having a low Schottky barrier with respect to the P-type and N-type field effect transistors 50A and 50B can be simultaneously formed, preferably, without a blocking process.

【0051】 2A to 2D are cross-sectional views illustrating a method of manufacturing a semiconductor device 200 according to another embodiment of the present invention. Hereinafter, descriptions of constituent members having the same reference numerals as those of the constituent members illustrated in FIGS. 1A to 1F will be omitted, and the above-described matters may be referred to.

【0052】 Referring to FIG. 2A, a P-type field effect transistor 50A and an N-type field effect transistor 50B are formed on a first active region and a second active region of a substrate 10, respectively. Thereafter, on source / drain regions (32a, 32b) of the first exposing and the second active areaThe SiGe epitaxial layer (42L) is formed. Thereafter, a Si epitaxial layer 41L is formed on the SiGe epitaxial layer 42L on the first and second active regions. These epitaxial layers 41L and 42L may be formed simultaneously on the first and second active regions using a selective epitaxial growth method. The epitaxial double layer 40E2 composed of the SiGe epitaxial layer 42L and the Si epitaxial layer 41L has a stacked structure in which the stacking order of the epitaxial double layers 40E1 shown in FIG. 1A is reversed.

【0053】 Thereafter, an ion implantation process may be performed on the epitaxial double layers 40E2 on the first active region and the second active region. However, this is merely an example, and as will be described later with reference to FIGS. 2B and 2C, an ion implantation process may be performed on the contact pad layer 40PA on the exposed first active region

after the first contact hole HA is formed in the interlayer insulating layer 60, and then the ion implantation process may be performed on the contact pad layer 40PB on the exposed second active region after the second contact hole HB is formed. Although not shown, the epitaxial double layer 40E2 may extend onto a partial region of the adjacent device isolation layer 11.

【0054】 In some embodiments, before forming the epitaxial double layer 40E2, a trench region (see 10T of FIG. 3C) having a predetermined depth may be formed in the region of the substrate 10 between the gate spacer film 24 of the first active region and the device isolation film 11. In this case, the SiGe epitaxial layer 42L formed on the first active region may be buried in the trench region. The buried SiGe epitaxial layer applies a compressive stress to the channel region of the P-type field effect transistor 50A. As a result, the hole of the P-type field effect transistor 50A is formed.The sameness betters. On current can be improved. This will be completely described with reference to FIGS. 3A to 3F to be described later.

【0055】 Referring to FIG. 2B, an interlayer insulating layer 60 is formed on the substrate 10 to cover upper portions of the P-type and N-type field effect transistors 50A and 50B and the epitaxial double layers 40E2. Thereafter, a mask layer M1 exposing a region where the first contact hole H1 is to be formed is formed on the interlayer insulating layer 60. Thereafter, a first contact hole HA is formed in the interlayer insulating layer 60 by an etching process using the mask layer M1.

【0056】 The etching depth of the first contact hole HA is adjusted so that the bottom surface of the first contact hole HA penetrates the Si epitaxial layer 41L′ to expose the underlying SiGe epitaxial layer 42L. The etching process of the first contact hole HA may be continuously performed using the same etching gas with respect to the interlayer insulating layer 60 and the Si epitaxial layer 41L, or may be discontinuously performed using other

known etching gases in consideration of etching selectivity of the interlayer insulating layer 60 and the Si epitaxial layer 41L.

【0057】 Referring to FIG. 2C, a mask layer M2 is formed on the interlayer insulating layer 60 to expose a region where the second contact hole HB is to be formed. Thereafter, a second contact hole HB is formed in the interlayer insulating layer 60 using a plasma dry etching process. The etching depth of the second contact hole HB is adjusted so that the bottom surface of the second contact hole HB exposes the Si epitaxial layer 41L. As a result, the contact pad layer 40PB for the N-type field effect transistor 50B is completed.

【0058】 In this embodiment, unlike the embodiment described above with reference to FIGS. 1A to 1F, the second embodiment is different from the second embodiment.The SiGe epitaxial layer is not exposed to the sidewall of the contact hole HB. Accordingly, the diffusion barrier 65 shown in FIG. 1D may not be formed.

【0059】 Referring to FIG. 2D, a barrier metal layer 70 having a predetermined thickness is formed in the first and second contact holes HA and HB. The barrier metal layer 70 may be formed by a blanket process without a mask. The thickness of the barrier metal layer 7 may have a size of 10 Å to 400 Å.

【0060】 After the barrier metal layer 70 is formed, the barrier metal layer 70 and the exposed SiGe epitaxial layer 42L and Si epitaxial layer 41L react with each other through heat treatment, and low-resistance silicide films 80A and 80B are formed at their contact interfaces. In some embodiments, the barrier metal layer 70 that does not participate in the silicidation reaction may be removed by an appropriate etching process to locally leave the silicide layers 80A and 80B only on the bottom surfaces of the first and second contact holes HA and HB.

【0061】 As a result, silicide layers 80A and 80B having different compositions are formed in the first contact hole HA and the second contact hole HB.

That is, the silicide film 80A in the first contact hole HA is exposed by the SiGe epitaxial layer 42L to form an M (Si) layer including $Ge._{1-y}Ge_y$The silicide film 80B in the second contact hole HB may be an MSi film formed by the Si epitaxial layer 41L.

【0062】 Thereafter, as described above with reference to FIG. 1F, contact plugs 90 are formed on the silicide layers 80A and 80B to fill the first and second contact holes HA and HB, and appropriate.One metal wiring process may be performed to complete the semiconductor device 200.

【0063】 According to the above-described embodiment, by simultaneously forming the epitaxial double layer 40E2 having the same structure with respect to the P-type field effect transistor 50A and the N-type field effect transistor 50B and adjusting the depths of the contact holes HA and HB exposing the epitaxial double layer 40E2 in the interlayer insulating film 60, silicide films 80A and 80B capable of providing a low Schottky barrier with respect to the P-type field effect transistor 50A and the N-type field effect transistor 50B may be simultaneously formed, preferably, without a blocking process.

【0064】 3A to 3D are cross-sectional views illustrating a method of manufacturing a semiconductor device 300 according to another embodiment of the present invention. Hereinafter, descriptions of constituent members having the same reference numerals as those of the constituent members illustrated in FIGS. 1A to 2D will be omitted, and the above-described matters may be referred to.

【0065】 Referring to FIG. 3A, first and second gate stacks 20A and 20B are formed on the first active region and the second active region of the substrate 10, respectively. The gate stacks 20A and 20B may include a gate insulating layer 21, gate conductive layers 22a and 22b, and a capping layer 23. After the gate stacks 20A and 20B are formed, the low-doped

drain regions 31a and 31b may be formed by an ion implantation process. Thereafter, a gate spacer layer 24 may be formed on sidewalls of the gate stacks 20A and 20B. Thereafter, a suitable mask layer (not shown) is formed by a photolithography process to form a high-concentration source/drain region 32b in the second active region of the substrate 10.

【0066】 Referring to FIG. 3B, an interlayer insulating layer 60 is formed on the substrate 10 to cover the P-type and N-type field effect transistors 50A and 50B. In some embodiments, the etch stop layer 60S may be formed on the first active region and the second active region exposed before the interlayer insulating layer 60 is formed, in order to accurately adjust an overetch amount of the substrate 10 to be described later. The etch stop layer 60S may be formed of a material having an etch selectivity with respect to the interlayer insulating layer 60. For example, when the interlayer insulating layer 60 is a silicon oxide layer, the interlayer insulating layer 60 may be formed of a silicon nitride layer having an etch selectivity with respect to the silicon oxide layer.

【0067】 Referring to FIG. 3C, a mask layer M1 is formed on the interlayer insulating layer 60 to expose a region where the first contact hole HA is to be formed. Thereafter, a first contact hole HA exposing the surface of the first active region of the substrate 10 is formed by an etching process using the mask layer M1. An etching process is further performed on the surface of the first active region exposed by the first contact hole HA to form trench regions 10T in contact with the channel region of the P-type field effect transistor 50A. The depth h of the trench region 10T is adjusted so that compressive deformation can be induced in the channel by the buried SiGe epitaxial layer 43L (FIG. 3D). The depth h of the trench region 10T may be, for example, 100 Å to 1500 Å. Reference numeral 60S′ denotes an etch stop layer penetrated when the first contact hole HA is formed.

【0068】 The etching process for forming the first contact hole HA and the trench region 10T may be continuously performed by plasma etching using the same etching gas. Optionally, the first contact hole HA and the trench region 10T may be discontinuously performed using other known etching gases in consideration of an etch selectivity. Moreover, the first contactThe hole HA may be formed by an anisotropic etching method, and the trench region 10T may be formed by an isotropic etching method, as illustrated in FIG. 3C. For example, reactive ion etching using plasma may be performed for anisotropic etching of the first contact hole HA. In addition, isotropic etching for forming the trench region 10T may be performed by a dry etching method using plasma or a wet etching method using an etching solution. The undercut d by isotropic etching of the trench region 10T may be in a range of 30 Å to 1500 Å in a direction parallel to the main surface of the substrate 10.

【0069】 Referring to FIG. 3D, the mask film M1 is removed, and the SiGe epitaxial layer 43L is buried in the trench region 10T of the first active region. The buried SiGe epitaxial layer 43L may be formed by a selective epitaxial growth method. The concentration of Ge in the buried SiGe epitaxial layer 43L may be 3% to 50%. The thickness of the SiGe epitaxial layer 43L may be 100 Å to 1500 Å. In this case, the thickness of the SiGe epitaxial layer 43L may be equal to the depth h of the trench region 10T or may be thicker as shown in FIG. 3D. However, the inventive concept is not limited thereto, and the thickness of the SiGe epitaxial layer 43L may be smaller than the depth h of the trench region 10T.

【0070】 When isotropic etching is performed during the formation of the trench region 10T, the distance between the channel of the P-type field effect transistor 50A and the buried SiGe epitaxial layer 43L may be further shortened by the undercut, thereby further increasing the channel compressive stress effect by the SiGe epitaxial layer 43L. In the case where a

silicon single crystal substrate is used as the substrate 10, in the case where the channel direction of the P-type field effect transistor 50A is <110>, the in-channel hole mobility is maximized.Therefore, in the above-described embodiment, by designing the layout of the semiconductor device 300 so that the channels of the P-type field effect transistor 50A are aligned in the direction 110, it is possible to optimize the effect of improving the hole mobility by the buried SiGe epitaxial layer 43L.

【0071】 In some embodiments, an ion implantation process may be performed on the buried SiGe epitaxial layer 43L to form source/drain regions of the P-type field effect transistor 50A. Alternatively, in-situ doping may be performed simultaneously with the formation of the buried SiGe epitaxial layer 43L. For example, together with the formation gas of the SiGe epitaxial layer 43L, $B._2H_5$The P-type SiGe epitaxial layer 43L doped with a high concentration may be formed using a Group III element-containing gas.

【0072】 Referring to FIG. 3E, a mask layer M2 is formed on the interlayer insulating layer 60 to expose a region where the second contact hole HB is to be formed. Thereafter, a second contact hole HB is formed in the interlayer insulating layer 60 by an etching process. The etching depth of the second contact hole HB is adjusted so that the bottom surface of the second contact hole HB exposes the surface of the second active region of the substrate 10.

【0073】 Referring to FIG. 3F, a barrier metal layer 70 having a predetermined thickness is formed in the first contact hole HA and the second contact hole HB by a blanket process. The barrier metal layer 70 may have a thickness of about 10 Å to about 400 Å. After the barrier metal layer(70) is formed, the thermal process is proceed.

【0074】 SiGe buried with the barrier metal layer (70) in the first active region by the heat treatmentA silicide film (80A) is formed between the epitaxial layers (43L), and a silicide film (80B) is formed between the barrier metal layer

(70) and the exposed source/drain regions (32b) of the substrate (10) in the second active region. As a result, silicide layers 80A and 80B having different compositions are formed in the first contact hole HA and the second contact hole HB. That is, the silicide film 80A in the first contact hole HA is exposed by the SiGe epitaxial layer 42L to form an M (Si) layer including $Ge._{1-y}Ge_y$The silicide film 80B in the second contact hole HB may be an MSi film formed by the Si epitaxial layer 41L.

【0075】 Thereafter, a contact plug (see 90 of FIG. 1F) filling the first and second contact holes HA and HB may be formed on the silicide layers 80A and 80B, and a metal wiring process may be performed as well known in the art, thereby completing the semiconductor device 300.

【0076】 In the above-described embodiment, after the interlayer insulating layer 60 is formed, the first contact hole HA is formed, and then the buried SiGe epitaxial layer 43L is formed using the first contact hole HA. Accordingly, in order to form the SiGe epitaxial layer 43L buried only in the first active region, it is not necessary to separately form a blocking film for passivating the second active region.

【0077】 Conventionally, a blocking film was formed on the second active region to form the SiGe epitaxial layer 43L in the first active region. a photolithography process and an etching process to form, for example, a silicon nitride film on the entire surface of the substrate (10) to cover the second active region and expose the first active regionIt is proceed and it exposes only the first active region. After the SiGe epitaxial layer 43L is formed on the exposed first active region, an etching process for removing the blocking film covering the transistor of the second active region should be performed again to complete the transistor of the second active region. However, according to embodiments of the inventive concept, since the interlayer insulating layer 60 functions as a blocking layer and a transistor

forming process such as a SiGe epitaxial layer forming process using the contact holes HA and HB is completed, there is an advantage in a process in which a photolithography process and an etching process are not required.

【0078】 4 is a cross-sectional view showing a method of manufacturing a semiconductor device 400 according to another embodiment of the present invention.

【0079】 Referring to FIG. 4, an interlayer insulating layer 60 is formed on the substrate 10 to cover the P-type and N-type field effect transistors 50A and 50B. Thereafter, a suitable mask layer is used to form a first contact hole HA exposing the surface of the first active region of the substrate 10. Thereafter, a SiGe epitaxial layer 44L may be formed on the first active region exposed on the bottom surface of the first contact hole. The SiGe epitaxial film 44L may be formed by a selective epitaxial growth method.

【0080】 Thereafter, as described above with reference to FIG. 3E, the second contact hole HB is formed in the interlayer insulating layer, and as described above with reference to FIG. 3F, the metal barrier layer 70 is formed in the first contact hole HA and the second contact hole HB, and a heat treatment is performed. Accordingly, silicide layers 80A and 80B having different compositions may be formed in the first contact hole HA and the second contact hole HB. That is, the silicide layer 80A in the first contact hole HAM (Si) including Ge by the SiGe epitaxial layer $44L_{1-y}Ge_y$The silicide layer 80B in the second contact hole HB may be an MSi layer formed by the exposed second active region.

【0081】 According to the present embodiment, $M(Si)_{1-y}Ge_yM(Si)$ capable of improving the contact resistance of the P-type field effect transistor (50A) without a separate photolithography or etching process by using the first contact hole (HA) formed in the interlayer insulating layer (60) to form a layer$_{1-y}Ge_y$) There is an advantage that a film can be obtained.

【0082】 5 is a cross-sectional view showing a method of manufacturing a semiconductor device 500 according to another embodiment of the present invention.

【0083】 Referring to FIG. 5, an interlayer insulating layer 60 may be formed on the substrate 10 to cover the P-type and N-type field effect transistors 50A and 50B. Thereafter, a suitable mask layer is used to form a first contact hole HA exposing the surface of the first active region of the substrate 10. Thereafter, a Ge ion implantation process may be performed to provide Ge atoms on the first active region exposed on the bottom surface of the first contact hole HA. The Ge ions may form a Ge atomic layer 45L deposited on the first active region as shown in FIG. 5 according to the acceleration energy of the Ge ions, or may penetrate into the source/drain region 32a to form a SiGe layer near the upper surface of the source/drain region 32a. In some embodiments, a heat treatment may be performed at a suitable temperature after the Ge ion implantation process.

【0084】 The above-described Ge ion implantation process is exemplary, and the present invention is not limited thereto. For example, a Ge source may be formed on the first active region exposed to the bottom surface of the first contact hole HAthe pulsed laser ablation deposition to provide the ruler; PLAD) or a gas cluster ion beam deposition method; The Ge atomic layer 45L may be formed by GCIB. The structure of the Ge atomic layer 45L according to the present embodiment may be single crystal, amorphous, microcrystalline, or polycrystalline.

【0085】 Thereafter, as described above with reference to FIG. 3E, the second contact hole HB is formed in the interlayer insulating layer, and as described above with reference to FIG. 3F, the metal barrier layer 70 is formed in the first contact hole HA and the second contact hole HB, and a heat treatment is performed. Accordingly, silicide layers 80A and 80B having different

compositions may be formed in the first contact hole HA and the second contact hole HB. That is, the silicide layer 80A in the first contact hole HA includes M (Si) including the Ge atomic layer 45L.$_{1-y}Ge_y$The silicide layer 80B in the second contact hole HB may be an MSi layer formed by the exposed second active region.

【0086】According to the present embodiment, $M(Si)_{1-y}Ge_yM(Si)$ capable of improving the contact resistance of the P-type field effect transistor (50A) without a separate photolithography or etching process by using the first contact hole (HA) formed in the interlayer insulating layer (60) to form a layer$_{1-y}Ge_y$) There is an advantage that a film can be obtained.

【0087】The embodiments disclosed with reference to the accompanying drawings may be practiced alone or in combination, unless expressly limited. For example, in the embodiments shown in FIGS. 1A-1F, the SiGe epitaxial layer 42L may be the Ge atomic layer 45L shown in FIG. 5.

【0088】While the inventive concept has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the inventive concept as defined by the following claims.

【Claims】

【Claim 1】

The substrate including first and second active area

The respective formed P-type field effect transistor on first and second active area and N type field effect transistor

The first and the second contact pad layer including the Si epitaxial layer and the SiGe epitaxial layer which successively is laminated on the source / drain regions of N type MOSFET and P-type field effect transistor

and an interlayer insulating film which is formed on the P-type and N-type field effect transistors and includes a first contact hole which has a first bottom surface to expose the SiGe epitaxial layer of the first contact pad layer and a second contact hole which has a second bottom surface to expose the Si epitaxial layer by penetrating the SiGe epitaxial layer of the second contact pad layer.

The second metal silicide layer which may not contain the Ge formed on the first metal silicide layer and the second bottom surface containing the Ge formed on the first bottom surface and

and contact plugs which are formed on the first and second metal silicide layers and fill the first and second contact holes.

【Claim 2】

The method according to claim 1, wherein the method comprises the following steps:

The semiconductor device further includes a diffusion barrier layer between the sidewall of the second contact hole and the metal silicide layer.

【Claim 3】

The method according to claim 1, wherein the method comprises the following steps:

At least one of the first and second contact pad layers is grown in a direction parallel to the main surface of the substrate to be extended onto a partial region of a device isolation layer defining the first and second active regions.

【Claim 4】

The method according to claim 1, wherein the method comprises the following steps:

The thickness of the Si epitaxial layer may be in range of 10 Å to 500 Å

The semiconductor device in which the thickness of the SiGe epitaxial layer is in range of 30 Å to 500 Å.

【Claim 5】

The method according to claim 1, wherein the method comprises the following steps:

The Ge molarity of the SiGe epitaxial layer is in a range of 3% to 50%.

【Claim 6】

The substrate including first and second active area

The respective formed P-type field effect transistor on first and second active area and N type field effect transistor

The respective first contact pad layer included and the second contact pad layer the SiGe epitaxial layer and the Si epitaxial layer laminated on the source / drain regions of N type field effect transistor and P-type field effect transistor according to order

and an interlayer insulating film which is formed on the P-type and N-type field effect transistors and includes a first contact hole having a first bottom surface which penetrates the Si epitaxial layer of the first contact pad layer and exposes the SiGe epitaxial layer and a second contact hole having a second bottom surface which exposes the Si epitaxial layer of the second contact pad layer.

The second metal silicide layer which may not contain the Ge formed on the first metal silicide layer and the second bottom surface containing the Ge formed on the first bottom surface and

and contact plugs which are formed on the first and second metal silicide layers and fill the first and second contact holes.

【Claim 7】

The method according to claim 6, wherein the method comprises the following steps:

The semiconductor device in which at least a part of the SiGe epitaxial layer of the first contact pad layer is buried within the first active region.

【Claim 8】

The method according to claim 6, wherein the method comprises the following steps:

At least one of the first and second contact pad layers is grown in a direction parallel to the main surface of the substrate to be extended onto a partial region of a device isolation layer defining the first and second active regions.

【Claim 9】

The method according to claim 6, wherein the method comprises the following steps:

The thickness of the Si epitaxial layer may be in range of 10 Å to 500 Å

The semiconductor device in which the thickness of the SiGe epitaxial layer is in range of 30 Å to 500 Å.

【Claim 10】

The method according to claim 6, wherein the method comprises the following steps:

The Ge molarity of the SiGe epitaxial layer is in a range of 3% to 50%.

【Claim 11】

The substrate including first and second active area

The respective formed P-type field effect transistor on first and second active area and N type field effect transistor

The respective first included and the second contact pad layer the Si epitaxial layer and the Ge atomic layer successively laminated on the source / drain regions of N type MOSFET and P-type field effect transistor

The inter-layer insulating film which is formed on P-type and N type field effect transistors and includes the second contact hole having the second bottom surface exposing the Si epitaxial layer through the Ge atomic layer of the second contact pad layer and the first contact hole having the first bottom surface exposing the Ge atomic layer of the first contact pad layer

The second metal silicide layer which may not contain Ge formed in the bottom surface of the first metal silicide layer and the second contact hole containing Ge formed in the first bottom surface of the first contact hole and

the first and second metal silicide layers formed on the first and second metal silicide layersA semiconductor device including contact plugs filling a contact hole.

【Claim 12】

The step of forming the second active area for the first active region for the P-type field effect transistor in the substrate and N type field effect transistor

The step of forming the first gate stack on the first active region

The step of forming the second gate stack on the second active area

The step of at the same time, forming first and second epitaxial bilayers including the Si epitaxial layer on the second active area except for the first active region except for the first gate stack and the second gate stack and SiGe epitaxial layer

The step forming the inter-layer insulating film covering first and second gate stacks and top of epitaxial double layers

The step forming the first contact hole having the first bottom surface exposing the SiGe epitaxial layer of the first epitaxial double layer within the inter-layer insulating film

The step forming the second contact hole having the second bottom surface exposing the Si epitaxial layer within the inter-layer insulating film through the SiGe epitaxial layer of the second epitaxial double layer

Step of at the same time, forming the first metal silicide layer containing Ge in the first bottom surface and the second metal silicide layer which contain may not Ge in the second bottom surface

and forming contact plugs which bury the first and second contact holes on the first and second silicide layers.

【Claim 13】

The method of claim 12, wherein forming the first and second epitaxial double layers at the same time is performed by a selective epitaxial growth method.

【Claim 14】

The method of claim 12, further comprising simultaneously forming the first and second metal silicide layers.

The method may further include forming a diffusion barrier layer covering at least a portion of the SiGe epitaxial layer exposed to a sidewall of the second contact hole.

【Claim 15】

The step of forming the second active area for the first active region for the P-type field effect transistor in the substrate and N type field effect transistor

The step of forming the first gate stack on the first active region

The step of forming the second gate stack on the second active area

The step of at the same time, forming first and second epitaxial bilayers including the SiGe epitaxial layer on the second active area except for the first active region except for the first gate stack and the second gate stack and Si epitaxial layer

The step forming the inter-layer insulating film covering first and second gate stacks and top of epitaxial double layers

forming a first contact hole having a first bottom surface which penetrates the Si epitaxial layer of the first epitaxial double layer and exposes the Si epitaxial layer in the interlayer insulating filmThe step

The step forming the second contact hole having the second bottom surface exposing the Si epitaxial layer of the second epitaxial double layer within the inter-layer insulating film

Step of at the same time, forming the first metal silicide layer containing Ge in the first bottom surface and the second metal silicide layer which contain may not Ge in the second bottom surface

and forming contact plugs which bury the first and second contact holes on the first and second silicide layers.

【Claim 16】

The method of claim 15, wherein forming the first and second epitaxial double layers at the same time is performed by a selective epitaxial growth method.

【Description of Drawings】

【0089】 1A to 1F are cross-sectional views illustrating a method of manufacturing a semiconductor device 100 according to an embodiment of the present invention.

【0090】 2A to 2D are cross-sectional views illustrating a method of manufacturing a semiconductor device 200 according to another embodiment of the present invention.

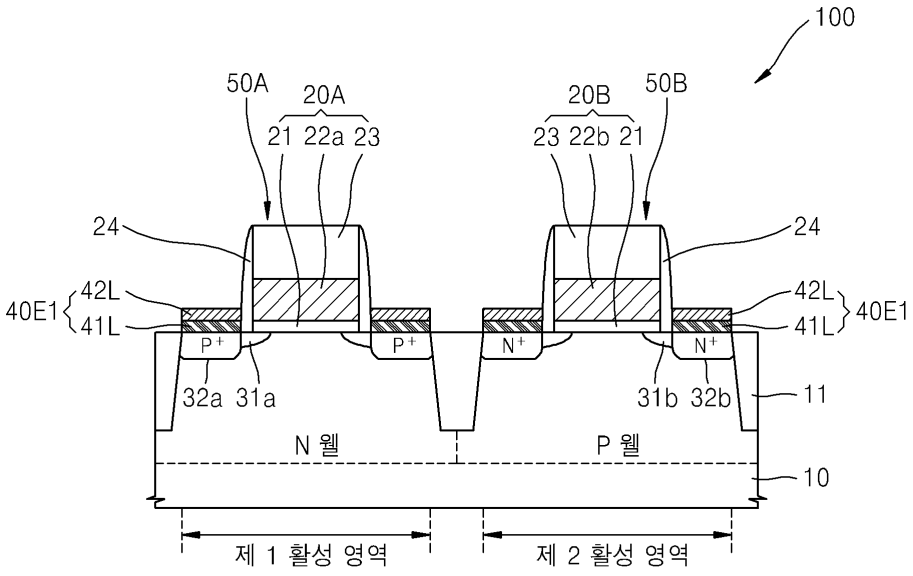
【0091】 3A to 3D are cross-sectional views illustrating a method of manufacturing a semiconductor device 300 according to another embodiment of the present invention.

【0092】 4 is a cross-sectional view showing a method of manufacturing a semiconductor device 400 according to another embodiment of the present invention.

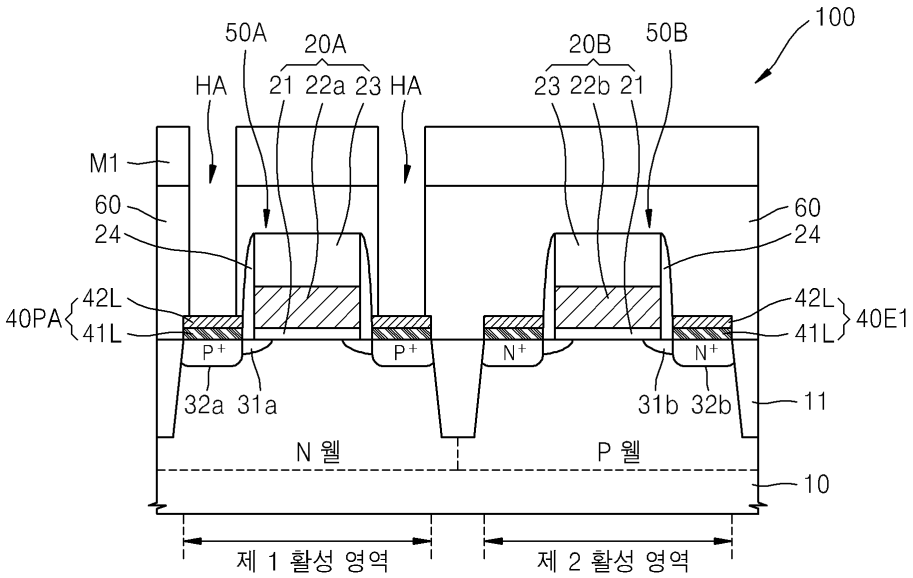
【0093】 5 is a cross-sectional view showing a method of manufacturing a semiconductor device 500 according to another embodiment of the present invention.

【Drawings】

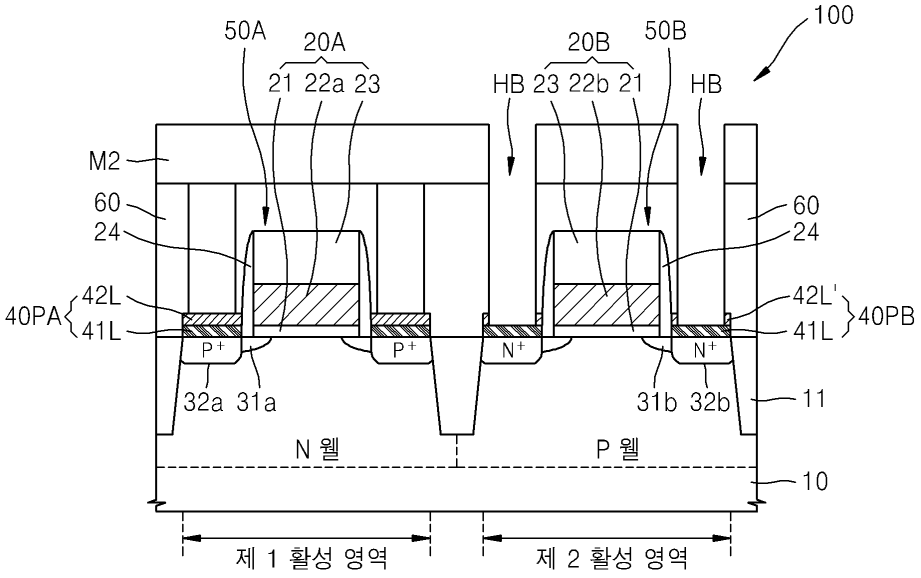
【Drawing 1a】



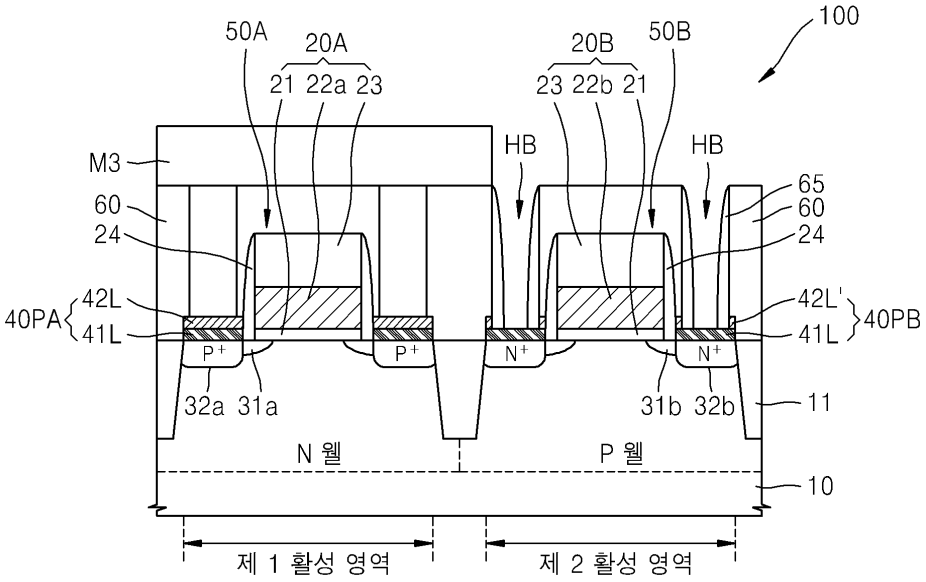
【Drawing 1b】



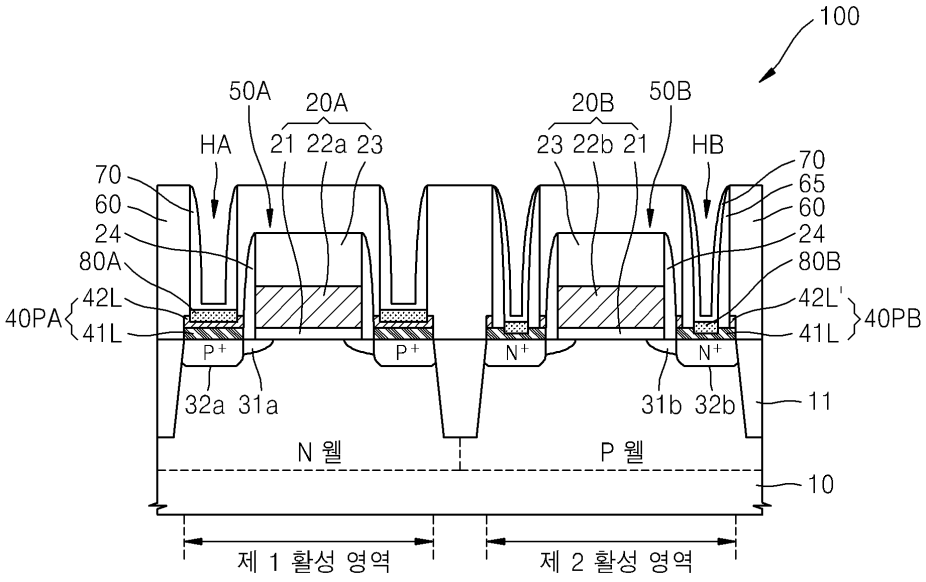
【Drawing 1c】



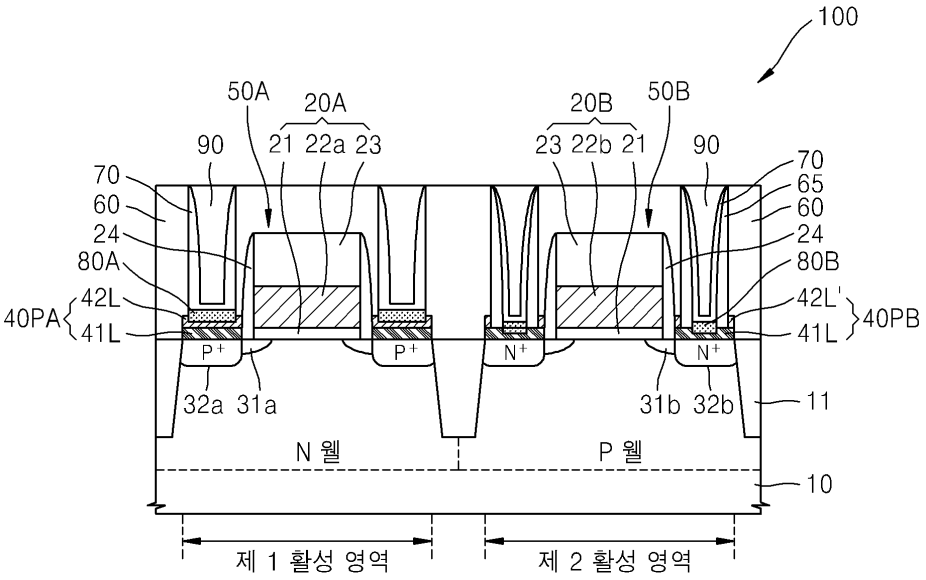
【Drawing 1d】



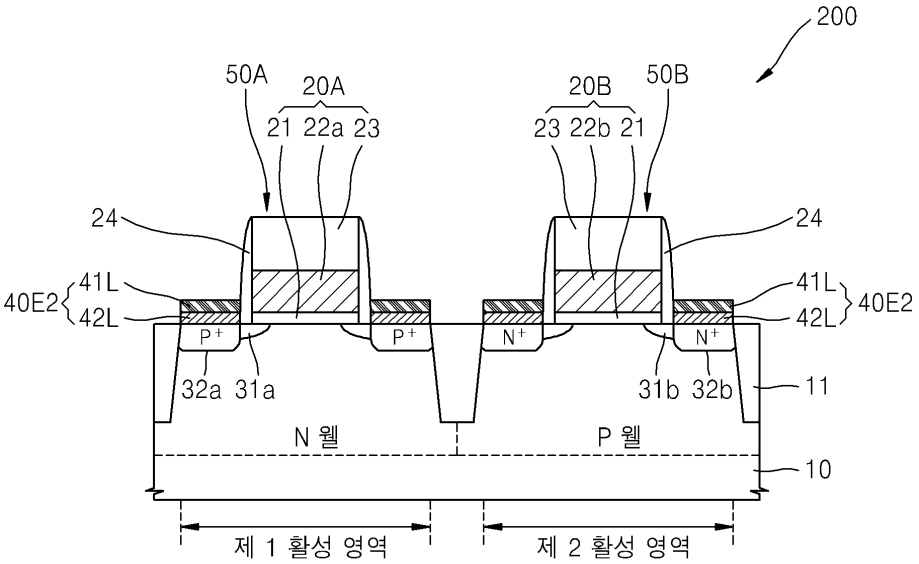
【Drawing 1e】



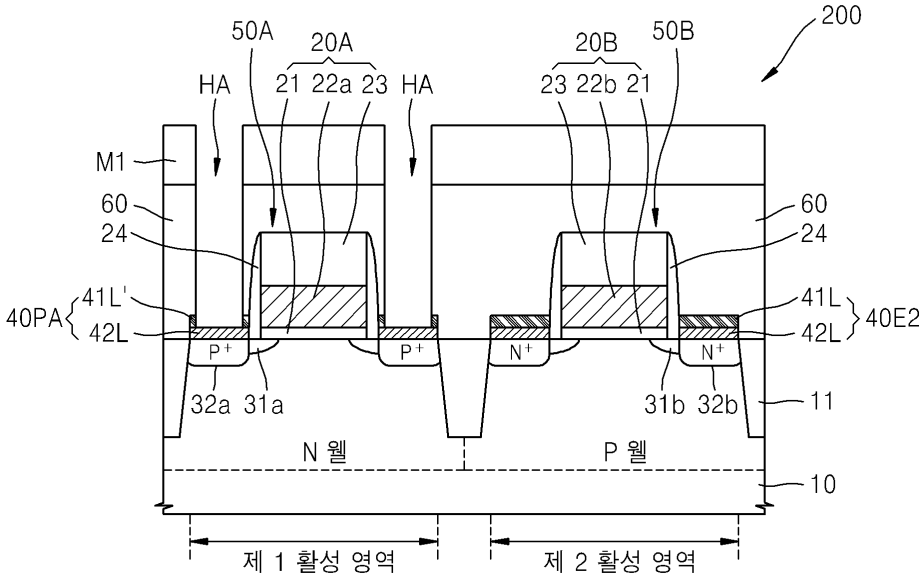
【Drawing 1f】



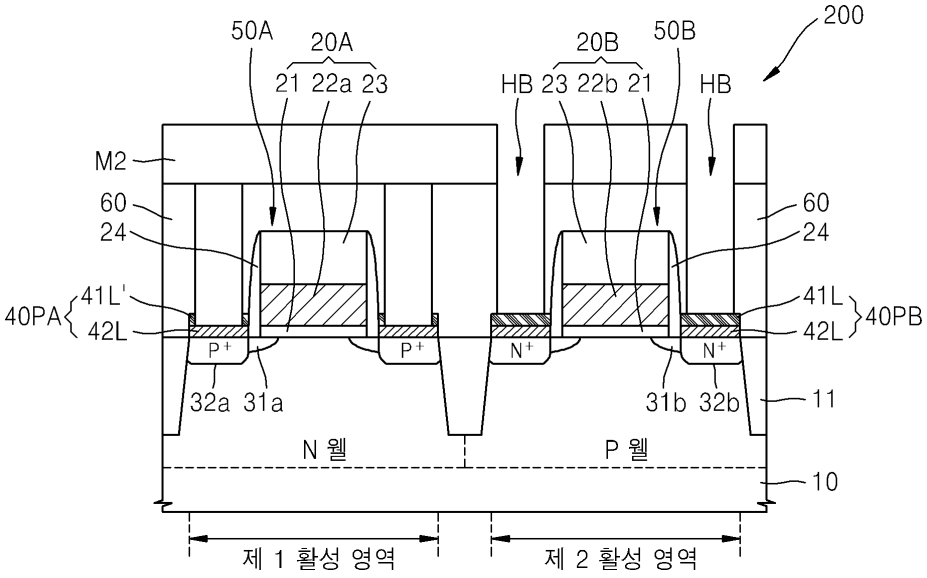
【Drawing 2a】



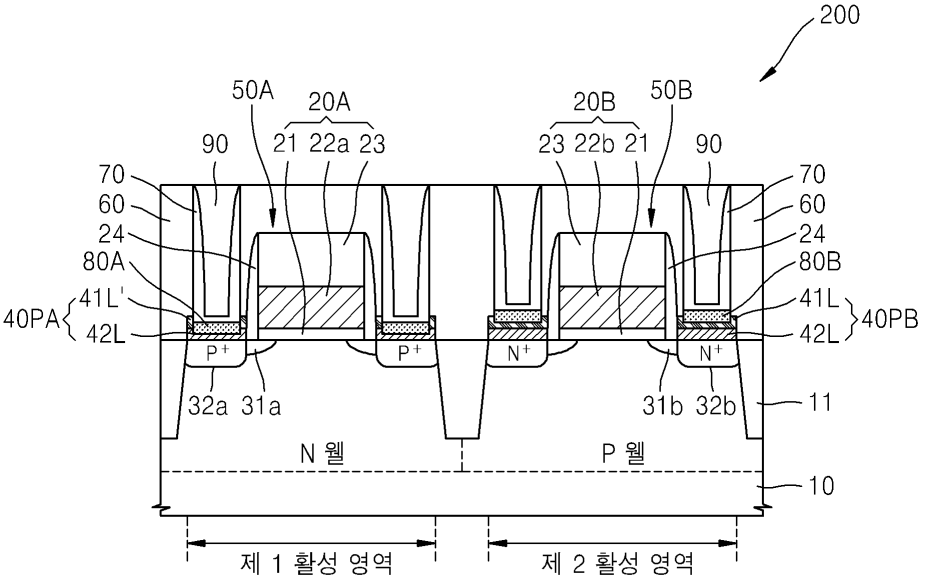
【Drawing 2b】



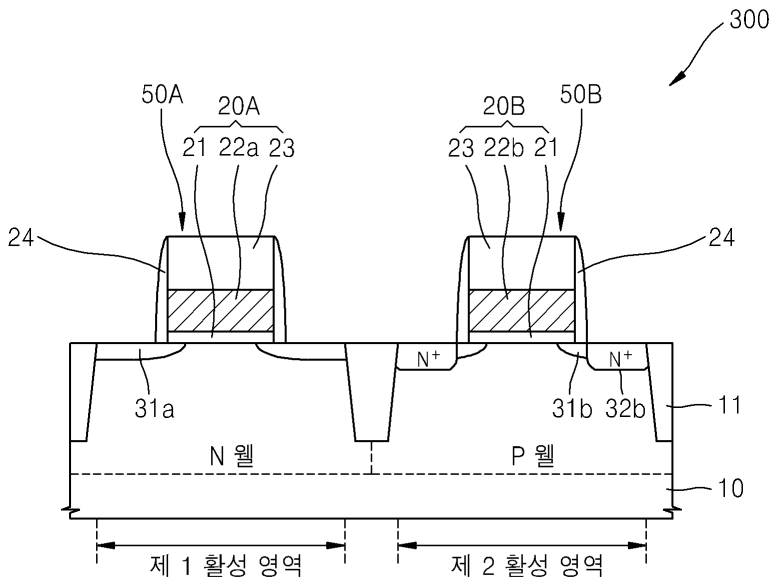
【Drawing 2c】



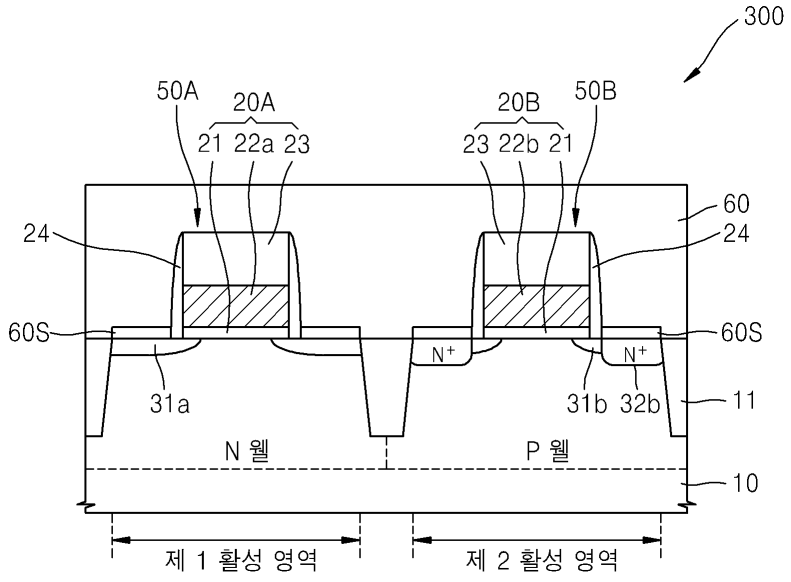
【Drawing 2d】



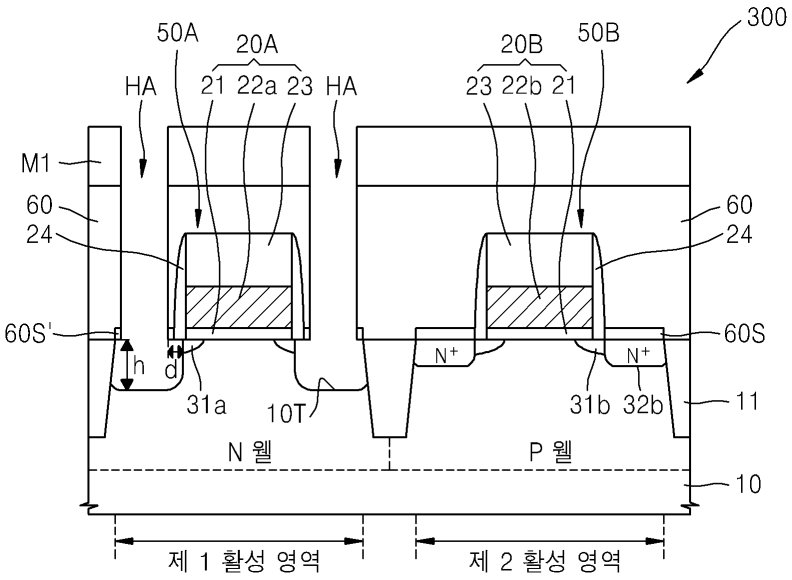
【Drawing 3a】



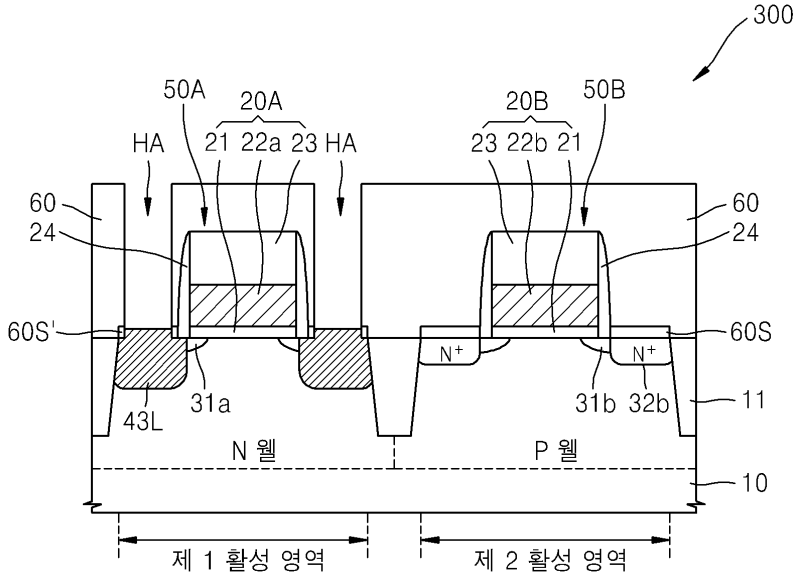
【Drawing 3b】



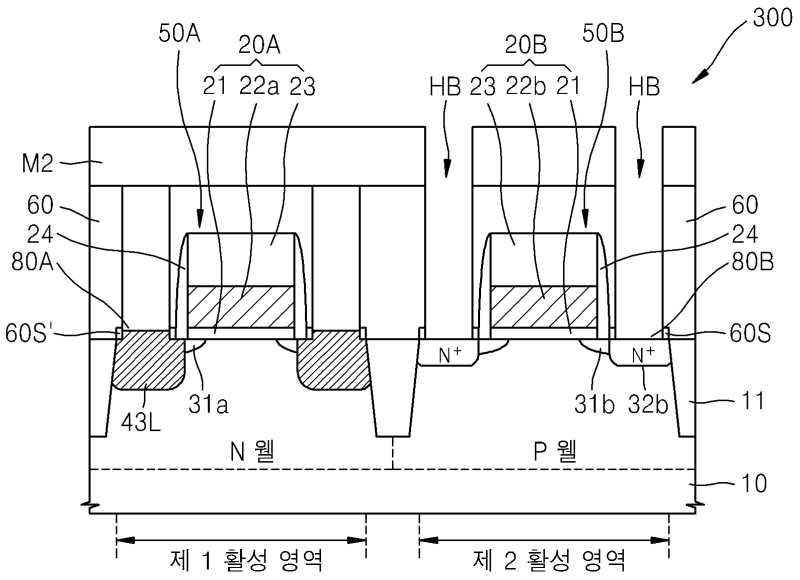
【Drawing 3c】



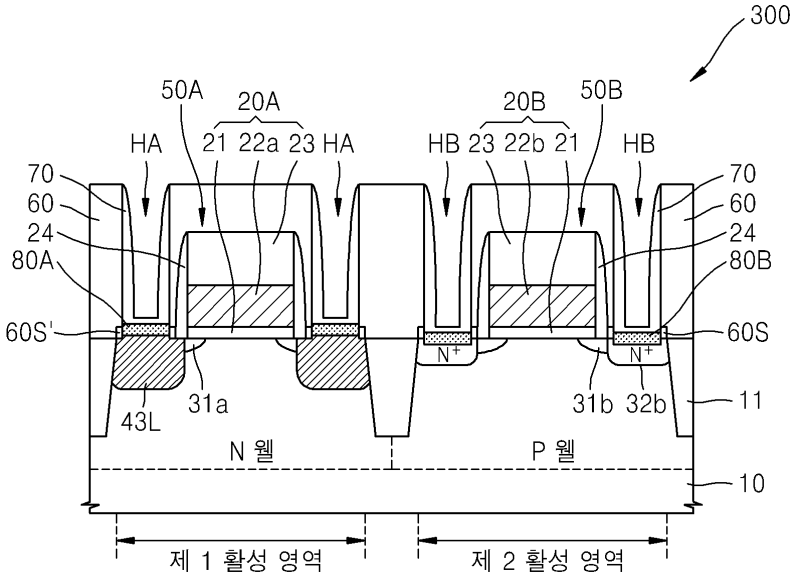
【Drawing 3d】



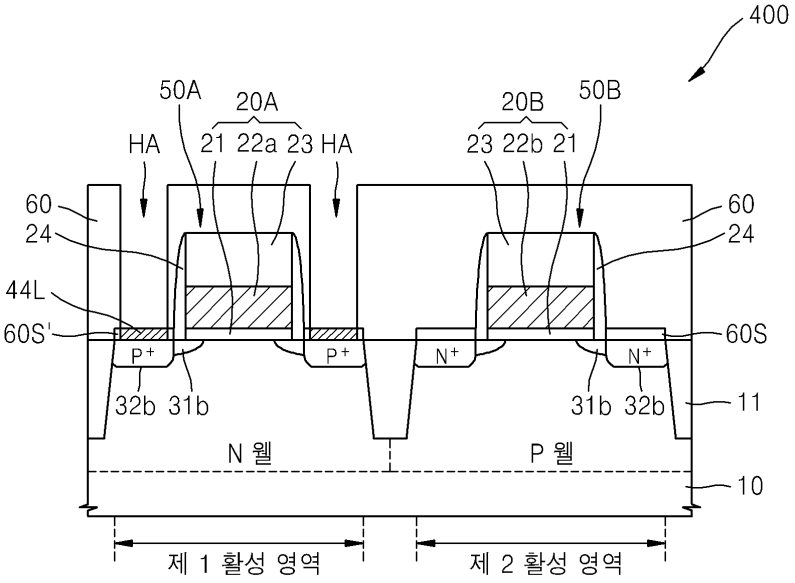
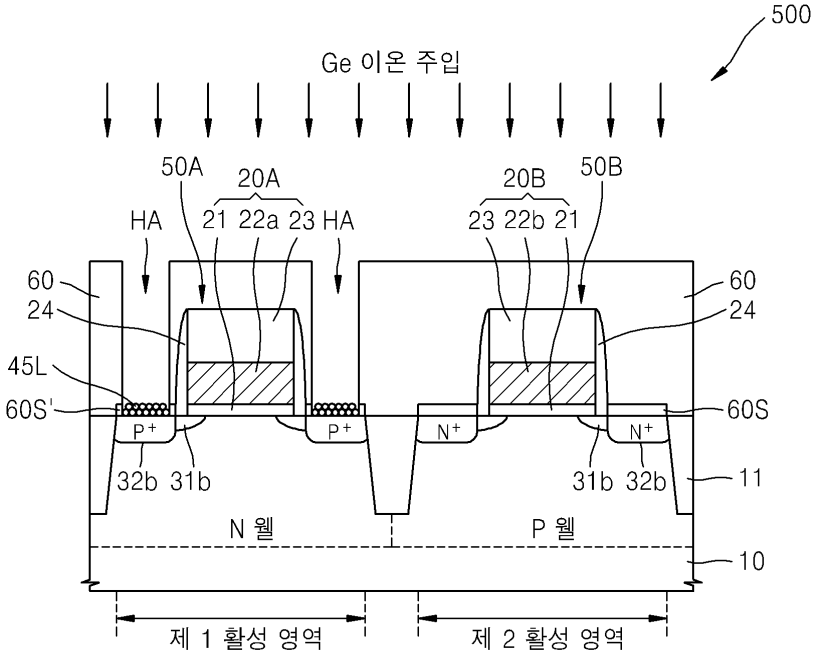
【Drawing 3e】



【Drawing 3f】



【Drawing 4】



【Drawing 5】