A Novel Elevated Source/Drain PMOSFET Formed by Ge-B/Si Intermixing

Pushkar Ranade, *Student Member, IEEE*, Hideki Takeuchi, *Member, IEEE*, Vivek Subramanian, *Member, IEEE*, and Tsu-Jae King, *Senior Member, IEEE*

***Abstract*—Driven by strain relaxation, the rapid thermal annealing (RTA) of B-doped Ge on an Si substrate forms graded $Si_{1-x}Ge_x$ layers with B confined inside. Based on this observation of Ge-B/Si intermixing, a novel elevated source/drain (S/D) PMOSFET fabrication process is proposed. The new process consists of three simple steps: a) selective Ge deposition in S/D regions by conventional LPCVD, b) B implantation, and c) RTA for Ge-B/Si intermixing to form S/D extensions to the channel. Fabricated PMOSFETs with sub–100 nm gate lengths display excellent short channel performance.**

***Index Terms*—Boron diffusion, elevated source–drain MOSFET, silicon–germanium, ultra-shallow junctions.**

I. Introduction

THE elevated source/drain (S/D) MOSFET structure has several advantages in suppressing short channel effects (SCE) [1] and is a promising candidate for planar CMOS technology beyond the 50 nm technology node [2]. While it is compatible with ultrashallow junctions, controlling the lateral dopant profiles to have adequate overlap underneath the gate electrode remains a major challenge. Recent publications have proposed the control of the overlap by dopant ion implantation and rapid thermal annealing before epitaxial Si growth [3] or by recessing the Si substrate and selectively filling it with RTCVD $Si_{1-x}Ge_x$ [4]. B-doped Ge has also been used as a solid-diffusion source to form S/D junctions [5]. In this letter, a novel elevated S/D PMOSFET technology using Ge-B/Si intermixing is described. RTA of the Ge/Si heterostructure forms a graded $Si_{1-x}Ge_x$ layer by strain relaxation, with B completely confined inside the $Si_{1-x}Ge_x$ Lateral Ge-B/Si intermixing enables the formation of S/D extensions without degrading junction abruptness or risking gate dielectric damage.

II. Observation of Ge-B/Si Intermixing

Samples were prepared by depositing Ge (60 nm) and SiO_2 (capping layer [20 nm] to prevent undesirable Ge evaporation) onto Si (100) substrates. This was followed by B implantation (6×10^{15} cm^{-2} @ 5 keV) and 900 °C RTA in N_2 ambient. Fig. 1 shows Ge and B depth profiles obtained by SIMS analysis. Although the expected diffusion length of Ge in Si is less than 1 nm, RTA of undoped Ge/Si formed a ~50 nm graded $Si_{1-x}Ge_x$ layer at the interface. In the presence of B, the intermixing is more enhanced, with the Ge mole fraction varying from ~80% at the top surface to ~1% at 20 nm inside the Si. B was found to be perfectly confined in $Si_{1-x}Ge_x$ region, with a high surface concentration of $\sim 1 \times 10^{21}$ cm^{-3}. Kinks in the concentration profiles are evident for Ge and B at the same depth, where the B concentration is equal to the intrinsic carrier concentration in Si at 900 °C. Detailed analysis indicates that Ge and B are redistributed by strain relaxation so that the p–n junction is located within the graded $Si_{1-x}Ge_x$ layer, and that excess vacancies generated by the intermixing induce Ge-B co-diffusion starting from the kink location [6].

III. Novel Elevated Source/Drain Structure and Fabrication Process

The observed Ge-B/Si intermixing can be advantageous for the formation of ultrashallow p+/n junctions for sub-100 nm PMOSFETs in the following respects: 1) both lateral and vertical B profiles in S/D extensions can be tailored by controlling Ge-B co-diffusion, 2) low sheet resistance is achievable due to high solubility and activation efficiency of B in Ge [7], and 3) the narrow band gap of $Si_{1-x}Ge_x$, combined with the high carrier concentration, should provide lower contact resistance. In this letter, we propose a novel elevated S/D structure that makes use of the aforementioned effects. The processing sequence used to fabricate PMOSFETs is outlined in Fig. 2. The gate dielectric was 2 nm thermal SiO_2 and B implanted poly-$Si_{0.8}Ge_{0.2}$ (150 nm) was used as the gate material in order to reduce the gate depletion effect. The gate was capped with CVD SiO_2 (20 nm) to prevent Ge deposition on the gate electrode. After gate definition using e-beam lithography and reactive ion etching (RIE), Si_3N_4 sidewall spacers (25 nm wide) were formed, and undoped Ge (60 nm) was deposited using LPCVD (340 °C, 600 mTorr using GeH_4). Notably, the Ge deposition was perfectly limited to the S/D regions, in spite of being carried out in a conventional LPCVD furnace. B was then implanted into the Ge layer (6×10^{15} cm^{-2}, 5 keV) through a 20 nm capping layer (SiO_2). The wafers were then annealed at 900 °C for 7 min. During this step, the Ge and B co-diffused vertically as well as laterally (under the sidewall spacers) into the Si to form S/D extensions. Device fabrication was completed with standard contact and metallization processes using Al-2%Si metallurgy.

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P. Ranade is with the Department of Materials Science and Engineering, University of California, Berkeley, CA 94720 USA (e-mail: pranade@eecs.berkeley.edu).

H. Takeuchi, V. Subramanian, and T.-J. King are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA.

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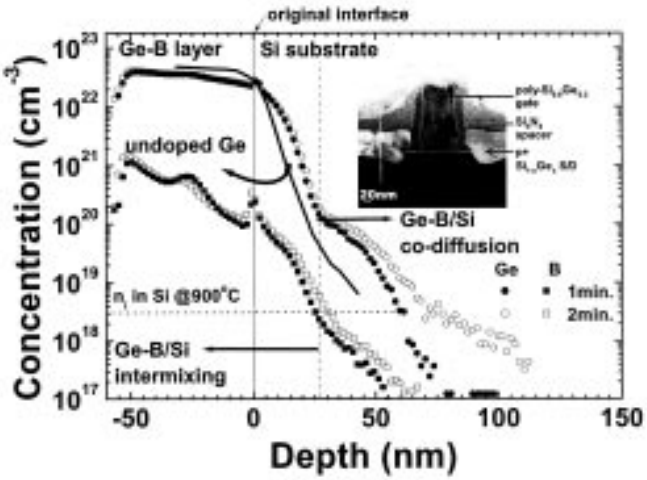

Fig. 1. Ge and B concentration-depth profiles determined by SIMS after RTA at 900 °C. An HRTEM cross-sectional view of a completed PMOSFET is shown in the inset. The dotted line in the inset indicates the approximate location of the SIMS analysis.

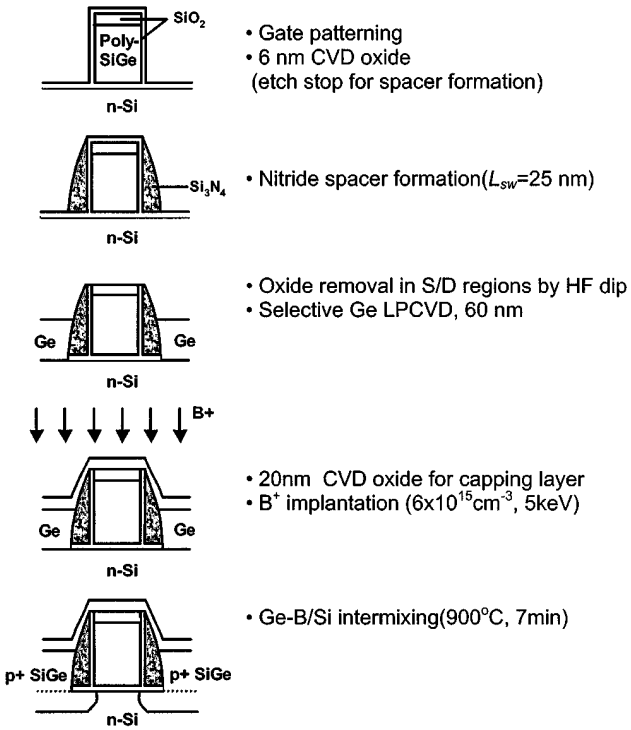

Fig. 2. Process flow used for PMOSFET device fabrication.

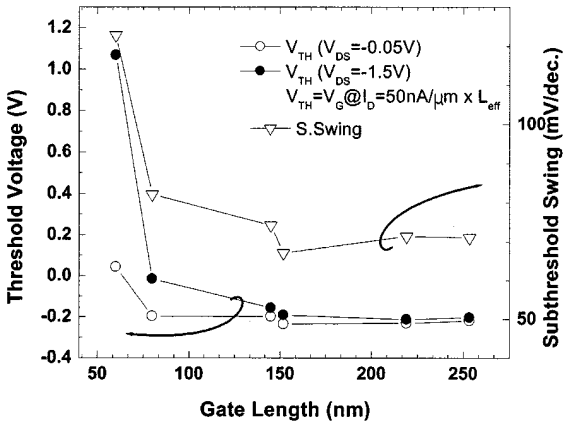

Fig. 3. PMOSFET short-channel performance (subthreshold swing and drain-induced barrier lowering).

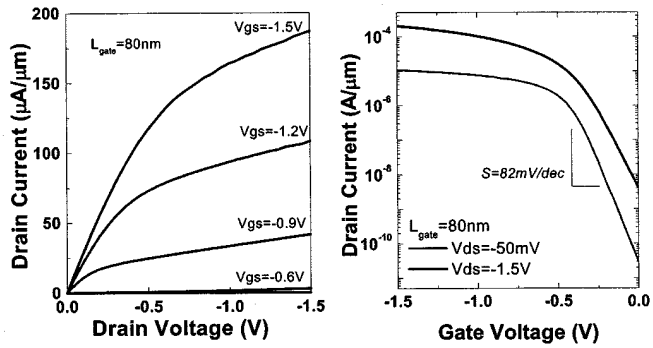

Fig. 4. PMOSFET I–V characteristics, $L_{\rm gate} = 80$ nm.

IV. Device Characterization Results and Discussions

A cross-sectional transmission electron microscope (TEM) image of the PMOSFET is shown in the inset of Fig. 1. The Ge/Si interface is located 10–32 nm inside the Si substrate, and the location of the metallurgical p–n junction is vertically 44 nm and laterally 30 nm from the new interface. Fig. 3 plots the threshold voltage rolloff (at $V_{\rm DS} = -50$ mV and -1.5 V) and subthreshold swing chracteristics. The data show that the new elevated S/D structure effectively suppresses SCE down to 80 nm gate lengths. Severe SCE at 60 nm gate length may be due to the use of a relatively low dopant concentration ($\sim 10^{17}$ cm^{-3}) in the channel regions (designed for the poly-$Si_{0.8}Ge_{0.2}$ gate with a work function of $\sim$4.9 V). The current–voltage (I–V) characteristics for a transistor with $L_{\rm gate} = 80$ nm are shown in Fig. 4. Measured $I_{\rm ON}$ and $I_{\rm OFF}$ are 187 μA/μm and 4.2 nA/μm, respectively, while the subthreshold swing, DIBL, S/D sheet resistance, gate-to-S/D capacitance, and contact resistance were 82 mV/decade, 104 mV/V, 196 $\Omega/\square$, 0.225 fF/μm at $V_G = -1$ V, and 3.3 Ω for 1 μm contact size, respectively.

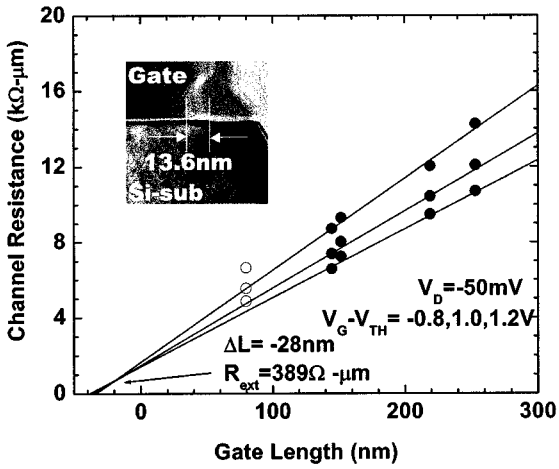

Fig. 5. Channel resistance plot to extract effective gate length ($L_{\rm eff}$) and external resistance. Open points ($L_{\rm gate} = 80$ nm) are excluded from the extraction because of increased short-channel effects. Inset shows an XTEM image that shows the location of the metallurgical junction. Extracted gate length offset value (-28 nm) and the observed location of the metallurgical junction (-13.6 nm) agree reasonably well.

It should be noted that the measured Miller capacitance and estimated contact resistance of 3.3×10^{-8} Ω-μm^2 are comparable to those reported for comparable technology generations [8], [9]. The relatively high sheet resistance is, in part, due to B implantation through the screen oxide, which retained almost half of the implanted dose. Fig. 5 shows the dependence of the channel resistance on channel length. The measured external resistance ($R_{\rm EXT}$) and channel length offset (ΔL) were 389 Ω-μm and -28 nm, respectively. The extracted gate offset coincides reasonably well with the estimated location of the metallurgical junction ($\sim$13.6 nm outside the gate as seen in the TEM image in the inset of Fig. 5). This offset is attributed to high parasitic resistance imposed by the unintentional "foot" of sidewall spacers created by nonoptimized gate and sidewall etching processes, as observed in the TEM image (inset of Fig. 1). Further improvement of short channel performance and drive current is expected by optimizing channel dopant profiles and gate/spacer etch processes.

V. Conclusion

Ge-B co-diffusion into Si substrates was used to fabricate elevated S/D PMOSFET devices. The new device structure enables the suppression of short-channel effects in bulk-Si PMOSFETs down to 80 nm gate lengths.

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