Strained p-Channel FinFETs With Extended Π-Shaped Silicon–Germanium Source and Drain Stressors

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***Abstract*—Further enhancement of performance in a strained p-channel multiple-gate or fin field-effect transistor (FinFET) device is demonstrated by utilizing an extended-Π-shaped SiGe source/drain (S/D) stressor compared to that utilizing only Π-shaped SiGe S/D. With the usage of a longer hydrofluoric acid cleaning time prior to the selective-epitaxy-raised S/D growth, a recess in the buried oxide is formed. This recess allows the subsequent SiGe growth on the fin sidewalls of the S/D regions to extend into the recessed buried oxide to provide a larger compressive stress in the channel for enhanced electrical performance compared to a device with SiGe S/D stressor. Process simulation shows that longitudinal compressive stress in the channel region is higher in a FinFET with extended-Π-SiGe S/D than that with Π-SiGe S/D. An enhancement of 26% in the drive current was experimentally observed, demonstrating further boost in enhancement of strained p-channel FinFET with little additional cost using this novel process.**

***Index Terms*—Extended-Π, FinFET, multiple gate, SiGe, source/drain stressors, strain, stress.**

I. Introduction

FIN field-effect transistors (FinFETs) or multiple-gate transistors are serious contenders for sub-32-nm technology due to excellent control of short-channel effects (SCEs). Strain engineering techniques such as raised source/drain (S/D) stressor [1]–[3], gate stressor [4]–[7], and high-stress silicon nitride (SiN) etch stop layer [8], [9] have been introduced to enhance the performance of FinFETs. Unlike the conventional planar transistor, a significant portion of the drain current is conducted along the fin sidewalls in FinFETs. Therefore, to realize a large performance enhancement in strained FinFETs, the strain that is induced on the fin sidewalls, including the portion near the base of the fin [as shown in Fig. 1(a)], must be large, particularly, for FinFETs with narrower fins. In particular, for p-channel FinFETs with silicon–germanium (SiGe) S/D stressors, the SiGe stressors should be grown on as much of the fin sidewalls in the S/D regions as possible, which can be hindered by the existence of SiN spacer stringer at the sides of the fin. Currently, there is little reported work on maximizing the lattice interaction between SiGe S/D and the 3-D topology of the Si fin by stressor extension and shape manipulation.

In this letter, we report a p-channel strained FinFET with a SiGe S/D that encapsulates the Si fin on all fin sidewall surfaces, forming a Pi-shaped SiGe stressor (Π-SiGe) [Fig. 1(b)]. Further structural improvement was also made to extend the SiGe S/D into the buried oxide below the bottom of the fin to form an *extended* Pi-shaped stressor (eΠ-SiGe) [Fig. 1(c)] for a larger strain effect, particularly, at the bottom of the fin channel. We report strain enhancement due to such structural optimization through both stress simulations and demonstration of enhanced driving current performance.

II. Device Fabrication

As performance enhancement of FinFETs with SiGe S/D over those with Si S/D has been demonstrated and is well established [1], [3], no control device with Si S/D was fabricated here. Eight-inch silicon-on-insulator substrates with 30-nm-thick Si were used for the fabrication of p-channel FinFETs with Π-SiGe and eΠ-SiGe S/D. After threshold voltage V_t adjust implant, 248-nm lithography with phase-shift mask, resist trimming, and reactive ion etching were used to define Si fins with fin widths W_{fin} down to 60 nm. The fin height is 30 nm. A SiO_2 gate dielectric ($\sim$3 nm) was then thermally grown, followed by poly-Si gate deposition, gate predoping, and SiO_2 hardmask formation. Gate definition was performed to achieve sub-70-nm gate lengths, followed by S/D extension implantation. In the spacer formation process, a SiO_2 liner was deposited, followed by silicon nitride (SiN). The SiN stringers at the base of the fins were removed using a prolonged spacer overetch. This allows epitaxial growth of SiGe on the entire fin sidewall.

A hydrofluoric acid (HF) clean removed the native oxide on the Si surface prior to selective epitaxy of SiGe S/D. For the FinFET with Π-SiGe S/D, an HF clean of 30 s was performed without significant recess in the buried oxide. For the FinFET with eΠ-SiGe S/D, an extended HF clean of 120 s was done to form a recess in the buried oxide, so that SiGe can be grown

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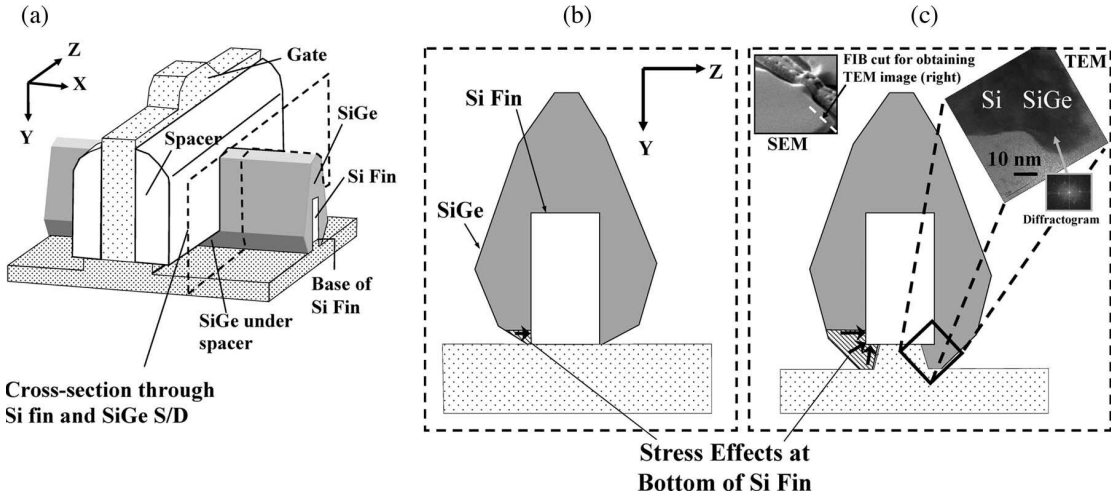

Fig. 1. (a) Three-dimensional schematic showing a FinFET with an extended Π-shaped SiGe S/D and a recessed buried oxide. The cross-sectional views (*not drawn to scale*) of the fin taken along the plane, as indicated in (a), are shown for two structural designs in the S/D regions: (b) Π-shaped SiGe S/D and (c) eΠ-shaped SiGe S/D. A scanning electron microscope image of the FinFET is shown in the left inset in (c), where a focused ion beam cut-line from which a TEM sample is extracted is also indicated. The TEM image [right inset in (c)] is taken at the edge of the S/D pad, and the diffractogram shows high-quality crystalline SiGe formed on the S/D regions.

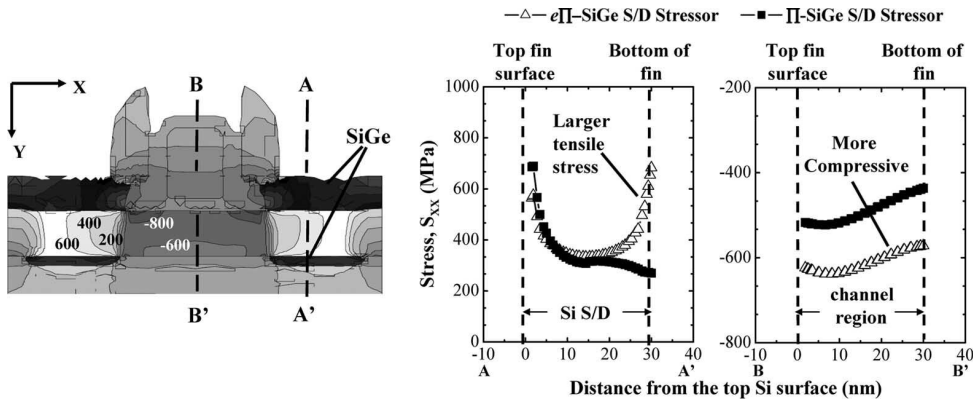

Fig. 2. (a) Two-dimensional distribution of the longitudinal stress S_{xx} (in megapascals) for FinFET with eΠ-SiGe S/D, showing a compressive stress in the channel that is induced by the tensile stress from the Si in the S/D region. (b) Profiles of S_{xx} that were taken along a vertical line A−A′ in the S/D region and along a vertical line B−B′ through the channel region are compared for FinFETs with Π-SiGe S/D and eΠ-SiGe S/D. The FinFET with eΠ-SiGe S/D has a higher magnitude of compressive stress in the channel region and a higher magnitude of tensile stress in the S/D region.

below the bottom of the Si fin in a subsequent epitaxy step. The etch rate of thermally grown SiO_2 is ∼10 nm/min using this HF bath. Selective epitaxy of $Si_{0.75}Ge_{0.25}$ was then performed. S/D formation, oxide passivation, and metallization were finally done. The S/D regions were not silicided.

III. Results and Discussion

Fig. 1(a) shows a schematic of a FinFET with SiGe grown on the entire Si fin sidewall surface in the S/D regions. The key differences between FinFET devices having a Π-SiGe S/D and an eΠ-SiGe S/D are highlighted in Fig. 1(b) and (c), where the cross sections are taken from a plane that cuts through the fin in the S/D region, as shown in Fig. 1(a). While the Π-SiGe stressor only encompasses the fin in the S/D region, the eΠ-SiGe stressor extends into the recessed buried oxide and perhaps even encroaching beneath or almost wrapping the Si fin. The stress at the bottom of the Si fin is affected by its lattice interaction with the SiGe in its vicinity, as shaded in Fig. 1(b) and (c). The portion of the eΠ-SiGe stressor that extends into the buried oxide can contribute to stronger lattice interaction and, therefore, additional stress at the bottom of the fin. Transmission electron microscope (TEM) image and diffractogram that were taken at the S/D region show the excellent crystallinity and the successful growth of the eΠ-SiGe stressor that extends into the buried oxide. It should be noted that, while slight encroachment of the eΠ-SiGe stressor beneath the fin may be desirable for high stress effects, very tight process control on the amount of lateral encroachment in the buried oxide recess etch will be required for narrow (e.g., sub-20 nm) and stand-alone fins (e.g., in static random access memory cells) for maintaining the stability of fin structure and minimizing device variability. The slightly larger cross-sectional profile of the eΠ-SiGe stressor as compared to that of the Π-SiGe stressor could also lead to a slightly lower series resistance.

Three-dimensional stress simulations were performed using the Taurus Process simulator for FinFETs with Π-SiGe and

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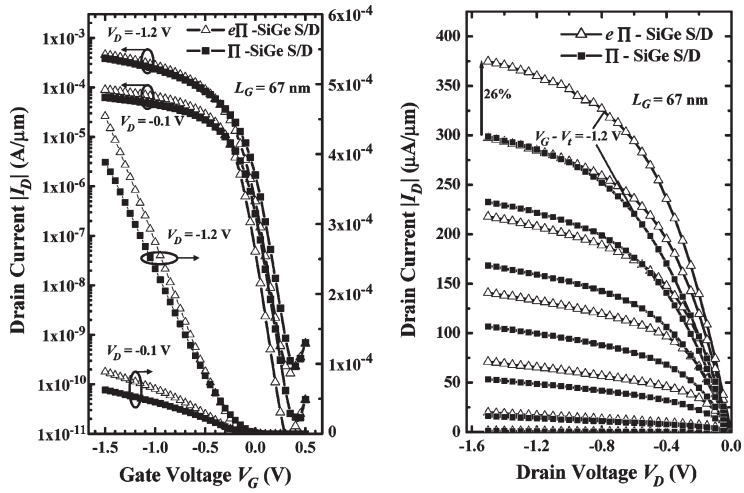

(a) (b)

Fig. 3. (a) I_D–V_G characteristics of FinFETs with a gate length L_G of 67 nm having a Π-shaped and eΠ-shaped SiGe S/D measured at a V_D of -0.1 and -1.2 V. (b) I_D–V_D characteristics are plotted for gate overdrives $(V_G - V_t)$ of 0 to -1.2 V in steps of -0.2 V. A 26% enhancement in the driving current was observed for the FinFET with eΠ-SiGe S/D over that with Π-SiGe S/D.

eΠ-SiGe S/D stressors. The FinFET with eΠ-SiGe S/D has a 6-nm recess in the buried oxide. The distribution of the longitudinal stress component S_{xx} (along the S/D direction) near the fin sidewall is shown in Fig. 2(a). The SiGe stressor, having a larger lattice constant, exerts a tensile stress in the Si in the S/D regions [Fig. 2(a)], which results in a compressive stress in the Si channel region for hole mobility enhancement. Fig. 2(b) shows the profile of the longitudinal stress S_{xx} taken vertically in the S/D region [along A–A′ in Fig. 2(a)] and in the channel region [along B–B′ in Fig. 2(a)]. The compressive stress in the channel of the FinFET with eΠ-SiGe S/D is indeed larger compared to that with Π-SiGe S/D. This is attributed to the higher tensile stress that is induced in the Si at the base of the S/D region (A–A′). Therefore, the device with eΠ-SiGe S/D is expected to show a higher driving current than that with Π-SiGe S/D. Generally, with reduction in fin width and gate length, we expect the average stress levels in the fin to be higher for FinFETs with Π-SiGe S/D or eΠ-SiGe S/D stressors. In order not to compromise fin stability issues due to a buried oxide undercut (for an extremely small fin width), a vertical recess etch (without lateral encroachment) may be adopted. From process simulation results, when the lateral encroachment of the recess etch beneath the fin is 0 and 6 nm, the fin stress is 17% and 30% higher than that in a device with Π-SiGe stressor, respectively.

The electrical characteristics of the fabricated FinFETs with Π-SiGe and eΠ-SiGe stressors were measured and compared in Fig. 3. The I_D–V_G plot is shown in Fig. 3(a). Comparable subthreshold swing (SS) and drain-induced barrier lowering (DIBL) values are obtained, which indicates that the longer preepitaxy HF cleaning process that was employed for the FinFET device with eΠ-SiGe S/D does not degrade its control of SCEs. The V_t for the FinFET with eΠ-SiGe S/D is slightly higher, and the SS is slightly smaller, possibly due to less boron diffusion from the S/D during S/D anneal, as the SiGe grown beneath the spacer [labeled in Fig. 1(a)] may retain some of these dopants. Furthermore, the gate leakage current (not shown) of these two devices are comparable (0.01–0.02 A/cm^2) at a gate voltage V_G of -1 V. Device parameters are summarized in Table I. The FinFET with eΠ-SiGe S/D demonstrates 26% higher saturation driving current than the FinFET with Π-SiGe S/D [Fig. 3(b)]. Superior electrical characteristics are demonstrated by the FinFET with eΠ-SiGe S/D. Fig. 4 plots the transconductance against V_G for both types of devices. The

TABLE I
COMPARISON OF DEVICE PARAMETERS FOR FinFET DEVICES WITH eΠ-SiGe AND Π-SiGe S/D, INCLUDING THRESHOLD VOLTAGE V_t, DIBL, AND SS

FinFET with	V_t (V) obtained at ($I_D = 1\times10^{-6}$ (A/μm), V_D = -1.2 V)	DIBL (V/V)	SS (mv/decade)
eΠ-SiGe S/D	-0.032	0.08	81
Π-SiGe S/D	0.027	0.08	84

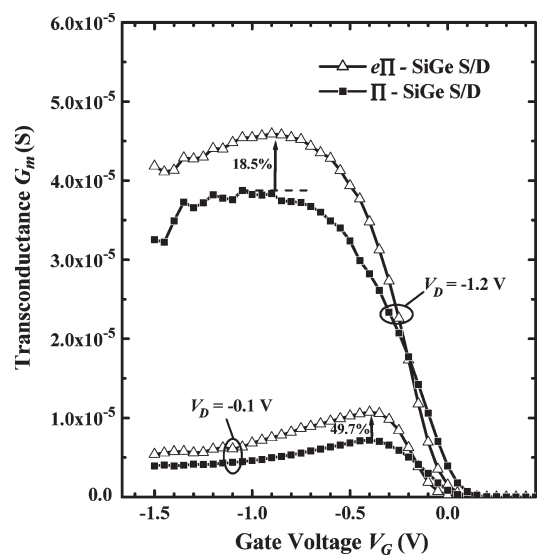

Fig. 4. FinFET with eΠ-SiGe S/D stressors shows a higher maximum transconductance G_m than the FinFET with Π-SiGe S/D stressors at $V_D = -0.1$ V, which is an indication of higher hole mobility. The peak transconductance at $V_D = -1.2$ V is also higher for the FinFET with eΠ-SiGe S/D.

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peak linear transconductance for the FinFET with $e\Pi$-SiGe S/D is much higher compared to that for the FinFET with Π-SiGe S/D, indicating a higher hole mobility enhancement due to the larger induced stress.

IV. Conclusion

A strained p-channel FinFET with the Si fin encapsulated by SiGe in the S/D regions to form a Π-shaped SiGe S/D stressor was realized. By employing a longer pre-epitaxy HF clean, a FinFET with extended Π-shaped SiGe S/D ($e\Pi$-SiGe S/D) was formed. Simulation shows that the $e\Pi$-SiGe S/D stressor gives a higher longitudinal compressive stress in the channel region, as compared to the Π-shaped SiGe S/D stressor. Experimentally, a FinFET with $e\Pi$-SiGe S/D shows 26% higher driving current than that with Π-SiGe S/D. This approach can be further improved by fully surrounding a Si fin with SiGe S/D stressor for even higher strain effects and better electrical performance.

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