

Stress Enhanced Performance Analysis for Trigate FinFETs at 7nm Node

J. Jena^{1a*}, T. P. Dash^{2a}, S. Das^{3b}, E. Mohapatra^{4a}, and C. K. Maiti^{5a}

^aDepartment of Electronics and Communication Engineering,

Siksha O' Anusandhan (Deemed to be University), Bhubaneswar, Odisha, India-751030

^bDepartment of ECE, Silicon Institute of Technology, Bhubaneswar, Odisha, India-751024

^{1a}jhansiranijena@soa.ac.in; ²tpdiitkgp@gmail.com; ³sanghamitra.das@silicon.ac.in;

⁴eleenamohapatra@gmail.com; ⁵ckmaiti@outlook.com.

Abstract — Short channel effect becomes a serious concern below 22nm technology node. This can be overcome by multi-gate devices such as double gate (DG), trigate (TG). Trigate FinFET structures have shown great potential for both digital and analog applications. In this work, we have simulated a realistic PMOS bulk-Si FinFET with epi-SiGe as a source/drain (S/D) stressor at a 7nm technology node. The strain enhancement mechanisms have been used in the diamond-shaped bridges patterned on SiGe S/D stressor. The stress in the channel due to epitaxial S/D stressor has been calculated using the stress history model and the theory of elasticity. A 30% improvement of the 'on current' in the channel as compared to the device without stress is demonstrated.

Keywords— SiGe S/D, Stressor, TCAD, FinFET, Fabrication process.

I. INTRODUCTION

The semiconductor industry has been consistently improving with fulfilling challenging demands over the time since 1960. With rapid shrinking in transistor size and high demand of integration for integrated circuits (ICs), short channel effect (SCE) becomes predominant. It becomes severe over the downscaling of technology nodes. To overcome such challenges, the planar architecture (planar MOSFETs) has to be replaced by multi-gate or non-planar architecture. Trigate FinFET are quite promising devices in order to reduce SCE [1, 2]. The two most important FinFET structures are the tri-gate and double-gate SOI MOSFETs. The tri-gate FinFET has the advantage of less parasitic capacitance and larger magnitude of on-current.

Several studies have reported the various aspects of FinFETs, such as scaling effects, reliability, variability, and implementation in integrated circuits, memory circuits, etc. But the implementation of local or global strain on FinFET to achieve higher performance has not been explored except in a few reports [1-4]. As process-induced strain effects have become significant with the shrinking of dimensions, it is desirable to adopt such techniques in FinFET like non-planar devices.

Strain technology is one the promising technology in order to boost up the device performance since 90nm technology node for planar devices. The implementation of this technology for non-planar structures is always challenging and mostly process dependent [2]. The SiGe source/drain

stressor technique has emerged to be a consistent performance booster for advanced devices below 14nm technology node. Recently experimental measurements on strain mapping in FinFETs have been reported by several researchers. At this nanoscale regime, the omnipresent residual stress is now becoming an important source of variability in advanced VLSI technologies that influence circuit performance [2]. The mechanical stress simulations have been studied using Technology CAD (TCAD) tools [5-7]. Tan et al. [8-9] reported a strained p-FinFET with a SiGe S/D.

The epitaxy of the SiGe layer (SiGe-epi) is known to generate a lattice mismatch stress at the silicon interface since Si1-xGex alloy has a larger lattice constant. As the Ge mole fraction increases, the Si1-xGex lattice constant increases further, thus increasing the strain in the SiGe lattice. So the tensile stress on the S/D and longitudinal compressive stress on the channel increases. It leads to an improvement in the overall electrical performance of the devices [10-11].

In this work, an appropriate 3D TCAD modeling approach is proposed for the specific FinFET design and virtual fabrication processes. The process simulation for FinFET with epitaxially grown source/drain has been discussed for an extremely scaled range at the 7nm technology node. Here, the stress profile is analyzed by simulating the epitaxial growth process of SiGe Si channel p-type FinFETs with SiGe epitaxial stressor. Compressive stress is observed in the channel through the SiGe-epi stressor [12, 13]. In the simulation, the theory of linear elasticity is implemented to describe the stress evolutions at the various process steps. We have studied the effect of mechanical stress on the electrical behavior that shows better improvement in the FinFET device performance at the 7nm technology node (7N). The process simulation for FinFET with epitaxially grown source/drain has been discussed for an extremely scaled range that is at the 7nm technology node. This observation will undoubtedly show a path for the optimized design (for tuning) of FinFETs at 7nm and below utilizing the mechanical stress in the channel.

The paper is organized as follows: In Section II, the several critical steps of virtual fabrication simulations are discussed. Strain mapping is discussed in the section III. Simulation environment is discussed in the section IV. Corresponding simulation results is shown in the section V. Device key performance parameters are analyzed such as Vth,

Ion, SS and Ioff. Finally, the conclusions are drawn in Section VI.

II. PROCESS SIMULATION

A Performed process steps play a vital role in determining device characteristics [14]. The process steps of bulk FinFET are quite different than planar MOSFETs. Though FinFET process steps are already implemented by many semiconductor manufacturing companies and research groups [15-16], the optimized fabrication steps are still going on due to unavailability in the public domain. Hence we have tried TCAD simulations for tri-gate FinFETs involving several important process steps. The steps are described briefly and optimized in consideration with 2D and 3D geometry. The basic processes for the p-channel FinFET are:

- Si Substrate
- Strain-Relaxed Buffer (SRB) Growth (virtual substrate).
- Fin Formation.
- SiO₂ deposition
- Poly-gate deposition and Reactive Ion Etching (RIE).
- Equal Spacer Formation.
- S/D-epi with SiGe.
- High-K gate material (HKMG) Formation and recess.
- Self-aligned contact (SAC) Formation.

A. Fin formation

Initially, the silicon substrate layer is grown on the Si wafer. Dry etching step with geometrical models is carried out to transfer the masks into the structure. A 35nm deep etching process at an angle of 870 is used to transfer the mask pattern into the silicon substrate optimally. It forms the tapered strain-relaxed buffer (SRB) layer with a base width of 10nm and a top width of 7nm. Oxidation followed by etching steps is adopted to prepare the substrate for fin formation and trench isolation with the help of a suitable mask. The resulted fin height is 20nm, and the fin width is 7nm, as shown in Figure 1(a-c). Fin is doped with a boron implant with a doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$ to form a p-channel device, which is also a vital part of setting the threshold voltage of the device.

B. Poly gate deposition and spacer Formation

Once the fin is formed, it can be covered with SiO₂. After patterning of SiO₂, polysilicon gate material selective etched to create the gate area. The polysilicon is deposited and etched away with a suitable mask to cover the gate area. The nitride layer is deposited and etched to form the spacer layer on both sides of poly. The poly and nitride layer deposition steps are shown in Figure 1(d, e).

C. Source-Drain Epitaxy

One of the critical processes in the semiconductor industry is epitaxy. We have simulated conformal epitaxial growth over 3D structures using selective deposition. Normally, the deposit statement is used to deposit material with a given rate and ratio over all exposed surfaces. For selective deposition,

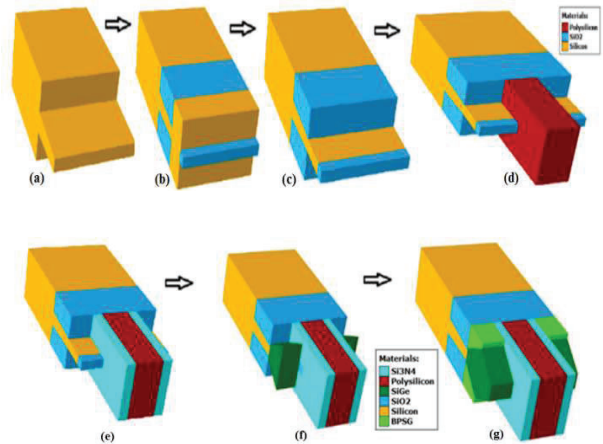
Si is considered as the base material over which we want to deposit SiGe. Then, we have invoked the deposition after stating the simulator SiGe as epi material for deposition. The epi growth is controlled with an initial epi angle of 120° up to vertical 21nm height and then 60° from the mid of the epi with a thickness of 21nm. The source and drain doping values are $1 \times 10^{20} \text{ cm}^{-3}$. The lower side of the SiGe epi layer is surrounded by insulating material Borophosphoro silicate glass (BPSG). The simulated epitaxial growth of SiGe on top of silicon is shown in Figure 1(f-h).

D. HKMG Formation and Contacts

After the formation of the SiGe epi layer, gate oxide has to be deposited. HfO₂ is introduced as a high-k material at 7nm node in such a way that it can reduce threshold voltage (V_{th}) dependency on gate length (L_g) as high-k is separated from the self-aligned contact cap and fully encapsulated by metal, which prevents OH diffusion into the HfO₂. In our simulation, initially, 0.8nm thick SiO₂ is deposited, followed by HfO₂, which has been used as the high-k gate material. The thickness of the HfO₂ is 0.16nm. The effective gate oxide thickness is maintained at ~1nm. Finally, contacts are made for source, drain, and gate with Al. The detailed steps are shown in Figure 1(i-k). The final structure has been shown in Figure 1(k). Table-I shows the key device parameters of the FinFET. The front and cross-sectional views have been compared with the reported device by Auth et al. [2].

TABLE I. GEOMETRICAL DETAILS OF THE VIRTUALLY FABRICATED DEVICE SHOWN IN FIGURE 1(K).

Geometrical Key Parameters	Value
Gate length(L_g)	14 nm
Fin Height	20nm
Fin Width	7nm
Source/Drain (S/D) Doping	$1 \times 10^{20} \text{ cm}^{-3}$
Substrate Doping	$1 \times 10^{15} \text{ cm}^{-3}$
Gate oxide thickness	1 nm



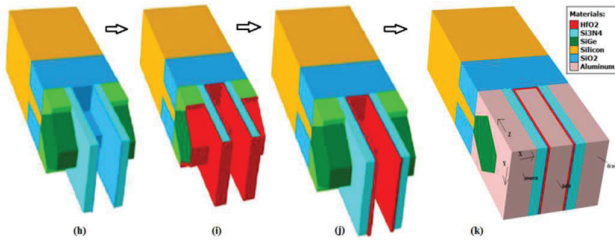


Figure 1. (a) Fin formation and (b) Trench isolation with SiO₂, (c) Active area formation, (d) Formation of polysilicon layer, (e) Nitride spacer formation, (f) Formation of SiGe epitaxial layer (SiGe growth with initial 1200 angle), (g) Diamond shape S/D Stressor after epitaxial layer growth, (h) Formation of the gate oxide, (i) HfO₂ deposition, (j) Etching of HfO₂ and (k) Full Device after metal contact.

A reported FinFET structure is used for calibration of the TCAD simulation, which motivates this study. Here we have simulated the tri-gate p-FinFET using the TCAD tool following the TEM image reported by Auth et al. [2]. The Nanoscale device performance has been analyzed using different models such as Lombardi (CVT), Shockley-Read-Hall (SRH), and Auger models, etc. The structure is shown in Figure 2, which is the simulated device obtained from the Victory Device tool with an optimized process step.

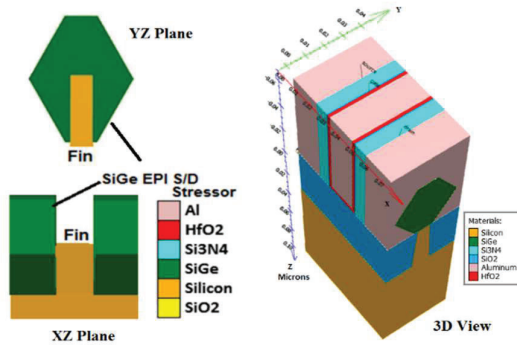


Figure 2. 2D and 3D view of simulated FinFET structure. YZ and XZ planes show the cross-sectional view of S/D epi with SiGe as a stressor.

III. STRAIN MAPPING

The stress impact is analyzed at 50% of Ge in the SiGe S/D-epi by the tool Victory Stress. It shows the stress profile in the various fin regions. The slight mismatch of lattice constant between Si and Si_{1-x}Ge_x, generates uniaxial compressive stress in the longitudinal direction that increases the carrier mobility [17]. Figure 3 shows both the 2D and 1D stress distribution profile along with the XZ and YZ planes of the fin region. Here we observed a maximum negative compressive stress of the XZ plane in the fin region of about 6×10^9 dyne/cm².

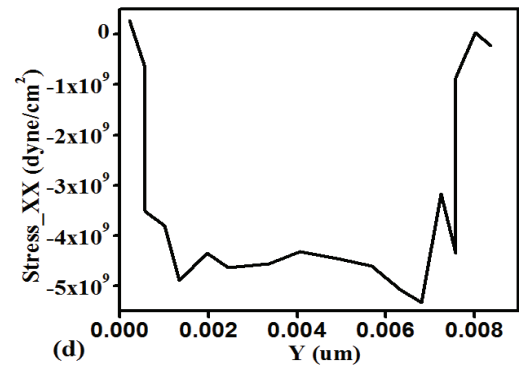
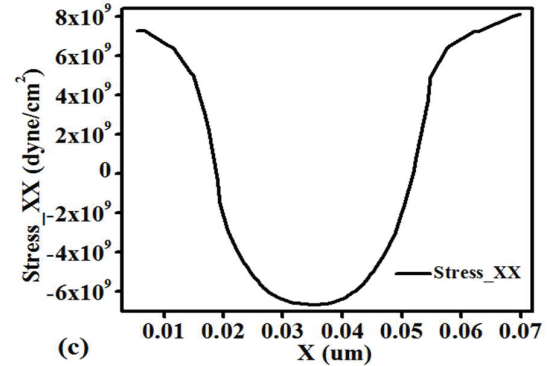
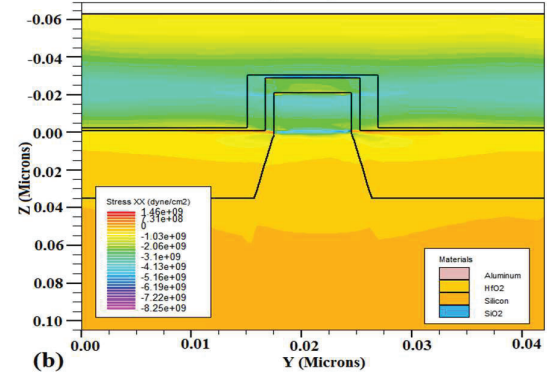
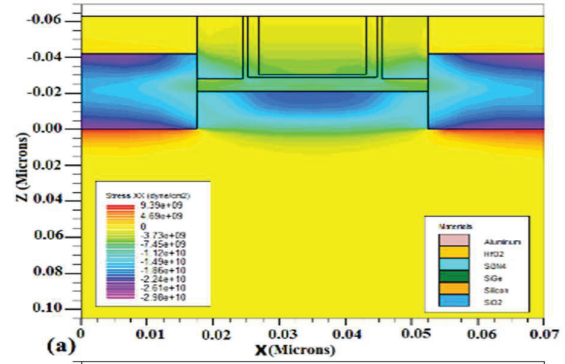


Figure 3. (a) and (b) show the 2-dimensional (2D) cut plane of the stress distribution map along XZ and YZ regions, respectively. Figures (c) and (d) show the corresponding stress profile of (a) and (b).

IV. SIMULATION ENVIRONMENT

The mechanical stress effect is modeled with the elasticity theory by relating strain with stress. Hook has been developed this phenomenon under a particular condition where stress and strain tensor deformation takes place linearly in the elastic solids. It is expressed as

$$\sigma_{ij} = C_{ijkl} \epsilon_{kl} \quad (1)$$

Where σ_{ij} , ϵ_{kl} and C_{ijkl} represent stress tensor, strain tensor, and elastic stiffness of 4th order of 81 components, respectively. At the equilibrium, under the symmetries considerations, C_{ijkl} is limited to 36 tensor components for both the tensors.

The diagonal (off) strain components are equal to one and half of the shear strain. So for simplicity, the converted diagonal (off) components into shear strains can be used as vectors in the following notations:

$$\begin{bmatrix} \epsilon_{xx} & 2\epsilon_{xy} & 2\epsilon_{xz} \\ 2\epsilon_{yx} & \epsilon_{yy} & 2\epsilon_{yz} \\ 2\epsilon_{zx} & 2\epsilon_{zy} & \epsilon_{zz} \end{bmatrix} = \begin{bmatrix} \epsilon_{xx} & \gamma_{xy} & \gamma_{xz} \\ \gamma_{yx} & \epsilon_{yy} & \gamma_{yz} \\ \gamma_{zx} & \gamma_{zy} & \epsilon_{zz} \end{bmatrix} \quad (2)$$

Where in the mechanical engineering, γ , Y , and ν represent the shear strain, Young's modulus and Poisson ratio (for isotropic material and the homogeneous) to relate strain. For the simulation of the Si and Ge material, these compliance coefficients (C_{ij}) are considered.

Mostly the Piezoresistive approach is used as it has provided the mobility relationship at unstrained and strained conditions. The mobility of the carrier is given by [18-19]

$$\Delta\mu_{ij} = \frac{\mu_{ij}}{\mu_0} \approx \sum_{k=1}^3 \sum_{l=1}^3 \Pi_{ijkl} \sigma_{kl} \quad (3)$$

where σ_{kl} represents the component of the stress tensor. Π_{ijkl} represents the first-order component of the hole/electron piezoconductance tensor. For symmetric, the mobility of the isotropic no-strained cubic crystal has obtained from the above equation (3) as:

$$\Delta\mu_{ij} = \frac{\mu_{ij}}{\mu_0} \approx \sum_{k=1}^3 \Pi_{jk} \sigma_k \quad (4)$$

The piezoconductance components are related to piezoresistance tensors. The carrier mobility depends upon the drift velocity corresponds to the average mobility of the carriers.

In figure 4, the hole concentration and mobility distribution profiles are shown in the XZ plane of the channel region. The maximum carrier mobility is about 140 cm²/V-Sec because of the low carrier concentration in the middle of the channel. The electric field profile has also been analyzed in figure 5 along the channel axis to realize the behavior of the carrier conduction between the channel and S/D region

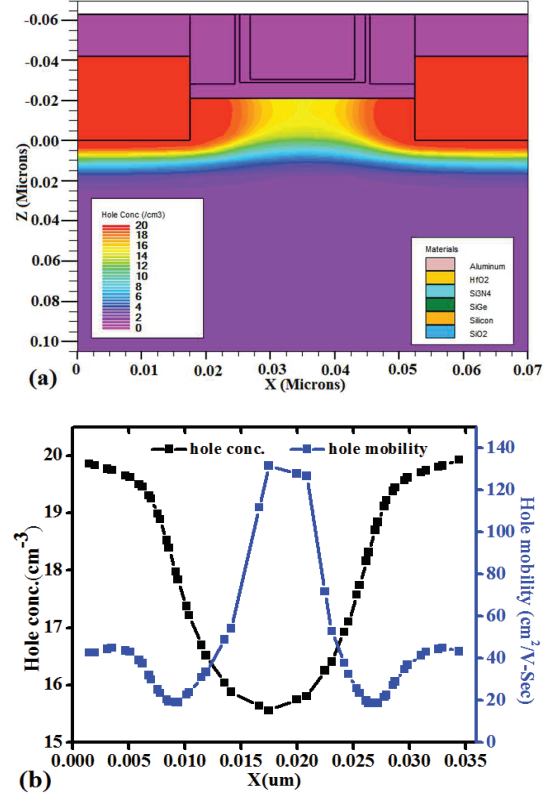
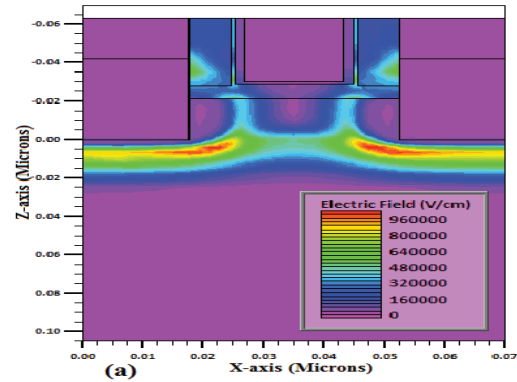


Figure 4. (a) and (b) show the 2D and 1D cut planes of hole concentration and mobility profile distribution in the XZ plane of the fin regions, respectively.

Figure 5 shows the 2D cut plane of the electric field profile distribution along with the XZ and YZ plane of the channel region. It is observed that the high electric field is induced at both of the junctions of the S/D region. It characterizes the current density profile of the device.



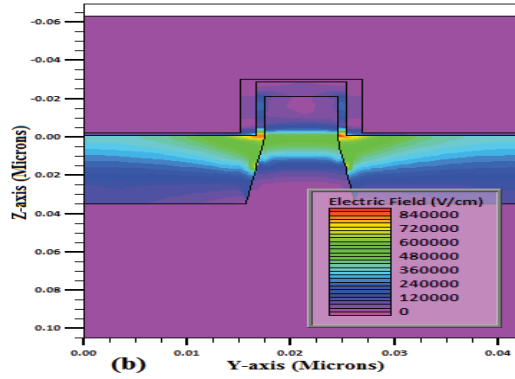


Figure 5. (a) and (b) show the 2D cut plane of the electric field distribution profile along with the XZ and YZ plane of the channel regions, respectively.

V. RESULT AND DISCUSSION

The simulations must have constant currents consistent. The Density Gradient (DG) transport model has been used, which is resulting from the method of moments of the carriers in the Wigner equations. The electrical characteristics such as I_d - V_g , transconductance, and I_d - V_d have been shown in Figure 6 (a), (b), and (c), respectively. The subthreshold conduction parameters are extracted and listed in Table II using different transport models.

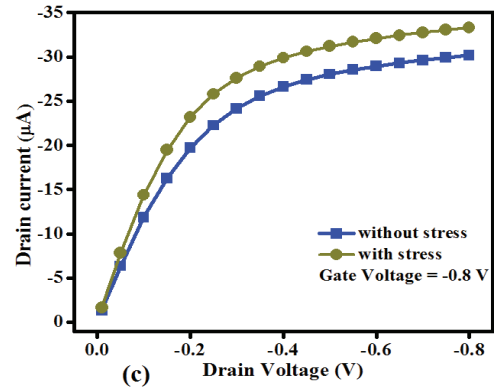
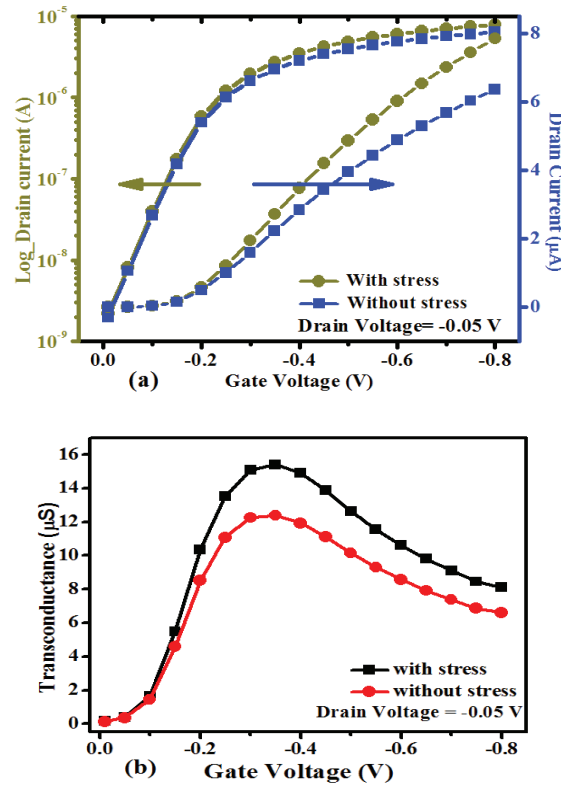


Figure 6. (a) transfer characteristics, (b) transconductance, and (c) output drain current characteristics of the device at stress and no-stress condition. Table-II shows the critical device parameters obtained for the 'No strain' and 'strain enhanced' 7nm p-channels FinFET. Optimum results have been observed at stress condition comparatively.

TABLE II. THE EXTRACTED DEVICE PARAMETERS.

Device	No stress	With stress
V_{th} (mV)	147.31	149.90
Beta (10^{-4})	2.51	3.10
Theta	0.439	0.438
SS (mV/dec)	70.80	70.41
I_{on} (μA)	6.36	7.85
I_{off} (nA)	2.01	2.20

VI. CONCLUSIONS

TCAD simulations of a tri-gate FinFET have been carried out using the necessary virtual fabrication process steps in silicon CMOS technology. The epitaxial S/D stressor technique has been implemented in a p-type FinFET at 7N node. The linear elasticity theory is used to evaluate the stress-induced in process simulation stages. The stress maps across the channel in different 2D planes have been studied. The stress-xx distribution along XZ and YZ regions is analyzed and found maximum in the XZ plane. The improvement of 'on current' is ~30% in the case of strained devices compared to devices without stress. The critical device parameters such as V_{th} , SS, and I_{off} are also extracted for both devices.

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