

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner

v.

Daedalus Prime LLC,

Patent Owner

Patent No. 10,700,178 B2

Filing Date: May 20, 2019

Issue Date: June 30, 2020

Title: CONTACT RESISTANCE REDUCTION EMPLOYING
GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Inter Partes Review No. IPR2023-01120

PETITION FOR *INTER PARTES* REVIEW

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TABLE OF EXHIBITS

Exhibit	Description of Exhibit
1001	U.S. Patent No. 10,700,178 to Glass et al. (“’178 Patent”).
1002	Declaration of Dr. Scott E. Thompson, Ph.D. (“Thompson”).
1003	U.S. Patent Appl. Pub. No. 2008/0121932 A1 to Ranade (“ <i>Ranade</i> ”).
1004	U.S. Patent Appl. Pub. No. 2010/0123198 A1 to Kim et al. (“ <i>Kim</i> ”).
1005	U.S. Patent No. 7,611,943 to Liu (“ <i>Liu</i> ”).
1006	U.S. Patent Appl. Pub. No. 2010/0276761 A1 to Tung et al. (“ <i>Tung</i> ”).
1007	U.S. Patent No. 7,361,958 to Brask et al. (“ <i>Brask</i> ”).
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1027	U.S. Patent Appl. Pub. No. 2008/0067545 A1 to Rhee et al.
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1029	E.D. Marshall et al., <i>Metal-Germanium Contacts and Germanide Formation</i> , Materials Research Society Symposia Proceedings, vol. 47: Symposium C – Thin Films: The Relationship of Structure to Properties, pp. 161-166 (1985).
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1037	S. Gannavaram et al., <i>Low Temperature ($\leq 800^{\circ}\text{C}$) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for Sub-70 nm CMOS</i> , Technical Digest of the 2000 International Electron Devices Meeting (IEDM), pp. 437-40 (2000).
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1039	R. Wittman, <i>Miniaturization Problems in CMOS Technology: Investigation of Doping Profiles and Reliability</i> , Doctoral Dissertation, Wien University Austria (Jan. 2007) (excerpted).
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1044	Prosecution File History, U.S. Patent No. 10,700,178 (“File History”).
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1058	P. Bai et al., <i>A 65nm Logic Technology Featuring 35 nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell</i> , Technical Digest of the 2004 International Electron Devices Meeting (IEDM), pp. 657-660 (2004).
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1062	U.S. Patent No. 8,362,575 to Kwok et al.
1063	U.S. Patent Appl. Pub. No. 2007/0123042 A1 to Rim et al.

CLAIM LISTING

Element	Claim Language
[1.0]	An integrated circuit structure, comprising:
[1.1]	a fin comprising silicon;
[1.2]	a gate electrode over the fin;
[1.3]	a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface,
[1.4]	wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[1.5]	a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[1.6]	a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface,
[1.7]	wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and
[1.8]	a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

Element	Claim Language
2	The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than 1E20.
3	The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.
4	The integrated circuit structure of claim 1, wherein the fin comprises a strained channel between the first and second source or drain regions.
5	The integrated circuit structure of claim 1, wherein the first and second source or drain regions are P-type.
[6.0]	An integrated circuit structure, comprising:
[6.1]	a body comprising silicon;
[6.2]	a gate electrode over the body;
[6.3]	a first source or drain region in the body proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface,
[6.4]	wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[6.5]	a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

Element	Claim Language
[6.6]	a second source or drain region in the body proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface,
[6.7]	wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and
[6.8]	a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.
7	The integrated circuit structure of claim 6, wherein the first and second source or drain regions have a boron concentration greater than 1E20.
8	The integrated circuit structure of claim 6, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.
9	The integrated circuit structure of claim 6, wherein the body comprises a strained channel between the first and second source or drain regions.
10	The integrated circuit structure of claim 6, wherein the first and second source or drain regions are P-type.
[11.0]	A computing device, comprising:
[11.1]	a board; and

Element	Claim Language
[11.2]	a component coupled to the board, the component including an integrated circuit structure, comprising:
[11.3]	a fin comprising silicon;
[11.4]	a gate electrode over the fin;
[11.5]	a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface,
[11.6]	wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[11.7]	a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[11.8]	a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface,
[11.9]	wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and
[11.10]	a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

Element	Claim Language
12	The computing device of claim 11, further comprising: a memory coupled to the board.
13	The computing device of claim 11, further comprising: a communication chip coupled to the board.
14	The computing device of claim 11, further comprising: a camera coupled to the board.
15	The computing device of claim 11, further comprising: a global positioning system coupled to the board.
16	The computing device of claim 11, further comprising: a battery coupled to the board.
17	The computing device of claim 11, further comprising: an antenna coupled to the board.
18	The computing device of claim 11, wherein the component is a packaged integrated circuit die.
19	The computing device of claim 11, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.
20	The computing device of claim 11, wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box.

I. INTRODUCTION

Titled “Contact Resistance Reduction Employing Germanium Overlayer Pre-Contact Metalization,” the ’178 Patent¹ describes field-effect transistors (“FETs”) with a germanium layer over their source/drain regions to lower contact resistance—an approach others had taught. This Petition, supported by Dr. Scott Thompson’s declaration, requests *inter partes* review of challenged claims 1-20 and demonstrates their unpatentability.

II. RELIEF REQUESTED

Petitioner requests *inter partes* review on the following grounds:

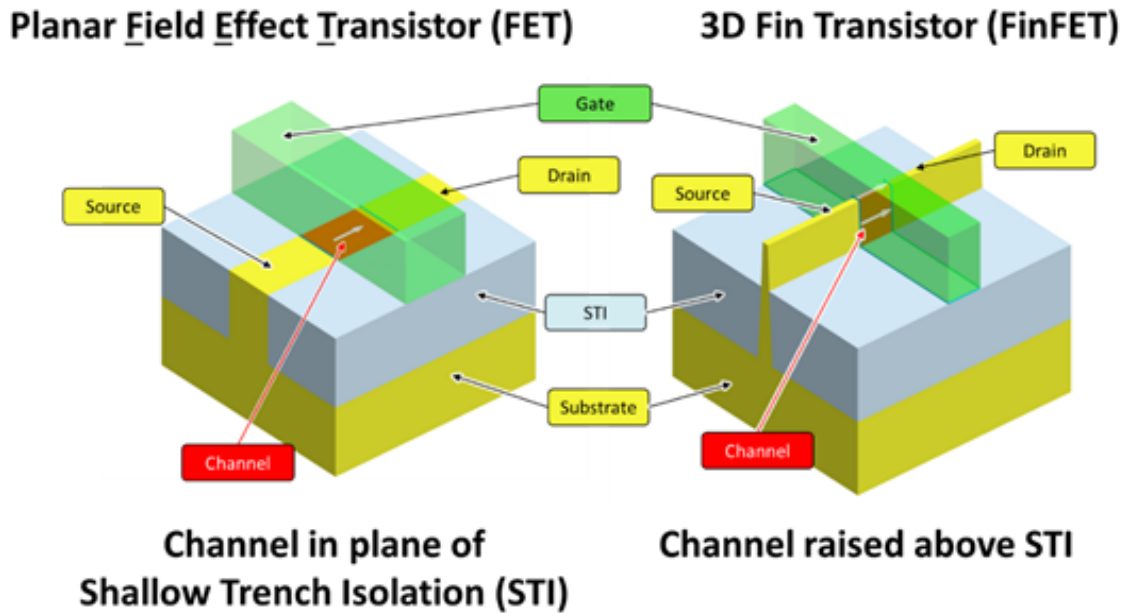
Ground	References	Basis	Claims
1A	<i>Ranade, Kim</i>	§103	1-20
1B	<i>Ranade, Kim, Liu</i>	§103	11-20
2A	<i>Tung, Brask</i>	§103	1-20
2B	<i>Tung, Brask, Liu</i>	§103	11-20

III. STATE OF THE ART

A. Planar and Non-Planar FETs

A FET is a switch operated by voltage applied to a “gate” between “source” and “drain” regions. Thompson ¶51. When turned on, current flows between the source/drain regions through a “channel” under the gate. *Id.* The figures below illustrate two types of FETs: a planar FET and a non-planar “FinFET.” *Id.* ¶50.

¹ U.S. Patent No. 10,700,178 (EX1001).

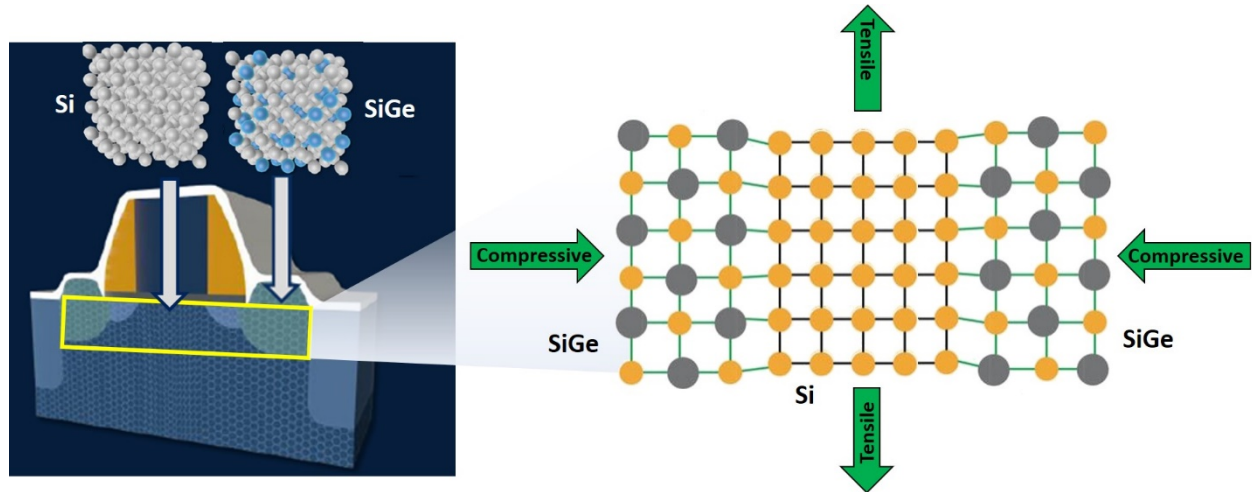


The operation of both is the same, as is the underlying physics. *Id.* ¶51. And except for forming the fin shape in the latter, their fabrication is the same. *Id.* ¶52; *see also* EX1008 at 1; EX1009 at Abstract, 2:11-14, 5:37-40; EX1010 at 1.

B. SiGe/Strained Silicon Technology

Integrated circuits include p-type FETs (“pFETs”), where positive charges generate a “1” logic, and n-type FETs (“nFETs”), where negative charges generate a “0” logic. Thompson ¶¶55-56. PFETs were once much slower than nFETs. *Id.* ¶¶54-58. What Dr. Thompson calls SiGe/Strained Si technology changed this. *See id.* Because Ge atoms are larger than Si atoms, using silicon-germanium (“Si_xGe_{1-x}” or “SiGe”) source/drain regions strains the Si channel region (illustrated below), which improves pFET charge carrier mobility and thus

operating speed. *Id.* ¶¶57-60; *see also* EX1011 at 9; EX1012 ¶0007. By 2004, SiGe source/drain regions had doubled pFET speeds. Thompson ¶¶56-58.



SiGe/Strained Si technology was well-known by December 2010. *See* '178 Patent at 4:58-65. Four generations of high-volume commercial devices already used it. Thompson ¶¶64-65. And because smaller transistors experience less strain at a given Ge concentration, Ge concentration increased as transistors shrank. *Id.* ¶61. The industry knew further scaling required even “higher germanium concentrations in the S/D area.” EX1013 at 5; *see also* EX1014 at 7.

To continue this trend and add strain while increasing Ge concentration, a person of ordinary skill in the art (“POSITA”) would have appreciated the need to minimize dislocations in the SiGe source/drain regions. Thompson ¶62; *see also* Ranade ¶0040; EX1015 at 3:30-44, 3:60-64, 4:2-8, 4:28-60; EX1012 ¶¶0030-0032; EX1016 at 2:10-22. And a POSITA would have known to achieve this by grading the Ge concentration. Thompson ¶¶62-63; *see also* EX1017 at 1:56-64; EX1018 at

Title, Abstract, ¶¶0001, ¶0044, ¶¶0053-0058, Figs. 14, 15; EX1012 ¶¶0008, ¶0032, ¶0042; EX1019 ¶¶0083-0095; *Ranade* ¶0040; EX1020 at 2-3, Figs. 1-4, 6, 7; EX1015 at Abstract, 4:38-5:19, 7:61-8:31; EX1016 at 2:10-22, 5:56-6:6, 6:38-7:11, Fig. 5b; EX1021 ¶¶0059-0060.

C. Schottky Barrier Engineering

An electrode contacts source/drain regions to pass electricity. Thompson ¶¶68. The electrical resistance at the interface between the electrode and underlying semiconductor is called contact resistance. *Id.* A POSITA would have sought lower contact resistance to avoid slower switching speeds and increased power consumption and heating. *Id.* ¶¶66.

The equation governing contact resistance dictates that lowering the so-called the “Schottky” energy barrier reduces contact resistance—something the ’178 Patent itself acknowledges. *Id.* ¶¶68-73; *see also* ’178 Patent at 4:3-9, 12:7-12, 14:30-46; EX1022 at 10-12; EX1023 at 7. A POSITA would have known this. *See* EX1024 at 8:34-9:63, Figs. 5-8; EX1019 ¶¶0039-0045, ¶0086; EX1011 at 3-4, 6-7.

Since the 1980s, long before SiGe/Strained Si technology, the industry used metal-silicon compounds called “silicides” to lower the Schottky barrier height for silicon source/drain regions. Thompson ¶¶87-90. Silicides are formed by metalizing a Si layer—depositing a metal layer (e.g., Ti, Co, Ni) on a layer of Si

and applying enough heat for the Si and metal atoms to bond. *Id.* ¶89. The textbook figure below shows a “Titanium silicide contact.” *Id.* ¶¶88-89; *see also* EX1025 at 20-21, 41-45, Figs. 9.19-9.22, 12.9, 12.14.

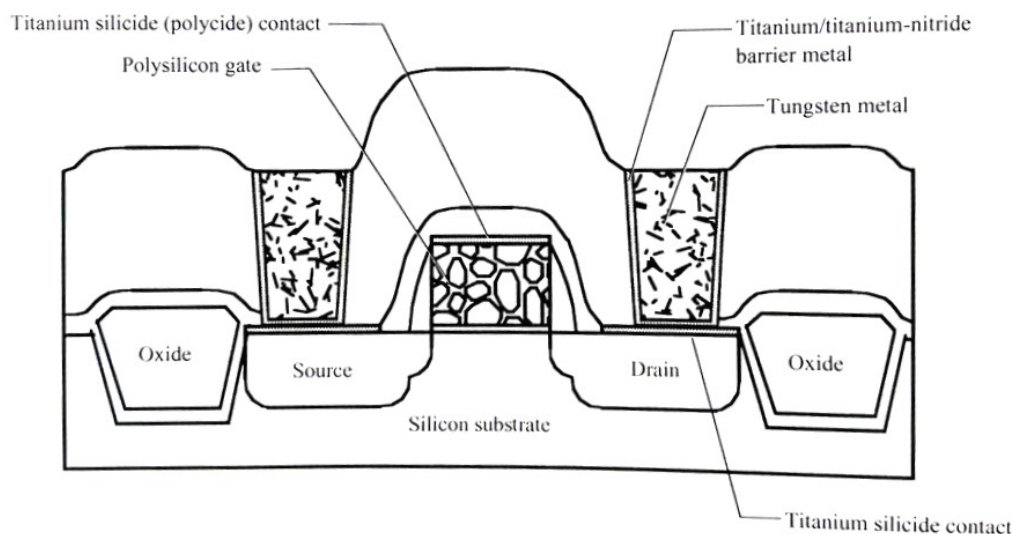
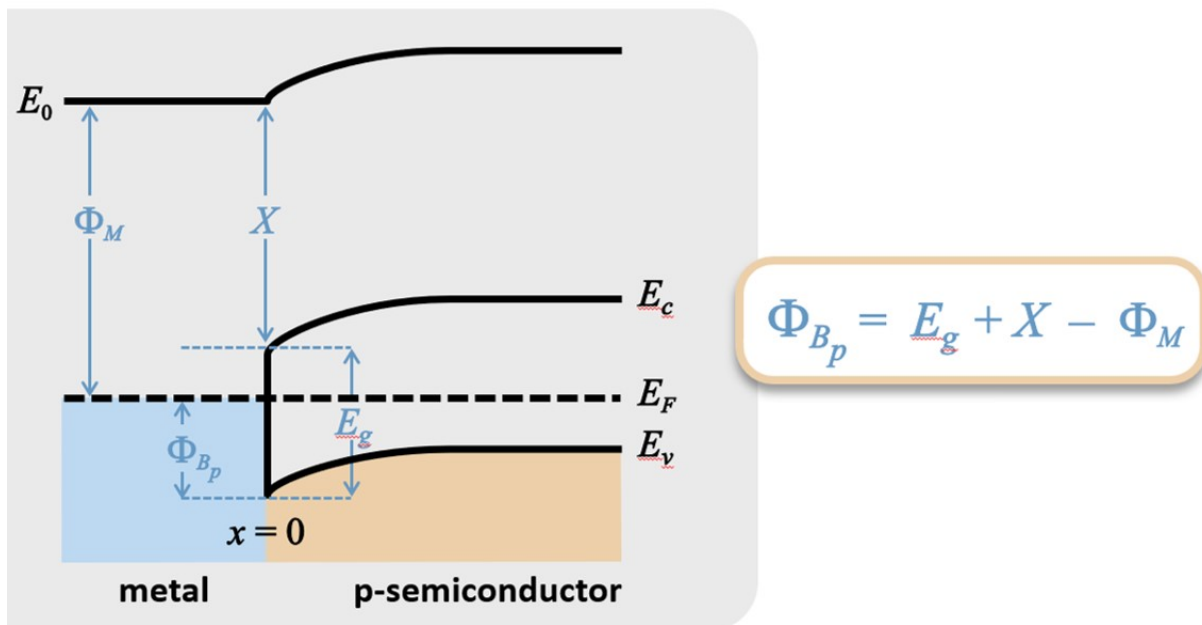


FIGURE 12.9 Refractory Metal Silicide at a Silicon Contact

EX1025, Fig. 12.9

This technique remained pervasive as the industry shifted to SiGe source/drain regions. Thompson ¶90; *see also* EX1024 at Abstract, 2:66-3:13, 8:34-9:63; EX1026 at 1:10-14; *Kim* ¶0007, ¶¶0050-0051, ¶0074; EX1027 ¶0021, ¶¶0024-0025, ¶0042; *Tung* ¶0005, ¶¶0029-0031, ¶0034, ¶0061, ¶0078; EX1019 ¶¶0023-0025, ¶¶0039-0045, ¶0050, ¶0066, ¶0086; EX1021 ¶0086, ¶0096; EX1011 at 6.



As the energy diagram above illustrates, the Schottky barrier height (Φ_{Bp}) for a pFET source/drain region depends on the bandgap (E_g) and electron affinity (χ) of the source/drain semiconductor, and the work function (Φ_M) of the metal. Thompson ¶¶69-72. A POSITA would have understood the electron affinity (χ) of SiGe and the work function (Φ_M) of a metal-SiGe compound remain nearly unchanged no matter the Ge concentration. Thompson ¶74; *see also* EX1023 at 11; EX1028 at Tbl. 1; EX1029 at Fig. 1. On the other hand, a POSITA would have known the SiGe bandgap (E_g) varies with Ge concentration as shown below. Thompson ¶¶74-76; *see also* EX1030 at Fig. 17; EX1031 at 7, Fig. 9; EX1011 at 4, 6-7, Fig. 12; EX1032 at 15-16, Fig. 1.5.

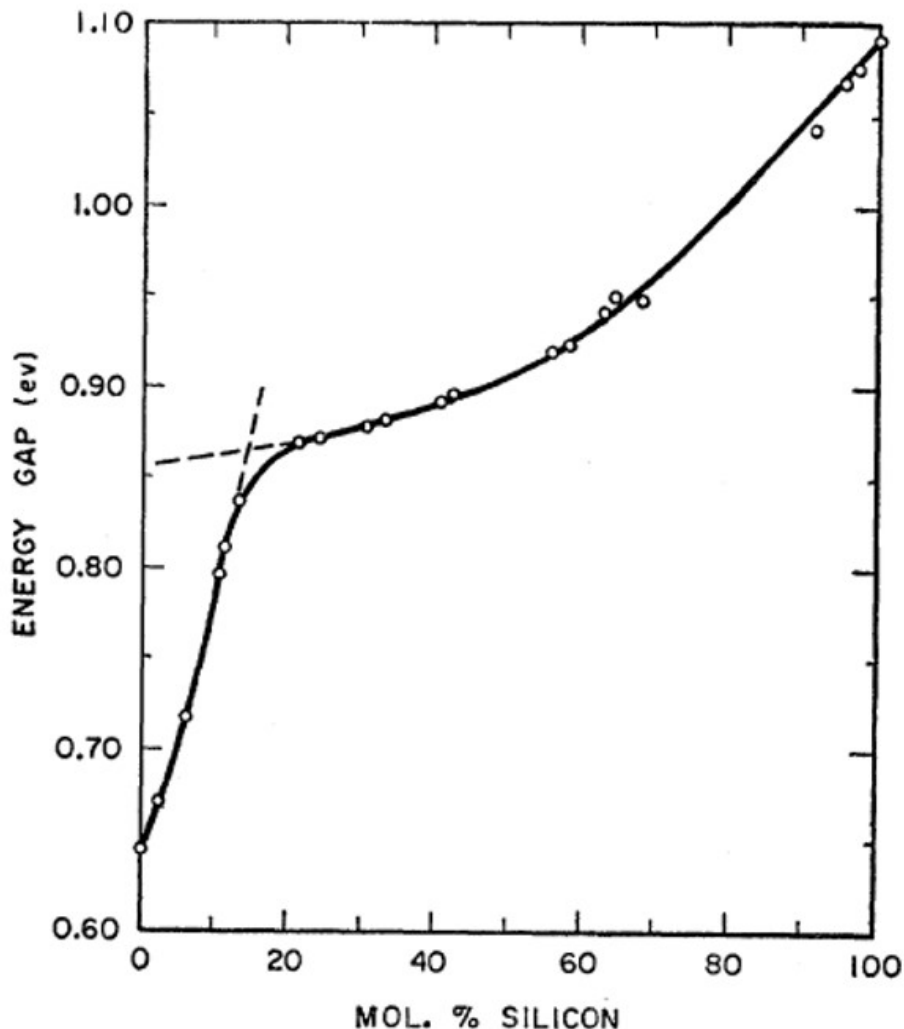


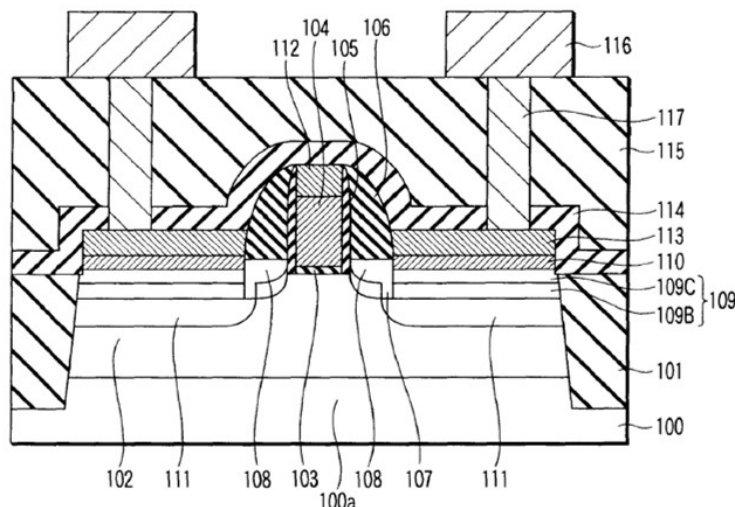
FIG. 17. Composition dependence of energy gap in Ge-Si alloys at 296°K, based on one-phonon Macfarlane-Roberts expression; see Eq. (1) in text.

EX1030, Fig. 17

The SiGe bandgap notably drops around 15 at. % Si (i.e., 85 at. % Ge),² where a “crossover from ... Si-like” behavior to “Ge-like” behavior occurs. EX1031 at 7. A POSITA thus would have expected using a Ge overlayer (e.g.,

² All percentages in this Petition are atomic percentages.

more than about 85% Ge) on the source/drain regions to further reduce Schottky barrier height and lower contact resistance significantly. Thompson ¶¶67, ¶¶76-80; *see also* EX1019 ¶¶0042-0045, ¶0086; *Kim* ¶¶0072-0074; *Tung* ¶¶0058-0061, ¶¶0078-0081; EX1033 at 1:8-15, 4:46-53, 7:20-43.



EX1019, Fig. 16

This approach was known. One example, shown above, teaches p-type SiGe source/drain regions 109 and a Ge overlayer 110. EX1019 ¶0086, ¶0090, ¶¶0094-0095, Fig. 16. SiGe layer 109C is graded such that the Ge concentration at its lower interface with SiGe layer 109B “is approximately 10 to 30 at %” and the Ge concentration at its upper interface with Ge capping layer 110 “is approximately 100 at %.” *Id.* ¶0085. Ge overlayer 110 reacts with a metal to form germanide layer 113 and create a low-resistance contact. *Id.* ¶0024.

This structure was derived by applying the basic Schottky barrier engineering principles noted above. *Id.* ¶¶0042-0045. Predictably, “as compared

with the conventional technology where the silicide film is formed on the silicon layer or the silicon germanium layer, the contact resistance in the source/drain layer can be reduced in this embodiment where the germanide layer is formed on the germanium layer.” *Id.* ¶¶0045; *see also* EX1021 ¶¶0060, ¶¶0086. Dr. Thompson explains that using such a Ge overlayer is a “proposal I would have expected my graduate students to provide if I asked on an exam how to reduce the source/drain contact resistance of a SiGe pFET.” Thompson ¶76.

D. Source/Drain Doping Profiles

Not only was it known that SiGe source/drain regions improve channel mobility, *see* Section III.B, but it was also known they improve source/drain doping control, Thompson ¶84. “Doping” refers to the addition of impurities to a semiconductor to change its conductivity, and the most common dopant for pFET source/drain regions is boron. *Id.* ¶81.

As the ’178 Patent acknowledges, the equation governing contact resistance dictates that higher doping concentrations at a metal-semiconductor interface reduce contact resistance. *Id.* ¶¶68, ¶84; *see also* ’178 Patent 10:42-60; EX1022 at 10-12; EX1023 at 7. That is, “[t]o lower the contact resistance, we need a small Schottky barrier height at the interface and a sufficiently high doping level under the metal contact.” EX1011 at 3.

But short-channel effects (“SCEs”) can occur if the boron concentration is too high deeper below the metal-semiconductor interface. *See* EX1034 at 1; EX1035 at 3, Fig. 11. It was thus known to grade the boron concentration such that “the boron concentration at the near surface regions is extremely high ($1\text{E}20$ to $2\text{E}21/\text{cm}^3$) and boron concentration at the middle and lower portion of the S/D region is relatively low ($1\text{E}18$ to $1\text{E}20/\text{cm}^3$).” EX1036 ¶0124; *see also* Thompson ¶¶85; EX1020 at 2-3, Fig. 5; EX1019 ¶0059; *Tung* ¶¶0005, 0027, 0031, 0034, 0065, 0069, Figs. 11b, 12b; EX1037 at 1-2, Fig. 7; EX1035 at 1-4, Fig. 7.

One way to achieve a graded doping profile is also the most common doping technique—ion implantation. Thompson ¶¶82-83. It necessarily results in a graded doping profile. *Id.* ¶83. For p-type SiGe, ion implantation involves irradiating the source/drain regions with boron ions, which are scattered by the Si/Ge atoms and spread out below the semiconductor surface. *Id.*; *see also* EX1038 at 7-11. The boron atoms are incorporated into the semiconductor with a profile comparable to the ones below, which in these examples peak at about 3×10^{20} atoms/cm³. *See* EX1039 at Fig. 4.5; EX1034 at Figs. 2, 5; EX1020 at 3, Fig. 5; EX1035 at 3, Fig. 9. Boron profiles like these in SiGe source/drain regions were routinely used to reduce contact resistance and mitigate SCEs. Thompson ¶¶83-86.

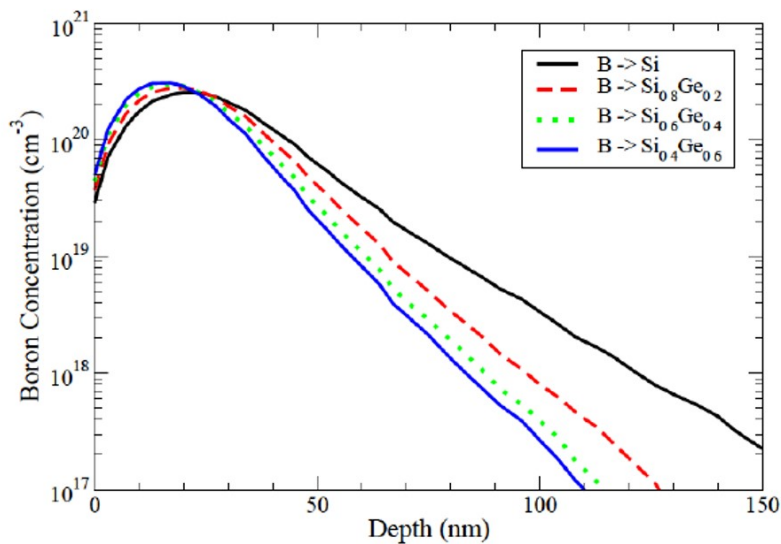


Figure 4.5: Simulated 5keV boron profiles in (100) $\text{Si}_{1-x}\text{Ge}_x$ with $x = 0, 20\%, 40\%, 60\%$ using a dose of 10^{15}cm^{-2} and a tilt of 7° .

EX1039, Fig. 4.5

E. Characteristics of Epitaxial SiGe Source/Drain Regions

As shown below, epitaxially grown SiGe source/drain regions have either a diamond shape or a rectangular shape, depending on wafer orientation. Thompson ¶94; *see also* EX1040 at 50, Fig. 2.37; *Tung* ¶0058; EX1041 at 5:29-43, 10:6-24, Fig. 5A.

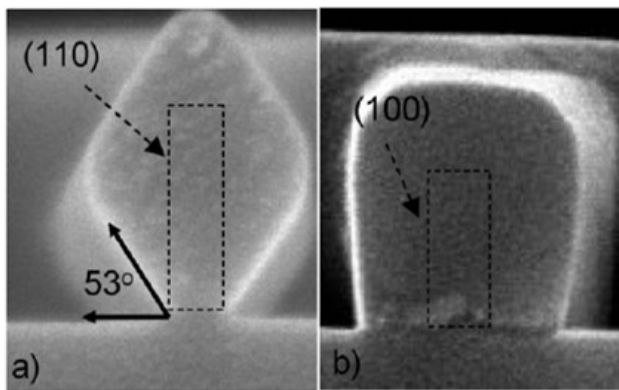


Fig. 2.37. Cross sectional SEM images on fins after epitaxial growth. a) (110) side wall surface result in diamond-shaped fin; b) (100) sidewall surface result in square-shaped fin.

EX1040, Fig. 2.37

A POSITA also would have understood that, to be commercially viable, strain engineering requires FET channels aligned with the $\langle 110 \rangle$ axis on “industry-standard Si wafers with (001) surface and wafer notch on the $[110]$ axis.” EX1042 at 2; *see also* Thompson ¶95; EX1043 at 1, Fig. 4b. For such an orientation, a POSITA would have understood SiGe naturally grows in a diamond shape (see below). Thompson ¶¶95-96; *see also* EX1043 at Fig. 7b; EX1040 at 50, Fig. 2.37; EX1041 at 5:29-43, 10:6-24, Fig. 5A.

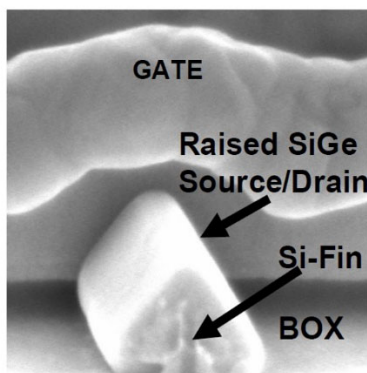
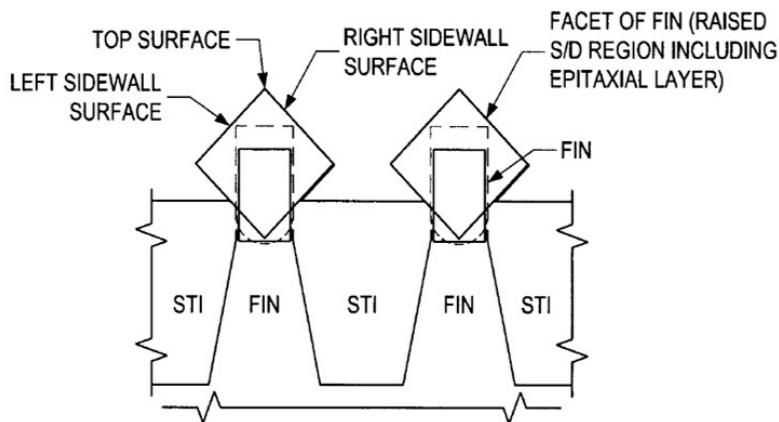


Fig. 7b Y-dir. cross-section of PMOS Trigate with SiGe raised source/drain

EX1043, Fig. 7b



EX1041, Fig. 5A

Thus, a POSITA would have understood epitaxial SiGe source/drain regions grown using the industry-standard wafer and channel orientation, which is necessary for effective strain engineering, naturally grow in a diamond shape. Thompson ¶97.

IV. THE '178 PATENT

The '178 Patent centers on a Ge capping layer that reduces Schottky barrier height: “[A]n intermediate boron doped germanium layer is provided between the

source/drain and contact metals to significantly reduce contact resistance.” ’178 Patent at 2:17-25; *see also id.* at 3:44-50 (calling this “a bilayer construction” comprising “SiGe (for the source/drain regions) capped with an overlayer of a boron doped germanium layer”).

The ’178 Patent tries to distinguish itself from prior art based on this Ge capping layer. *See id.* at 2:36-49, 14:3-16, Fig. 7. The patent purports to “marry superior contact properties of germanium with superior semiconductor transistor properties of Si and SiGe to provide next generation low resistance contacts.” *Id.* at 2:66-3:2. Specifically, “an overlayer or cap of boron doped germanium can be formed directly over the source/drain regions,” and a “contact metal (or series of metals) can then be deposited and a subsequent reaction (annealing) can be carried out to form metal germanide source and drain contacts.” *Id.* at 3:17-23. The specification attributes alleged improvements to the well-known principles described in Section III.C. *Compare id.* at 4:3-9, 10:43-60, 12:7-12, 14:30-46, with Section III.C; EX1019 ¶¶0039-0045, ¶¶0085-0086; Thompson ¶¶66-80.

The embodiment below shows a transistor in which SiGe source/drain regions 318/320 are formed “using any number of conventional techniques,” such as “epitaxially depositing a silicon or silicon germanium material (e.g., with a germanium concentration in the range of, for instance, 10 to 70 atomic %).” ’178 Patent at 4:18-25; *see also id.* at 7:46-9:16, Figs. 3A-3B. Boron-doped “germanium

layers” 317/319 are then deposited on source/drain regions 318/320. *Id.* at 9:31-35, Fig. 3C. These “germanium layers” contain at least 90% Ge. *Id.* at 9:35-45; *see also id.* at 3:12-20, 7:2-11, 10:43-60, 12:21-31, 16:14-17, 16:40-45, 16:59-62, 17:17-21, 17:34-40, 18:4-6. After depositing a “metal and annealing to form silicide/germanide” layers 325/327, contact plugs 329/331 are formed. *See id.* at 11:56-12:7, Figs. 3H, 3I. “The boron doped germanium layer 317/319 allows for metal-germanide formation,” which “significantly lower[s] Schottky-barrier height and improve[s] contact resistance (including R_{ext}) over that in conventional metal-silicide systems.” *Id.* at 12:7-12.

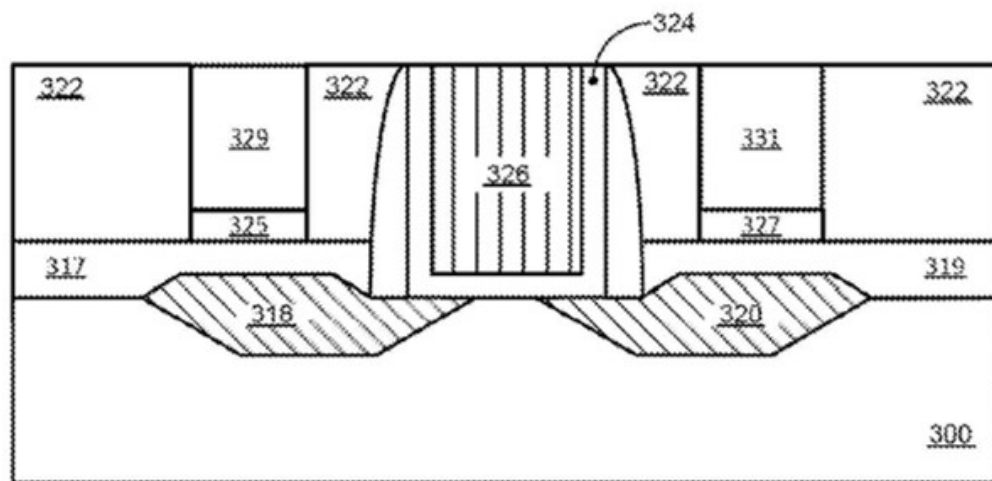
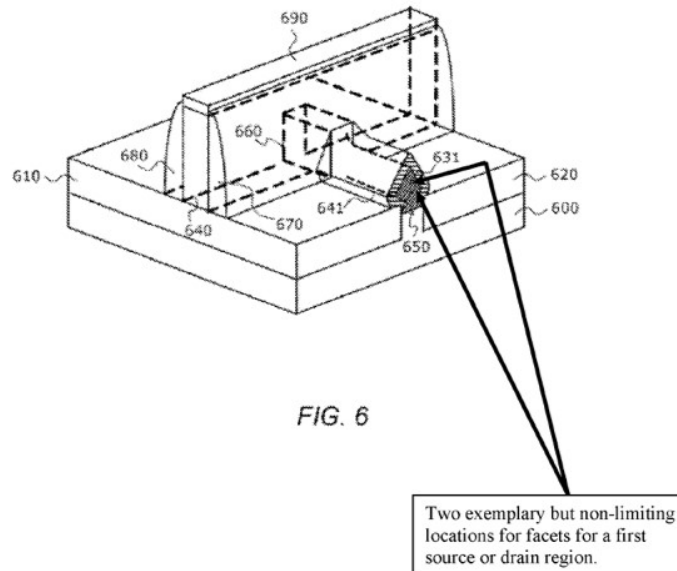


FIG. 3I

Prosecution of the '178 Patent was fairly uneventful. The Examiner rejected the claims for failing to describe the claimed “facets.” File History at 223-28. The Applicant submitted the annotated figure below in response, and the Examiner allowed the claims without amendment. *Id.* at 293-95, 307-10.



Annotated Figure 6 of Applicant's specification.

Parroting claim 1, the Examiner stated that “prior art failed to disclose or fairly suggest an integrated circuit structure, comprising, along with other recited claim limitations, first and second germanide layers and graded germanium concentration in excess of 50%” and source/drain regions in a fin that “compris[e] two or more facets and a top surface.” *Id.* at 308.

V. LEVEL OF ORDINARY SKILL

A POSITA would have had at least a Master’s degree in electrical engineering, physics, materials science, or a related field and at least two years of work experience in integrated circuit device design or manufacturing, although additional education could substitute for professional experience and significant work experience could substitute for formal education. Thompson ¶46.

VI. CLAIM CONSTRUCTION

The Board construes claims under the standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). A POSITA would have understood “germanide layer” refers to a “germanium layer metalized with one or more metals.” Thompson ¶¶125-131.

According to the '178 Patent, a nominal “germanium” layer has at least 90% Ge. *See* '178 Patent at 3:12-20, 9:35-45. The '178 Patent describes a “germanide layer” as such a germanium layer once it is metalized (made metallic by annealing the Ge layer with a metal to induce a chemical reaction between them). *Id.* at Title, 3:20-23, 12:1-12, 14:30-37. And it distinguishes “germanides” from “industry standard silicides” based on the presence of this Ge layer. *Id.* at 2:36-57, 14:3-16, Fig. 7; *see also* EX1024 at 2:66-3:9 (same inventors referring to a “nickel silicon germanium ***silicide***” formed by directly metalizing SiGe source/drain regions); EX1019 ¶0045 (comparing “the conventional technology where the silicide film is formed on the silicon layer or the silicon germanium layer” with a “germanide layer ... formed on the germanium layer”). Moreover, the title, abstract, and every description characterizes the invention as providing a Ge layer and metalizing it to form a germanide layer. *See* '178 Patent at Title, Abstract, 1:37-40, 1:41-44, 1:45-48, 2:22-25, 2:32-57, 3:17-20, 3:26-29, 3:44-50, 3:55-58, 3:63-4:2, 4:14-18, 4:56-58, 4:66-5:4, 5:20-24, 5:50-54, 6:11-16, 6:42-48,

6:54-56, 7:2-11, 7:23-27, 9:17-20, 9:23-28, 9:34-45, 9:50-55, 9:61-64, 10:33-39, 10:43-63, 11:50-59, 12:7-12, 12:21-31, 12:34-48, 13:53-59, 14:3-16, 14:30-37, 16:12-45, 16:50-69, 17:17-21, 17:23-40, 17:44-55, 18:4-8, 18:12-15. During prosecution of a related European application, the applicant emphasized: “It is clear that according to the invention” the devices “comprise a heavily doped germanium layer. More specifically, there is a germanium layer that is ‘pure’, that is, close to 100% (ie over 90% according to the specification).” EX1045 at 1-2; *see also Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1374 (Fed. Cir. 2005) (using applicant’s statements to the EPO to construe claim).

Because the ’178 Patent “repeatedly and consistently characterizes” a germanide layer as a germanium layer metalized with one or more metals, “it is proper to construe [it] in accordance with that characterization.” *WARF v. Apple Inc.*, 905 F.3d 1341, 1351 (Fed. Cir. 2018); *see also In re Abbott Diabetes Care, Inc.*, 696 F.3d 1142, 1150 (Fed. Cir. 2012); *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 790 (Fed. Cir. 2021).

In a related ITC proceeding, Patent Owner argued “germanide layer” means “thickness of material, comprising germanium and a metal.” This position lack merit. Thompson ¶¶132-136. First, a layer without chemical bonding between metal and semiconductor atoms would qualify. Such a layer would undermine the purpose of the invention and raise, not lower, contact resistance. *Id.* ¶133. Second,

it encompasses admitted prior art—“industry standard silicides” formed “without the intermediate boron doped germanium layer between the source/drain regions and contact metal.” ’178 Patent at 2:36-49; *see also id.* at 2:66-3:2, 3:17-23, 10:43-60, 14:3-16, 14:30-46, Fig. 7; Thompson ¶134. Third, as noted above, every description of every embodiment hinges on the Ge layer and its metalization to lower Schottky barrier height and reduce contact resistance. Patent Owner’s proposed construction would eliminate this fundamental feature of the ’178 Patent and result in a structure not described. Thompson ¶135.

VII. OVERVIEW OF ASSERTED PRIOR ART

A. *Ranade* (U.S. Patent Application Pub. No. 2008/0121932)

Ranade is prior art under pre-AIA §102(b). It describes planar FETs and non-planar FinFETs. *Ranade* ¶0010, ¶0025, ¶0044. As Figure 2N shows below,³ *Ranade*’s devices include a gate electrode 260 and $\text{Si}_x\text{Ge}_{1-x}$ epitaxial source/drain regions 220 made of “a graded epitaxial layer” to “minimize[] surface defects.” *Id.* ¶0040; *see also id.* ¶0042. Specifically, “the pair of source/drain regions 220 is a crystalline silicon/germanium region of the stoichiometry $\text{Si}_x\text{Ge}_{1-x}$, where $0 \leq x \leq 1$,” meaning the Ge concentration may vary within a range of 0 to 100%. *Id.* ¶0040; *see also* Thompson ¶139.

³ Annotated with more references for clarity.

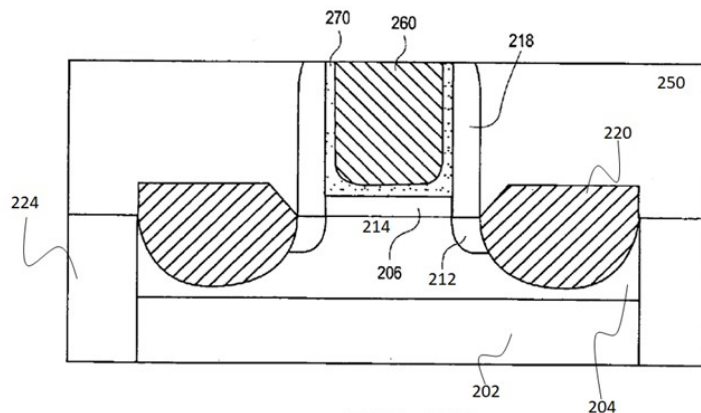


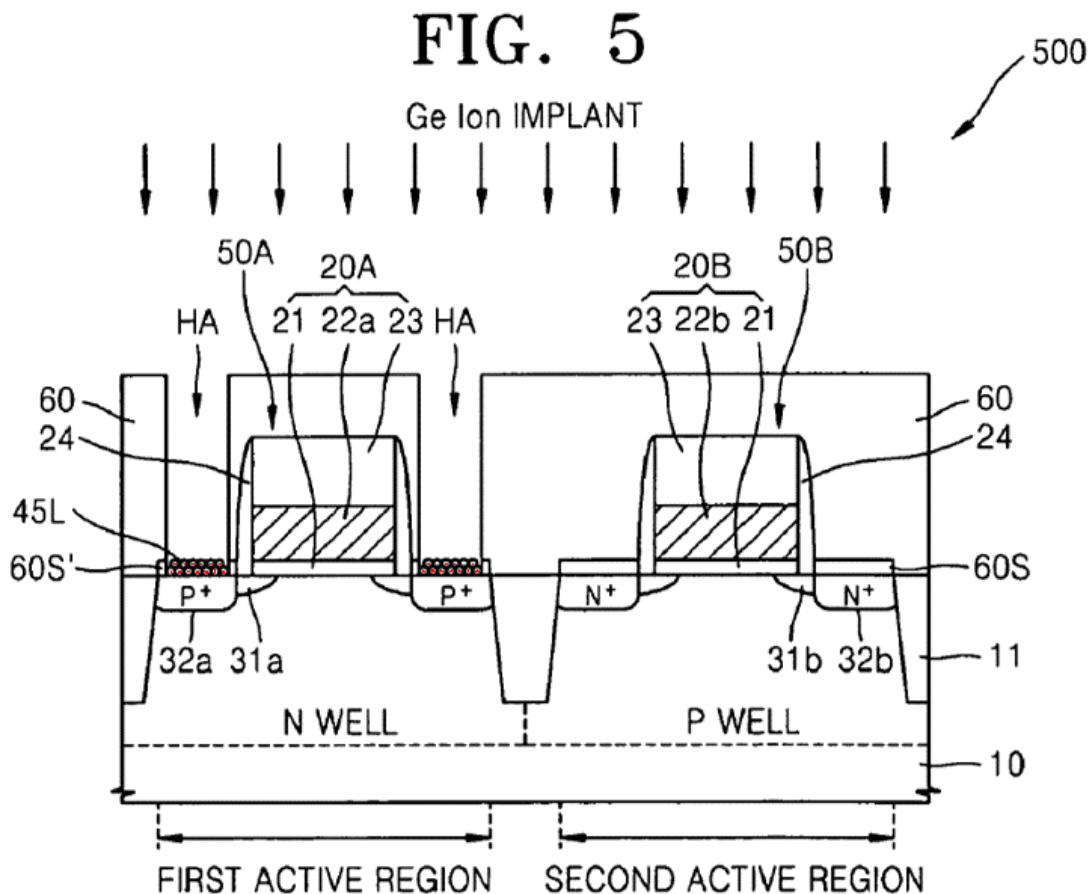
FIG. 2N

B. *Kim* (U.S. Patent Application Pub. No. 2010/0123198)

Kim is prior art under pre-AIA §§102(a) and (e). “In order to provide a low resistance contact to a CMOS transistor,” *Kim* explains “the P-channel and N-channel MOSFETs need to be provided with a contact having a low Schottky barrier.” *Kim* ¶0007; *see also id.* ¶0050. *Kim* describes two processes for forming such contacts: Ge Overlayer Metalization and Direct Metalization. Thompson ¶¶143-147.

1. Ge Overlayer Metalization

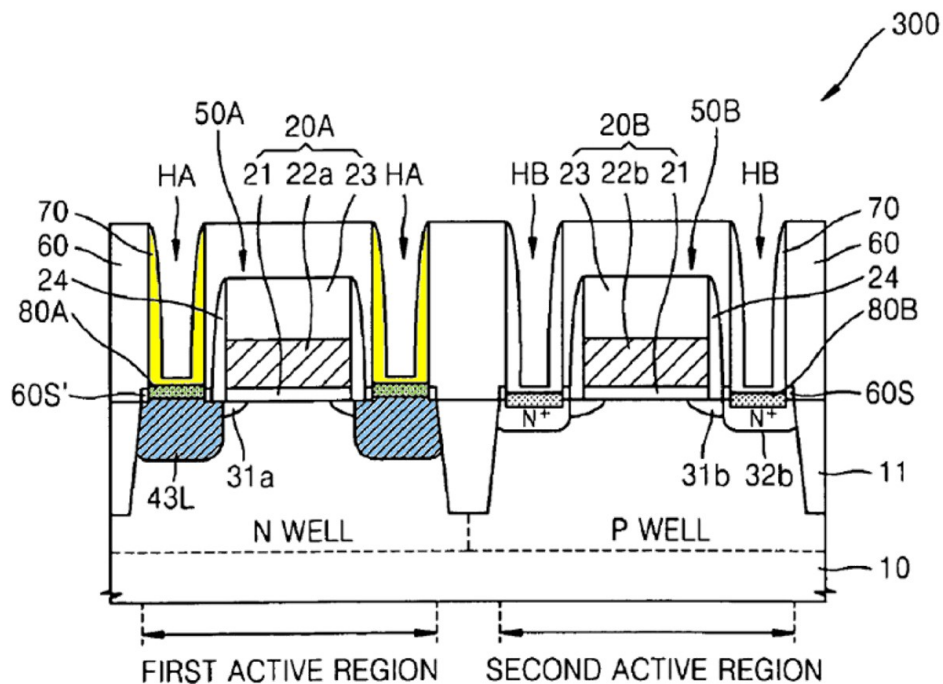
Figure 5 below shows what Dr. Thompson calls *Kim*’s Ge Overlayer Metalization. A thin Ge overlayer 45L (red below) is metalized by reacting it with metal layer 70 (e.g., Ti, not shown). *Kim* ¶¶0070-0073; *see also* Thompson ¶¶144-145. *Kim* explains “a $M(Si_{1-y}Ge_y)$ film” 80A results, where the metal “M” may be titanium. *Kim* ¶0047, ¶0071, ¶0073.



2. Direct Metalization

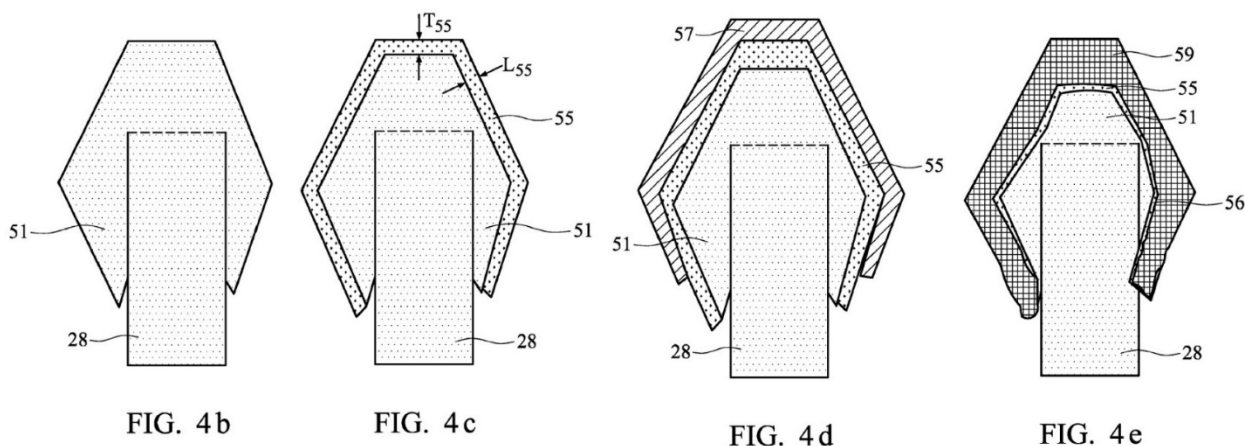
Figure 3F below shows what Dr. Thompson calls *Kim's* Direct Metalization. Instead of metalizing a Ge overlayer as above, exposed SiGe source/drain regions 43L (blue) are metalized by reacting them with metal layer 70 (yellow). *Kim* ¶0050; *see also id.* ¶0046, Fig. 3F. This creates metal-semiconductor film 80A (green)—a “M(Si_{1-y}Ge_y) film containing Ge due to the exposed SiGe epitaxial layer 43L,” where “M” represents the metal of metal layer 70 (e.g., Ti). *Id.* ¶0067; *see also id.* ¶¶0046-0050, ¶0057, ¶¶0063-0067, ¶0071, Fig. 3F; Thompson ¶¶146-147.

FIG. 3F



C. *Tung* (U.S. Patent Application Pub. No. 2010/0276761)

Tung is prior art under pre-AIA §§102(a) and (e). It teaches FinFET “structures and methods of fabrication thereof with low resistance contacts for non-planar semiconductor structures.” *Tung* ¶0006; *see also id.* ¶0005, ¶0034, ¶0061; Thompson ¶¶149-154.



As in Figure 4b, SiGe semiconductor material 51 grows over fin 28 in the source/drain areas. *Tung* ¶¶0040, ¶¶0074, ¶¶0076, Figs. 4b, 13. As in Figure 4c, “another selective epitaxial growth is used to form a doped semiconductor layer 55” in the source/drain areas, which may be “doped SiGe, or doped Ge.” *Id.* ¶¶0041; *see also id.* ¶¶0034, ¶¶0058, ¶¶0078, Figs. 4c, 14. Then, as in Figure 4d, “metal 57 [e.g., Ti] is deposited” over doped semiconductor layer 55. *Id.* ¶¶0042; *see also id.* ¶¶0079-0080, Figs. 4d, 15. “[M]etal 57 is annealed to form ... layer 59,” and any unreacted metal 57 “is removed by an etching process.” *Id.* ¶¶0043; *see also id.* ¶¶0081, Figs. 4e, 16. During annealing, “metal 57 (FIG. 4d) reacts with the doped semiconductor layer 55” to form layer 59, as in Figure 4e. *Id.* ¶¶0043; *see also id.* ¶¶0045, ¶¶0063-0064, ¶¶0081.

D. *Brask* (U.S. Patent No. 7,361,958)

Brask is prior art under pre-AIA §102(b). As highlighted below, *Brask* teaches FinFETs with raised source/drain fin regions 410 made by growing $\text{Si}_x\text{Ge}_{1-x}$ ($0 \leq x \leq 0.99$) on fins 330/370. *Brask* at 10:20-49, Figs. 4A, 4B. According to *Brask*, this $\text{Si}_x\text{Ge}_{1-x}$ film 410 may “be graded.” *Id.* at 10:20-29.

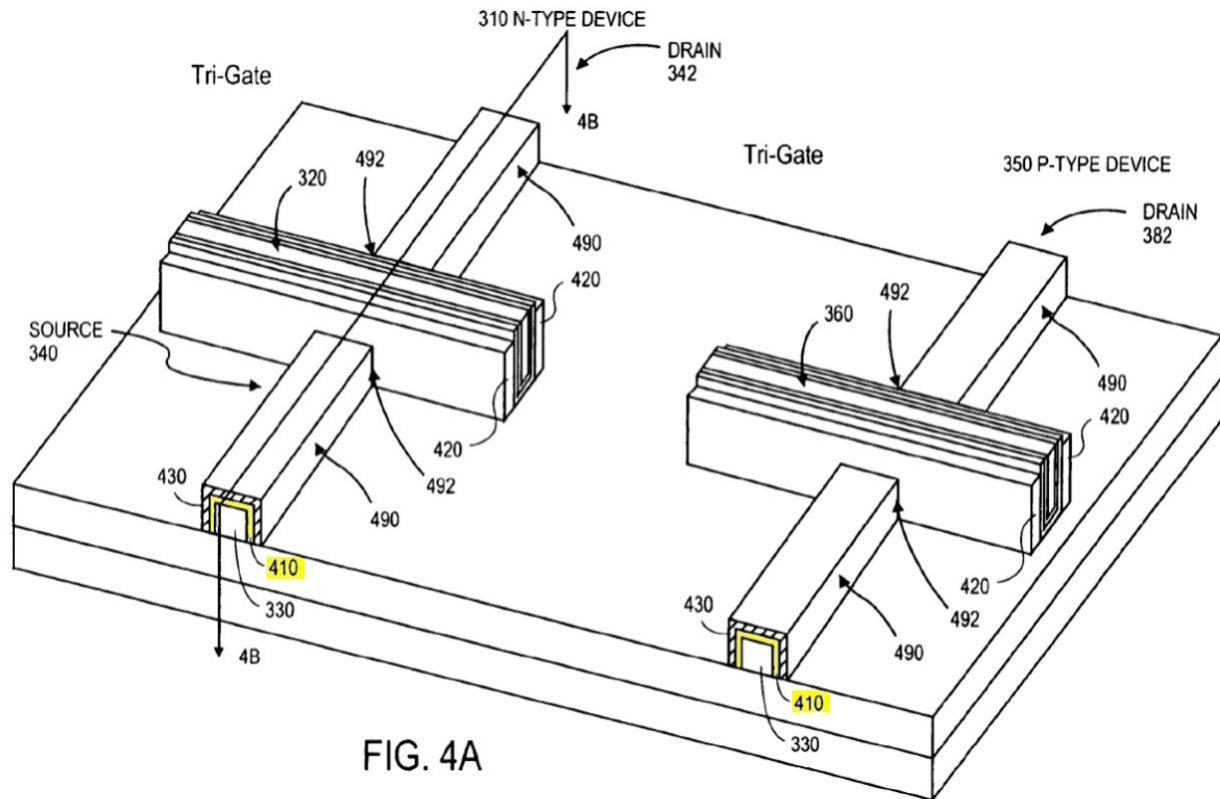


FIG. 4A

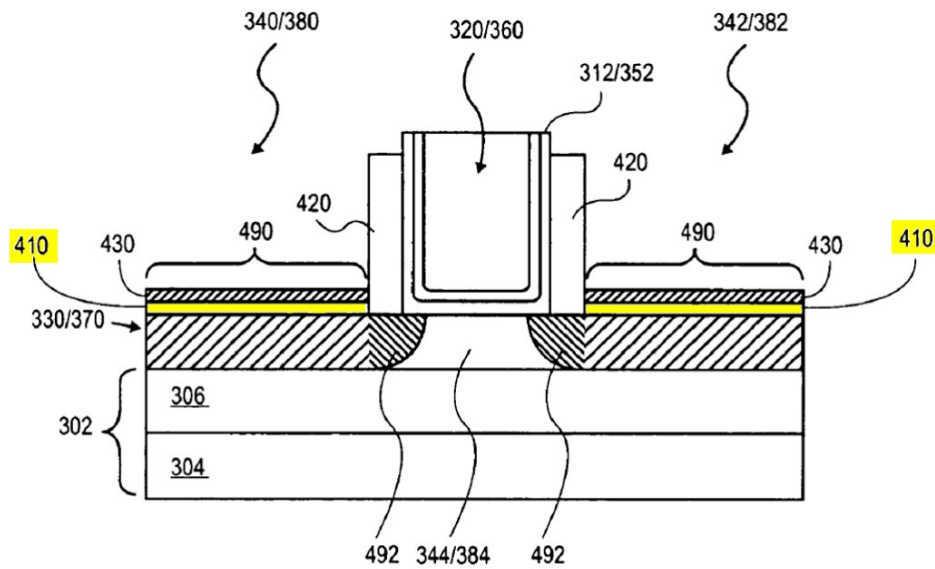
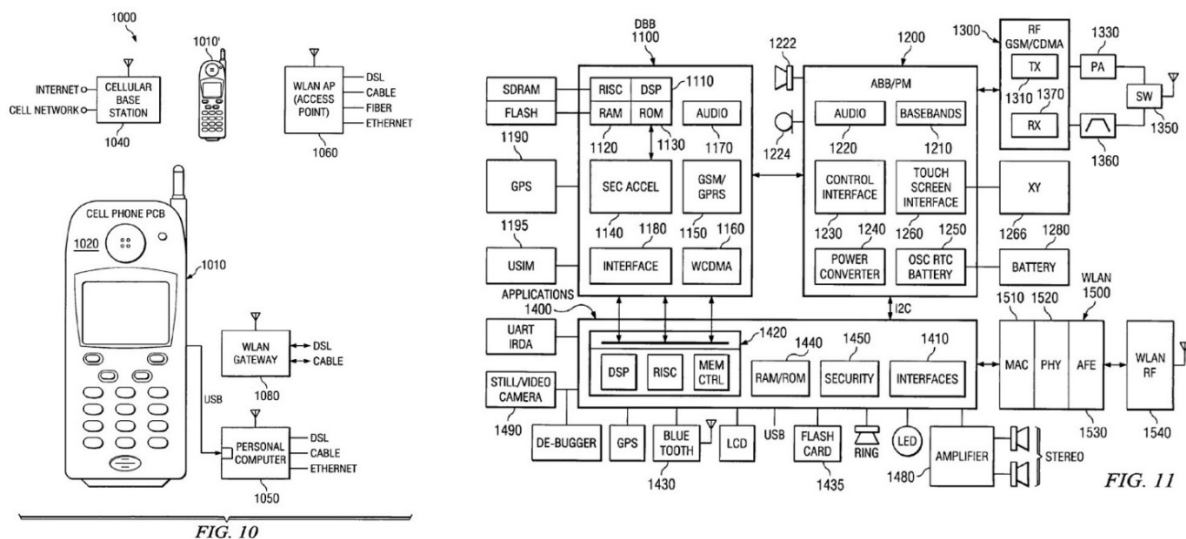


FIG. 4B

E. *Liu* (U.S. Patent No. 7,611,943)

Liu is prior art under pre-AIA §102(b). As Figures 10 and 11 illustrate, *Liu* confirms that FinFETs were used for computing devices, including smartphones. *Liu* at 1:29-32, 1:47-50, 33:10-37:40, Figs. 10, 11.



VIII. THE CHALLENGED CLAIMS ARE UNPATENTABLE

The '178 Patent purports to provide low-resistance contacts to SiGe source/drain regions by adding a Ge overlayer. The principles that suggest using a Ge overlayer, and the Ge overlayer itself, were known. Thompson ¶162.

The '178 Patent's alleged improvements stem from three principles: (1) high Ge concentration in the Ge overlayer to lower Schottky barrier height; (2) high boron concentration in the Ge overlayer to reduce contact resistance, and (3) boron diffusion suppression due to high Ge concentration in the Ge overlayer. Thompson ¶163; *see also* '178 Patent at 2:33-57, 4:3-9, 10:43-60, 14:30-46. These are the

foundational principles underlying all of SiGe/Strained Si technology. Thompson ¶163; *see also* EX1011 at 5; EX1037 at 1-2, Fig. 3. The '178 Patent claims an obvious and known structure based on these principles. Thompson ¶164.

Not only does the '178 Patent claim a prior-art solution, but it describes a known result. *Id.* ¶165; *compare also* '178 Patent at 2:36-57 (reducing Schottky barrier height from 0.5 eV to 0.2 eV), *with* EX1011 at 9 (“[W]e expect a barrier height change of approximately 0.3 eV.”), *and* EX1019 ¶0045 (“ $\phi_B=0.2$ eV is achieved” by forming a “germanide layer on [a] germanium layer”).

Because these principles, structures, and benefits were known, a POSITA would have found the challenged claims obvious. Thompson ¶166.

A. Ground 1A: The *Ranade-Kim* Combination

1. A POSITA Would Have Found the *Ranade-Kim* Combination Obvious

Kim recognizes the need to reduce source/drain contact resistance, *Kim* ¶¶0006-0007, and instructs the reader to do so by forming a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film over p-type source/drain regions to “reduce the height of Schottky barriers,” *id.* ¶0050. A POSITA would have found it obvious to apply such a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film to *Ranade*’s source/drain regions to reduce contact resistance. Thompson ¶¶167-171.

a. A POSITA would have wanted to apply *Kim*'s contacts to *Ranade*'s FinFET

Ranade describes a FinFET with SiGe source/drain regions but does not provide details about source/drain contacts, including contact materials. Thompson ¶¶173-174. As the literature commonly does, *Ranade* focuses on the transistor itself and simply relies on a POSITA's general understanding of "typical process steps to complete the formation of a MOS-FET, ... such as a silicidation step."⁴ *Ranade* ¶0041; *see also* Thompson ¶¶174-175; *Brask* at 27:20-27, Fig. 5Z; EX1046 at 4:43-48; *Tung* ¶0023, ¶0036, ¶0064; EX1018 ¶0043; EX1027 ¶0021.

Like *Ranade*, *Kim* discloses FinFETs with SiGe source/drain regions, but it further describes source/drain contacts that include a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film. Since *Ranade*'s FinFETs require source/drain contacts to operate, a POSITA would have found it obvious to follow *Ranade*'s instructions and apply a "silicidation" process—like the ones *Kim* describes—to contact *Ranade*'s FinFETs. *Compare Ranade* ¶0041, with *Kim* ¶¶0050, 0072-0074; *see also* Thompson ¶176.

Kim teaches two silicidation processes: Ge Overlayer Metalization and Direct Metalization. *Supra* Section VII.B; *Kim* ¶¶0066-0069, 0072-0074. In both,

⁴ "Silicidation" refers to the process of depositing metal on a semiconductor layer and annealing to induce a chemical reaction between the semiconductor atoms and metal atoms. Thompson ¶¶88-90, ¶127.

the result is a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film that “reduce[s] sheet resistance.” *Kim* ¶0050. A POSITA seeking to implement *Ranade*’s FinFET as instructed would have wanted to apply either technique to reduce contact resistance. Thompson ¶¶178-182.

b. A POSITA would have reasonably expected to succeed

It was well known to form metal-semiconductor compounds like *Kim*’s $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film to contact source/drain regions. Thompson, ¶¶184-185. It was also well-known that metal-semiconductor compounds like *Kim*’s $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film reduce contact resistance in SiGe pFETs. *Id.* ¶¶186-187; *see also Kim* at Abstract, ¶0003, ¶0010, ¶0050, ¶0071, ¶0074; EX1026 at 1:10-14; *supra* Section III.C.

A POSITA would have understood such metal-semiconductor compounds are formed by depositing a metal onto a semiconductor, then annealing to cause atoms near the metal-semiconductor interface to react. Thompson ¶92, ¶¶127-128; *see also Kim* ¶0050; EX1026 at 1:10-25; EX1019 ¶0024. This technique was routine. Thompson ¶¶185-186; *see also* EX1025 at 20, 41-43, Figs. 9.19-9.22, 12.9. *Kim* also expressly states that its teachings apply to FinFETs. Thompson ¶¶188-190; *see also Kim* ¶0033; Korean *Kim* ¶0023. A POSITA thus would have reasonably expected to succeed when applying *Kim*’s $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ films to *Ranade*’s FinFET. Thompson ¶¶183-187.

A POSITA also would have reasonably expected such combination to reduce contact resistance. A POSITA would have understood, as *Kim* teaches, that

Kim's $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ films can be applied to FinFETs with SiGe source/drain regions. *Id.* ¶¶189-190; *see also Kim* ¶0033; Korean *Kim* ¶0023. A POSITA would have understood that remains true regardless of the Ge concentration in those regions. Thompson ¶191; *see also EX1027* ¶¶0024-0025, ¶0042; *EX1019* ¶¶0039-0042; *EX1026* at 6:40-46. Because $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ metal-semiconductor films like *Kim*'s were widely known and applied to SiGe source/drain regions with various Ge concentrations and geometries, there was no reason to think they would behave any differently when applied to *Ranade*'s FinFET. Thompson ¶192.

c. A POSITA would have found it obvious to combine *Ranade*'s FinFET with *Kim*'s Source/Drain Contacts

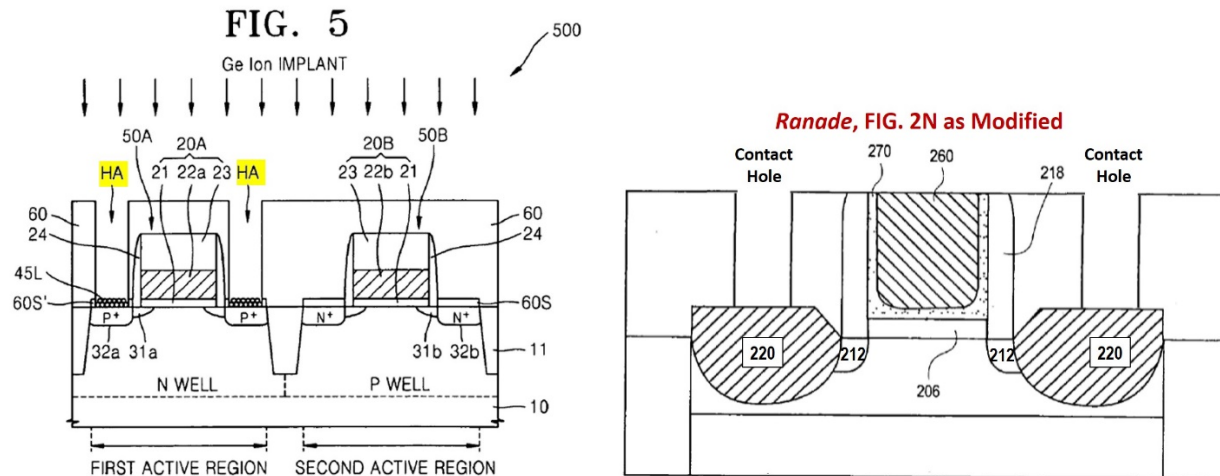
A POSITA would have found *Kim*'s Ge Overlay Metalization and *Kim*'s Direct Metalization suitable for forming source/drain contacts to *Ranade*'s FinFET. Thompson ¶¶193-194. Both were known techniques, and a POSITA would have recognized both as obvious ways to implement *Ranade*'s FinFET. *Id.*

i. Ge Overlay Metalization

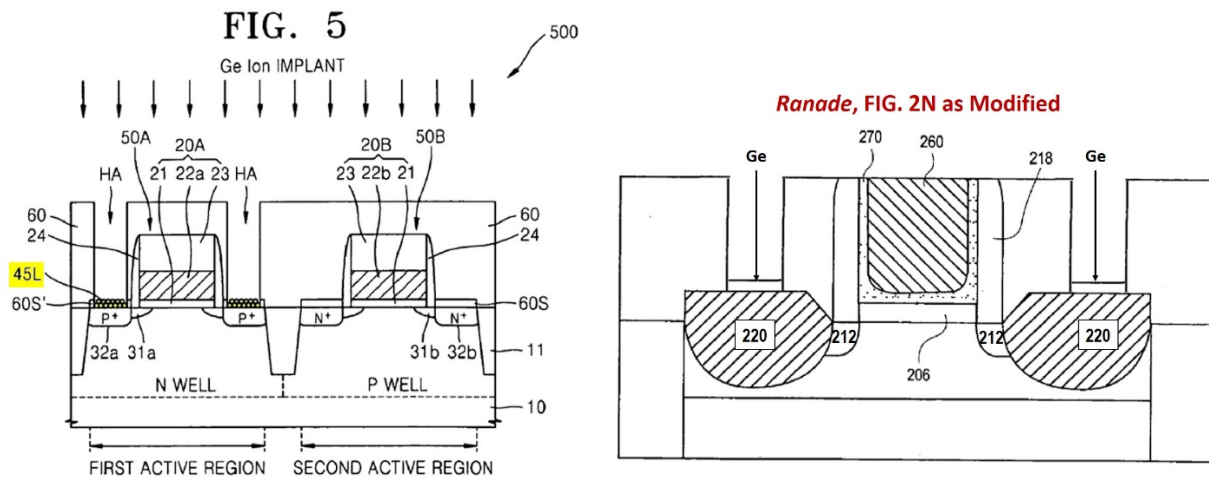
Kim's Ge Overlay Metalization has five steps⁵: (1) Etch Contact Holes; (2) Form a Ge Overlay; (3) Deposit Titanium; (4) Anneal to Form a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film; and (5) Form Contact Plugs. Thompson ¶196. Each applies readily to *Ranade*'s FinFET.

⁵ Same as the '178 Patent. *See* '178 Patent at Title, 11:50-12:12, 14:30-37, Fig. 7.

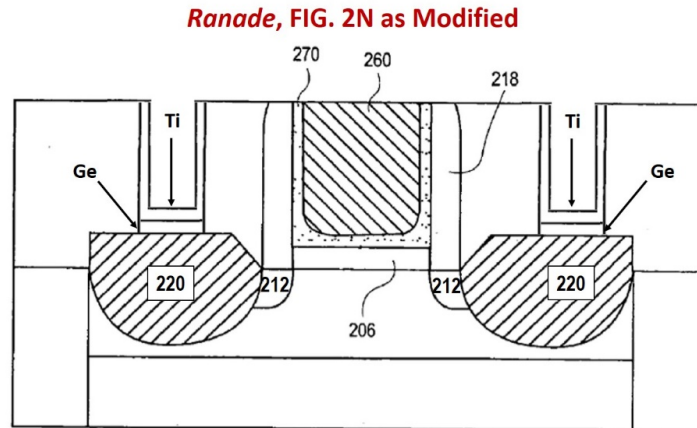
First, *Kim* teaches contact holes HA etched into interlayer insulating film 60, as Figure 5 shows (below left). *Kim* ¶0072. Applied to *Ranade*'s FinFET, it would resemble the figure on the right below. Thompson ¶197, ¶204.



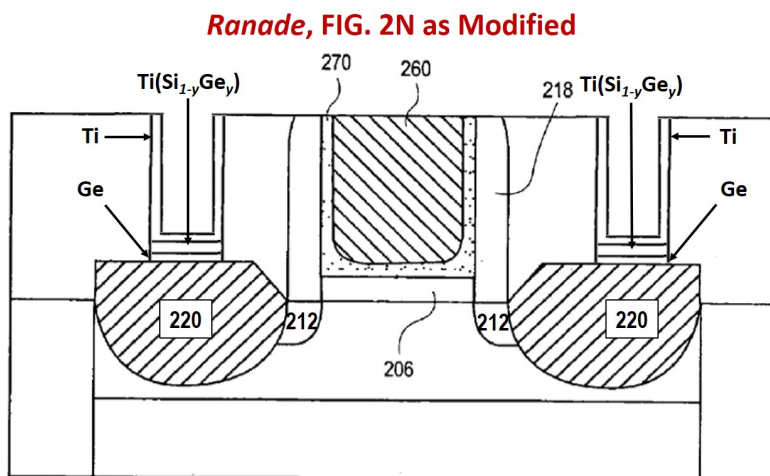
Second, *Kim* teaches forming a thin Ge overlayer 45L on the source/drain regions, as Figure 5 shows (below left). *Kim* ¶¶0072-0074. Applied to *Ranade's* FinFET, it would resemble the figure on the right below. Thompson ¶198, ¶205.



Third, a Ti layer 70 is deposited into contact holes HA. *Kim* ¶¶0047, ¶¶0057, ¶¶0066, ¶¶0071, ¶¶0073. Applied to *Ranade's* FinFET, it would resemble the figure below. Thompson ¶¶199, ¶¶206.

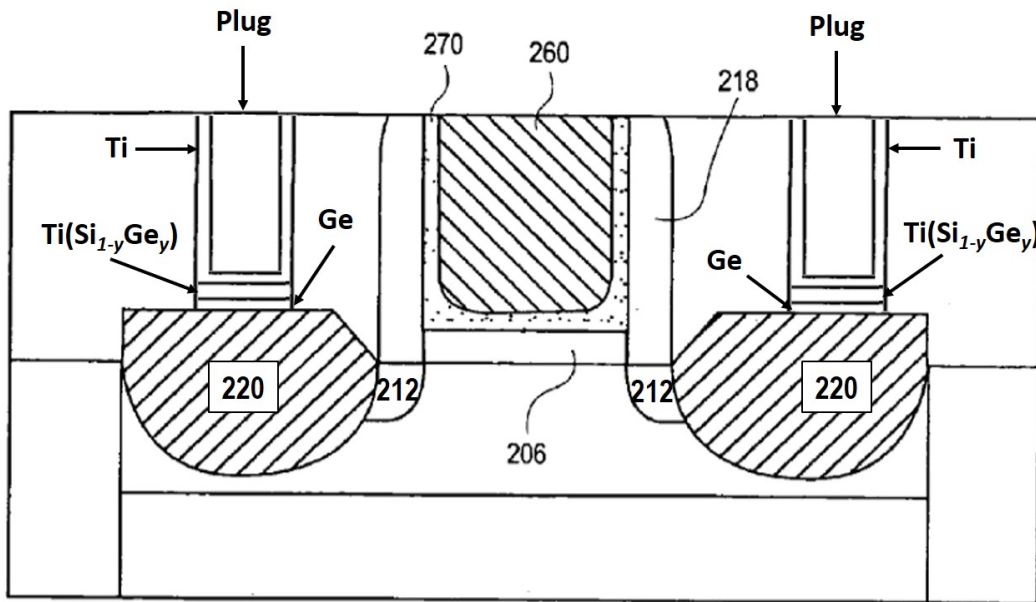


Fourth, annealing causes Ti layer 70 to chemically react with the thin Ge layer 45L and atoms diffused from the source/drain region such that $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A forms. *Kim* ¶¶0072-0074. Applied to *Ranade's* FinFET, it would resemble the figure below. Thompson ¶¶200, ¶¶207.



Fifth, *Kim* teaches forming “contact plugs” 90 on the $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A in contact holes HA. *Kim* ¶¶0049, ¶¶0068, ¶¶0074. Applied to *Ranade*’s FinFET, it would resemble the figure below. Thompson ¶¶201, ¶¶208.

Ranade, FIG. 2N as Modified



Ranade-Kim: First Obvious Implementation (Ge Overlayer Metalization)

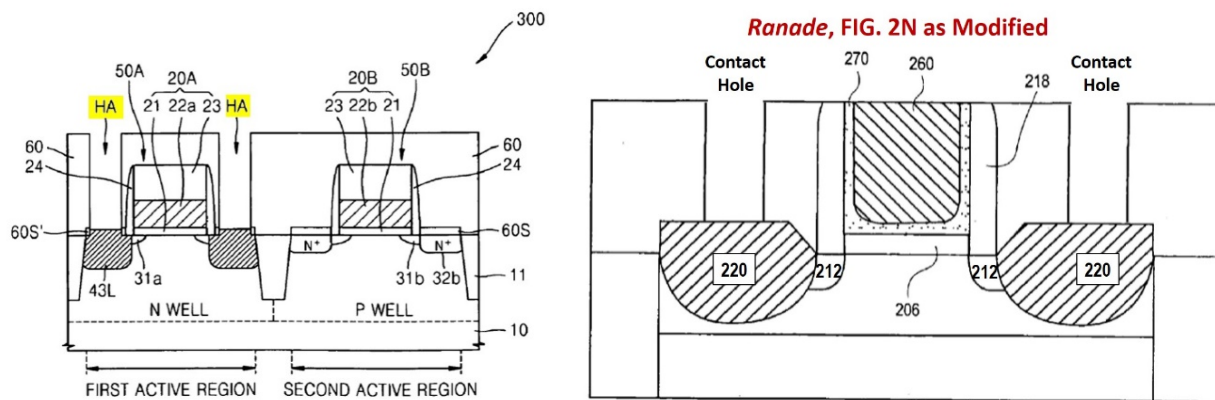
Ranade explains its FinFET is completed using “typical process steps to complete the formation of a MOS-FET, ... such as a silicidation step.” *Ranade* ¶¶0041. *Kim* discloses a silicidation step—Ge Overlayer Metalization. *Kim* ¶¶0072-0074, Fig. 5. A POSITA would have found a combination of *Ranade* and *Kim* resembling the above to be obvious. Thompson ¶¶209.

ii. Direct Metalization

Kim's Direct Metalization⁶ includes four steps: (1) Etch Contact Holes; (2) Deposit Titanium; (3) Anneal to Form a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film; and (4) Form Contact Plugs. Thompson ¶211; *see also Kim* at Figs. 3D-3F. Each applies readily to *Ranade*'s FinFET.

First, *Kim* teaches contact holes HA etched into interlayer insulating film 60, as Figure 3D shows (below left). *Kim* ¶¶0060-0061. Applied to *Ranade*'s FinFET, it would resemble the figure on the right below. Thompson ¶212, ¶218.

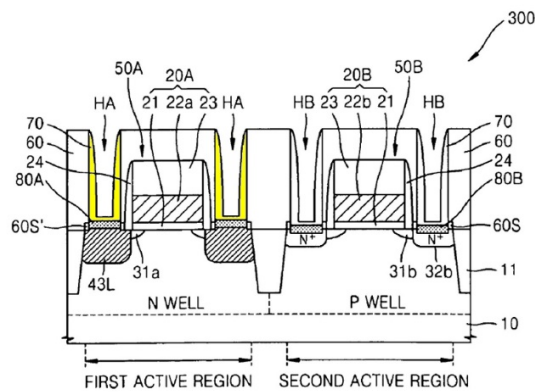
FIG. 3D



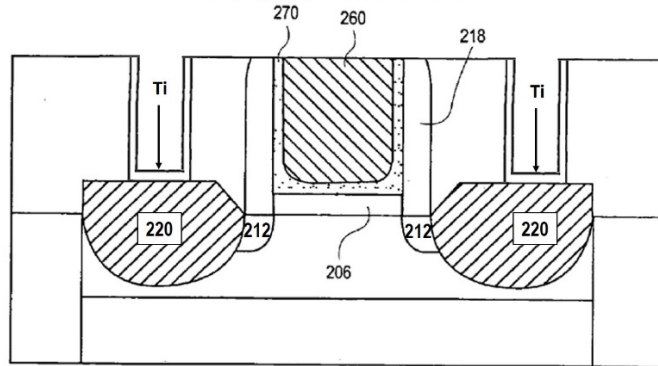
Second, a Ti layer 70 is deposited into contact holes HA, as Figure 3F shows (below left). *Kim* ¶0047, ¶0066. Applied to *Ranade*'s FinFET, it would resemble the figure on the right below. Thompson ¶213, ¶219.

⁶ Admitted prior art. *See* '178 Patent at 2:36-57, 14:3-16, Fig. 7.

FIG. 3F

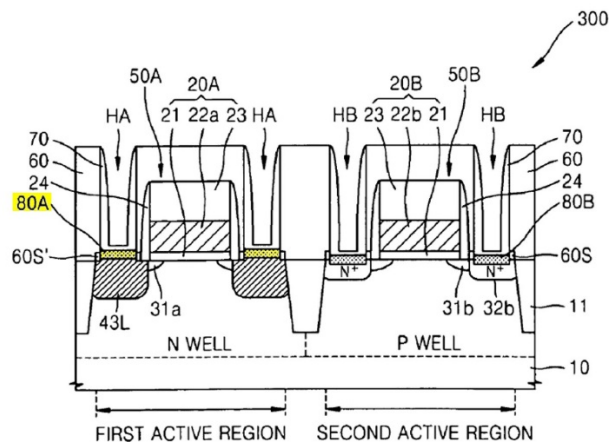


Ranade, FIG. 2N as Modified

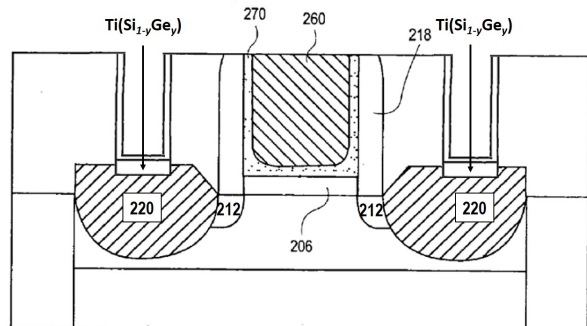


Third, annealing causes Ti layer 70 to chemically react with SiGe source/drain regions 43L to form $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A (below left). *Kim* ¶¶0047-0050, ¶0067. Applied to *Ranade*'s FinFET, a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film likewise would form (below right). Thompson ¶214, ¶220.

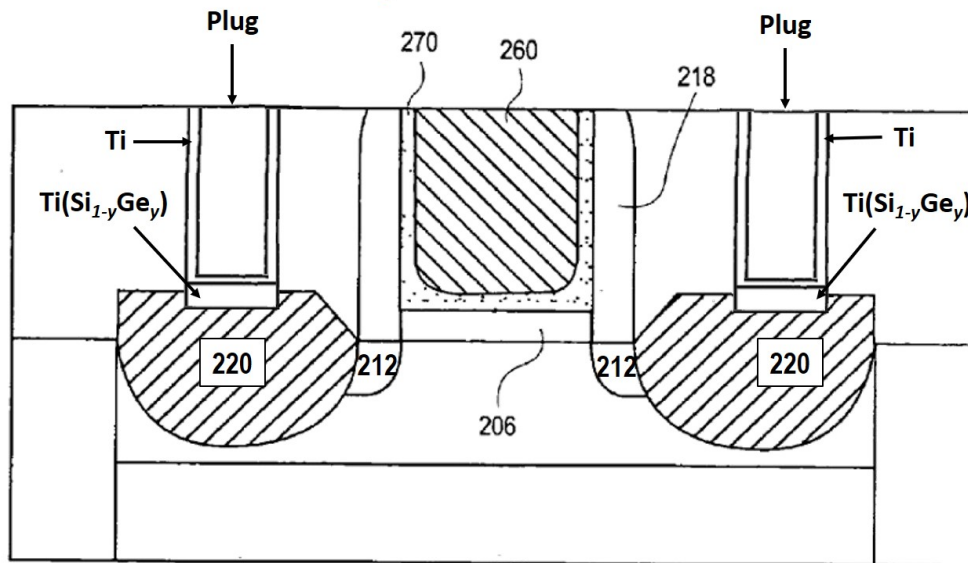
FIG. 3F



Ranade, FIG. 2N as Modified



Fourth, *Kim* teaches forming “contact plugs” on $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A in contact holes HA. *Kim* ¶¶0049, ¶0068. Applied to *Ranade*'s FinFET, it would resemble the figure below. Thompson ¶215, ¶221.

Ranade, FIG. 2N as Modified**Ranade-Kim: Second Obvious Implementation (Direct Metalization)**

Ranade explains its FinFET is completed using “typical process steps to complete the formation of a MOS-FET, ... such as a silicidation step.” *Ranade* ¶¶0041. *Kim* discloses a silicidation step—Direct Metalization. *Kim* ¶¶0047-0050, ¶¶0066-00668, Fig. 3F. A POSITA would have found a combination of *Ranade* and *Kim* resembling the above to be obvious. Thompson ¶222.

d. Rationales for combining *Ranade*’s and *Kim*’s teachings

First, a POSITA would have understood the combinations above combine known elements (*Ranade*’s FinFET and *Kim*’s source/drain contacts) according to known methods (*Kim*’s Ge Overlayer Metalization or Direct Metalization) to yield predictable results (reduced contact resistance). Thompson ¶224.

Second, a POSITA would have understood the combinations above use a known technique (*Kim*'s Ge Overlayer Metalization or Direct Metalization) to improve similar devices (*Ranade*'s and *Kim*'s FinFETs) in the same way (by lowering contact resistance). Thompson ¶225.

Third, a POSITA would have understood the combinations above apply a known technique (*Kim*'s Ge Overlayer Metalization or Direct Metalization) to a known device ready for improvement (*Ranade*'s FinFET) to yield predictable results (reduced contact resistance). Thompson ¶226.

Fourth, a POSITA would have arrived at the combinations above due to a teaching, suggestion, or motivation in the prior art (those in *Ranade* and *Kim* and those discussed in Section III, including the need to reduce contact resistance) to arrive at the claimed invention. Thompson ¶227; *see also Ranade* ¶0038, ¶0041; *Kim* ¶¶0003-0007, ¶0010, ¶0047, ¶0050, ¶¶0071-0074.

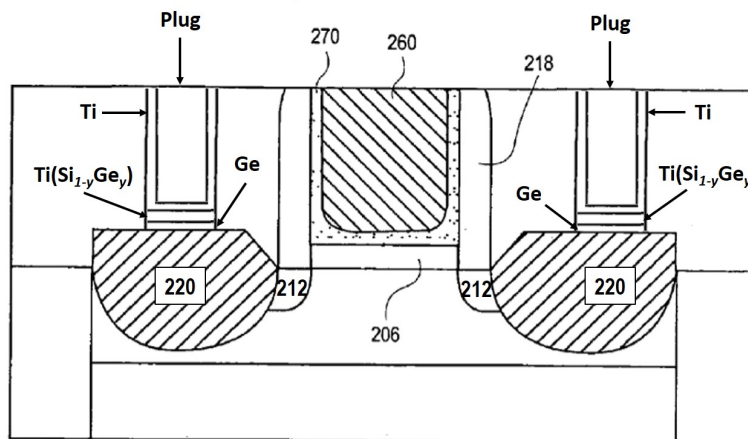
2. Claim 1

Because a POSITA would have wanted to combine *Ranade*'s and *Kim*'s teachings as described above, because a POSITA would have reasonably expected to succeed, and because at least one of the asserted *Ranade-Kim* combinations meets all elements of claim 1, claim 1 is unpatentable. *See Thompson* ¶312.

a. Element [1.0]

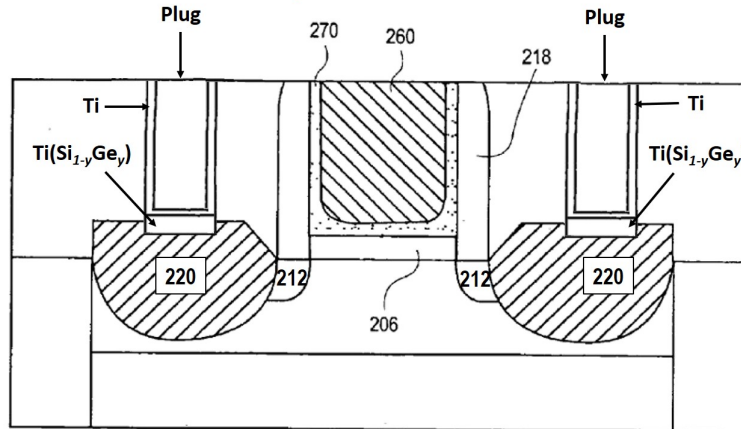
To the extent the preamble is limiting, the *Ranade-Kim* combinations provide “[a]n integrated circuit structure.” Thompson, ¶¶238-240. *Ranade* teaches a non-planar “tri-gate or FIN-FET transistor.” *Ranade* ¶0025, ¶¶0043-0044, Figs. 2N, 3C. Such FinFETs, approximated by the cross-section below, “may be incorporated into an integrated circuit” using “conventional processing steps, as known in the art.” *Id.* ¶0043, ¶0046.

Ranade, FIG. 2N as Modified



Ranade-Kim: First Obvious Combination (Ge Overlayer Metalization)

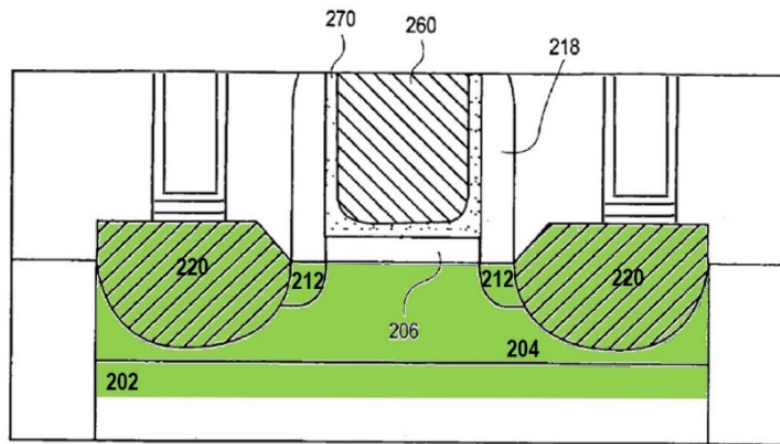
Ranade, FIG. 2N as Modified



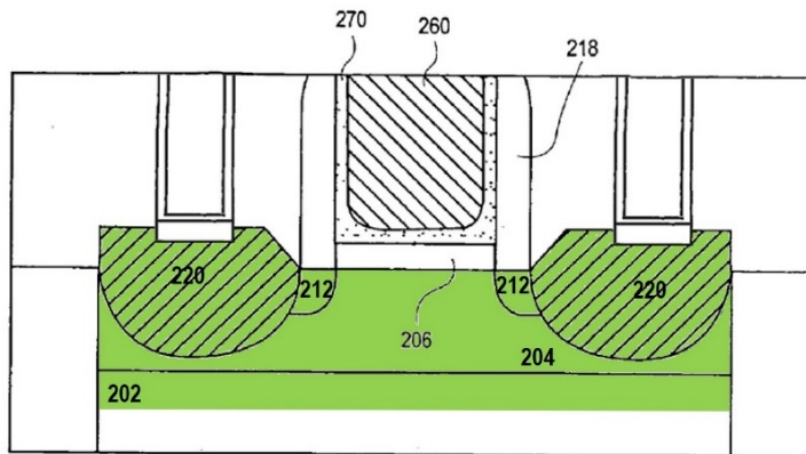
Ranade-Kim: Second Obvious Combination (Direct Metalization)

b. Element [1.1]

The *Ranade-Kim* combinations include “a fin comprising silicon.” Shown in green below, *Ranade* teaches a FinFET with a fin that includes active region 204, epitaxial source/drain regions 220, source/drain tip extensions 212, and part of substrate 202. *Id.* ¶¶245-249.



***Ranade-Kim*: First Obvious Implementation (Ge Overlayer Metalization)**



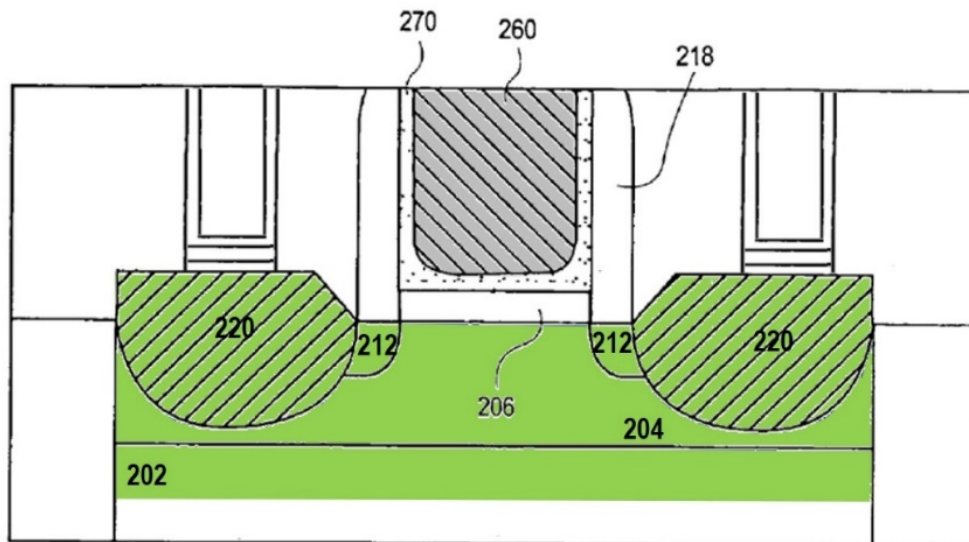
***Ranade-Kim*: Second Obvious Implementation (Direct Metalization)**

Substrate 202 is crystalline silicon or SiGe, and active region 204 and epitaxial source/drain regions 220 are “crystalline silicon/germanium.” *Ranade*

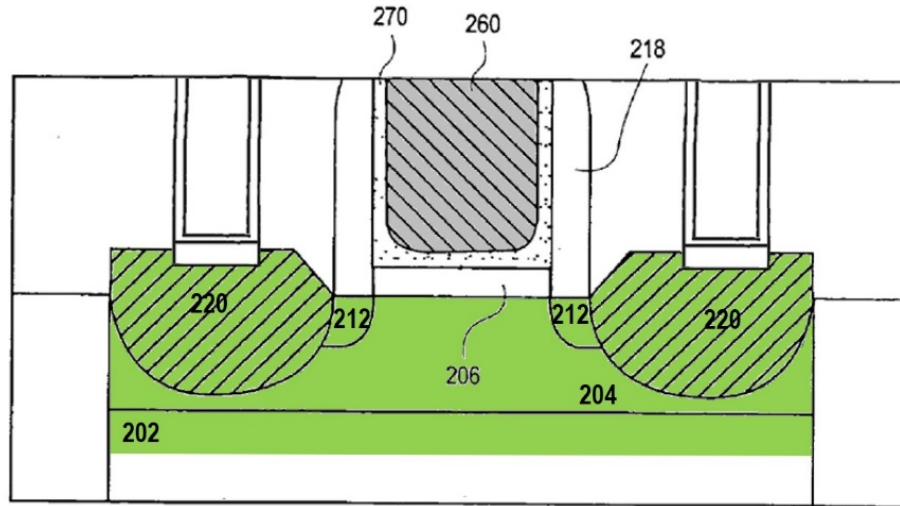
¶¶0026, ¶¶0032, ¶¶0040; *see also id.* ¶¶0016-0017, ¶¶0023. Tip extensions 212 are made of the same material as active region 204 because they are formed “by implanting charge-carrier dopant impurity atoms into active region 204.” *Id.* ¶¶0040. Each of these constituent fin regions (green) comprises silicon.

c. Element [1.2]

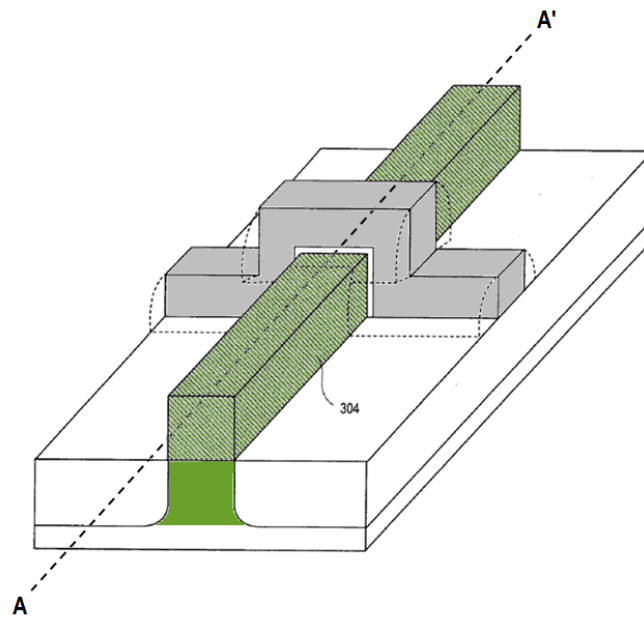
The *Ranade-Kim* combinations include “a gate electrode over the fin.” *Ranade* teaches a gate electrode 208/260/308 over the fin. *Ranade* ¶¶0042; *see also id.* ¶¶0015, ¶¶0018-0020, ¶¶0028-0031, ¶¶0033-0037, ¶¶0041-0042, ¶¶0044-0046, Figs. 1A, 1B, 2B-3C. As the figures below show, the *Ranade-Kim* combinations likewise include a gate electrode (gray) over the fin (green). Thompson ¶¶253-256; *see also Kim* ¶¶0033; Korean *Kim* ¶¶0023.



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



Ranade-Kim: Second Obvious Combination (Direct Metalization)

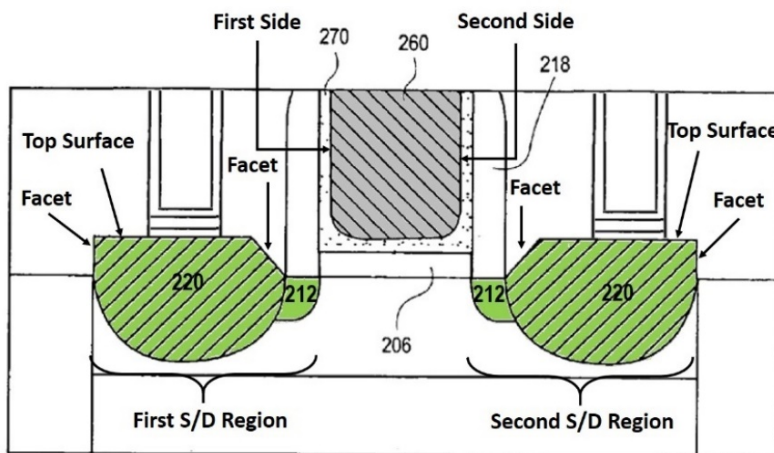


Ranade Fig. 3C⁷

⁷ Figure 3C illustrates a stage of processing analogous to *Ranade*'s Figure 2E (before forming tip extensions 212, source/drain regions 220, ILD 250, or replacement gate 260). Thompson ¶247 & n.288; see also *Ranade* ¶¶0025, ¶¶0032, ¶¶0044-0046, Figs. 2E-2N, 3A-3C.

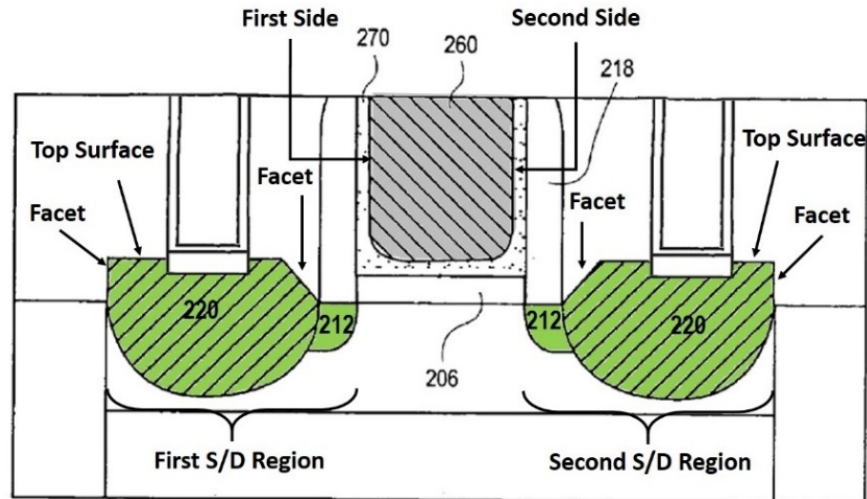
d. Elements [1.3] and [1.6]

The *Ranade-Kim* combinations include “a [first/second] source or drain region in the fin proximate a [first/second] side of the gate electrode, the [first/second] source or drain region comprising two or more facets and a top surface.” *Ranade* teaches epitaxial source/drain regions 220 and source/drain tip extensions 212, which together comprise the claimed source/drain regions (green).⁸ See *Ranade* ¶¶0020-0023, ¶0031, ¶¶0034-0041, ¶¶0044-0046, Figs. 1B, 2G-3C; Thompson ¶259. As these figures show, each source/drain region is proximate to a side of the gate electrode (gray). Thompson ¶259.



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**

⁸ The '178 Patent says “each of the source and drain regions includ[es] a tip region.” '178 Patent at 17:12-17; see also *id.* at 3:30-58, 4:27-43, 8:65-9:10, Figs. 1A, 3A, 5A.

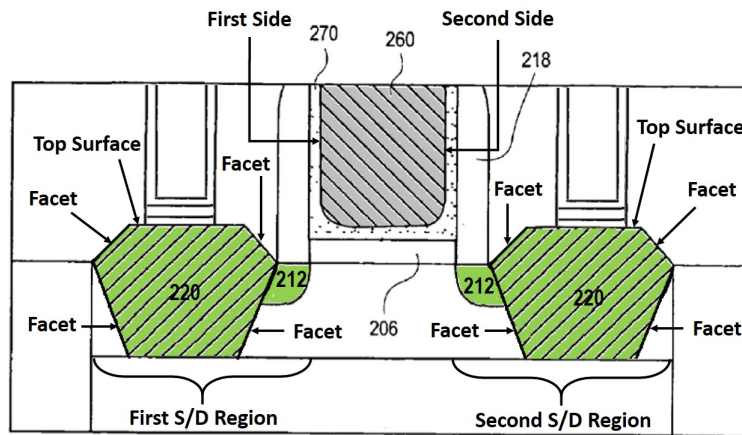


Ranade-Kim: Second Obvious Combination (Direct Metalization)

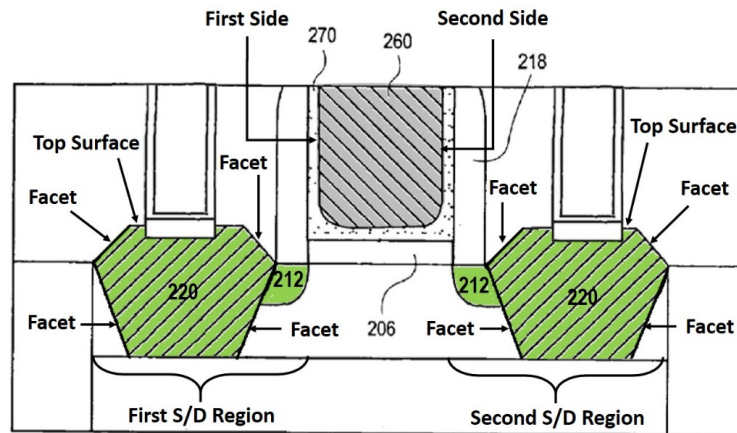
As these figures further illustrate, the *Ranade-Kim* FinFETs include two or more facets and a top surface. Thompson ¶267. A POSITA would have understood “facet” refers to a semiconductor crystal surface. *Id.* ¶261. The ’178 Patent does not actually mention facets; it simply notes the source/drain regions are “epitaxial.” ’178 Patent at 4:20-25, 5:36-44, 13:32-36. So are *Ranade*’s source/drain regions 220. *Ranade* ¶0040. A POSITA would have known that, by definition, epitaxial films are crystalline and terminated by facets. Thompson ¶266.

The '178 Patent also briefly mentions “an ammonia etch to form [a] faceted fin recess” where epitaxial growth takes place. '178 Patent at 7:18-23; *see also id.* at Figs. 3A, 5A. So does *Ranade*. *Ranade* ¶¶0031, ¶¶0038, Figs. 2D', 2J. A POSITA would have understood this ensures <111> crystal facets along the sides of the fin. Thompson ¶¶262-264. As shown above, the source/drain regions (green) in the *Ranade-Kim* combinations comprise epitaxial source/drain regions 220 and

source/drain tip extensions 212, which include at least two facets and a top surface. Thompson ¶267. By applying *Ranade's* ammonia etch (which *Ranade* expressly does not illustrate), epitaxial source/drain regions 220 would further include the facets below. *Id.* ¶264, ¶268; *see also Ranade* ¶0031, ¶0038, Figs. 2D', 2J; EX1048 at Fig. 2; EX1049 at Fig. 6.



Ranade-Kim: First Obvious Combination (Ge Overlayer Metalization)

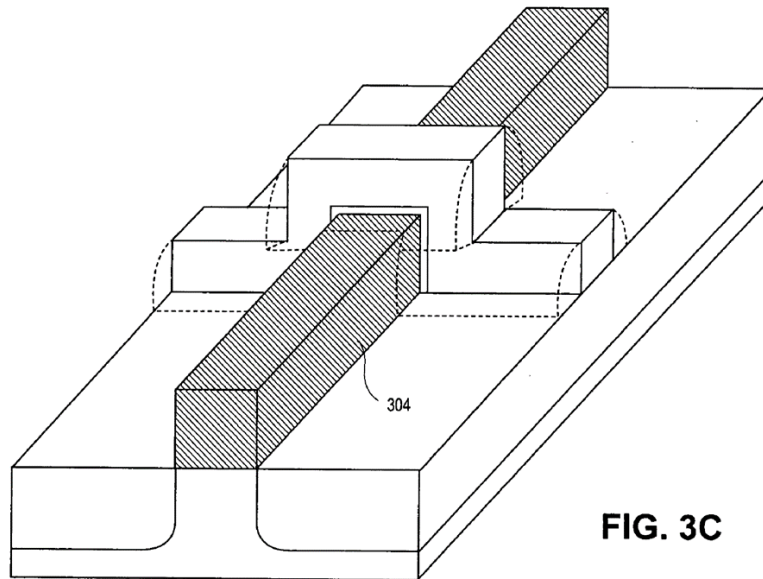


Ranade-Kim: Second Obvious Combination (Direct Metalization)

A POSITA would have understood *Ranade's* Figure 3C below shows *Ranade's* FinFET at a stage of processing analogous *Ranade's* Figure 2E.

Thompson ¶260. Faceted epitaxial source/drain regions 220 replace the exposed parts of active region 304 not covered by the gate in the manner described above.

See id.; *Ranade* ¶¶0038-0040, ¶0044, Figs. 2I-2K.



In addition to these express disclosures, a POSITA would have understood epitaxially grown SiGe fin regions have either a faceted diamond shape or a faceted rectangular shape, depending on wafer and channel orientation. *Supra* Section III.E; Thompson ¶265. A POSITA would have understood *Ranade*'s source/drain regions 220 use (100) surface-oriented wafers and “naturally grow in a diamond shape” as illustrated below. EX1041 at 10:25-26; *see also id.* at 1:27-43, 5:21-6:7, 7:42-50, 10:1-40, 10:61-66, 12:12-20, Fig. 5A; EX1043 at Fig. 7b; *supra* Section III.E; Thompson ¶265.

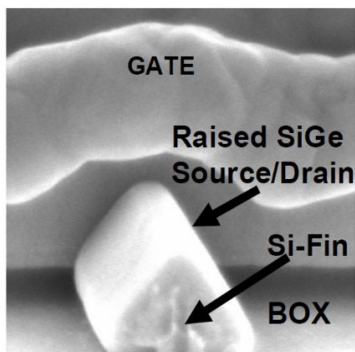
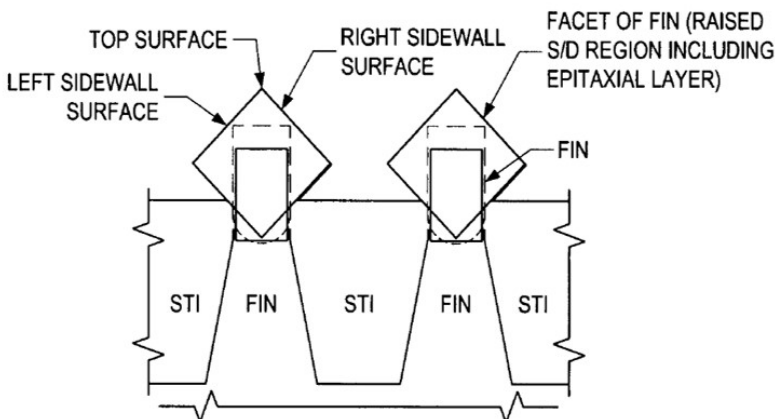


Fig. 7b Y-dir. cross-section of PMOS Trigate with SiGe raised source/drain

EX1043, Fig. 7b



EX1041, Fig. 5A

Thus, in addition to satisfying elements [1.3] and [1.6] based on *Ranade's* express disclosures, a POSITA also would have found it obvious from his or her training and experience. Thompson ¶¶269-270.

e. Elements [1.4] and [1.7]

In the *Ranade-Kim* combinations, “the [first/second] source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%.”

According to *Ranade*, “the pair of source/drain regions 220 comprises a **graded** epitaxial layer,” which “is a crystalline silicon/germanium region of the stoichiometry $\text{Si}_x\text{Ge}_{1-x}$, where $0 \leq x \leq 1$.” *Ranade* ¶0040. Epitaxial source/drain regions 220 thus have a graded Ge concentration ranging anywhere between 0 to 100%. Thompson ¶277. As *Ranade* explains, the Ge concentration in epitaxial source/drain regions 220 is increased from a lower concentration compatible with the Ge concentration in active region 204 (where the channel is) to a higher

concentration to compressively stress the channel. *Ranade* ¶¶0023; *see also id.* ¶¶0039-0040, ¶0064; Thompson ¶273, ¶¶277-278. Active region 204 itself can have up to or more than 50% Ge. *See Ranade* ¶¶0032-0033; Thompson ¶245.

In addition to this express disclosure of source/drain regions 220 graded in excess of 50% Ge, a POSITA would have found it obvious. Thompson ¶279. *Ranade*'s first-named inventor even previously described pFET source/drain regions with "a ~50 nm graded Si_{1-x}Ge_x layer at the interface" that had a "Ge mole fraction varying from 80% at the top surface to 1%" below. EX1051 at 1; *see also id.* at Fig. 1.

First, a POSITA would have known SiGe/Strained Silicon technology was ubiquitous. Thompson ¶¶280-282; *see also supra* Section III.B. For example, Intel's 90 nm, 65 nm, 45 nm, and 32 nm processes (released in 2003, 2005, 2007, and 2009, respectively) all used SiGe/Strained Si technology. Thompson ¶282. And Moore's Law was driving the amount of Ge in the source/drain regions higher over time. Thompson ¶277, ¶293; *see also* EX1013 at 4; EX1014 at 7.

Second, consistent with this trend, a POSITA would have been motivated to grade the Ge concentration in *Ranade*'s source/drain regions 220 to a concentration exceeding 50% to increase strain. Thompson ¶280, ¶¶284-285. A POSITA would have known adding more Ge to the source/drain regions strains the channel more but that generating more strain requires grading to minimize dislocations. *Id.*;

supra Section III.B. Applying both principles, it was known that FET performance “can be improved through implementation of a graded high-germanium content compound, such as a silicon-germanium alloy in the source and drain regions of the transistor.” EX1018 ¶0020; *see also id.* ¶0038, ¶0044, ¶¶0053-0058; *Ranade* at ¶0014, ¶0023, ¶¶0038-0040; *Brask* at 10:20-29; EX1020 at 2-3; EX1012 at Abstract, ¶¶0003-0008, ¶¶0030-0032, ¶0042, ¶0063; EX1019 ¶¶0004-0005, ¶0034, ¶¶0085-0093; EX1050 ¶¶0022-0024; EX1016 at 1:55-63, 2:59-67, 4:56-5:20, Fig. 5b; EX1015 at Abstract, 3:10-5:19, 6:61-7:13, 8:62-10:27; EX1036 at Abstract, ¶0044, ¶0055, ¶¶0084-0094.

Specifically, a POSITA would have wanted to grade the Ge concentration in source/drain regions 220 (green below) in excess of 50% to provide more stress to active region 204 (peach below) where the pFET channel is located.⁹ Thompson ¶¶286-287; *see also Ranade* ¶0023, ¶0039; *supra* Section III.B.

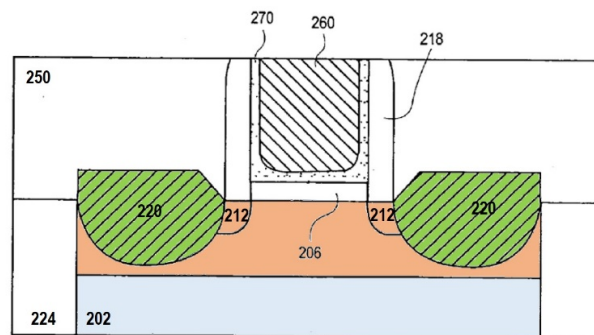
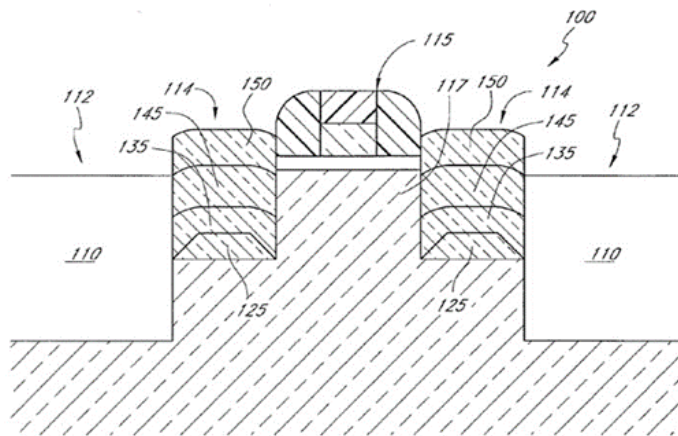


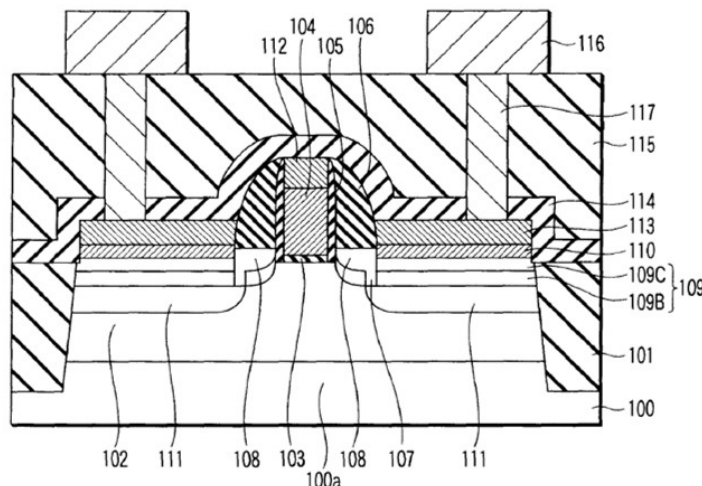
FIG. 2N

⁹ Active region 204 may itself have more than 50% Ge. *Ranade* ¶0023, ¶0032.

As the reference depicted below instructs, Ge grading increases the amount of Ge that can be incorporated into the SiGe crystal without excessive dislocations. EX1012 ¶¶0031-0034, ¶¶0042-0044, Fig. 5D; *see also* Thompson ¶288; *Ranade* ¶0040. For instance, in the figure below “layers 125, 135, 145, etc. may form a continuously graded layer” from as little as “10 atomic %” Ge at the bottom of the source/drain regions to as much as “60 atomic %” or even “100 atomic %” Ge at the top. EX1012 ¶¶0042-0045; Thompson ¶289.



Another exemplary reference confirms the same. *See* Thompson ¶290; EX1019 ¶¶0085-0094, Fig. 16. As shown below, the “germanium concentrations in the silicon germanium layer 109B and the germanium layer 110 are 10 to 30 at % and approximately 100 at %, respectively.” EX1019 ¶0085. Between those layers 109B and 110, layer 109C has a graded Ge concentration that “is approximately 10 to 30 at %” at its lower interface with layer 109B and “approximately 100 at %” at its upper interface with layer 110. *Id.*



These and the other exemplary references, including *Ranade*, confirm it was known to grade epitaxial SiGe source/drain regions from as little as 0% Ge to as much as 100% Ge, including in excess of 50%. Thompson ¶291.

Third, a POSITA would have known that grading the Ge concentration in excess of 50% differs only in degree, not in kind, from grading to a concentration less than 50% and does not yield any new or unexpected results. Thompson ¶280, ¶292. “[E]ven a slight overlap in range establishes a *prima facie* case of obviousness.” *Genentech, Inc. v. Hospira, Inc.*, 946 F.3d 1333, 1341 (Fed. Cir. 2020) (quotation omitted). Here, *Ranade* discloses the entire range. *Ranade* ¶0040. Patent Owner may overcome this “presumption of obviousness” only by showing a “critical” result—a “new and unexpected result which is different in kind and not merely in degree from the results of the prior art.” *DuPont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1006 (Fed. Cir. 2018). Nothing in the ’178 Patent or the literature suggests 50% Ge is “critical” or associated with unexpected results.

Thompson ¶¶294-296. As Dr. Thompson explains, the difference between 50 and 51% Ge, for example, “is negligible (and well within the range of normal process variation).” *Id.* ¶¶295-296.

By failing to distinguish source/drain regions with more than 50% Ge and less than 50% Ge, the '178 Patent confirms the lack of criticality. *See* '178 Patent at 3:50-55 (20-100% Ge), 4:20-25 (10-70% Ge), 6:56-64 (30-70% Ge). The '178 Patent confirms that source/drain regions at any concentration (including more than 50% Ge) can be formed “using any number of conventional techniques.” *Id.* at 4:18-25. The only examples that specifically mention 50% Ge appear in a long list of permutations with no significance attributed to that value. *See id.* at 16:4-18:17. Because a Ge concentration in excess of 50% Ge is not critical, and because there was a known trend towards increasing the Ge concentration, a POSITA would have found claim elements [1.4] and [1.7] obvious. Thompson ¶280, ¶293, ¶297.

In sum, a POSITA would have understood *Ranade* expressly discloses “the [first/second] source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%.” Further, a POSITA would have found this feature obvious based on *Ranade*’s teachings viewed with his or her training, experience, and industry trends. Thompson ¶297.

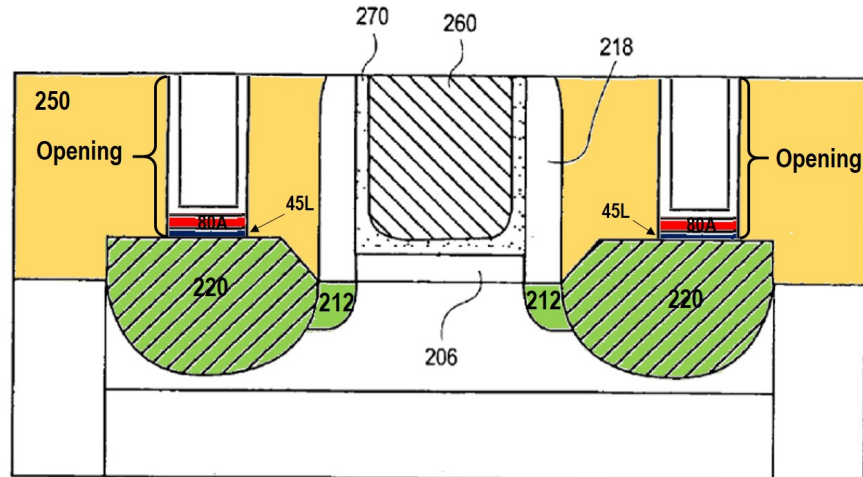
f. Elements [1.5] and [1.8]

Depending how “germanide layer” is construed and how the phrase “over the top surface” is applied, at least one of the asserted *Ranade-Kim* combinations includes “a [first/second] germanide layer over the top surface of the [first/second] source or drain region, the [first/second] germanide layer comprising silicon, germanium and titanium.” Thompson ¶298.

As Section VIII.A.1 explains, a POSITA would have recognized two obvious applications of *Kim*’s teachings to *Ranade*’s FinFET—Ge Overlayer Metalization and Direct Metalization. The Ge Overlayer combination satisfies claim elements [1.5] and [1.8] under either party’s construction of “germanide layer” and any conceivable interpretation of “over the top surface.” *Id.* ¶299. The Direct Metalization combination satisfies claim elements [1.5] and [1.8] under Patent Owner’s construction of “germanide layer” and its apparent interpretation of “over the top surface” (by which a germanide layer partially within a source/drain region is nevertheless “over the top surface” of the source/drain region). *Id.*

i. Ge Overlayer Metalization

The figure below provides an approximate cross-section for the Ge Overlayer Metalization combination. *Supra* Section VIII.A.1.c.i. $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A (red) forms by reacting a Ti layer with a thin Ge Overlayer (dark blue) and atoms diffused from the SiGe source/drain regions (green). Thompson ¶300.



Ranade-Kim: First Obvious Combination (Ge Overlayer Metalization)

Ti(Si_{1-y}Ge_y) film 80A (red) is a “germanide layer” under either party’s proposed construction, and it “compris[es] silicon, germanium, and titanium.” Ti(Si_{1-y}Ge_y) film 80A (red) also satisfies any conceivable interpretation of the phrase “over the top surface of the [first/second] source or drain region” because it lies wholly above the source/drain regions. Thus, the Ge Overlayer Metalization combination satisfies claim elements [1.5] and [1.8]. Thompson ¶¶301-304.

For comparison, annotated Figure 5F of the ’178 Patent appears below.

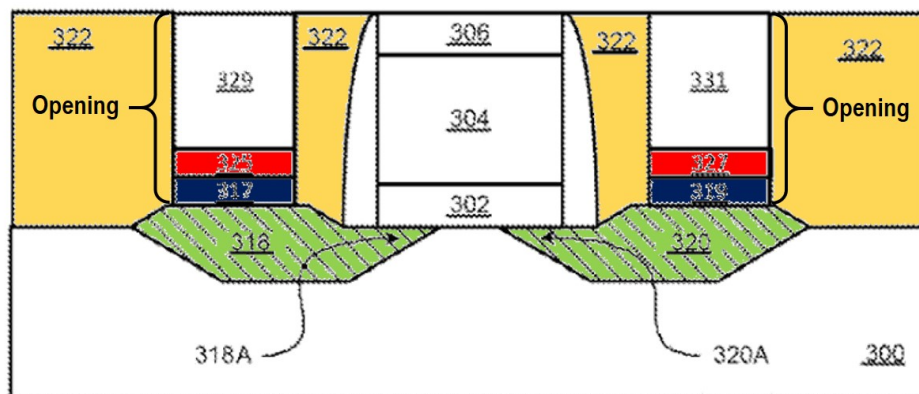
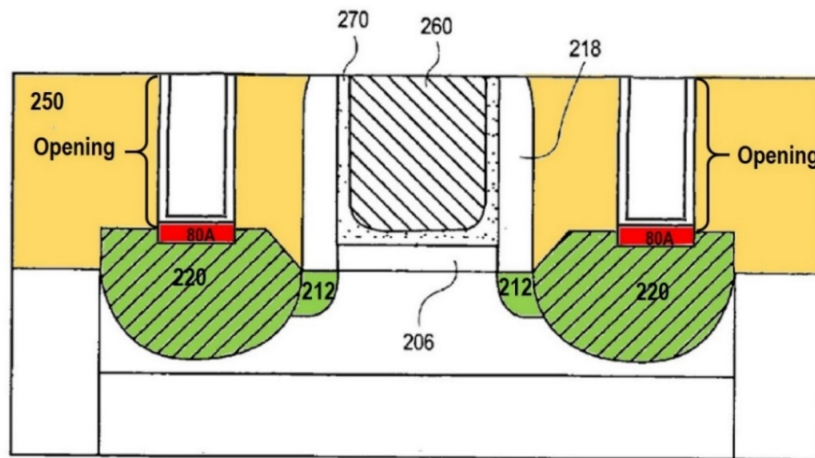


FIG. 5F

ii. Direct Metalization

The figure below provides an approximate cross-section for the Direct Metalization combination. *Supra* Section VIII.A.1.c.ii. $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A (red) forms by chemically reacting *Ranade*'s SiGe source/drain regions (green) with a Ti layer. Thompson ¶305.



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

$\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A (red) is a “thickness of material, comprising germanium and a metal” (Patent Owner’s construction of “germanide layer”), and it “compris[es] silicon, germanium, and titanium.” Also, under Patent Owner’s apparent interpretation of “over the top surface,” it is “over the top surface of the [first/second] source or drain region” because it at least partially extends above the top surface of the source/drain regions. Thus, the Direct Metalization combination satisfies limitations [1.5] and [1.8] under Patent Owner’s proposed construction of “germanide layer” and apparent interpretation of “over the top surface.” Thompson ¶¶306-308.

For comparison, annotated Figure 5F of the '178 Patent appears below.

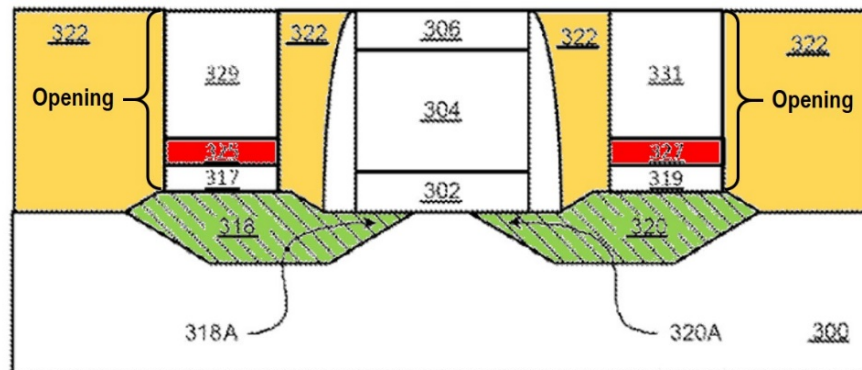


FIG. 5F

3. Claim 2

In the *Ranade-Kim* combinations, “the first and second source or drain regions have a boron concentration greater than 1E20.” *Ranade*’s source/drain regions include tip extensions 212 “formed by implanting charge-carrier dopant impurity atoms into [the] active region.” *Ranade* ¶¶0035; *see also id.* ¶¶0020-0021, ¶¶0035-0038, Figs. 2G-2I; Thompson ¶315; *supra* Section VIII.A.2.d. The source/drain tip extensions are doped with boron. *Ranade* ¶¶0021, ¶¶0035, ¶¶0040; *see also* Thompson ¶316. And their concentration is “in the range of 1E20 atoms/cm³-1E21 atoms/cm³.” *Ranade* ¶¶0035; *see also* Thompson ¶317. Since combining *Ranade* with *Kim* would not alter these teachings, the *Ranade-Kim* combination satisfies claim 2. Thompson ¶¶318-319.

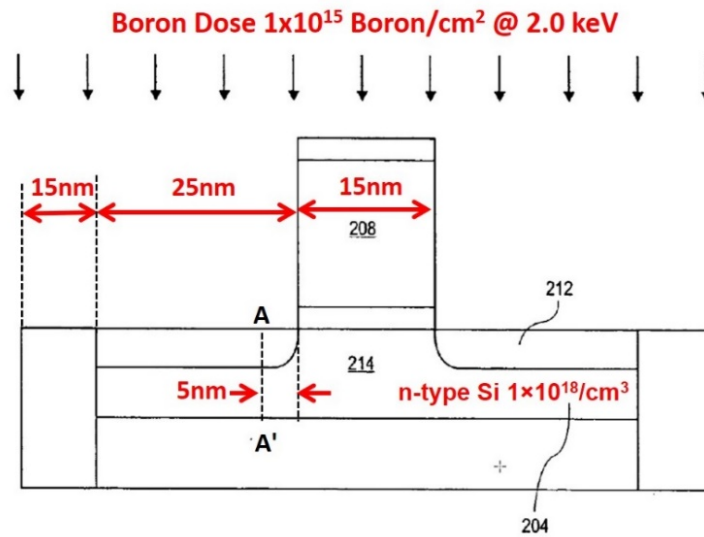
4. Claim 3

In the *Ranade-Kim* combinations, “the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of $1\text{E}20$.”

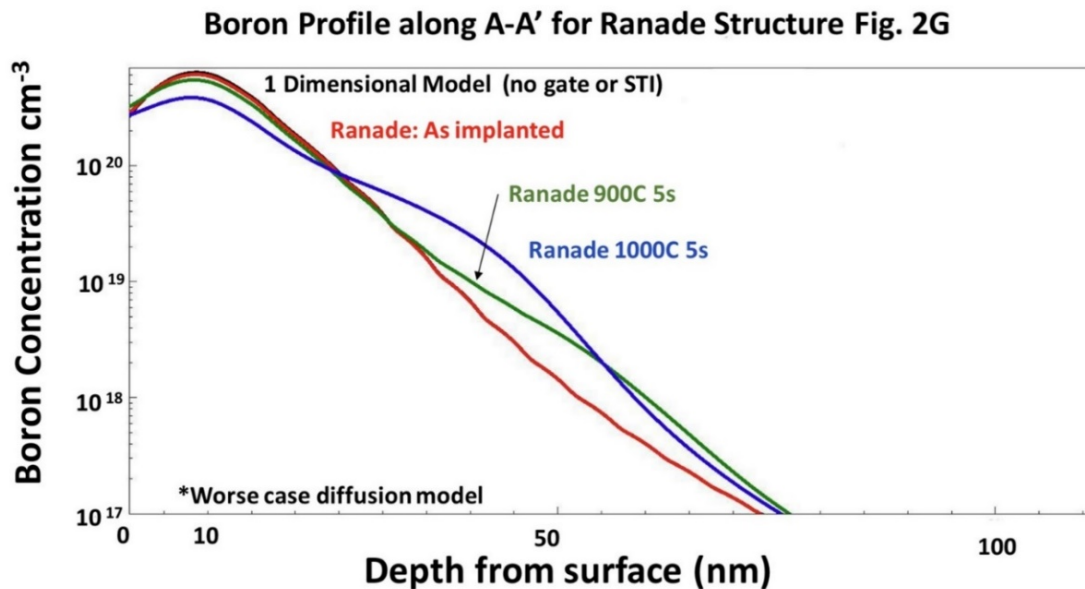
Ranade teaches to dope the pFET source/drain tip extensions 212 with boron by ion implantation. *Ranade* ¶¶0035, ¶¶0040. As Section III.D explains, this necessarily results in a graded boron doping profile. See Thompson ¶¶83, ¶¶323; EX1038 at 7-11. Specifically, *Ranade* teaches to dope source/drain extensions 212 to a level of $1\text{E}20$ to $1\text{E}21$ boron atoms/ cm^3 at a depth of 5 to 30 nm using “an energy in the range of 0.2 keV-10 keV at a dose in the range of $5\text{E}14$ atoms/ cm^2 - $5\text{E}15$ atoms/ cm^2 .” *Ranade* ¶¶0035. A POSITA would have understood this expressly satisfies claim 3. Thompson ¶¶323-324.

Additionally, a prior-art reference need not “expressly spell out” a claimed feature to disclose it if a POSITA “would at once envisage” that feature from the reference’s teachings. *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quotations omitted). That is true here.

Using an industry standard Synopsis tool for simulating ion implantation and annealing, Dr. Thompson simulated *Ranade*’s disclosed ion implantation on Figure 2G below. Thompson ¶¶324-326.

Ranade Fig. 2G as Modeled

Ranade defines source/drain extension regions 212 by implanting the basic structure above (although Dr. Thompson applied typical physical dimensions and channel doping). The graph below shows boron doping profiles along line A–A' (above) for an exemplary dose of $1 \times 10^{15}/\text{cm}^2$ and an energy of 2 keV.



The black curve represents a control simulation—a Si wafer with no gate or isolation structures as in Figure 2G. Thompson ¶325. The colored curves show results of modeling Figure 2G above. The red curve shows the boron profile as implanted. *Id.* The green curve shows the boron profile after annealing at 900°C for 5 seconds. *Id.* And the blue curve shows the boron profile after annealing at 1000°C for 5 seconds. *Id.* Dr. Thompson considers these “worst case” anneals where SCEs become intolerable. *Id.*

These conditions are exemplary of *Ranade*’s disclosed conditions (dose between $5 \times 10^{14}/\text{cm}^2$ and $5 \times 10^{15}/\text{cm}^2$ and energy between 0.2 and 10 keV). So are the resulting boron profiles (peak concentration between $1 \times 10^{20}/\text{cm}^3$ and $1 \times 10^{21}/\text{cm}^3$ at a depth between 5 to 30 nm). As the exemplary graph above illustrates, the boron concentration is graded from a base level to a peak between about $4 \times 10^{20}/\text{cm}^3$ to $6 \times 10^{20}/\text{cm}^3$ at a depth of about 10 nm. Thompson ¶326. When *Ranade* teaches a peak between $1\text{E}20$ and $1\text{E}21$ boron atoms/ cm^3 located 5 to 30 nm below the surface, such profiles are what a POSITA would have immediately envisioned. *See id.*; *Ranade* ¶0035; EX1038 at Fig. 8.13.

The literature agrees. The graph below, for example, illustrates a dose of $1\text{E}15/\text{cm}^2$ at 5 keV and a 7° tilt angle for SiGe with 0, 20, 40, and 60% Ge. EX1039 at Fig. 4.5; *see also* Thompson ¶327; EX1051 at 1, Figs. 1, 2; EX1034 at Figs. 1, 2, 5; EX1035 at Fig. 9; EX1052 at 1, Fig. 2.

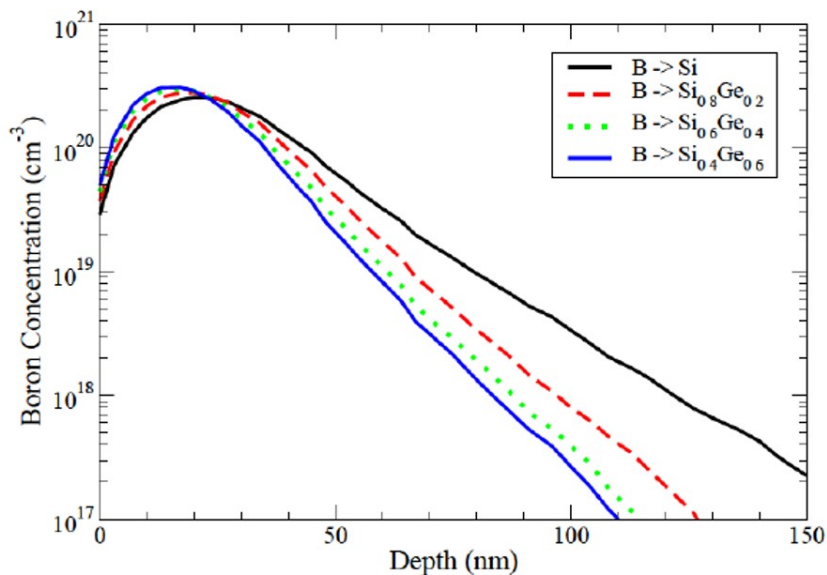


Figure 4.5: Simulated 5keV boron profiles in (100) $\text{Si}_{1-x}\text{Ge}_x$ with $x = 0, 20\%, 40\%, 60\%$ using a dose of 10^{15}cm^{-2} and a tilt of 7° .

EX1039, Fig. 4.5

Thus, because a POSITA would immediately envisage profiles like the ones above based on the profile *Ranade* discloses, a POSITA would have understood the source/drain tip extensions in the *Ranade-Brask* combination satisfy claim 3. Thompson ¶¶322-328. In the alternative, claim 3 would have been obvious based on the same disclosures, and because such grading was known to prevent SCEs and help reduce contact resistance. *See supra* Section III.D; Thompson ¶¶329-332.

5. Claim 4

In the *Ranade-Kim* combinations, “the fin comprises a strained channel between the first and second source or drain regions.” *Ranade* teaches that “source/drain regions 220 have a composition different from the composition of the semiconductor material of active region 204 and impart a uniaxial strain to

channel region 214.” *Ranade* ¶¶0040; *see also id.* ¶¶0023, ¶¶0025, ¶¶0039, ¶¶0044, ¶¶0047, ¶¶0064; Thompson ¶342. Since the application of *Kim*’s teachings does not disturb this aspect of *Ranade*’s FinFET, the combination satisfies claim 4. *Id.* ¶¶343-344.

6. Claim 5

In the *Ranade-Kim* combinations, “the first and second source or drain regions are P-type.” *Ranade*’s FinFET “may be an N-type or a P-type” device and “both N—and P-channel transistors may be fabricated in a single substrate or epitaxial layer to form a CMOS integrated circuit.” *Ranade* ¶¶0043; *see also id.* ¶¶0044. A POSITA would have understood P-type FETs have P-type source/drain regions. Thompson ¶¶347-349.

7. Claim 6

Claim 6 is identical to claim 1, except limitations [6.1]-[6.3], and [6.6], recite a “body” instead of a “fin.” The ’178 Patent uses the term “body” only once, equating it with a “fin.” ’178 Patent at 13:24-27; *see also* Thompson ¶351; *Brask* at 5:26-30, 18:3-16, Figs. 3, 5I. Thus, a POSITA would have understood there is no meaningful difference between claims 1 and 6, and at least one of the asserted *Ranade-Kim* combinations satisfies claim 6 for the reasons in Sections VIII.A.2.a-f. Thompson ¶¶350-359; *see also Mycogen Plant Sci., Inc. v. Monsanto Co.*, 243 F.3d 1316, 1329 (Fed. Cir. 2001) (“It is not unusual that separate claims

may define the invention using different terminology, especially where (as here) independent claims are involved.”).

8. Claim 7

At least one of the *Ranade-Kim* combinations satisfies claim 7 for the reasons in Section VIII.A.3. *See* Thompson ¶¶360-362.

9. Claim 8

At least one of the *Ranade-Kim* combinations satisfies claim 8 for the reasons in Section VIII.A.4. *See* Thompson ¶¶363-365.

10. Claim 9

At least one of the *Ranade-Kim* combinations satisfies claim 9 for the reasons in Section VIII.A.5. *See* Thompson ¶¶366-368.

11. Claim 10

At least one of the *Ranade-Kim* combinations satisfies claim 10 for the reasons in Section VIII.A.6. *See* Thompson ¶¶369-371.

12. Claims 11-20

At least one of the *Ranade-Kim* combinations satisfies claims 11-20 for the reasons in Section VIII.C *infra*.

B. Ground 2A: The *Tung-Brask* Combination**1. A POSITA Would Have Found the *Tung-Brask* Combination Obvious****a. A POSITA would have found it obvious to use *Brask*'s graded source/drain region in *Tung*'s FinFET**

Tung teaches “structures and methods of fabrication thereof with low resistance contacts for non-planar semiconductor structures” (FinFETs). *Tung* ¶0006; *see also id.* ¶0005, ¶0021, ¶¶0027-0032, ¶0034, ¶0039, ¶0061. Over each fin 28 lies a semiconductor material 51, a doped semiconductor layer 55, and a metal-semiconductor contact layer 59. *Supra* Section VII.C. As explained below, a POSITA would have found it obvious to grade the Ge concentration of *Tung*'s SiGe semiconductor material 51 from a level compatible with the underlying Si fin 28 to a level compatible with the overlying doped SiGe or Ge semiconductor layer 55. *See* Thompson ¶¶527-528; EX1018 ¶0020, ¶0038, ¶0044, ¶¶0053-0058; EX1019 ¶¶0004-0005, ¶0034, ¶¶0085-0094; EX1012 at Abstract, ¶¶0003-0008, ¶¶0030-0032, ¶0042, ¶0063; EX1050 ¶¶0022-0024; EX1021 ¶¶0059-0060.

Tung teaches a FinFET that begins with a fin region 28 made of silicon (below). *Tung* ¶¶0048-0051, Figs. 6a-6b.

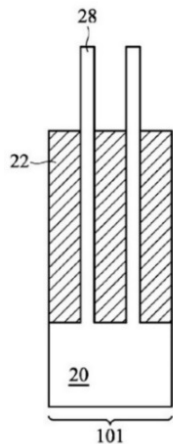


FIG. 6a

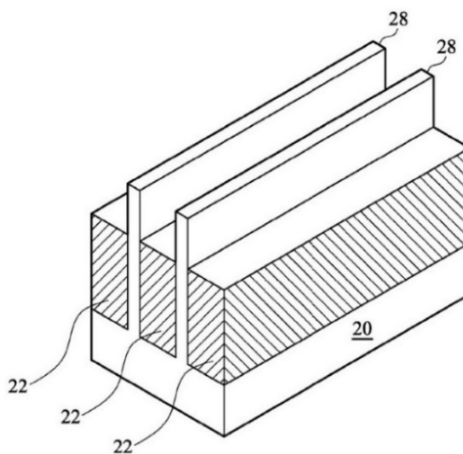


FIG. 6b

To form *Tung*'s source/drain regions, SiGe semiconductor material 51 selectively grows over fin 28 as in Figure 4b below. *Id.* ¶¶0040, ¶¶0074, ¶¶0076. A doped semiconductor layer 55 (e.g., SiGe or Ge) then selectively grows over SiGe layer 51 as in Figure 4c below. *Id.* ¶¶0034, ¶¶0041, ¶¶0058, ¶¶0078. After depositing a metal layer 57 (e.g., Ti) over doped semiconductor layer 55 as in Figure 4d below, the structure is annealed so metal layer 57 “reacts with the doped semiconductor layer 55” to form a metal-semiconductor layer 59 (e.g., TiSiGe) as in Figure 4e. *Id.* ¶¶0041-0043, ¶¶0045, ¶¶0061-0064, ¶¶0080-0081; *see also* Thompson ¶¶529-533.

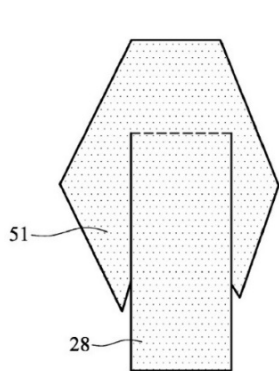


FIG. 4b

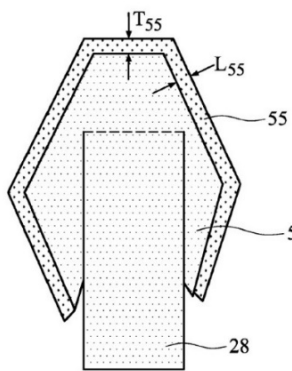


FIG. 4c

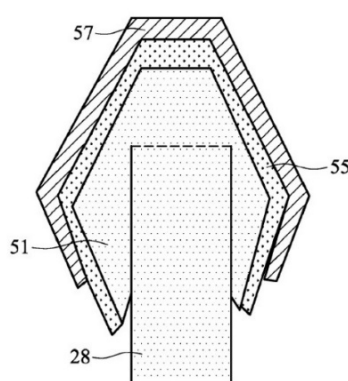


FIG. 4d

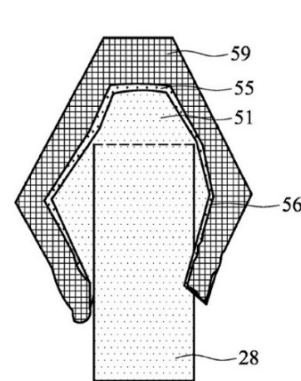


FIG. 4e

Because the interface between doped semiconductor layer 55 and metal-semiconductor layer 59 defines the Schottky barrier height and “determines the source/drain series resistance of the transistor,” *Tung* ¶0034, a POSITA would have desired using more than about 85% Ge in doped semiconductor layer 55 to minimize contact resistance. *See* Thompson ¶¶538-540; *supra* Section III.C. *Tung* expressly teaches that layer 55 may be “doped SiGe, or doped Ge.” *Tung* ¶0058, ¶0078.

Since a POSITA would have wanted to use such a large amount of Ge in doped semiconductor layer 55 to minimize contact resistance, he or she would have understood from basic principles of epitaxy that SiGe layer 51 should be graded from a Ge amount compatible with underlying fin 28 to an amount compatible with doped semiconductor layer 55. Thompson ¶¶545-546; *see also supra* Section III.B; EX1018 ¶0020, ¶0038, ¶0044, ¶¶0053-0058; EX1019 ¶¶0004-0005, ¶0034, ¶¶0085-0094; EX1012 at Abstract, ¶¶0003-0008, ¶¶0030-0032, ¶0042, ¶0063; EX1050 ¶¶0022-0024; EX1021 ¶¶0059-0060.

Brask expressly discloses such a layer. Specifically, *Brask* discloses a $\text{Si}_x\text{Ge}_{1-x}$ semiconductor film 410 ($0 \leq x \leq 0.99$) on fins 330/370, which is highly analogous to *Tung*’s semiconductor material 51. *Brask* at 10:20-49, Figs. 4A, 4B; *see also* Thompson ¶¶541-544. According to *Brask*, this $\text{Si}_x\text{Ge}_{1-x}$ film may “be graded.” *Brask* at 10:20-29.

As Figures 4A and 4B illustrate below, *Brask* teaches the same basic FinFET as *Tung*. Thompson ¶¶542-543; *see also* EX1011 at 10, Fig. 18; EX1053 at 1-4, Figs. 1-2; EX1043 at 1, Figs. 7a-7b.

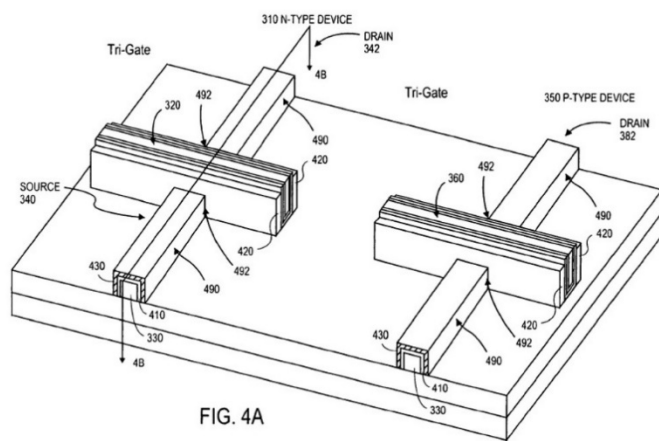


FIG. 4A

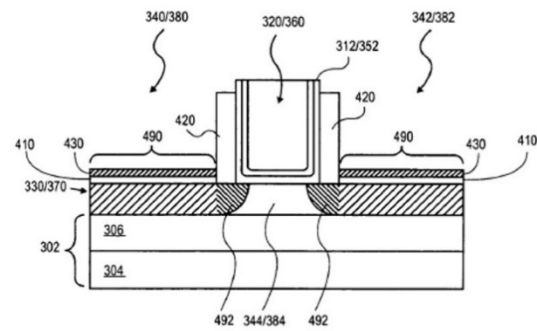


FIG. 4B

Like *Tung*'s fin 28, *Brask*'s FinFET has a silicon fin 330/370. *Tung* ¶¶0048-0052, Figs. 5-6b; *Brask* at 5:30-34, 12:51-56, 15:21-34, Figs. 4A-4B, 5E-5F. Both have source/drain extensions. *Tung* ¶¶0057, ¶¶0073, Figs. 2d, 11c; *Brask* at 9:61-10:11, 11:15-31, Fig. 4B. Both have raised SiGe source/drain regions (*Tung*'s semiconductor material 51 and *Brask*'s semiconductor film 410). *Tung* ¶¶0039-0041, ¶¶0074-0078, Figs. 2a-2d, 4a-4c, 8, 11a-11c, 13-14; *Brask* at 10:20-49, Figs. 4A-4B. And both include a metal-semiconductor contact layer (*Tung*'s layer 59 and *Brask*'s layer 430). *Tung* ¶¶0042-0045, ¶¶0059-0065, ¶¶0079-0081, Figs. 2a-2d, 4d, 4e, 9a-11c, 15-16; *Brask* at 10:50-64, Figs. 4A-4B.

Since their FinFETs are highly analogous, a POSITA would have looked to *Brask*'s teachings to better understand how *Tung*'s SiGe semiconductor layer 51

may be structured. And since *Tung*'s SiGe semiconductor layer 51 corresponds to *Brask*'s semiconductor film 410, a POSITA would have understood its Ge concentration may “be graded” in a range between 1 and 100%. *Brask* at 10:24-29; *see also* Thompson ¶¶543-544.

Tung's SiGe layer 51 sits between a fin region 28 with little or no Ge and semiconductor layer 55 with much more Ge. To avoid unwanted dislocations and preserve strain, a POSITA would have known to grade the Ge concentration of *Tung*'s SiGe layer 51 from an amount compatible with the underlying fin region to an amount compatible with the overlying semiconductor layer. Thompson ¶545. This approach and its benefits were already well-known. *Id.* ¶546; *see also supra* Section III.B; EX1018 ¶0020, ¶0038, ¶0044, ¶¶0053-0058; EX1019 ¶¶0004-0005, ¶0034, ¶¶0085-0094; EX1012 at Abstract, ¶¶0003-0008, ¶¶0030-0032, ¶0042, ¶0063; EX1050 ¶¶0022-0024; EX1021 ¶¶0059-0060.

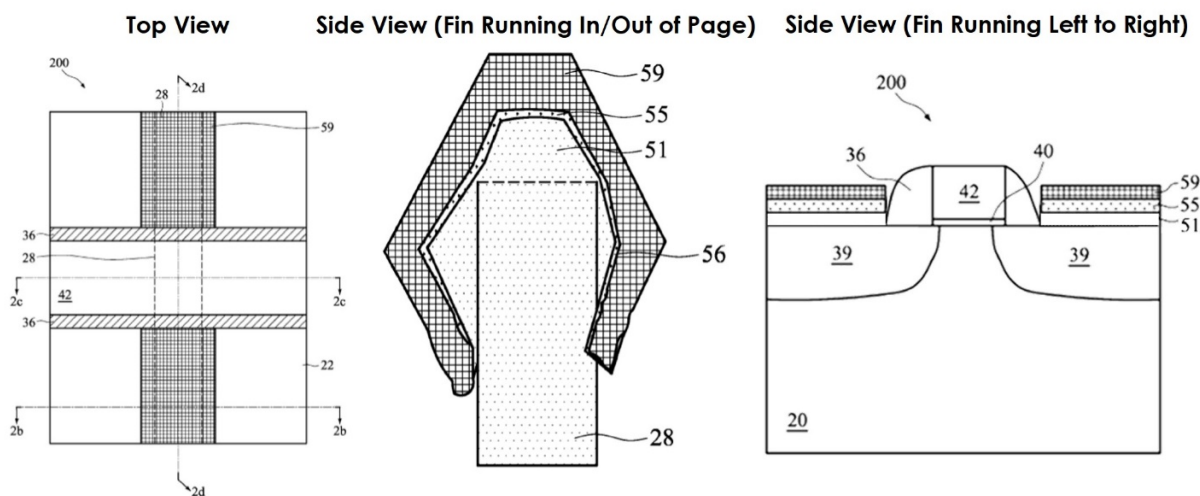
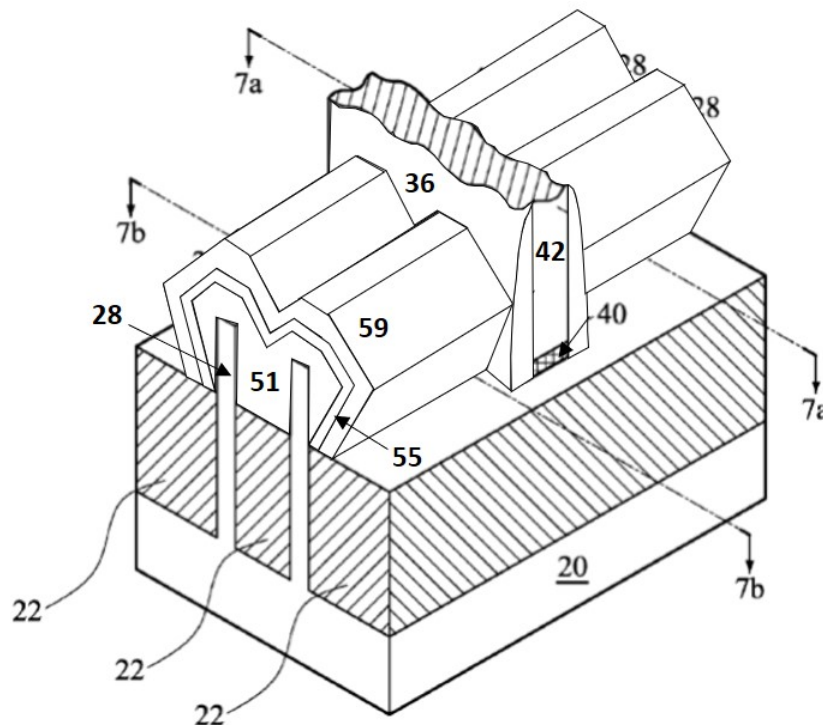


FIG. 2a

FIG. 4e

***Tung-Brask* Combination**

Applying these considerations, a POSITA would have found it obvious to create the structure above. Thompson ¶¶547-548. The left figure (Fig. 2a) shows *Tung*'s device from above. The middle figure (Fig. 4e) shows a side view along the fin (cross-section "2b" in Fig. 2a). And the right figure (Fig. 2d, modified to show SiGe layer 51¹⁰) shows a side view with the fin running left-to-right (cross-section "2d" in Fig. 2a). In an orthographic view, it would resemble the structure below (although the fins might not merge, *see Tung* ¶0058, ¶0078). Thompson ¶547.



¹⁰ See *Tung* ¶0033, ¶0074, Fig. 4e.

b. Rationales for applying *Brask's* teachings to *Tung's* FinFET

First, a POSITA would have understood the combination above combines known elements (*Brask's* graded Ge concentration in raised SiGe source/drain regions and *Tung's* raised source/drain regions) according to known methods (graded SiGe epitaxy) to yield predictable results (low-defect SiGe source/drain regions, a highly strained channel, and low contact resistance). Thompson, ¶550.

Second, a POSITA would have understood the combination above uses a known technique (graded SiGe epitaxy) to improve similar devices (*Tung's* and *Brask's* FinFETs, which include equivalent raised SiGe source/drain regions) in the same way (by minimizing crystal defects, enhancing channel strain, and ensuring low contact resistance). Thompson ¶551.

Third, a POSITA would have understood the combinations above apply a known technique (graded SiGe epitaxy) to a known device ready for improvement (*Tung's* FinFET) to yield predictable results (low-defect SiGe source/drain regions, a highly strained channel, and low contact resistance). Thompson ¶552.

Fourth, a POSITA would have arrived at the combinations above due to a teaching, suggestion, or motivation in the prior art (those in *Tung* and *Brask* and those discussed in Section III, including the desire for a high Ge concentration) to arrive at the claimed invention. Thompson ¶553; *see also Ranade* ¶¶0038-0040; *Brask* at 10:29-49; *supra* Sections III.B, III.C.

2. Claim 1

Because a POSITA would have wanted to combine *Tung*'s and *Brask*'s teachings, because a POSITA would have reasonably expected to succeed, and because the *Tung-Brask* combination meets all elements of claim 1, claim 1 is unpatentable. See Thompson ¶¶596.

a. Element [1.0]

To the extent the preamble is limiting, the *Tung-Brask* combination provides “[a]n integrated circuit structure.” *Tung* describes FinFET “[s]emiconductor devices [that] comprise integrated circuits.” *Tung* ¶0003. As Section VIII.B.1 explains, a POSITA would have found it obvious to apply *Brask*'s teachings to *Tung*'s FinFET (below), which is an integrated circuit structure. Thompson ¶¶563-566.

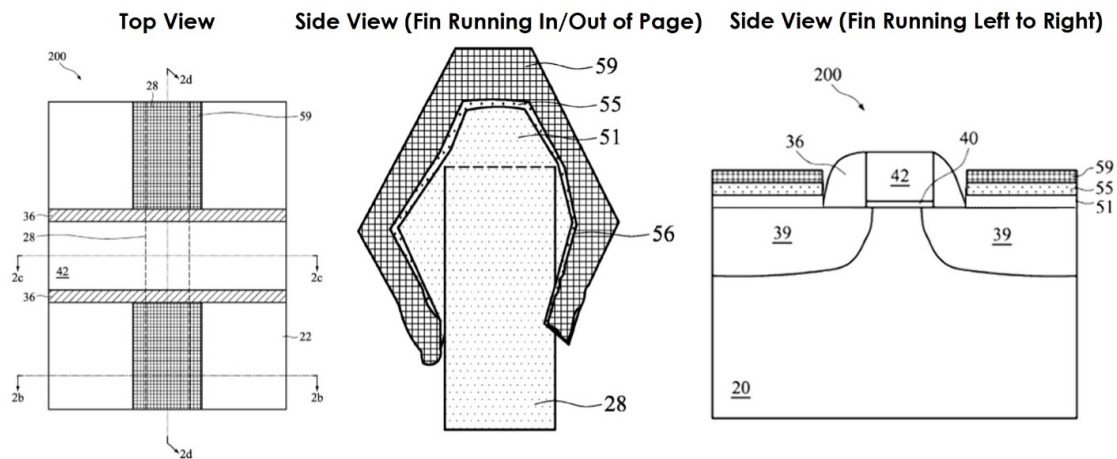
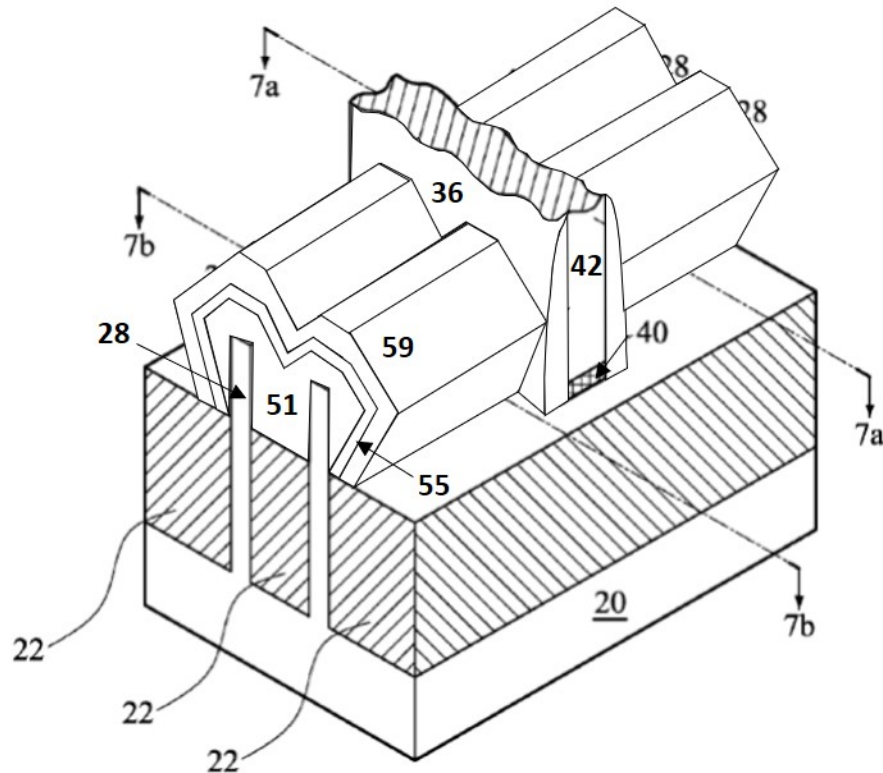


FIG. 2a

FIG. 4e

Tung-Brask Combination



Tung-Brask Combination

b. Element [1.1]

The *Tung-Brask* combination includes “a fin comprising silicon.” The claimed fin (green below) comprises fin 28 (e.g., Si), semiconductor material 51 (graded SiGe), and doped semiconductor layer 55 (e.g., >85% Ge or even pure Ge). *Tung* ¶¶0048-0051, ¶0058, ¶0074, ¶0078; *see also* Thompson ¶¶76-80, ¶¶539-540, ¶545, ¶568; *supra* Section III.C. Because each constituent portion of the fin includes silicon, the fin comprises silicon. Thompson ¶¶568-569.

Side View (Fin Running In/Out of Page)

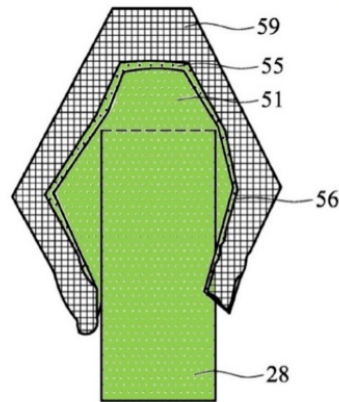
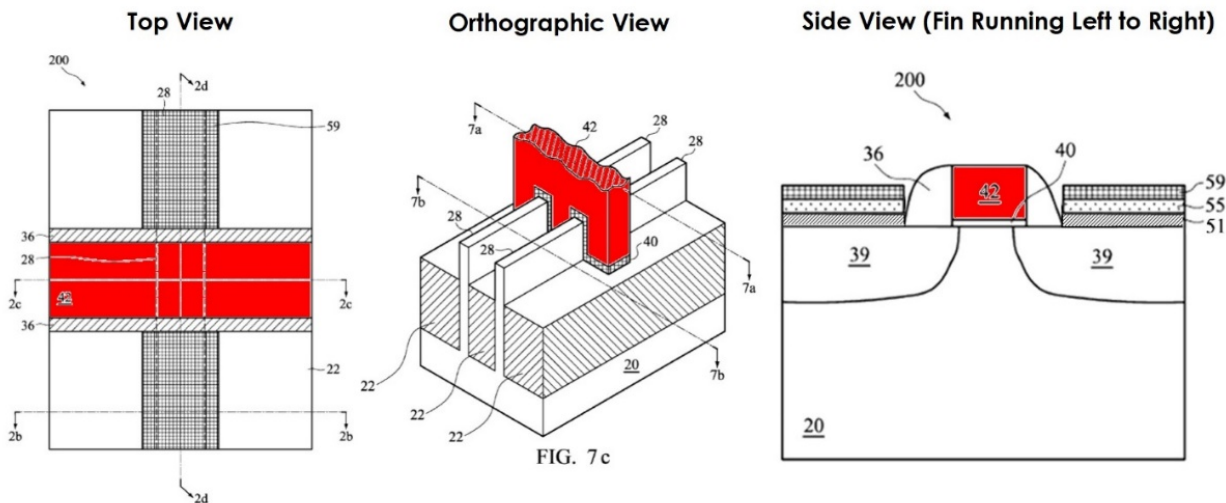


FIG. 4e

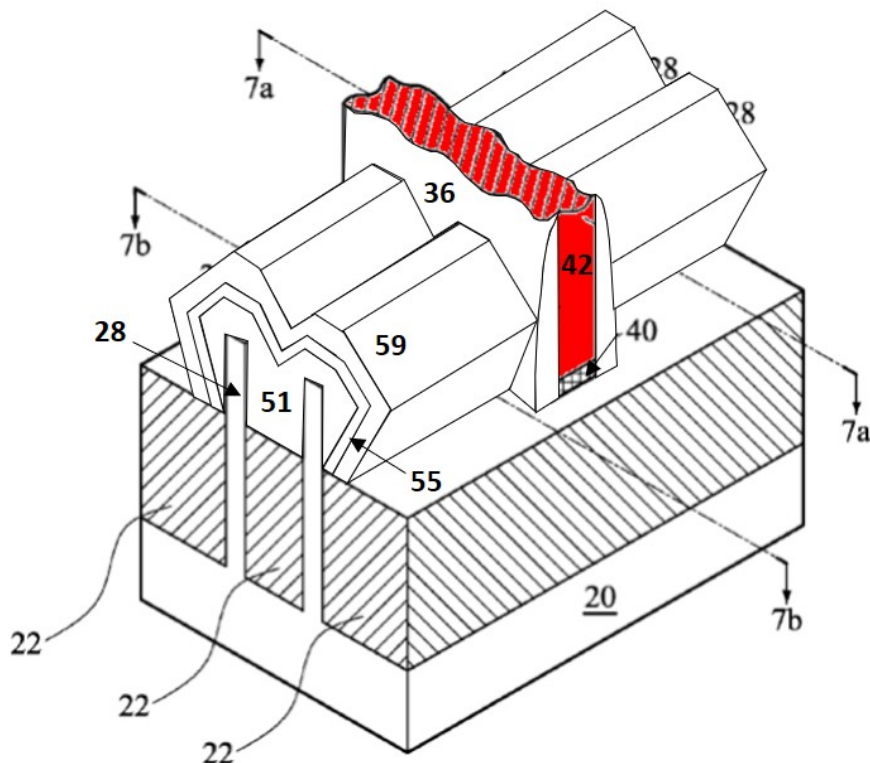
c. Element [1.2]

The *Tung-Brask* combination includes “a gate electrode over the fin.” As the images below show, “[a] gate electrode 42 [red] is disposed over the fin 28.” *Tung* ¶¶0023; *see also id.* ¶¶0033, ¶¶0053-0055, Figs. 2a, 2d, 7a, 7c, 11c; Thompson ¶¶571-573.



Tung-Brask Combination

The figure in the middle above represents the *Tung-Brask* combination as it would appear earlier in manufacturing than in the other two figures. The equivalent image at the later stage of processing would resemble the structure below (although the fins might not merge, see *Tung* ¶0058, ¶0078). Thompson ¶572.



Gate electrode 42 (red) lies over the fin. *Id.* ¶573.

d. Elements [1.3] and [1.6]

The *Tung-Brask* combination includes “a [first/second] source or drain region in the fin proximate a [first/second] side of the gate electrode, the [first/second] source or drain region comprising two or more facets and a top surface.”

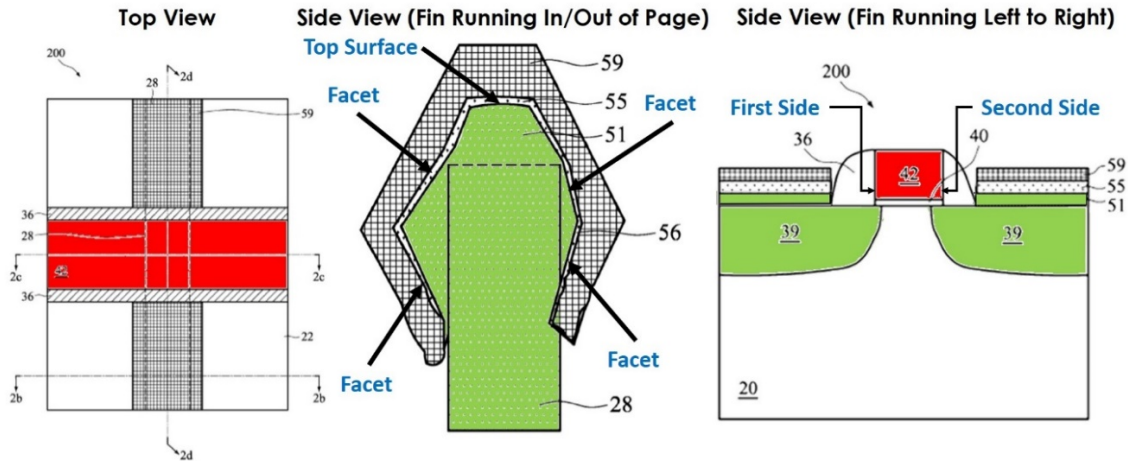


FIG. 2a

FIG. 4e

Tung-Brask Combination

Each “source or drain region” in the *Tung-Brask* combination has at least two components. First, *Tung* teaches “source/drain regions 39 ... disposed within the *fin*s 28.” *Tung* ¶0033. This includes source/drain extension regions (not identified by number but extending under gate spacers 36).¹¹ *Id.* ¶0057, ¶0073. Second, *Tung* teaches *semiconductor material 51* is a “raised source/drain” region of “source/drain regions 39.” *Id.* ¶0074; *see also id.* ¶0033, ¶0072, ¶0075. The figures above illustrate the claimed source/drain regions (green),¹² each proximate

¹¹ *See supra* note 8.

¹² Optionally, *doped semiconductor layer 55* may be considered a third part of each claimed “source or drain region.” Thompson ¶576 & n.575; *Tung* ¶0033.

to one side of the gate electrode (red). Thompson ¶¶575-576; *see also Tung* ¶0033, ¶0074, Figs. 2a, 2d, 7c, 11c.

As the figures further illustrate, the *Tung-Brask* FinFETs include two or more facets and a top surface. Thompson ¶¶577-578. A POSITA would have understood that a “facet” refers to a semiconductor crystal surface. *Id.* ¶577. Since semiconductor material 51 (SiGe) is epitaxial, it is, by definition, crystalline and terminated by facets. *Id.* ¶578; *see also Tung* ¶¶0040-0041, ¶¶0057-0058, ¶¶0074-0075, ¶0078.

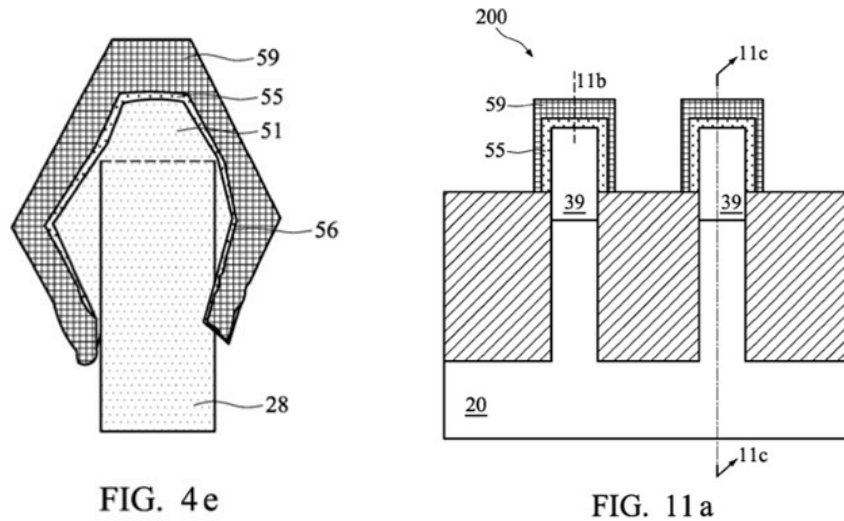
Tung also makes clear that semiconductor material 51 (SiGe) grows “at different rates on different crystal planes” and that the fin “form[s] facets” with a diamond shape as in Figures 4b-4e. *Tung* ¶0040, ¶0078; *see also Thompson* ¶578. Semiconductor material 51 is shown above with four facets along (111) crystal planes and a top surface aligned with a (100) crystal plane.¹³ *Tung* ¶0040; *see also Thompson* ¶578; *supra* Section III.E.

e. Elements [1.4] and [1.7]

In the *Tung-Brask* combination, “the [first/second] source or drain region comprises silicon and germanium having a germanium concentration graded to a

¹³ A POSITA would have known grading the Ge concentration, as *Brask* instructs, would not change this. Thompson ¶578.

concentration in excess of 50%.” As Figures 4e and 11a illustrate, “semiconductor material 51 forms the source/drain regions 39 (raised source/drain)” and “is formed of a material different from that of substrate 20, for example, silicon germanium (SiGe).” *Tung ¶0074; see also id. ¶0033, ¶0040, ¶¶0057-0058, ¶¶0074-0078, Figs. 4b-4e, 11a, 13-16.*



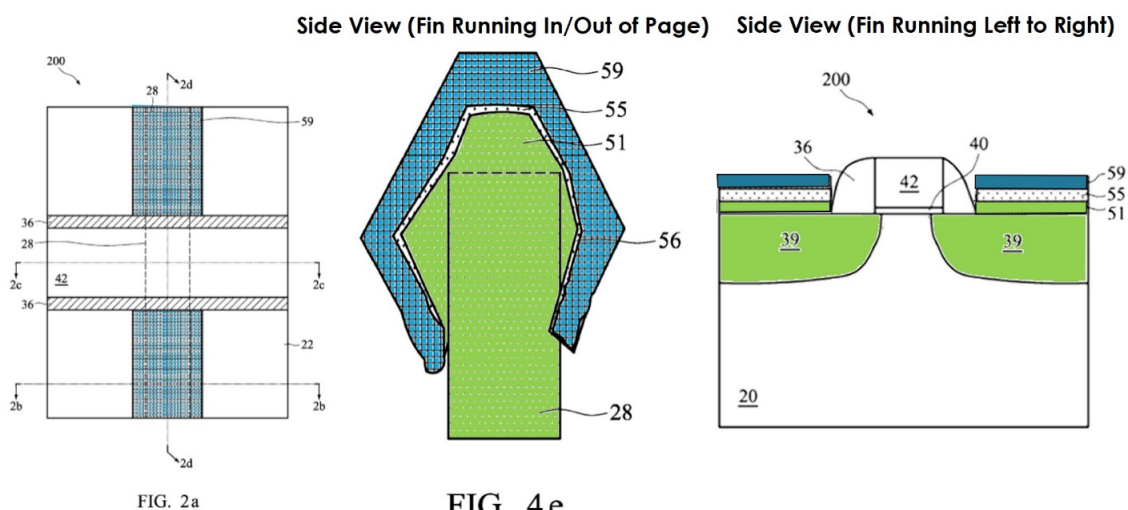
When implemented in the *Tung-Brask* combination, the Ge concentration of SiGe semiconductor material 51 is graded in excess of 50%. As Section VIII.B.1.a explains, a POSITA would have found it obvious from basic strain engineering principles and *Brask* (because *Brask*'s SiGe raised source/drain layer 410 corresponds to *Tung*'s SiGe raised source/drain layer 51 and can be graded over a range between 1 and 100% Ge) to grade the Ge concentration of *Tung*'s semiconductor material 51 from a level compatible with the underlying fin 28 to a level compatible with the overlying doped semiconductor layer 55 (e.g., >85%

Ge), thereby exceeding 50%. Thompson ¶¶581-584; *see also Tung* ¶0058, ¶0078; *Brask* at 10:20-29; EX1019 ¶0042, ¶¶0085-0092; *supra* Section III.B.

Additionally, there is a presumption of obviousness since *Brask*'s disclosed range of 1 to 100% Ge encompasses the claimed range of >50% Ge. *See DuPont*, 904 F.3d at 1006. As Section VIII.A.2.e explains, these ranges differ only in degree, not in kind, and the claimed range does not yield new or unexpected results. Thompson ¶¶292-296; *see also Genentech*, 946 F.3d at 1341.

f. Elements [1.5] and [1.8]

The *Tung-Brask* combination includes “a [first/second] germanide layer over the top surface of the [first/second] source or drain region, the [first/second] germanide layer comprising silicon, germanium and titanium.” The annotated figures below confirm a germanide layer (blue) lies over the top surface of the source/drain regions (green). Thompson ¶¶586-591.



***Tung-Brask* Combination**

Tung's "doped semiconductor layer 55 comprises ... doped SiGe, or doped Ge." *Tung* ¶¶0058, 0078. As Section III.C explains, a POSITA would have found it obvious to use such a layer with >85% Ge to minimize contact resistance. Thompson ¶¶76-80, ¶¶539-540, ¶545, ¶548. *Tung* further explains "metal 57 comprises a suitable metal," such as "Ti," and "is deposited over the doped semiconductor layer 55." *Tung* ¶0042, ¶¶0060-0061, ¶0080. During annealing, the metal atoms in layer 57 react with the semiconductor atoms in doped semiconductor layer 55 (and atoms diffused from semiconductor material 51 when layer 55 is thin enough). *Id.* ¶¶0041-0045, ¶¶0063-0065, ¶0081; *see also* Thompson ¶586; EX1054 at 4-6, Fig. 1; EX1055 at 2-3, Fig. 5. Thus, a TiSiGe layer 59 forms. Thompson ¶586. TiSiGe layer 59 (blue above) is a germanide layer,¹⁴ and it comprises Ge, Si, and Ti. *Id.* ¶¶588-591.

¹⁴ Although *Tung* calls layer 59 a metal "silicide" layer, "silicide" is being used generically. *See* Thompson ¶587. A POSITA would not have understood the metal-semiconductor compound that results when metalizing a doped Ge semiconductor layer 55, *see Tung* ¶¶0058, ¶0078, to be a "silicide" in a strict sense. *See* Thompson ¶¶127-128, ¶587.

3. Claim 2

In the *Tung-Brask* combination, “the first and second source or drain regions have a boron concentration greater than 1E20.” *Tung* explains semiconductor material 51 is doped with a boron concentration “between about $1 \times 10^{17}/\text{cm}^3$ to about $5 \times 10^{20}/\text{cm}^3$.” *Tung* ¶¶0076-0077. *Brask* similarly teaches source/drain boron concentrations exceeding 1E20/cm³. *Brask* at 7:65-8:1 (source/drain regions doped “between 1×10^{19} to 1×10^{21} atoms/cm³”), 20:36-53 (tip extensions doped “between 1×10^{19} to 1×10^{21} atoms/cm³”), 22:52-60 (raised source/drain regions doped “between 1×10^{20} to 1×10^{21} atoms/cm³”). Since both *Tung* and *Brask* disclose boron concentrations exceeding 1E20/cm³, a POSITA would have adopted such concentrations in the *Tung-Brask* combination. Thompson ¶¶599-601.

4. Claim 3

In the *Tung-Brask* combination, “the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.” As Section VIII.B.3 explains, the source/drain regions in the *Tung-Brask* combination include a peak boron concentration exceeding 1E20/cm³. A POSITA also would have understood the boron concentration is graded from a base level up to that peak. Thompson ¶¶83, ¶323, ¶¶605-606; *see also* EX1038 at 7-11.

First, consider raised source/drain regions 51. *Tung* says semiconductor material 51 is doped “between about $1 \times 10^{17}/\text{cm}^3$ to about $5 \times 10^{20}/\text{cm}^3$.” *Tung*

¶0076. For example, semiconductor material 51 may be “an intrinsic semiconductor ... doped by implantation and annealing” a p-type dopant like boron. *Id.* ¶0040; *see also id.* ¶0077. *Brask* similarly teaches to implant its analogous raised source/drain regions 410/542 with boron “between 1×10^{20} to 1×10^{21} atoms/cm³.” *Brask* at 22:52-60; *see also id.* at 10:20-49. This results in a graded boron profile. *Supra* Section III.D; Thompson ¶¶604-608. A POSITA thus would have understood these raised source/drain regions have a boron profile graded to a peak exceeding $1 \text{E}20/\text{cm}^3$. Thompson ¶608.

Second, consider the source/drain extensions. *Tung* explains: “Suitable drain extension and source/drain implants are performed into the fin 28 after forming spacers (as required) to form the source/drain regions 39.” *Tung* ¶0057; *see also id.* ¶0073. Although *Tung* does not disclose a doping profile, *Brask* teaches a peak concentration “between 1×10^{19} to 1×10^{21} atoms/cm³.” *Brask* at 20:36-53; *see also id.* at 11:15-31. This is a graded boron doping profile, so a POSITA would have understood these source/drain extensions have a boron profile graded to a peak exceeding $1 \text{E}20/\text{cm}^3$. *Supra* Section III.D; Thompson ¶608. *Brask* additionally teaches the source/drain extensions are “subregions of different concentration” than the rest of the source/drain region. *Brask* at 7:65-8:4.

Third, consider doped semiconductor layer 55, which is optionally part of the source/drain regions.¹⁵ “[T]o minimize [source/drain] resistance,” it is “heavily doped” to a concentration exceeding “about $5 \times 10^{19}/\text{cm}^3$ ” using “a p-type dopant such as boron.” *Tung* ¶0034; *see also id.* ¶0078. Moreover, “a graded or a step like concentration may be used.” *Id.* ¶0062.

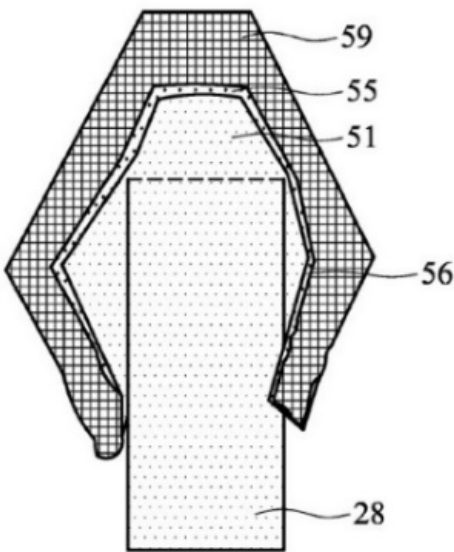


FIG. 4e

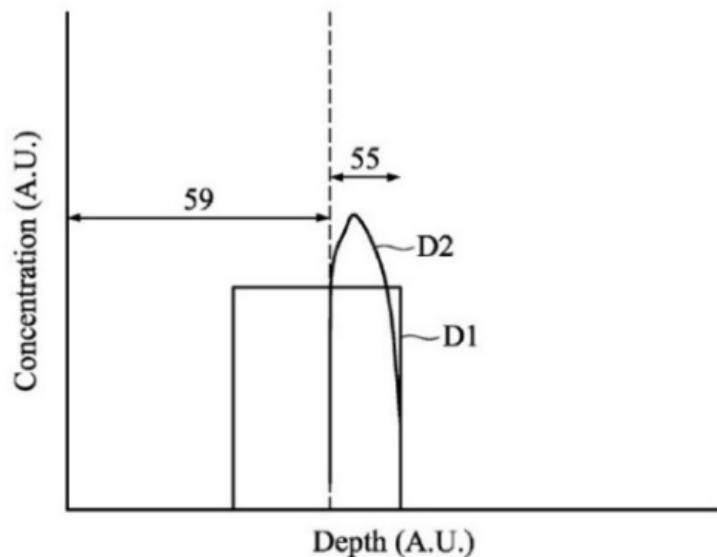


FIG. 11b

Additionally, as curves D1 and D2 show above, when metal layer 57 and doped semiconductor layer 55 are annealed to form TiSiGe layer 59, “dopant atoms segregate away from the [TiSiGe] metal silicide layer 59 into the doped semiconductor layer 55 (also referred as ‘snow-plough’ effect).” *Tung* ¶0063. “[A]s the dopant preferentially segregates out of the metal silicide layer 59, ... the

¹⁵ *Supra* note 12.

resulting doping profile (D2) in the doped semiconductor layer 55 is higher than a maximum concentration of the as-deposited doping profile (D1).” *Id.* ¶0065; *see also id.* at Figs. 9b, 11b. Thus, the concentration in doped semiconductor layer 55 (already $5 \times 10^{19}/\text{cm}^3$ at a *minimum*, *id.* ¶0034) becomes even larger with a clear gradient profile D2. *Id.* ¶0065, Fig. 11b. A POSITA would have understood the peak boron concentration in this “heavily doped” layer may exceed $1\text{E}20/\text{cm}^3$. Thompson ¶¶616-619; *see also Tung* ¶0034.

A POSITA further would have understood *Tung*’s source/drain regions have a graded boron profile that exceeds $1 \times 10^{20}/\text{cm}^3$ because the boron profiles in doped semiconductor layer 55, semiconductor material 51, and fin 28 differ from one another, and the concentration in semiconductor material 51 exceeds $1 \times 10^{20}/\text{cm}^3$. *See Tung* ¶0034, ¶0040, ¶0057, ¶¶0062-0065, ¶0073, ¶¶0076-0077.

Further to these express disclosures, a POSITA would have found it obvious to use a boron concentration graded from a base level to a peak exceeding $1\text{E}20/\text{cm}^3$. Thompson ¶¶610-615. Doing so was common to ensure low contact resistance and mitigate SCEs. *See supra* Section III.D; Thompson ¶607, ¶609, ¶¶611-613; *Brask* at 7:65-8:4; EX1039 at Fig. 4.5; EX1051 at 1, Figs. 1, 2; *Tung* ¶0076; *Brask* at 22:56-60; EX1034 at Figs. 1, 2, 5; EX1035 at Fig. 9; EX1052 at 1, Fig. 2; EX1037 at Fig. 7. A POSITA would have had no reason *not* to grade the

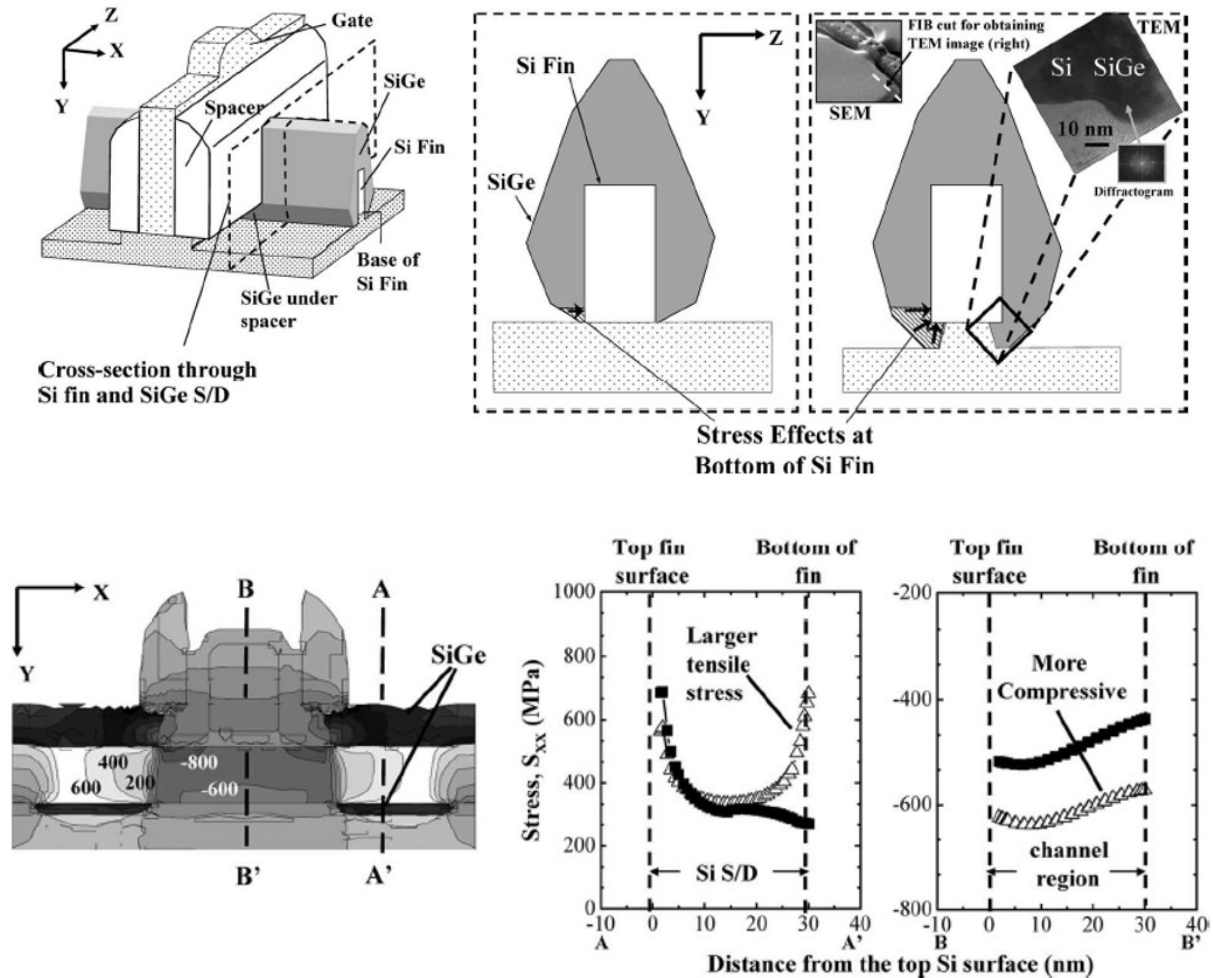
boron concentration in the *Tung-Brask* combination, which requires more effort to achieve. Thompson ¶609.

For these reasons, individually or collectively, a POSITA would have understood the *Tung-Brask* combination satisfies claim 3. Thompson ¶620.

5. Claim 4

In the *Tung-Brask* combination, “the fin comprises a strained channel between the first and second source or drain regions.” The source/drain regions of the *Tung-Brask* combination “are separated by a channel” in fin 28. *Tung* ¶0065; *see also id.* ¶0052, Figs. 2a, 2d, 7c, 11c. A POSITA would have understood from the basic tenets of SiGe/strained Si technology that this channel is strained. *See supra* Section III.B; Thompson ¶622. Various publications describe the strain profile for the same FinFET structure and confirm its channel would be strained. *See* Thompson ¶¶623-626.

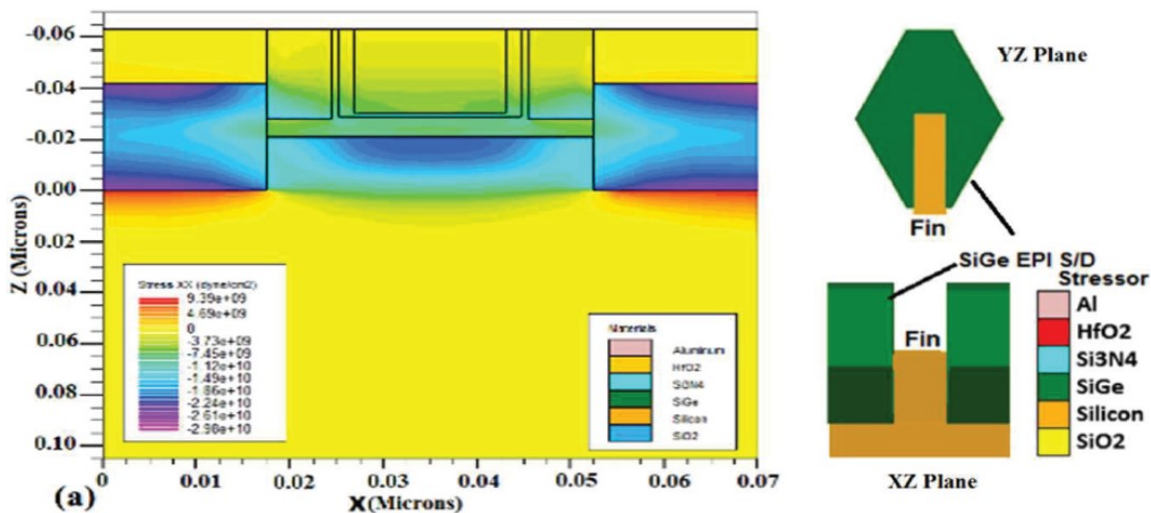
The study below, for example, used “the Taurus Process simulator for FinFETs” to perform “[t]hree-dimensional stress simulations” on devices having the same structure. EX1053 at 2-3; *see also id.* at Figs. 1, 2.



EX1053, Figs. 1, 2

It explains “[t]he SiGe stressor” (analogous to *Tung*’s semiconductor material 51 and *Brask*’s semiconductor film 410) has “a larger lattice constant” and therefore “exerts a tensile stress in the Si in the S/D regions,” thereby causing “compressive stress in the Si channel region for hole mobility enhancement.” *Id.* at 3. As the figures on the lower-left and lower-right above illustrate, the channel is compressively strained. *Id.* at Fig. 2; Thompson ¶624.

A similar study, shown below, also confirms “[c]ompressive stress is observed in the channel through the SiGe-epi stressor.” EX1056 at 1; *see also id.* at Figs. 2, 3; Thompson ¶¶625. Consistent with basic tenets of SiGe/Strained Si technology, it explains “the SiGe layer (SiGe-epi) is known to generate lattice mismatch stress at the silicon interface since [the] Si_{1-x}Ge_x alloy has a larger lattice constant.” EX1056 at 1.



EX1056, Figs. 2, 3 (excerpted and combined)

Others stated that “strained channel engineering and epitaxially grown raised source/drains have been successfully demonstrated” in the structure on the left below, EX1043 at 1, and explained that the figure on the right below “introduce[s] compressive strain into the Si channel,” EX1011 at 10; *see also* Thompson ¶¶627-628.

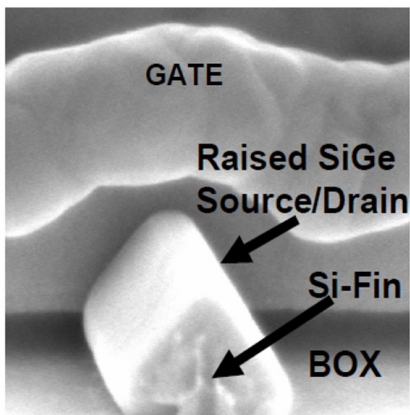
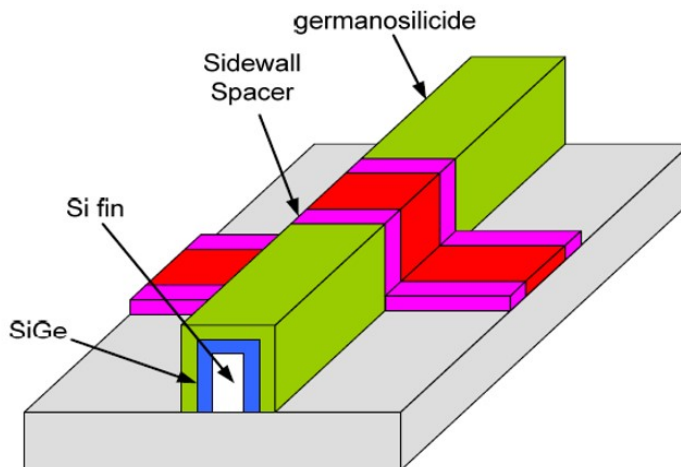


Fig. 7b Y-dir. cross-section of PMOS Trigate with SiGe raised source/drain

EX1043 Fig. 7b



EX1011, Fig. 18

Given the lattice mismatch between semiconductor material 51 and fin 28 in the *Tung-Brask* combination, as these references confirm, the channel is strained. Thompson ¶¶626-629.

6. Claim 5

In the *Tung-Brask* combination, “the first and second source or drain regions are P-type.” *Tung* describes forming “a PMOS transistor,” which a POSITA would have understood has P-type source/drain regions. *Tung* ¶¶0034, ¶¶0052, ¶¶0073, ¶¶0077, ¶¶0080; *see also* Thompson ¶¶633.

7. Claim 6

Claim 6 is identical to claim 1, except limitations [6.1]-[6.3], and [6.6], recite a “body” instead of a “fin.” The ’178 Patent uses the term “body” only once, equating it with a “fin.” ’178 Patent at 13:24-27; *see also* Thompson ¶¶636 & n.643; *Brask* at 5:26-30, 18:3-16, Figs. 3, 5I. Thus, a POSITA would have understood

there is no meaningful difference between claims 1 and 6, and the asserted *Tung-Brask* combination satisfies claim 6 for the reasons in Sections VIII.B.2.a-f. Thompson ¶¶635-644; *see also Mycogen*, 243 F.3d at 1329.

8. Claim 7

The *Tung-Brask* combination satisfies claim 7 for the reasons in Section VIII.B.3. *See* Thompson ¶¶645-647.

9. Claim 8

The *Tung-Brask* combination satisfies claim 8 for the reasons in Section VIII.B.4. *See* Thompson ¶¶648-650.

10. Claim 9

The *Tung-Brask* combination satisfies claim 9 for the reasons in Section VIII.B.5. *See* Thompson ¶¶651-653.

11. Claim 10

The *Tung-Brask* combination satisfies claim 10 for the reasons in Section VIII.B.6. *See* Thompson ¶¶654-656.

12. Claims 11-20

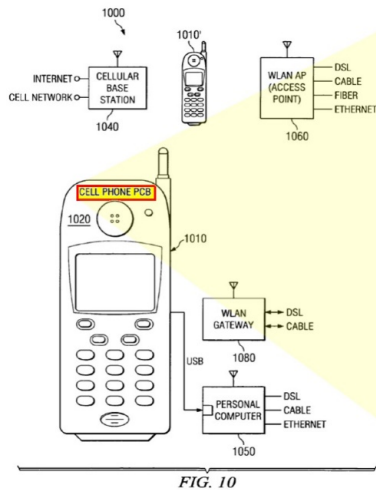
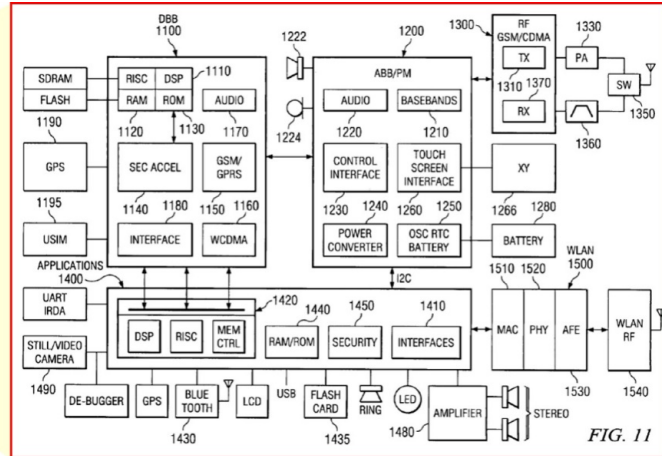
The *Tung-Brask* combination satisfies claims 11-20 for the reasons in Section VIII.C *infra*.

C. Claims 11-20: The *Ranade-Kim* and *Tung-Brask* Combinations, Alone (Grounds 1A and 2A) or Further in View of *Liu* (Grounds 1B and 2B)

It was beyond question that FinFETs would go into computing devices. *See* Thompson ¶¶229, ¶438, ¶555, ¶723. Computing devices that use integrated circuits made of FETs (their primary application) were known long before December 2010. *Id.* Although the section below discusses disclosures in *Liu* that demonstrate why claims 11-20 would have been obvious, a POSITA would have understood simply from his or her knowledge of the electronics industry that a typical computer or smartphone had the additional features recited in those claims. A POSITA would have found claims 11-20 obvious even without recourse to *Liu*. *See id.*

1. A POSITA Would Have Found It Obvious to Deploy the *Ranade-Kim* and *Tung-Brask* FinFETs in Systems Like the Ones *Liu* Describes

Liu confirms that FETs, including FinFETs, “are widely used in the electronics industry.” *Liu* at 1:47-50; *see also id.* at 32:22-40, Fig. 8. A POSITA would have known they are fundamental building blocks of integrated circuits, which, after packaging, become “chips” that are added to other circuit elements on a circuit board for use in devices like smartphones. Thompson ¶¶374, ¶659; *see also id.* ¶¶439-441; *Liu* at 1:29-61, 5:27-6:9, 6:55-56, 32:22-40, 33:11-37:59. *Liu*’s Figures 10 and 11 below illustrate such a system. *Liu* at 33:10-37:40, Figs. 10-11.

**Liu Fig. 10****Liu Fig. 11**

A POSITA would have found it obvious to incorporate the *Ranade-Kim* and *Tung-Brask* FinFETs in such a system because it would have involved (1) combining prior art elements (FETs) according to known methods (semiconductor fabrication) to yield predictable results (a computing device); (2) using known a technique (using FinFETs) to improve similar devices (computing devices) in the same way; (3) applying a known technique (using FinFETs) to a known device (a computing device) ready for improvement to yield predictable results; and/or (4) applying *Liu's* teachings, suggestions, and motivations to arrive at the claimed application of the FinFET structures discussed in Sections VIII.A and VIII.B. Thompson ¶¶442-447, ¶¶724-729.

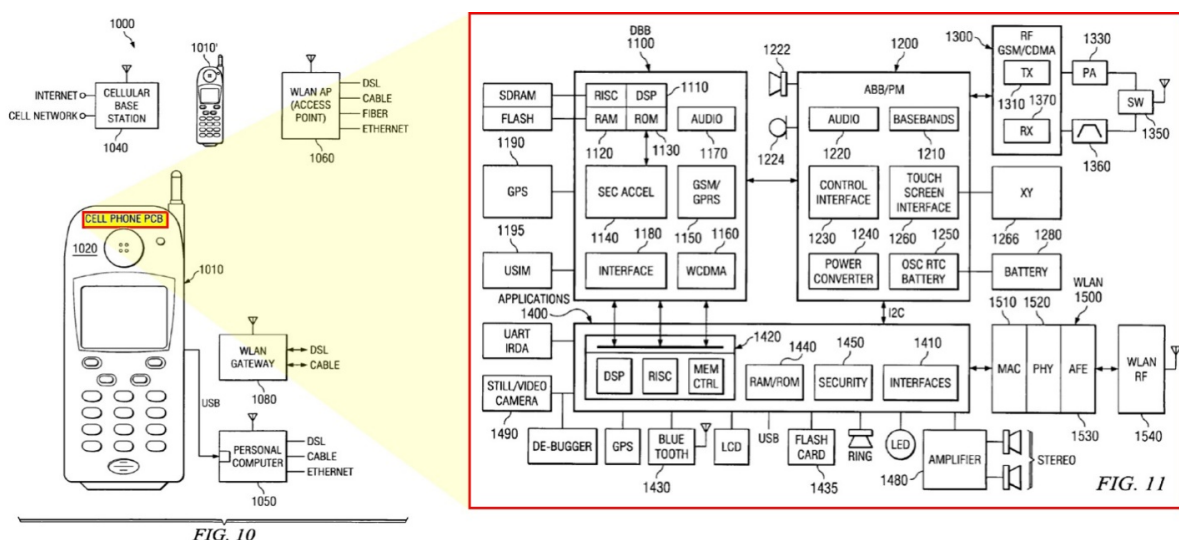
2. Claim 11

a. Element [11.0]

To the extent the preamble is limiting, the *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide for “[a] computing device.” A POSITA would have understood FinFETs are intended almost exclusively for such applications. Thompson ¶¶374, ¶¶659. *Liu* further discloses a “wireless handset” that uses FinFET-based integrated circuits. *Liu* at 32:23-40, 33:11-37:59, Figs. 8, 10-11; *see also* Thompson ¶¶450-451, ¶¶732-733.

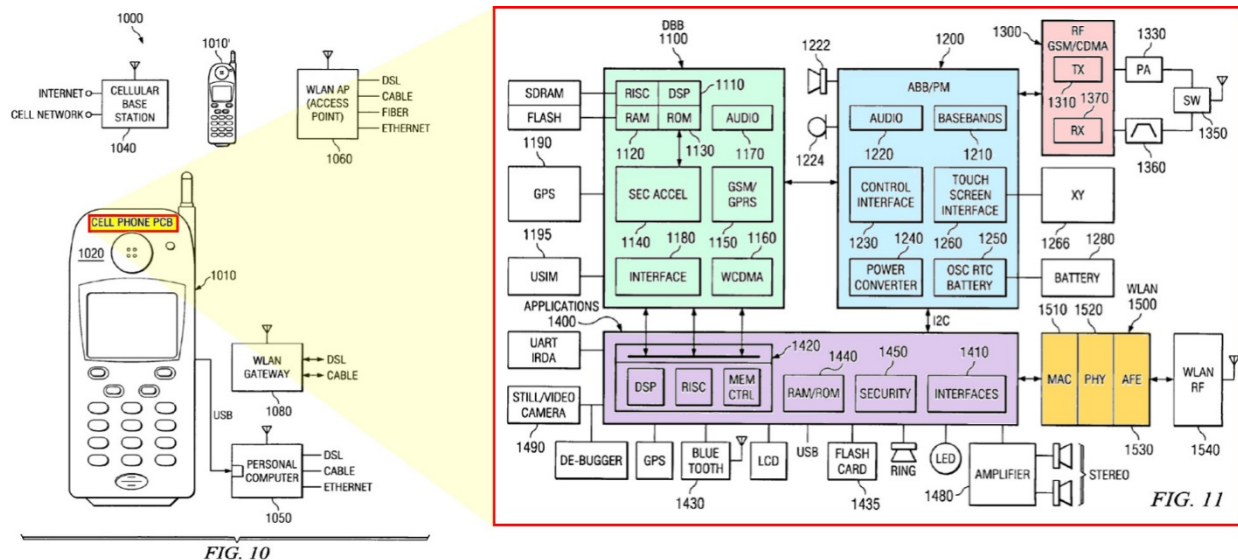
b. Element [11.1]

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide for “[a] board.” A POSITA would have understood FinFETs are intended almost exclusively for such applications. Thompson ¶¶378, ¶¶663. *Liu* further discloses a “cell phone printed circuit board” (red) in a “wireless handset.” *Liu*, 33:46-34:2, Figs. 10-11; *see also* Thompson ¶¶455, ¶¶737.



c. Element [11.2]

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide for “a component coupled to the board, the component including an integrated circuit structure.” A POSITA would have understood FinFETs are intended almost exclusively for such applications. Thompson ¶382, ¶667. *Liu* further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. *Liu*’s PCB includes FinFET-based integrated circuits, such as digital baseband chip 1100 (green), analog baseband chip 1200 (blue), GSM chip 1300 (red), applications processor chip 1400 (purple), and WLAN chip 1500 (orange). *Id.* at 6:48-51, 32:23-40, 34:23-30, 35:14-20, 35:64-67, 36:15-16, 37:14-17, Figs. 8, 10-11; *see also* Thompson ¶459, ¶741.

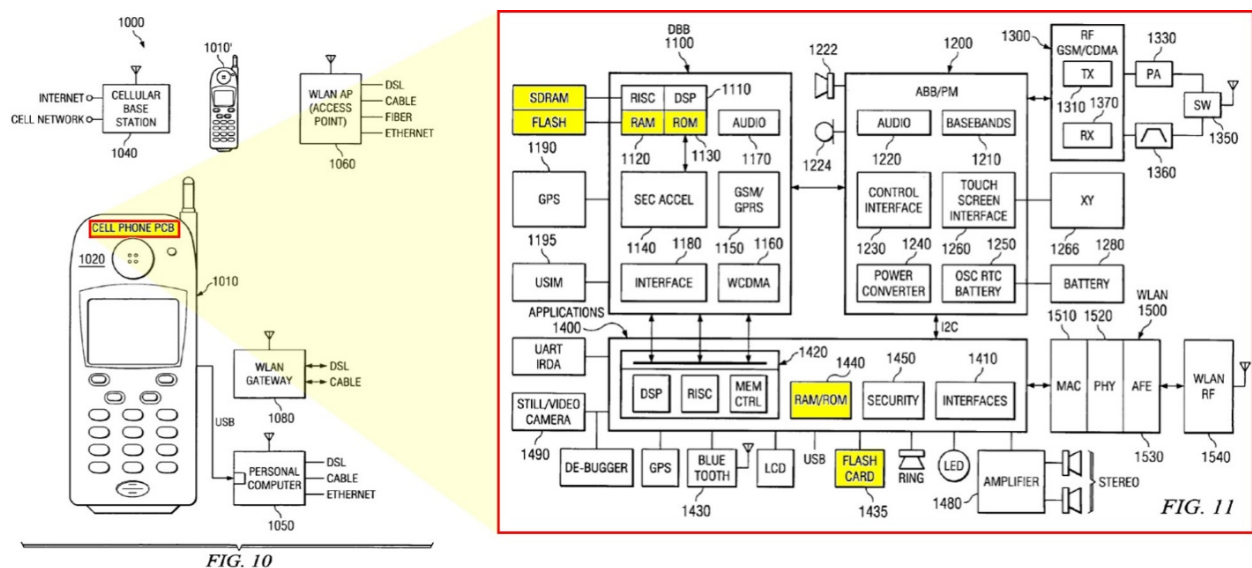


d. Elements [11.3] through [11.10]

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, satisfy elements [11.3] through [11.10] for the reasons in Sections VIII.A.2.a-f and VIII.B.2.a-f. See Thompson ¶¶384-391, ¶¶461-468, ¶¶669-676, ¶¶743-750.

3. Claim 12

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide for “a memory coupled to the board.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed to going into chips that go on circuit boards and exchange information with a memory. Thompson ¶¶395-396, ¶¶680-681.

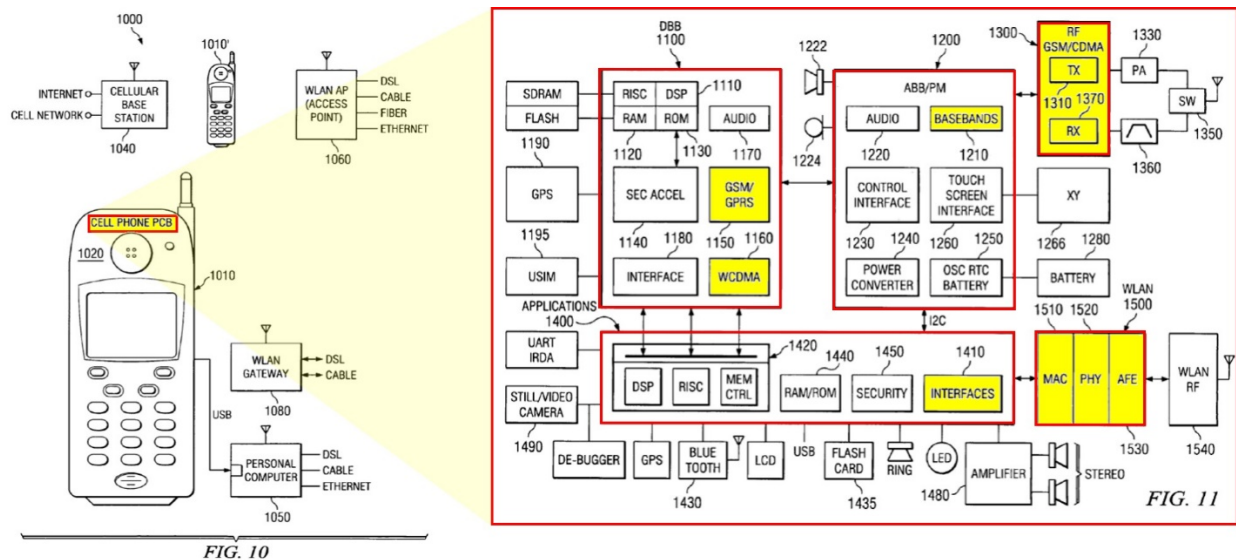


Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. Coupled to the PCB are various memories (yellow above), including off-chip Flash and SDRAM and memory elements 1120,

1130, 1435, and 1440. *Id.* at 34:28-33, 36:24-33, Figs. 10-11; *see also* Thompson ¶¶472-473, ¶¶754-755.

4. Claim 13

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide for “a communication chip coupled to the board.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits, including communication chips, that go onto circuit boards in smartphones and computers. Thompson ¶¶400-401, ¶¶685-686.



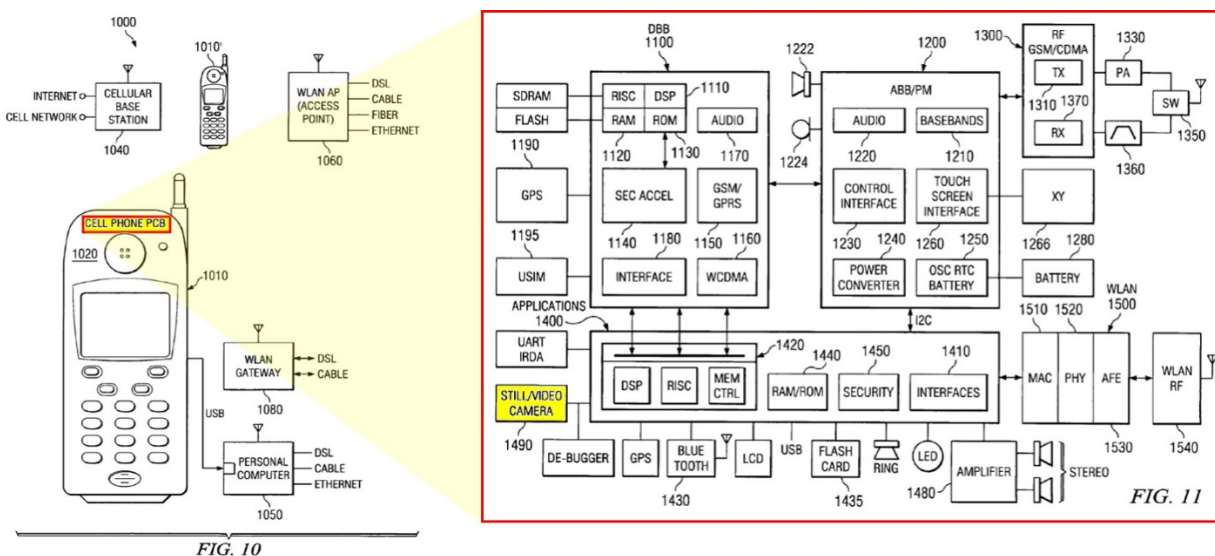
Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. Coupled to the PCB are various communication chips (circled in red; relevant functional blocks highlighted in yellow), including integrated circuits 1100, 1200, 1300, 1400, and 1500. *Id.* at

34:33-42, 35:14-20, 35:64-36:36, 37:14-36, Figs. 10-11; *see also* Thompson ¶¶478-479, ¶¶760-761.

5. Claim 14

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide for “a camera coupled to the board.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a camera. Thompson ¶¶405-406, ¶¶690-691.

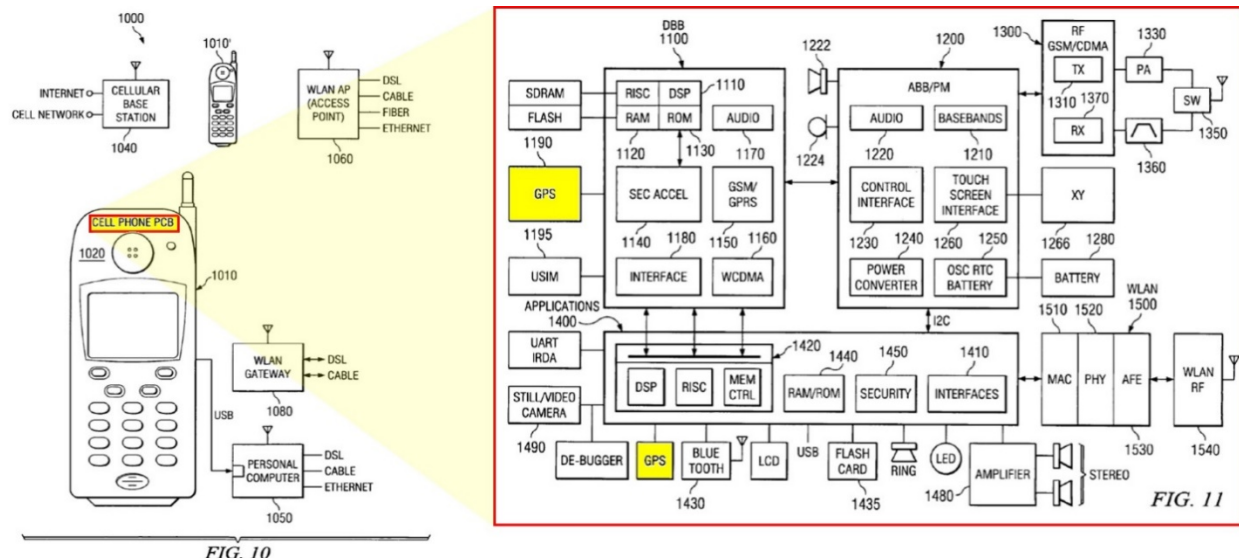
Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. Coupled to the PCB is a camera 1490 (yellow). *Id.* at 36:60-65, Figs. 10-11; *see also* Thompson ¶¶484-485, ¶¶766-767.



6. Claim 15

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide for “a global positioning system coupled to the board.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a GPS. *Id* Thompson ¶¶410-411, ¶¶695-696.

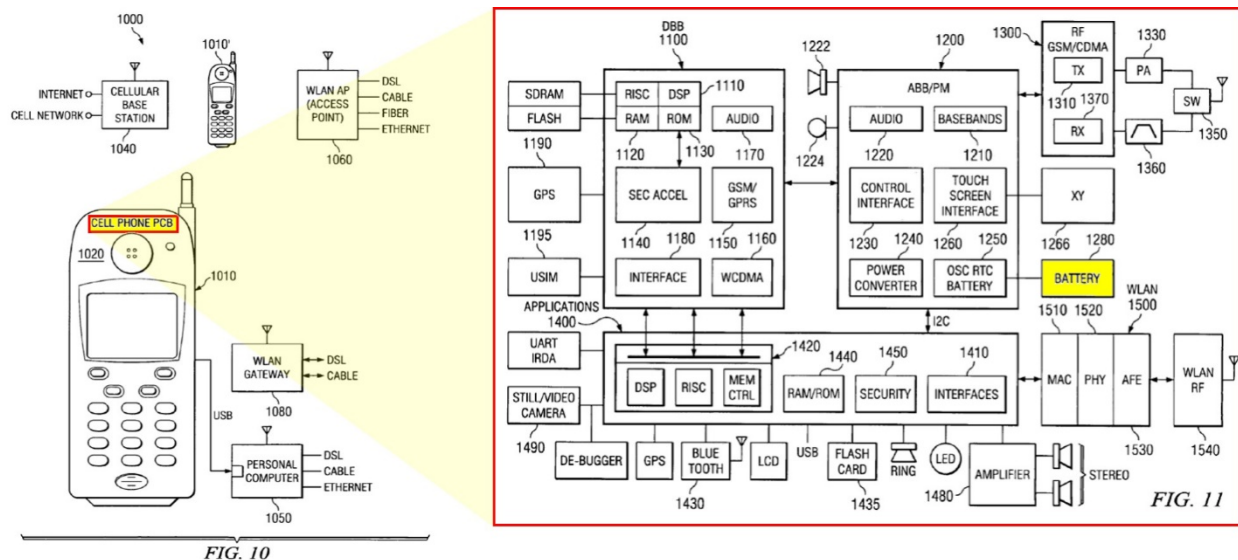
Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. Coupled to the PCB is a GPS 1190 (yellow). *Id.* at 34:66-35:4, 36:60-65, Figs. 10-11; *see also* Thompson ¶¶490-491, ¶¶772-773.



7. Claim 16

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide for “a battery coupled to the board.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a battery. Thompson ¶¶415-416, ¶¶700-701.

Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. Coupled to the PCB is a battery 1280 (yellow). *Id.* at 35:54-63, Figs. 10-11; *see also* Thompson ¶¶496-497, ¶¶778-779.

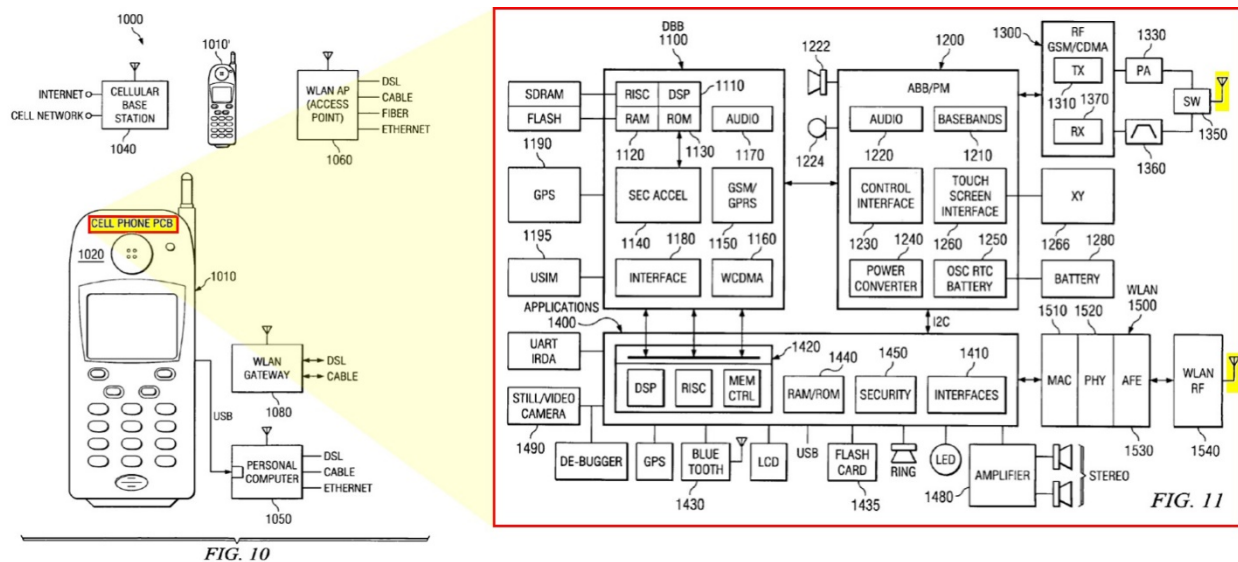


8. Claim 17

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide for “an antenna coupled to the board.” A POSITA, applying common

knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to an antenna. Thompson ¶¶420-421, ¶¶705-706.

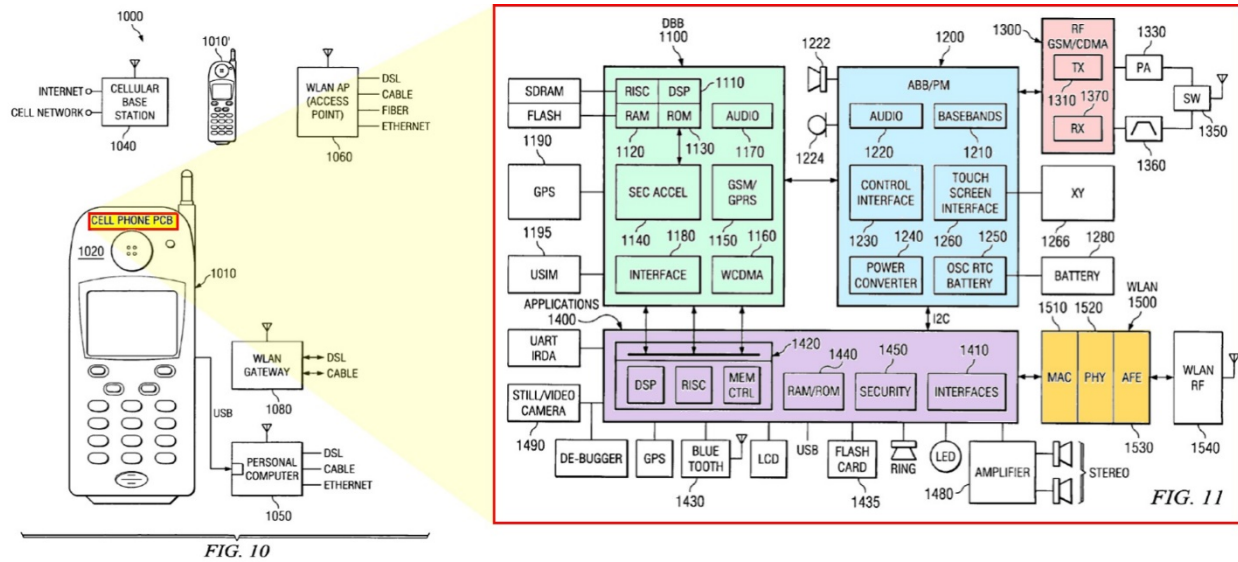
Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. Coupled to the PCB are a wireless antenna and WLAN antenna (yellow). *Id.* at 36:4-7, 37:26-27; *see also id.* at 5:62-65, Figs. 10-11; Thompson ¶¶502-503, ¶¶784-785.



9. Claim 18

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provides that “the component is a packaged integrated circuit die.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits that go onto

circuit boards as packaged integrated circuit dies. Thompson ¶¶435-436, ¶¶710-711.

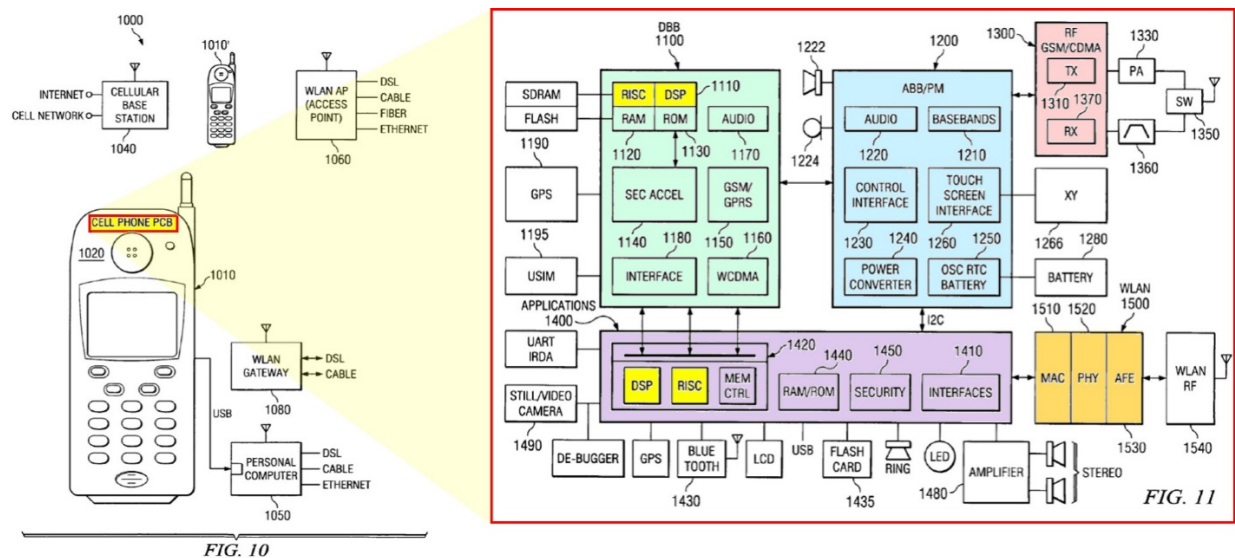


Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. As shown above, the PCB includes FinFET-based integrated circuits 1100 (green), 1200 (blue), 1300 (red), 1400 (purple), and 1500 (orange). *Id.* at 6:48-51, 32:23-40, 34:23-30, 35:14-20, 35:64-67, 36:15-16, 37:14-17, Figs. 8, 10-11; Thompson ¶¶508-509, ¶¶790-791. A POSITA would have understood these are packaged dies (chips/chiplets) because unpackaged integrated circuits are used only for testing or to be packaged. Thompson ¶510, ¶792.

10. Claim 19

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide that “the component is selected from the group consisting of a processor, a

communications chip, and a digital signal processor.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits (including processors, communications chips, and digital signal processors (DSPs)) that go onto circuit boards of smartphones, computers, and the like. Thompson ¶¶430-431, ¶¶715-716.

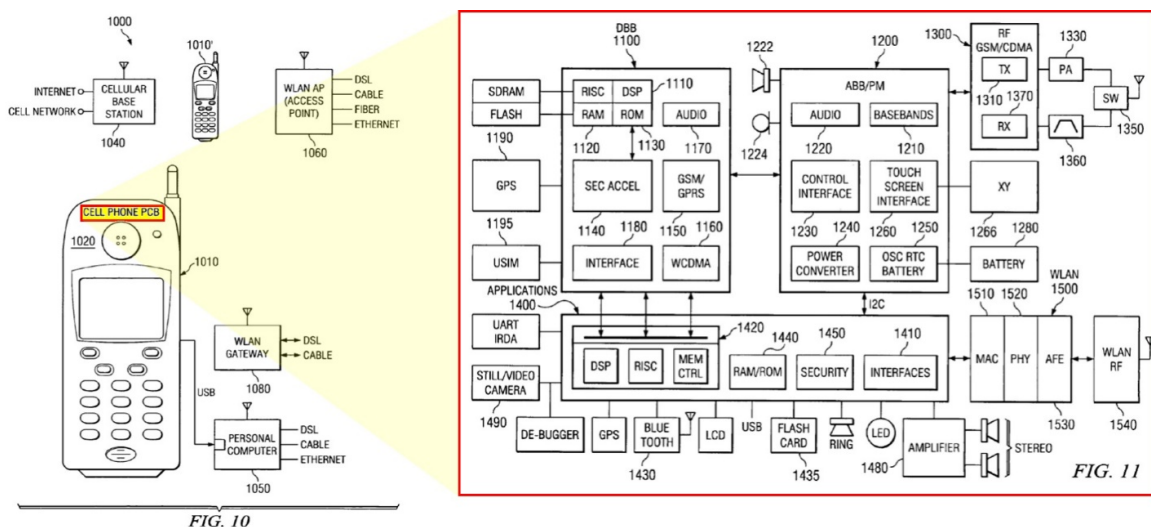


Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. As shown above, coupled to the PCB are communication chips 1100 (green), 1200 (blue), 1300 (red), 1400 (purple), and 1500 (orange). *Id.* at 34:33-42, 35:14-20, 35:64-36:36, 37:14-36, Figs. 10, 11; Thompson ¶¶515-516, ¶¶797-798. Additionally, highlighted in yellow, the component may be “a RISC processor (such as MIPS core, ARM processor, or other suitable processor)” or “a digital signal processor (DSP).” *Liu* at 34:23-30, 36:18-31; *see also* Thompson ¶517, ¶799.

11. Claim 20

The *Ranade-Kim* and *Tung-Brask* combinations, alone or in view of *Liu*, provide that “the computing device is selected from the group consisting of a mobile phone, a laptop, a desktop computer, a server, and a set-top box.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits that go onto the circuit boards of such devices. Thompson ¶¶435-436, ¶¶720-721.

Liu further discloses FinFETs for use in a “cell phone printed circuit board (PCB)” in a “wireless handset,” as shown below. *Liu* at 33:46-34:2; *see also id.* at 6:48-51, 32:23-40, Figs. 8, 10-11; Thompson ¶¶522-523, ¶¶804-805. *Liu* also describes using such components in other computing devices like “radios and televisions, fixed and portable entertainment units, routers, pagers, personal digital assistants (PDA), organizers, scanners, faxes, copiers, household appliances, [and] office appliances.” *Liu* at 34:3-22.



IX. TRIAL SHOULD BE INSTITUTED

Because no substantive action has occurred in the related district court proceeding, which remains stayed, all *Fintiv* factors weigh against discretionary denial under §314(a). *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, at 5-6 (P.T.A.B. Mar. 20, 2020). “The PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding.” EX1057 at 6.

Likewise, there is no reason to deny institution under §314(a) based on Samsung’s IPR2023-00536. It is stayed pending voluntary dismissal. Patent Owner has not filed a preliminary response, nor has the Board taken any substantive action. All *General Plastics* factors weigh against denial. *See General Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357 *et seq.*, Paper 19, at 8-10 (P.T.A.B. Sept. 6, 2017).

Finally, there is no reason to deny institution under §325(d). Neither the art nor the arguments in this Petition are the same or substantially the same as previously presented to the Office. *See Advanced Bionics, LLC. v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, at 7-9 (P.T.A.B. Feb. 13, 2020). None of the asserted art was cited or considered during prosecution. Although Samsung’s IPR2023-00536 relies on *Tung*, the Board has not considered the merits of those arguments, nor are they the same or substantially the same in this Petition.

X. MANDATORY NOTICES**A. Real Party-in-Interest**

The real parties-in-interest are Taiwan Semiconductor Manufacturing Company Ltd. and TSMC North America.

B. Related Matters

The '178 Patent is, or has been, involved in the following:

Name	Number	Court	Filed
Semiconductor Devices, Mobile Devices Containing the Same, and Components Thereof	Inv. No. 337-TA-1336	ITC	9/12/2022
Daedalus Prime LLC v. Samsung Electronics Co., Ltd.	2:22-cv-00352	EDTX	9/12/2022
Taiwan Semiconductor Mfg. Co. Ltd. v. Daedalus Prime LLC et al.	1:22-cv-01647	DDE	12/30/2022
Samsung Electronics Co., Ltd. v. Daedalus Prime LLC	IPR2023-00536	PTAB	2/24/2023

C. Lead and Back-Up Counsel, and Service Information

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XI. PAYMENT OF FEES

The Office may charge additional fees to Deposit Account No. 06-0916.

XII. TIME FOR FILING PETITION

This Petition is being filed more than nine months after the '178 Patent was granted, *see* 37 C.F.R. §42.102(a)(1), and within one year of Petitioner being served with a complaint alleging infringement, *see* 37 C.F.R. §42.101(b).

XIII. GROUNDS FOR STANDING

Under 37 C.F.R. §42.104(a), Petitioner certifies the '178 Patent is available for *inter partes* review and Petitioner is not barred or estopped from requesting such review on any grounds identified in this Petition.

XIV. CERTIFICATION UNDER 37 C.F.R. §42.24(d)

As calculated by the “Word Count” feature of Microsoft Word for Microsoft 365, this Petition contains 13,952 words, excluding this Certification and the following: Table of Contents, Table of Authorities, List of Exhibits, Claim Listing, Mandatory Notices Under 37 C.F.R. §42.8, and Certificate of Service.

XV. CONCLUSION

For the reasons above, claims 1-20 are unpatentable. Trial should be instituted and the challenged claims cancelled.

Dated: June 22, 2023

Respectfully submitted,

/ J. Preston Long, Reg.# 65,125 /

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CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), **Petition for *Inter Partes* Review, Petitioner's Power of Attorney, and the associated Exhibits 1001-1063** were served via FedEx on June 22, 2023, on the correspondence address of record below indicated in the Patent Office's public PAIR system for U.S. Patent No. 10,700,178.

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Dated: June 22, 2023

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