

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Daedalus Prime LLC,

Patent Owner.

Patent No. 10,700,178 B2

Filing Date: May 20, 2019

Issue Date: June 30, 2020

Title: CONTACT RESISTANCE REDUCTION EMPLOYING
GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Inter Partes Review No. IPR2023-01120

PETITIONER'S UPDATED EXHIBIT LIST

Pursuant to 37 C.F.R. § 42.63(e), Petitioner Taiwan Semiconductor Manufacturing Company Ltd. submits a current listing of exhibits to counsel for Patent Owner Daedalus Prime LLC. Exhibit 1064 is being filed today.

LIST OF EXHIBITS

Exhibit	Description of Exhibit
Exhibit 1001	U.S. Patent No. 10,700,178 to Glass et al. (“’178 Patent”).
Exhibit 1002	Declaration of Dr. Scott E. Thompson, Ph.D. (“Thompson”).
Exhibit 1003	U.S. Patent Appl. Pub. No. 2008/0121932 A1 to Ranade (“ <i>Ranade</i> ”).
Exhibit 1004	U.S. Patent Appl. Pub. No. 2010/0123198 A1 to Kim et al. (“ <i>Kim</i> ”).
Exhibit 1005	U.S. Patent No. 7,611,943 to Liu (“ <i>Liu</i> ”).
Exhibit 1006	U.S. Patent Appl. Pub. No. 2010/0276761 A1 to Tung et al. (“ <i>Tung</i> ”).
Exhibit 1007	U.S. Patent No. 7,361,958 to Brask et al. (“ <i>Brask</i> ”).
Exhibit 1008	M.-H. Chi, <i>Challenges in Manufacturing FinFET at 20nm Node and Beyond</i> , Technology Development, GlobalFoundries (2012).
Exhibit 1009	U.S. Patent No. 6,413,802 to Hu et al.
Exhibit 1010	B. Doyle et al., <i>Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout</i> , Digest of the 2003 Symposium on VLSI Technology, pp. 133-34 (2003).
Exhibit 1011	M.C. Ozturk & J. Liu, <i>Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond</i> , 2005 AIP Conference Proceedings, International Conference on Characterization and Metrology for ULSI Technology, vol. 788, at 222-31 (Mar. 2005).

Exhibit	Description of Exhibit
Exhibit 1012	U.S. Patent Appl. Pub. No. 2009/0075029 A1 to Thomas et al.
Exhibit 1013	G. Eneman et al., <i>Scalability of the Si_xGe_{1-x} Source/Drain Technology for the 45-nm Technology Node and Beyond</i> , IEEE Transactions on Electron Devices, vol. 53, no. 7, pp. 1647-56 (July 2006).
Exhibit 1014	D.K. Sadana et al., <i>Applications of Epitaxy for Semiconductor Technology</i> , ECS Transactions, 218th ECS Meeting, vol. 33, no. 6, pp. 59-70 (Oct. 2010).
Exhibit 1015	U.S. Patent No. 7,767,560 to Jin et al.
Exhibit 1016	U.S. Patent No. 7,821,772 to Kavalieros et al.
Exhibit 1017	U.S. Patent No. 7,288,443 to Zhu.
Exhibit 1018	U.S. Patent Appl. Pub. No. 2010/0148217 A1 to Simonelli et al.
Exhibit 1019	U.S. Patent Appl. Pub. No. 2007/0187767 A1 to Yasutake.
Exhibit 1020	J.-P. Han et al., <i>Novel Enhanced Stressor With Graded Embedded SiGe Source/Drain for High Performance CMOS Devices</i> , Technical Digest of the 2006 IEEE International Electron Devices Meeting (IEDM), pp. 437-440 (2006).
Exhibit 1021	U.S. Patent Appl. Pub. No. 2007/0122953 A1 to Liu et al.
Exhibit 1022	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice, and Modeling</i> (1st ed. 2000) (excerpted).
Exhibit 1023	S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (excerpted).
Exhibit 1024	U.S. Patent No. 6,949,482 to Murthy et al.
Exhibit 1025	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> (1st ed. 2000) (excerpted).
Exhibit 1026	U.S. Patent No. 8,358,012 to Haran et al.

Exhibit	Description of Exhibit
Exhibit 1027	U.S. Patent Appl. Pub. No. 2008/0067545 A1 to Rhee et al.
Exhibit 1028	E. Bucher et al., <i>Work Function and Barrier Heights of Transition Metal Silicides</i> , Applied Physics A, no. 40, pp. 71-77 (1986).
Exhibit 1029	E.D. Marshall et al., <i>Metal-Germanium Contacts and Germanide Formation</i> , Materials Research Society Symposia Proceedings, vol. 47: Symposium C – Thin Films: The Relationship of Structure to Properties, pp. 161-166 (1985).
Exhibit 1030	R. Braunstein et al., <i>Intrinsic Optical Absorption in Germanium-Silicon Alloys</i> , Physical Review, vol. 109, no. 3, pp. 695-710 (1958).
Exhibit 1031	J. Weber & M.I. Alonso, <i>Near-Band-Gap Photoluminescence of Si-Ge Alloys</i> , Physical Review B, vol. 40, no. 8, pp. 5683-5693 (1989).
Exhibit 1032	V.E. Houtsma, <i>Gate Oxide Reliability of Poly-Si and Poly-SiGe CMOS Devices</i> , Doctoral Dissertation, University of Twente (1999) (excerpted).
Exhibit 1033	U.S. Patent No. 5,644,166 to Honeycutt et al.
Exhibit 1034	C.C. Wang et al., <i>Boron Diffusion in Strained and Strain-Relaxed SiGe</i> , Materials Science and Engineering B, vols. 124-125, pp. 39-44 (2005).
Exhibit 1035	H. Okamoto et al., <i>A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-Node High-Performance pMOSFET Technology</i> , Proceedings of the 2008 38th European Solid-State Device Research Conference (ESSDERC), pp. 326-29 (Sept. 2008).
Exhibit 1036	U.S. Patent Appl. Pub. No. 2007/0235802 A1 to Chong et al.

Exhibit	Description of Exhibit
Exhibit 1037	S. Gannavaram et al., <i>Low Temperature ($\leq 800^{\circ}\text{C}$) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for Sub-70 nm CMOS</i> , Technical Digest of the 2000 International Electron Devices Meeting (IEDM), pp. 437-40 (2000).
Exhibit 1038	H. Xiao, <i>Introduction to Semiconductor Manufacturing Technology</i> (2001) (excerpted).
Exhibit 1039	R. Wittman, <i>Miniaturization Problems in CMOS Technology: Investigation of Doping Profiles and Reliability</i> , Doctoral Dissertation, Wien University Austria (Jan. 2007) (excerpted).
Exhibit 1040	<i>FinFETs and Other Multi-Gate Transistors</i> (J.-P. Colinge ed., 2008) (excerpted).
Exhibit 1041	U.S. Patent No. 8,652,894 to Lin et al.
Exhibit 1042	S. Thompson et al., <i>A Logic Nanotechnology Featuring Strained-Silicon</i> , IEEE Electron Device Letters, vol. 25, no. 4, pp. 191-93 (Apr. 2004).
Exhibit 1043	J. Kavalieros et al., <i>Tri-Gate Transistor Architecture With High-k Gate Dielectric Metal Gates and Strain Engineering</i> , 2006 IEEE Symposium on VLSI Technology Digest of Technical Papers, pp. 1-2 (June 2006).
Exhibit 1044	Prosecution File History, U.S. Patent No. 10,700,178 (“File History”).
Exhibit 1045	Amendment to European Patent Application No. 11851579.0 (June 23, 2015).
Exhibit 1046	U.S. Patent No. 9,245,805 to Yeh et al.
Exhibit 1047	English Translation of Korean Patent Application Serial No. 10-20080115801 to Kim et al. (“Korean <i>Kim</i> ”).

Exhibit	Description of Exhibit
Exhibit 1048	S. Natarajan et al., <i>A 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors, Enhanced Channel Strain and 0.171μm² SRAM Cell Size in a 291Mb Array</i> , Technical Digest of the 2008 IEEE International Electron Devices Meeting (IEDM), pp. 1-3 (2008).
Exhibit 1049	K. Mistry et al., <i>A 45nm Logic Technology with High-k + Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging</i> , Technical Digest of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (2007).
Exhibit 1050	U.S. Patent Appl. Pub. No. 2008/0054347 A1 to Wang.
Exhibit 1051	P. Ranade et al., <i>A Novel Elevated Source/Drain PMOSFET Formed by Ge-B/Si Intermixing</i> , IEEE Electron Device Letters, vol. 23, no. 4, pp. 218-20 (Apr. 2002).
Exhibit 1052	Y.-M. Sheu et al. <i>Modeling Dopant Diffusion in Strained and Strain-Relaxed Epi-SiGe</i> , 2005 Int'l Conference on Simulation of Semiconductor Processes and Devices, pp. 75-78 (Sept. 2005).
Exhibit 1053	K.-M. Tan et al., <i>Strained p-Channel FinFETs With Extended Π-Shaped Silicon–Germanium Source and Drain Stressors</i> , IEEE Electron Device Letters, vol. 28, no. 10, pp. 905-08 (Oct. 2007).
Exhibit 1054	S. Zaima & Y. Yasuda, <i>Study of Reaction and Electrical Properties at Ti/SiGe/Si(100) Contacts for Ultralarge Scale Integrated Applications</i> , Journal of Vacuum Science & Technology B, vol. 16, pp. 2623-28 (1998).
Exhibit 1055	S. Gaudet et al., <i>Thin Film Reaction of Transition Metals with Germanium</i> , Journal of Vacuum Science & Technology A, vol. 24, no. 3, pp. 474-486 (2006).

Exhibit	Description of Exhibit
Exhibit 1056	J. Jena et al., <i>Stress Enhanced Performance Analysis for Trigate FinFETs at 7nm Node</i> , 2021 International Conference in Advances in Power, Signal, and Information Technology (APSIT), pp. 1-6 (Oct. 2021).
Exhibit 1057	Memorandum from Katherine K. Vidal to the Members of the Patent Trial and Appeal Board on Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (June 21, 2022).
Exhibit 1058	P. Bai et al., <i>A 65nm Logic Technology Featuring 35 nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell</i> , Technical Digest of the 2004 International Electron Devices Meeting (IEDM), pp. 657-660 (2004).
Exhibit 1059	S. Thompson, et al., <i>A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 μm^2 SRAM Cell</i> , Technical Digest of the 2002 International Electron Devices Meeting (IEDM), pp. 61-64 (2002).
Exhibit 1060	S.E. Thompson & S. Parthasarathy, <i>Moore's Law: The Future of Si Microelectronics</i> , Materials Today, vol. 9, no. 6, pp. 20-25 (June 2006).
Exhibit 1061	Y. Sun et al., <i>Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors</i> , Journal of Applied Physics, vol. 101, 104503, pp. 1-22 (2007).
Exhibit 1062	U.S. Patent No. 8,362,575 to Kwok et al.
Exhibit 1063	U.S. Patent Appl. Pub. No. 2007/0123042 A1 to Rim et al.
Exhibit 1064	Settlement Agreement between Petitioner and Patent Owner— BUSINESS CONFIDENTIAL INFORMATION PROTECTED UNDER 35 U.S.C. 317(b).

Date: October 26, 2023

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that the foregoing
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record for the Patent Owner on October 26, 2023, at the following addresses:

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