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(54) **SEMICONDUCTOR DEVICES AND METHODS OF MANUFACTURING THE SAME**

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(57) **ABSTRACT**

Provided are semiconductor devices having low resistance contacts and methods of manufacturing the same. One or more of the semiconductor devices include a substrate having first and second active regions; a P-channel field-effect transistor associated with the first active region and including at least one of the source and drain regions; a N-channel field-effect transistor associated with the second active region and including at least one of the source and drain regions; a first contact pad layer comprising silicon (Si) and SiGe epitaxial layers on the at least one of the source and drain regions of the P-channel field-effect transistor, the SiGe epitaxial layer being sequentially stacked on the Si epitaxial layer; a second contact pad layer comprising silicon (Si) and SiGe epitaxial layers on the at least one of the source and drain regions of the N-channel field-effect transistor, the SiGe epitaxial layer being sequentially stacked on the Si epitaxial layer; an inter-layer insulating film formed on the P-channel and the N-channel field-effect transistors and including first and second contact holes, wherein the first contact hole includes a first lower region that exposes the SiGe epitaxial layer of the first contact pad layer and the second contact hole includes a second lower region that penetrates through the SiGe epitaxial layer of the second contact pad layer to expose the Si epitaxial layer of the second contact pad layer; first and second metal silicide films formed respectively in the first and second lower regions of the contact holes; and contact plugs formed on the first and second metal silicide films and filled in the first and second contact holes.

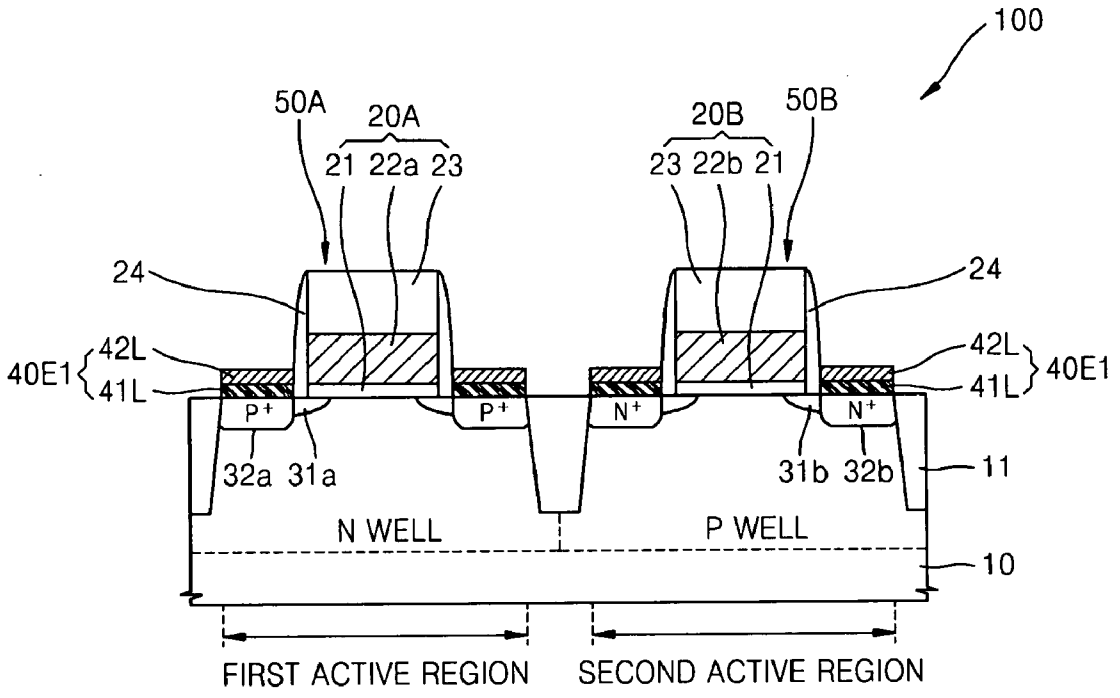


FIG. 1A

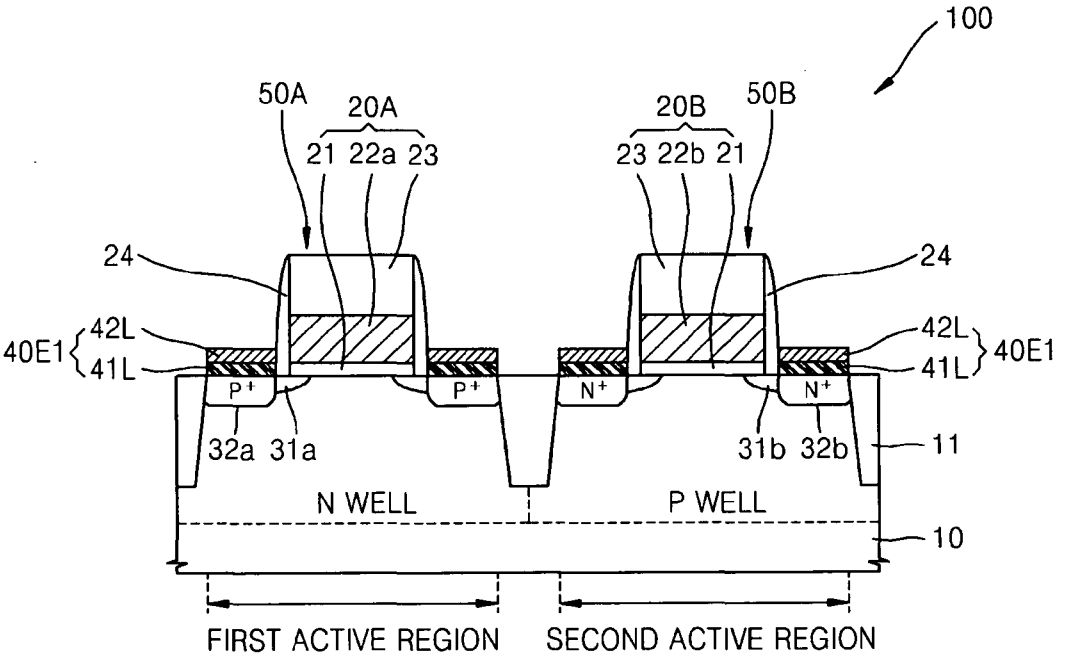

100
50A
20A
21 22a 23
20B
23 22b 21
50B
24
24
40E1
42L
41L
42L
41L
40E1
P+
P+
N+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 1B

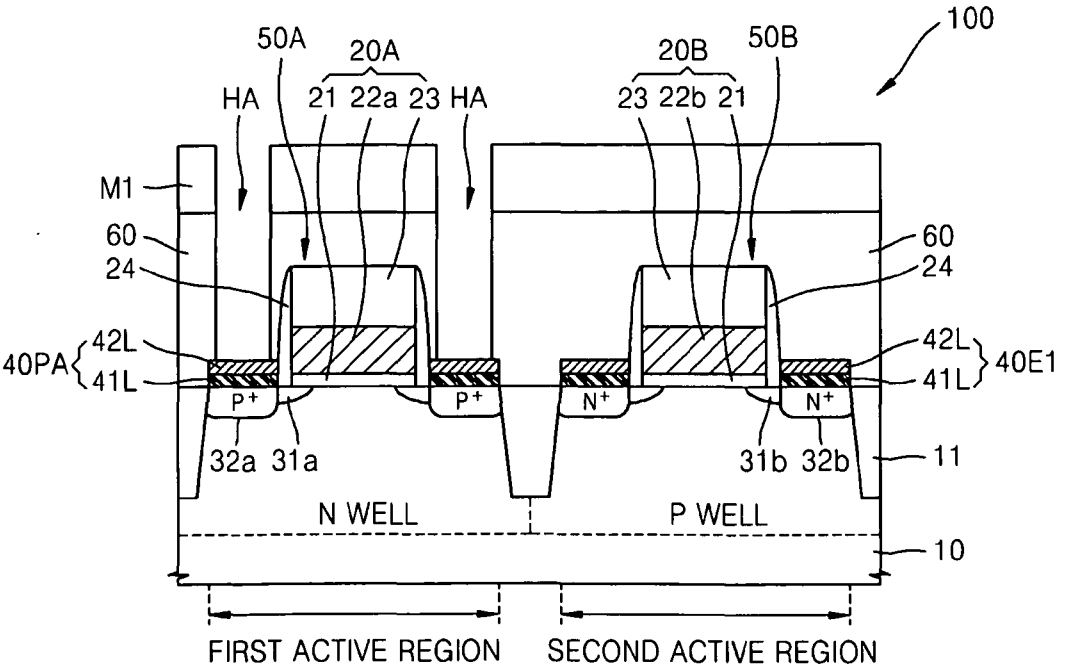

100
50A
20A
HA
21 22a 23 HA
20B
23 22b 21
50B
M1
60
24
60
24
40PA
42L
41L
42L
41L
40E1
P+
P+
N+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 1C

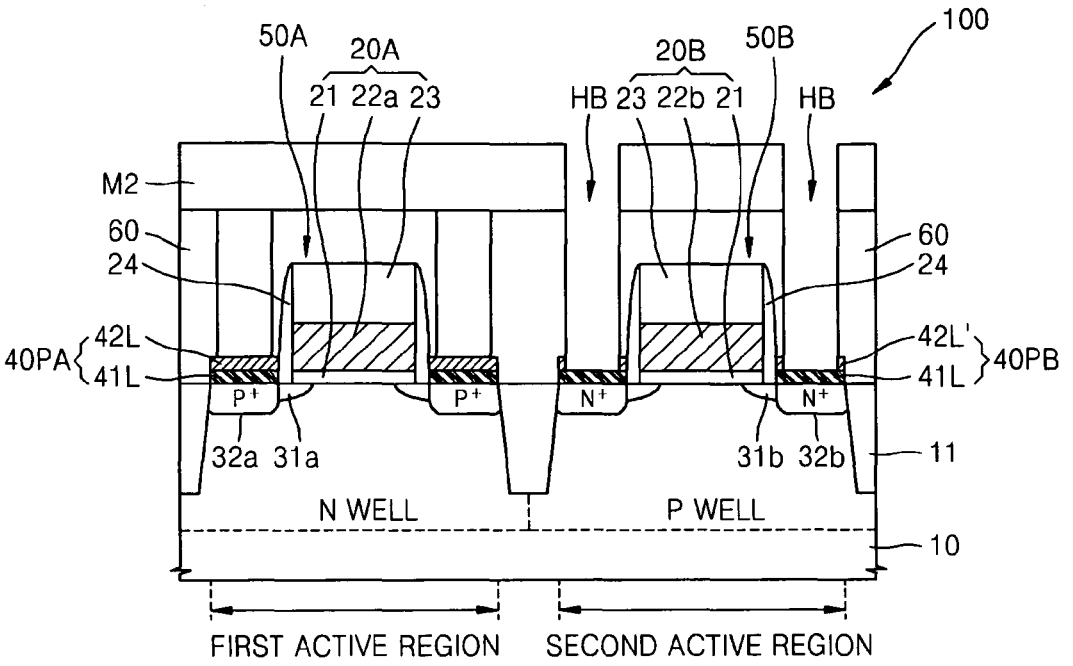

100
50A
20A
21 22a 23
20B
50B
HB 23 22b 21
HB
M2
60
24
40PA
42L
41L
42L'
41L
40PB
P+
P+
N+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 1D

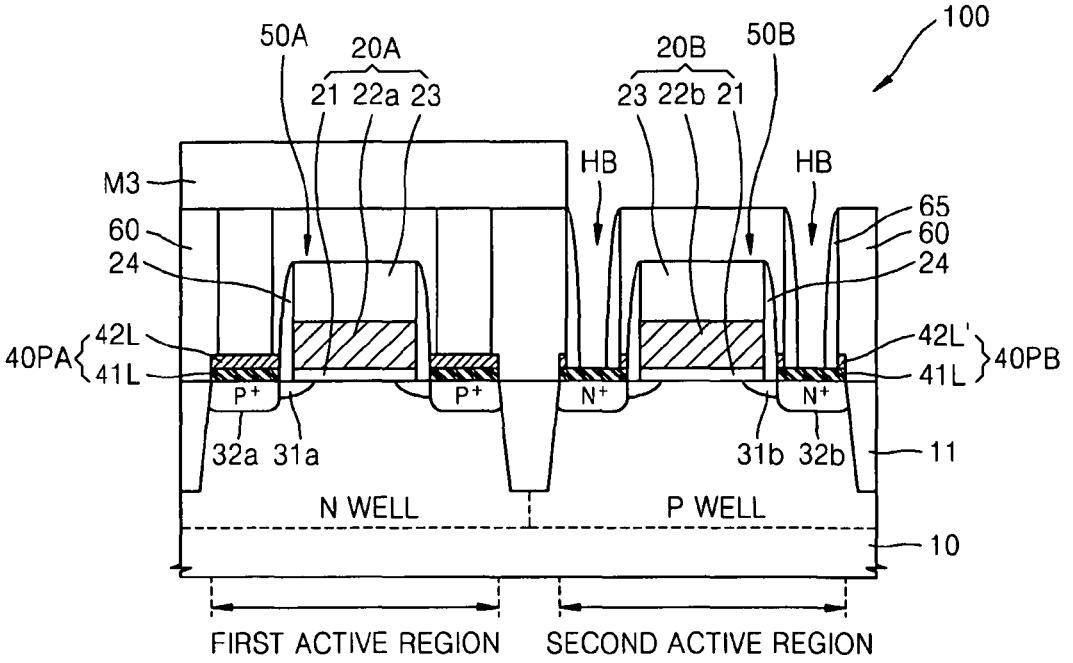

100
50A
20A
21 22a 23
20B
50B
23 22b 21
HB
HB
M3
60
24
65
60
24
40PA
42L
41L
42L'
41L
40PB
P+
P+
N+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 1E

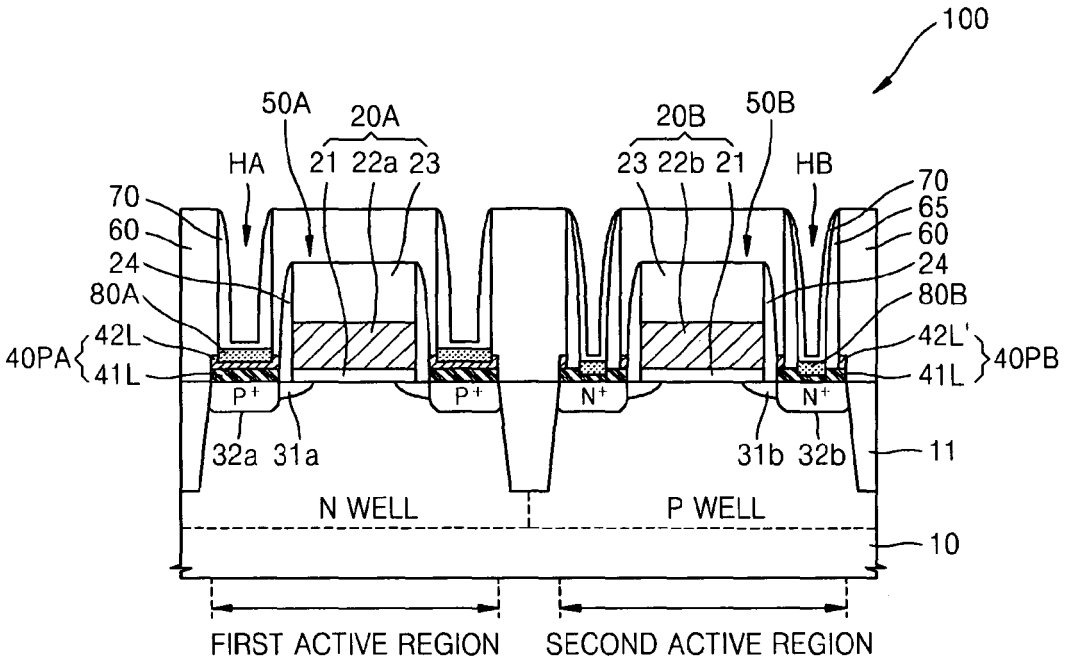

100
50A
20A
20B
50B
HA
21 22a 23
23 22b 21
HB
70
60
24
80A
42L
41L
40PA
70
65
60
24
80B
42L'
41L
40PB
P+
P+
N+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 1F

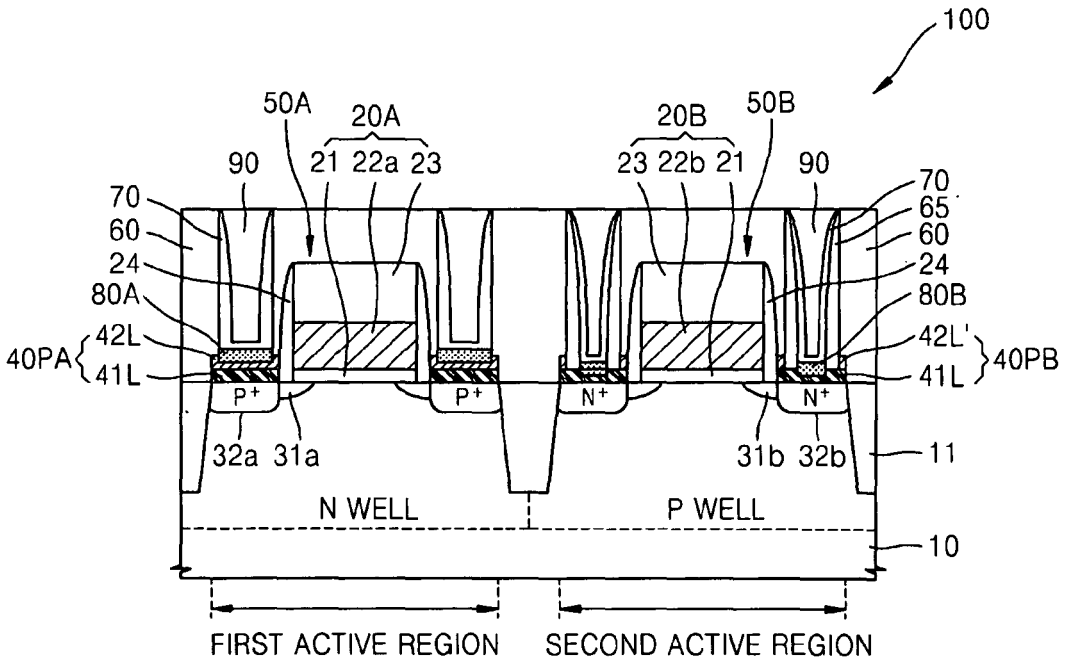

100
50A
20A
20B
50B
90
21 22a 23
23 22b 21
90
70
60
24
80A
42L
41L
40PA
70
65
60
24
80B
42L'
41L
40PB
P+
P+
N+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 2A

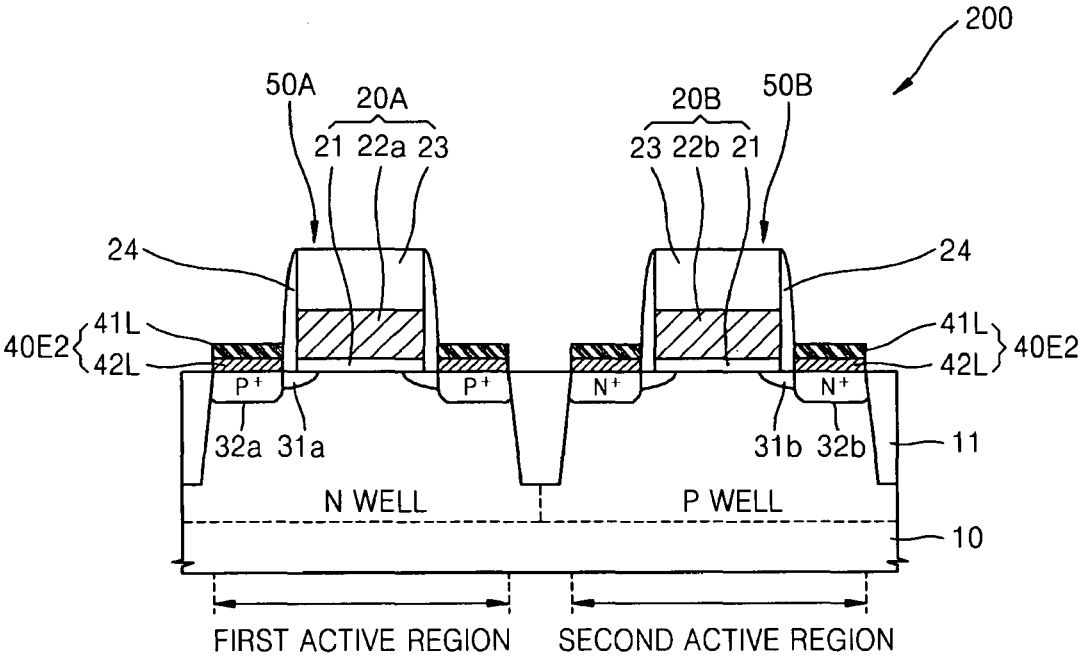

200
50A
20A
21 22a 23
20B
50B
23 22b 21
24
24
40E2
41L
42L
41L
42L
40E2
P+
P+
N+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 2B

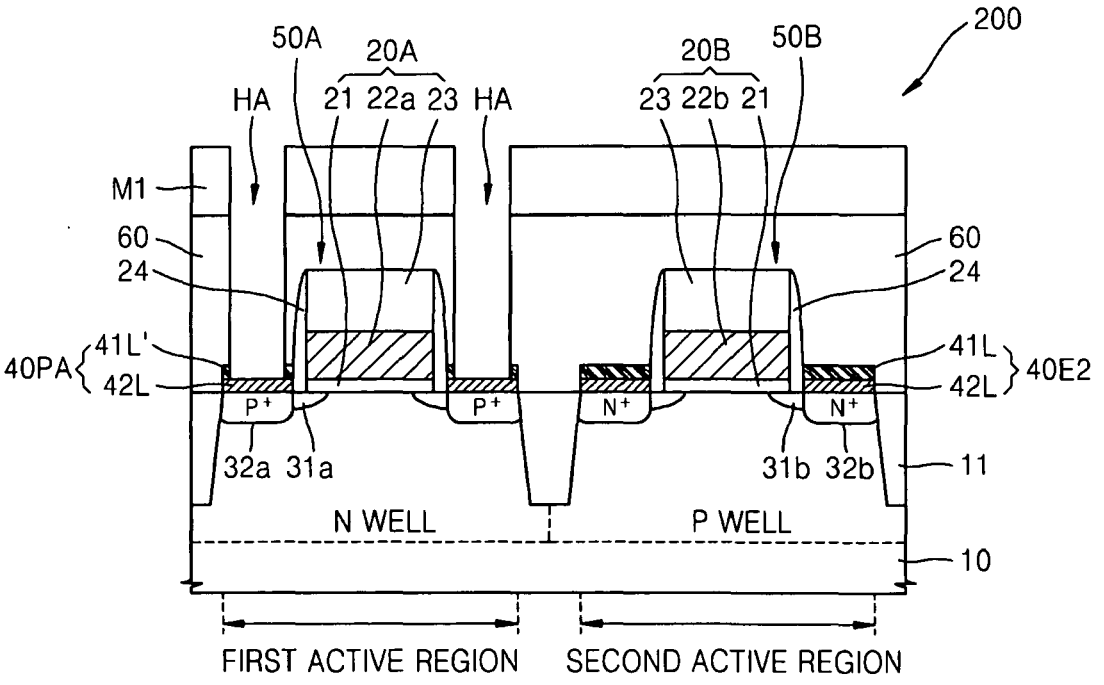

200
50A
20A
HA
21 22a 23
HA
20B
50B
23 22b 21
M1
60
24
60
24
40PA
41L'
42L
41L
42L
40E2
P+
P+
N+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 2C

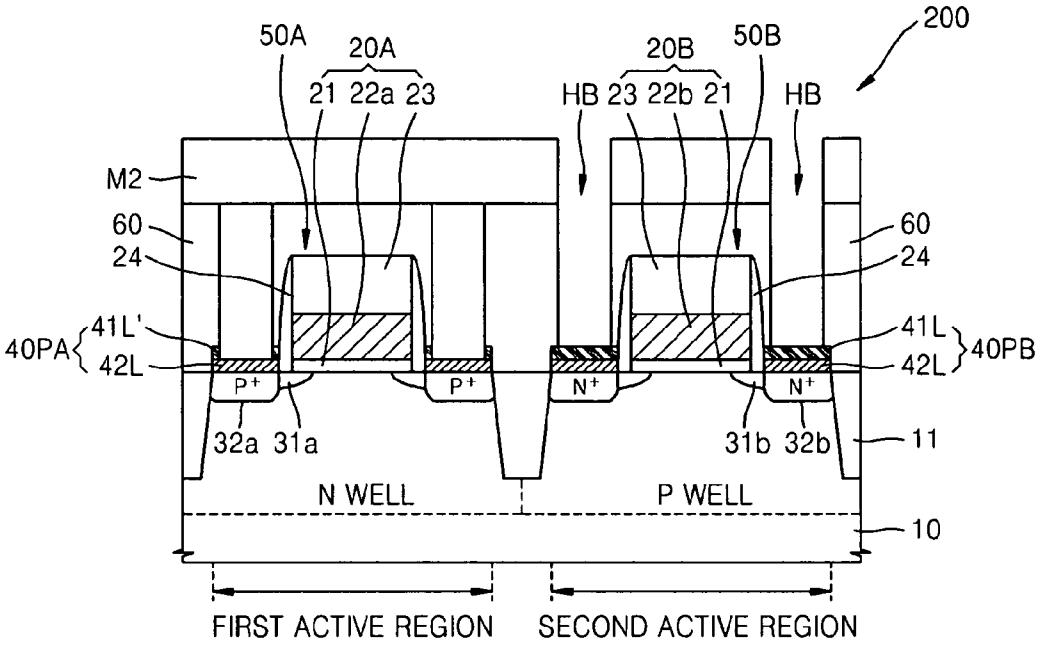

200
50A
20A
21 22a 23
20B
50B
HB 23 22b 21
HB
M2
60
24
40PA
41L'
42L
41L
42L
40PB
P+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 2D

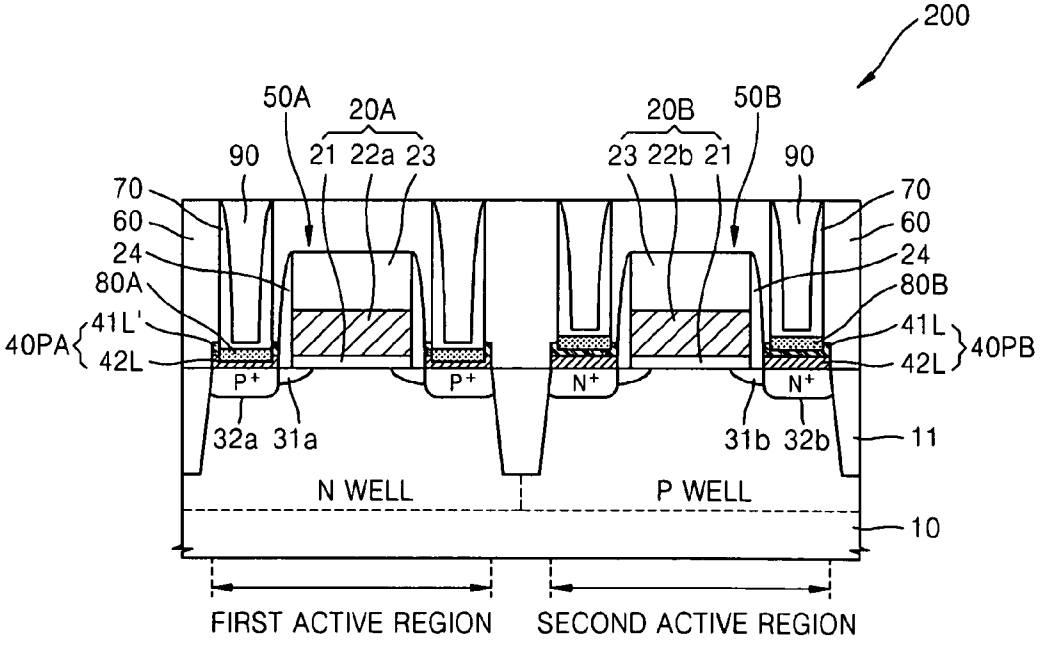

200
50A
20A
90
21 22a 23
20B
50B
23 22b 21
90
70
60
24
80A
80B
40PA
41L'
42L
41L
42L
40PB
P+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 3A

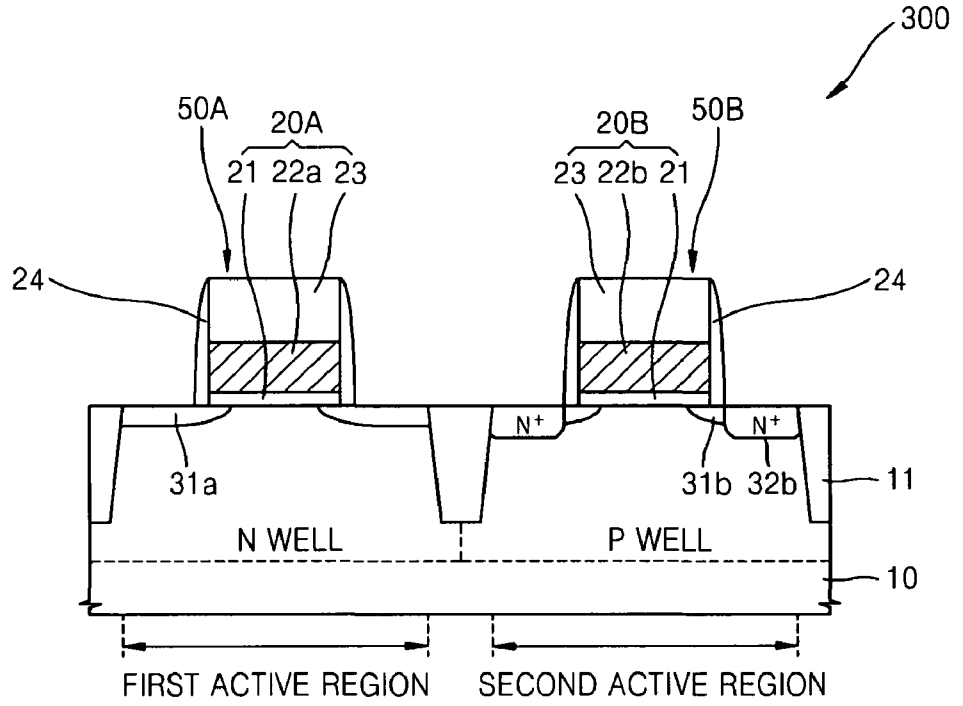

300
50A
20A
21 22a 23
20B
50B
23 22b 21
24
24
N+
N+
31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 3B

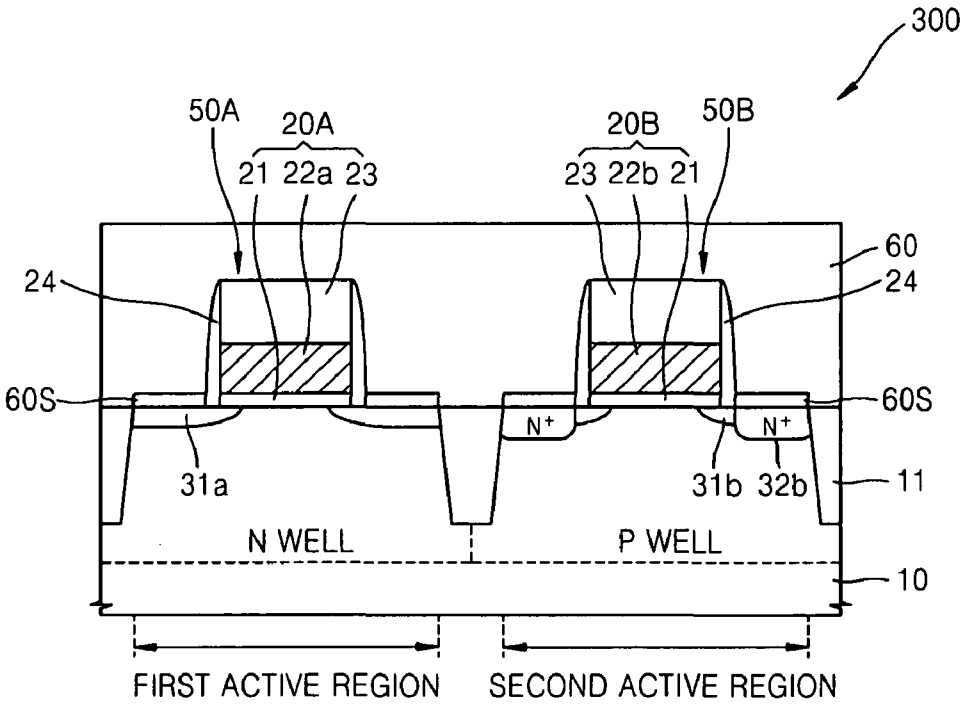

300
50A
20A
21 22a 23
20B
50B
23 22b 21
60
24
24
60S
60S
N+
N+
31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 3C

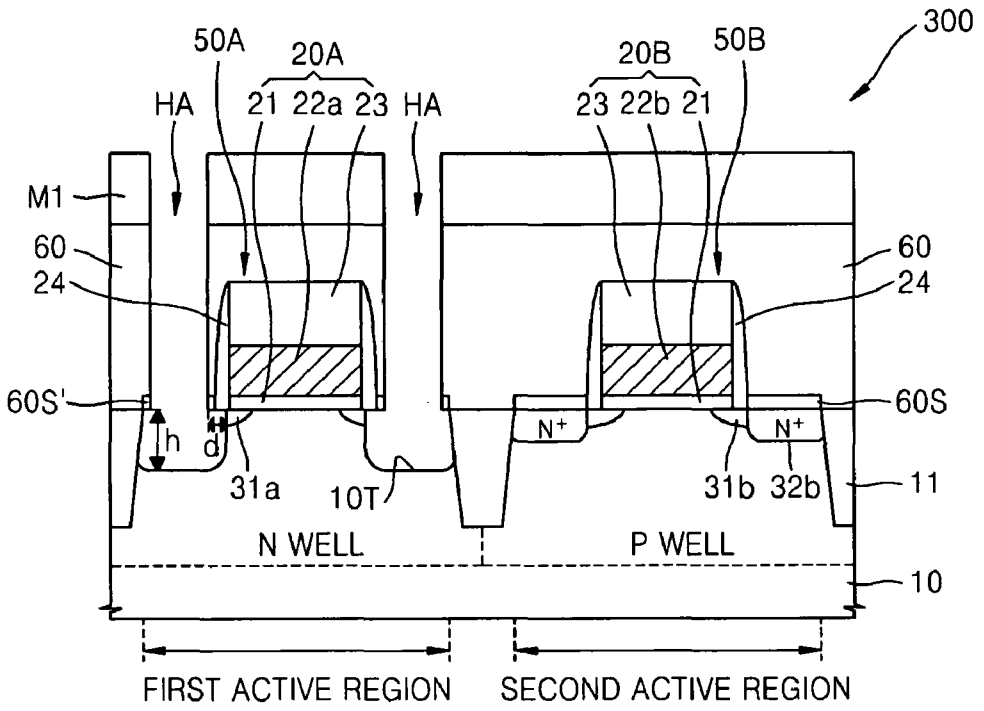

300
50A
20A
HA
21 22a 23 HA
20B
50B
23 22b 21
M1
60
24
60S'
h
d
31a
10T
N+
N+
60S
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 3D

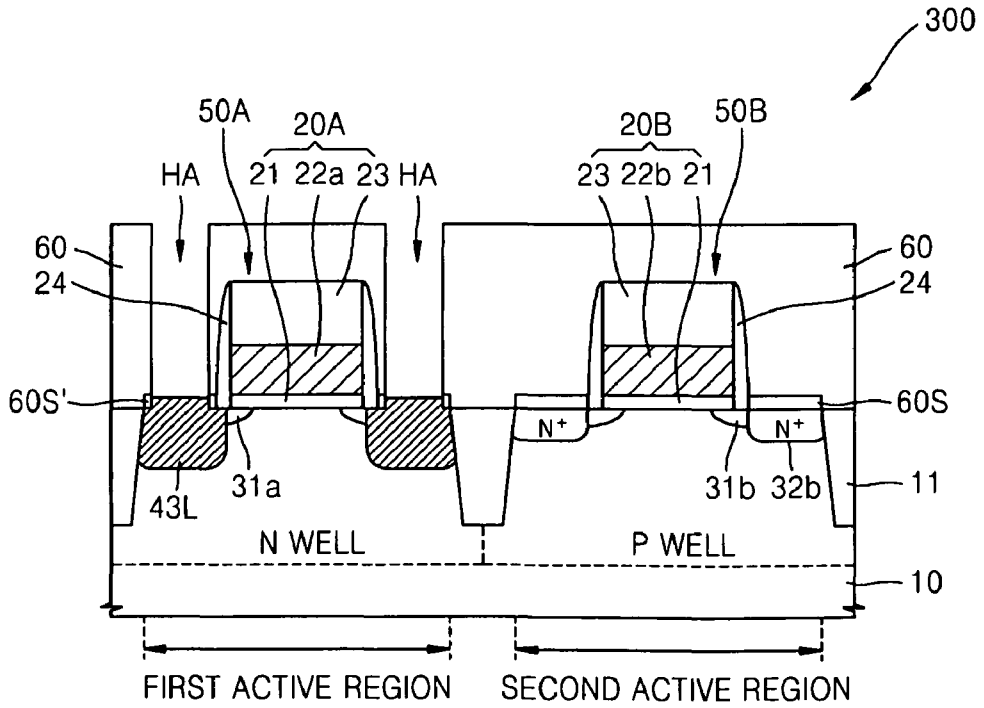

300
50A
20A
HA
21 22a 23 HA
20B
50B
23 22b 21
60
24
60S'
43L
31a
N+
N+
60S
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 3E

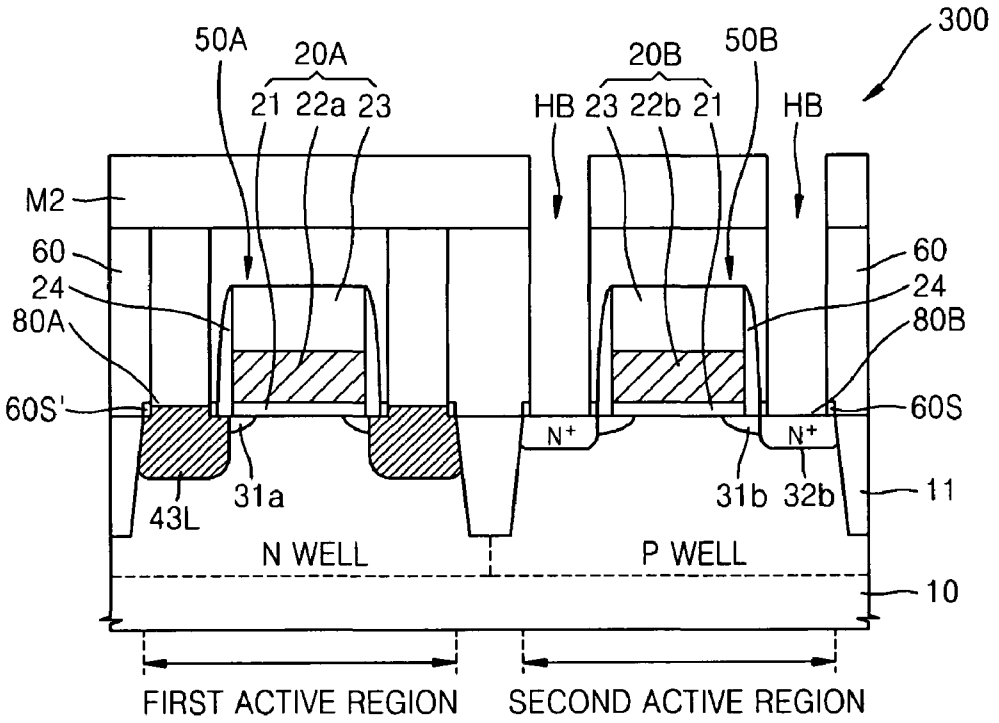

300
50A
20A
21 22a 23
20B
50B
HB 23 22b 21
HB
M2
60
24
80A
60S'
80B
60S
N+
N+
31a
43L
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 3F

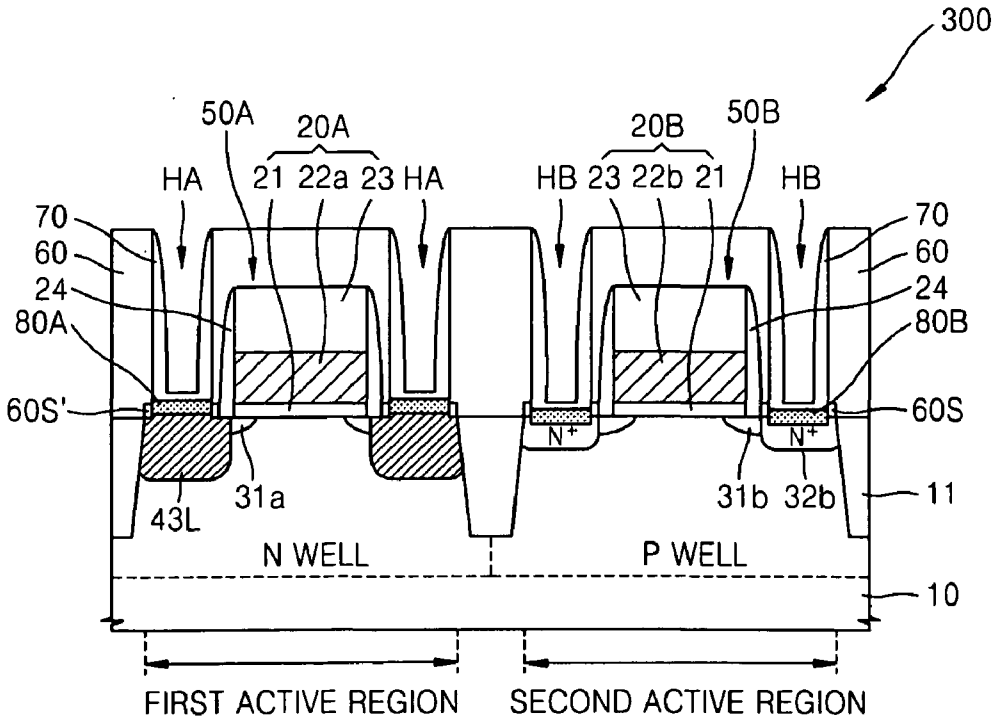

300
50A
20A
HA
21 22a 23 HA
20B
50B
HB 23 22b 21
HB
70
60
24
80A
60S'
80B
60S
N+
N+
31a
43L
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 4

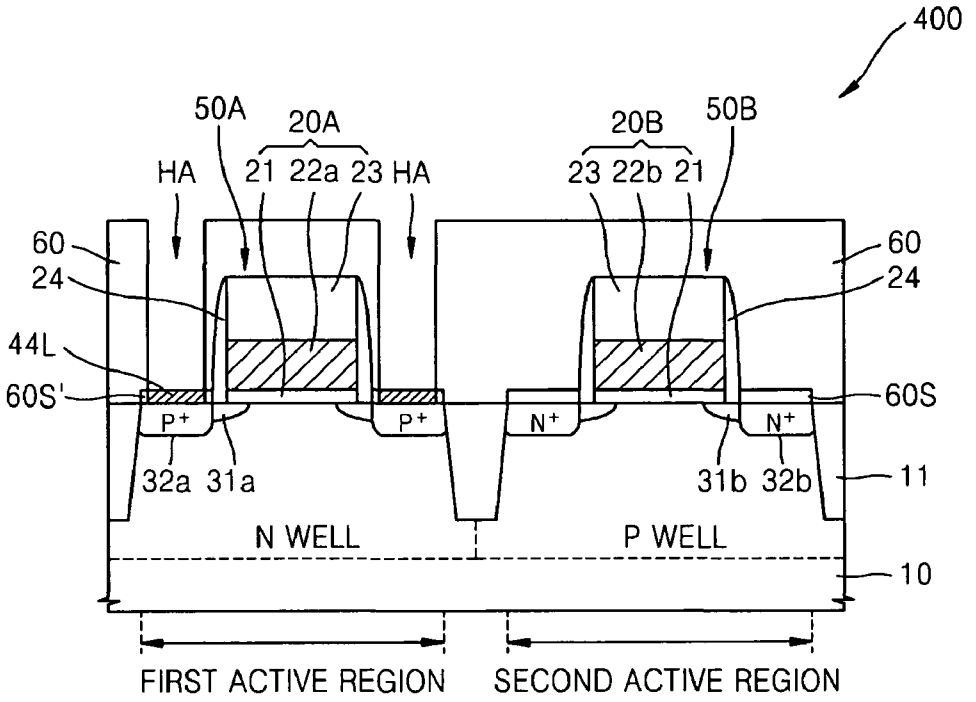
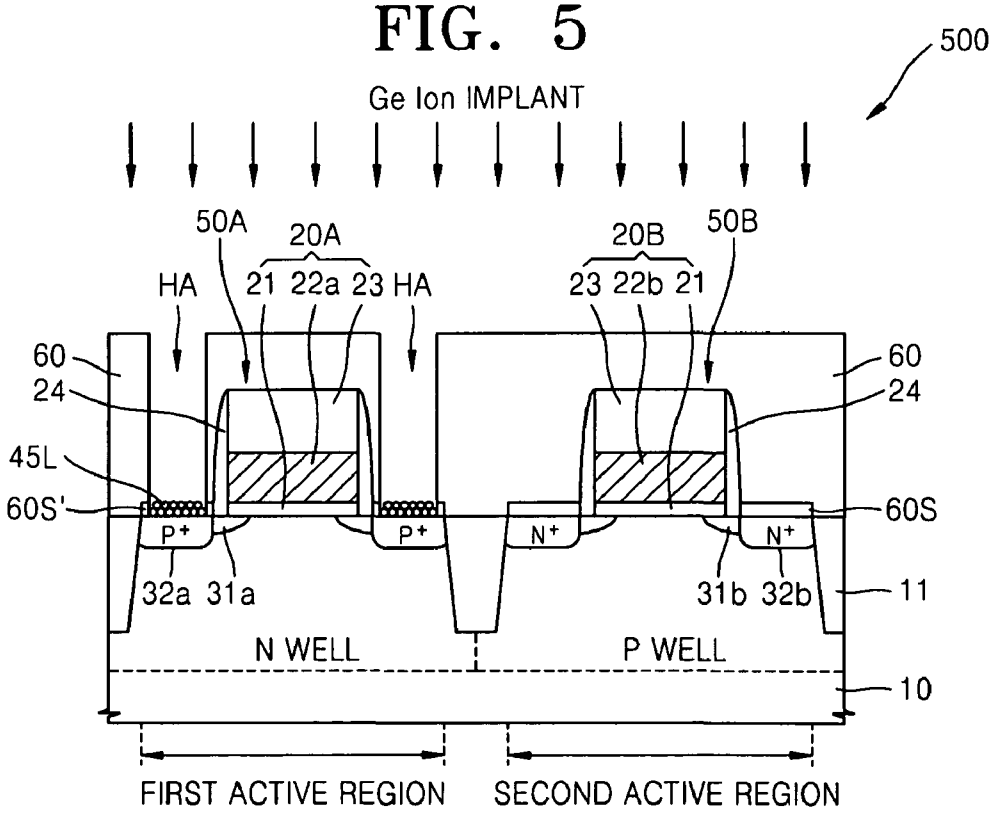

400
50A
20A
20B
50B
HA
21 22a 23 HA
23 22b 21
60
24
44L
60S'
60S
P+
P+
N+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

FIG. 5


500
Ge Ion IMPLANT
50A
20A
20B
50B
HA
21 22a 23 HA
23 22b 21
60
24
45L
60S'
60S
P+
P+
N+
N+
32a 31a
31b 32b
11
N WELL
P WELL
10
FIRST ACTIVE REGION
SECOND ACTIVE REGION

SEMICONDUCTOR DEVICES AND METHODS OF MANUFACTURING THE SAME

PRIORITY STATEMENT

[0001] This application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2008-0115801, filed on Nov. 20, 2008, in the Korean Intellectual Property Office (KIPO), the entire contents of which is incorporated herein by reference.

BACKGROUND

[0002] 1. Field

[0003] Example embodiments relate to semiconductor devices and methods of manufacturing the same, and more particularly, to field-effect transistors including one or more low resistance contacts and methods of manufacturing the same.

[0004] 2. Description of the Related Art

[0005] Electronic devices such as computers, cellular phones, and digital cameras require an active element in order to implement logic circuits. A complementary metal-oxide semiconductor (CMOS) transistor having low power driving and high linear characteristics has been commonly used as the active element.

[0006] Currently, design rules of semiconductor devices have been narrowed in order to manufacture electronic products with lighter weight and small and/or decreased form factor. Accordingly, a contact area of a source/drain region of the CMOS transistor has been reduced. Because the reduction of the contact area increases contact resistance, reduction of contact resistance is an important issue with respect to high integration density CMOS transistor devices.

[0007] The CMOS transistor includes P-channel and N-channel metal-oxide semiconductor field-effect transistors (MOSFETs) connected to each other in series. In order to provide a low resistance contact to a CMOS transistor, the P-channel and N-channel MOSFETs need to be provided with a contact having a low Schottky barrier. Conventionally, a technology for reducing the Schottky barrier of a contact by applying metal silicide films having different work functions respectively to P-channel and N-channel MOSFETs has been suggested.

[0008] In order to apply different metal silicide films to the P-channel and N-channel MOSFETs, the silicide films of the P-channel and N-channel MOSFETs are independently formed by different processes. For example, in order to form a metal silicide film having a high work function (e.g., a PtSi film) in the P-channel MOSFET, a mask for completely blocking the N-channel MOSFET may be initially formed after which a high work function film may be formed in the P-channel MOSFET. In order to form a metal silicide film having a low work function (e.g., an ErSi film) in the N-channel MOSFET, the mask for blocking the N-channel MOSFET has to be removed so as to expose the N-channel MOSFET.

[0009] The process of forming a mask selectively for blocking one of P-channel and N-channel MOSFETs and then forming silicide films having different metals at the P-channel and N-channel MOSFETs through separate deposition processes requires additional photolithography and etching processes, thereby increasing process complexity and cost.

SUMMARY

[0010] Example embodiments provide semiconductor devices having reduced contact resistance for both P-channel and N-channel metal-oxide semiconductor field-effect transistors (MOSFETs), by including a silicide film in an N-Channel MOSFET having a different composition than a silicide film in a P-channel MOSFET, between source/drain regions and contact plugs of the MOSFETs. Example embodiments provide methods of manufacturing semiconductor devices without performing a blocking process.

[0011] According to example embodiments, there is provided a semiconductor device. The semiconductor device includes source regions, drain regions, first and second contact pad layers including silicon (Si) and SiGe epitaxial layers, the Si and SiGe epitaxial layers on the source and drain regions.

[0012] The semiconductor device may include an interlayer insulating film and first and second contact holes. According to example embodiments, the first contact hole may penetrate the interlayer insulating film and may include a first lower region that exposes the SiGe epitaxial layer of the first contact pad layer. The second contact hole may penetrate the interlayer insulating film and may include a second lower region penetrating through the SiGe epitaxial layer of the second contact pad layer, exposing the Si epitaxial layer. A diffusion barrier may be included between sidewalls of the second contact hole and the second metal silicide film. According to example embodiments, the first contact hole may penetrate the interlayer insulating film and may include a first lower region penetrating through the Si epitaxial layer of the first contact pad layer, exposing the SiGe epitaxial layer. The second contact hole may penetrate the interlayer insulating film and may include a second lower region exposing the Si epitaxial layer of the second contact pad layer. At least a portion of the SiGe epitaxial layer of the first contact pad layer may be buried in the first active region.

[0013] The semiconductor device may include a substrate having first and second active regions. P-channel and N-channel field-effect transistors may be on the first and second active regions, respectively, the P-channel and N-channel field-effect transistors including at least one of the first and second source and drain regions. The interlayer insulating film may be on the P-channel and the N-channel field-effect transistors. First and second metal silicide films may be respectively in the first and second lower regions of the contact holes. The first metal silicide film may contain germanium (Ge) and the second metal silicide film may not contain Ge. Contact plugs may be on the first and second metal silicide films and filled in the first and second contact holes. At least one of the first and second contact pad layers may extend in a direction parallel to a principal plane of the substrate and may extend over a region of a device isolation film defining the first and second active regions.

[0014] According to example embodiments, there is provided a semiconductor device. The semiconductor device includes source and drain regions, first and second contact pad layers including a silicon (Si) epitaxial layer and a germanium (Ge) atomic layer, where the Si epitaxial layer and Ge atomic layer are on the source and drain regions.

[0015] The semiconductor device may include an interlayer insulating film. First and second contact holes may

penetrate the interlayer insulating film. The first contact hole may include a first lower region that exposes the Ge atomic layer of the first contact pad layer. The second contact hole may include a second lower region that penetrates through the Ge atomic layer of the second contact pad layer and exposes the Si epitaxial layer. The semiconductor device may include a substrate including first and second active regions. P-channel and N-channel field-effect transistors may be respectively on the first and second active regions and may include at least one of the source and drain regions. The interlayer insulating film may be on the P-channel and the N-channel field-effect transistors. First and second metal silicide films may be respectively in the first and second lower regions of the contact holes, where the first metal silicide film may contain Ge and the second metal silicide film may not contain Ge. Contact plugs may be on the first and second metal silicide films and filled in the first and second contact holes.

[0016] According to example embodiments, there is provided a method of manufacturing a semiconductor device. The method includes forming a first active region for a P-channel field-effect transistor and a second active region for an N-channel field-effect transistor in a substrate, forming a first gate stack on the first active region, forming a second gate stack on the second active region, simultaneously forming first and second layers on regions of the first and second active regions where the first and second gate stacks are not formed, the first and second layers including a silicon germanium (SiGe) epitaxial layer sequentially stacked on a silicon (Si) epitaxial layer.

[0017] Example embodiments may include forming an interlayer insulating film to cover upper regions of the first and second gate stacks and the first and second layers. A first contact hole may be formed in the interlayer insulating film, the first contact hole including a first lower portion to expose the SiGe epitaxial layer of the first layer. A second contact hole may be formed in the interlayer insulating film, the second contact hole including a second lower region penetrating through the SiGe epitaxial layer of the second layer and exposing the Si epitaxial layer. First and second metal silicide films may be formed respectively in the first and second lower regions of the contact holes, where the first metal silicide film may include germanium (Ge) and the second metal silicide film may not include Ge. Contact plugs may be formed on the first and second metal silicide films so as to be filled in the first and second contact holes

[0018] According to example embodiments, there is provided a method of manufacturing a semiconductor device. The method includes forming a first active region for a P-channel field-effect transistor and a second active region for an N-channel field-effect transistor in a substrate, forming a first gate stack on the first active region, forming a second gate stack on the second active region and simultaneously forming first and second layers on regions of the first and second active regions where the first and second gate stacks are not formed, the first and second layers including a silicon (Si) epitaxial layer sequentially stacked on a silicon germanium (SiGe) layer.

[0019] An interlayer insulating film may be formed to cover upper regions of the first and second gate stacks and the first and second layers. A first contact hole may be formed in the interlayer insulating film, the first contact hole including a first lower region penetrating through the Si epitaxial layer of the first layer and exposing the SiGe epitaxial layer. A second contact hole may be formed in the interlayer insulating film, the second contact hole including a second lower region exposing the Si epitaxial layer of the second layer. First and second metal silicide films may be respectively formed in the first and second lower regions, simultaneously, where the first metal silicide film may include germanium (Ge) and the second metal silicide film may not include Ge. Contact plugs may be formed on the first and second metal silicide films so as to be filled in the first and second contact holes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Example embodiments will be more clearly understood from the following brief description taken in conjunction with the accompanying drawings. FIGS. **1A-5** represent non-limiting, example embodiments as described herein.

[0021] FIGS. **1A-1F** are cross-sectional diagrams illustrating methods of manufacturing a semiconductor device according to example embodiments;

[0022] FIGS. **2A-2D** are cross-sectional diagrams illustrating methods of manufacturing a semiconductor device according to example embodiments;

[0023] FIGS. **3A-3F** are cross-sectional diagrams illustrating methods of manufacturing a semiconductor device according to example embodiments;

[0024] FIG. **4** is a cross-sectional diagram illustrating methods of manufacturing a semiconductor device according to example embodiments; and

[0025] FIG. **5** is a cross-sectional diagram illustrating methods of manufacturing a semiconductor device according to an example embodiment.

[0026] It should be noted that these Figures are intended to illustrate the general characteristics of methods, structure and/or materials utilized in certain example embodiments and to supplement the written description provided below. These drawings are not, however, to scale and may not precisely reflect the precise structural or performance characteristics of any given embodiment, and should not be interpreted as defining or limiting the range of values or properties encompassed by example embodiments. For example, the relative thicknesses and positioning of molecules, layers, regions and/or structural elements may be reduced or exaggerated for clarity. The use of similar or identical reference numbers in the various drawings is intended to indicate the presence of a similar or identical element or feature.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0027] Example embodiments will now be described more fully with reference to the accompanying drawings, in which example embodiments are shown. Example embodiments may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the concept of example embodiments to those of ordinary skill in the art. In the drawings, the thicknesses of layers and regions are exaggerated for clarity. Like reference numerals in the drawings denote like elements, and thus their description will be omitted.

[0028] It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected"

or "directly coupled" to another element, there are no intervening elements present. Like numbers indicate like elements throughout. As used herein the term "and/or" includes any and all combinations of one or more of the associated listed items. Other words used to describe the relationship between elements or layers should be interpreted in a like fashion (e.g., "between" versus "directly between," "adjacent" versus "directly adjacent," "on" versus "directly on").

[0029] It will be understood that, although the terms "first", "second", etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of example embodiments.

[0030] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated **90** degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0031] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of example embodiments. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0032] Example embodiments are described herein with reference to cross-sectional illustrations that are schematic illustrations of idealized embodiments (and intermediate structures) of example embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, example embodiments should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, an implanted region illustrated as a rectangle may have rounded or curved features and/or a gradient of implant concentration at its edges rather than a binary change from implanted to non-implanted region. Likewise, a buried region formed by implantation may result in some implantation in the region between the buried region and the surface through which the implantation takes place. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to limit the scope of example embodiments.

[0033] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which example embodiments belong. It will be further understood that terms, such as those defined in commonly-used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein. As used herein, a field-effect transistor can be interchangeably used with a metal-oxide semiconductor field-effect transistor (MOSFET), a channel MOSFET, or a metal-insulator-semiconductor field-effect transistor (MISFET). Although a field-effect transistor having a flat channel is described by example herein, it will be understood by one of ordinary skill in the art that many configurations are possible, for example, a metal-oxide semiconductor (MOS) transistor having a pin-type or recessed channel.

[0034] FIGS. **1**A-**1**F are cross-sectional diagrams illustrating methods of manufacturing a semiconductor device **100** according to example embodiments. Referring to FIG. **1**A, a substrate **10** may include a first active region in which a P-channel field-effect transistor **50**A is to be formed and a second active region in which an N-channel field-effect transistor **50**B is to be formed. The substrate **10** may be a substrate that is subjected to a semiconductor device manufacturing process, for example, a silicon (Si) monocrystalline substrate, a silicon-on-insulator (SOI) substrate, and/or a silicon-on-sapphire (SOS) substrate.

[0035] The first and second active regions of the substrate **10** may be defined by a device isolation film **11** (e.g., a shallow trench isolation (STI) film). The substrate **10** may include N and P wells respectively in the first and second active regions. If a specific conductive type substrate is used, one of the N and P wells may be omitted. For example, a P-channel substrate may be used as the substrate **10** and only the N well may be formed in the first active region of the substrate **10**, or vice versa. First and second gate stacks **20**A and **20**B may be respectively formed on the first and second active regions. The first and second gate stacks **20**A and **20**B may be formed by forming a gate insulating layer **21**, gate conductive films **22***a* and **22***b*, and optionally a capping film **23** on the first and second active regions, and then patterning the gate insulating layer **21**, the gate conductive films **22***a* and **22***b*, and the capping film **23**. The capping film **23** may protect the gate insulating layer **21** and the gate conductive films **22***a* and **22***b*.

[0036] The gate insulating layer **21** may include a silicon oxide film. However, example embodiments are not limited to a silicon oxide film. The gate insulating layer **21** may include a high-k dielectric film having a dielectric constant greater than that of the silicon oxide film. For example, the gate insulating layer may include a silicon nitride (SiNx) film, a tantalum oxide (TaOx) film, a hafnium oxide (HfOx) film, an aluminum oxide (AlOx) film, and/or a zinc oxide (ZnOx) film.

[0037] Each of the gate conductive films **22***a* and **22***b* may be, for example, a heavily-doped polysilicon film, a metal film (e.g., a tungsten (W), nickel (Ni), molybdenum (Mo) and/or cobalt (Co) film), a metal silicide film, or any combination thereof For example, one combination included in the

gate conductive films **22***a* and **22***b* may be a stacked film including a heavily-doped polysilicon film and a nickel cobalt silicide film. According to example embodiments, the gate conductive films **22***a* and **22***b* in the first and second gate stacks **20**A and **20**B may be materials having different work functions. For example, the gate conductive film **22***a* of the first gate stack **20**A may be a metal silicide film and the gate conductive film **22***b* of the second gate stack **20**B may be a metal film. The capping film **23** may be, for example, a silicon nitride film or a silicon oxide film.

[0038] According to one or more example embodiments, in order to prevent a hot carrier effect that may occur in drain regions of the P-channel and N-channel field-effect transistors **50**A and **50**B, lightly-doped drain (LDD) regions **31***a* and **31***b*, which may also be referred to as shallow source/drain extension (SDE) regions, may be formed by using the first and second gate stacks **20**A and **20**B as ion implantation masks. A gate spacer **24** may be formed on sidewalls of the first and second gate stacks **20**A and **20**B. The gate spacer **24** may be, for example, silicon nitride. Heavily-doped source/drain regions **32***a* and **32***b* may be formed by, for example, a high-concentration ion implantation into the first and second active regions using the first and second gate stacks **20**A and **20**B and the gate spacer **24** as a mask.

[0039] A Si epitaxial layer **41**L may be formed simultaneously on the exposed source/drain regions **32***a* and **32***b* of the first and second active regions. A SiGe epitaxial layer **42**L may be formed simultaneously on the Si epitaxial layer **41**L of the first and second active regions. The thickness of the Si epitaxial layer **41**L may be, for example, from about 10 Å to about 500 Å. The thickness of the SiGe epitaxial layer **42**L may be, for example, from about 30 Å to about 500 Å. The molarity of germanium (Ge) in the SiGe epitaxial layer **42**L may be from about 3% to about 50%.

[0040] The Si and SiGe epitaxial layers **41**L and **42**L may be formed by, for example, selective epitaxial growth (SEG). The Si epitaxial layer **41**L may be formed by, for example, a chemical vapor deposition (CVD) at about 700° C. using a Si-containing gas (e.g., SiH4, Si2H6, and/or SiH2Cl2). The SiGe epitaxial layer **42**L may be formed by, for example, growing SiGe crystal films on the Si epitaxial layer **41**L using a mixed gas of a silicon-containing gas and a Ge-containing gas (e.g., GeH4 and/or GeH). However, example embodiments are not limited thereto. The Si and SiGe epitaxial layers **41**L and **42**L may also be formed by, for example, molecular beam epitaxy.

[0041] According to one or more embodiments, the Si and SiGe epitaxial layers **41**L and **42**L, which may grow in a direction perpendicular to the corresponding active regions, may also grow in a direction parallel to a principal plane of the substrate **10** so as to extend over a portion of the device isolation film **11**. The extended Si and SiGe epitaxial layers **41**L and **42**L may secure photolithography process margins for subsequent processes (e.g., contact plug formation) and may reduce contact resistance due to the increased area of the upper surface of the Si and SiGe epitaxial layers **41**L and **42**L.

[0042] In order to provide conductivity to a double epitaxial layer **40**E**1** including the Si and SiGe epitaxial layers **41**L and **42**L on the first and second active regions, an ion implant may be performed with an ion implantation mask (not shown). For example, the double epitaxial layer **40**E**1** of the first active region may be doped by a group III element such as boron (B) and the double epitaxial layer **40**E**1** of the second active region may be doped by a group V element such as phosphorus (P) or arsenic (As). Alternatively, as described below with reference to FIGS. **1**B and **1**C, the ion implantation may be performed on a contact pad layer **40**PA of the first active region, which is exposed after forming first contact holes HA, and may be performed on a contact pad layer **40**PB of the second active region, which is exposed after forming second contact holes HB.

[0043] Referring to FIG. **1**B, an interlayer insulating film **60** may be formed to cover upper regions of the P-channel and N-channel field-effect transistors **50**A and **50**B and the double epitaxial layer **40**E**1**. The interlayer insulating film **60** may be, for example, silicon oxide, phosphosilicate glass (PSG), and/or borophosphosilicate glass (BPSG). As another example, the interlayer insulating film **60** may be formed of a low-k material such as impurity-doped CVD glass. However, example embodiments are not limited to the above materials.

[0044] The first contact holes HA may be formed in one of the first and second active regions, for example, the first active region as illustrated in FIG. **1**B. In order to form the first contact holes HA, a mask M**1** for exposing regions in which the first contact holes HA are to be formed, may be formed on the interlayer insulating film **60** by performing a photolithography process. The first contact holes HA may be formed in the interlayer insulating film **60** by, for example, performing a plasma dry etch. By controlling an etch depth of the first contact holes HA, a lower region of the first contact holes HA may expose the SiGe epitaxial layer **42**L. The contact pad layer **40**PA for the P-channel field-effect transistor **50**A may be formed.

[0045] Referring to FIG. **1**C, a mask M**2** for exposing regions in which the second contact holes HB are to be formed may be formed on the interlayer insulating film **60** by performing a photolithography process. The second contact holes HB may be formed in the interlayer insulating film **60** by, for example, performing a plasma dry etch. By controlling an etch depth of the second contact holes HB, a lower region of the second contact holes HB may penetrate through a SiGe epitaxial layer **42**L to expose the underlying Si epitaxial layer **41**L. The contact pad layer **40**PB for the N-channel field-effect transistor **50**B may be formed. If a plasma dry etch is used, the plasma dry etch for the second contact holes HB may be continuously performed on the interlayer insulating film **60** and the SiGe epitaxial layer **42**L by using the same etch gas. In some cases, the interlayer insulating film **60** and the SiGe epitaxial layer **42**L may be discontinuously etched by using different etch gases in consideration of etch selectivity therebetween.

[0046] Referring to FIG. **1**D, a diffusion barrier **65** may be formed on sidewalls of the second contact holes HB to cover the exposed SiGe epitaxial layer **42**L'. The diffusion barrier **65** may be formed to prevent a silicide reaction between the exposed SiGe epitaxial layer **42**L' and a barrier metal layer (see a reference numeral **70** of FIG. **1**E). As illustrated in FIG. **1**D, the diffusion barrier **65** may be a spacer formed on the sidewalls of the second contact holes HB. The thickness of the spacer may be from about 20 Å to about 500 Å. The spacer may be, for example, a silicon nitride film having etch selectivity with respect to the interlayer insulating film **60**. The silicon nitride film may be formed, for example, in the second contact holes HB after forming a mask M**3** for exposing the second contact holes HB and the insulating film **60** of the second active region. The diffusion barrier **65** may be formed as a spacer that covers the sidewalls of the second contact holes HB by performing an etch back process, where etch

selectivity exists between the interlayer insulating film **60** and the silicon nitride film. However, example embodiments are not limited to the above examples. The diffusion barrier **65** may be formed on the sidewalls of the first and second contact holes HA and HB without forming the mask M**3**.

[0047] Referring to FIG. **1**E, barrier metal layers **70** may be formed in the first and second contact holes HA and HB. The barrier metal layers **70** may be formed, for example, by performing a blanket deposition process without using a mask. The barrier metal layers **70** may be formed by performing, for example, a CVD or atomic layer deposition (ALD) process capable of forming a conformal film. The barrier metal layers **70** may also be formed, for example, by performing a physical vapor deposition (PVD) (e.g., a sputter process). The barrier metal layers **70** may be, for example, titanium (Ti), Nickel (Ni), cobalt (Co), palladium (Pd), platinum (Pt), and/or alloys thereof The thickness of the barrier metal layers **70** may be from about 10 Å to about 400 Å.

[0048] Silicide films **80**A and **80**B may be respectively formed between the barrier metal layers **70** and the exposed SiGe and Si epitaxial layers **42**L and **41**L by performing, for example, thermal processing at a relatively low temperature (e.g., from about 300° C. to about 650° C.). According to one or more example embodiments, the silicide films **80**A and **80**B may locally remain only on the lower portions of the first and second contact holes HA and HB by removing the residue of barrier metal layers **70** which do not participate in the silicide reaction, by performing an appropriate etch.

[0049] The silicide films **80**A and **80**B having different compositions may be formed in the first and second contact holes HA and HB. The silicide film **80**A in the first contact holes HA may be a M(Si1-yGey) film containing Ge due to the SiGe epitaxial layer **42**L and the silicide film **80**B in the second contact holes HB may be a MSi film due to the exposed Si epitaxial layer **41**L. As illustrated in FIG. **1**F, contact plugs **90** may be formed on the silicide films **80**A and **80**B in the first and second contact holes HA and HB (e.g., to fill the first and second contact holes **80**A and **80**B). The contact plugs **90** may include, for example, tungsten (W), aluminum (Al), copper (Cu), molybdenum (Mo), titanium (Ti), tantalum (Ta), ruthenium (Ru), and/or alloys thereof. However, example embodiments are not limited to the above materials. The contact plugs **90** may be, for example, a conductive nitride of the above-mentioned metals. The semiconductor device **100** may include additional circuitry, for example, power supply circuitry and interconnections to the contact plugs **90**. The semiconductor device **100** may function as, for example, a P-channel MOSFET in a peripheral circuit region of dynamic random access memory (DRAM) and an N-channel MOSFET in the peripheral circuit region and a memory cell region.

[0050] On both of the first and second active regions, the silicide films **80**A and **80**B that contact the contact plugs **90** may reduce the height of Schottky barriers in contact regions and thus reduce sheet resistance. In the first active region on which the P-channel field-effect transistor **50**A may be formed, during the silicide reaction between the SiGe epitaxial layer **42**L and the barrier metal layers **70**, Si having reactivity higher than that of Ge reacts more dominantly than Ge. As a result, concentration of Ge may increase at an interface between the SiGe epitaxial layer **42**L and the barrier metal layers **70**. As the concentration of Ge increases, a band gap of contact regions may be reduced. The reduced band gap may reduce the height of Schottky barriers and thus contact resistance of the P-channel field-effect transistor **50**A may be considerably reduced.

[0051] According to example embodiments, for the P-channel and N-channel field-effect transistors **50**A and **50**B, the silicide films **80**A and **80**B having low Schottky barriers may be simultaneously formed and formed without performing a blocking process, by forming the double epitaxial layer **40**E**1** for each of the P-channel and N-channel field-effect transistors **50**A and **50**B simultaneously, and by controlling depths of the first and second contact holes HA and HB that expose the double epitaxial layer **40**E**1** formed under the interlayer insulating film **60**.

[0052] FIGS. **2**A-**2**D are cross-sectional diagrams illustrating methods of manufacturing a semiconductor device **200** according to example embodiments. In FIGS. **2**A-**2**D, repeated descriptions of elements having the same reference numerals as in FIGS. **1**A-**1**F may not be provided. Referring to FIG. **2**A, P-channel and N-channel field-effect transistors **50**A and **50**B may be respectively formed on first and second active regions of a substrate **10**. A SiGe epitaxial layer **42**L may be formed on exposed source/drain regions **32***a* and **32***b* of the first and second active regions. A Si epitaxial layer **41**L may be formed on the SiGe epitaxial layer **42**L of the first and second active regions. The SiGe epitaxial layers **42**L may be simultaneously formed on the first and second active regions by using, for example, selective epitaxial growth. The Si epitaxial layers **41**L may be simultaneously formed on the first and second active regions by using, for example, selective epitaxial growth. A double epitaxial layer **40**E**2** including the SiGe and Si epitaxial layers **42**L and **41**L may have a reversed stack order in comparison with the double epitaxial layer **40**E**1** illustrated in FIG. **1**A.

[0053] Ion implantation may be performed, for example, on the double epitaxial layer **40**E**2** of the first and second active regions. However, example embodiments are not so limited. As will be described later with reference to FIGS. **2**B and **2**C, ion implantation may be performed, for example, on a contact pad layer **40**PA of the first active region, which may be exposed after forming first contact holes HA in the interlayer insulating film **60**. Another ion implantation may be also performed, for example, on a contact pad layer **40**PB of the second active region, which is exposed after forming the second contact holes HB in the interlayer insulating film **60**. Although not illustrated, the double epitaxial layer **40**E**2** may be extended over regions of a device isolation film **11**.

[0054] According to one or more example embodiments, prior to forming the double epitaxial layer **40**E**2**, trench regions (see a reference numeral **10**T of FIG. **3**C) may be formed in regions of the substrate **10** between a gate spacer **24** and the device isolation film **11** of the first active region. The SiGe epitaxial layer **42**L formed on the first active region may be in the trench regions (e.g., fill the trench regions). The SiGe epitaxial layer **42**L in the trench regions may apply compressive stress to a channel of the P-channel field-effect transistor **50**A. Hole mobility of the P-channel field-effect transistor **50**A may be improved and thus an on current may be enhanced, which will be fully described later with reference to FIGS. **3**A-**3**F.

[0055] Referring to FIG. **2**B, an interlayer insulating film **60** may be formed on the substrate **10** so as to cover upper regions of the P-channel and N-channel field-effect transistors **50**A and **50**B and the double epitaxial layer **40**E**2**. A mask M**1** for exposing regions in which first contact holes HA are

to be formed may be formed on the interlayer insulating film **60**. The first contact holes HA may be formed in the interlayer insulating film **60** by performing, for example, an etch using the mask M**1**. By controlling the etch depth of the first contact holes HA, lower regions of the first contact holes HA may penetrate through a Si epitaxial layer **41**L' to expose the underlying SiGe epitaxial layer **42**L. The etching of the first contact holes HA may be continuously performed on the interlayer insulating film **60** and the Si epitaxial layer **41**L by using the same etch gas, or may be discontinuously performed by using different well-known etch gases in consideration of etch selectivity therebetween.

[0056] Referring to FIG. **2**C, a mask M**2** for exposing regions in which the second contact holes HB are to be formed may be formed on the interlayer insulating film **60**. The second contact holes HB may be formed in the interlayer insulating film **60** by performing, for example, plasma dry etching. By controlling an etch depth of the second contact holes HB, lower regions of the second contact holes HB may expose the Si epitaxial layer **41**L. The contact pad layer **40**PB for the N-channel field-effect transistor **50**B may be formed. According to example embodiments illustrated in FIGS. **2**A-**2**D, sidewalls of the second contact holes HB do not expose the SiGe epitaxial layer **42**L and a diffusion barrier **65** as illustrated in FIG. **1**D may be omitted.

[0057] Referring to FIG. **2**D, barrier metal layers **70** may be formed in the first and second contact holes HA and HB. The barrier metal layers **70** may be formed by performing, for example, a blanket deposition process without a mask. The thickness of the barrier metal layers **70** may be, for example, from about 10 Å to about 400 Å. By performing a thermal anneal, the barrier metal layers **70** and the exposed SiGe and Si epitaxial layers **42**L and **41**L may react to each other, and the silicide films **80**A and **80**B may be formed at interfaces between the barrier metal layers **70** and the exposed SiGe and Si epitaxial layers **42**L and **41**L. According to one or more example embodiments, the silicide films **80**A and **80**B may locally remain only on the lower portions of the first and second contact holes HA and HB, and residue of the barrier metal layers **70** (e.g., the barrier metal layers **70** that did not participate in the silicide reaction), may be removed by performing, for example, an appropriate barrier metal etch. The silicide films **80**A and **80**B having different compositions may be formed in the first and second contact holes HA and HB. The silicide film **80**A in the first contact holes HA may be a M(Si1-yGey) film containing Ge due to the exposed SiGe epitaxial layer **42**L, and the silicide film **80**B in the second contact holes HB may be a MSi film due to the Si epitaxial layer **41**L.

[0058] Contact plugs **90** may be formed on the silicide films **80**A and **80**B in the first and second contact holes HA and HB (e.g., to fill the contact holes HA and HB) and the semiconductor device **200** may include appropriate metal interconnections. According to example embodiments, for the P-channel and N-channel field-effect transistors **50**A and **50**B, the silicide films **80**A and **80**B having low Schottky barriers may be simultaneously formed without performing a blocking process, by forming the double epitaxial layer **40**E**2** for each of the P-channel and N-channel field-effect transistors **50**A and **50**B simultaneously, and by controlling depths of the first and second contact holes HA and HB that expose the double epitaxial layer **40**E**2** formed under the interlayer insulating film **60**.

[0059] FIGS. **3**A-**3**F are cross-sectional diagrams illustrating methods of manufacturing a semiconductor device **300** according to example embodiments. In FIGS. **3**A-**3**F, repeated descriptions of elements having the same reference numerals as in FIGS. **1**A-**1**F and **2**A-**2**D may not be provided. Referring to FIG. **3**A, first and second gate stacks **20**A and **20**B may be respectively formed on first and second active regions of a substrate **10**. The first and second gate stacks **20**A and **20**B may include a gate insulating layer **21**, gate conductive films **22***a* and **22***b*, and optionally a capping film **23**. LDD regions **31***a* and **31***b* may be formed by performing ion implantation (e.g., after forming the first and second gate stacks **20**A and **20**B). A gate spacer **24** may be formed on sidewalls of the first and second gate stacks **20**A and **20**B. An appropriate mask (not shown) may be formed by performing a photolithography process and heavily doped source/drain regions **32***b* may be formed in the second active region of the substrate **10**.

[0060] Referring to FIG. **3**B, the interlayer insulating film **60** may be formed on the substrate **10** so as to cover the P-channel and N-channel field-effect transistors **50**A and **50**B. According to one or more example embodiments, in order to accurately control over-etching of the substrate **10**, which will be described later, an etch stop **60**S may be formed on the exposed first and second active regions before forming the interlayer insulating film **60**. The etch stop **60**S may be formed of a material having etch selectivity with respect to the interlayer insulating film **60**. For example, if the interlayer insulating film **60** is a silicon oxide film, the etch stop **60**S may be a silicon nitride film having etch selectivity with respect to the silicon oxide film.

[0061] Referring to FIG. **3**C, a mask M**1** for exposing regions in which the first contact holes HA are to be formed may be formed on the interlayer insulating film **60**. The first contact holes HA may be formed by performing, for example, an etch process using the mask M**1** so as to expose the first active region of the substrate **10**. Trench regions **10**T that may be adjacent to channel of the P-channel field-effect transistor **50**A may be formed by performing an etch process on the first active region exposed by the first contact holes HA. A depth h of the trench regions **10**T may be controlled so that compressive deformation of the channel is caused by a SiGe epitaxial layer (see a reference numeral **43**L of FIG. **3**D) that is deposited in the trench regions **10**T (e.g., filling the trench regions **10**T). The depth h of the trench regions **10**T may be, for example, from about 100 Å to about 1500 Å. A reference numeral **60**S' may represent the etch stop that is penetrated by the first contact holes HA.

[0062] The etch for forming the first contact holes HA and the trench regions **10**T may be, for example, a plasma etch continuously performed by using the same etch gas. Alternatively, the etching of the first contact holes HA and the trench regions **10**T may be discontinuously performed by using different well-known etching gases in consideration of etch selectivity therebetween. The first contact holes HA may be formed by, for example, using an anisotropic etch and the trench regions **10**T may be formed by using an isotropic etch as illustrated in FIG. **3**C. For example, the anisotropic etch for forming the first contact holes HA may be a reactive ion etch (REI) using plasma. The isotropic etch for forming the trench regions **10**T may be, for example, a dry etch using plasma or a wet etch using an etchant. An undercut d caused by the

isotropic etching of the trench regions **10**T may be from about 30 Å to about 1500 Å in a direction parallel to a principal plane of the substrate **10**.

[0063] Referring to FIG. **3**D, the mask M**1** may be removed and a SiGe epitaxial layer **43**L may be deposited in the trench regions **10**T of the first active region (e.g., filling the trench regions **10**T). The SiGe epitaxial layer **43**L may be formed by, for example, using a selective epitaxial growth. Concentration of Ge in the filled SiGe epitaxial layer **43**L may be from about 3% to about 50%. The thickness of the SiGe epitaxial layer **43**L may be from about 100 Å to about 1500 Å. The thickness of the SiGe epitaxial layer **43**L may be equal to the depth h of the trench regions **10**T and/or may be greater than the depth h of the trench regions **10**T as illustrated in FIG. **3**D. However, example embodiments are not limited thereto and the thickness of the SiGe epitaxial layer **43**L may be less than the depth h of the trench regions **10**T.

[0064] If an isotropic etch is used to form the trench regions **10**T, the distance between the channel of the P-channel field-effect transistor **50**A and the SiGe epitaxial layer **43**L may be reduced by the undercut d and a channel compressive stress effect caused by the SiGe epitaxial layer **43**L may be increased. When a silicon monocrystalline substrate is used as the substrate **10**, if a channel direction of the P-channel field-effect transistor **50**A is the <110> direction, hole mobility in the channel may be maximized and/or improved. According to example embodiments, improvement of hole mobility due to the SiGe epitaxial layer **43**L may be optimized and/or increased by designing the semiconductor device **300** to align the channel of the P-channel field-effect transistor **50**A in the <110> direction.

[0065] According to one or more example embodiments, in order to form source/drain regions of the P-channel field-effect transistor **50**A, an ion implantation may be performed on the SiGe epitaxial layer **43**L. Alternatively, the SiGe epitaxial layer **43**L may be doped by in-situ doping. For example, if a group III element-containing gas such as B2H5 is used in addition to a forming gas of the SiGe epitaxial layer **43**L, a P-type heavily-doped SiGe epitaxial layer **43**L may be formed.

[0066] Referring to FIG. **3**E, the mask M**2** for exposing regions in which the second contact holes HB are to be formed may be formed on the interlayer insulating film **60**. The second contact holes HB may be formed in the interlayer insulating film **60**. By controlling an etch depth of the second contact holes HB, lower portions of the second contact holes HB may expose the second active region of the substrate **10**. Referring to FIG. **3**F, barrier metal layers **70** may be formed in the first and second contact holes HA and HB by performing a blanket deposition process. The thickness of the barrier metal layers **70** may be from about 10 Å to about 400 Å.

[0067] The barrier metal layers **70** may be thermally annealed. Due to thermal annealing, the silicide film **80**A may be formed on the first active region between the barrier metal layers **70** and the SiGe epitaxial layer **43**L, and the silicide film **80**B may be formed on the second active region between the barrier metal layers **70** and the exposed source/drain regions **32***b* of the substrate **10**. The silicide films **80**A and **80**B having different compositions may be formed in the first and second contact holes HA and HB. The silicide film **80**A in the first contact holes HA may be a M(Si1-yGey) film containing Ge due to the exposed SiGe epitaxial layer **43**L, and the silicide film **80**B in the second contact holes HB may be a MSi film due to the Si of the exposed source/drain regions **32***b*.

[0068] Contact plugs (see a reference numeral **90** of FIG. **1**F) may be formed on the silicide films **80**A and **80**B of the first and second contact holes HA and HB (e.g., to fill the first and second contact holes HA and HB). The semiconductor device **300** may include well-known metal wiring formed by a well-known metal wiring process in the art. According to example embodiments, the first contact holes HA may be formed after forming the interlayer insulating film **60**, and then the SiGe epitaxial layer **43**L may be formed by using the first contact holes HA. A blocking film for passivating the second active region may not be needed in order to form the filled SiGe epitaxial layer **43**L only in the first active region.

[0069] Conventionally, a blocking film may be formed on the second active region in order to form a SiGe epitaxial layer on the first active region. In order to form the blocking film, for example, a silicon nitride film may be formed on an entire surface of a substrate, and a photolithography and an etching are performed so that the silicon nitride film covers the second active region and exposes only the first active region. A SiGe epitaxial layer may be formed on the exposed first active region and an etch process for removing the blocking film that covers the second active region has to be performed in order to complete a transistor of the second active region. However, according to example embodiments, an interlayer insulating film may function as a blocking film, a transistor forming process such as a forming process of a SiGe epitaxial layer may be performed by using first and second contact holes, and a photolithography step and an etch step may be eliminated.

[0070] FIG. **4** is a cross-sectional diagram illustrating methods of manufacturing a semiconductor device **400** according to example embodiments. Referring to FIG. **4**, an interlayer insulating film **60** may be formed on a substrate **10** so as to cover P-channel and N-channel field-effect transistors **50**A and **50**B. First contact holes HA may be formed by using an appropriate mask so as to expose a first active region of the substrate **10**. A SiGe epitaxial layer **44**L may be formed on the first active region exposed by lower portions of the first contact holes HA. The SiGe epitaxial layer **44**L may be formed by using, for example, selective epitaxial growth.

[0071] Second contact holes HB may be formed in the interlayer insulating film **60** as described above with reference to FIG. **3**E, a barrier metal layers **70** may be formed in the first and second contact holes HA and HB and thermal annealing may be performed, as described above with reference to FIG. **3**F. Silicide films **80**A and **80**B having different compositions may be formed in the first and second contact holes HA and HB. The silicide film **80**A in the first contact holes HA may be a M(Si1-yGey) film containing Ge due to the SiGe epitaxial layer **44**L and the silicide film **80**B in the second contact holes HB may be a MSi film due to the exposed second active region. According to example embodiments, the first contact holes HA formed in the interlayer insulating film **60** may be used to form the M(Si1-yGey) film and thus the M(Si1-yGey) film capable of improving contact resistance of the P-channel field-effect transistor **50**A may be obtained without additionally performing a photolithography or etching process.

[0072] FIG. **5** is a cross-sectional diagram illustrating methods of manufacturing a semiconductor device **500** according to example embodiments. Referring to FIG. **5**, an

interlayer insulating film **60** may be formed on a substrate **10** so as to cover P-channel and N-channel field-effect transistors **50**A and **50**B. First contact holes HA may be formed by using an appropriate mask so as to expose a first active region of the substrate **10**. A Ge ion implantation may be performed to provide Ge atoms to the first active region exposed by lower portions of the first contact holes HA. According to acceleration energy of Ge ions, the Ge ions may form a Ge atomic layer **45**L piled on the first active region as illustrated in FIG. **5** and/or may penetrate into source/drain regions **32***a* so as to form a SiGe layer in upper surfaces of the source/drain regions **32***a*. According to one or more example embodiments, thermal annealing may be performed after performing the Ge ion implantation.

[0073] Example embodiments are not limited to Ge ion implantation. For example, in order to provide the Ge atoms to the first active region exposed by the lower surfaces of the first contact holes HA, the Ge atomic layer **45**L may be formed by, for example, using a pulsed laser ablation deposition (PLAD) and/or a gas cluster ion beam (GCIB) deposition. According to example embodiments, the Ge atomic layer **45**L may be monocrystalline, amorphous, microcrystalline, and/or polycrystalline. Second contact holes HB may be formed in the interlayer insulating film **60** as described above with reference to FIG. **3**E, barrier metal layers **70** may be formed in the first and second contact holes HA and HB and thermal annealing may be performed, as described above with reference to FIG. **3**F. Silicide films **80**A and **80**B having different compositions may be formed in the first and second contact holes HA and HB. The silicide film **80**A in the first contact holes HA may be a M(Si1-yGey) film including the Ge atomic layer **45**L and the silicide film **80**B in the second contact holes HB may be a MSi film due to the exposed second active region.

[0074] According to example embodiments, the first contact holes HA formed in the interlayer insulating film **60** may be used to form the M(Si1-yGey) film capable of improving contact resistance of the P-channel field-effect transistor **50**A and the M(Si1-yGey) film may be obtained. A photolithography and/or etch process may be eliminated with respect to conventional methods. Example embodiments described with reference to the attached drawings may be implemented independently or in combination with the other embodiments. For example, the SiGe epitaxial layer **42**L illustrated in FIGS. **1**A-**1**F may comprise the Ge atomic layer **45**L illustrated in FIG. **5**. While example embodiments have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and scope of the claims.

What is claimed is:

1. A semiconductor device comprising:

a substrate having first and second active regions;

a P-channel field-effect transistor associated with the first active region and including at least one of the source and drain regions;

a N-channel field-effect transistor associated with the second active region and including at least one of the source and drain regions;

a first contact pad layer comprising silicon (Si) and SiGe epitaxial layers on the at least one of the source and drain regions of the P-channel field-effect transistor, the SiGe epitaxial layer being sequentially stacked on the Si epitaxial layer;

a second contact pad layer comprising silicon (Si) and SiGe epitaxial layers on the at least one of the source and drain regions of the N-channel field-effect transistor, the SiGe epitaxial layer being sequentially stacked on the Si epitaxial layer;

an interlayer insulating film formed on the P-channel and the N-channel field-effect transistors and including first and second contact holes, wherein the first contact hole includes a first lower region that exposes the SiGe epitaxial layer of the first contact pad layer and the second contact hole includes a second lower region that penetrates through the SiGe epitaxial layer of the second contact pad layer to expose the Si epitaxial layer of the second contact pad layer;

first and second metal silicide films formed respectively in the first and second lower regions of the contact holes; and

contact plugs formed on the first and second metal silicide films and filled in the first and second contact holes.

2. The semiconductor device of claim **1**, wherein the first metal silicide film includes germanium (Ge) and the second metal silicide film does not include Ge.

3. The semiconductor device of claim **1**, further comprising a diffusion barrier between sidewalls of the second contact holes and the second metal silicide film.

4. The semiconductor device of claim **1**, further comprising:

a device isolation film defining the first and second active regions,

wherein at least one of the first and second contact pad layers extends in a direction parallel to a principal plane of the substrate and extends over a region of the device isolation film.

5. The semiconductor device of claim **1**, wherein a thickness of the Si epitaxial layer is from about 10□ to about 500□, and a thickness of the SiGe epitaxial layer is from about 30□ to about 500□.

6. The semiconductor device of claim **1**, wherein a concentration of Ge in the SiGe epitaxial layer is from about 3 mole % to about 50 mole %.

7. A semiconductor device comprising:

a substrate having first and second active regions;

a P-channel field-effect transistor associated with the first active region and including at least one of the source and drain regions;

a N-channel field-effect transistor associated with the second active region and including at least one of the source and drain regions;

a first contact pad layer comprising silicon (Si) and SiGe epitaxial layers on the at least one of the source and drain regions of the P-channel field-effect transistor, the Si epitaxial layer being sequentially stacked on the SiGe epitaxial layer;

a second contact pad layer comprising silicon (Si) and SiGe epitaxial layers on the at least one of the source and drain regions of the N-channel field-effect transistor, the Si epitaxial layer being sequentially stacked on the SiGe epitaxial layer;

an interlayer insulating film formed on the P-channel and the N-channel field-effect transistors and including first and second contact holes, wherein the first contact hole includes a first lower region that penetrates through the Si epitaxial layer of the first contact pad layer to expose the SiGe epitaxial layer of the first contact pad layer and

the second contact hole includes a second lower region that exposes the Si epitaxial layer of the second contact pad layer;

first and second metal silicide films formed respectively in the first and second lower regions of the contact holes; and

contact plugs formed on the first and second metal silicide films and filled in the first and second contact holes.

8. The semiconductor device of claim **7**, wherein the first metal silicide film includes germanium (Ge) and the second metal silicide film does not include Ge

9. The semiconductor device of claim **7**, wherein at least a portion of the SiGe epitaxial layer of the first contact pad layer is buried in the first active region.

10. The semiconductor device of claim **7**, further comprising:

a device isolation film defining the first and second active regions,

wherein at least one of the first and second contact pad layers extends in a direction parallel to a principal plane of the substrate so as to extend over a region of the device isolation film.

11. The semiconductor device of claim **7**, wherein a thickness of the Si epitaxial layer is from about 10□ to about 500□, and a thickness of the SiGe epitaxial layer is from about 30□ to about 500□.

12. The semiconductor device of claim **7**, wherein a concentration of Ge in the SiGe epitaxial layer is from about 3 mole % to about 50 mole %.

13. A semiconductor device comprising:

a substrate having first and second active regions;

a P-channel field-effect transistor associated with the first active region and including at least one of the source and drain regions;

a N-channel field-effect transistor associated with the second active region and including at least one of the source and drain regions;

a first contact pad layer comprising a silicon (Si) epitaxial layer and a germanium (Ge) atomic layer on the at least one of the source and drain regions of the P-channel field-effect transistor, the Ge atomic layer being sequentially stacked on the Si epitaxial layer;

a second contact pad layer comprising a silicon (Si) epitaxial layer and a germanium (Ge) atomic layer on the at least one of the source and drain regions of the N-channel field-effect transistor, the Ge atomic layer being sequentially stacked on the Si epitaxial layer;

an interlayer insulating film formed on the P-channel and the N-channel field-effect transistors and including first and second contact holes, wherein the first contact hole includes a first lower region that exposes the Ge atomic layer of the first contact pad layer and the second contact hole includes a second lower region that penetrates through the Ge atomic layer of the second contact pad layer to expose the Si epitaxial layer of the second contact pad layer;

first and second metal silicide films formed respectively in the first and second lower regions of the contact holes; and

contact plugs formed on the first and second metal silicide films and filled in the first and second contact holes.

14. The semiconductor device of claim **13**, wherein the first metal silicide film includes germanium (Ge) and the second metal silicide film does not include Ge

15. A method of manufacturing a semiconductor device, the method comprising:

forming a first active region for a P-channel field-effect transistor in a substrate;

forming a second active region for an N-channel field-effect transistor in the substrate;

forming a first gate stack on the first active region;

forming a second gate stack on the second active region;

forming a first layer on the first active region in a region where the first gate stack is not formed,

forming a second layer on the second active region in a region where the second gate stack is not formed, the first and second layers including a silicon germanium (SiGe) epitaxial layer sequentially stacked on a silicon (Si) epitaxial layer;

forming an interlayer insulating film to cover upper regions of the first and second gate stacks and the first and second layers;

forming a first contact hole in the interlayer insulating film, the first contact hole including a first lower region exposing the SiGe epitaxial layer of the first layer;

forming a second contact hole in the interlayer insulating film, the second contact hole including a second lower region penetrating through the SiGe epitaxial layer of the second layer and exposing the Si epitaxial layer of the second layer;

forming a first metal silicide film including germanium (Ge) in the first lower region;

forming a second metal silicide film not including Ge in the second lower region simultaneously with the forming of the first metal silicide film; and

forming contact plugs on the first and second metal silicide films in the first and second contact holes.

16. The method of claim **15**, wherein the forming of the first and second layers is performed by selective epitaxial growth.

17. The method of claim **15**, further comprising:

forming a diffusion barrier on sidewalls of the second contact hole so as to cover a region of the exposed SiGe epitaxial layer.

18. A method of manufacturing a semiconductor device, the method comprising:

forming a first active region for a P-channel field-effect transistor in a substrate;

forming a second active region for an N-channel field-effect transistor in the substrate;

forming a first gate stack on the first active region;

forming a second gate stack on the second active region;

forming a first layer on the first active region in a region where the first gate stacks are not formed;

forming a second layer simultaneously with the forming of the first layer on the second active region in a region where the second gate stacks are not formed, the first and second layers including a silicon (Si) epitaxial layer sequentially stacked on a silicon germanium (SiGe) layer;

forming an interlayer insulating film to cover upper regions of the first and second gate stacks and the first and second layers;

forming a first contact hole in the interlayer insulating film, the first contact hole including a first lower region penetrating through the Si epitaxial layer of the first layer and exposing the SiGe epitaxial layer;

forming a second contact hole in the interlayer insulating film, the second contact hole including a second lower region exposing the Si epitaxial layer of the second layer;

forming a first metal silicide film including Ge in the first lower region;

forming a second metal silicide film not including Ge in the second lower region simultaneously with first metal silicide film; and

forming contact plugs on the first and second metal silicide films in the first and second contact holes.

19. The method of claim **18**, wherein the forming of the first and second layers is performed by selective epitaxial growth.

20. A semiconductor device comprising:

source regions;

drain regions;

a first contact pad layer;

a second contact pad layer, the first and second contact pad layers including a silicon (Si) epitaxial layer and a silicon germanium (SiGe) epitaxial layer, the Si and SiGe epitaxial layers on the source and drain regions

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