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Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Devices

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Abstract

We present an advanced CMOS integration scheme based on embedded SiGe (eSiGe) with a novel graded germanium process. The retention of channel strain enabled a pFET performance gain of 15% over a non-graded eSiGe control. When combined with a compressive stress liner (CSL), the pFET drive current reached 770μA/μm at I_{off}=100nA/μm with V_{DD}=1V. Competitive nFET performance was maintained. Parasitics such as silicide and junction characteristics were not degraded.

Introduction

Channel strain engineering such as eSiGe [1-4] and CSL [5,6] for pFET drive current enhancement has been pursued aggressively in scaled CMOS technologies. Raising the Ge concentration (%Ge) is known to result in higher stress in eSiGe. However, due to competing mechanisms for strain relaxation and defect propagation in a highly strained SiGe layer on a lattice mismatched Si substrate [7], it is difficult to maintain the stress for a high %Ge eSiGe source/drain (S/D). In previous experiments, the film experienced significant relaxation as %Ge was increased. As an alternative method to minimize the misfit dislocation nucleation and propagation and hence retain maximum strain from eSiGe, a novel process of grading the %Ge in the eSiGe (graded eSiGe) has been developed and optimized. The degree of stress relaxation of graded eSiGe has been proven to be smaller than that of high uniform %Ge eSiGe.

In this paper, we have experimentally demonstrated that: (1) high stress cannot be easily retained in SiGe films with uniformly high Ge concentration; (2) higher channel stress can be achieved with a graded eSiGe process; (3) very high pFET performance can be realized by integrating graded eSiGe with CSL without silicide and junction characteristics degradation.

Blanket film stress study

We conducted blanket experiments on SiGe films with low, medium, and high uniform %Ge and compared the results to SiGe with graded Ge. Schematic Ge profiles of graded SiGe vs uniform SiGe with low, medium and high %Ge are shown in Fig. 1. A rocking curve XRD residual strain study revealed that beyond a threshold point, SiGe films do relax readily as %Ge increases, while a higher residual strain can be achieved by grading the Ge concentration in the SiGe film (Fig. 2). The results of the TEM and AFM analysis show that much less misfits occured near the bottom SiGe/Si interface and fewer cross-hatches at the SiGe surface for the graded SiGe film than in a high %Ge SiGe film. This indicates that stress relaxation caused by misfits dislocation and defect propagation is much smaller for graded SiGe. This finding is consistent with XRD data. Similar results were observed on structural samples. The sources of defect and misfit generation and propagation are likely related to interfacial contamination due to insufficient surface pre-cleaning, high temperatures during epitaxial growth, and subsequent implantation and annealing steps.

Process flow

The basic front-end process flow used in the present work has been reported previously [4] and is summarized in Fig.3. An 11Å SiON gate dielectric and gate lengths from 240nm down to 43nm were employed. For both, control and graded eSiGe processes, isotropic-RIE and selective epitaxial growth (SEG) were used to recess and re-grow the Si S/D regions of pFETs with in-situ-doped SiGe. Before proceeding to the back-end processing (wiring levels), the wafers completed silicidation and stress liner formation.

Results and Discussion

The cross-sectional SEM of a graded eSiGe transistor is shown in Fig. 4 (a), eSiGe S/D and CSL are shown for a pFET. The Ge profile for the graded eSiGe (Fig. 4 (b)) was

determined by Auger Electron Spectroscopy (AES), while the Ge profile of the eSiGe control cell has been reported elsewhere [4]. The eSiGe with peak Ge concentration is set to grow close to the channel because it is expected that the eSiGe stress enhancement is mainly determined by the peak Ge concentration near the channel. Although the Ge profile of graded eSiGe differed considerably from the eSiGe control, a similar B dopant concentration profile was achieved (Figs. 5), which contribute to similar silicide sheet resistance and junction characteristics between graded eSiGe and SiGe control samples.

Numerical stress simulations using the Tsuprem-4 software tool [8] were conducted to compare strain levels between the graded and control eSiGe samples. The results predicted greater pFET channel stress enhancement in the graded eSiGe than in the control samples (Fig. 6). In the graded eSiGe films, the peak value of the %Ge was found to be the key parameter for further enhancements of pFET performance. The stress data obtained from the SiGe films confirmed that the film stress depended strongly on the peak %Ge and much less on the %Ge at the surface (Fig. 7). The graded eSiGe process has been optimized to achieve substantially reduced defectivity at a higher peak %Ge with much less cross-hatches and a much smoother surface, as evidenced by the AFM morphology in Fig. 8.

CMOS integration with implementing graded eSiGe S/D and dual stress liner (DSL) was demonstrated. nFETs were found to be unaffected by the graded eSiGe process, performance remained competitive, a drive-on current of approximately 1100 μA/μm at drive-off current 100 nA/μm was achieved (Fig. 9). The I_{on}-I_{off} characteristics of pFETs with graded eSiGe showed performance gains of 15% over control eSiGe transistors. A drive-on current I_{on} of 770 μA/μm was obtained at I_{off} = 100 nA/μm with V_{DD} = 1V, as shown in Fig. 10. A reference value obtained from the literature [2], labeled as star in Fig. 10, falls between graded eSiGe and eSiGe control.

The output and subthreshold characteristics of graded eSiGe pFETs are plotted in Figures 11 and 12 respectively. The Ids-Vds characteristics of these graded devices (Fig. 11) were consistent with the dependence of Ion on Ioff. Typical subthreshold curves obtained from these devices are shown in the Ids-Vg plot of pFETs with graded eSiGe @ Vds = -0.05V and -1V (Fig. 12).

In order to identify the major contribution to the observed drive-on-current enhancement, the normalized I_{odlin} at I_{off} = 100 nA/μm was examined (s. Fig. 13). The graph indicates that carrier mobility enhancement was the major component of drive-on current improvement.

The normalized external resistance of an eSiGe control was compared to that of a graded eSiGe sample (s. Fig. 14). A comparable external resistance was found and again confirmed that the drive-on current improvement was mainly due to an increase in carrier mobility, consistent with the conclusion drawn from Fig. 13.

The silicide sheet resistances measured in an eSiGe control and a graded eSiGe test sample were found to be similar (s. Fig. 15). This similarity is hypothesized to be causally related to comparable Boron profiles (Fig. 5) and a similar Ge surface concentration found in both samples and controls.

The junction characteristics is another device feature which needs to be evaluated for additional parasitic properties. The evaluation of the junction characteristics (Fig. 16) for the present test and control samples does not indicate a significant difference in junction leakage and capacitance (Fig. 16 inset) between the graded eSiGe and eSiGe control devices. This similarity may also be attributed to similar Boron junction profiles.

Conclusion

A novel enhanced stressor based on graded eSiGe has been studied analytically, evaluated electrically, and has been implemented successful into CMOS integration for the first time. Without degrading the nFETs device performance and parasitic characteristics, a significant pFET performance gain has been demonstrated.

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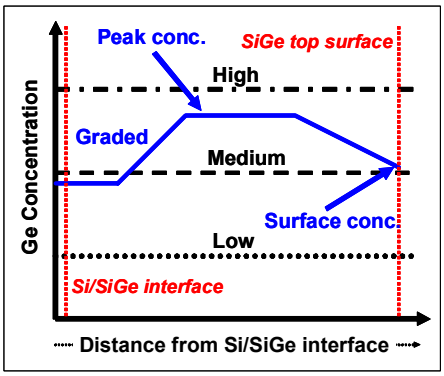

Fig. 1: Schematic Ge profile of graded SiGe vs uniform SiGe with low, medium and high Ge concentration (%Ge).

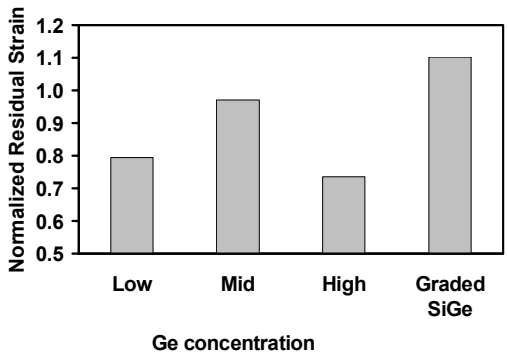

Fig. 2: Normalized XRD residual strain of SiGe with various %Ge showing that stress was relaxed in high %Ge and graded SiGe has the highest residual strain.

- Formation of well and isolation
- Gate stack formation and PC patterning
- Spacer formation and ext/halo/SD I/I
- S/D recess
- Controlled eSiGe or graded eSiGe epi- growth
- S/D Anneal
- Silicidation
- CSL

Fig. 3: Process flow of pFET integration with eSiGe and CSL.

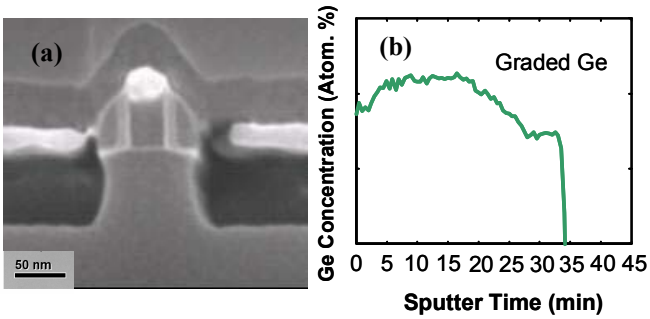

Fig. 4: (a) Cross-sectional SEM of pFET device structure and (b) AES depth profile of Ge component in the graded eSiGe.

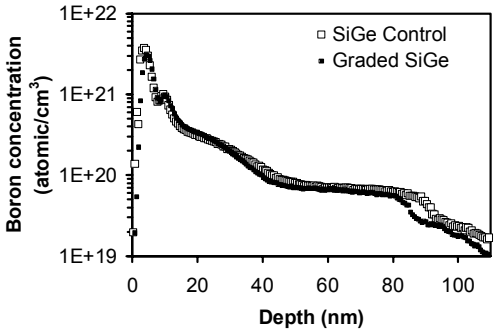

Fig. 5: Comparable Boron depth profiles of SIMS data for eSiGe control and graded eSiGe.

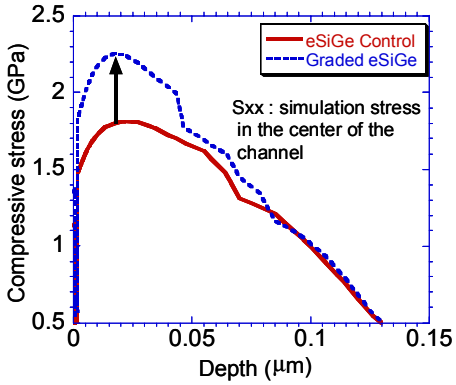

Fig. 6: Higher channel stress, S_{xx}, in the graded eSiGe transistor than in the eSiGe control device.

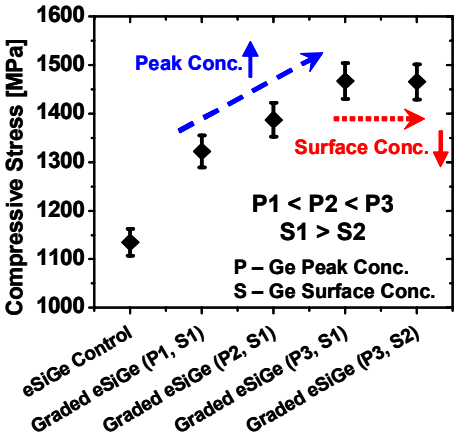

Fig. 7: Stress study of graded eSiGe with different peak and surface %Ge showing that stress depended strongly on peak %Ge and much less on %Ge at surface.

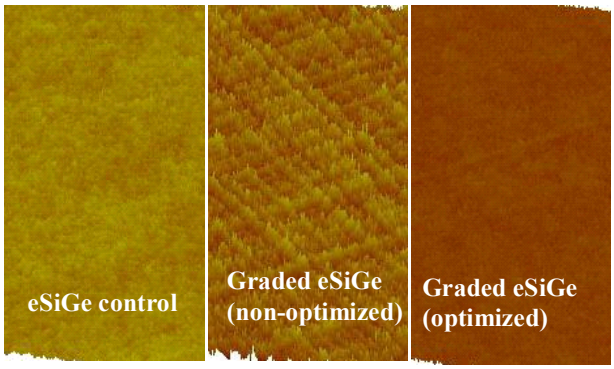

Fig. 8: AFM morphology of graded eSiGe samples with higher peak %Ge before and after optimization compared to an eSiGe control sample.

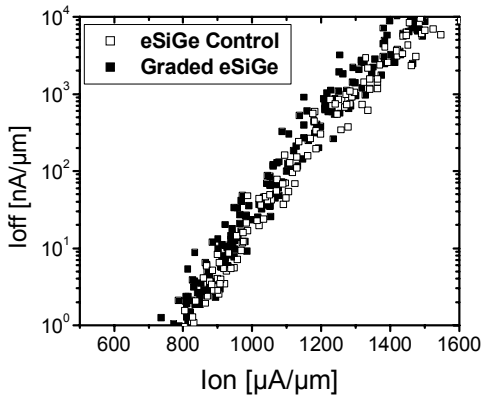

Fig. 9: I_{on} vs. I_{off} @V_{DD}=1V of nFETs indicating that nFETs performance was not affected by the graded eSiGe process.

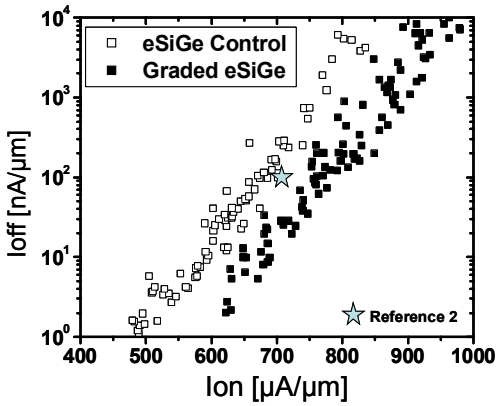

Fig. 10: pFET I_{on}-I_{off} characteristics showing 18% performance gain of the graded eSiGe devices over eSiGe control.

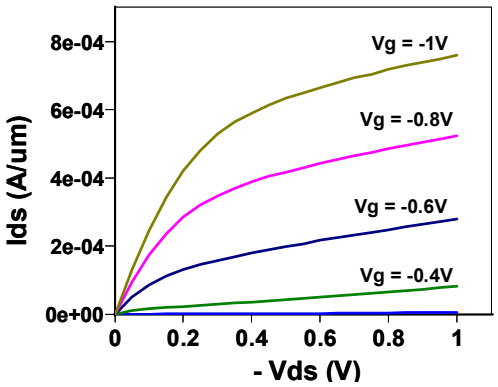

Fig. 11: I_{ds}-V_{ds} characteristics of pFETs with graded eSiGe.

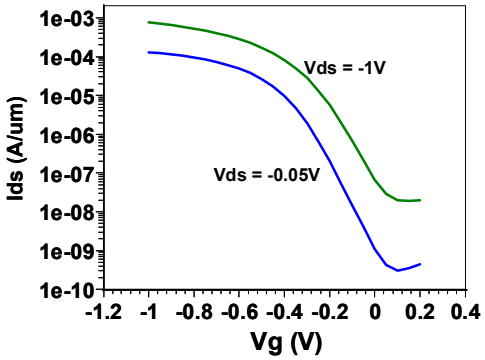

Fig. 12: Subthreshold I_{ds}-V_g characteristics of pFETs with graded eSiGe @ V_{ds} = -0.05V and -1V.

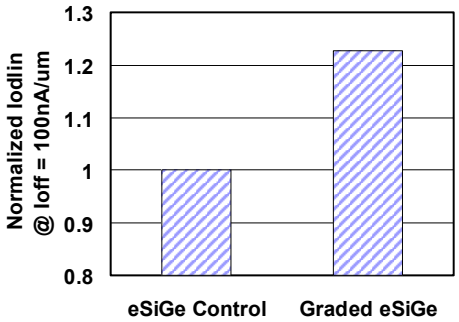

Fig. 13: Normalized I_{odlin} data indicating mobility enhancement is a major component of I_{on} improvement.

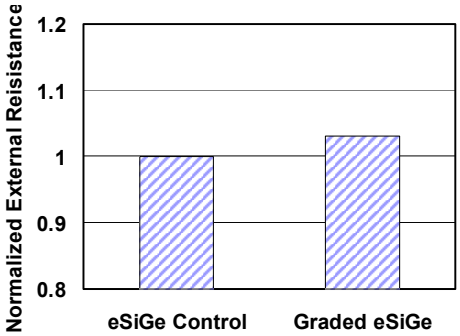

Fig. 14: Comparison of normalized external resistance between eSiGe control and graded eSiGe.

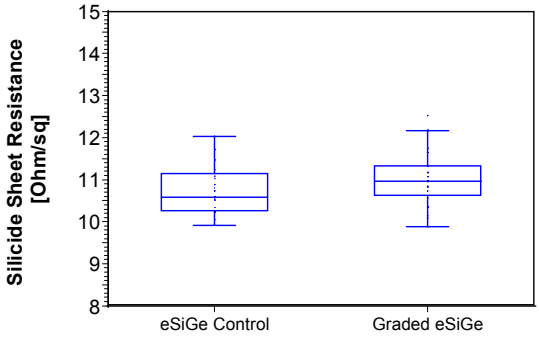

Fig. 15: Similar silicide sheet resistance data obtained from eSiGe control and graded eSiGe.

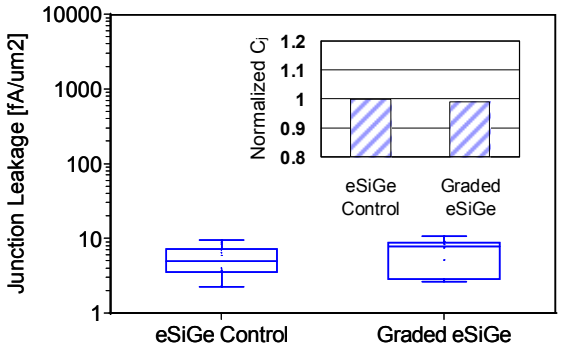

Fig. 16: Comparable junction capacitance and junction leakage between graded eSiGe and eSiGe control devices.