PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1-C1 111548
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Glenn	A.	GLASS	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	5009 NW 124th Avenue		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Anand	S.	MURTHY	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	10934 NW Lucerne Ct.		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Tahir		GHANI	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1-C1 111548
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	14191 NW Stonebridge Drive		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	31817		
Email Address	intelpatent@schwabe.com	Add Email	Remove Email

Application Information:

Title of the Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION		
Attorney Docket Number	P38507USC2-C1-C1 111548	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	11	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1-C1 111548
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	31817		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16416445	2019-05-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16416445	Continuation of	15339308	2016-10-31	10297670	2019-05-21

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15339308	Continuation of	14673143	2015-03-30	9484432	2016-11-01

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14673143	Continuation of	13990224	2013-05-29	8994104	2015-03-31

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13990224	a 371 of international	PCT/US2011/054198	2011-09-30

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1-C1 111548
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
PCT/US2011/0541	Continuation in part of	12975278	2010-12-21	8901537	2014-12-02
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.					Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1-C1 111548
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1-C1 111548
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	INTEL CORPORATION		
Mailing Address Information For Applicant:			
Address 1	2200 MISSION COLLEGE BLVD.		
Address 2			
City	SANTA CLARA	**State/Province**	CA
Country	US	Postal Code	95054
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1-C1 111548
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	INTEL CORPORATION

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	2200 MISSION COLLEGE BLVD.		
Address 2			
City	SANTA CLARA	**State/Province**	CA
Country i	US	Postal Code	95054
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Justin K. Brask/			Date (YYYY-MM-DD)	2020-05-22
First Name	Justin K.	Last Name	Brask	Registration Number	61080

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1-C1 111548
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Inventors:
Glenn A. Glass
Anand S. Murthy
Tahir Ghani

RELATED APPLICATIONS

[0001] This patent application is a continuation of U.S. Patent Application No. 16/164,445, filed May 20, 2019, which is a continuation of U.S. Patent Application No. 15/339,308, filed October 31, 2016, now U.S. Patent No. 10,297,670 issued may 21, 2019, which is a continuation of U.S. Patent Application No. 14/673,143, filed March 30, 2015, now U.S. Patent No. 9,484,432 issued November 1, 2016, which is a continuation of U.S. Patent Application No. 13/990,224, filed May 29, 2013, now U.S. Patent No. 8,994,104 issued March 31, 2015, which is a U.S. National Phase application under 35 U.S.C. § 371 of International Application No. PCT/US2011/054198, filed September 30, 2011, which is a continuation-in-part of U.S. Patent Application No. 12/975,278 filed December 21, 2010, now U.S. Patent No. 8,901,537, each of which are incorporated herein by reference in their entireties.

BACKGROUND

[0002] Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to minimize the parasitic resistance associated with contacts otherwise known as external resistance R_{ext}. Decreased R_{ext} enables higher current from an equal transistor design.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1A illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention.

[0004] Figure 1B illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0005] Figure 1C illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0006] Figure 2 is a method for forming a transistor structure with low contact resistance in accordance with an embodiment of the present invention.

[0007] Figures 3A to 3I illustrate structures that are formed when carrying out the method of Figure 2, in accordance with various embodiment of the present invention.

[0008] Figure 4 is a method for forming a transistor structure with low contact resistance in accordance with another embodiment of the present invention.

[0009] Figures 5A to 5F illustrate structures that are formed when carrying out the method of Figure 4, in accordance with various embodiment of the present invention.

[0010] Figure 6 shows a perspective view of a FinFET transistor architecture, configured in accordance with one embodiment of the present invention.

[0011] Figure 7 shows a plot of a split lot showing contact resistance for transistor structures configured with in accordance with embodiments of the present invention and standard transistor structures configured with no cap.

[0012] Figure 8 illustrates a computing system implemented with one or more transistor structures in accordance with an example embodiment of the present invention.

[0013] As will be appreciated, the figures are not necessarily drawn to scale or intended to limit the claimed invention to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of a transistor structure may have less than perfect straight lines, right angles,

and some features may have surface topology or otherwise be non-smooth, given real world limitations of the processing equipment and techniques used. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

[0014] Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures. The techniques are particularly well-suited for implementing p-type devices, but can be used for n-type devices if so desired.

General Overview

[0015] As previously explained, increased drive current in the transistors can be achieved by reducing device resistance. Contact resistance is one component of a device's overall resistance. A standard transistor contact stack typically includes, for example, a silicon or SiGe source/drain layer, a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad. In such configurations, the contact resistance is effectively limited by the silicon or SiGe valence band alignment to the pinning level in the metal. Typically, using industry standard silicides such as nickel (or other suitable silicides, such as titanium, cobalt, or platinum), this results in a band misalignment of about 0.5 eV. Thus, and in accordance with an example embodiment of the present invention, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce the band misalignment value and contact resistance.

[0016] In one specific example embodiment, contacts configured with the intermediate boron doped germanium layer exhibit a reduction in the band misalignment value to less than 0.2 eV and a corresponding reduction in contact resistance of about 3X (relative to a conventional contact stack similarly configured, but without the intermediate boron doped germanium layer

between the source/drain regions and contact metal). A transmission electron microscopy (TEM) cross section or secondary ion mass spectrometry (SIMS) profile can be used to show the germanium concentration throughout the vertical stack of the film structure, as profiles of epitaxial alloys of silicon and SiGe can readily be distinguished from germanium concentration profiles.

[0017] Thus, transistor structures configured in accordance with embodiments of the present invention provide an improvement over conventional structures with respect to lower contact resistance. Some such embodiments effectively marry superior contact properties of germanium with superior semiconductor transistor properties of Si and SiGe to provide next generation low resistance contacts.

[0018] Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., such as double-gate and trigate transistor structures), as well as strained and unstrained channel structures. Any number of such structural features and material systems can be used in conjunction with a germanium overlayer as described herein. The transistor structure may include p-type source/drain regions, n-type source/drain regions, or both n-type and p-type source/drain regions. In some example embodiments, the transistor structure includes dopant-implanted source/drain regions or epitaxial (or poly) replacement source/drain regions of silicon, SiGe alloys, or nominally pure germanium films (e.g., such as those with less than 10% silicon) in a MOS structure. In any such implementations, an overlayer or cap of boron doped germanium can be formed directly over the source/drain regions, in accordance with an embodiment of the present invention. A contact metal (or series of metals) can then be deposited and a subsequent reaction (annealing) can be carried out to form metal germanide source and drain contacts. As will be appreciated, the contact may be implemented as a stack including one or more of a silicide layer, an adhesion layer, and/or a metal pad layer. The boron doped germanium overlayer can be formed directly over other parts of the transistor structure as well, such as the poly gate and/or grounding tap regions, if so desired.

[0019] As is known, a MOS transistor may include source and drain tip regions that are designed to decrease the overall resistance of the transistor while improving short channel effects (SCE). Conventionally, these tip regions are portions of the substrate where a dopant such as boron or carbon is implanted using an implant and diffusion technique. The source tip region is

formed in the area between the source region and the channel region. Likewise, the drain tip region is formed in the area between the drain region and the channel region. Some embodiments of the present invention are configured with such conventionally formed tip regions. In other example embodiments, fabrication techniques are employed to extend self-aligned epitaxial tip (SET) transistors to achieve very near to the theoretical limit of uniaxial strain. This can be accomplished, for instance, by selective epitaxial deposition in the source and drain regions as well as their corresponding tip regions to form a bilayer construction of boron doped silicon or SiGe (for the source/drain regions) capped with an overlayer of a boron doped germanium layer in the source/drain and respective tip regions. The germanium and boron concentrations can vary, but in some example embodiments, the germanium concentration is in the range of 20 atomic % to 100 atomic %, and the boron concentration is in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., germanium concentration in excess of 50 atomic % and boron concentration in excess of 2E20 cm^{-3}). Note that the boron doped germanium layer may be provided in the tip regions, but in other embodiments is just provided over the source/drain regions (and not in the tip regions).

[0020] In still other example embodiments, an optional thin buffer with graded germanium concentration and/or boron concentration can be used as an interfacial layer between the underlying substrate with the source/drain layer (e.g., silicon or SiGe). Likewise, a thin buffer with graded germanium concentration and/or boron concentration can be used as an interfacial layer between the source/drain layer and the boron doped germanium cap. In still other embodiments, the boron doped germanium overlayer or source/drain layer themselves can have a graded germanium and/or boron concentration in a similar fashion as to the optional buffers. In any such case, since boron diffusion is suppressed in germanium (the higher the concentration, the greater the relative suppression), a high concentration of boron can be doped in the germanium, which in turn results in lower parasitic resistance and without degrading tip abruptness. In addition, the contact resistance is reduced from lowering of Schottky-barrier height.

Architecture and Methodology

[0021] Figure 1A illustrates a MOS device 100A formed on a substrate 102 and configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention. In particular, boron doped germanium

layer 117 is provided between the source layer 110 and contact metals 125, and boron doped germanium layer 119 is provided between the drain layer 112 and contact metals 127. The source region 110 and the drain region 112 can be formed using any number of conventional techniques. In this example embodiment, for instance, the source region 110 and the drain region 112 are formed by etching the substrate and then epitaxially depositing a silicon or silicon germanium material (e.g., with a germanium concentration in the range of, for instance, 10 to 70 atomic %).

[0022] A gate stack 122 is formed over a channel region 120 of the transistor 100A. As can further be seen, the gate stack 122 includes a gate dielectric layer 106 and a gate electrode 104, and spacers 108 are formed adjacent to the gate stack 122. In some example cases, and depending on the technology node, the spacers 108 create a distance of about 10 to 20 nanometers (nm) between the edges of the gate dielectric layer 106 and the edges of each of the source and drain regions 110/112. It is within this space that a source tip region 110A and a drain tip region 112A can be formed. In this example embodiment, the tip regions 110A/112A are formed via a typical implantation-diffusion based process, and overlap the spacers 108 and may also overlap or underdiffuse the gate dielectric layer 106 by a distance of, for instance, less than 10 nm. In forming the implantation-diffusion based tip regions 110A/112A, a dopant such as boron or carbon is implanted into the source region 110 and the drain region 112. The transistor 100A is then annealed to cause the dopant to diffuse towards the channel region 120. Angled ion implantation techniques may also be used to further implant dopants into those areas between the gate dielectric layer 106 and the source/drain regions 110/112. Such implantation-diffusion-based tip formation processes generally do not induce a strain on the channel region.

[0023] In any case, and as will be appreciated in light of this disclosure, whether a transistor structure has a strained or unstrained channel, or source-drain tip regions or no source-drain tip regions, is not particularly relevant to various embodiments of the present invention, and such embodiments are not intended to be limited to any particular such structural features. Rather, any number of transistor structures and types can benefit from employing a boron doped germanium overlayer as described herein. The techniques provided herein are compatible, for instance, with conventional dopant implanted silicon, raised source/drain, strained SiGe (or other suitable materials), and any deposited epitaxial tip (sometimes referred to as source-drain

extensions) that extend below the gate electrode dielectric or are spaced away from the vertical line defined by the gate electrode dielectric.

[0024] The germanium overlayer 117/119 is generally provided after formation of the source/drain regions 110/112 and prior to formation of the contacts 125/127. The thickness of this overlayer 117/119 can vary from one embodiment to the next, but in one example embodiment is in the range of 50 to 250 Angstroms (Å). The boron concentration of overlayer 117/119 can also vary, but in one example embodiment is in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., in excess of 2E20 cm^{-3}). The overlayer 117/119 can be selectively deposited over the source/drain 110/112 regions (and/or other regions as desired, such as the poly gate or grounding tap regions). Any number of suitable deposition techniques can be used to provide the overlayer 117/119 (e.g., chemical vapor deposition, molecular beam epitaxy, etc). In accordance with one example embodiment, the contact metals 125 and 127 each comprise a stack a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad, and although any number of contact metal configurations can be used as will be appreciated in light of this disclosure. Standard deposition techniques can be used in providing the contact metals 125/127.

[0025] Figure 1B illustrates an example MOS device 100B formed on a substrate 102 and configured with a boron doped germanium layer 117/119 between the source/drain layer 110/112 and contact metals 125/127, in accordance with another embodiment of the present invention. This example configuration includes source and drain epitaxial tips (generally referred to herein as epi-tips). In more detail, the MOS transistor 100B uses an undercut etch to allow the source region 110 and the drain region 112 to extend below the spacers 108, and in some cases, below the gate dielectric layer 106. The portions of the source/drain regions 110/112 that extend below the spacers 108 (and possibly the gate dielectric layer 106) are generally referred to as the source epi-tip 110B and the drain epi-tip 112B, respectively. The source and drain epi-tips 110B/112B replace the implantation/diffusion based tip regions 110A/112A described with regard to Figure 1A. In accordance with one embodiment, the source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be formed, for example, by etching the substrate 102, which includes undercutting the spacers 108 (and possibly the gate dielectric layer 106), and then using selective epitaxial deposition to provide, for instance, an in situ doped silicon, germanium, or SiGe to fill the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, as shown in Figure 1B. Note the epitaxial fill may be raised relative to the surface of substrate 102, as further shown

in Figure 1B, although non-raised configurations can be used as well. The germanium overlayer 117/119 and the contact metals 125/127 can be implemented, for instance, as previously described with respect to Figure 1A.

[0026] Figure 1C illustrates a MOS device 100C formed on a substrate 102 and configured with boron doped germanium layers 117/119 between the respective source/drain layers 110/112 and contact metals 125/127, in accordance with another embodiment of the present invention. The source region 110 and the drain region 112 in this example embodiment are formed by implanting dopants such as boron into the substrate. The gate stack 122 is formed over a channel region 120 of the transistor 100C and is this example case does not include sidewalls 108. Nor does this example transistor structure include an undercut or tip regions like the embodiments shown in Figures 1A and 1B. The germanium overlayer 117/119 and the contact metals 125/127 can be implemented, for instance, as previously described with respect to Figure 1A.

[0027] Numerous other variations and features can be implemented for transistor structures configured in accordance with an embodiment of the present invention. For example, a graded buffer may be used in one or more locations of the structure. For instance, the substrate 102 can be a silicon substrate, or a silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate comprising silicon, silicon germanium, germanium, and/or III-V compound semiconductors. Thus, and by way of example, in an embodiment having a silicon or silicon germanium substrate 102 and an in situ boron doped SiGe fill in the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, a buffer can be provided between the underlying substrate 102 and the source/drain material. In one such embodiment, the buffer can be a graded boron doped (or intrinsic) silicon germanium layer with the germanium concentration graded from a base level compatible with the underlying substrate up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). The boron concentration within this buffer can be either fixed (e.g., at a high level) or graded, for instance, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 2E20 cm^{-3}). Note that 'compatibility' as used herein does not necessitate an overlap in concentration levels (for instance, the germanium concentration of underlying substrate can be 0 to 20 atomic % and initial germanium concentration of the buffer can be 30 to 40 atomic %). In addition, as used herein, the term 'fixed' with respect to a concentration level is intended to indicate a relatively

constant concentration level (e.g., the lowest concentration level in the layer is within 10% of the highest concentration level within that layer). In a more general sense, a fixed concentration level is intended to indicate the lack of an intentionally graded concentration level. The thickness of the buffer can vary depending on factors such as the range of concentrations being buffered, but in some embodiments is in the range of 30 to 120 Å, such as 50 to 100 Å (e.g., 60 Å or 65 Å). As will be further appreciated in light of this disclosure, such a graded buffer beneficially lowers the Schottky-barrier height.

[0028] Alternatively, rather than using a thin buffer between the substrate 102 and the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, the source/drain material itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, boron doped SiGe source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to 70 atomic %) up to 100 atomic %. In some such embodiments, the boron concentration within this boron doped germanium layer can range, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 2E20 cm^{-3}).

[0029] In other embodiments, a buffer can be provided between the source/drain material and the boron doped germanium overlayer 117/119. In one such embodiment, the source/drain material is a boron doped SiGe layer having a fixed concentration of germanium (e.g., in the range of 30 to 70 atomic %) and the buffer can be a thin SiGe layer (e.g., 30 to 120 Å, such as 50 to 100 Å) having a germanium concentration graded from a base level concentration compatible with the underlying boron doped SiGe layer up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). In some such cases, the boron concentration within this buffer can be fixed at a desired high level or can range, for example, from a base concentration at or otherwise compatible with the underlying SiGe layer up to the desired high concentration (e.g., in excess of 1E20 cm^{-3}, 2E20 cm^{-3}, or 3E20 cm^{-3}). Alternatively, rather than using a buffer between the source/drain material and the boron doped germanium overlayer 117/119, the overlayer 117/119 itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, the boron doped overlayer 117/119 can be configured with a germanium concentration graded from a base level

concentration compatible with the underlying substrate and/or source/drain regions (e.g., in the range of 30 to 70 atomic %) up to 100 atomic % (or near 100 atomic %). The boron concentration within this overlayer 117/119 layer can be fixed at a desired high level or can range, for example, from a base concentration at or otherwise compatible with the underlying substrate and/or source/drain regions up to the desired high level (e.g., in excess of 2E20 cm^{-3}).

[0030] Thus, a low contact resistance architecture for numerous transistor devices is provided. The devices may be formed in part using any number of conventional processes such as, for example, by gate oxide, poly gate electrode, thin spacer, and an isotropic undercut etch in the source/drain regions (or an ammonia etch to form faceted fin recess in monocrystalline substrate, or other suitable etch to form fin recess). In accordance with some embodiments, selective epitaxial deposition can be used to provide in situ doped silicon or alternatively, a fully strained silicon germanium layer to form source/drain regions with or without tips. Optional buffers may be used as previously explained. Any suitable high-k replacement metal gate (RMG) process flow can also be used, where a high-k dielectric replaces the conventional gate oxide. Silicidation with, for example, nickel, nickel-platinum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. The techniques provided herein can be applied, for example, to benefit any technology nodes (e.g., 90nm, 65nm, 45nm, 32nm, 22nm, 14nm, and 10nm transistors, and lower), and the claimed invention is not intended to be limited to any particular such nodes or range of device geometries. Other advantages will be apparent in light of this disclosure.

[0031] Figure 2 is a method for forming a transistor structure with low contact resistance in accordance with an embodiment of the present invention. Figures 3A through 3I illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments.

[0032] As can be seen, the method begins with forming 202 a gate stack on a semiconductor substrate upon which a MOS device, such as a PMOS transistor, may be formed. The semiconductor substrate may be implemented, for example, with a bulk silicon or a silicon-on-insulator configuration. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, such as germanium, silicon germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. In a more general sense, any material that may serve as

a foundation upon which a semiconductor device may be built can be used in accordance with embodiments of the present invention. The gate stack can be formed as conventionally done or using any suitable custom techniques. In some embodiments of the present invention, the gate stack may be formed by depositing and then patterning a gate dielectric layer and a gate electrode layer. For instance, in one example case, a gate dielectric layer may be blanket deposited onto the semiconductor substrate using conventional deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Alternate deposition techniques may be used as well, for instance, the gate dielectric layer may be thermally grown. The gate dielectric material may be formed, for example, from materials such as silicon dioxide or high-k dielectric materials. Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some specific example embodiments, the high-k gate dielectric layer may be between around 5 Å to around 200 Å thick (e.g., 20 Å to 50 Å). In general, the thickness of the gate dielectric layer should be sufficient to electrically isolate the gate electrode from the neighboring source and drain contacts. In further embodiments, additional processing may be performed on the high-k gate dielectric layer, such as an annealing process to improve the quality of the high-k material. Next, a gate electrode material may be deposited on the gate dielectric layer using similar deposition techniques such as ALD, CVD, or PVD. In some such specific embodiments, the gate electrode material is polysilicon or a metal layer, although other suitable gate electrode materials can be used as well. The gate electrode material, which is may be a sacrificial material that is later removed for a replacement metal gate (RMG) process, has a thickness in the range of 50Å to 500Å (e.g., 100Å), in some example embodiments. A conventional patterning process may then be carried out to etch away portions of the gate electrode layer and the gate dielectric layer to form the gate stack, as shown in Figure 3A. As can be seen, Figure 3A illustrates a substrate 300 upon which a gate stack is formed. In this example embodiment, the gate stack includes a gate dielectric layer 302 (which may be high-k gate dielectric material) and a sacrificial gate electrode 304. In one specific example case, the gate stack includes a silicon dioxide gate dielectric layer 302 and a polysilicon gate electrode

304. The gate stack may also include a gate hard mask layer 306 that provides certain benefits or uses during processing, such as protecting the gate electrode 304 from subsequent ion implantation processes. The hard mask layer 306 may be formed using typical hard mask materials, such as such as silicon dioxide, silicon nitride, and/or other conventional dielectric materials. Figure 3A further illustrates spacers 310 formed on either side of the stack. The spacers 310 may be formed, for example, using conventional materials such as silicon oxide, silicon nitride, or other suitable spacer materials. The width of the spacers 310 may generally be chosen based on design requirements for the transistor being formed. In accordance with some embodiments, however, the width of the spacers 310 is not subject to design constraints imposed by the formation of the source and drain epi-tips, given sufficiently high boron doped germanium content in the source/drain tip regions, as described herein (boron won't diffuse into channel).

[0033] With further reference to Figure 2, after the gate stack is formed, the method continues with defining 204 the source/drain regions of the transistor structure. As previously explained, the source/drain regions can be implemented with any number of suitable processes and configurations. For example, the source/drain regions may be implanted, etched and epi filled, raised, silicon or SiGe alloy, p-type and/or n-type, and have a planar or fin shaped diffusion region. In the example embodiment shown in Figure 3A, substrate 300 has been etched to provide cavities 312/314 as well as respective tip areas 312A/314A which undercuts the gate dielectric 302. Figure 3B illustrates the substrate 300 after cavities 312/314 and tip areas 312A/314A have been filled to provide the source/drain regions 318/320 and tip regions 318A/320A. In accordance with some example embodiments, the source and drain region cavities 312/314 along with their respective tip areas 312A/314A are filled with in situ doped silicon or SiGe, thereby forming source region 318 (along with epi-tip 318A) and drain region 320 (along with drain epi-tip 320A). Any number of source/drain layer configurations can be used here, with respect to materials (e.g., silicon, SiGe, III-V materials), dopant (e.g., boron in excess of 2E21 cm^{-3}, or other suitable dopant/concentration), and dimension (e.g., thickness of source/drain layer may range, for instance, from 50 to 500 nm so as to provide a flush or raised source/drain region).

[0034] As previously explained, some such embodiments may include with a thin buffer between the source/drain layer and the substrate or the source/drain and boron doped germanium overlayer. For instance, and as can further be seen in the example embodiment shown in Figure

3B, a source buffer 313 and a drain buffer 315 are deposited prior to depositing the source/drain materials. In some embodiments, the buffers 313 and 315 can be a graded boron doped silicon germanium layer with the germanium composition graded from a base level concentration compatible with the underlying substrate 300 material up to 100 atomic % (or near to 100 atomic % as previously described). The boron concentration can be appropriately graded as well. Numerous buffer schemes will be apparent in light of this disclosure.

[0035] With further reference to Figure 2, after the source/drain regions are defined, the method continues with depositing 206 boron doped germanium on the source/drain regions of the transistor structure. Figure 3C shows the boron doped germanium layer 317/319. In some example embodiments, the boron doped germanium layer 317/319, which may be epitaxially deposited in one or more layers, has a germanium concentration in excess of 90 atomic %, although other suitable concentration levels can be used as will be appreciated in light of this disclosure (e.g., in excess of 91 atomic %, or 92 atomic %, …, or 98 atomic %, or 99 atomic %, or truly pure germanium). As previously explained, this germanium concentration may be fixed or graded so as to increase from a base level (near substrate 300) to a high level (e.g., in excess of 90 atomic %). The boron concentration in some such embodiments can be in excess of 1E20 cm^{-3}, such as higher than 2E20 cm^{-3} or 2E21 cm^{-3}, and may also be graded so as to increase from a base level near substrate 300 to a high level (e.g., in excess of 1E20 cm^{-3} or 2E20 cm^{-3} or 3E20 cm^{-3}, …, 2E21 cm^{-3}). In embodiments where the germanium concentration of the underlying source/drain regions 318/320 is fixed or otherwise relatively low, a graded buffer may be used to better interface source/drain regions 318/320 with the boron doped germanium layer 317/319, as previously explained. The thickness of the boron doped germanium cap 317/319 may have a thickness in the range, for example, of 50 to 250 Å, in accordance with some specific example embodiments, although alternative embodiments may have other layer thicknesses, as will be apparent in light of this disclosure.

[0036] In some embodiments, a CVD process or other suitable deposition technique may be used for the depositing 206 or otherwise forming the boron doped germanium layer 317/319. For example, the depositing 206 may be carried out in a CVD, or rapid thermal CVD (RT-CVD), or low pressure CVD (LP-CVD), or ultra-high vacuum CVD (UHV-CVD), or gas source molecular beam epitaxy (GS-MBE) tool using germanium and boron containing precursors such as germane (GeH_4) or digermane (Ge_2H_6) and diborane (B_2H_6) or boron difluoride (BF_2). In

some such embodiments, there may be a carrier gas such as, for instance, hydrogen, nitrogen, or a noble gas (e.g., precursor is diluted at 1-5% concentration of carrier gas). There may also be an etchant gas such as, for example, halogen-based gas such as hydrogen chloride (HCl), chlorine (Cl), or, hydrogen bromide (HBr). The basic deposition of germanium and also boron doped germanium is possible over a wide range of conditions using deposition temperature in the range, for example, of 300°C to 800°C (e.g., 300-500°C) and reactor pressure, for instance, in the range 1 Torr to 760 Torr. Germanium is naturally selective in that it deposits on silicon or silicon-germanium alloy, and does not deposit on other materials such as silicon dioxide and silicon nitride. Since this natural selectivity is not entirely perfect, a small flow of etchant can be used to increase the selectivity of the deposition, as previously noted. Each of the carrier and etchants can have a flow in the range of 10 and 300 SCCM (typically, no more than 100 SCCM of flow is required, but some embodiments may require higher flow rates). In one specific example embodiment, the deposition 206 is carried out using GeH_4 that is diluted in hydrogen at a 1% concentration and at a flow rate that ranges between 100 and 1000 SCCM. For an in situ doping of boron, diluted B_2H_6 may be used (e.g., the B_2H_6 may be diluted in H_2 at 3% concentration and at a flow rate that ranges between 100 and 600 SCCM. In some such specific example cases, an etching agent of HCl or Cl_2 is added at a flow rate that ranges, for example, between 10 and 100 SCCM, to increase the selectivity of the deposition.

[0037] As will be appreciated in light of this disclosure, the selectivity at which the boron doped germanium layer 317/319 is deposited can vary as desired. In some cases, for instance, the boron doped germanium layer 317/319 is deposited only on the source/drain regions 318/320 or a portion of the source/drain regions 318/320 (rather than across the entire structure). Any number of masking/patterning techniques can be used to selectively deposit layer 317/319. Moreover, other embodiments may benefit from layer 317/319 covering, for example, poly gate regions or grounding tap regions. As will further be appreciated in light of this disclosure, the combination of high germanium concentration (e.g., in excess of 90 atomic % and up to pure germanium) and high boron concentration (e.g., in excess of 2E20 cm^{-3}) can be used to realize significantly lower contact resistance in the source and drain regions (and other areas where low contact resistance is desirable, such as ground tap regions), in accordance with some example embodiments. Further, and as previously explained, since boron diffusion is sufficiently suppressed by pure germanium, no adverse SCE degradation is realized with subsequent thermal

anneals despite any high boron concentration proximate the channel (if applicable). Barrier height lowering is also enabled from the higher concentration of germanium at the contact surface. In some example embodiments, a germanium concentration in excess of 95 atomic % and up to pure germanium (100 atomic %) can be used to achieve such benefits.

[0038] With further reference to Figure 2, after the boron doped germanium layer 317/319 is provided, the method continues with depositing 208 a dielectric over layer 317/319. Figure 3D shows dielectric 322 as being flush with the hard mask 306 of the gate stack, but it need not be. The dielectric can be configured in a number of ways. In some embodiments, dielectric 322 is implemented with silicon dioxide (SiO_2) or other low-k dielectric materials. In other embodiments, dielectric 322 is implemented with a silicon nitride (SiN) liner followed by one or more layers of SiO_2, or any combination of nitride, oxide, oxynitride, carbide, oxycarbide, or other suitable dielectric materials). The dielectric 322, which may be referred to as an interlayer dielectric (ILD), may be planarized as commonly done. Other example dielectric materials include, for instance, carbon doped oxide (CDO), organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. In some example configurations, the ILD layer may include pores or other voids to further reduce its dielectric constant.

[0039] Next, in some embodiments of the present invention where a replacement metal gate (RMG) process is used and as best shown in Figure 3E, the method may further include removing the gate stack (including the high-k gate dielectric layer 302, the sacrificial gate electrode 304, and the hard mask layer 306) using an etching process as conventionally done. In alternate implementations, only the sacrificial gate 304 and hard mask layer 306 are removed. Figure 3E illustrates the trench opening that is formed when the gate stack is etched away, in accordance with one such embodiment. If the gate dielectric layer is removed, the method may continue with depositing a new gate dielectric layer into the trench opening (designated as 324 in Figure 3F). Any suitable high-k dielectric materials such as those previously described may be used here, such as hafnium oxide. The same deposition processes may also be used. Replacement of the gate dielectric layer may be used, for example, to address any damage that may have occurred to the original gate dielectric layer during application of the dry and wet etch processes, and/or to replace a low-k or sacrificial dielectric material with a high-k or otherwise desired gate dielectric material. As further shown in Figure 3F, the method may further continue

with depositing the metal gate electrode layer 326 into the trench and over the gate dielectric layer 324. Conventional metal deposition processes may be used to form the metal gate electrode layer, such as CVD, ALD, PVD, electroless plating, or electroplating. The metal gate electrode layer may include, for example, a P-type workfunction metal, such as ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. In some example configurations, two or more metal gate electrode layers may be deposited. For instance, a workfunction metal may be deposited in the gate trench followed by a suitable metal gate electrode fill metal such as aluminum or silver.

[0040] With further reference to Figure 2, after dielectric layer 322 is provided over layer 317/319 (and any desired RMG process), the method continues with etching 210 to form the source/drain contact trenches. Any suitable dry and/or wet etch processes can be used. Figure 3G shows the source/drain contact trenches after etching is complete, in accordance with one example embodiment. The method then continues with depositing 212 contact resistance reducing metal and annealing to form silicide/germanide, and then depositing 214 the source/drain contact plugs. Figure 3H shows the contact metals 325/327, which in some embodiments includes the silicide/germanide, although other embodiments may include additional layers (e.g., adhesion layer). Figure 3I shows the contact plug metal 329/331, which in some embodiments includes aluminum, although any suitably conductive contact metal or alloy can be used for the contact plug 329/331, such as silver, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium, using conventional deposition processes. The germanide/metalization 212 of the source and drain contacts can be carried out, for instance, by silicidation with nickel, aluminum, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants to form a low resistance germanide. The boron doped germanium layer 317/319 allows for metal-germanide formation (e.g., nickel-germanium). The germanide allows for significantly lower Schottky-barrier height and improved contact resistance (including R_{ext}) over that in conventional metal-silicide systems. For instance, conventional transistors typically use a source/drain SiGe epi process, with germanium concentration in the range of 30-40 atomic %. Such conventional systems exhibit R_{ext} values of about 140 Ohm*um, limited by epi/silicide interfacial resistance, which is high and may impede future gate pitch scaling. Some embodiments of the present invention allow for a significant improvement in R_{ext} in PMOS

devices (e.g., about a 2x improvement or better, such as a R_{ext} of about 70 Ohm*um), which can better support PMOS device scaling. Thus, transistors having a source/drain configured with boron doped germanium cap 317/319 in accordance with an embodiment of the present, with a boron concentration in excess of 1E20 cm^{-3} and a germanium concentration in excess of 90 atomic % and up to or otherwise near pure germanium (100 atomic %) at the interface between the source/drain regions 318/320 and the contact metals 325/327, can exhibit R_{ext} values of less than 100 Ohm*um, and in some cases less than 90 Ohm*um, and in some cases less than 80 Ohm*um, and in some cases less than 75 Ohm*um, or lower.

[0041] Figure 4 is a method for forming a transistor structure with low contact resistance in accordance with another embodiment of the present invention. Figures 5A through 5F illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments. In general, this method is similar to the method described with reference to Figures 2 and 3A-H, except that the deposition of the boron doped germanium layer 317/319 on the source/drain regions is carried out after the dielectric 322 is deposited and etched to form the contact trench. Thus, the method includes depositing 406 the dielectric 322 directly over the source/drain regions 318/320, and then continues with etching 408 to form the source/drain contact trench and then selectively deposting 410 the boron doped germanium layer 317/319 into the trench (and directly onto the source/drain regions 318/320), as best shown in Figures 5C through 5E. Deposting 410 can be carried out using any suitable deposition process, such as selective epitaxy. Once layer 317/319 is provided, the contact metals 325/327 can be provided on top of the layer 317/319, as shown in Figure 5F. This alternate methodology provides the same benefit of improved contact resistance, but is more selective in where the boron doped germanium is deposited. Other such selective deposition processes will be apparent in light of this disclosure, using any suitable combination of masking/patterning and selective deposition techniques.

[0042] As will be further appreciated, the previous relevant discussion with respect to similar parts of the method is equally applicable here. In particular, forming 402 a gate stack and defining 404 the source/drain regions of the transistor structure can be carried as previously discussed with reference to the forming 202 and defining 204 previously discussed with reference to Figure 2. Likewise, depositing 412 contact resistance reducing metal and annealing to form silicide/germanide, and then depositing 414 the source/drain contact plugs can be carried

as previously discussed with reference to the forming 212 and defining 214 previously discussed with reference to Figure 2.

FinFET Configuration

[0043] As is known, FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin). The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, a source region, and a drain region. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both sidewalls of the fin (sides perpendicular to the substrate surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate FinFET. Other types of FinFET configurations are also available, such as so-called double-gate FinFETs, in which the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin).

[0044] Figure 6 shows a perspective view of an example tri-gate architecture, configured in accordance with one embodiment of the present invention. As can be seen, the tri-gate device includes a substrate 600 having a semiconductor body or fin 660 (represented by dashed lines) extending from the substrate 600 through isolation regions 610, 620. A gate electrode 640 is formed over 3 surfaces of the fin 660 to form 3 gates. A hard mask 690 is formed on top of the gate electrode 640. Gate spacers 670, 680 are formed at opposite sidewalls of the gate electrode 640.

[0045] A source region comprises the epitaxial region 631 formed on a recessed source interface 650 and on one fin 660 sidewall, and a drain region comprises the epitaxial region 631 formed on a recessed source interface 650 and on the opposing fin 660 sidewall (not shown). A cap layer 641 is deposited over the epitaxial regions 631. Note that the boron cap layer 641 may be provided in the recessed (tip) regions, but in other embodiments is just provided over the source/drain regions (and not in the recessed regions). In one embodiment, the isolation regions 610, 620 are shallow trench isolation (STI) regions formed using conventional techniques, such as etching the substrate 600 to form trenches, and then depositing oxide material onto the trenches to form the STI regions. The isolation regions 610, 620 can be made from any suitable dielectric/insulative material, such as SiO_2. The previous discussion with respect to the substrate

102 is equally applicable here (e.g., substrate 600 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).

[0046] As will be appreciated in light of this disclosure, conventional processes and forming techniques can be used to fabricate the FinFET transistor structure. However, and in accordance with one example embodiment of the present invention, the bilayer structure of the epitaxial region 631 and cap layer 641 can be implemented, for instance, using an in situ doped silicon or SiGe (for 631) capped with a boron doped germanium (for 641), with an optional germanium and/or boron graded buffer between the two bilayers. As previously explained, such a buffer may be used to transition from a base level germanium/boron concentration compatible with the epitaxial region 631 to the boron doped germanium cap 641. Alternatively, germanium and/or boron concentration grading can be implemented directly in the epitaxial region 631 and/or the cap 641, rather than in an intervening graded buffer arrangement. As will further be appreciated, note that an alternative to the tri-gate configuration is a double-gate architecture, which includes a dielectric/isolation layer on top of the fin 660.

[0047] Figure 7 shows a plot of a split lot showing contact resistance for transistor structures configured with in accordance with embodiments of the present invention and standard transistor structures configured with no cap. The transistor structures associated with the high resistance numbers in excess of 0.18 are all implemented with standard SiGe alloy raised PMOS source/drain regions with contact metal deposited directly thereon. The transistor structures associated with the resistance numbers of 0.107 and lower are all similarly implemented but with the addition a boron doped germanium cap between the source/drain regions and contact metal, in accordance with various embodiments of the present invention. Table 1 shows the raw data quantiles resulting from testing of the example structures with and without a boron doped germanium cap as described herein.

Ge Cap	Min	10%	25%	Median	75%	90%	Max
Yes	0.032	0.032	0.033	0.040	0.078	0.105	0.107
No	0.183	0.183	0.192	0.239	0.250	0.265	0.265

Table 1

As can be seen, this example lot actually shows an improvement (reduction) in contact resistance of about a three to six times (3X to 6X) over conventional transistor structures. The units are Ohms per arbitrary area.

[0048] Other improvements enabled by using a boron doped germanium cap in accordance with an embodiment of the present invention will be apparent in light of this disclosure. In particular, the resulting germanide materials and Schottky barrier height improvement enables more than a 2x R_{ext} improvement over that in conventional SiGe source/drain PMOS devices, in accordance with some example embodiments of the present invention. As is known, the Schottky barrier height is the barrier for electrical conduction across a semiconductor-metal junction. The magnitude of the Schottky barrier height reflects a mismatch in the energy position of the metal's Fermi level and the majority carrier band edge of the semiconductor across the semiconductor-metal interface. For a p-type semiconductor-metal interface, the Schottky barrier height is the difference between the metal Fermi level and the valence band maximum of the semiconductor.

Example System

[0049] Figure 8 illustrates a computing device 1000 configured in accordance with one embodiment of the invention. As can be seen, the computing device 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board or a daughterboard mounted on a main board or the only board of device 1000, etc. Depending on its applications, computing device 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing device 1000 may include one or more transistor

structures as described herein. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

[0050] The communication chip 1006 enables wireless communications for the transfer of data to and from the computing device 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0051] The processor 1004 of the computing device 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments of the present invention, the integrated circuit die of the processor includes an onboard non-volatile memory or cache, and/or is otherwise communicatively coupled to off-chip memory that is implemented with one or more transistor structures as described herein. The term "processor" may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0052] The communication chip 1006 may also include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more devices implemented with one or more transistor structures as described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the

processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

[0053] In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the device 1000 may be any other electronic device that processes data or employs transistors.

[0054] Numerous embodiments will be apparent in light of this disclosure, and features described herein can be combined in any number of configurations. One example embodiment of the present invention provides a transistor device. The device includes a substrate having a channel region, and a gate electrode above the channel region. A gate dielectric layer is provided between the gate electrode and the channel region, and source and drain regions are provided in the substrate and adjacent to the channel region. The device further includes a boron doped germanium layer on at least a portion of the source and drain regions. This boron doped germanium layer comprises a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}. The device further includes metal-germanide source and drain contacts on the boron doped germanium layer. In one such example, the device is one of a planar or FinFET transistor. In another example case, the device comprises a PMOS transistor. In another example case, the device further includes an interlayer dielectric. In another example case, the device further includes a graded buffer between the substrate and the source and drain regions and/or a graded buffer between the source and drain regions and the boron doped germanium layer. In one such case, the graded buffer between the source and drain regions and the boron doped germanium layer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %. In one such specific example case, the high concentration reflects pure germanium. In another example case, the graded buffer between the source and drain regions and the boron doped germanium layer has a boron concentration that is graded from a base level

concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron. In another example case, the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %. In another example case, the source and drain regions comprise boron doped silicon germanium having a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}. In another example case, the source and drain regions comprise silicon or silicon germanium, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}. In another example case, the boron doped germanium layer comprises a germanium concentration in excess of 98 atomic %, and a boron concentration in excess of 2E20 cm^{-3}. Another embodiment provides an electronic device that includes a printed circuit board having one or more integrated circuits, wherein at least one of the one or more integrated circuits comprises one or more transistor devices as variously defined in in this paragraph. In one such case, the one or more integrated circuits includes at least one of a communication chip and/or a processor, and at least one of the communication chip and/or processor comprises the one or more transistor devices. In another such case, the device is a computing device (e.g., mobile telephone or smartphone, laptop, tablet computer, etc).

[0055] Another embodiment of the present invention provides a transistor device. In this example case, the device includes a substrate having a channel region, and a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The device further includes source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers. The device further includes a boron doped germanium layer

on at least a portion of the source and drain regions, and comprising a germanium concentration in excess of 95 atomic % and a boron concentration in excess of 2E20 cm^{-3}. The device further includes metal-germanide source and drain contacts on the boron doped germanium layer. The device is one of a planar or FinFET transistor. In one such example case, the device further includes a buffer between the source and drain regions and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron. In another example case, the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 98 atomic %. In another example case, the source and drain regions have a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}. In another example case, the source and drain regions comprise silicon germanium having a fixed germanium concentration, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms. Another embodiment provides a computing device (e.g., desktop or portable computer, etc) that includes a printed circuit board having a communication chip and/or a processor, wherein at least one of the communication chip and/or processor comprises one or more transistor devices as variously defined in this paragraph.

[0056] Another embodiment of the present invention provides a method for forming a transistor device. The method includes providing a substrate having a channel region, and providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region. The method continues with providing source

and drain regions in the substrate and adjacent to the channel region, and providing a boron doped germanium layer on at least a portion of the source and drain regions. The boron doped germanium layer comprises a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}. The method continues with providing metal-germanide source and drain contacts on the boron doped germanium layer. In some example such cases, the method further includes providing a graded buffer between the substrate and the source and drain regions, and/or providing a graded buffer between the source and drain regions and the boron doped germanium layer. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron (which may be used with or without graded buffers). This method may be employed, for example, in the fabrication of any electronic devices such as a computing device.

[0057] The foregoing description of example embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

CLAIMS

What is claimed is:

1. A transistor device, comprising:

source and drain regions adjacent to a channel region;

a boron doped germanium layer on at least a portion of the source and drain regions, the boron doped germanium layer comprising a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3}; and

a contact on the boron doped germanium layer, the contact including metal-germanide.

ABSTRACT OF THE DISCLOSURE

Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on, for example, silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures. Graded buffering can be used to reduce misfit dislocation. The techniques are particularly well-suited for implementing p-type devices, but can be used for n-type devices if so desired.

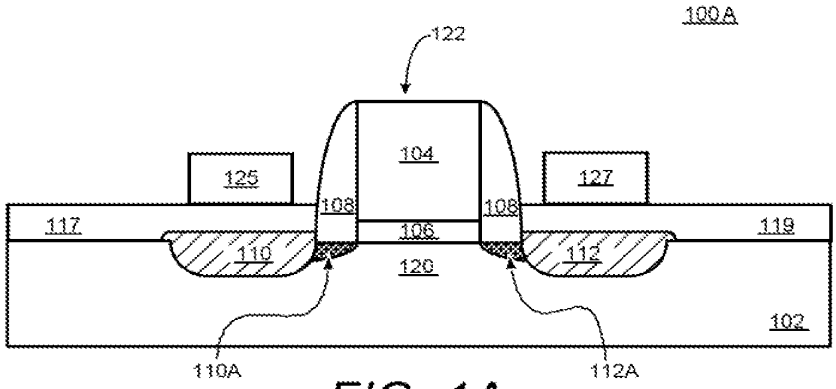


FIG. 1A

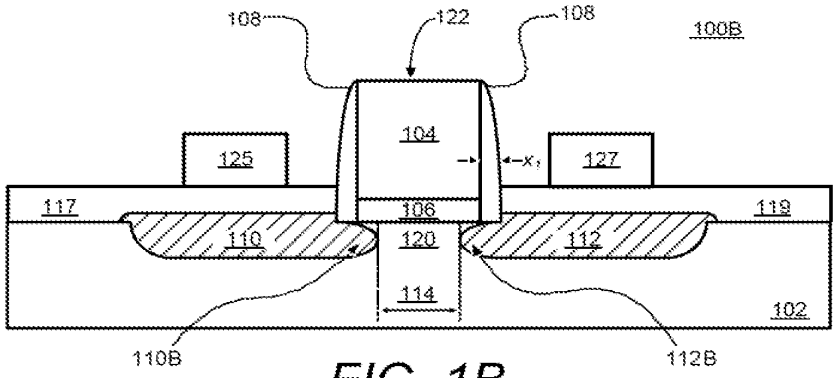


FIG. 1B

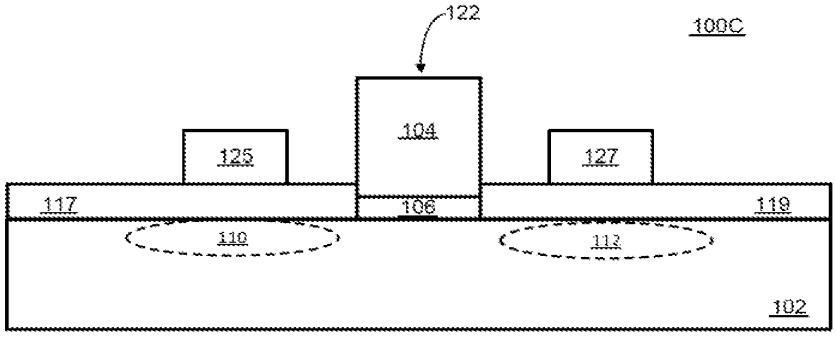


FIG. 1C

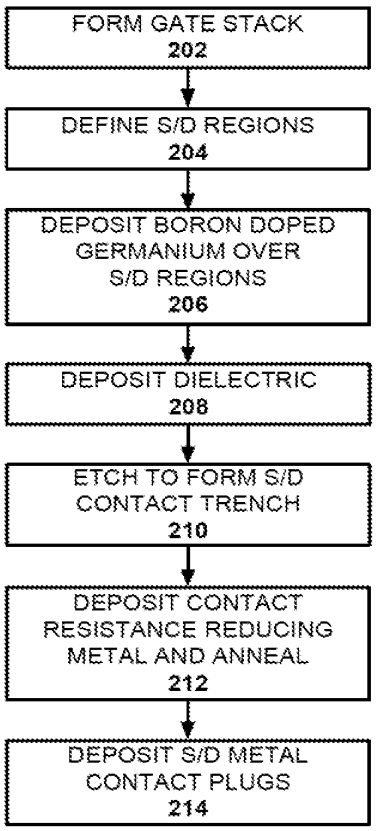

FORM GATE STACK
202
DEFINE S/D REGIONS
204
DEPOSIT BORON DOPED GERMANIUM OVER S/D REGIONS
206
DEPOSIT DIELECTRIC
208
ETCH TO FORM S/D CONTACT TRENCH
210
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
212
DEPOSIT S/D METAL CONTACT PLUGS
214

FIG. 2

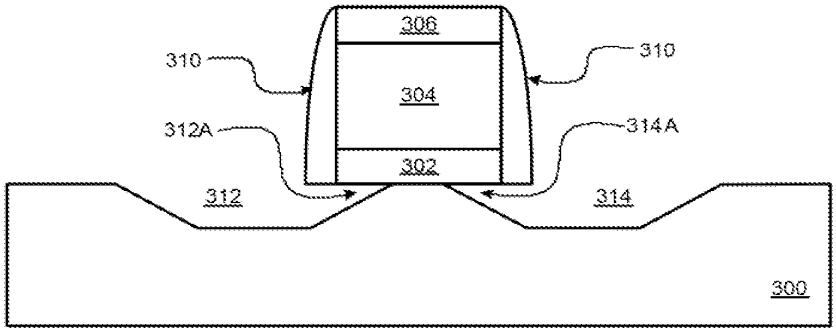


FIG. 3A

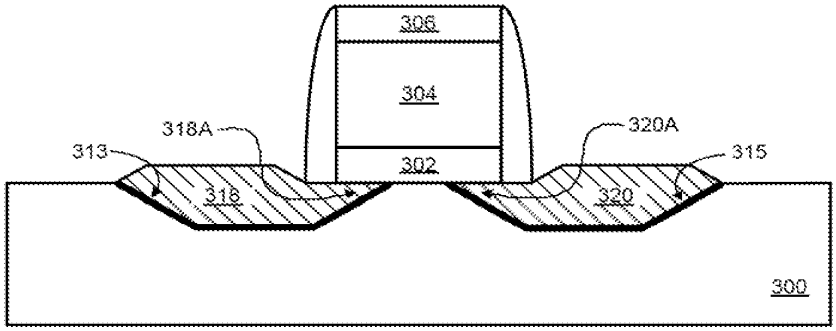


FIG. 3B

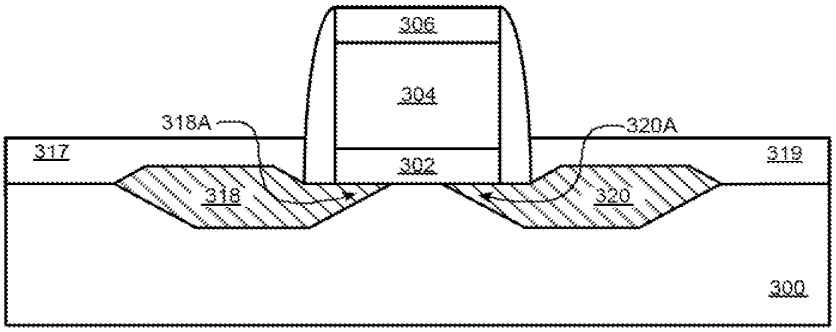


FIG. 3C

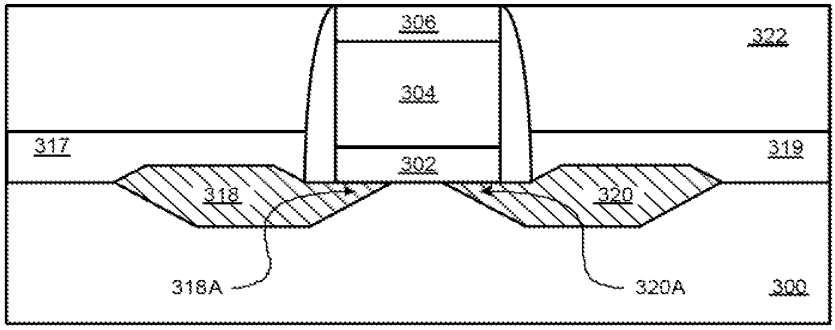


FIG. 3D

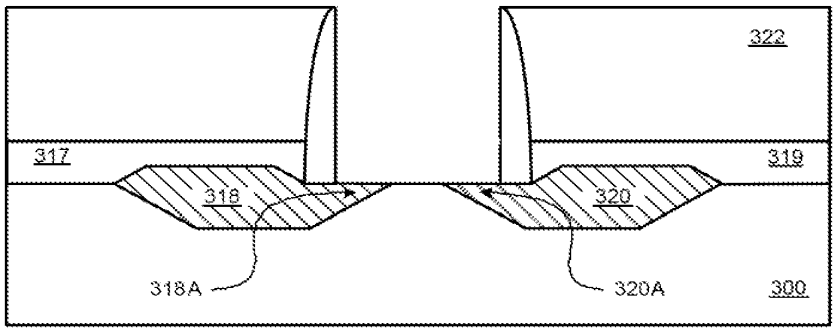


FIG. 3E

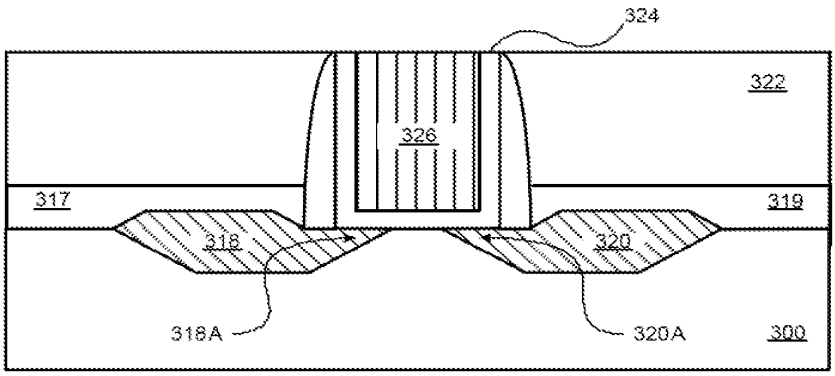


FIG. 3F

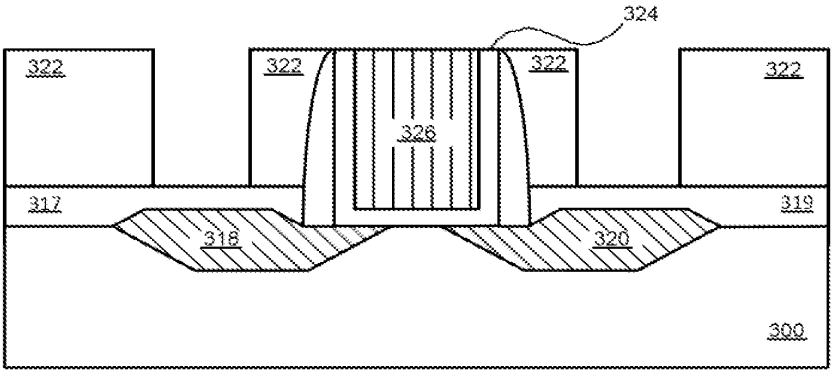


FIG. 3G

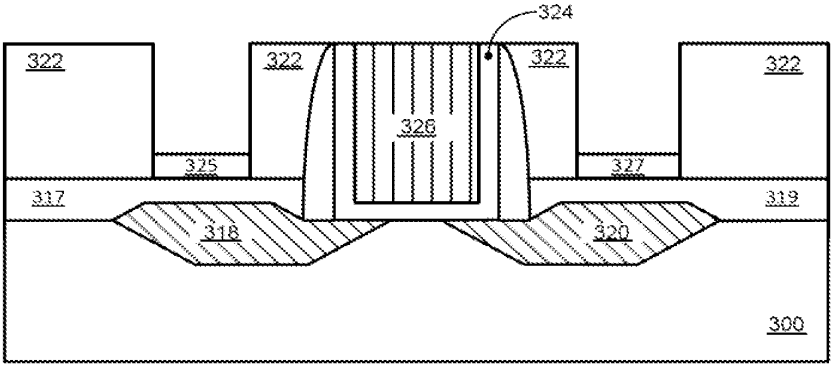


FIG. 3H

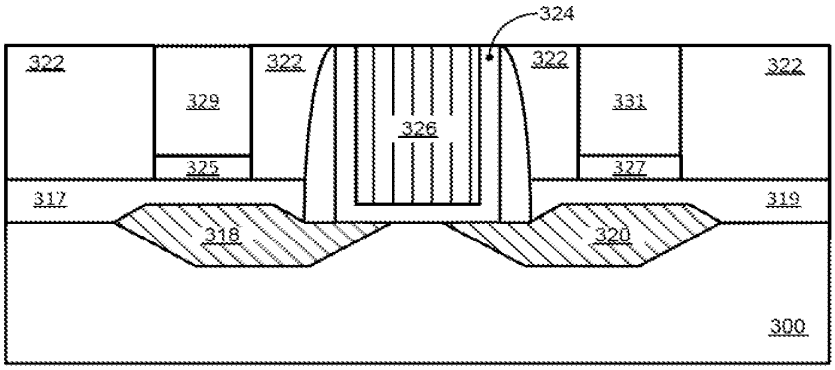


FIG. 3I

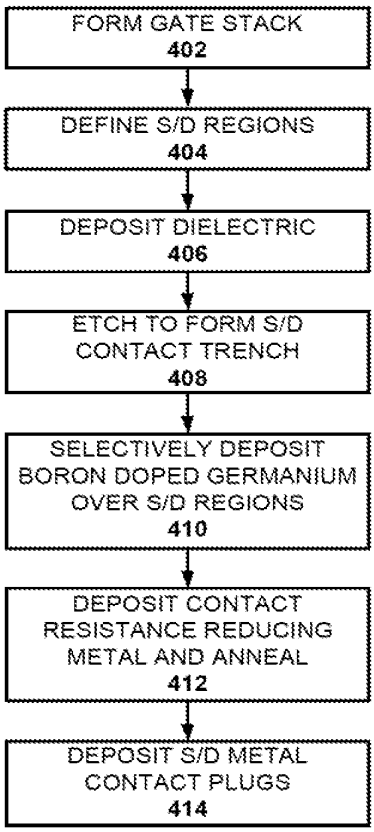

FORM GATE STACK
402
DEFINE S/D REGIONS
404
DEPOSIT DIELECTRIC
406
ETCH TO FORM S/D CONTACT TRENCH
408
SELECTIVELY DEPOSIT BORON DOPED GERMANIUM OVER S/D REGIONS
410
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
412
DEPOSIT S/D METAL CONTACT PLUGS
414

FIG. 4

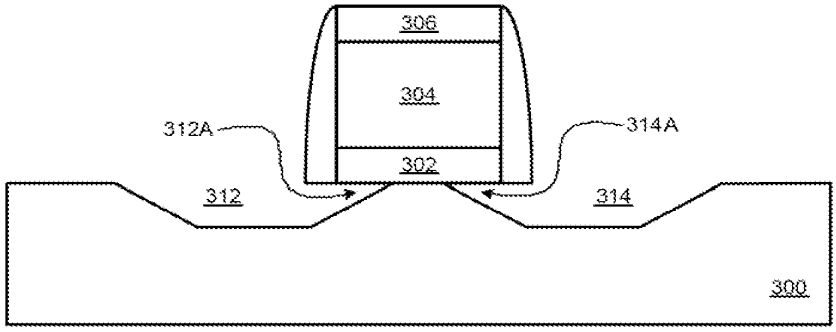


FIG. 5A

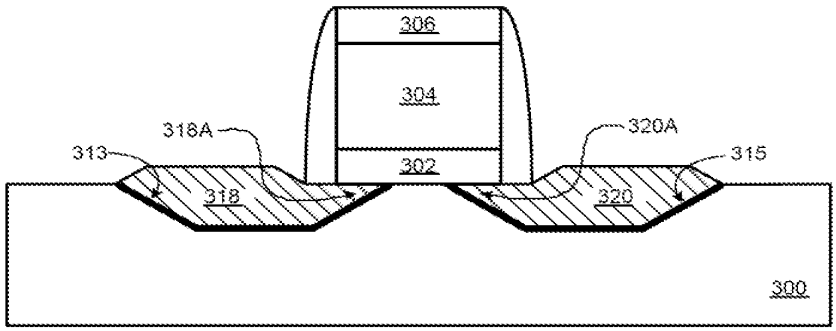


FIG. 5B

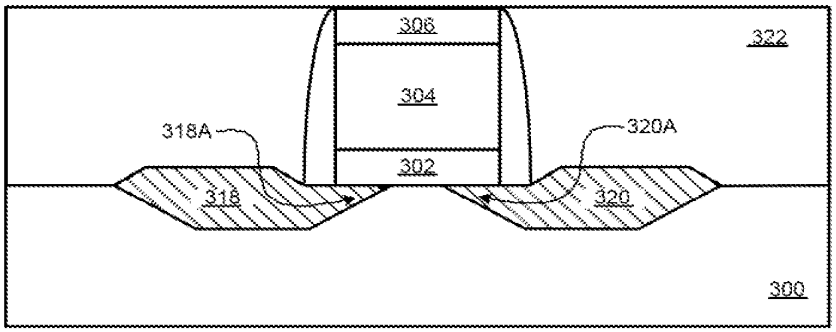


FIG. 5C

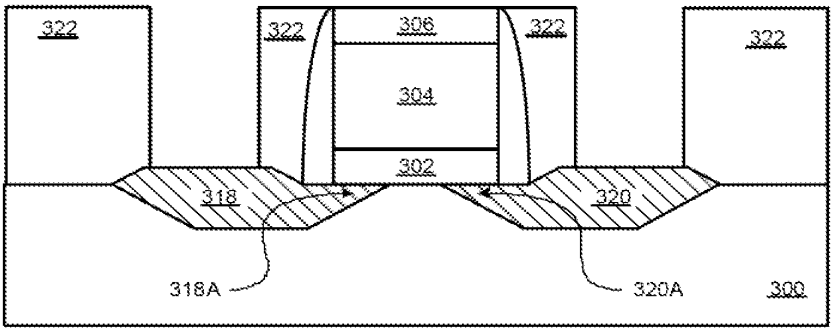


FIG. 5D

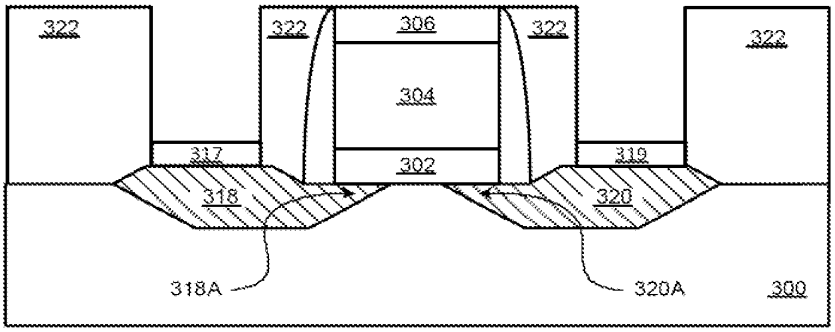


FIG. 5E

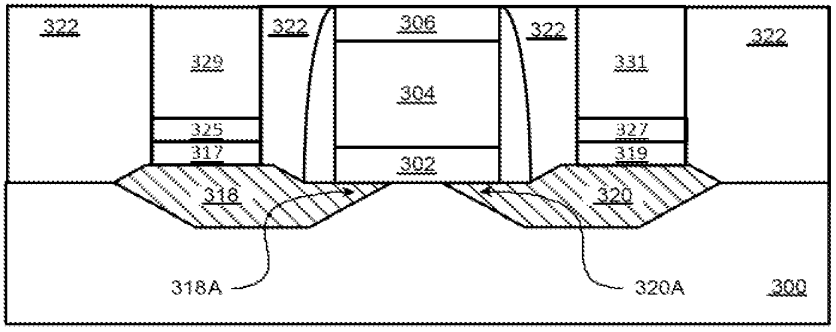


FIG. 5F

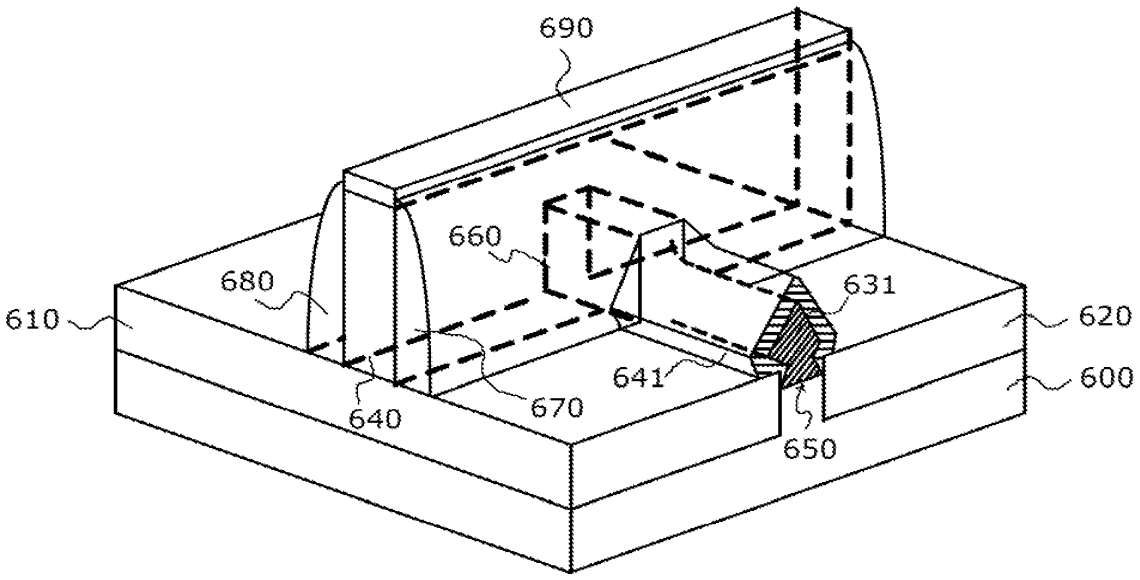


FIG. 6

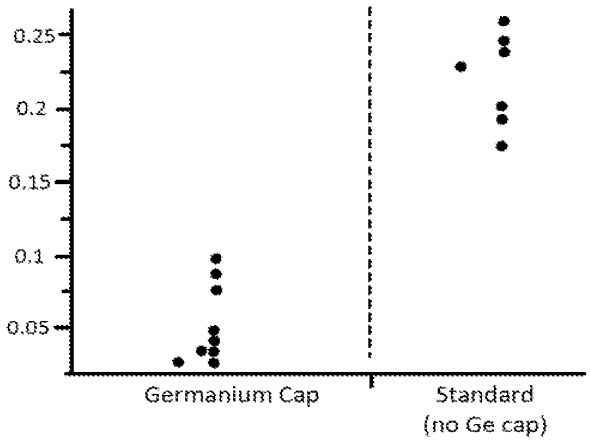


FIG. 7

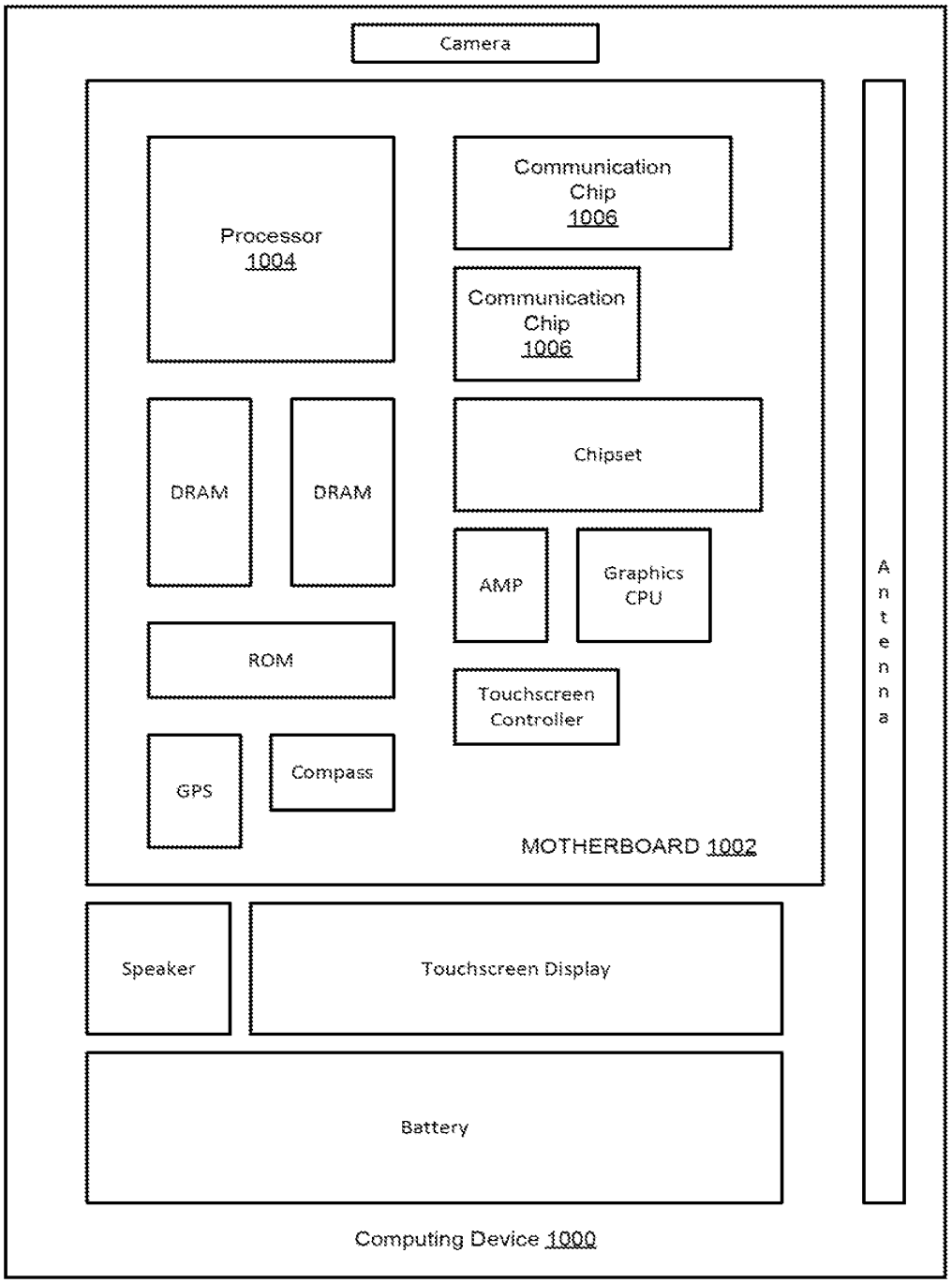

Camera
Processor
1004
Communication
Chip
1006
Communication
Chip
1006
DRAM
DRAM
Chipset
AMP
Graphics
CPU
ROM
Touchscreen
Controller
GPS
Compass
MOTHERBOARD 1002
Antenna
Speaker
Touchscreen Display
Battery
Computing Device 1000

Fig. 8

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

As the below named inventor, I hereby declare that:

This declaration is directed to: ■ The attached application, or

☐ United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: GLENN A. GLASS Date (Optional): 5-22-13

Signature: Glenn A. Glass

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

As the below named inventor, I hereby declare that:

This declaration is directed to: ■ The attached application, or

☐ United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: ANAND S. MURTHY Date (Optional): 5/23/13

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (08-12)
Approved for use through 01/31/2014 OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

As the below named inventor, I hereby declare that:

This declaration is directed to: ■ The attached application, or

☐ United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: TAHIR GHANI Date (Optional): 5-23-13

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Filer:	Justin K. Brask/Sheri Villarreal
Attorney Docket Number:	P38507USC2-C1-C1 111548
Filed as Large Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1720

Electronic Acknowledgement Receipt	
EFS ID:	39518177
Application Number:	16881541
International Application Number:	
Confirmation Number:	8383
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Customer Number:	31817
Filer:	Justin K. Brask/Sheri Villarreal
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38507USC2-C1-C1 111548
Receipt Date:	22-MAY-2020
Filing Date:	
Time Stamp:	14:34:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1720
RAM confirmation Number	E20205LE35364117
Deposit Account	500393
Authorized User	Sheri Villarreal
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	P38507USC2-C1-C1_ADS_05_22_20.pdf	1823675 4fca0b64ce4dc1629a7757076678b67bfd1f218e	no	9
Warnings:					
Information:					
2		P38507USC2-C1-C1_APP_05_22_20.pdf	201152 e473e12cdbd079c9c571e84b33aee6c200bdef87	yes	27

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	25
	Claims	26	26
	Abstract	27	27

Warnings:					
Information:					
3	Drawings-only black and white line drawings	P38507USC2-C1-C1_FIGS_05_22_20.pdf	834128 e2c65a5e494bbefe039bf9df528a28ae0a079b17	no	11
Warnings:					
Information:					
4	Oath or Declaration filed	P38507USC2-C1-C1_DEC_05_22_20.pdf	1463377 3083c1275816f91b3af012972 4023cef3ba8cdd2	no	3
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	35059 b14f0e9477f29b962cbe4dc3a51e01ff6e25146f	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	4357391

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2811
	Examiner Name	N/A
Sheet 1 of 3	Attorney Docket No: P38507USC2-C1-C1 111548	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-5,312,766	05-17-1994	Sheldon Aronowitz et al.	
		US-5,296,387	03-22-1994	Sheldon Aronowitz et al.	
		US-5,296,386	03-22-1994	Sheldon Aronowitz et al.	
		US-7,821,044	10-26-2010	Mark T. Bohr et al.	
		US-8,575,652	11-05-2013	Yoshiki Kamata	
		US-7,221,006	05-22-2007	Marius Orlowski et al.	
		US-7,732,285	06-08-2010	Intel Corporation	
		US-7,880,228	02-01-2011	Toshiba Corp.	
		US-7,683,362	03-23-2010	Fujitsu Ltd.	
		US-7,667,227	02-23-2010	Fujitsu Ltd.	
		US-6,607,948	08-2003	Suigiyama, Naoharu	
		US-9,349,810	05-2016	Glass, Glenn A.	
		US-20030057416	03-27-2003	Matthew Currie	
		US-20050130454	06-16-2005	Anand Murthy et al.	
		US-20050184354	08-25-2005	Chu et al.	
		US-20060156080	07-13-2006	John P. Tellkamp et al	
		US-20060237746	10-26-2006	Marius Orlowski et al.	
		US-20060255330	11-16-2006	Chen et al.	
		US-20070187767	08-16-2007	Yasutake, Nobuaki	
		US-20070238236	10-11-2007	Ted Cook Jr. et al.	
		US-20070275548	11-29-2007	Lavoie et al.	
		US-20080135878	06-12-2008	Kim et al.	
		US-20080179752	07-31-2008	Takashi Yamauchi et al.	
		US-20080197412	08-21-2008	Zhang et al.	
		US-20080242037	10-02-2008	Bernhard Sell et al.	
		US-20090224369	09-10-2009	Harold Samuel Gamble et al.	
		US-20100148217	06-17-2010	Danielle Simonelli	
		US-20110062498	03-17-2011	Frank Yang et al.	
		US-20110068407	03-24-2011	Chih Chieh Yeh et al.	
		US-20120007051	01-12-2012	Sarunya Bangsaruntip et al.	
		US-20120037998	02-16-2012	Bedell et al.	
		US-20130240989	09-19-2013	Glenn Glass et al.	
		US-20140070377	03-13-2014	Yu et al.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2811
	Examiner Name	N/A
Sheet 2 of 3	Attorney Docket No: P38507USC2-C1-C1 111548	

		US-20090206370	08-2009	Chu, Jack O.	
		US-20090302348	12-2009	Adam, Thomas N.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
		JP-2007-165665	06-28-2007	Renesas Tech Corp		
		WO 2010-068530	06-17-2010	Intel Corporation		
		JP-2007-214481	08-23-2007	Toshiba Corp		
		CN-101622690	01-06-2010	Intel Corporation		
		JPH-07-169958	07-04-1995	NEC Corp		
		JPH-05-183160	07-23-1993	Toshiba Corp		
		JP-2007-318132	12-06-2007	IBM		
		JP-2007-036205	02-08-2007	Fujitsu Ltd.		
		JP-2006-186240	07-13-2006	Fujitsu Ltd.		
		JP-2012-510720	05-10-2012	Intel Corporation		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		International Search Report and Written Opinion for International Patent Application No. PCT/US11/054198 (Attorney Docket No. P38507PCT) mailed April 19, 2012, 13 pgs.	
		International Preliminary Report Patentability for International Patent Application No. PCT/US11/054198 (Attorney Docket No. P38507PCT) mailed July 4, 2013, 9 pgs.	
		Office Action for Korean Patent Application No. 2013-7016072 (Attorney Docket No. P38507KR) mailed May 23, 2014, 4 pgs., with English translation	
		Notice of Allowance for Korean Patent Application No. 2013-7016072 (Attorney Docket No. P38507KR) mailed November 13, 2014, 3 pgs., with English translation.	
		Office Action for Japanese Patent Application No. 2013-546134 (Attorney Docket No. P38507JP) mailed August 26, 2014, 4 pgs. of English translation and 3 pgs. with no translation.	
		Notice of Allowance for Japanese Patent Application No. 2013-546134 (Attorney Docket No. P38507JP) mailed February 10, 2015, 3 pgs., no translation.	
		Extended European Search Report for European Patent Application No. 11852027.9 (Attorney Docket No. P38507EP) mailed August 11, 2014, 14 pgs.	
		"Metal/Semi conductor Ohmic Contacts Technology or Gate Length Series Resistance (ohms)", 1997, XP055127433, Retrieved from the Internet: URL:http://web.stanford.edu/class/ee311/N0 TES/Ohmic_Contacts.pdf [retrieved on 2014-07-08] the whole document	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2811
	Examiner Name	N/A
Sheet 3 of 3	Attorney Docket No: P38507USC2-C1-C1 111548	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		Office Action for European Patent Application No. 11852027.9 (Attorney Docket No. P38507EP) mailed October 12, 2015, 4 pgs.	
		First Office Action for Chinese Patent Application No. 201180062116.2 (Attorney Docket No. P38507CN) mailed May 5, 2015, 6 pgs., no translation	
		Second Office Action for Chinese Patent Application No. 201180062116.2 (Attorney Docket No. P38507CN) mailed October 20, 2015, 3 pgs., no translation	
		Notice of Allowance for Chinese Patent Application No. 201180062116.2 (Attorney Docket No. P38507CN) mailed February 26, 2016, 4 pgs., with English translation	x
		First Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed May 4, 2018, 6 pgs., no translation	
		Second Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed December 3, 2018, 5 pgs., no translation	
		Third Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed April 10, 2019, 4 pgs., no translation	
		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed November 29, 2019, 6 pgs	
		Office Action for European Patent Application No. 11852027.9 (Attorney Docket No. P38507EP) mailed December 12, 2019, 2 pgs.	
		Search Report for European Patent Application No. 19188924.5 (Attorney Docket No. P38507EP-D1) mailed October 23, 2019, 2 pgs.	
		STANTON P. ASHBURN ET AL: FORMATION OF C54 TITANIUM GERMANOSILICIDE USING RAPID THERMAL PROCESSING AND APPLICATION TO RAISED, ULTRASHALLOW JUNCTIONS", MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, vol. 320, 1 January 1993, pages 311-316, XP055631293	
		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed March 24, 2020, 12 pgs.	
		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed April 24, 2020, 3 pgs.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	16/881,541
Filing Date	May 22, 2020
First Inventor	Glenn A. GLASS, et al.
Art Unit	2811
Examiner Name	N/A
Attorney Docket No.	P38507USC2-C1-C1 111548

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of the first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 CFR § l.98(d)(l) copies of the references were provided in prior applications 13/990,224 filed September 30, 2011, 14/673,143 filed March 30, 2015, 15/339,308 filed October 31, 2016, 16/416,445 filed May 20, 2019 which are relied on for priority.

It is respectfully requested that the examiner consider information which has been previously submitted to the Patent Office in the parent application and any prior related applications.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☐ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	05-26-2020
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Sheri Villarreal */Sheri Villarreal/* *Date* 05-26-2020

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Electronic Acknowledgement Receipt	
EFS ID:	39540051
Application Number:	16881541
International Application Number:	
Confirmation Number:	8383
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Customer Number:	31817
Filer:	Justin K. Brask/Sheri Villarreal
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38507USC2-C1-C1 111548
Receipt Date:	26-MAY-2020
Filing Date:	
Time Stamp:	18:50:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38507USC2-C1-C1_IDS_05_26_20.pdf	383191 d66b93ab23a15ef23375fdb7195cdd71e181dc0d	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Information Disclosure Statement (IDS) Form (SB08)	2	4
	Transmittal Letter	1	1
Warnings:			
Information:			
	Total Files Size (in bytes):	383191	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/881,541	Filing Date 05/22/2020	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	05/29/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/TINA M. BELL/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Glenn A. GLASS	Examiner: Not Yet Assigned
Application No.: 16/881,541	Art Unit: 2811
Filed: May 22, 2020	Confirmation No.: 8383
For: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Examiner:

Prior to examination of the above-referenced application, applicants respectfully request the Examiner to enter the following amendments and to consider the following remarks.

The Listing of Claims begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

Electronic Acknowledgement Receipt	
EFS ID:	39581495
Application Number:	16881541
International Application Number:	
Confirmation Number:	8383
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38507USC2-C1-C1 111548
Receipt Date:	29-MAY-2020
Filing Date:	
Time Stamp:	20:04:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Intel_P38507USC2-C1-C1_Preliminary_Amendment_05-29-20.pdf	95031 44a91a754e9b27aa439f1dec0d3c1a7fa62af4e5	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	10	10
	Claims	2	9
	Preliminary Amendment	1	1
Warnings:			
Information:			
	Total Files Size (in bytes):	95031	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Pursuant to 37 C.F.R. 1.136(a)(3), the Applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 50-0393.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, P.C.

May 29, 2020
Date

/Justin K. Brask/
Justin K. Brask
Reg. No. 61,080

1211 SW 5th, Ste. 1900
Portland, OR 97204
Telephone: (503) 222-9981
Facsimile: (503) 796-2900

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Canceled)

2. (New) An integrated circuit structure, comprising:

a fin comprising silicon;

a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;

a first dielectric spacer along the first side of the gate electrode;

a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a second dielectric spacer along the second side of the gate electrode;

a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;

a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;

a first contact plug in the first opening and on the first germanide layer; and

a second contact plug in the second opening and on the second germanide layer.

3. (New) The integrated circuit structure of claim 2, further comprising:

a first boron doped germanium layer on the first source or drain region, wherein the first germanide layer is on the first boron doped germanium layer, and wherein the first boron doped germanium layer has a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20cm-3; and

a second boron doped germanium layer on the second source or drain region, wherein the second germanide layer is on the second boron doped germanium layer, and wherein the second boron doped germanium layer has a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20cm-3.

4. (New) The integrated circuit structure of claim 3, wherein the first boron doped germanium layer is in the first opening of the dielectric layer, and wherein the second boron doped germanium layer is in the second opening of the dielectric layer.

5. (New) The integrated circuit structure of claim 3, wherein the first boron doped germanium layer is below first opening of the dielectric layer and extends beyond the first opening of the dielectric layer, and wherein the second boron doped germanium layer is below the second opening of the dielectric layer and extends beyond the first opening of the dielectric layer.

6. (New) The integrated circuit structure of claim 2, further comprising:

an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region.

7. (New) The integrated circuit structure of claim 2, further comprising:

a gate dielectric layer, wherein the gate electrode is on the gate dielectric layer, wherein the gate dielectric layer comprises a high-k dielectric material, and wherein the gate electrode comprises a metal layer.

8. (New) The integrated circuit structure of claim 2, wherein the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets.

9. (New) An integrated circuit structure, comprising:

a body comprising silicon;

a gate electrode over the body, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;

a first dielectric spacer along the first side of the gate electrode;

a first source or drain region in the body proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a second dielectric spacer along the second side of the gate electrode;

a second source or drain region in the body proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;

a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;

a first contact plug in the first opening and on the first germanide layer; and

a second contact plug in the second opening and on the second germanide layer.

10. (New) The integrated circuit structure of claim 9, further comprising:

a first boron doped germanium layer on the first source or drain region, wherein the first germanide layer is on the first boron doped germanium layer, and wherein the first boron doped germanium layer has a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20cm-3; and

a second boron doped germanium layer on the second source or drain region, wherein the second germanide layer is on the second boron doped germanium layer, and wherein the second boron doped germanium layer has a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20cm-3.

11. (New) The integrated circuit structure of claim 10, wherein the first boron doped germanium layer is in the first opening of the dielectric layer, and wherein the second boron doped germanium layer is in the second opening of the dielectric layer.

12. (New) The integrated circuit structure of claim 10, wherein the first boron doped germanium layer is below first opening of the dielectric layer and extends beyond the first opening of the dielectric layer, and wherein the second boron doped germanium layer is below the second opening of the dielectric layer and extends beyond the first opening of the dielectric layer.

13. (New) A computing device, comprising:

a board; and

a component coupled to the board, the component including an integrated circuit structure, comprising:

a fin comprising silicon;

a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;

a first dielectric spacer along the first side of the gate electrode;

a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a second dielectric spacer along the second side of the gate electrode;

a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric

spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;

a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;

a first contact plug in the first opening and on the first germanide layer; and

a second contact plug in the second opening and on the second germanide layer.

14. (New) The computing device of claim 13, further comprising:

a memory coupled to the board.

15. (New) The computing device of claim 13, further comprising:

a communication chip coupled to the board.

16. (New) The computing device of claim 13, further comprising:

a camera coupled to the board.

17. (New) The computing device of claim 13, further comprising:

a battery coupled to the board.

18. (New) The computing device of claim 13, further comprising:

an antenna coupled to the board.

19. (New) The computing device of claim 13, wherein the component is a packaged integrated circuit die.

20. (New) The computing device of claim 13, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

21. (New) The computing device of claim 13, wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/881,541

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/881,541	05/22/2020	2811	1720	P38507USC2-C1-C1 111548	20	3

CONFIRMATION NO. 8383

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

FILING RECEIPT

OC000000117408131

Date Mailed: 06/04/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Glenn A. GLASS, Portland, OR;
Anand S. MURTHY, Portland, OR;
Tahir GHANI, Portland, OR;

Applicant(s)

INTEL CORPORATION, Santa Clara, CA;

Assignment For Published Patent Application

INTEL CORPORATION, SANTA CLARA, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 16/416,445 05/20/2019
which is a CON of 15/339,308 10/31/2016 PAT 10297670
which is a CON of 14/673,143 03/30/2015 PAT 9484432
which is a CON of 13/990,224 05/29/2013 PAT 8994104
which is a 371 of PCT/US2011/054198 09/30/2011
which is a CIP of 12/975,278 12/21/2010 PAT 8901537

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 06/02/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/881,541**

Projected Publication Date: 09/10/2020

Non-Publication Request: No

Early Publication Request: No

Title

CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/881,541	05/22/2020	Glenn A. GLASS	P38507USC2-C1-C1 111548

CONFIRMATION NO. 8383

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

PUBLICATION NOTICE

OC000000119791813

Title:CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Publication No.US-2020-0287011-A1
Publication Date:09/10/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2826
	Examiner Name	ERDEM, FAZLI
Sheet 1 of 1	Attorney Docket No: P38507USC2-C1-C1 111548	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action for European Patent Application No. 19188924.5 (Attorney Docket No. P38507EP-D1) mailed July 14, 2020, 5 pgs.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	16/881,541
Filing Date	May 22, 2020
First Inventor	Glass, et al.
Art Unit	2826
Examiner Name	ERDEM, FAZLI
Attorney Docket No.	P38507USC2-C1 Conf No. 8383

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of the first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has bee n made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	10-14-2020
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli */Lisa Puccinelli/* *Date* 10-14-2020

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Electronic Acknowledgement Receipt	
EFS ID:	40847121
Application Number:	16881541
International Application Number:	
Confirmation Number:	8383
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38507USC2-C1-C1 111548
Receipt Date:	14-OCT-2020
Filing Date:	22-MAY-2020
Time Stamp:	19:44:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Other Reference-Patent/App/Search documents	P38507EP-D1_OA_07-14-20.pdf	248143 4520f85f6e5b58d48811fb5201f0ede755e11d81	no	5

Warnings:

Information:					
2		P38507USC2-C1-C1_IDS_10-14-20.pdf	493356 f69f1fb09085d5e7b8e94ba187e618764e48da28	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Information Disclosure Statement (IDS) Form (SB08)	2	2
	Transmittal Letter	1	1

Warnings:	
Information:	
Total Files Size (in bytes):	741499

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2826
	Examiner Name	ERDEM, FAZLI
Sheet 1 of 1	Attorney Docket No: P38507USC2-C1-C1 111548	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed October 23, 2020, 3 pgs	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	16/881,541
Filing Date	May 22, 2020
First Inventor	Glass, et al.
Art Unit	2826
Examiner Name	ERDEM, FAZLI
Attorney Docket No.	P38507USC2-C1 Conf No. 8383

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of the first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has bee n made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	01-22-2021
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli /Lisa Puccinelli/ Date 01-22-2021

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Electronic Acknowledgement Receipt	
EFS ID:	41721827
Application Number:	16881541
International Application Number:	
Confirmation Number:	8383
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38507USC2-C1-C1 111548
Receipt Date:	22-JAN-2021
Filing Date:	22-MAY-2020
Time Stamp:	18:35:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38507USC2-C1-C1_IDS_01-22-21.pdf	396705 5607b5916b159e90820c30c4d92c4212a2645e8e	yes	2

	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
	Transmittal Letter		1	1	
Warnings:					
Information:					
2	Other Reference-Patent/App/Search documents	CN_OA_10-23-20.pdf	97880 3cd87705ad443969e61ac667b729b6502a86cdee	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	494585		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16/881,541
Filing Date	May 22, 2020
First Named Inventor	Glenn A. GLASS
Title	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
Art Unit	2826
Examiner Name	Fazli ERDEM
Attorney Docket Number	97259.00223

SIGNATURE of Applicant or Patent Practitioner

Signature	/Lucius L. Lockwood/	Date (Optional)	
Name	Lucius L. Lockwood	Registration Number	53231
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Intel Corporation		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
16/881,541	May 22, 2020

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 35161

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Intel Corporation

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Lisa Hopkinson	Date (Optional)	3 June 2021
Name	Lisa Hopkinson		
Title	Administrator of Patents, Intel Corporation		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.151, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	42920580
Application Number:	16881541
International Application Number:	
Confirmation Number:	8383
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Customer Number:	31817
Filer:	Lucius Lavoisier Lockwood/Ariana Sanchez
Filer Authorized By:	Lucius Lavoisier Lockwood
Attorney Docket Number:	P38507USC2-C1-C1 111548
Receipt Date:	07-JUN-2021
Filing Date:	22-MAY-2020
Time Stamp:	18:56:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	541.pdf	1334814 2df63624ad4c7e58d29fca3bbfba6ffda08fc7e5	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	1334814

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/881,541	05/22/2020	Glenn A. GLASS	97259.00223

CONFIRMATION NO. 8383

35161
Dickinson Wright PLLC - Washington, DC
1825 EYE ST., NW
SUITE 900
WASHINGTON, DC 20006

POA ACCEPTANCE LETTER

OC000000126185078

Date Mailed: 06/10/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/07/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dtdinh/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

35161 7590 07/14/2021

DICKINSON WRIGHT PLLC - WASHINGTON, DC
1825 EYE ST., NW
SUITE 900
WASHINGTON, DC 20006

EXAMINER	
ERDEM, FAZLI	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/14/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/881,541	05/22/2020	Glenn A. GLASS	97259.00223	8383

TITLE OF INVENTION: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	10/14/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

35161 7590 07/14/2021
DICKINSON WRIGHT PLLC - WASHINGTON, DC
1825 EYE ST., NW
SUITE 900
WASHINGTON, DC 20006

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/881,541	05/22/2020	Glenn A. GLASS	97259.00223	8383

TITLE OF INVENTION: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	10/14/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
ERDEM, FAZLI	2826	257-190000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/881,541	05/22/2020	Glenn A. GLASS	97259.00223	8383

35161 7590 07/14/2021

DICKINSON WRIGHT PLLC - WASHINGTON, DC
1825 EYE ST., NW
SUITE 900
WASHINGTON, DC 20006

EXAMINER	
ERDEM, FAZLI	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 07/14/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/881,541	Applicant(s) GLASS et al.	
	Examiner FAZLI ERDEM	Art Unit 2826	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to Claims filed on 5/29/20.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 2-21 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 5/26/20, 10/14/20, 1/22/21.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

2. Claims 2-21 are allowed.

3. The following is an examiner's statement of reasons for allowance:

4. Regarding Claim 2, prior art failed to disclose or fairly suggest an integrated circuit structure comprising, along with other recited claim limitations,

5. a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium; a first contact plug in the first opening and on the first germanide layer; and a second contact plug in the second opening and on the second germanide layer. Claims 3-8 depend from claim 2 and hence are allowed for the same reason therein.

6. Regarding Claim 9, prior art failed to disclose or fairly suggest an integrated circuit structure comprising, along with other recited claim limitations,

7. a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium; a first contact plug in the first opening and on the first germanide layer; and a

second contact plug in the second opening and on the second germanide layer. Claims 10-12 depend from claim 9 and hence are allowed for the same reason therein.

8. Regarding Claim 13 prior art failed to disclose or fairly suggest an integrated circuit structure comprising, along with other recited claim limitations, a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium; a first contact plug in the first opening and on the first germanide layer; and a second contact plug in the second opening and on the second germanide layer. Claims 14-21 depend from claim 13 and hence are allowed for the same reason therein.

9.

10. Parent case of this case, which is patented under 10,700,178 is not qualified for a double patenting rejection because the claims for 10,700,178 fail to disclose opening or plug limitations. Furthermore, Yasutake 20070187767 can be considered a close prior art, however, this reference discloses that (see paragraphs 0024 and 0050), germanide layer does not contain silicon ("without containing Si").

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to FAZLI ERDEM whose telephone number is (571)272-1914. The examiner can normally be reached on M-F, 8am-5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826
7/3/2021

Notice of References Cited	Application/Control No. 16/881,541	Applicant(s)/Patent Under Reexamination GLASS et al.	
	Examiner FAZLI ERDEM	Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-10700178-B2	06-2020	Glass; Glenn A.	H01L21/76864	1/1
*	B	US-20070187767-A1	08-2007	Yasutake; Nobuaki	H01L29/7848	257/368
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/881,541	GLASS et al.
	Examiner	Art Unit
	FAZLI ERDEM	2826

CPC						
Symbol					Type	Version
H01L	/	29	/	45	F	2013-01-01
H01L	/	29	/	66795	I	2013-01-01
H01L	/	29	/	7848	I	2013-01-01
H01L	/	29	/	785	I	2013-01-01
H01L	/	29	/	66636	I	2013-01-01
H01L	/	29	/	7833	I	2013-01-01
H01L	/	29	/	0847	I	2013-01-01
H01L	/	29	/	165	I	2013-01-01
H01L	/	21	/	28525	I	2013-01-01
H01L	/	21	/	28518	I	2013-01-01
H01L	/	29	/	66545	I	2013-01-01
H01L	/	21	/	76805	I	2013-01-01
H01L	/	21	/	76843	I	2013-01-01
H01L	/	21	/	76864	I	2013-01-01
H01L	/	21	/	76895	I	2013-01-01
H01L	/	29	/	7851	I	2013-01-01

CPC Combination Sets							
Symbol					Type	Set	Ranking	Version
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/FAZLI ERDEM/ Primary Examiner, Art Unit 2826	03 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	2	5F

U.S. Patent and Trademark Office — Part of Paper No.: 20210703

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/881,541	GLASS et al.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L	/	21	/	28
H01L	/	29	/	45
H01L	/	29	/	66
H01L	/	29	/	78

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
257	190

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/FAZLI ERDEM/ Primary Examiner, Art Unit 2826 (Primary Examiner)	03 July 2021 (Date)	O.G. Print Claim(s) 2	O.G. Print Figure 5F

U.S. Patent and Trademark Office — Part of Paper No.: 20210703

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/881,541	GLASS et al.
	Examiner	Art Unit
	FAZLI ERDEM	2826

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	2	10	11	19	20										
2	3	11	12	20	21										
3	4	12	13												
4	5	13	14												
5	6	14	15												
6	7	15	16												
7	8	16	17												
8	9	17	18												
9	10	18	19												

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 20	
/FAZLI ERDEM/ Primary Examiner, Art Unit 2826 (Primary Examiner)	03 July 2021 (Date)	O.G. Print Claim(s) 2	O.G. Print Figure 5F

U.S. Patent and Trademark Office Part of Paper No.: 20210703

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/881,541	GLASS et al.
	Examiner	Art Unit
	FAZLI ERDEM	2826

CPC - Searched*		
Symbol	Date	Examiner
H01L21/28, 28518, 28525, 76, 76805, 76843, 76864, 76895	7/3/2021	FE
H01L29/45, 0847, 165, 66, 66545, 66636, 66795, 78, 7833, 7848, 785, 7851	7/3/2021	FE

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	190	7/3/2021	FE

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventors are searched	7/3/2021	FE
Assignee is searched	7/3/2021	FE
Searched 257/190 limited with text	7/3/2021	FE
Searched H01L21/28, 28518, 28525, 76, 76805, 76843, 76864, 76895 limited with text	7/3/2021	FE
Searched H01L29/0847, 45, 165, 66, 66545, 66636, 66795, 78,7833, 7848, 785, 7851	7/3/2021	FE
Interference search is conducted	7/3/2021	FE
EAST Search History is attached	7/3/2021	FE

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/881,541	GLASS et al.
	Examiner	Art Unit
	FAZLI ERDEM	2826

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
257	190	7/3/2021	FE
H01L21	28, 28518, 28525, 76, 76805, 76843, 76864, 76895	7/3/2021	FE
H01L29	0847, 45, 165, 66, 66545, 66636, 66795, 78, 7833, 7848, 785, 7851	7/3/2021	FE

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	4	"16881541"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:20
S2	1	"16881541" and germanide same titanium.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:20
S3	1	"16881541" and contact same germanide same titanium.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:21
S4	1	germanium same concentration same contact same germanide same titanium.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:22
S5	44	germanium same concentration same contact same germanide same titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:22
S6	27	germanium same concentration same contact same germanide near10 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:23

S7	1	germanium same concentration same contact same germanide near10 germanium near10 silicon near10 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:24
S8	102	germanide near10 germanium near10 silicon near10 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:24
S9	5	germanide near10 germanium near10 silicon near10 titanium.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:24
S10	3	second near2 germanide near10 germanium near10 silicon near10 titanium.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:28
S11	4	second near2 germanide near10 germanium near10 silicon near10 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:29
S12	5	second near2 germanide with (ge or germanium) with (si or silicon) with (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:30
S13	2	contact same plug same second near2 germanide with (ge or germanium) with (si or silicon) with (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:31

S14	8	contact same plug same germanide with (ge or germanium) with (si or silicon) with (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:31
S15	1	contact same concentration same germanide with (ge or germanium) with (si or silicon) with (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:56
S16	4	(ge or germanium) near2 concentration same germanide with (ge or germanium) with (si or silicon) with (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 11:57
S17	3	(ge or germanium) near2 concentration.clm. and germanide with (ge or germanium) with (si or silicon) with (ti or titanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 12:03
S18	29	(ge or germanium) near2 concentration.clm. and (germanium or germanide or ge) with (ge or germanium) with (si or silicon) with (ti or titanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 12:03
S19	11	(ge or germanium) near2 concentration.clm. and (germanium or germanide or ge) with (ge or germanium) with (si or silicon) with (ti or titanium).clm. and contact near plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 12:03
S20	20	(ge or germanium) near2 concentration.clm. and (germanium or germanide or ge) with (ge or germanium) with (si or silicon) with (ti or titanium) same contact near plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:47

S21	5	(ge or germanium) near2 concentration same (germanium or germanide or ge) same (ge or germanium) same (si or silicon) same (ti or titanium) same contact near plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:47
S22	28	(ge or germanium) near2 concentration same (germanium or germanide or ge) near10 (ti or titanium) same contact near plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:48
S23	7	(ge or germanium) near2 concentration.clm. and (germanium or germanide or ge) near10 (ti or titanium).clm. and contact near plug.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:49
S24	11	(ge or germanium) near2 concentration.clm. and (germanium or germanide or ge) near10 (ti or titanium) near10 (si or silicon) and contact near plug.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:50
S25	9	contact with (germanium or germanide or ge) near10 (ti or titanium) near10 (si or silicon) same plug.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:51
S26	114	contact with (germanium or germanide or ge) near10 (ti or titanium) near10 (si or silicon) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:52
S27	30	contact near10 (germanium or germanide or ge) near10 (ti or titanium) near10 (si or silicon) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:52

S28	4,346	germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:53
S29	223	germanide near titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:53
S30	59	germanide near titanium.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:53
S31	0	germanide near titanium same formula	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:54
S32	11	germanide near titanium and (germanium or ge) near5 concentration.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:54
S33	2	(source or drain or source/drain or s/d) same germanide near titanium and (germanium or ge) near5 concentration.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:55
S34	55	(source or drain or source/drain or s/d) same germanide same titanium and (germanium or ge) near5 concentration.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:56

S35	39	(source or drain or source/drain or s/d) same germanide same titanium same (si or silicon) and (germanium or ge) near5 concentration.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:56
S36	27	(source or drain or source/drain or s/d) same germanide same titanium same (si or silicon) and (germanium or ge) near5 concentration.clm. and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:59
S37	25	(source or drain or source/drain or s/d) same germanide same titanium same (si or silicon) and (germanium or ge) near5 concentration.clm. and (contact or source or drain or source/drain or s/d) same germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 14:59
S38	496	(gesi or sige) near10 germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 15:58
S39	5	(gesi or sige) near10 germanide and germanide near10 (ti or titanum)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 15:59
S40	104	(gesi or sige) near10 germanide and contact same (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 16:03
S41	10	(gesi or sige) near10 germanide and contact same (ti or titanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 16:04

S42	495	sige near10 germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:00
S43	20	sige near10 germanide near10 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:00
S44	14,324,504	sige near10 germanide near10 titanium samne (source or drain or source/drain or s/d)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:01
S45	14	sige near10 germanide near10 titanium same (source or drain or source/drain or s/d)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:02
S46	14	resistance same contact same (silicon near2 germanium or sige) near10 germanide near10 titanium same (source or drain or source/drain or s/d)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:03
S47	14	resistance same (silicon near2 germanium or sige) near10 germanide near10 titanium same (source or drain or source/drain or s/d)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:03
S48	54	resistance same (silicon near2 germanium or sige) same germanide same titanium same (source or drain or source/drain or s/d)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:04

S49	48	contact near2 resistance same (silicon near2 germanium or sige) same germanide same titanium same (source or drain or source/drain or s/d)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:04
S50	40	contact near2 resistance same (silicon near2 germanium or sige) same germanide same titanium same (source or drain or source/drain or s/d) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:05
S51	9	contact near2 resistance same (silicon near2 germanium or sige) same germanide same titanium same (source or drain or source/drain or s/d) same plug and (ti or titanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:06
S52	40	contact near2 resistance same (silicon near2 germanium or sige) same germanide same titanium same (source or drain or source/drain or s/d) same plug same (silicide or silicidation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:07
S53	53	(US-20190341464-$ or US-20200287011-$ or US-20130277752-$ or US-20150311204-$ or US-20160118384-$ or US-20200127091-$ or US-20100093147-$ or US-20190096885-$ or US-20200135476-$ or US-20100213538-$ or US-20150206942-$ or US-20120153387-$ or US-20130248999-$ or US-20070187767-$ or US-20100213532-$ or US-20100065886-$ or US-20070286952-$ or US-20130285155-$ or US-20200006229-$ or US-20170047419-$ or US-20160027781-$ or US-20160329431-$ or US-20130240989-$ or US-	US-PGPUB; USPAT; DERWENT	OR	ON	2021/06/30 17:08

		20130264639-$ or US-20150333180-$ or US-20160322359-$).did. or (US-20160372547-$ or US-20170373147-$ or US-20190259835-$ or US-20210005712-$).did. or (US-10700178-$ or US-9059024-$ or US-9224735-$ or US-9754940-$ or US-6093968-$ or US-8334561-$ or US-9484432-$ or US-10297670-$ or US-9153583-$ or US-9397102-$ or US-9705000-$ or US-8994104-$ or US-9117791-$ or US-9349810-$ or US-9437691-$ or US-9722023-$ or US-10090383-$ or US-10304927-$ or US-10553680-$ or US-10811496-$ or US-10879353-$).did. or (US-20200287011-$ or US-20080311710-$).did.				
S54	46	S53 and germanide same titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:08
S55	45	S53 and germanide same titanium same (silicide or silicidation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:08
S56	41	S53 and germanide same titanium same (silicide or silicidation) same (nickel or ni)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:09
S57	41	S53 and germanide same (ti or titanium) same (silicide or silicidation) same (nickel or ni)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:09
S58	41	S53 and germanide same (ti or titanium) same (silicide or	US-PGPUB; USPAT; USOCR;	OR	ON	2021/06/30 17:09

		silicidation) same (nickel or ni) same (sige or si or silicon)	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S59	74	contact near resistance same germanide same (ti or titanium) same (silicide or silicidation) same (nickel or ni) same (sige or si or silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:10
S60	69	contact near resistance same germanide same (ti or titanium) same (silicide or silicidation) same (nickel or ni) same (sige or si or silicon) and (ge or germanium) near10 concentration	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:10
S61	20	contact near resistance same germanide same (ti or titanium) same (silicide or silicidation) same (nickel or ni) same (sige or si or silicon) and (ge or germanium) near10 concentration and (ti or titanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:11
S62	5	contact near resistance same germanide same (ti or titanium) same (silicide or silicidation) same (nickel or ni) same (sige or si or silicon) and (ge or germanium) near10 concentration and (ti or titanium).clm. and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:11
S63	34	contact near resistance same germanide same (ti or titanium) same (silicide or silicidation) same (nickel or ni) same (sige or si or silicon) same (ge or germanium) near10 concentration same (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:12
S64	1	"12975178" and germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:14
S65	0	"7969784".pn. and germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2021/06/30 17:15

			JPO; DERWENT; IBM_TDB			
S66	2	"7969784".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:15
S67	9	"12975178"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:15
S68	430	"6373746"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:16
S69	4	"6373746".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:16
S70	1	"16881541" and (germanide near10 titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:19
S71	1	"16881541" and contact with (germanide near10 titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:20
S72	1	"16881541" and silicidation with contact with (germanide near10 titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/06/30 17:20

			DERWENT; IBM_TDB			
S73	23	silicidation with contact with (germanide near10 titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:21
S74	101	(silicide or silicidation) with contact with (germanide near10 titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:21
S75	39	resistance same (silicide or silicidation) with contact with (germanide near10 titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:22
S76	34	resistance same (silicide or silicidation) with contact with (germanide near10 titanium) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:23
S77	34	resistance same (silicide or silicidation) same contact same (germanide near10 titanium) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/30 17:23
S78	75	contact near resistance same germanide same titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 08:30
S79	56	contact near resistance same germanide same titanium same nickel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/07/01 08:31

			DERWENT; IBM_TDB			
S80	54	contact near resistance same germanide same titanium same nickel same aluminum	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 08:31
S81	12	13/990224	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 08:32
S82	32	contact near resistance and silicidation same germanide same titanium same nickel same aluminum	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 08:33
S83	73	contact near resistance and (silicide or silicidation) same germanide same titanium same nickel same aluminum	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 10:41
S84	54	contact near resistance same (silicide or silicidation) same germanide same titanium same nickel same aluminum	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 10:43
S85	1,106	(silicide or silicidation) near10 (ti or titanium) near10 (ge or germanium or germanide) near10 (si or silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 12:26
S86	30	(silicide or silicidation) near10 (ti or titanium) near10 (ge or germanium or germanide) near10 (si or silicon) same contact near resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/07/01 12:27

			DERWENT; IBM_TDB			
S87	15	(silicide or silicidation) near10 (ti or titanium) near10 (ge or germanium or germanide) near10 (si or silicon) same contact near resistance and tungsten with nickel with aluminum	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 12:37
S88	0	(silicide or silicidation) near10 (ti or titanium) near10 (ge or germanium or germanide) near10 (si or silicon) same contact near resistance and tungsten with nickel with aluminum with germanide with contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 12:37
S89	0	tungsten with nickel with aluminum with germanide with contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 12:37
S90	0	titanium with nickel with aluminum with germanide with contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 12:37
S91	36	titanium with nickel with aluminum with germanide same contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 12:38
S92	34	titanium with nickel with aluminum with germanide same (source or drain or source/drain or s/d) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 12:48
S93	34	(ti or titanium) same (ni or nickel) with (al or aluminum) with germanide same (source or drain or source/drain or s/d) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/07/01 12:49

			DERWENT; IBM_TDB			
S94	54	(ti or titanium) same (ni or nickel) same (al or aluminum) same germanide same (source or drain or source/drain or s/d) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 12:49
S95	28	(ti or titanium) same (ni or nickel) same (al or aluminum) same germanide same (source or drain or source/drain or s/d) same plug same (opening or trench)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 12:49
S96	27	(ti or titanium) same (ni or nickel) same (al or aluminum) same germanide same (source or drain or source/drain or s/d) same plug same (opening or trench) same contact near resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 12:50
S97	88	(ti or titanium) same (ni or nickel) same (al or aluminum) same (germanide or sige or ge or germanium) same (source or drain or source/drain or s/d) same plug same (opening or trench) same contact near resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 17:52
S98	98	(ti or titanium) same (ni or nickel) same (al or aluminum) same (germanide or sige or ge or germanium) same (source or drain or source/drain or s/d) same (opening or trench) same contact near resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 17:52
S99	83	(ti or titanium) same (ni or nickel) same (al or aluminum) same (germanide or sige or ge or germanium) same (source or drain or source/drain or s/d) same (opening or trench) same contact near resistance same adhesion	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 17:53
S100	95	(ti or titanium) same (ni or nickel) same (al or aluminum) same (germanide or sige or ge or germanium) same (source or drain or source/drain or s/d) same (opening or trench) same adhesion	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/07/01 18:06

			DERWENT; IBM_TDB			
S101	84	S100 and contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/01 18:06
S102	60	(US-20190341464-$ or US-20200287011-$ or US-20130277752-$ or US-20150311204-$ or US-20160118384-$ or US-20200127091-$ or US-20100093147-$ or US-20190096885-$ or US-20200135476-$ or US-20100213538-$ or US-20150206942-$ or US-20120153387-$ or US-20130248999-$ or US-20070187767-$ or US-20100213532-$ or US-20100065886-$ or US-20070286952-$ or US-20130285155-$ or US-20200006229-$ or US-20170047419-$ or US-20160027781-$ or US-20160329431-$ or US-20130240989-$ or US-20130264639-$ or US-20150333180-$ or US-20160322359-$).did. or (US-20160372547-$ or US-20170373147-$ or US-20190259835-$ or US-20210005712-$ or US-20200006330-$ or US-20210111246-$ or US-20140001520-$ or US-20160240534-$ or US-20200303373-$ or US-20180248011-$).did. or (US-10700178-$ or US-9059024-$ or US-9224735-$ or US-9754940-$ or US-6093968-$ or US-8334561-$ or US-9484432-$ or US-10297670-$ or US-9153583-$ or US-9397102-$ or US-9705000-$ or US-8994104-$ or US-9117791-$ or US-9349810-$	US-PGPUB; USPAT; DERWENT	OR	ON	2021/07/02 08:55

		or US-9437691-$ or US-9722023-$ or US-10090383-$ or US-10304927-$ or US-10553680-$ or US-10811496-$ or US-10879353-$ or US-7969784-$).did. or (US-20200287011-$ or US-20080311710-$).did.				
S103	6	S102 and (germanide with titanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 08:55
S104	50	S102 and (germanide with titanium) same (source or drain or source/drain or s/d)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 08:57
S105	25	S102 and (germanide with titanium) same (source or drain or source/drain or s/d) same (opening or trench)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 08:57
S106	25	S102 and (germanide with titanium) same (source or drain or source/drain or s/d) same (opening or trench) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 08:58
S107	32	S102 and (germanide same titanium) same (source or drain or source/drain or s/d) same (opening or trench) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 08:58
S108	3	S102 and (germanide same titanium same (silicon or si)) same (source or drain or source/drain or s/d) same (opening or trench) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 08:58

S109	23	S102 and (germanide same titanium same (silicon or si or sige)) same (source or drain or source/drain or s/d) same (opening or trench) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 08:58
S110	21	S102 and (germanide same titanium same (silicon or si or sige) same (silicide or silicidation)) same (source or drain or source/drain or s/d) same (opening or trench) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 08:59
S111	21	(germanide same titanium same (silicon or si or sige) same (silicide or silicidation)) same (source or drain or source/drain or s/d) same (opening or trench) same plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:00
S112	17	((ti or titanium) same (silicon or si or sige) same (silicide or silicidation)) same (source or drain or source/drain or s/d) same (opening or trench) same plug and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:00
S113	22	((ti or titanium) same (silicon or si or sige) same (silicide or silicidation)) same (source or drain or source/drain or s/d) same (opening or trench) and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:00
S114	125	finfet and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:01
S115	17	finfet and germanide.clm. and germanide near10 (ti or titanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:01

S116	15	S115 and contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:02
S117	124	finfet same (stack or stacking or stacked) same contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:03
S118	5	S117 and (germanide or ge or sige or germanium) near10 (ti or titanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:03
S119	27	S117 and (germanide or ge or sige or germanium) near10 (ti or titanium) same contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:04
S120	2	"20070187767"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:05
S121	2	S120 and germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:06
S122	1	S120 and germanide with (si or silicon or silicide or silicidation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:07

S123	0	S120 and germanide with (si or silicon or silicide or silicidation).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:08
S124	413	germanide with (si or silicon or silicide or silicidation).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:08
S125	104	germanide with (si or silicon or silicide or silicidation).clm. and germanide with (ti or titanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:08
S126	40	S125 and contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:08
S127	39	S126 and germanide same (ti or titanium) same (silicide or silicidation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:10
S128	35	S126 and germanide same (ti or titanium) same (silicide or silicidation).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:11
S129	3	S126 and (source or drain or source/drain or s/d) same germanide same (ti or titanium) same (silicide or silicidation).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:11

S130	23	S126 and (source or drain or source/drain or s/d) same germanide same (ti or titanium) same (silicide or silicidation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:11
S131	3	S126 and (source or drain or source/drain or s/d) same germanide same (ti or titanium) same (silicide or silicidation) same contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:12
S132	71	(source or drain or source/drain or s/d) same germanide same (ti or titanium) same (silicide or silicidation) same contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:12
S133	54	(source or drain or source/drain or s/d) same germanide same (ti or titanium) same (silicide or silicidation) same contact adj resistance same (opening or trench or plug or stack or stacking or stacked) near2 contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 09:13
S134	54	(source or drain or source/drain or s/d) same germanide same (ti or titanium) same (silicide or silicidation) same contact adj resistance same (opening or trench or plug or stack or stacking or stacked) near2 contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 11:02
S135	31	contact adj resistance same germanide same plug same (opening or trench) same (s/d or source or drain or source/drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 13:03
S136	23	contact near resistance same (source or drain or s/d or source/drain) same (ge or germanium or sige or germanide).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 16:00

S137	58	contact near resistance same (source or drain or s/d or source/drain) same (ge or germanium or sige or germanide) same contact near2 (stack or stacking or stacked)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/02 18:50

7/3/2021 2:39:50 PM
C:\Users\ferdem\Documents\EAST\Workspaces\16881541_case.wsp

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L14	0	"intel.as,aanm"	US-PGPUB; USPAT	OR	ON	2021/07/03 14:34
L15	70,118	intel.as,aanm.	US-PGPUB; USPAT	OR	ON	2021/07/03 14:34
L16	7,885	glass.in. or murthy.in. or ghani.in.	US-PGPUB; USPAT	OR	ON	2021/07/03 14:34
L17	1,602	257/190.ccls.	US-PGPUB; USPAT	OR	ON	2021/07/03 14:35
L18	84,003	H01L21/28.cpc. or H01L21/28518.cpc. or H01L21/28525.cpc. or H01L21/76.cpc. or H01L21/76805.cpc. or H01L21/76895.cpc.or H01L21/76843.cpc. or H01L21/76864.cpc. or H01L29/45.cpc. or H01L29/0847.cpc. or H01L29/165.cpc. or H01L29/66.cpc. or H01L29/66545.cpc. or H01L29/66636.cpc. or H01L29/66795.cpc. or H01L29/78.cpc. or H01L29/7833.cpc. or H01L29/7848.cpc. or H01L29/785.cpc. or H01L29/7851.cpc.	US-PGPUB; USPAT	OR	ON	2021/07/03 14:35
L19	159,776	l15 or l16 or l17 or l18	US-PGPUB; USPAT	OR	ON	2021/07/03 14:35
L20	259	l19 and (ge or germanium or sige) same (ti or titanium) same (silicide or silicidation or silicon) same (contact adj resistance)	US-PGPUB; USPAT	OR	ON	2021/07/03 14:36
L21	48	l19 and (fin or finfet) same (ge or germanium or sige) same (ti or titanium) same (silicide or silicidation or silicon) same (contact adj resistance)	US-PGPUB; USPAT	OR	ON	2021/07/03 14:36
L22	121	l19 and (fin or finfet) and (ge or germanium or sige) same (ti or titanium) same (silicide or silicidation or silicon) same (contact adj resistance) and (ge or germanium) near10 concentration	US-PGPUB; USPAT	OR	ON	2021/07/03 14:37
L23	95	l22 and (ti or titanium) with (nickel or ni) same (al or aluminum)	US-PGPUB; USPAT	OR	ON	2021/07/03 14:37

7/3/2021 2:39:18 PM
C:\Users\ferdem\Documents\EAST\Workspaces\16881541_case.wsp

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2826
	Examiner Name	ERDEM, FAZLI
Sheet 1 of 1	Attorney Docket No: P38507USC2-C1-C1 111548	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/F.E/		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed October 23, 2020, 3 pgs	

EXAMINER /FAZLI ERDEM/ DATE CONSIDERED 07/03/2021

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	223,271	intel.as,aanm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:24
L2	24,331	glass.in. or murthy.in. or ghani.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:24
L3	2,737	257/190.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:24
L4	200,494	H01L21/28.cpc. or H01L21/28518.cpc. or H01L21/28525.cpc. or H01L21/76.cpc. or H01L21/76805.cpc. or H01L21/76895.cpc.or H01L21/76843.cpc. or H01L21/76864.cpc. or H01L29/45.cpc. or H01L29/0847.cpc. or H01L29/165.cpc. or H01L29/66.cpc. or H01L29/66545.cpc. or H01L29/66636.cpc. or H01L29/66795.cpc. or H01L29/78.cpc. or H01L29/7833.cpc. or H01L29/7848.cpc. or H01L29/785.cpc. or H01L29/7851.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:27
L5	440,476	l1 or l2 or l3 or l4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:28
L6	1,466	l5 and (ge or germanium or sige or germanide) same contact adj	US-PGPUB; USPAT;	OR	ON	2021/07/03 14:28

		resistance same (source or drain or source/drain or s/d)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L7	432	l5 and (ge or germanium or sige or germanide) same contact adj resistance same (source or drain or source/drain or s/d) same (opening or trench or plug)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:28
L8	213	l7 and (ge or germanium or sige or germanide) with (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:29
L9	154	l8 and (ge or germanium) near10 concentration	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:31
L10	132	l9 and (fin or finfet)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:31
L11	126	l10 and (silicide or silicidation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:32
L12	108	l11 and (ti or titanium) same (nickel or ni) same (al or aluminum)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/03 14:32
L13	20	l12 and (ti or titanium).clm.	US-PGPUB; USPAT; USOCR;	OR	ON	2021/07/03 14:32

			FPRS; EPO; JPO; DERWENT; IBM_TDB			

7/3/2021 2:34:04 PM
C:\Users\ferdem\Documents\EAST\Workspaces\16881541_case.wsp

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2826
	Examiner Name	ERDEM, FAZLI
Sheet 1 of 1	Attorney Docket No: P38507USC2-C1-C1 111548	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/F.E/		Office Action for European Patent Application No. 19188924.5 (Attorney Docket No. P38507EP-D1) mailed July 14, 2020, 5 pgs.	

EXAMINER /FAZLI ERDEM/ DATE CONSIDERED 07/03/2021

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 8383

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
16/881,541	05/22/2020 RULE	257	2826	97259.00223

APPLICANTS
INTEL CORPORATION, Santa Clara, CA;

INVENTORS
Glenn A. GLASS, Portland, OR;
Anand S. MURTHY, Portland, OR;
Tahir GHANI, Portland, OR;

**** CONTINUING DATA ***************************
This application is a CON of 16/416,445 05/20/2019 PAT 10700178
which is a CON of 15/339,308 10/31/2016 PAT 10297670
which is a CON of 14/673,143 03/30/2015 PAT 9484432
which is a CON of 13/990,224 05/29/2013 PAT 8994104
which is a 371 of PCT/US2011/054198 09/30/2011
which is a CIP of 12/975,278 12/21/2010 PAT 8901537

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
06/02/2020

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /FAZLI ERDEM/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		OR	11	20	3

ADDRESS
DICKINSON WRIGHT PLLC - WASHINGTON, DC
1825 EYE ST., NW
SUITE 900
WASHINGTON, DC 20006
UNITED STATES

TITLE
CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1720	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2811
	Examiner Name	N/A
Sheet 1 of 3	Attorney Docket No: P38507USC2-C1-C1 111548	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-5,312,766	05-17-1994	Sheldon Aronowitz et al.	
		US-5,296,387	03-22-1994	Sheldon Aronowitz et al.	
		US-5,296,386	03-22-1994	Sheldon Aronowitz et al.	
		US-7,821,044	10-26-2010	Mark T. Bohr et al.	
		US-8,575,652	11-05-2013	Yoshiki Kamata	
		US-7,221,006	05-22-2007	Marius Orlowski et al.	
		US-7,732,285	06-08-2010	Intel Corporation	
		US-7,880,228	02-01-2011	Toshiba Corp.	
		US-7,683,362	03-23-2010	Fujitsu Ltd.	
		US-7,667,227	02-23-2010	Fujitsu Ltd.	
		US-6,607,948	08-2003	Suigiyama, Naoharu	
		US-9,349,810	05-2016	Glass, Glenn A.	
		US-20030057416	03-27-2003	Matthew Currie	
		US-20050130454	06-16-2005	Anand Murthy et al.	
		US-20050184354	08-25-2005	Chu et al.	
		US-20060156080	07-13-2006	John P. Tellkamp et al	
		US-20060237746	10-26-2006	Marius Orlowski et al.	
		US-20060255330	11-16-2006	Chen et al.	
		US-20070187767	08-16-2007	Yasutake, Nobuaki	
		US-20070238236	10-11-2007	Ted Cook Jr. et al.	
		US-20070275548	11-29-2007	Lavoie et al.	
		US-20080135878	06-12-2008	Kim et al.	
		US-20080179752	07-31-2008	Takashi Yamauchi et al.	
		US-20080197412	08-21-2008	Zhang et al.	
		US-20080242037	10-02-2008	Bernhard Sell et al.	
		US-20090224369	09-10-2009	Harold Samuel Gamble et al.	
		US-20100148217	06-17-2010	Danielle Simonelli	
		US-20110062498	03-17-2011	Frank Yang et al.	
		US-20110068407	03-24-2011	Chih Chieh Yeh et al.	
		US-20120007051	01-12-2012	Sarunya Bangsaruntip et al.	
		US-20120037998	02-16-2012	Bedell et al.	
		US-20130240989	09-19-2013	Glenn Glass et al.	
		US-20140070377	03-13-2014	Yu et al.	

EXAMINER /FAZLI ERDEM/ **DATE CONSIDERED** 07/03/2021

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.E/

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2811
	Examiner Name	N/A
Sheet 2 of 3	Attorney Docket No: P38507USC2-C1-C1 111548	

		US-20090206370	08-2009	Chu, Jack O.	
		US-20090302348	12-2009	Adam, Thomas N.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
		JP-2007-165665	06-28-2007	Renesas Tech Corp		
		WO 2010-068530	06-17-2010	Intel Corporation		
		JP-2007-214481	08-23-2007	Toshiba Corp		
		CN-101622690	01-06-2010	Intel Corporation		
		JPH-07-169958	07-04-1995	NEC Corp		
		JPH-05-183160	07-23-1993	Toshiba Corp		
		JP-2007-318132	12-06-2007	IBM		
		JP-2007-036205	02-08-2007	Fujitsu Ltd.		
		JP-2006-186240	07-13-2006	Fujitsu Ltd.		
		JP-2012-510720	05-10-2012	Intel Corporation		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		International Search Report and Written Opinion for International Patent Application No. PCT/US11/054198 (Attorney Docket No. P38507PCT) mailed April 19, 2012, 13 pgs.	
		International Preliminary Report Patentability for International Patent Application No. PCT/US11/054198 (Attorney Docket No. P38507PCT) mailed July 4, 2013, 9 pgs.	
		Office Action for Korean Patent Application No. 2013-7016072 (Attorney Docket No. P38507KR) mailed May 23, 2014, 4 pgs., with English translation	
		Notice of Allowance for Korean Patent Application No. 2013-7016072 (Attorney Docket No. P38507KR) mailed November 13, 2014, 3 pgs., with English translation.	
		Office Action for Japanese Patent Application No. 2013-546134 (Attorney Docket No. P38507JP) mailed August 26, 2014, 4 pgs. of English translation and 3 pgs. with no translation.	
		Notice of Allowance for Japanese Patent Application No. 2013-546134 (Attorney Docket No. P38507JP) mailed February 10, 2015, 3 pgs., no translation.	
		Extended European Search Report for European Patent Application No. 11852027.9 (Attorney Docket No. P38507EP) mailed August 11, 2014, 14 pgs.	
		"Metal/Semi conductor Ohmic Contacts Technology or Gate Length Series Resistance (ohms)", 1997, XP055127433, Retrieved from the Internet: URL:http://web.stanford.edu/class/ee311/N0 TES/Ohmic_Contacts.pdf [retrieved on 2014-07-08] the whole document	

EXAMINER /FAZLI ERDEM/ **DATE CONSIDERED** 07/03/2021

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.E/

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2811
	Examiner Name	N/A
Sheet 3 of 3	Attorney Docket No: P38507USC2-C1-C1 111548	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		Office Action for European Patent Application No. 11852027.9 (Attorney Docket No. P38507EP) mailed October 12, 2015, 4 pgs.	
		First Office Action for Chinese Patent Application No. 201180062116.2 (Attorney Docket No. P38507CN) mailed May 5, 2015, 6 pgs., no translation	
		Second Office Action for Chinese Patent Application No. 201180062116.2 (Attorney Docket No. P38507CN) mailed October 20, 2015, 3 pgs., no translation	
		Notice of Allowance for Chinese Patent Application No. 201180062116.2 (Attorney Docket No. P38507CN) mailed February 26, 2016, 4 pgs., with English translation	x
		First Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed May 4, 2018, 6 pgs., no translation	
		Second Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed December 3, 2018, 5 pgs., no translation	
		Third Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed April 10, 2019, 4 pgs., no translation	
		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed November 29, 2019, 6 pgs	
		Office Action for European Patent Application No. 11852027.9 (Attorney Docket No. P38507EP) mailed December 12, 2019, 2 pgs.	
		Search Report for European Patent Application No. 19188924.5 (Attorney Docket No. P38507EP-D1) mailed October 23, 2019, 2 pgs.	
		STANTON P. ASHBURN ET AL: FORMATION OF C54 TITANIUM GERMANOSILICIDE USING RAPID THERMAL PROCESSING AND APPLICATION TO RAISED, ULTRASHALLOW JUNCTIONS", MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, vol. 320, 1 January 1993, pages 311-316, XP055631293	
		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed March 24, 2020, 12 pgs.	
		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed April 24, 2020, 3 pgs.	

EXAMINER /FAZLI ERDEM/ **DATE CONSIDERED** 07/03/2021

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.E/

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16/881,541
Filing Date	2020-05-22
First Named Inventor	Glenn A. GLASS
Title	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
Art Unit	2826
Examiner Name	ERDEM, FAZLI
Attorney Docket Number	D480-012044

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ian D. MacKinnon/	Date (Optional)	2021-07-23
Name	Ian D. MacKinnon	Registration Number	34,660
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
16/881,541	2011-09-30

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 00164

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Intel Corporation

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Lisa Hopkinson	Date (Optional)	15 July 2021
Name	Lisa Hopkinson		
Title	Administrator of Patents		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.191, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	43326847
Application Number:	16881541
International Application Number:	
Confirmation Number:	8383
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Customer Number:	35161
Filer:	Ian David MacKinnon
Filer Authorized By:	
Attorney Docket Number:	97259.00223
Receipt Date:	23-JUL-2021
Filing Date:	22-MAY-2020
Time Stamp:	17:43:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	2021-07-23_POA_D480-012044.pdf	3542229 3b57af8ccc11e0b8cd8b611e2f452c5790a71b09	no	2

Warnings:

Information:	
Total Files Size (in bytes):	3542229

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/881,541	05/22/2020	Glenn A. GLASS	97259.00223

CONFIRMATION NO. 8383

35161
DICKINSON WRIGHT PLLC - WASHINGTON, DC
1825 EYE ST., NW
SUITE 900
WASHINGTON, DC 20006

POWER OF ATTORNEY NOTICE

OC000000127250559

Date Mailed: 07/28/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/23/2021.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rmohamed/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/881,541	05/22/2020	Glenn A. GLASS	D480-012044

CONFIRMATION NO. 8383

164
KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

POA ACCEPTANCE LETTER

OC000000127250574

Date Mailed: 07/28/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/23/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rmohamed/

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	16/881,541	Filing Date	2020-05-22	Docket Number (if applicable)	D480-012044	Art Unit	2826
First Named Inventor	Glenn A. Glass			Examiner Name	Fazli Erdem		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 110982

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Ian D. MacKinnon/	Date (YYYY-MM-DD)	2021-10-08
Name	Ian D. MacKinnon	Registration Number	34660

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Espacenet

Bibliographic data: CN101087002 (A) — 2007-12-12

Semiconductor structure with stressor channel and its forming method

Inventor(s): ZHIJIONG LUO [US]; NIVO ROVEDO [US] ± (LUO ZHIJIONG, ; ROVEDO NIVO)

Applicant(s): IBM [US] ± (IBM)

Classification: - international: ***H01L21/336; H01L21/822; H01L21/8234; H01L21/8238; H01L27/04; H01L27/088; H01L27/092; H01L29/78***
- cooperative: **H01L21/26513 (EP, US); H01L29/66636 (EP); H01L29/7848 (EP);** H01L21/823807 (EP); H01L21/823814 (EP); H01L29/1083 (EP); H01L29/165 (EP); H01L29/6656 (EP)

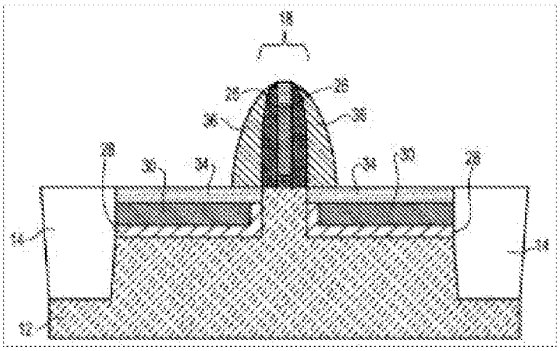
Application number: CN200710103297 20070515

Priority number (s): US20060423227 20060609

Also published as: CN100524826 (C) JP2007329477 (A) JP5220348 (B2) TW200807715 (A) US2008006818 (A1) more

Abstract not available for CN101087002 (A)
Abstract of corresponding document: US2008006818 (A1)

A multilayer embedded stressor having a graded dopant profile for use in a semiconductor structure for inducing strain on a device channel region is provided. The inventive multilayer stressor is formed within areas of a semiconductor structure in which source/drain regions are typically located. The inventive multilayer stressor includes a first conformal epi semiconductor layer that is undoped or lightly doped and a second epi semiconductor layer that is highly dopant relative to the first epi semiconductor layer. The first and second epi semiconductor layers each have the same lattice constant, which is different from that of the substrate they are embedded in. The structure including the inventive multilayer



embedded stressor achieves a good balance between stress proximity and short channel effects, and even eliminates or substantially reduces any possible defects that are typically generated during formation of the deep source/drain regions.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION CN101087002A

Semiconductor structure with stress device channel and its forming method

[0001]

Technical field

[0002]

The invention relates to a semiconductor device and a method of forming the same.

More specifically, the present invention relates to a complementary metal oxide semiconductor (CMOS) structure that includes a multi-layer embedded stressor (streesor) with a graded dopant distribution and at least one conformal first Epitaxy (epi) semiconductor.

[0003]

Background technique

[0004]

The mechanical stress inside the semiconductor device substrate is widely used to adjust device performance. For example, in general Si technology, the transistor channel is oriented along the {110} plane of silicon. In this arrangement, when the channel is subjected to compressive stress along the film direction and/or tensile stress along the direction perpendicular to the channel, the mobility of holes increases, and when the silicon film is subjected to compression stress along the film direction Under tensile stress and/or compressive stress along a direction perpendicular to the channel, the mobility of electrons increases. Therefore, compressive and/or tensile stress can be advantageously generated in the channel region of a p-channel field effect transistor (pFET) and/or an n-channel field effect transistor (nFET) to improve the performance of such a device.

[0005]

A possible method for generating the required stress in the silicon channel region is to form buried SiGe or SiC stressors (that is, stress wells) in the source and drain regions of the CMOS device, so that the source and drain regions Compressive or tensile stress is induced in the channel region between the drain regions.

Although the embedded stressor technology is now well known, it is extremely challenging to integrate the embedded stressor into the conventional CMOS process. The performance range of CMOS devices strongly depends on the stress generated by the embedded stressor itself, the active dopant concentration in the embedded stressor, and the proximity of the embedded stressor to the channel region of the device.

[0006]

A large amount of technical research and development devoted to this subject material shows the importance of overcoming the above-mentioned various defects in the embedded stressor technology.

Some recent developments in this technology can be found in the following documents, for example, U.S. Patent Nos. 6,921,913; 6,831,292; 6,844,227; 6,323,525; and 5,442,205, and U.S. Patent Application Publication Nos. 20050082522 and 2004026269 4A1.

[0007]

Although these advances have been made in the semiconductor industry, there is still a need to further improve the embedded stressor technology in order to obtain a good balance between the proximity of the stressor and the short channel effect.

Moreover, there is also a need for an embedded stressor technology that can eliminate possible defects. In the embedded stressor technology of the prior art, the defects are typically generated during ion implantation into the deep source/drain region.

[0008]

Summary of the invention

[0009]

In the present invention, a multilayer embedded stressor is provided, which has a graded dopant distribution and at least one conformal first epitaxial semiconductor layer.

The multilayer stressor of the present invention is formed in the region of the semiconductor structure where the active/drain regions are normally located.

The structure with the multi-layer embedded stressor of the present invention achieves a good balance between the proximity of the stressor and the short channel effect, and even eliminates or greatly reduces the usual use of deep implantation during the formation of deep source/drain regions. Any possible defects produced.

[0010]

According to the present invention, there is provided a semiconductor structure including the multilayer embedded stressor of the present invention, which includes:

[0011]

At least one field effect transistor located on one surface of the semiconductor substrate; and

[0012]

A multilayer embedded stressor having a graded dopant distribution and at least one first conformal epitaxial semiconductor layer, the epitaxial semiconductor layer being located on the footprint of the at least one field effect transistor and the semiconductor substrate In the recessed region of the wafer, the multilayer embedded stressor induces stress on the channel region of the at least one field effect transistor.

[0013]

In one embodiment of the present invention, the at least one field effect transistor (FET) is a pFET, and the multilayer embedded stressor includes SiGe.

In another embodiment of the present invention, the at least one field effect transistor is an nFET, and the multilayer embedded stressor includes Si:C.

In another embodiment of the present invention, the structure includes at least one pFET and at least one nFET, which are separated by an isolation region, wherein the multilayer embedded stressor related to the pFET includes SiGe, and the nFET-related multilayer embedded stressors include Si:C.

[0014]

As described above, the multilayer embedded stressor at least includes the first epitaxial semiconductor layer conformally arranged in the recessed area of the substrate.

The first epitaxial semiconductor layer may be undoped or lightly doped.

The multilayer embedded stressor of the present invention further includes a second epitaxial semiconductor layer located on top of the first epitaxial semiconductor layer.

The second epitaxial semiconductor layer is highly doped with respect to the dopant concentration of the first epitaxial semiconductor layer.

[0015]

In the embodiment of forming a pFET on a single crystal Si substrate, the multilayer embedded stressor includes a first epitaxial SiGe layer conformally arranged in the recessed area and a second epitaxial SiGe layer located on top of the first epitaxial SiGe layer.

According to the present invention, the first epitaxial SiGe layer is undoped or lightly doped.

The second epitaxial SiGe layer is highly doped relative to the first epitaxial SiGe layer.

[0016]

In the embodiment of forming an nFET on a single crystal Si substrate, the multilayer embedded stressor includes a first epitaxial Si:C layer conformally arranged in the recessed area and a second epitaxial Si:C layer on top of the first epitaxial Si:C layer. Epitaxial Si: C layer.

According to the present invention, the first epitaxial Si:C layer is undoped or lightly doped.

The second epitaxial Si:C layer is highly doped relative to the first epitaxial Si:C layer.

[0017]

According to the above structure, the present invention also provides a method of manufacturing the structure.

In general, the method of the present invention includes:

[0018]

At least one field effect transistor is provided, which has an extension spacer on one surface of a semiconductor substrate, and the semiconductor substrate has a recessed area on the occupying area of the at least one field effect transistor;

[0019]

Conformally grow a first epitaxial semiconductor layer on the exposed surface of the semiconductor substrate in the recessed area, and the lattice constant of the first epitaxial semiconductor layer is different from the lattice constant of the semiconductor substrate;

[0020]

A second epitaxial semiconductor layer is formed on the first epitaxial semiconductor layer, wherein the lattice constant of the second epitaxial semiconductor layer is the same as that of the first epitaxial semiconductor layer and is higher than the dopant concentration of the first epitaxial semiconductor layer ;with

[0021]

An expansion region is formed in the upper part of the first and second epitaxial semiconductor layers.

[0022]

Note that because the first epitaxial (epi) semiconductor layer is conformally formed with the recessed region, the multilayer embedded stressor thus formed (for example, a combination of the first and second epitaxial semiconductor layers) is similar to the one formed in the semiconductor substrate. The contours of the recessed areas are the same.

In some embodiments of the present invention, the multilayer embedded stressor has substantially no rounded corners.

[0023]

Description of the drawings

[0024]

FIG. 1 is a diagram (cross-sectional view) showing a structure in which a portion of a substrate located on a occupant region of a field effect transistor including a single narrow spacer is recessed.

[0025]

2 is a diagram (cross-sectional view) showing the structure of FIG. 1 after the first epitaxial semiconductor layer is conformally arranged, in which the lattice constant of the first epitaxial semiconductor layer and the lattice constant of the substrate in the recessed area of the substrate different.

[0026]

3 is a diagram (cross-sectional view) showing the structure of FIG. 2 after the second epitaxial semiconductor layer is arranged, in which the lattice constant of the second epitaxial semiconductor layer and the lattice constant of the first epitaxial semiconductor layer in the recessed area of the substrate same.

[0027]

4 is a diagram (cross-sectional view) showing the structure of FIG. 3 during the formation of source/drain extension regions in the upper portions of the first and second semiconductor layers.

[0028]

5 is a diagram (cross-sectional view) showing the structure of FIG. 4 after forming a second wider spacer next to the first narrow spacer.

[0029]

Detailed ways

[0030]

The present invention will now be described in more detail with reference to the additional discussion and drawings of the patent application in the following text. The present invention provides a structure that includes a multilayer embedded stressor adjacent to the device channel, and the present invention also provides manufacturing This structure method.

Note that the drawings are provided for illustrative purposes only, and therefore are not drawn to scale.

[0031]

In the following description, a large number of special details are proposed, such as special structures, components, materials, dimensions, processing steps and techniques, in order to gain a complete understanding of the present invention.

However, those of ordinary skill in the art should realize that the present invention can be implemented without these special details.

In other cases, well-known structures or process steps are not described in detail to avoid obscuring the description of the present invention.

[0032]

It should be understood that when an element, such as a layer, region or substrate, is referred to as being "on" or "above" another element, it can be directly on the other element, or there may also be isolation elements.

In contrast, when one element is referred to as being "directly on" or "directly on" or "directly on" another element, there is no isolation element.

It should also be understood that when an element is referred to as being "below" or "under" another element, it can be directly under the other element, or an isolation element may also be present.

In contrast, when it is mentioned that an element is "directly located" or "directly under" or "under" another element, there is no isolation element.

[0033]

As described above, a multilayer embedded stressor is provided in the semiconductor substrate, which has a graded dopant distribution and at least one first epitaxial semiconductor layer conformally arranged in a recessed area provided in the semiconductor substrate, For use in a semiconductor structure with at least one CMOS device.

The multilayer stressor of the present invention is formed in a semiconductor structure that typically has source/drain regions.

The structure containing the multilayer embedded stressor of the present invention achieves a good balance between stress proximity and short channel effect, and even eliminates or greatly reduces possible defects usually generated during the formation of deep source/drain regions .

In some embodiments of the present invention, the multilayer embedded stressor of the present invention does not substantially include rounded corners.

[0034]

Reference is first made to Fig. 1, which illustrates the initial structure 10 employed in the present invention.

As shown in the figure, the initial structure 10 includes a semiconductor substrate 12 in which at least one isolation region 14 is formed (a pair of isolation regions is specifically shown in the drawing).

The initial structure 10 also includes a recessed area 16 formed in a portion of the semiconductor substrate 12.

The recessed area 16 is located on the occupying area of at least one field effect transistor (FET) 18.

[0035]

Although FIG. 1 and the remaining drawings show a single FET, the present invention also considers forming a plurality of FETs on the same semiconductor substrate 12.

Multiple FETs can have the same conductivity (that is, all nFETs or all pFETs).

Optionally, multiple FETs may have different conductivity (that is, some are nFETs and some are pFETs).

When forming a plurality of different FETs, the same basic process steps as shown in FIGS. 1-5 are used, except that a block mask can be used to process one group of FETs while protecting another group of FETs.

[0036]

The at least one FET 18 includes a gate stack including a gate dielectric 20, a gate conductor 22 and a dielectric cap 24.

A first narrow spacer 26 is arranged on one sidewall of the gate stack.

The device channel 25 is located in the mesa portion of the substrate 12.

[0037]

The various components of the initial structure are made of traditional materials well known to those skilled in the art.

In addition, the manufacturing of the initial structure 10 until the formation of the first narrow spacer 26, but the formation of the recessed region 16 is not included, all use techniques well known to those skilled in the art.

[0038]

The semiconductor substrate 12 of the initial structure 10 used in the present invention includes any semiconductor material, including but not limited to: Si, Ge, SiGe, SiC, SiGeC, Ga, GaAs, InAs, InP and all other III/V or II/V Compound semiconductor.

The semiconductor substrate 12 may also include organic semiconductors or layered semiconductors, such as Si/SiGe, silicon on insulator (SOI), or SiGe on insulator (SGOI).

In some embodiments of the present invention, preferably, the semiconductor substrate 12 includes a Si-containing semiconductor material, that is, a silicon-containing semiconductor material.

The semiconductor substrate 12 may be doped, undoped, or contain doped and undoped regions therein.

According to the present invention, the semiconductor substrate 12 has a first lattice constant, which is different from that of the embedded multiple stressor formed subsequently.

[0039]

When SOI substrates are used, these substrates include top and bottom semiconductors, such as Si layers, which are at least partially separated by a buried insulating layer.

The buried insulating layer includes, for example, crystalline or amorphous oxide, nitride, or any combination thereof.

Preferably, the buried insulating layer is an oxide.

Typically, the buried insulating layer is formed in the initial stage of the layer transfer process or during ion implantation and annealing treatments, such as SIMOX (isolation by oxygen ion implantation).

[0040]

The substrate 12 may have a single crystal orientation, or alternatively, a mixed semiconductor substrate having surface regions with different crystal orientations may also be used.

Hybrid substrates allow FETs to be fabricated in specific crystal orientations, improving the performance of the specific FETs formed.

For example, a hybrid substrate allows the fabrication of a structure in which pFETs can be formed in the {110} crystal direction while nFETs can be formed in the {100} crystal direction.

When a hybrid substrate is used, it can have SOI-like properties, bulk-like properties, or a combination of SOI-like and bulk-like properties.

[0041]

The semiconductor substrate 12 may also include a first doped (n- or p-) region and a second doped (n- or p-) region.

For the sake of clarity, the doped regions are not specifically shown in the drawings of the present invention.

The first doped region and the second doped region may be the same, or they may have different conductivity and/or doping concentrations.

These doped regions are called "wells".

[0042]

Then, at least one isolation region 14 is typically formed in the semiconductor substrate 12.

The isolation region 14 may be a trench isolation region (as shown in the figure) or a field oxide isolation region.

The formation of the trench isolation region uses a conventional trench isolation process well known to those skilled in the art.

For example, photolithography, etching, and filling the trench with trench dielectric can be used when forming the trench isolation region.

Optionally, a liner may be formed in the trench before the trench filling, a densification step is performed after the trench filling, and a planarization process is performed after the trench filling.

The field oxide can be formed by a so-called partial silicon oxidation process.

Note that the at least one isolation region provides isolation between adjacent gate regions, which is usually required when adjacent gates have opposite conductivity.

Adjacent gate regions can have the same conductivity (that is, all n- or p-type), or alternatively, they can have different conductivity (that is, one is n-type and the other is p-type). -type).

[0043]

In this aspect of the present invention, a conventional CMOS process flow can be used when forming the FET 18, including deposition of various material layers of the gate stack, photolithography, and etching.

Alternatively, replacement gate processing can be used when forming the FET 18.

[0044]

As mentioned above, the FET 18 includes a gate stack containing a gate dielectric 20, a gate conductor 22, and a dielectric cap 24.

The gate dielectric 20 is arranged on one surface of the semiconductor substrate 12 and can be formed by a thermal growth process such as oxidation, nitridation or oxynitridation.

Alternatively, the gate dielectric 20 can be processed by deposition, such as chemical vapor deposition (CVD), plasma assisted CVD, metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), evaporation, reactive sputtering, chemical solution Deposition and other similar deposition processes are formed.

The gate dielectric 20 can also be formed by any combination of the above-mentioned processes.

[0045]

The gate dielectric 20 includes an insulating material having a dielectric constant of about 4.0 or more.

All dielectric constants mentioned in this article are compared with vacuum, unless specifically mentioned.

In one embodiment, the gate dielectric 20 includes a high-k material.

The term "high-k" refers to a dielectric with a dielectric constant greater than 4.0, preferably greater than 7.0.

Specifically, the gate dielectric 20 used in the present invention includes but is not limited to: oxide, nitride, oxynitride and/or silicide, including metal silicide and metal silicide nitride.

In one embodiment, preferably, the gate dielectric 20 includes an oxide, such as SiO_2, HfO_2, ZrO_2, Al_2O_3, TiO_2, La_2O_3, $SrTiO_3$, LaAlO3, Y_2O_3, Ga_2O_3, GdGaO, and mixtures thereof.

[0046]

The physical thickness of the gate dielectric 20 can vary, but typically, the thickness of the gate dielectric 20 is about 0.5 to about 10 nm, and a more typical thickness is about 0.5 to about 3 nm.

[0047]

Next, a gate conductor 22 is formed on the upper exposed surface of the gate dielectric 20.

The gate conductor 22 includes a conductive material, including, for example, polycrystalline Si, SiGe, metal, metal alloy, metal silicide, metal nitride, metal carbide, or a combination of multiple layers thereof.

When there are multiple layers, a diffusion barrier layer (not shown), such as TiN or TaN, may be provided between each conductor layer.

[0048]

The gate conductor 22 is formed by conventional deposition processes, including, for example, chemical vapor deposition, plasma-enhanced chemical vapor deposition, atomic layer deposition, sputtering, electroplating, evaporation, and any other similar deposition processes.

In one embodiment, where polycrystalline Si or SiGe is used as the gate electrode, an in-situ deposition process may be used, or alternatively, deposition may be performed after ion implantation.

At this time, in the present invention, the gate conductor 22 may be doped by ion implantation, thereby changing the work function of the gate electrode.

Examples of dopant ions that can be used include As, P, B, Sb, Bi, In, Al, Ga, Tl, or mixtures thereof.

The thickness of the gate conductor 22 is not important to the present invention.

However, the thickness of the gate conductor 22 is typically about 20 to about 250 nm.

[0049]

The gate stack of each FET 18 also includes a dielectric cap 24 on the surface of the gate conductor 22.

The dielectric cap 24 includes oxide, nitride, oxynitride, or any combination thereof, and is formed by conventional deposition processes, including, for example, CVD, PECVD, and evaporation.

The range in which the thickness of the dielectric cap 24 can vary is typically about 10 to about 100 nm.

[0050]

The first narrow spacer 26 formed before (in the replacement gate process flow) or after (in the conventional CMOS process flow) is formed before the gate stack is formed, and its constituent material is the same as or different from the dielectric material of the dielectric cap 24.

The first narrow spacer 26 is typically formed by deposition and etching, and the width along its bottommost surface is typically about 1 to about 50 nm.

The narrow spacer 26 may also be formed by oxidation treatment.

The first narrow spacer 26 may also be referred to as an extended spacer because it is usually present when the source/drain extension regions are formed.

[0051]

After the substrate 12 is processed, the FET 18 and the first narrow spacer 26 are formed, the first narrow spacer 26 and the dielectric cap 24 are used as an etching mask to form at least A recessed area 16.

The formation of the recessed region 16 may use an anisotropic etching process, such as reactive ion etching (RIE).

The recessed area 16 provided by the anisotropic etching process has an outer edge aligned with the outer edge of the isolation area 14 and another edge substantially aligned with the first narrow spacer 26.

The term "substantially aligned" means that the anisotropic etching process provides little or no undercut under the gate stack of the FET 18.

Anisotropic etching, which is a preferred technique for providing recessed regions 16 here, also helps to improve isolation by causing smaller trench isolation recesses.

In addition to anisotropic etching, the present invention also considers the use of an isotropic etching process, which typically provides a lateral undercut region (not shown) under each FET 18 gate stack.

[0052]

After the recessed area 16 is provided in the substrate 12 as shown in FIG. 1, a first epitaxial semiconductor layer 28 is formed in the recessed area 16, the lattice constant of which is different from the lattice constant of the semiconductor substrate 12 below.

Note that the first epitaxial semiconductor layer 28 and the second epitaxial semiconductor layer 30 (described in more detail below) together form the multilayer embedded stressor of the present invention.

For example, FIG. 2 shows the final structure including the first epitaxial semiconductor layer 28.

For the sake of clarity, the various components of the FET are not numbered in Figure 2 or the rest of the drawings.

[0053]

According to the present invention, the first epitaxial semiconductor layer 28 is undoped, lightly doped or a combination thereof.

"Lightly doped" means that the dopant concentration of the first epitaxial semiconductor layer 28 is about 1E18 atoms/cm3 or lower, and a more typical dopant concentration is about 1e14-1e18 atoms/cm3.

Depending on the type of device to be formed, the dopant in the first epitaxial semiconductor layer 28 may be an n-type or p-type dopant.

[0054]

When the semiconductor substrate 12 includes single crystal silicon, the first epitaxial semiconductor layer 28 includes dummy SiGe or SiC.

Because the lattice constant of the first epitaxial semiconductor layer 28 is different from that of the semiconductor substrate 12, tensile or compressive stress will be generated in the recessed area 15.

This stress region in turn applies stress to the channel region of the FET.

For example, SiGe is used to form a compressive stress buried stressor, which is used to generate compressive stress in the channel region of the pFET.

The channel region of the FET is the area of the substrate 12 under the gate stack of the FET 18.

Optionally, SiC can be used to form a tensile stress embedded stressor for generating tensile stress in the trench region of the nFET.

[0055]

According to the present invention, the first epitaxial semiconductor layer 28 is formed in the recessed region 16 using a conformal epitaxial growth process.

Utilizing a conformal epitaxial process ensures that the first epitaxial semiconductor layer 28 is conformal to the exposed surface of the semiconductor substrate 12 that defines the recessed region 16.

That is, the conformal epitaxial process provides the first epitaxial semiconductor layer 28 in the recessed region 16 that follows the contour of the recessed region 16.

[0056]

The thickness of the first epitaxial semiconductor layer 28 may be changed according to the precise conditions of the epitaxial growth process.

These conditions are well known to those skilled in the art, so this article will not describe the epitaxial growth conditions in more detail.

Typically, the thickness of the first epitaxial semiconductor layer 28 is about 1 to about 30 nm, and a more typical thickness is about 2 to about 15 nm.

[0057]

Next, as shown in FIG. 3, a second epitaxial semiconductor 30 is formed in the recessed region 16 on top of the first epitaxial semiconductor layer 28, for example, FIG. 3 provides this structure.

According to the present invention, the second epitaxial semiconductor layer 30 has the same lattice constant as the first epitaxial semiconductor layer 28 and typically includes the same semiconductor material as the first epitaxial semiconductor layer 28.

However, the difference between the second epitaxial semiconductor layer 30 and the first epitaxial semiconductor layer 28 is that the second epitaxial semiconductor layer is highly doped.

"Highly doped" means that the dopant concentration (p-type or n-type) is greater than 1E18 atoms/cm3, and a more typical dopant concentration is greater than 1e18 to about 1e22 atoms/cm3.

In an embodiment of the present invention, when a single crystal Si substrate is used, the second epitaxial semiconductor layer 30 includes dummy SiGe or Si:C.

[0058]

The second epitaxial semiconductor layer 30 is formed through a conventional epitaxial growth process, including the above-mentioned conformal process.

[0059]

FIG. 4 shows the structure during the ion implantation of the source/drain extension region, where the reference numeral 32 indicates the ions used in forming the source/drain extension region.

Note that the source/drain extension regions are formed into the upper portion of the second epitaxial semiconductor layer 30 and into the upper portion of the first epitaxial semiconductor layer 28 on the sidewall of the mesa portion of the semiconductor substrate 12.

The ion implantation of the source/drain extension regions is performed using standard conditions well known to those skilled in the art.

Typically, the provided source/drain extension has a shallow junction with a dopant concentration of 1e19-1e23 atoms/cm3.

After ion implantation, activation annealing can be performed to activate the implanted material, or the source/drain extension can be activated in a heat treatment that may be subsequently used.

[0060]

In some embodiments, haloimplant can be performed together with extended implantation.

In other embodiments of the present invention, halo implantation may be performed before recessing the semiconductor substrate.

Traditional halo injection conditions are used in the present invention.

[0061]

The structure shown in FIG. 5 includes source/drain extension regions 34 in the upper portions of the first and second epitaxial semiconductor layers.

FIG. 5 also shows the structure after the second wide spacer 36 adjacent to the first narrow spacer 26 is formed.

The second wide spacer 36 typically, but not always, includes an insulating material that is different from the first narrow spacer 26.

The width of the second wide spacer 36 when measured along the bottom surface adjacent to the second epitaxial semiconductor layer 30 is about 5 to about 100 nm.

[0062]

Because the second epitaxial semiconductor layer 30 is highly doped, it can avoid the traditional deep source/drain ion implantation, so it will not cause damage in the multi-embedded stressors (that is, the epitaxial semiconductor layers 28 and 30) .

However, in some embodiments, conventional deep source/drain ion implantation can also be performed.

[0063]

The above process provides a structure that includes a multilayer buried stressor (ie, epitaxial semiconductor layers 28 and 30) very close to the device channel and having a graded dopant distribution.

"Very close" means that the distance between the stressor of the present invention and the channel of the device is about 30 nm or less.

This distance is usually the width of the first narrow spacer 26.

In the prior art process, the embedded stressor is further away from the device channel, typically the width of the first and second spacers described above.

[0064]

Another advantage of this patent application is that the present invention has a hierarchical dopant distribution and a multilayer buried stressor with at least the first epitaxial semiconductor layer conformally arranged in the recessed area, which provides an improvement compared with the conventional structure. The threshold voltage roll-off (roll-off), and there is little or no short channel effect.

In the epitaxial treatment or subsequent heat treatment, due to the first undoped or lightly doped first epitaxial layer, much less dopant diffuses into the channel. At the same time, the entire stressor is very close to the channel, but it is significantly reduced The short channel effect is improved, and the high channel stress is maintained.

[0065]

Although the present invention is specifically shown and described with reference to its preferred embodiments, those skilled in the art should understand that the foregoing and other details can be made on the form and details without departing from the spirit and scope of the present invention. Change.

Therefore, it should be noted that the present invention is not limited to the precise form and details described and illustrated, and its scope is limited only by the appended claims.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS CN101087002A

1.

A semiconductor structure having a stress device channel, including:

At least one field effect transistor located on one surface of the semiconductor substrate; and

A multi-layer embedded stressor having a graded dopant distribution and at least a first conformal epitaxial semiconductor layer located on the occupying area of the at least one field effect transistor and located in the recessed area of the semiconductor substrate, wherein The multilayer embedded stressor induces stress on the channel region of the at least one field effect transistor.

2.

The semiconductor structure according to claim 1, wherein the lattice constant of the multilayer embedded stressor is different from that of the semiconductor substrate.

3.

The semiconductor structure according to claim 1, wherein said multi-layer embedded stressor further comprises a second epitaxial semiconductor layer on top of said first conformal epitaxial semiconductor layer.

4.

The semiconductor structure according to claim 1, wherein the first epitaxial semiconductor layer is undoped, or the dopant concentration is about 1E18 atoms/cm3 or less.

5.

The semiconductor structure according to claim 3, wherein the dopant concentration of the second epitaxial semiconductor layer is greater than 1E18 atoms/cm3.

6.

The semiconductor structure according to claim 1, wherein said semiconductor substrate is a single crystal Si substrate, and said multilayer embedded stressor includes SiGe.

7.

The semiconductor structure according to claim 1, wherein said semiconductor substrate is a single crystal Si substrate, and said multilayer embedded stressor includes Si:C.

8.

The semiconductor structure according to claim 1, wherein said at least one field-effect transistor includes a pFET and an nFET, said multi-layer embedded stressor related to said pFET is under compressive stress, and said multi-layer embedded stressor related to said nFET is under compressive stress. The stressor is under tensile stress.

9.

The semiconductor structure according to claim 8, wherein said compressively stressed multilayer embedded stressor comprises SiGe, and said tensile stressed multilayer embedded stressor comprises Si:C.

10.

The semiconductor structure according to claim 1, further comprising an expansion region in the upper portion of the multilayer embedded stressor.

11.

A type of semiconductor including:

At least one p-field effect transistor located on the surface of a single crystal Si substrate; and

Multi-layer buried SiGe stressor, which has a graded dopant distribution and at least a first conformal epitaxial semiconductor layer located on the occupying area of the at least one p-field effect transistor and located in the recessed area of the substrate , Wherein the multi-layer buried SiGe stressor induces compressive stress on the channel region of the at least one p-field effect transistor.

12.

A method of forming a semiconductor structure with a stress device channel includes:

Providing at least one field effect transistor, which has an extended spacer on one surface of a semiconductor substrate, and the semiconductor substrate has a recessed area on the occupying area of the at least one field effect transistor;

Conformally grow a first epitaxial semiconductor layer on the exposed surface of the semiconductor substrate in the recessed area, and the lattice constant of the first epitaxial semiconductor layer is different from the lattice constant of the semiconductor substrate;

A second epitaxial semiconductor layer is formed on the first epitaxial semiconductor layer, wherein the lattice constant of the second epitaxial semiconductor layer is the same as that of the first epitaxial semiconductor layer and is higher than the dopant concentration of the first epitaxial semiconductor layer ;with

An expansion region is formed in the upper part of the first and second epitaxial semiconductor layers.

13.

The method according to claim 12, wherein said recessed area is formed by anisotropic etching.

14.

The method according to claim 12, wherein said recessed area is formed by isotropic etching.

15.

The method according to claim 12, wherein said first epitaxial semiconductor layer is undoped, or a dopant concentration is about 1E18 atoms/cm3 or less.

16.

The method according to claim 12, wherein the dopant concentration of the second epitaxial semiconductor layer is greater than 1E18 atoms/cm3.

17.

The method according to claim 12, wherein said semiconductor substrate is a single crystal Si substrate, and said first and second epitaxial semiconductor layers form a multilayer embedded stressor including SiGe.

18.

The method according to claim 12, wherein said semiconductor substrate is a single crystal Si substrate, and said first and second epitaxial semiconductor layers form a multilayer embedded stressor including Si:C.

19.

The method according to claim 12, wherein said at least one field-effect transistor includes pFET and nFET, and said first and second epitaxial semiconductor layers related to said pFET are subjected to compressive stress, and said first epitaxial semiconductor layer related to said nFET The first and second epitaxial semiconductor layers are under tensile stress.

20.

The method according to claim 12, further comprising forming a second spacer adjacent to said extended spacer, said second spacer being formed after said step of forming said extended area.

[19] 中华人民共和国国家知识产权局

[12] 发明专利申请公布说明书

[21] 申请号 200710103297.4

[51] Int. Cl.
H01L 29/78 (2006.01)
H01L 27/04 (2006.01)
H01L 27/088 (2006.01)
H01L 27/092 (2006.01)
H01L 21/336 (2006.01)
H01L 21/822 (2006.01)

[43] 公开日 2007 年 12 月 12 日

[11] 公开号 CN 101087002A

[51] Int. Cl. (续)
H01L 21/8234 (2006.01)
H01L 21/8238 (2006.01)

[22] 申请日 2007.5.15

[21] 申请号 200710103297.4

[30] 优先权

[32] 2006. 6. 9 [33] US [31] 11/423,227

[71] 申请人 国际商业机器公司

地址 美国纽约

[72] 发明人 骆志炯 里基·阿默斯 尼沃·洛维多 亨利·K.·尤托莫

[74] 专利代理机构 中国国际贸易促进委员会专利商标事务所

代理人 秦 晨

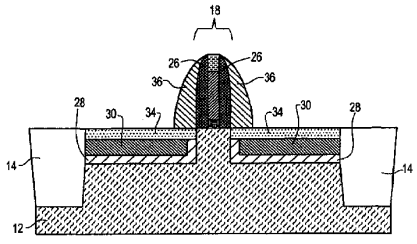
权利要求书 3 页 说明书 11 页 附图 3 页

[54] 发明名称

具有应力器件沟道的半导体结构及其形成方法

[57] 摘要

具有应力器件沟道的半导体结构及其形成方法。一种具有分级的掺杂剂分布的多层埋置应力器，其用于在半导体结构中对器件沟道区引发应力。本发明的多层埋置应力器在半导体结构的如下区域内形成，其中典型地定位有源极/漏极区。本发明的多层埋置应力器包括非掺杂或轻掺杂的第一共形外延半导体层，和相对于第一外延半导体层高掺杂的第二外延半导体层。第一和第二外延半导体层的每一个具有相同的点阵常数，其与埋置它们的基片的点阵常数不同。包含本发明多层埋置应力器的结构在应力接近度和短沟道效应之间获得了良好的平衡，甚至消除或大大减少了在形成深源极/漏极区期间通常会产生的任何可能的缺陷。



1. 一种半导体结构，其具有应力器件沟道，包括:

至少一个位于半导体基片的一个表面上的场效应晶体管；和

多层埋置应力器，其具有分级的掺杂剂分布和位于该至少一个场效应晶体管的占位区上，并处于所述半导体基片凹陷区内的至少第一共形外延半导体层，其中所述多层埋置应力器在所述至少一个场效应晶体管的沟道区上引发应力。

2. 根据权利要求 1 的半导体结构，其中所述多层埋置应力器的点阵常数与半导体基片不同。

3. 根据权利要求 1 的半导体结构，其中所述多层埋置应力器进一步包括位于所述第一共形外延半导体层的上面的第二外延半导体层。

4. 根据权利要求 1 的半导体结构，其中所述第一外延半导体层是非掺杂的，或者掺杂剂浓度为大约 1E18 原子/cm^3 或者更低。

5. 根据权利要求 3 的半导体结构，其中所述第二外延半导体层的掺杂剂浓度大于 1E18 原子/cm^3。

6. 根据权利要求 1 的半导体结构，其中所述半导体基片是单晶 Si 基片，且所述多层埋置应力器包括 SiGe。

7. 根据权利要求 1 的半导体结构，其中所述半导体基片是单晶 Si 基片，且所述多层埋置应力器包括 Si:C。

8. 根据权利要求 1 的半导体结构，其中所述至少一个场效应晶体管包括 pFET 和 nFET，与所述 pFET 相关的所述多层埋置应力器受压缩应力，与所述 nFET 相关的所述多层埋置应力器受拉伸应力。

9. 根据权利要求 8 的半导体结构，其中所述压缩应力多层埋置应力器包括 SiGe，且所述拉伸应力多层埋置应力器包括 Si:C。

10. 根据权利要求 1 的半导体结构，在多层埋置应力器的上部分内进一步包括扩展区。

11. 一种半导体，包括:

至少一个位于单晶 Si 基片的表面上的 p-场效应晶体管；和

多层埋置 SiGe 应力器，其具有分级的掺杂剂分布和位于该至少一个 p-场效应晶体管的占位区上并且处于所述基片的凹陷区内的至少第一共形外延半导体层，其中所述多层埋置 SiGe 应力器在所述至少一个 p-场效应晶体管的沟道区上引发压缩应力。

12. 一种形成具有应力器件沟道的半导体结构的方法，包括：

提供至少一个场效应晶体管，其在半导体基片的一个表面上有扩展间隔件，所述半导体基片在该至少一个场效应晶体管的占位区上有凹陷区；

在所述凹陷区内所述半导体基片的暴露表面上共形生长第一外延半导体层，所述第一外延半导体层的点阵常数与所述半导体基片的点阵常数不同；

在所述第一外延半导体层上形成第二外延半导体层，其中所述第二外延半导体的点阵常数与第一外延半导体层的相同，并且比第一外延半导体层的掺杂剂浓度更高；和

在所述第一和第二外延半导体层的上部内形成扩展区。

13. 根据权利要求 12 的方法，其中所述凹陷区是通过各向异性刻蚀形成的。

14. 根据权利要求 12 的方法，其中所述凹陷区是通过各项同性刻蚀形成的。

15. 根据权利要求 12 的方法，其中所述第一外延半导体层是非掺杂的，或者掺杂剂浓度为大约 1E18 原子/cm^3 或更小。

16. 根据权利要求 12 的方法，其中所述第二外延半导体层的掺杂剂浓度大于 1E18 原子/cm^3。

17. 根据权利要求 12 的方法，其中所述半导体基片是单晶 Si 基片，且所述第一和第二外延半导体层形成包括 SiGe 的多层埋置应力器。

18. 根据权利要求 12 的方法，其中所述半导体基片是单晶 Si 基片，且所述第一和第二外延半导体层形成包括 Si:C 的多层埋置应力

器。

19. 根据权利要求 12 的方法，其中所述至少一个场效应晶体管包括 pFET 和 nFET，且与所述 pFET 有关的所述第一和第二外延半导体层受压缩应力，与所述 nFET 有关的所述第一和第二外延半导体层受拉伸应力。

20. 根据权利要求 12 的方法，进一步包括形成临近所述扩展间隔件的第二间隔件，所述第二间隔件在形成所述扩展区的所述步骤之后形成。

具有应力器件沟道的半导体结构及其形成方法

技术领域

本发明涉及一种半导体器件及其形成方法。更明确地讲，本发明涉及一种互补金属氧化物半导体（CMOS）结构，其包括多层埋置应力器(streesor)，具有分级的(graded)掺杂剂分布和至少一个共形的第一外延(epi)半导体。

背景技术

半导体器件基片内部的机械应力被广泛地用于调节器件性能。例如，在通用 Si 技术中，晶体管沟道沿着硅的{110}面取向。在这种布置中，当沟道受到沿着膜方向的压缩应力和/或沿着与沟道垂直方向的拉伸应力时，空穴的迁移率提高，而当硅膜受到沿着膜方向的拉伸应力和/或沿着与沟道垂直方向的压缩应力时，电子的迁移率提高。因此，能够在 p 沟道场效应晶体管(pFET)和/或 n 沟道场效应晶体管(nFET)的沟道区内有利地产生压缩和/或拉伸应力，以提高这种器件的性能。

一种可能的用于产生所需应力硅沟道区的方法是在 CMOS 器件的源极和漏极区形成埋置的 SiGe 或 Si:C 应力器(也就是应力阱)，从而在源极和漏极区之间的沟道区内引发压或拉伸应力。尽管现在埋置应力器技术是众所周知的，但是将埋置的应力器集成进常规 CMOS 的工艺流程是极具挑战性的。CMOS 器件的性能范围强烈地取决于埋置应力器自身所产生的应力、埋置应力器中的活性掺杂剂浓度和埋置应力器与器件沟道区的接近度。

大量致力于这一主题材料的技术研发表明了克服埋置应力器技术中上述各种缺陷的重要性。该技术中的一些最新进展在如下的文献中能够发现，例如，美国专利 No.6,921,913; 6,831,292; 6,844,227; 6,323,525;和 5,442,205，以及美国专利申请公布 No.20050082522 和

20040262694 A1。

尽管在半导体工业中已经取得了这些进展，但是仍然需要进一步提高埋置应力器技术，以便在应力器接近度与短沟道效应之间获得良好的平衡。而且，还需要有一种能够消除可能的缺陷产生的埋置应力器技术，在现有技术的埋置应力器技术中，缺陷典型地在离子注入深源极/漏极区期间产生。

发明内容

在本发明中，提供了一种多层埋置应力器，其具有分级的掺杂剂分布和至少一个共形的第一外延半导体层。本发明的多层应力器在通常定位有源极/漏极区的半导体结构区域内形成。该具有本发明多层埋置应力器的结构在应力器接近度与短沟道效应之间获得了良好的平衡，甚至消除或者大大减少了通常在使用深注入形成深源极/漏极区期间产生的任何可能的缺陷。

根据本发明，提供了一种包含本发明多层埋置应力器的半导体结构，其包括:

至少一个场效应晶体管，其位于半导体基片的一个表面上；和

多层埋置应力器，其具有分级的掺杂剂分布和至少一个第一共形外延半导体层，该外延半导体层位于该至少一个场效应晶体管的占位区(footprint)上和所述半导体基片的凹陷区内，其中所述多层埋置应力器在所述至少一个场效应晶体管的沟道区上引发应力。

在本发明的一个实施例中，该至少一个场效应晶体管（FET）是pFET，该多层埋置应力器包括 SiGe。在本发明的另一个实施例中，该至少一个场效应晶体管是 nFET，该多层埋置应力器包括 Si:C。在本发明的另外一个实施例中，该结构包括至少一个 pFET 和至少一个 nFET，它们由隔离区分离，其中与所述 pFET 相关的所述多层埋置应力器包括 SiGe，而该与所述 nFET 相关的多层埋置应力器包括 Si:C。

如上所述，该多层埋置应力器至少包括共形布置于基片凹陷区内的第一外延半导体层。第一外延半导体层可以是非掺杂或轻掺杂的。

本发明的多层埋置应力器还包括第二外延半导体层，其位于第一外延半导体层的顶上。该第二外延半导体层相对于第一外延半导体层的掺杂剂浓度是高掺杂的。

在单晶 Si 基片上形成 pFET 的实施例中，该多层埋置应力器包括共形布置于凹陷区内的第一外延 SiGe 层和位于第一外延 SiGe 层顶上的第二外延 SiGe 层。根据本发明，第一外延 SiGe 层是非掺杂或轻掺杂的。而第二外延 SiGe 层相对于第一外延 SiGe 层是高掺杂的。

在单晶 Si 基片上形成 nFET 的实施例中，该多层埋置应力器包括共形布置于凹陷区内的第一外延 Si:C 层和位于第一外延 Si:C 层顶上的第二外延 Si:C 层。根据本发明，第一外延 Si:C 层是非掺杂或轻掺杂的。而第二外延 Si:C 层相对于第一外延 Si:C 层是高掺杂的。

根据上述的结构，本发明还提供一种制造该结构的方法。大体上，本发明的方法包括:

提供至少一个场效应晶体管，其在半导体基片的一个表面上有扩展间隔件(extension spacer)，所述半导体基片在该至少一个场效应晶体管的占位区上有凹陷区;

在所述凹陷区内所述半导体基片的暴露表面上共形生长第一外延半导体层，所述第一外延半导体层的点阵常数与所述半导体基片的点阵常数不同;

在所述第一外延半导体层上形成第二外延半导体层，其中所述第二外延半导体的点阵常数与第一外延半导体层的相同，并且比第一外延半导体层的掺杂剂浓度更高；和

在所述第一和第二外延半导体层的上部内形成扩展区。

注意，因为第一外延(epi)半导体层与凹陷区共形地形成，因此如此形成的多层埋置应力器（例如第一和第二外延半导体层的组合）与形成于半导体基片内的凹陷区的轮廓相同。在本发明的一些实施例中，多层埋置应力器基本上没有圆角。

附图说明

图 1 是显示一种结构的图示（剖面图），其中基片在位于包含单窄间隔件的场效应晶体管的占位区上的部分是凹陷的。

图 2 是显示图 1 的结构在共形布置了第一外延半导体层之后的图示（剖面图），其中该第一外延半导体层的点阵常数与基片凹陷区域内基片的点阵常数不同。

图 3 是显示图 2 的结构在布置了第二外延半导体层之后的图示（剖面图），其中第二外延半导体层的点阵常数与基片凹陷区内第一外延半导体层的点阵常数相同。

图 4 是显示图 3 的结构在第一和第二半导体层上部分内形成源极/漏极扩展区期间的图示（剖面图）。

图 5 是显示图 4 的结构在形成紧邻第一窄间隔件的第二较宽间隔件之后的图示（剖面图）。

具体实施方式

现在将参考下文本专利申请附加的讨论和附图对本发明进行更详细的说明，本发明提供了一种结构，其包括紧邻器件沟道的多层埋置应力器，并且本发明还提供了制造这种结构的方法。注意，附图只是出于例证的目的提供的，因此并没有按照比例加以绘制。

在下文的说明中，提出了大量特殊的细节，例如特殊的结构、部件、材料、尺寸、处理步骤和技巧，以便获得对本发明的完全理解。然而，本领域的普通技术人员应当意识到，本发明可以在没有这些特殊细节的情况下实现。在其他情况下，没有对众所周知的结构或工艺步骤进行详细的说明，以避免模糊本发明的描述。

应当理解，当提到一个元件，例如一个层、区域或基片，位于另一个元件的“上面”或“上方”时，它可以直接位于另一个元件上，或者也可以存在隔离元件。对比地，当提到一个元件“直接位于”或“直接处于”另一个元件的“上面”或“上方”时，则不存在隔离元件。还应当理解，当提到一个元件位于另一个元件的“下面”或“下方”时，它可以直接位于另一个元件下面，或者也可以存在隔离元件。对比地，当提到一个

元件“直接位于”或“直接处于”另一个元件的“下面”或“下方”时，则不存在隔离元件。

如上所述，在半导体基片内提供了多层埋置应力器，其具有分级的掺杂剂分布和共形布置在提供于半导体基片中的凹陷区内的至少一个第一外延半导体层，用于在具有至少一个 CMOS 器件的半导体结构内使用。本发明的多层应力器形成于半导体结构中典型地具有源极/漏极区的区域内。含有本发明多层埋置应力器的结构在应力接近度和短沟道效应之间实现了良好的平衡，甚至消除或大大减少了通常在形成深源极/漏极区期间产生的可能的缺陷。在本发明的一些实施例中，本发明的多层埋置应力器基本上不包含圆角。

首先参考图 1，其图解了本发明采用的初始结构 10。如图所示，初始结构 10 包括半导体基片 12，其中形成有至少一个隔离区 14（在附图中具体显示了一对隔离区）。初始结构 10 还包括凹陷区 16，其形成于半导体基片 12 的一部分内。该凹陷区 16 位于至少一个场效应晶体管（FET）18 的占位区上。

尽管图 1 和其余的附图都显示了单一的 FET，但是本发明也考虑在同一个半导体基片 12 上形成多个 FET。多个 FET 可以具有相同的导电性（也就是全为 nFET 或全为 pFET）。选择地，多个 FET 可以具有不同的导电性（也就是，一些为 nFET 而一些为 pFET）。当形成不同的多个 FET 时，采用与图 1-5 所示相同的基本工艺步骤，只是可以使用阻挡掩模处理一组的 FET，而保护另一组的 FET。

该至少一个 FET 18 包括栅极堆叠，其包括栅极电介质 20、栅极导体 22 和电介质帽 24。在栅极堆叠的一个侧壁上布置第一窄间隔件 26。器件沟道 25 位于基片 12 的台面部分中。

初始结构的各个部件都用本领域技术人员熟知的传统材料构成。另外，初始结构 10 的制造，直到第一窄间隔件 26 的形成，但不包括凹陷区 16 的形成，都是利用本领域技术人员所熟知的技术。

本发明所采用的初始结构 10 的半导体基片 12 包括任何半导体材料，包括但不仅限于：Si、Ge、SiGe、SiC、SiGeC、Ga、GaAs、InAs、

InP 和所有其它 III/V 或 II/V 化合物半导体。半导体基片 12 也可以包括有机半导体或分层半导体，例如 Si/SiGe、绝缘体上硅（SOI）或绝缘体上 SiGe（SGOI）。在本发明的一些实施例中，优选地，半导体基片 12 包括含 Si 半导体材料，也就是，含有硅的半导体材料。半导体基片 12 可以是掺杂的、非掺杂的或者其中含有掺杂和非掺杂区。根据本发明，半导体基片 12 具有第一点阵常数，其与随后形成的埋置多应力器的不同。

当采用 SOI 基片时，这些基片包括顶和底半导体，例如 Si 层，它们通过埋置的绝缘层至少部分分离。该埋置的绝缘层包括，例如，晶体或非晶体氧化物、氮化物或其任意组合。优选地，埋置绝缘层是一种氧化物。典型地，埋置绝缘层在层转移处理的初始阶段或在离子注入和退火处理，例如 SIMOX（通过氧离子注入隔离）期间加以形成。

基片 12 可以具有单晶体取向，或者选择地，还可以采用具有不同晶体取向的表面区的混合半导体基片。混合基片允许在特定的晶体取向制造 FET，提高所形成的特定 FET 的性能。例如，混合基片允许制造一种结构，其中能够在{110}晶向上形成 pFET，同时在{100}晶向上形成 nFET。当使用混合基片时，它可以具有类似 SOI 的性质、类似块体(bulk-like)的性质或者类似 SOI 和类似块体性质的组合。

半导体基片 12 还可以包括第一掺杂（n-或 p-）区和第二掺杂（n-或 p-）区。为清楚起见，在本发明的附图中没有具体显示掺杂区。第一掺杂区和第二掺杂区可以是相同的，或者它们可以具有不同的导电性和/或掺杂浓度。这些掺杂区被称作“阱”。

然后，典型地在半导体基片 12 内形成至少一个隔离区 14。隔离区 14 可以是沟槽隔离区（如图所示）或场氧化物隔离区。沟槽隔离区的形成是利用本领域技术人员所熟知的传统沟槽隔离工艺。例如，可以在形成沟槽隔离区时使用光刻、刻蚀并用沟槽电介质填充沟槽。任选地，在沟槽填充之前可以在沟槽内形成内衬，在沟槽填充之后执行致密化(densification)步骤，以及在沟槽填充之后进行平面化处理。场

氧化物的形成可以采用所谓的局部硅氧化处理。注意，该至少一个隔离区在相邻栅极区之间提供了隔离，通常在相邻栅极具有相反导电性时需要如此。相邻栅极区可以具有相同的导电性（也就是，全为 n-或 p-型），或者选择地，它们能够具有不同的导电性（也就是，一个为 n-型，另一个为 p-型）。

在本发明的这个方面，在形成 FET 18 时可以使用传统的 CMOS 工艺流程，包括沉积栅极堆叠的各种材料层、光刻和刻蚀。选择地，在形成 FET 18 时可以使用置换栅极处理。

如上所述，FET 18 包括含有栅极电介质 20 的栅极堆叠、栅极导体 22 和电介质帽 24。栅极电介质 20 布置在半导体基片 12 的一个表面上，能够通过热生长处理，例如氧化、氮化或氧氮化而加以形成。选择地，栅极电介质 20 能够通过沉积处理，例如化学气相沉积（CVD）、等离子体辅助 CVD、金属有机化学气相沉积（MOCVD）、原子层沉积（ALD）、蒸镀、反应溅射、化学溶液沉积和其它类似的沉积处理，加以形成。栅极电介质 20 还可以用上述处理的任意组合加以形成。

栅极电介质 20 包括介电常数为大约 4.0 或更大的绝缘材料。本文所提及的所有介电常数都是与真空相比，除非特殊提及。在一个实施例中，栅极电介质 20 包括高 k 材料。术语“高 k”是指介电常数大于 4.0，优选地大于 7.0 的电介质。明确地讲，本发明采用的栅极电介质 20 包括但不仅限于：氧化物、氮化物、氧氮化物和/或硅化物，包括金属硅化物和氮化金属硅化物。在一个实施例中，优选地，栅极电介质 20 包括氧化物，例如 SiO_2、HfO_2、ZrO_2、Al_2O_3、TiO_2、La_2O_3、$SrTiO_3$、$LaAlO_3$、Y_2O_3、Ga_2O_3、GdGaO 及它们的混合物。

栅极电介质 20 的物理厚度可以改变，但典型地，栅极电介质 20 的厚度为大约 0.5-大约 10nm，更典型的厚度为大约 0.5-大约 3nm。

接着，在栅极电介质 20 的上暴露表面上形成栅极导体 22。栅极导体 22 包括导电材料，包括例如多晶 Si、SiGe、金属、金属合金、金属硅化物、金属氮化物、金属碳化物或含有其多层的组合。当存在多层时，可以在每个导体层之间设置扩散阻挡层（未显示），例如 TiN

或 TaN。

栅极导体 22 的形成是利用传统的沉积处理，包括例如，化学气相沉积、等离子体增强化学气相沉积、原子层沉积、溅射、电镀、蒸镀和任何其它类似的沉积处理。在一个实施例中，其中使用多晶 Si 或 SiGe 作为栅极电极，可以使用原位沉积处理，或者选择地，在离子注入之后进行沉积。此时，在本发明中，栅极导体 22 可以通过离子注入进行掺杂，从而改变栅极电极的功函数。能够使用的掺杂剂离子的实例包括 As、P、B、Sb、Bi、In、Al、Ga、Tl 或其混合物。栅极导体 22 的厚度对于本发明而言并不重要。然而典型地，栅极导体 22 的厚度为大约 20-大约 250nm。

每个 FET 18 的栅极堆叠还包括位于栅极导体 22 表面上的电介质帽 24。该电介质帽 24 包括氧化物、氮化物、氧氮化物或其任意组合，利用传统的沉积处理加以形成，包括例如 CVD、PECVD 和蒸镀。电介质帽 24 的厚度可以变化的范围典型地为大约 10-大约 100nm。

在形成栅极堆叠之前（在置换栅极处理流程中）或之后（在传统的 CMOS 处理流程中）形成的第一窄间隔件 26，其构成材料与电介质帽 24 的电介质材料相同或不同。该第一窄间隔件 26 典型地通过沉积和刻蚀加以形成，并且在沿着其最底表面的宽度典型地为大约 1-大约 50nm。窄间隔件 26 也可以通过氧化处理加以形成。第一窄间隔件 26 还可被称作扩展间隔件，因为它通常存在于形成源极/漏极扩展区的时候。

在处理基片 12、形成 FET 18 和第一窄间隔件 26 之后，利用第一窄间隔件 26 和电介质帽 24 作为刻蚀掩模在每个 FET 18 占位区上的基片 12 内形成至少一个凹陷区 16。凹陷区 16 的形成可以使用各向异性刻蚀处理，例如反应离子刻蚀（RIE）。各向异性刻蚀处理提供的凹陷区 16，其具有一个与隔离区 14 的外边缘对准的外边缘，和另一个与第一窄间隔件 26 基本上对准的边缘。术语“基本上对准”是指，各向异性刻蚀处理在 FET 18 的栅极堆叠下面提供很小或者不提供底切。作为在此提供凹陷区 16 优选技术的各向异性刻蚀还由于造成较小

的沟槽隔离凹陷而有助于提高隔离。除了各向异性刻蚀之外，本发明还考虑利用各向同性刻蚀处理，其典型地在每个 FET 18 栅极堆叠的下面提供横向底切区（未显示）。

在如图 1 所示地在基片 12 内提供了凹陷区 16 之后，在凹陷区 16 内形成第一外延半导体层 28，其点阵常数与下面的半导体基片 12 点阵常数不同。注意，第一外延半导体层 28 与第二外延半导体层 30（在下文有更详细的说明）一起形成本发明的多层埋置应力器。例如图 2 显示了包含该第一外延半导体层 28 的最终结构。为了清晰起见，FET 的各个元件在图 2 或其余附图中没有标定数字。

根据本发明，第一外延半导体层 28 是非掺杂、轻掺杂或其组合。“轻掺杂”是指第一外延半导体层 28 的掺杂剂浓度为大约 1E18 原子/cm^3 或者更低，更典型的掺杂剂浓度为大约 1e14-1e18 原子/cm^3。根据待形成器件的类型，第一外延半导体层 28 内的掺杂剂可以是 n-型或 p-型掺杂剂。

当半导体基片 12 包括单晶硅时，第一外延半导体层 28 包括假 SiGe 或 Si:C。因为第一外延半导体层 28 的点阵常数与半导体基片 12 的不同，因此在凹陷区 15 内会产生拉伸或压缩应力。该应力区进而将应力施加给 FET 的沟道区。例如，使用 SiGe 形成压缩应力埋置应力器，用于在 pFET 的沟道区内产生压缩应力。FET 的沟道区是基片 12 位于 FET 18 栅极堆叠下面的区域。选择地，能够使用 Si:C 形成拉伸应力埋置应力器，用于在 nFET 的沟槽区域内产生拉伸应力。

根据本发明，第一外延半导体层 28 利用共形外延生长处理在凹陷区 16 内形成。利用共形外延处理确保第一外延半导体层 28 与限定凹陷区 16 的半导体基片 12 的暴露表面共形。也就是说，共形外延处理在凹陷区 16 内提供了遵循凹陷区 16 的轮廓的第一外延半导体层 28。

第一外延半导体层 28 的厚度可以根据外延生长处理的精确条件而改变。这些条件对于本领域的技术人员而言是众所周知的，因此本文不再对外延生长条件进行更详细的说明。典型地，第一外延半导体

层 28 的厚度为大约 1-大约 30nm，更典型的厚度为大约 2-大约 15nm。

接着，如图 3 所示，在第一外延半导体层 28 顶上的凹陷区 16 内形成第二外延半导体 30，例如图 3 提供了该结构。根据本发明，第二外延半导体层 30 具有与第一外延半导体层 28 相同的点阵常数，并且典型地包括与第一外延半导体层 28 相同的半导体材料。然而，第二外延半导体层 30 与第一外延半导体层 28 的不同之处在于，第二外延半导体层是高掺杂的。“高掺杂”是指，掺杂剂浓度（p-型或 n-型）大于 1E18 原子/cm^3，更典型的掺杂剂浓度为大于 1e18-大约 1e22 原子/cm^3。在本发明的一个实施例中，当使用单晶 Si 基片时，第二外延半导体层 30 包括假 SiGe 或 Si:C。

第二外延半导体层 30 通过传统的外延生长处理，包括上面提到的共形处理，加以形成。

图 4 显示了在源极/漏极扩展区的离子注入期间的结构，其中指代数字 32 表示在形成源极/漏极扩展区时使用的离子。注意，源极/漏极扩展区形成到第二外延半导体层 30 的上部分之中以及位于半导体基片 12 台面部分侧壁上的第一外延半导体层 28 的上部分之中。源极/漏极扩展区的离子注入的执行利用的是本领域技术人员熟知的标准条件。典型地，所提供的源极/漏极扩展具有一个浅结，掺杂剂浓度为 1e19-1e23 原子/cm^3。在离子注入之后可以进行活性退火以活化注入的物质，或者可以在随后可能采用的热处理中对源极/漏极扩展进行活化。

在一些实施例中，可以和扩展注入一起执行晕轮注入(halo implant)。在本发明的另一些实施例中，晕轮注入可以在使半导体基片凹陷之前执行。本发明中使用传统的晕轮注入条件。

图 5 显示的结构包括位于第一和第二外延半导体层上部分内的源极/漏极扩展区 34。图 5 还显示了在形成了邻接第一窄间隔件 26 的第二宽间隔件 36 之后的结构。第二宽间隔件 36 典型地但不必总是包括与第一窄间隔件 26 不同的绝缘材料。第二宽间隔件 36 的宽度在沿着其邻近第二外延半导体层 30 的底表面加以测量时，是大约 5-大约

100nm。

因为第二外延半导体层 30 是高掺杂的，所以能够避免传统的深源极/漏极离子注入，因此在多埋置应力器（也就是，外延半导体层 28 和 30）内不会引发损伤。然而在一些实施例中，也可以执行传统的深源极/漏极离子注入。

上述的处理提供了一种结构，其包括非常临近器件沟道并具有分级的掺杂剂分布的多层埋置应力器（也就是，外延半导体层 28 和 30）。“非常临近”是指，本发明的应力器与器件沟道的距离为大约 30nm 或者更小。这个距离通常是第一窄间隔件 26 的宽度。在现有技术处理中，埋置应力器离器件沟道更远，典型地为上述第一和第二间隔件的宽度。

本专利申请的另一个优点在于，本发明具有分级的掺杂剂分布和共形布置在凹陷区内的至少第一外延半导体层的多层埋置应力器，与传统结构相比，提供了改善的阈值电压滚降(roll-off)，并且很少或没有短沟道效应。在外延处理或随后的热处理中，由于第一非掺杂或轻掺杂第一外延层，扩散进入沟道的掺杂剂要少得多，同时整个应力器与沟道非常临近，但显著降低了短沟道效应，并保持了高沟道应力。

尽管本发明是通过参考其优选的实施例加以具体显示和说明的，但是本领域的技术人员应当理解，在不背离本发明精神和范围的前提下，可以对形式和细节进行前述的和其他的改变。因此应当注意，本发明并不仅限于所描述和说明的精确形式和细节，其范围只由附加权利要求限定。

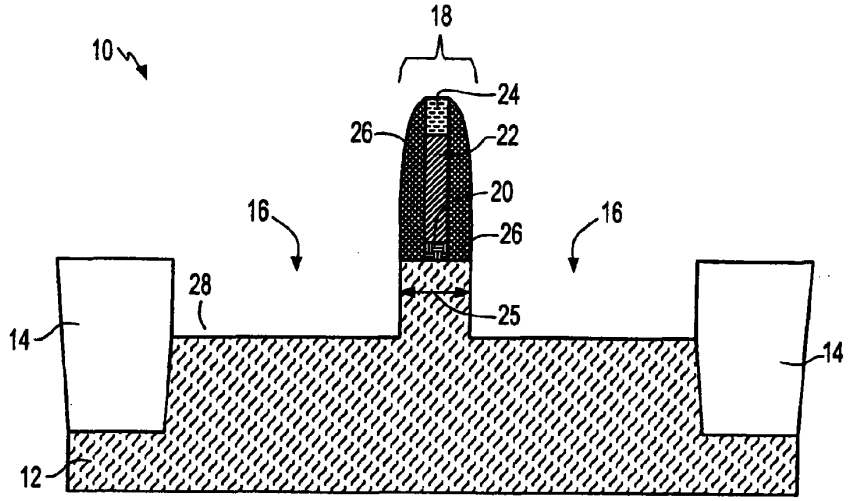


图 1

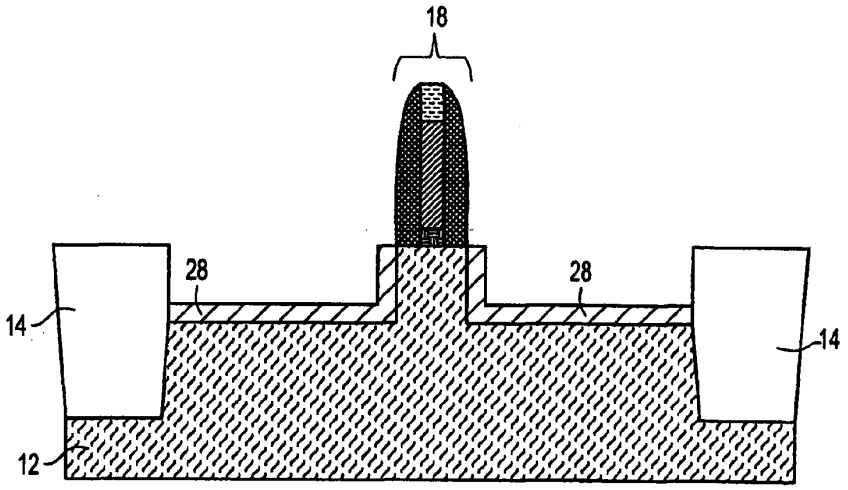


图 2

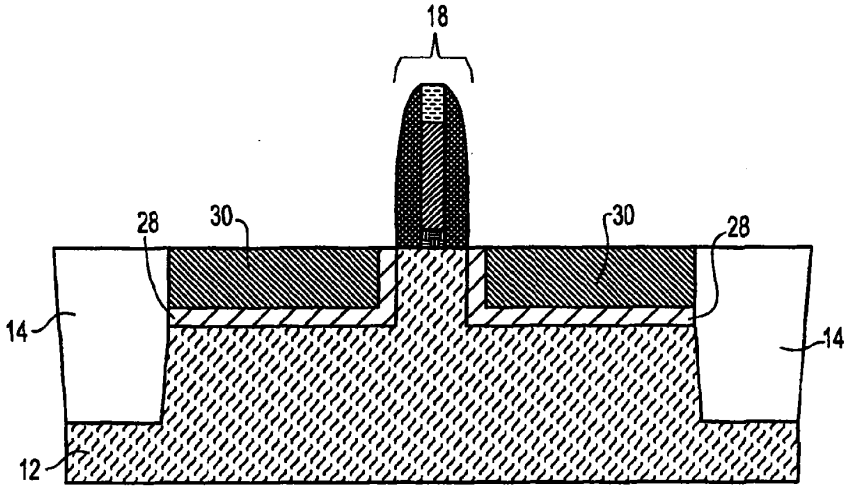


图 3

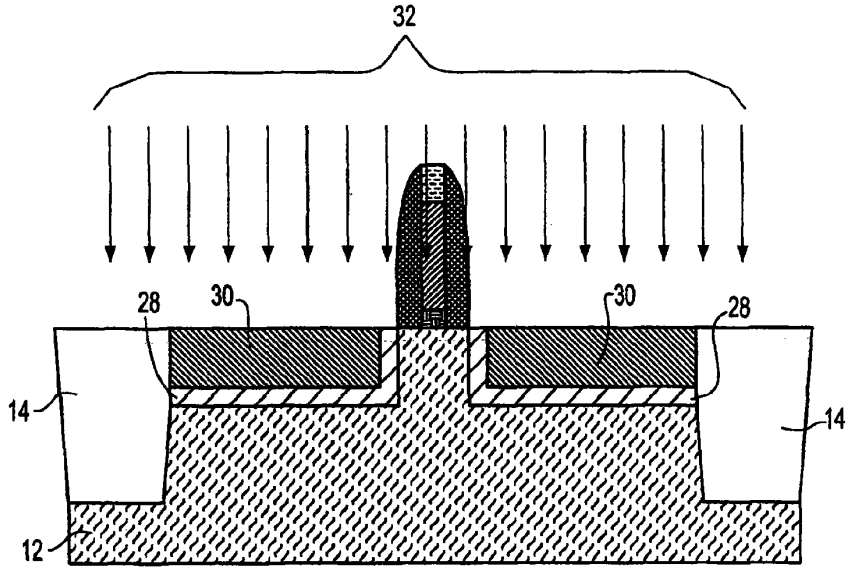


图 4

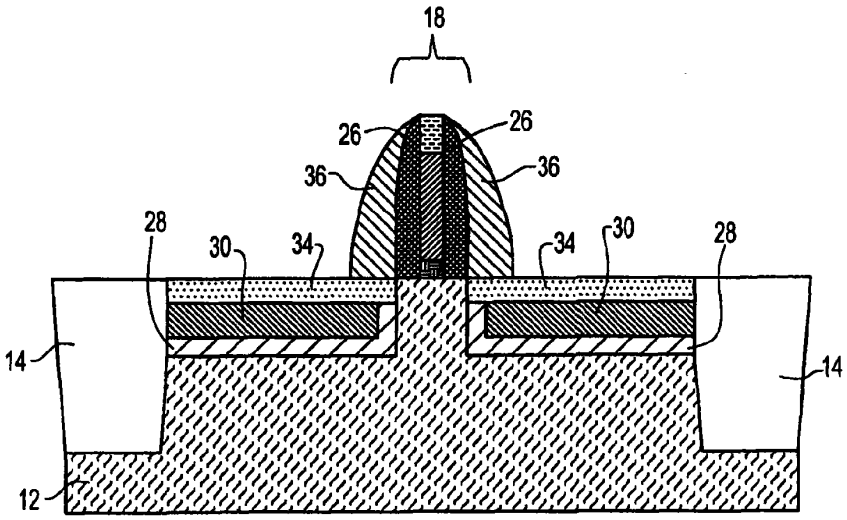


图 5

Espacenet

Bibliographic data: CN101140948 (A) — 2008-03-12

Semiconductor device and method of fabrication

Inventor(s):

Applicant(s): TAIWAN SEMICONDUCTOR MFG [CN] ± (TAIWAN SEMICONDUCTOR MFG)

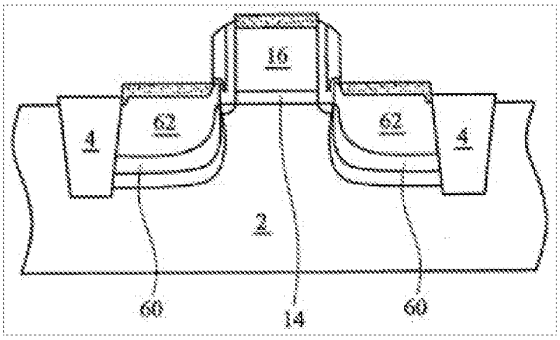
Classification: **- international:** ***H01L21/336; H01L29/78***
- cooperative: **H01L29/6653 (EP)**; **H01L29/66628 (EP)**; **H01L29/7848 (EP)**; H01L29/665 (EP); H01L29/66636 (EP)

Application number: CN200610173276 20061231

Priority number (s): US20060516265 20060906

Also published as: CN100539188 (C) TW200814317 (A) TWI323944 (B) US2008054347 (A1) US7605407 (B2)

Abstract not available for CN101140948 (A)
Abstract of corresponding document: US2008054347 (A1)



A semiconductor device includes a semiconductor substrate, a gate stack on the semiconductor substrate, and a stressor adjacent the gate stack and having at least a portion in the semiconductor substrate, wherein the stressor comprises an element for adjusting a lattice constant of the stressor. The stressor includes a lower portion and a higher portion on the lower portion, wherein the element in the lower portion has a first atomic percentage, and the element in the higher portion has a second atomic percentage substantially greater than the first atomic percentage.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION CN101140948A

Semiconductor device and its forming method

[0001]

Technical field

[0002]

The present invention relates to integrated circuits, and particularly to the structure of a MOS device with a stress source and a method of forming the same.

[0003]

Background technique

[0004]

In recent years, the semiconductor industry has been committed to reducing the size of semiconductor devices, reducing costs, and improving the speed, performance and density of semiconductor devices.

Changing the length of the channel region between the source and the drain can change the resistance of the channel region, thereby affecting the performance of the transistor. In particular, shortening the length of the channel region can reduce the distance from the source to the drain, and if other parameters remain unchanged, the current between the source and the drain can be increased.

[0005]

In order to further improve the performance of the MOS device, a stress can be applied to the channel region to increase the rate of movement of carriers.

Generally speaking, a tensile stress can be applied to the channel region of an NMOS device, and a compressive stress can be applied to the channel region of a PMOS device.

[0006]

Usually SiGe is epitaxially grown in the source/drain regions to apply a compressive stress to the channel region, including forming a stacked gate on the semiconductor substrate, and forming spacers on the sidewalls of the stacked gate along the The gate spacers form grooves in the silicon substrate, and SiGe stress sources are epitaxially grown in the grooves and tempered.

Because the lattice constant of SiGe is greater than that of silicon, after the tempering process, SiGe will expand and apply a compressive stress to the channel region, which is located between the source SiGe stress source and the drain SiGe stress source. Similarly, SiC stressors can be formed in the channel region of the NMOS device. Because the lattice constant of SiC is smaller than that of silicon, SiC will shrink and apply a tensile stress to the channel region.

[0007]

However, the traditional stress source forming method will cause leakage current in the MOS device.

The stress source needs to have high germanium or high carbon concentration, but high germanium or high carbon concentration will produce many defects, such as leakage current and reduced breakdown voltage. Therefore, in order to provide a better stress source, the industry urgently needs to improve the formation method of the stress source.

[0008]

Summary of the invention

[0009]

In an embodiment of the present invention, a semiconductor device is provided, including a semiconductor substrate; a stacked gate disposed on the semiconductor substrate; a stressor adjacent to the stacked gate, and at least a portion It is arranged in the semiconductor substrate, wherein the stressor contains an element, which can be used to adjust the lattice constant of the stressor.

The stressor includes a lower part and a higher part, wherein the element occupies a first atomic proportion in the lower part and a second atomic proportion in the higher part, and the second atomic proportion is substantially larger than the first atom Proportion.

[0010]

In another embodiment of the present invention, a semiconductor device is provided, including a semiconductor substrate, such as silicon; a stacked gate located on the semiconductor substrate; a stressor adjacent to the stacked gate, And at least a part is provided in the semiconductor substrate, wherein the stressor includes silicon and an element, and the element is selected from the group consisting of germanium and carbon, and the element occupies a first atomic ratio; and an intermediate region , Between the semiconductor substrate and the stressor, where the intermediate region contains silicon and the element, and where the element occupies a second atomic ratio, the second atomic ratio is smaller than the first atomic ratio.

[0011]

According to the semiconductor device, the first atomic ratio is between about 10% and 25%, and the second atomic ratio is between about 25% and 50%.

[0012]

According to the semiconductor device, the difference between the second atomic ratio and the first atomic ratio is greater than about 5%.

[0013]

According to the semiconductor device, the higher portion extends below the bottom of the channel region of the semiconductor device.

[0014]

According to the semiconductor device, the junction of the lower part and the higher part is substantially outside the depletion region of each source/drain junction.

[0015]

According to the semiconductor device, the thickness of the lower portion is less than 1/3 of the stressor.

[0016]

According to the semiconductor device, wherein the element includes germanium, and the semiconductor device includes a PMOS device.

[0017]

According to the semiconductor device, wherein the element includes carbon, and the semiconductor device includes an NMOS device.

[0018]

According to the semiconductor device, in the lower part, the concentration of the element increases from a part close to the semiconductor device to a higher part close to the stress source.

[0019]

In another embodiment of the present invention, a method for forming a semiconductor device is provided, including: providing a semiconductor substrate; forming a stacked gate on the semiconductor substrate; Forming a gate spacer; forming a groove in the semiconductor substrate adjacent to the gate spacer; and forming a stressor, and at least a part of it is in the groove, wherein the stressor contains an element, which can be used To adjust the lattice constant of the stressor.

The step of forming a stressor includes: forming a lower part in the groove, wherein the element occupies a first atomic ratio in the lower part; and forming a higher part on the lower part, wherein the element is in the higher part. The part occupies the second atomic ratio, and the second atomic ratio is substantially greater than the first atomic ratio.

[0020]

According to the method of forming a semiconductor device, wherein the step of forming a stress source includes epitaxial growth.

[0021]

According to the method of forming a semiconductor device, wherein the step of forming the higher portion includes gradually changing the flow rate of the precursor, and the precursor contains the element.

[0022]

According to the method of forming a semiconductor device, wherein the first atomic ratio is between about 10% and 25%, and wherein the second atomic ratio is between about 25% and 50%.

[0023]

According to the method of forming a semiconductor device, wherein the element includes germanium, and wherein the method further includes doping a p-type impurity to the source/drain region of a semiconductor device.

[0024]

According to the method of forming a semiconductor device, wherein the element includes carbon, and wherein the method further includes doping an n-type impurity to the source/drain region of a semiconductor device.

[0025]

In another embodiment of the present invention, a method for forming a semiconductor device is provided, which includes providing a semiconductor substrate; forming a stacked gate on the semiconductor substrate; and forming on the sidewall of the stacked gate A dummy partition wall; a groove is formed in the semiconductor substrate and substantially aligned with the edge of the dummy partition wall; and a stress source is formed, and at least a part is in the groove, wherein the stress source includes a The element is selected from germanium and carbon.

The step of forming a stressor includes: forming a lower part in the groove, wherein the element occupies a first atomic ratio in the lower part; and forming a higher part on the lower part, wherein the element is in the higher part. Part occupies a second atomic ratio, the second atomic ratio is substantially greater than the first atomic ratio, and further includes removing the dummy spacer, forming a gate spacer on the sidewall of the stacked gate, and doping An impurity to form a deep source/drain region.

[0026]

The method for forming a semiconductor device of the present invention utilizes a low-germanium SiGe region, which can make the defect region higher than the depletion region, reduce defects from falling into the depletion region, and reduce leakage current.

In addition, the bottom of the SiGe region is maintained below the channel region, which can prevent the pressure of the low-germanium SiGe stress region from adversely affecting the channel region.

[0027]

In order to make the above and other objects, features, and advantages of the present invention more obvious and understandable, the following is a detailed description of preferred embodiments in conjunction with the accompanying drawings:

[0028]

Description of the drawings

[0029]

Figure 1 shows the formation of shallow trench isolation regions in the substrate.

[0030]

Figure 2 shows the formation of stacked gates on the substrate.

[0031]

Figure 3 shows the formation of a dummy partition wall.

[0032]

FIG. 4 shows the patterning of the dummy partition wall to form another dummy partition wall.

[0033]

FIG. 5 shows that grooves are formed by etching along the edges of the dummy partition walls.

[0034]

Figure 6 shows the use of selective epitaxial growth to form an epitaxial region in the groove.

[0035]

Figure 7 shows the formation of a SiGe region at the bottom of the groove.

[0036]

FIG. 8 shows the removal of the dummy partition wall and the hard mask layer.

[0037]

Figure 9 shows the formation of partition walls.

[0038]

Figure 10 shows the channel region and depletion region of a MOS device.

[0039]

Figure 11 shows the NMOS device of the present invention.

[0040]

Wherein, the reference signs are explained as follows:

[0041]

2 Substrate; 4 Shallow trench isolation area;

[0042]

12 Stacked gate; 14 gate dielectric layer;

[0043]

16 Gate; 18 Hard mask layer;

[0044]

22 Dummy partition; 222 nitride layer;

[0045]

221 Lining oxide layer; 24 dummy partition walls;

[0046]

26 Groove; 30 extension area;

[0047]

32 SiGe area; 34 channel area;

[0048]

36 Vacant area; 38, 40 dotted line;

[0049]

44 The bottom of the channel region; 50 lightly doped source/drain regions;

[0050]

52 Partition wall; T, T1, T4, T3 thickness;

[0051]

54 Deep source/drain area; 56 Silicide area;

[0052]

60、62 Stress source; 60 SiGe area;

[0053]

62 SiC area

[0054]

Detailed ways

[0055]

FIG. 1 shows that shallow trench isolation regions (hereinafter referred to as STI regions) are formed in a substrate 2. The substrate 2 preferably includes a silicon wafer, and the substrate 2 may have a composite structure, such as a silicon-on-insulator (SOI).

The STI region 4 is formed to isolate the active region.

The method for forming the STI region 4 is the same as the generally known technology. For example, the substrate 2 can be etched to form a trench, and the trench can be filled with a dielectric material.

[0056]

2, a stacked gate 12 is formed on the substrate 2, and the stacked gate 12 includes a gate dielectric layer 14, a gate 16 and a hard mask layer 18.

The gate dielectric layer 14 may be formed of general dielectric materials, such as oxides, nitrides, oxynitrides, the above-mentioned multilayer structures, and combinations thereof.

The gate 16 may be made of generally known materials, such as doped polysilicon, metal, metal silicide, metal nitride, and combinations thereof.

The hard mask layer 18 preferably includes silicon nitride, oxide, oxynitride, and silicon carbide.

The method for forming the gate dielectric layer 14, the gate electrode 16 and the hard mask layer 18 is preferably to deposit a stacked layer containing the above-mentioned materials first, and then pattern the stacked layer.

[0057]

3, a dummy partition wall 22 is formed.

In one embodiment, the dummy spacer 22 includes a liner oxide layer 221 and a nitride layer 222.

In another embodiment, the dummy spacer 22 may be made of one or more layers of oxide, silicon nitride, silicon oxynitride, and/or other dielectric materials.

Preferred formation methods include general well-known techniques such as plasma etching chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), sub-atmospheric chemical vapor deposition (SACVD), and the like.

[0058]

FIG. 4 shows the patterning of the dummy partition wall 22 to form the dummy partition wall 24, wherein the method of patterning may be wet etching or dry etching.

The unetched portions of the liner oxide layer 221 and the nitride layer 222 serve as the liner oxide portion 241 and the nitrided portion 242, respectively.

[0059]

Referring to FIG. 5, the groove 26 is formed by isotropic or anisotropic etching along the edge of the dummy partition wall 24.

Although the depth of the groove 26 can be reduced according to integrated circuit technology, the preferable depth of the groove 26 is about 500 Å to 1000 Å, and more preferably about 700 Å to 900 Å.

[0060]

FIG. 6 shows that the epitaxial region 30 is formed by selective epitaxial growth (SEG) in the groove 26, which may also be referred to as a SiGe stressor or stress region.

The lattice constant of the SiGe stressor 30 is preferably greater than the lattice constant of the substrate 2.

In one embodiment, precursors containing Si and Ge (such as SiH4 and GeH4) are introduced, and the SiGe epitaxy is formed by the PECVD method.

The pressure in the reactor is preferably about 10 to 200 Torr, more preferably about 20 to 60 Torr.

The temperature of the substrate is preferably about 400°C to 1000°C, and more preferably about 500°C to 800°C.

In a preferred embodiment, the SiGe region 30 includes about 10% to 25% germanium, more preferably 15% to 20% germanium.

In one embodiment, the atomic ratio of germanium can be adjusted according to the partial pressures of SiH4 and GeH4.

[0061]

In another embodiment, during the epitaxial growth process, the ratio of germanium atoms is gradually adjusted to form the SiGe stress region 30.

The proportion of germanium atoms is preferably gradually increased from the bottom of the SiGe stress region 30 to the top of the SiGe stress region 30, for example, the flow rate of GeH4 is gradually increased.

In one embodiment, the proportion of germanium atoms at the bottom of the SiGe stress region 30 is less than about 10%, but the proportion of germanium atoms at the top of the SiGe stress region 30 is greater than about 15% or more.

[0062]

Referring to FIG. 7, the SiGe stress region 30 is preferably formed only at the bottom of the groove 26.

After the SiGe stress region 30 is formed, the conditions for epitaxial growth are changed to the conditions for forming the SiGe region 32 in the SiGe region 30, wherein the SiGe region 32 has a greater proportion of germanium atoms than the SiGe stress region 30.

The SiGe region 32 and the SiGe stress region 30 are preferably formed in the same reactor (in situ).

For example, increasing the flow rate of GeH4 to increase its partial pressure, so that the proportion of germanium atoms in the SiGe region 32 is preferably about 25% to 50%, more preferably about 25% to 35%.

Moreover, the germanium concentration of the SiGe region 32 is preferably greater than that of the SiGe stress region 30 by 5%.

[0063]

Referring to FIG. 8, the dummy partition wall 24 and the hard mask layer 18 are removed.

In one embodiment, the silicon nitride portion of the dummy spacer 24 and the hard mask layer 18 are etched with phosphoric acid, and the lining oxide portion of the dummy spacer 24 is removed with diluted hydrofluoric acid.

[0064]

A p-type impurity is implanted to form shallow doped source/drain regions (hereinafter referred to as LDD regions) 50.

Using the stacked gate 12 as a mask, the LDD region 50 is substantially aligned with the edge of the stacked gate 12.

In addition, an n-type impurity can also be injected to form a halo/pocket doped region (not shown).

[0065]

Referring to FIG. 9, a partition wall 52 is formed.

First, a lining oxide layer and a nitride layer are formed by coating, and then the lining oxide layer and the nitride layer are patterned to form the spacer 52.

In a preferred embodiment, the partition wall 52 has a thickness T4, which may be less than or equal to T3.

[0066]

Next, p-type impurities (such as boron, indium, etc.) are implanted to form deep source/drain regions 54.

FIG. 9 shows that the silicide region 56 is formed.

The silicide region 56 can be formed in a generally known manner, for example, depositing a thin metal layer (such as titanium, cobalt, nickel, tungsten, etc.) on the surface of the SiGe region 32 and the gate 16.

The substrate is heated to cause the silicide to react, bringing the metal into contact with the silicon. After the reaction, a silicide metal layer is formed between the silicon and the metal, and the unreacted metal is selectively removed.

[0067]

FIG. 10 shows that the channel region 34 and the depletion region 36 are adjacent to the junction (or junction).

To achieve the best effect, the thickness T1 of the SiGe stress region 30 is preferably less than 1/3 of the total thickness T of the SiGe regions 30 and 32 (refer to FIG. 7).

It can be seen from FIG. 10 that the SiGe regions 30 and 32 correspond to the positions of the depletion regions of the source/drain junctions.

The depleted region 36 is indicated by the dashed lines 38 and 40.

In a preferred embodiment, the junction of the SiGe regions 30 and 32 is higher than the depletion region 36.

Generally speaking, if the junction between two layers has different lattice constants, for example, the Si layer and the SiGe layer, defects and faults are often caused.

And as the gap between the lattice constants becomes larger, the defects and faults become more serious.

If the defect region around the Si and SiGe layer falls into the depletion region, the leakage current between the source/drain region and the substrate will be very high.

If the low-germanium SiGe region 30 is used, the defect region can be made higher than the depletion region 36, reducing defects falling into the depletion region, and the leakage current can be substantially reduced.

[0068]

The SiGe region 32 preferably extends below the bottom 44 of the channel region 34.

Since the magnitude of the stress is related to the ratio of germanium atoms in the SiGe stress source, the SiGe stress source on both sides of the channel region preferably has a high germanium concentration.

The bottom of the SiGe region 32 is maintained below the channel region 34, which can prevent the pressure of the low-germanium SiGe stress region 30 from adversely affecting the channel region.

[0069]

The above embodiment uses dummy spacers to form SiGe, but it is not necessary to use dummy spacers, for example, to form a stacked gate, an LDD region and a halo/pocket doped region to form A gate spacer, a groove is formed on the substrate, and a composite SiGe stress source is grown in the groove, wherein the composite SiGe stress source includes a low germanium layer disposed on a high germanium layer, and a deep source doped/ The drain region, and forming a silicide region on the deep source/drain region and the gate.

[0070]

FIG. 11 shows an NMOS device, which includes stressors 60 and 62 with a lattice constant smaller than that of the substrate 2.

In a preferred embodiment, the stressors 60 and 62 include SiC regions, the ratio of carbon atoms in the SiC region 60 is smaller than that of the SiC region 62, and the sizes of the stressors 60 and 62 are approximately the same as the aforementioned SiC stressors.

The proportion of carbon atoms in the SiC region 60 is preferably between about 1% and 5%.

The proportion of carbon atoms in the SiC region 62 is preferably between about 5% and 10%

[0071]

Although the present invention has been disclosed as above in preferred embodiments, it is not intended to limit the present invention. Those skilled in the art can make slight changes and modifications without departing from the spirit and scope of the present invention. Therefore, the present invention The scope of protection shall be subject to the scope defined by the appended claims.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS CN101140948A

1.

A semiconductor device including

A semiconductor substrate;

A stacked gate located on the semiconductor substrate; and

A stress source is adjacent to the stacked gate and at least a part of it is provided in the semiconductor substrate, wherein the stress source includes an element having a lattice constant different from the semiconductor substrate, and wherein the Stress sources include:

A lower part in which the element occupies a first atomic proportion, and

A higher part, where the element occupies a second atomic ratio, and the second atomic ratio is substantially greater than the first atomic ratio.

2.

3. The semiconductor device of claim 1, wherein the first atomic ratio is between about 10% and 25%, and wherein the second atomic ratio is between about 25% and 50%.

3.

The semiconductor device of claim 1, wherein the difference between the second atomic ratio and the first atomic ratio is greater than about 5%.

4.

The semiconductor device of claim 1, wherein the higher portion extends below the bottom of the channel region of the semiconductor device.

5.

The semiconductor device of claim 1, wherein the junction of the lower portion and the higher portion is substantially outside the depletion region of each source/drain junction.

6.

The semiconductor device of claim 1, wherein the thickness of the lower portion is less than 1/3 of the stressor.

7.

The semiconductor device of claim 1, wherein the element includes germanium, and the semiconductor device includes a PMOS device.

8.

The semiconductor device of claim 1, wherein the element includes carbon, and the semiconductor device includes an NMOS device.

9.

3. The semiconductor device according to claim 1, wherein in the lower part, the concentration of the element increases from a part close to the semiconductor device to a higher part close to the stressor.

10.

A method of forming a semiconductor device, including

Provide a semiconductor substrate;

Forming a stacked gate on the semiconductor substrate;

Forming a gate spacer on the sidewall of the stacked gate;

Forming a groove in the semiconductor substrate adjacent to the gate spacer; and

A stress source is formed, and at least a part of it is in the groove, wherein the stress source includes an element with a lattice constant different from that of the semiconductor substrate, and wherein the step of forming the stress source includes:

A lower part is formed in the groove, in which the element occupies a first atomic ratio, and

A higher part is formed on the lower part, wherein the element occupies a second atomic ratio, and the second atomic ratio is substantially greater than the first atomic ratio.

11.

The method of forming a semiconductor device according to claim 10, wherein said step of forming a stressor includes epitaxial growth.

12.

10. The method of forming a semiconductor device according to claim 10, wherein the step of forming the higher portion includes gradually changing the flow rate of the precursor, and the precursor contains the element.

13.

10. The method of forming a semiconductor device according to claim 10, wherein the first atomic ratio is between about 10% and 25%, and wherein the second atomic ratio is between about 25% and 50%.

14.

10. The method of forming a semiconductor device according to claim 10, wherein the element includes germanium, and wherein the method further comprises doping a p-type impurity into the source/drain region of a semiconductor device.

15.

10. The method of forming a semiconductor device according to claim 10, wherein the element includes carbon, and wherein the method further comprises doping an n-type impurity into the source/drain region of a semiconductor device.

[19] 中华人民共和国国家知识产权局

[51] Int. Cl.
H01L 29/78 (2006.01)
H01L 21/336 (2006.01)

[12] 发明专利申请公布说明书

[21] 申请号 200610173276.5

[43] 公开日 2008 年 3 月 12 日

[11] 公开号 CN 101140948A

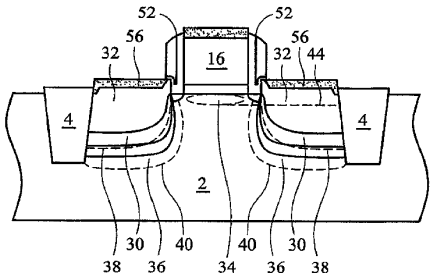
[22] 申请日 2006.12.31
[21] 申请号 200610173276.5
[30] 优先权
[32] 2006. 9. 6 [33] US [31] 11/516,265
[71] 申请人 台湾积体电路制造股份有限公司
地址 中国台湾新竹市
[72] 发明人 王盈斌
[74] 专利代理机构 隆天国际知识产权代理有限公司
代理人 陈 晨
权利要求书 2 页 说明书 7 页 附图 6 页

[54] 发明名称

半导体器件及其形成方法

[57] 摘要

本发明提供一半导体器件及其形成方法，该半导体器件包括：一半导体衬底；一叠置栅极，位于半导体衬底上；一应力源，邻接该叠置栅极，且至少有一部分设于半导体衬底中。其中该应力源包含一元素，可用来调整应力源的晶格常数。该应力源包括一较低部分及一较高部分，其中该元素在较低部分占第一原子比例，在较高部分占第二原子比例，且第二原子比例实质上大于第一原子比例。本发明的半导体器件的形成方法利用低锗的 SiGe 区，可使缺陷区高于空乏区，减少缺陷落入空乏区，从而可降低漏电流。另外 SiGe 区的底部维持在沟道区下方，可避免低锗 SiGe 应力区的压力对沟道区产生不良的影响。



1. 一种半导体器件，包括

一半导体衬底；

一叠置栅极，位于该半导体衬底上；以及

一应力源，邻近于该叠置栅极，且至少一部分设于该半导体衬底中，其中该应力源包含一元素，该元素具有一不同于该半导衬底的晶格常数，且其中该应力源包括：

一较低部分，其中该元素占一第一原子比例，以及

一较高部分，其中该元素占一第二原子比例，且该第二原子比例实质上大于该第一原子比例。

2. 如权利要求 1 所述的半导体器件，其中该第一原子比例介于约 10%至 25%之间，且其中该第二原子比例介于约 25%至 50%之间。

3. 如权利要求 1 所述的半导体器件，其中该第二原子比例与该第一原子比例的差距大于约 5%。

4. 如权利要求 1 所述的半导体器件，其中该较高部分延伸至该半导体器件的沟道区底部下方。

5. 如权利要求 1 所述的半导体器件，其中该较低部分和该较高部分的结实质上在各源/漏极结的空乏区外。

6. 如权利要求 1 所述的半导体器件，其中该较低部分的厚度小于该应力源的 1/3。

7. 如权利要求 1 所述的半导体器件，其中该元素包括锗，且该半导体器件包括一 PMOS 器件。

8. 如权利要求 1 所述的半导体器件，其中该元素包括碳，且该半导体器件包括一 NMOS 器件。

9. 如权利要求 1 所述的半导体器件，其中该较低部分中，该元素的浓度由靠近该半导体器件的部分朝靠近该应力源的较高部分增加。

10. 一种形成半导体器件的方法，包括

提供一半导体衬底；

在该半导体衬底上形成一叠置栅极；

在该叠置栅极的侧壁上形成一栅极间隔壁；

在邻近该栅极间隔壁的半导衬底中形成一凹槽；以及

形成一应力源，且至少有一部分于该凹槽中，其中该应力源包含一晶格常数不同于该半导体衬底的元素，且其中所述形成应力源的步骤包括：

在该凹槽中形成一较低部分，其中该元素占一第一原子比例，以及

在该较低部分上形成一较高部分，其中该元素占一第二原子比例，且该第二原子比例实质上大于该第一原子比例。

11. 如权利要求 10 所述的形成半导体器件的方法，其中所述形成应力源的步骤包括外延生长。

12. 如权利要求 10 所述的形成半导体器件的方法，其中所述形成较高部分的步骤包括逐渐地改变前驱物的流量，且该前驱物包含该元素。

13. 如权利要求 10 所述的形成半导体器件的方法，其中该第一原子比例介于约 10%至 25%之间，且其中该第二原子比例介于约 25%至 50%之间。

14. 如权利要求 10 所述的形成半导体器件的方法，其中该元素包括锗，且其中该方法还包括掺杂一 p 型杂质至一半导体器件的源/漏极区。

15. 如权利要求 10 所述的形成半导体器件的方法，其中该元素包括碳，且其中该方法还包括掺杂一 n 型杂质至一半导体器件的源/漏极区。

半导体器件及其形成方法

技术领域

本发明关于集成电路，且特别关于具有应力源的 MOS 器件的结构及其形成方法。

背景技术

近年来半导体行业致力于缩小半导体器件尺寸、降低成本，提高半导体器件的速度、性能及密度。改变源/漏极间的沟道区长度可改变沟道区的电阻，进而影响晶体管的性能。特别是，缩短沟道区的长度可减少源极至漏极的距离，若在其它参数不变的条件下，便可增加源/漏极间的电流。

为了进一步提高 MOS 器件的性能，可对沟道区施加一应力来增加载流子的移动速率。一般而言，可对 NMOS 器件的沟道区施加一拉应力，而对 PMOS 器件的沟道区施加一压应力。

通常会在源/漏极区中外延生长 SiGe 以对沟道区施加一压应力，包括在半导体衬底上形成一叠置栅极，在叠置栅极的侧壁上形成间隔壁，沿着栅极间隔壁在硅衬底中形成凹槽，在凹槽中外延生长 SiGe 应力源并回火。因为 SiGe 的晶格常数大于硅，所以在回火过程后，SiGe 会膨胀并对沟道区施加一压应力，而沟道区位于源极 SiGe 应力源及漏极 SiGe 应力源之间。同样地，在 NMOS 器件的沟道区中可形成 SiC 应力源，因为 SiC 的晶格常数小于硅，所以 SiC 会缩小并对沟道区施加一拉应力。

但传统的应力源形成方法会使 MOS 器件产生漏电流。应力源需有高锗或高碳浓度，但高锗或高碳浓度会产生许多缺陷，如漏电流及减小击穿电压。因此，为提供更好的应力源，业界急需针对应力源的形成方法加以改进。

发明内容

在本发明的一实施例中，提供一种半导体器件，包括一半导体衬底；一叠置栅极，设置于该半导体衬底上；一应力源，邻近于该叠置栅极，且至少

一部分设于该半导体衬底中，其中该应力源包含一元素，可用来调整该应力源的晶格常数。该应力源包括一较低部分及一较高部分，其中该元素在较低部分占第一原子比例，在较高部分占第二原子比例，且该第二原子比例实质上大于该第一原子比例。

在本发明的另一实施例中，提供一种半导体器件，包括一半导体衬底，如硅；一叠置栅极，位于该半导体衬底上；一应力源，邻近于该叠置栅极，且至少一部分设于该半导体衬底中，其中该应力源包含硅及一元素，该元素选自下列元素所组成的组：锗及碳，且其中该元素占第一原子比例；以及一中间区域，在半导体衬底和应力源之间，其中该中间区域包含硅及该元素，且其中该元素占第二原子比例，该第二原子比例小于该第一原子比例。

根据所述的半导体器件，其中该第一原子比例介于约 10%至 25%之间，且其中该第二原子比例介于约 25%至 50%之间。

根据所述的半导体器件，其中该第二原子比例与该第一原子比例的差距大于约 5%。

根据所述的半导体器件，其中该较高部分延伸至该半导体器件的沟道区底部下方。

根据所述的半导体器件，其中该较低部分和该较高部分的结实质上在各源/漏极结的空乏区外。

根据所述的半导体器件，其中该较低部分的厚度小于该应力源的 1/3。

根据所述的半导体器件，其中该元素包括锗，且该半导体器件包括一 PMOS 器件。

根据所述的半导体器件，其中该元素包括碳，且该半导体器件包括一 NMOS 器件。

根据所述的半导体器件，其中该较低部分中，该元素的浓度由靠近该半导体器件的部分朝靠近该应力源的较高部分增加。

在本发明的另一实施例中，提供一种半导体器件的形成方法，包括：提供一半导体衬底；在该半导体衬底上形成一叠置栅极；在该叠置栅极的侧壁上形成一栅极间隔壁；在邻近该栅极间隔壁的半导衬底中形成一凹槽；以及形成一应力源，且至少有一部分在该凹槽中，其中该应力源包含一元素，可用来调整应力源的晶格常数。形成应力源的步骤包括：在该凹槽中形成一较

低部分，其中该元素在较低部分占第一原子比例；以及在该较低部分上形成一较高部分，其中该元素在较高部分占第二原子比例，且该第二原子比例实质上大于该第一原子比例。

根据所述的形成半导体器件的方法，其中所述形成应力源的步骤包括外延生长。

根据所述的形成半导体器件的方法，其中所述形成较高部分的步骤包括逐渐地改变前驱物的流量，且该前驱物包含该元素。

根据所述的形成半导体器件的方法，其中该第一原子比例介于约 10%至 25%之间，且其中该第二原子比例介于约 25%至 50%之间。

根据所述的形成半导体器件的方法，其中该元素包括锗，且其中该方法还包括掺杂一 p 型杂质至一半导体器件的源/漏极区。

根据所述的形成半导体器件的方法，其中该元素包括碳，且其中该方法还包括掺杂一 n 型杂质至一半导体器件的源/漏极区。

在本发明的另一实施例中，提供一种半导体器件的形成方法，包括提供一半导体衬底；在该半导体衬底上形成一叠置栅极；在该叠置栅极的侧壁上形成一虚设间隔壁；在半导衬底中形成一凹槽，且实质上与该虚设间隔壁的边缘对齐；以及形成一应力源，且至少有一部分在该凹槽中，其中该应力源包含一元素，该元素选自锗和碳。形成应力源的步骤包括：在该凹槽中形成一较低部分，其中该元素在较低部分占第一原子比例；以及在该较低部分上形成一较高部分，其中该元素在较高部分占第二原子比例，该第二原子比例实质上大于该第一原子比例，且还包括去除该虚设间隔壁，在该叠置栅极的侧壁上形成一栅极间隔壁，以及掺杂一杂质以形成一深源/漏极区。

本发明的半导体器件的形成方法利用低锗的 SiGe 区，可使缺陷区高于空乏区，减少缺陷落入空乏区，从而可降低漏电流。另外 SiGe 区的底部维持在沟道区下方，可避免低锗 SiGe 应力区的压力对沟道区产生不良的影响。

为了让本发明的上述和其它目的、特征、和优点能更明显易懂，下文特举优选实施例，并结合附图，作详细说明如下：

附图说明

图 1 显示在衬底中形成浅沟槽隔离区。

图 2 显示在衬底上形成叠置栅极。

图 3 显示形成一虚设间隔壁。

图 4 显示图案化虚设间隔壁以形成另一虚设间隔壁。

图 5 显示沿着虚设间隔壁的边缘蚀刻形成凹槽。

图 6 显示利用选择性外延生长在凹槽中形成外延区。

图 7 显示在凹槽的底部形成 SiGe 区。

图 8 显示去除虚设间隔壁及硬掩模层。

图 9 显示形成间隔壁。

图 10 显示 MOS 器件的沟道区及空乏区。

图 11 显示本发明的 NMOS 器件。

其中，附图标记说明如下：

2	衬底；	4	浅沟槽隔离区；
12	叠置栅极；	14	栅极介电层；
16	栅极；	18	硬掩模层；
22	虚设间隔壁；	222	氮化层；
221	衬氧化层；	24	虚设间隔壁；
26	凹槽；	30	外延区；
32	SiGe 区；	34	沟道区；
36	空乏区；	38、40	虚线；
44	沟道区的底部；	50	轻掺杂源/漏极区；
52	间隔壁；	T、T1、T4、T3	厚度；
54	深源/漏极区；	56	硅化物区；
60、62	应力源；	60	SiGe 区；
62	SiC 区		

具体实施方式

图 1 显示浅沟槽隔离区(以下简称 STI 区)形成于衬底 2 中，衬底 2 优选包括硅晶片，且衬底 2 可具有一复合结构，例如硅上绝缘层(SOI)。形成 STI 区 4 以隔离有源区。形成 STI 区 4 的方法与一般公知技术相同，例如，可蚀刻衬底 2 以形成沟槽，并以介电材料填满该沟槽。

参照图 2，形成一叠置栅极 12 于衬底 2 上，叠置栅极 12 包括栅极介电层 14、栅极 16 及硬掩模层 18。栅极介电层 14 可以由一般的介电材质形成，例如，氧化物、氮化物、氮氧化物、上述的多层结构及其上述的组合。栅极 16 可包括一般公知的材质，例如，掺杂多晶硅、金属、硅化金属、氮化金属及上述的组合。硬掩模层 18 优选包括氮化硅、氧化物、氮氧化物及碳化硅。栅极介电层 14、栅极 16 及硬掩模层 18 的形成方法优选为先沉积包含上述材料的堆叠层，再图案化该堆叠层。

参照图 3，形成一虚设间隔壁 22。在一实施例中，虚设间隔壁 22 包括衬氧化层 221 及氮化层 222。在另一实施例中，虚设间隔壁 22 可为一层或多层氧化物、氮化硅、氮氧化硅和/或其它介电材质。优选的形成方法包括一般的公知技术，例如，等离子体蚀刻化学气相沉积法(PECVD)、低压化学气相沉积法(LPCVD)、次大气压化学气相沉积(SACVD)及其类似方法。

图 4 显示图案化虚设间隔壁 22 以形成虚设间隔壁 24，其中图案化的方法可为湿式蚀刻或干式蚀刻。衬氧化层 221 及氮化层 222 未蚀刻的部分分别作为衬氧化部 241 及氮化部 242。

参照图 5，沿着虚设间隔壁 24 的边缘以等向或异向性蚀刻形成凹槽 26。虽然凹槽 26 的深度可依集成电路技术缩小，但凹槽 26 优选的深度为约 500Å 至 1000Å，且更优选为约 700Å 至 900Å。

图 6 显示在凹槽 26 中以选择性外延生长(SEG)形成外延区 30，也可称为 SiGe 应力源或应力区。SiGe 应力源 30 的晶格常数优选大于衬底 2 的晶格常数。在一实施例中，导入含 Si 及 Ge 的前驱物(如 SiH_4 及 GeH_4)，以 PECVD 法形成 SiGe 外延。反应器中的压力优选为约 10 至 200 托，更优选为约 20 至 60 托。衬底的温度优选为约 400℃至 1000℃，且更优选为约 500℃至 800℃。在一优选实施例中，SiGe 区 30 包括约 10%至 25%的锗，更优选为 15%至 20%的锗。在一实施例中，锗的原子比例可依 SiH_4 及 GeH_4 的分压来调整。

在另一实施例中，在外延生长的过程中，逐渐调整锗原子比例来形成 SiGe 应力区 30。锗原子的比例优选由 SiGe 应力区 30 底部逐渐增加至 SiGe 应力区 30 顶部，例如，逐渐增加 GeH_4 的流速。在一实施例中，SiGe 应力区 30 底部的锗原子比例小于约 10%，但 SiGe 应力区 30 顶部的锗原子比例则大于约 15%或更高。

参照图 7，SiGe 应力区 30 优选只形成于凹槽 26 的底部。在形成 SiGe 应力区 30 之后，将外延生长的条件转变为形成 SiGe 区 32 于 SiGe 区 30 的条件，其中 SiGe 区 32 的锗原子比例比 SiGe 应力区 30 大。SiGe 区 32 与 SiGe 应力区 30 优选在同一反应器(in situ)中形成。例如，增加 GeH_4 的流速以增加其分压，使 SiGe 区 32 的锗原子比例优选介于约 25%至 50%，更优选为约 25%至 35%。且 SiGe 区 32 的锗浓度优选比 SiGe 应力区 30 大 5%。

参照图 8，去除虚设间隔壁 24 及硬掩模层 18。在一实施例中，以磷酸蚀刻虚设间隔壁 24 的氮化硅部及硬掩模层 18，且以稀释的氢氟酸去除虚设间隔壁 24 的衬氧化部。

注入一 p 型杂质来形成浅掺杂源/漏极区(以下简称 LDD 区)50。以叠置栅极 12 做为掩模，使 LDD 区 50 实质上与叠置栅极 12 的边缘对齐。此外，也可注入一 n 型杂质来形成晕轮状/口袋型(Halo/pocket)掺杂区(未图示)。

参照图 9，形成间隔壁 52。先涂覆形成一衬氧化层及一氮化层，再图案化衬氧化层及氮化层以形成间隔壁 52。在一优选实施例，间隔壁 52 有一厚度 T4，其可小于或等于 T3。

接着，注入 p 型杂质(如硼、铟等类似物)以形成深源/漏极区 54。图 9 显示形成硅化物区 56。可以一般公知的方式形成硅化物区 56，例如，沉积一金属薄层(如钛、钴、镍、钨等类似物)于 SiGe 区 32 与栅极 16 的表面。对衬底加热，让硅化物产生反应，使金属与硅接触，反应之后，一硅化金属层形成于硅与金属之间，并选择性去除未反应的金属。

图 10 显示沟道区 34 及空乏区 36 邻近于结（或称接面）。为达到最佳效果，SiGe 应力区 30 的厚度 T1 优选小于 SiGe 区 30 及 32 总厚度 T 的 1/3(参照图 7)。图 10 可看出 SiGe 区 30 和 32 与源/漏极结的空乏区的位置相对应。空乏区 36 以虚线 38、40 表示。在一优选实施例中，SiGe 区 30 和 32 的结高于空乏区 36。一般来说，若两层间的结具有不同的晶格常数，例如，Si 层及 SiGe 层，常会导致缺陷及断层。且随着晶格常数的差距愈大，缺陷及断层的情况就愈严重。若 Si 及 SiGe 层周围的缺陷区落入空乏区，源/漏极区及衬底间的漏电流会非常高。若利用低锗的 SiGe 区 30，可使缺陷区高于空乏区 36，减少缺陷落入空乏区，则可实质上降低漏电流。

SiGe 区 32 优选延伸至沟道区 34 的底部 44 下方。因应力大小与 SiGe 应

力源中的锗原子比例有关，因此沟道区两侧的 SiGe 应力源最好具高锗浓度。SiGe 区 32 的底部维持在沟道区 34 下方，可避免低锗 SiGe 应力区 30 的压力对沟道区产生不良的影响。

上述实施例是利用虚设间隔壁来形成 SiGe，但也可不必利用虚设间隔壁，例如，形成一叠置栅极，一 LDD 区及晕轮状/口袋型(Halo/pocket)掺杂区，形成一栅极间隔壁，于衬底上形成凹槽，生长复合式 SiGe 应力源于凹槽中，其中该复合式 SiGe 应力源包括一低锗层设置于一高锗层上，掺杂深源/漏极区，以及形成硅化物区于深源/漏极区与栅极上。

图 11 显示一 NMOS 器件，其中包括晶格常数小于衬底 2 的应力源 60、62。在一优选实施例中，应力源 60、62 包括 SiC 区， SiC 区 60 的碳原子比例较 SiC 区 62 小，且应力源 60、62 的尺寸与上述的 SiC 应力源大致相同。SiC 区 60 的碳原子比例优选为约 1%至 5%之间。SiC 区 62 的碳原子比例优选为约 5%至 10%之间

虽然本发明已以优选实施例揭示如上，然其并非用以限定本发明，所属领域技术人员，在不脱离本发明的精神和范围内，当可作些许的更动与润饰，因此本发明的保护范围当视后附的权利要求所界定的范围为准。

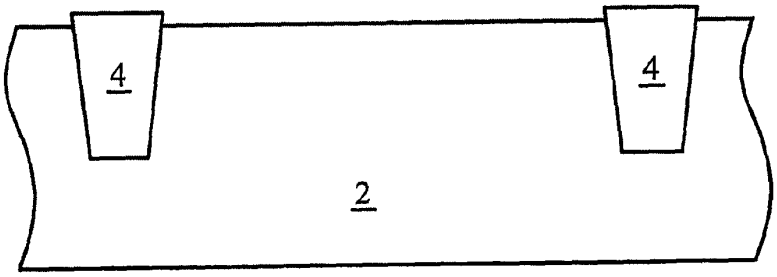


图1

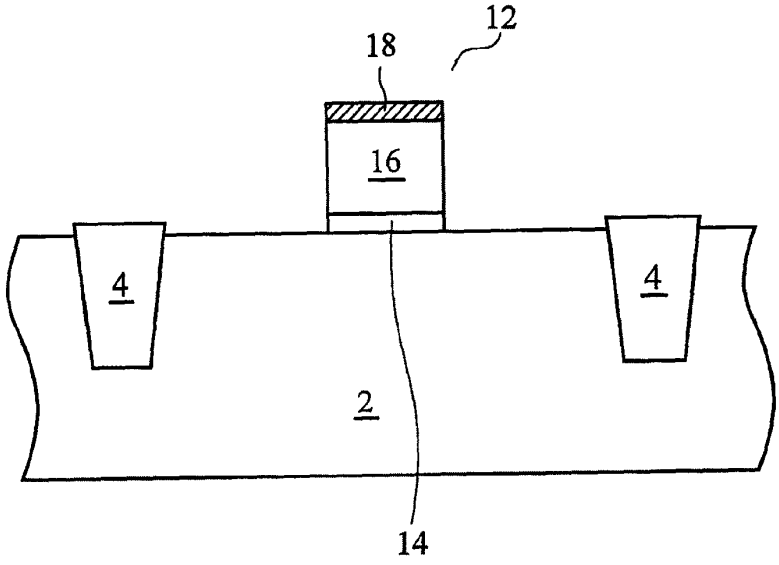


图2

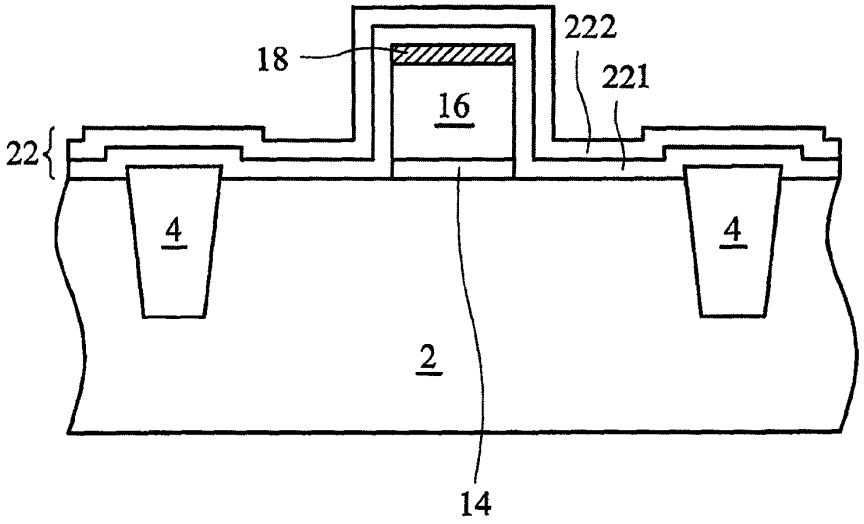


图3

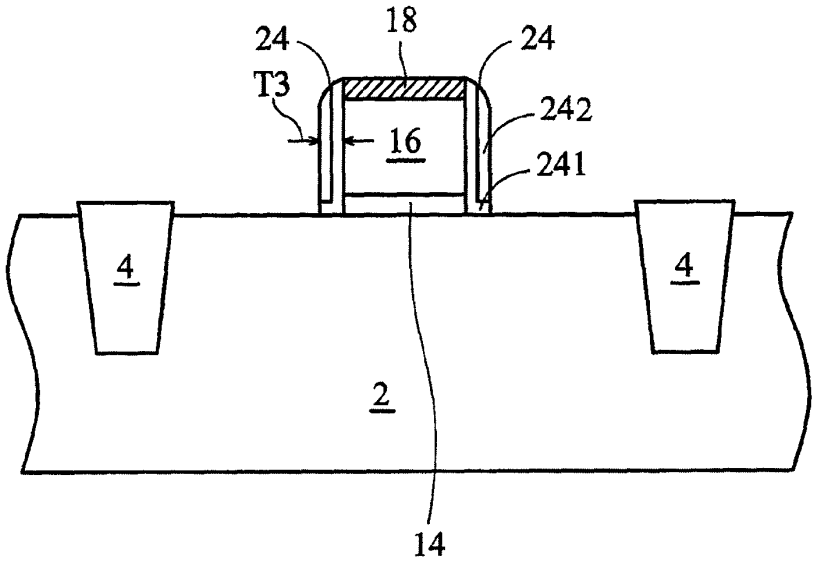


图4

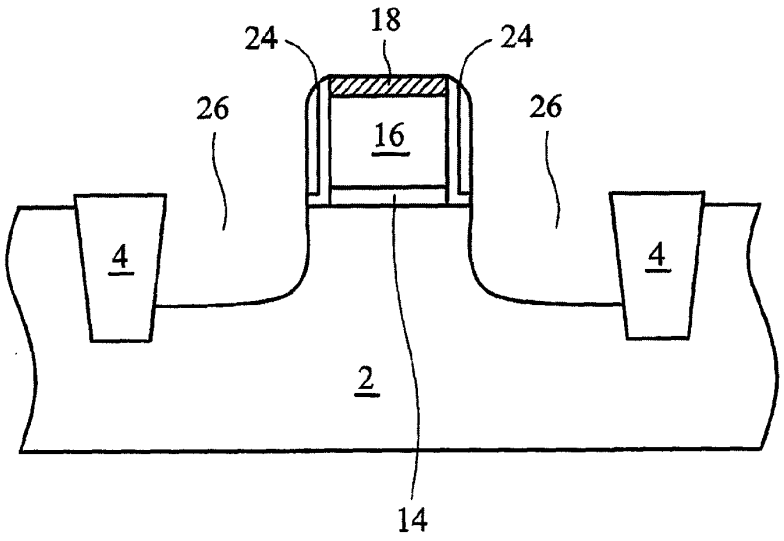


图5

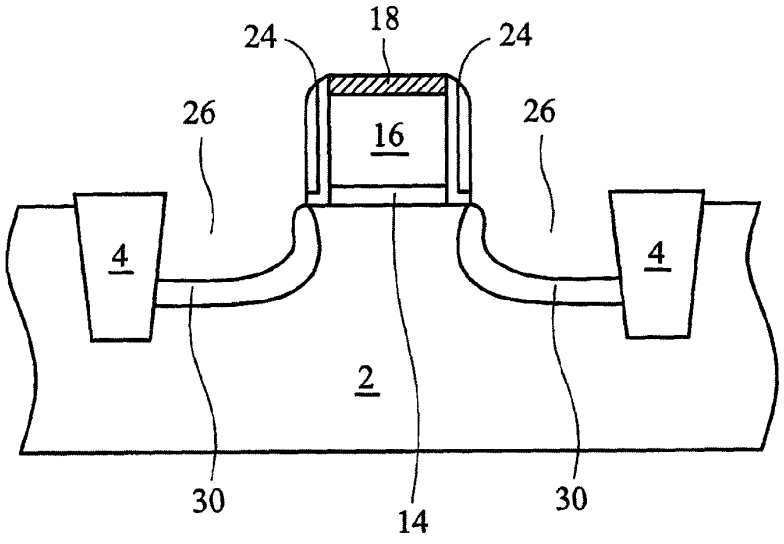


图6

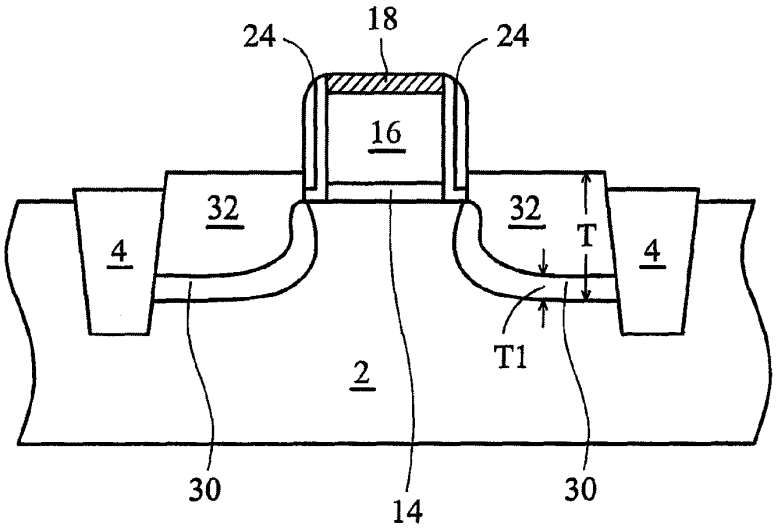


图7

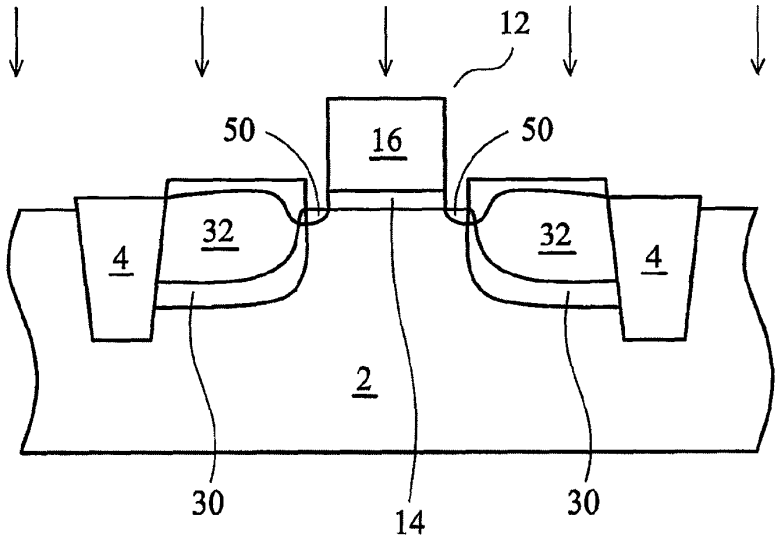


图8

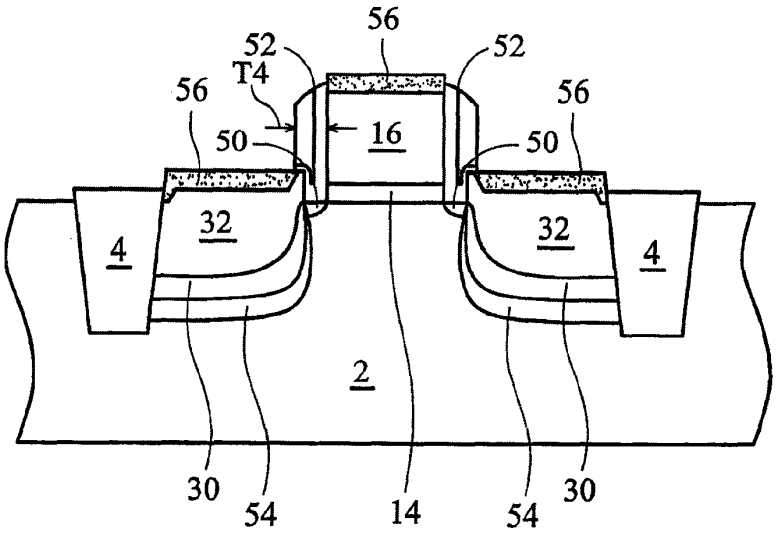

56
52
52
T4
56
56
50
16
50
32
32
4
4
2
30
54
14
54
30

图9

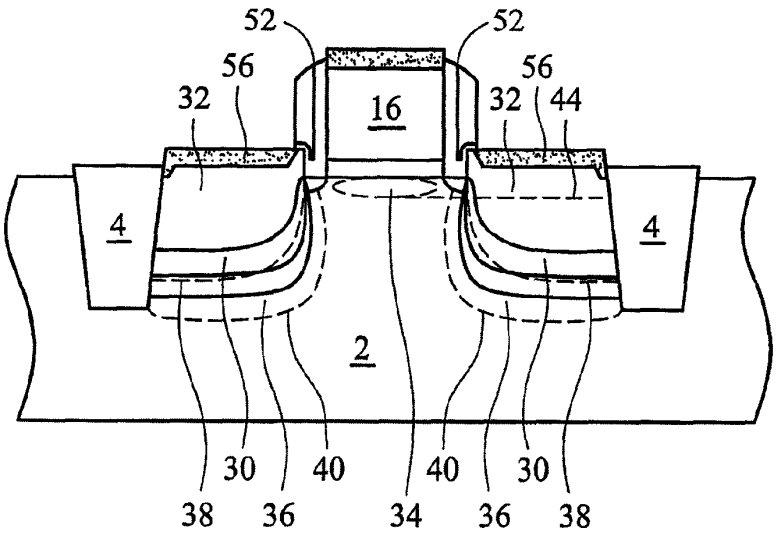

52
52
56
56
32
16
32
44
4
4
2
30
40
40
30
38
36
34
36
38

图10

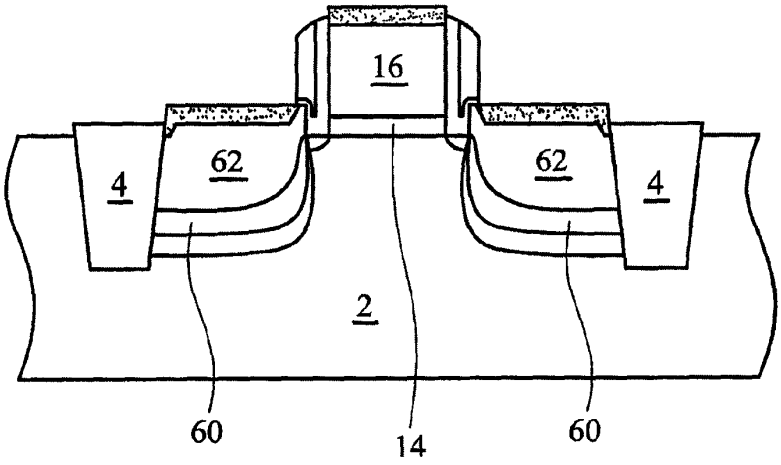


图11

Espacenet

Bibliographic data: CN101300664 (A) — 2008-11-05

Technique for strain engineering in si-based transistors by using embedded semiconductor layers including atoms with high covalent radius

Inventor(s): CHRISTOF STRECK [US]; VOLKER KAHLERT [US]; ALEXANDER HANKE [US] + (STRECK CHRISTOF, ; KAHLERT VOLKER, ; HANKE ALEXANDER)

Applicant(s): ADVANCED MICRO DEVICES INC [US] + (ADVANCED MICRO DEVICES INC)

Classification: - international: *H01L21/20; H01L21/205*
- cooperative: **H01L21/20 (KR)**; **H01L21/205 (KR)**; **H01L21/823807 (EP, US)**; **H01L21/823878 (EP, US)**; **H01L21/84 (EP, US)**; **H01L27/1203 (EP, US)**; **H01L29/1054 (EP, US)**; **H01L29/66628 (EP, US)**; **H01L29/66636 (EP, US)**; **H01L29/7848 (EP, US)**; H01L29/165 (EP, US); H01L29/665 (EP, US); H01L29/6656 (EP, US)

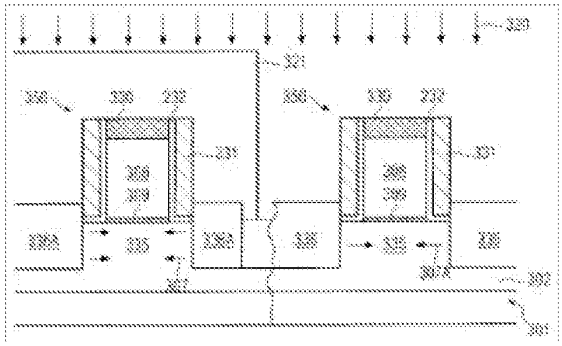
Application number: CN20068040454 20061023

Priority number(s): WO2006US41559 20061023 ; DE20051051994 20051031 ; US20060465592 20060818

Also published as: CN101300664 (B) DE102005051994 (A1) DE102005051994 (B4) JP2009514248 (A) KR101238432 (B1) more

Abstract of CN101300664 (A)

By incorporating an atomic species of increased covalent radius, which may at least partially substitute germanium, a highly efficient strain mechanism may be provided, in which the risk of stress relief due to germanium conglomeration and lattice defects may be reduced. The atomic species of increased radius, such as tin, may be readily incorporated by epitaxial growth techniques on the basis of tin hydride.



Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION CN101300664A

Technology for engineering strain in silicon-based transistors by using an embedded semiconductor layer containing atoms with a high covalent radius

[0001]

Technical field

[0002]

The present invention generally relates to the formation of integrated circuits, and more specifically, to the formation of different transistor types with strained channel regions by using embedded silicon/germanium to increase the charge carrier in the channel region of the transistor. Mobility.

[0003]

Background technique

[0004]

The manufacture of integrated circuits requires a large number of circuit elements to be formed on a given chip area according to a specific circuit layout.

In general, many process technologies are currently used. Among them, for complex circuits such as microprocessors, memory chips, etc., CMOS technology is currently the best because of its excellent performance in terms of operating speed and/or power consumption and/or cost efficiency. A promising approach. When using CMOS technology to manufacture complex integrated circuits, millions of transistors, that is, N-channel transistors and P-channel transistors are formed on a substrate containing a crystalline semiconductor layer. MOS transistors, whether they are N-channel transistors or P-channel transistors, include the so-called PN junction, which is formed by the interface of highly doped drain and source regions, where There are oppositely doped channel regions.

[0005]

The conductivity of the channel region, that is, the driving current capability of the conductive channel, is controlled by the gate formed on the channel region and separated by a thin insulating layer.

Once the conductive channel is formed, due to the application of appropriate control voltage on the gate electrode, the conductivity of the channel region depends on the concentration of dopants, the mobility of most charge carriers, and the source of the channel region for a given extension in the width direction of the transistor. The distance between the electrode and the drain (also known as the channel length). Therefore, by applying an appropriate control voltage to the gate electrode, combined

with the ability to quickly generate a conductive channel under the insulating layer, the conductivity of the entire channel region substantially determines the performance of the MOS transistor. Therefore, shortening the channel length reduces the channel resistance coefficient, which provides the main design standard for channel length to improve the operating speed of integrated circuits.

[0006]

However, the size of transistors continues to shrink, and many related issues must be addressed so as not to over-offset the advantages of stably shortening the channel length of MOS transistors.

One of the main issues in this regard is the development of improved photolithography and etching strategies to reliably and reproducibly produce circuit elements with critical dimensions for the new generation of devices, such as the gate electrodes of transistors. Furthermore, the drain and source regions are required to have high-precision dopant profiles in the vertical and side directions to provide low sheet and contact resistivity and desired channel control ability. In addition, considering the leakage current control, the vertical position of the PN junction of the gate insulating layer is also a key design criterion. Therefore, shortening the channel length generally also requires reducing the depth of the drain and source regions at the interface formed by the gate insulating layer and the channel region, which requires sophisticated implantation techniques. According to other methods, the epitaxial growth region (called the elevated drain and source region) is formed with a specific offset (offset) to the gate electrode to increase the conductivity of the elevated drain and source region while maintaining the Shallow PN junction of the gate insulating layer.

[0007]

Because the critical size, that is, the gate length of the transistor, continues to shrink, it is necessary to adapt and possibly newly develop highly complex process technologies related to the above-mentioned process steps. Some people have proposed to increase the charge in the channel region for a given channel length. The carrier mobility also improves the channel conductivity of the transistor device, thereby providing the possibility of achieving improved performance, matching with the advancement of future technology nodes, and avoiding or at least delaying many of the above-mentioned devices related to device scaling (scaling) Process adjustment.

An effective mechanism to increase the mobility of charge carriers is to modify the lattice structure of the channel region, for example, by generating tensile or compressive stress near the channel region to generate corresponding strain in the channel region, so that the mobility of electrons and holes are separated. Subject to modification. For example, tensile strain in the channel region increases the electron mobility, and a 50% or higher increase in mobility can be obtained. Depending on the magnitude and direction of the tensile strain, this increase in mobility can be directly converted into corresponding conductivity in sequence. Sexual improvement. On the other hand, the compressive strain of the channel region can increase hole mobility, thereby providing the possibility of improving the performance of P-type transistors. For further generations of devices, introducing stress or strain engineering into integrated circuit manufacturing is a very promising method, because, for example, strained silicon can be regarded as a "new" type of semiconductor material, which can make Fast and powerful semiconductor device manufacturing becomes possible without the use of expensive semiconductor materials, and many well-established manufacturing technologies are still available.

[0008]

Therefore, it has been proposed to introduce, for example, a silicon/germanium layer or a silicon/carbon layer in or under the channel region to generate tensile or compressive stress, which can cause corresponding strain.

By introducing a stress-generating layer in or under the channel region, the performance of the transistor can be improved to a considerable extent. Therefore, considerable effort has been invested to form the corresponding stress layer and implement it in the well-known and well-recognized MOS technology. For example, other epitaxial growth techniques are developed and added to the manufacturing process to form a germanium-containing or carbon-containing stress layer in the channel region or at an appropriate position under it.

[0009]

Other methods are to use, for example, overlaying layers, spacer elements, etc. to generate external stress to generate desired strain in the channel region.

However, the process of applying a specific external stress to generate strain in the channel region may encounter the problem of inefficient conversion of external stress into strain in the channel region. Therefore, although the above-mentioned method that requires an additional stress layer in the channel region has advantages in terms of process complexity, the efficiency of the stress transfer mechanism may be affected by the process and device characteristics, which may result in the reduction of a transistor Type performance improvements.

[0010]

Another method is to improve the hole mobility in PMOS transistors by forming strained silicon/germanium layers in the drain and source regions of the transistor, wherein the compressively strained drain region and source region are in the adjacent silicon channel region Produce uniaxial strain.

For this purpose, the drain and source regions of the PMOS transistor are selectively recessed, while the NMOS transistor is masked, and then a silicon/germanium layer is selectively formed in the PMOS transistor by epitaxial growth. This technology provides significant benefits for improving the performance of PMOS transistors and therefore the entire CMOS device.

[0011]

Therefore, using the engineering strain of embedded semiconductor materials, especially silicon/germanium, as a strain or relaxation layer depending on the desired effect, has proven to be a powerful method to increase the device performance of high-end silicon-based transistors.

However, as a result, the degree of strain induced by individual channel regions depends on the amount of lattice mismatch between the basic silicon and the embedded semiconductor compound. For silicon/germanium, the current established epitaxial growth technology limits the maximum germanium concentration to about 25%. Otherwise, germanium accumulation may occur, which in turn may lead to undesirable stress relief in the corresponding embedded semiconductor compound material, thereby reducing it Strain of individual channel regions.

[0012]

In view of the above situation, there is a real need for improving technologies that use embedded semiconductor materials to effectively increase strain while substantially avoiding or at least reducing one or more of the above-mentioned problems.

[0013]

Summary of the invention

[0014]

The following provides a brief summary of the present invention for a preliminary understanding of some aspects of the present invention.

This summary is not an exhaustive overview of the invention, and it is not intended to verify the key or important elements of the invention, or to describe the scope of the invention.

Its sole purpose is to present some concepts in a simplified form as an introduction to the more detailed description later.

[0015]

Generally speaking, the present invention relates to a technique for generating strain in a specific region of a crystalline semiconductor layer. For this purpose, a silicon-based crystal lattice (that is, a diamond-like crystal lattice) is used in this technique. The lattice mismatch between the lattice structure and the semiconductor compound that has an enlarged lattice gap.

Corresponding technology is commonly used to generate strained silicon channels in relatively high-end silicon-based MOS transistor devices. Among them, as mentioned above, the amount of strain obtained by this mechanism is particularly significantly limited in the limited germanium that can be successfully used in the currently established epitaxial growth technology. concentration.

Therefore, in the present invention, the method that can be used in addition to germanium or alternatively used with germanium can be used in silicon-like crystal structures that have significantly increased covalent radius of other atomic species for bonding characteristics. In this way, it is possible to greatly reduce the number of non-silicon atoms and high crystal distortion in individual silicon-based crystal structures.

In the illustrated embodiment of the present invention, since tin atoms have the same valence compared to silicon and germanium, and also exhibit a significantly larger covalent radius, tin (Sn) can be used as an additional additive of germanium Or substitutes.

[0016]

According to an exemplary embodiment of the present invention, a transistor device includes a substrate on which a crystalline semiconductor layer having a diamond-like crystal structure is formed.

The crystalline semiconductor layer includes a stress-inducing region. The stress-inducing region includes silicon and other atomic species having the same atomic valence as silicon in the crystalline structure, and the other atomic species has a covalent radius greater than that of germanium. Covalent radius.

In addition, the transistor device includes a gate electrode formed on the crystalline semiconductor layer, and a strained channel region.

[0017]

According to another exemplary embodiment of the present invention, a semiconductor device includes a crystalline semiconductor layer having a first portion containing silicon and tin to form a first strain region in the crystalline semiconductor layer.

[0018]

According to another exemplary embodiment of the present invention, a method includes forming a crystalline structure based on silicon and at least one other atomic species having a covalent radius greater than that of germanium in a crystalline semiconductor layer.

In addition, the method includes using the crystalline structure to generate strain in the first specific region of the semiconductor layer.

[0019]

Description of the drawings

[0020]

The present invention can be understood with reference to the accompanying drawings and the following description, wherein similar component symbols represent similar components, and among them:

[0021]

1a to 1d schematically show an exemplary embodiment of the present invention, in a crystalline semiconductor layer based on silicon and other atomic species that can be built into a silicon-diamond structure and have a larger covalent radius compared to germanium , Cross-sectional views of the semiconductor device during the different manufacturing stages in which the strain zone is formed;

[0022]

Figures 2a to 2d schematically show cross-sectional views during different manufacturing stages of forming a transistor device receiving an embedded strained semiconductor region to generate compressive strain in individual channel regions according to further exemplary embodiments of the present invention; and

[0023]

3 is a schematic cross-sectional view of a semiconductor device according to another exemplary embodiment of the present invention. The semiconductor device includes different transistor elements that receive different amounts of tin to generate different strain levels.

[0024]

Various modifications and changes can be easily made to the present invention, and its specific embodiments are shown in the form of examples with drawings, and are described in detail herein.

However, it should be understood that the description of the specific embodiments herein is not intended to limit the specific types of the present invention, but is intended to cover all that fall within the spirit and scope of the present invention as defined by the appended claims. Modifications, equivalences and changes.

[0025]

Detailed ways

[0026]

Hereinafter, illustrative examples of the present invention will be described.

For the sake of clarity, not all features actually implemented are described in this specification.

Of course, it should be understood that in any such actual development, many specific embodiments must be determined to achieve the developer's specific goals, such as complying with system-related and business-related restrictions, and these goals range from one embodiment to another. The embodiment will be different.

In addition, it will be understood that such development may be complicated and time-consuming, but for those skilled in the art who understand the disclosure of the present invention, such development is actually routine work.

[0027]

The present invention will now be described with reference to the drawings.

The various structures, systems, and devices in the figure are summarized descriptions, and are only used for explanation, so as not to obscure the present invention with details known to those skilled in the art.

Nevertheless, this specification still includes drawings to illustrate and explain the exemplary embodiments of the present invention.

It is necessary to understand the words and phrases used in this article, and interpret these words and phrases to have meanings that conform to those words and phrases that are understood by those familiar with the relevant field.

There is no specific term or phrase definition, that is, the definition that is different from the usual and customary meaning understood by those familiar with the art is implicit in the consistent usage of the term or phrase herein.

When a term or phrase means a special meaning, that is, when it has other meanings than understood by those familiar with the art, the special definition will be directly and clearly provided in this specification by providing the definition under the special definition of the term or phrase. In the description.

[0028]

Generally speaking, the present invention focuses on using the strain or relaxed semiconductor structure of a diamond-type crystal lattice structure with a different lattice gap compared to an unstrained silicon crystal to improve the strain initiation mechanism.

As mentioned earlier, the mechanism of placing strain or relaxing the silicon/germanium layer in the appropriate position of the silicon-based semiconductor device provides an efficient engineering strain technology to correspondingly improve the mobility of charge carriers, especially in relatively high-end MOS transistor devices.□□channel area.

These technologies rely on an epitaxial growth process in which a strained or relaxed silicon/germanium layer can be formed, depending on the requirements of the device.

[0029]

In addition, the recent development of local selective epitaxial growth technology can effectively inhibit significant material deposition on the dielectric surface, but efficiently deposit silicon, silicon/germanium equal to exposed silicon or silicon-like surfaces.

For example, if a silicon/germanium layer is deposited on a crystalline silicon layer, a silicon/germanium material can be deposited so as to have a lattice gap substantially like the underlying crystalline "template" to form a strained silicon/germanium layer. Because compared to pure silicon crystals, undisturbed silicon/germanium crystals may have slightly enlarged lattice gaps.

The difference in the lattice gap between the silicon/germanium layer and the silicon layer depends on the germanium concentration.

Therefore, the amount of strain generated in the silicon/germanium layer also depends on the germanium concentration.

However, as mentioned earlier, according to the current epitaxial growth technology, the maximum germanium concentration can be as high as about 25 to 30%, but a higher concentration may actually cause germanium to accumulate, which in turn may lead to an increase in the defect rate, making the initial strain silicon/ The germanium layer relaxes.

[0030]

According to the present invention, the desired degree of lattice mismatch and therefore the strain can be adjusted on the basis of atomic species having a significantly larger covalent radius than germanium. Among them, in some exemplary embodiments, regarding the diamond-like crystal structure The covalent bonding structure of, the atomic species considered to be used has essentially the same valence as silicon or germanium.

In an illustrative embodiment, tin with a covalent radius of 1.04 angstroms () can be used as an appropriate atomic species.

For example, silicon with a covalent radius of 1.17 angstroms can be used in combination with germanium with a covalent radius of 1.22 angstroms, where in addition a certain amount of tin can be used to create a significantly increased lattice mismatch.

Because the difference in covalent radius between silicon and tin is significantly greater than that between silicon and germanium, reducing the number of non-silicon atoms can achieve a more significant effect on the entire lattice structure.

In this way, the germanium concentration can be maintained below the threshold of about 25%, and the lattice mismatch can still be improved by adding a certain amount of tin.

[0031]

Furthermore, in some illustrative embodiments, silicon can be used in combination with tin without adding any germanium, thereby providing a moderately high degree of lattice modification and significantly reducing the number of non-silicon atoms.

For example, in some embodiments, in addition to introducing tin by epitaxial growth, other techniques such as implantation to introduce a certain amount of tin are also considered, or alternatively using the two methods.

Nevertheless, the reduction of the number of tin atoms can make a significant contribution to lattice distortion, and even the atomic concentration that can be achieved by the current implantation technology can fully produce a specific strain or at least fine-tune the lattice mismatch, so this strain can be achieved. .

Because ion implantation is a well-established technology, based on the resist mask formed by photolithography technology, ion implantation can be performed at room temperature, so the corresponding introduction of tin can be achieved in a highly efficient and even highly localized manner. , Thereby providing additional flexibility in process technology and device design.

For example, the currently implemented implantation technology can be used to achieve a concentration of approximately 1020 tin atoms/cm ^ 3 so that the strain in the corresponding silicon/tin or silicon/germanium/tin crystal structure can be efficiently adjusted or controlled.

[0032]

The following detailed description may refer to a specific application of the principle of the present invention, that is, introducing an atomic species with an increased covalent radius to generate strain in a specific crystalline semiconductor region.

However, it should be understood that there is no intention to impose any restrictions on specific transistor structures such as SOI-like transistors, bulk devices, transistors with raised drain and source regions, etc., except in the embodiments and claims. Special restrictions are explained.

[0033]

With reference to Figs. 1a to 1d, Figs. 2a to 2d and Fig. 3, further illustrative embodiments of the present invention will now be described in more detail.

[0034]

FIG. 1a schematically shows a cross-sectional view of the semiconductor device 100 in the initial manufacturing stage.

The semiconductor device 100 includes a substrate 101, which can be any suitable substrate with a semiconductor layer 102, and circuit elements such as transistors, capacitors, resistors, etc. can be formed in or on the substrate 101.

For example, the substrate 101 may be a bulk semiconductor substrate such as a silicon substrate, or may be any insulating substrate such as an SOI-like substrate, wherein the semiconductor layer 102 may be formed on a buried insulating layer (not shown).

It should be understood that although the present invention combines highly reduced MOS transistors typically made with high-end CMOS technology, including transistors with 50 nanometers (nm) and even smaller gate lengths, it has considerable advantages, but the The principles of the invention can also be applied to less critical applications, so that existing designs can achieve significant performance increases.

[0035]

The semiconductor layer 102 may be a silicon-based crystalline semiconductor layer, where the term silicon-based is understood to include a material layer with a silicon concentration of at least 50% by atom.

In the illustrated embodiment, the semiconductor layer 102 may be surface-doped with a silicon layer, as is typically used for highly complex integrated circuits, and the integrated circuit has a doped silicon layer for transistor elements whose gate length is within the above-mentioned specific range.

A substantially crystalline layer 103 may be further formed on the layer 102. The crystalline layer 103 may represent a so-called buffer layer. In this crystalline layer, the crystallization does not match and therefore the concentration of specific atomic species such as germanium, tin, etc. may gradually increase to A substantially relaxed stress-inducing crystalline layer 104 is formed thereon. The stress-inducing crystalline layer may include at least one atomic species having a covalent radius greater than that of germanium in combination with silicon.

In an illustrative embodiment, the stress-induced crystallization layer 104 may include silicon, germanium, and tin, where the germanium concentration may range from less than 1% to about 25%, and the tin concentration may range from about 0.1 to 25%.

In some embodiments, the germanium content can be selected to be much lower than 25%, for example, 1 to 10%, and the tin content can be selected to be in the range of about 0.1 to 10%.

In yet another embodiment, the stress-inducing crystallization layer 104 may include silicon and tin without substantially any germanium.

[0036]

The layer 104 may be a substantially relaxed layer, and has a diamond-like structure according to the crystallization template provided by the layer 102. The crystalline template is transferred to the layer 104 through the buffer layer 103. However, the lattice gap of the layer 104 may be different from the lattice gap of the layer 102. , Depending on the concentration of germanium and tin.

[0037]

As shown in FIG. 1a, the semiconductor device 100 can be formed according to the following process.

After the substrate 101 is provided, the substrate 101 may be a bulk silicon substrate with a layer 102 formed thereon or a silicon-on-insulation substrate. The thickness of the layer 102 may be suitable for an epitaxial growth process, and the buffer layer 103 may be formed by an epitaxial growth process. 105 is formed. In the epitaxial process 105, one or more non-silicon species may be deposited at different concentrations to form the buffer layer 103.

For example, the technology of forming a silicon/germanium buffer layer on the basis of germanium hydride (GeH4) is well established, and when it is deemed appropriate that no other atomic species such as tin is contained in the buffer layer 103, it can be used to form the layer 103.

In other embodiments, the buffer layer 103 can be formed on the basis of other atomic species such as tin. The buffer layer 103 can be made by using tin hydride (SnH4) as the precursor of the epitaxial growth process 105, where tin hydride can be Treat in the same way as germanium hydride.

[0038]

By appropriately depositing the material of the buffer layer 103, in terms of the lattice gap, the corresponding lattice structure can be gradually derived from the basic crystallization template of the layer 102, so that the layer 104 can finally be deposited as compared with the original crystal of the layer 102. The lattice gap has a semiconductor layer that increases the lattice gap and is substantially strain-free, that is, a relaxed semiconductor layer.

For this purpose, in the epitaxial growth process 105, if necessary, a desired amount of tin and a specific amount of a combination of germanium and silicon can be provided, and silicon is still the main material of the layer 104.

After the desired layer thickness is reached, the epitaxial growth process 105 can be interrupted, and then other epitaxial growth processes can be performed to deposit a substantially crystalline silicon layer on the layer 104.

In other embodiments, the epitaxial growth process 105 can be modified to facilitate subsequent deposition of doped silicon or undoped silicon, depending on requirements, wherein the relaxation layer 104 essentially serves as a crystallization template.

In this way, the silicon deposited thereon may have substantially the same crystalline structure, which is a strained crystalline structure compared to a naturally crystalline silicon layer such as layer 102.

Therefore, a certain degree of tensile strain can be generated.

[0039]

Figure 1b schematically shows the semiconductor device 100 in a further manufacturing stage.

As shown in the figure, another crystalline silicon layer 106 is formed in the layer 104 according to the above-mentioned epitaxial growth technique.

In this way, the layer 106 exhibits an intrinsic tensile strain, denoted as 107, so as to efficiently modify the mobility of the charge carriers in the layer 106.

In addition, a gate electrode 108 is formed on the layer 106 and is separated by a gate insulating layer 109.

The gate electrode 108 and the gate insulating layer 109 define the channel region 110 in the layer 106. As described above, the layer 106 exhibits a tensile strain 107 to increase the electron mobility in the channel region 110, for example.

As a result, the performance of the corresponding transistor element including the gate electrode 108 and the channel region 110 can be significantly improved, wherein on the basis of the epitaxial growth process 105, the degree of the tensile strain 107 can be efficiently adjusted and controlled.

Therefore, using the method of stress-induced crystalline layer 104 can provide an efficient strain generation mechanism for generating tensile strain in the silicon-based layer 106.

[0040]

FIG. 1c schematically shows a semiconductor device 100 according to another illustrative embodiment, in which a compressive strain can be generated in a specific region of the crystalline semiconductor layer.

In this embodiment, the stress-induced crystalline layer 104 can be directly formed on the crystalline layer 102, and the layer 102 is again used as a crystalilization template in the epitaxial growth process 105. Because the crystalline structure of the layer 102 is substantially maintained in the layer 104, the crystalline The template can now be configured so that the layer 104 itself grows into a substantially strained layer, thereby reducing its natural lattice gap, so that the channel region 110 can be a compressively strained region, thereby modifying the hole mobility, which can be beneficial in the trench A P-channel transistor is formed on the basis of the track region 110 and the gate electrode 108.

[0041]

Afterwards, starting from the device 100 in FIG. 1b or FIG. 1c, on the basis of establishing a complete MOS transistor formation technology, further manufacturing procedures can be continued, which will be described in more detail later with reference to FIGS. 2a to 2d.

[0042]

As previously explained, a moderately low concentration of atomic species with an increased covalent radius can sufficiently modify the corresponding lattice mismatch required to generate compressive or tensile strain, as described in Figures 1a to 1c.

Therefore, in some illustrative embodiments, additional techniques for introducing atomic species other than the epitaxial growth process 105 or alternatively to the epitaxial growth process 105 may be used, such as diffusion or implantation.

For example, an implantation process may be implemented to introduce, for example, tin atoms into the layer 104, thereby increasing the corresponding concentration, and thus introducing strain.

[0043]

FIG. 1d schematically shows an illustrative embodiment of a semiconductor device 100 including a first device region 150 and a second device region 160. A gate electrode 108 may be formed in the device region 150, and a second gate insulating device may be formed in the device region 160. A second gate electrode 118 is formed on the layer 119, wherein the second device region 160 can be covered by an implantation mask 121, which can be a resist mask.

In addition, the semiconductor device 100 undergoes ion implantation 120 to introduce tin in a localized manner.

For example, in the illustrated embodiment, it can be assumed that the layer 104 has been formed by the epitaxial growth process 105 (as described with reference to FIG. 1c), thereby providing the layer 104 with the intrinsic strain 107.

By further implanting tin ions near the gate electrode 108, the corresponding tin concentration can be increased, wherein a high dose such as 1016 to 1017 ions/cm^2 can be used to provide a moderately high additional tin atom concentration in the layer 104.

In order to obtain the implantation energy of substantially depositing tin ions in the layer 104 without excessively damaging the "template layer" 102, the implantation parameters of the process 120 can be selected based on a well-established simulation model.

[0044]

After the implantation process 120 is completed, the resist mask 121 can be removed, and then the device 100 can be subjected to a tempering process to recrystallize the damaged part of the layer 104 and place the implantation type substantially at the lattice position to rebuild the layer 104 Medium strain lattice.

As the tin concentration near the channel region 110 increases, a uniformly increased compressive strain can be generated therein, which also results in a more efficient modification of the charge carrier mobility.

[0045]

It should be understood that the above-mentioned embodiments are only illustrative in nature, and many modifications can be considered.

For example, before forming the gate electrodes 108 and 118 based on the mask 121, an implantation process 120 may be performed, so that the entire exposed portion of the layer 104 can receive an increased tin content.

In another exemplary embodiment, when the tin concentration introduced by the implantation process 120 is sufficient to produce the desired strain 107, the epitaxial growth process 105 can be omitted.

In yet another exemplary embodiment, the epitaxial growth process 105 can be performed on the basis of silicon and germanium, and the implantation process 120 can be used to locally introduce tin atoms to provide a method for fine-tuning the resulting strain.

For example, the first and second device regions 150 and 160 can represent regions of different transistor types, or can represent regions of different crystal grains, and these device regions have different strain requirements.

For example, in the high-sensitivity device area of a complex microprocessor, such as the static RAM area, it is desirable to have no strain or a relatively small strain; however, in the logic area, such as the CPU core, the stress is preferably increased to increase the operating speed of the CPU core.

As a result, since the effect of the atomic species having an increased covalent radius in the crystal structure, such as tin, is improved, the implantation technique can achieve an appropriate concentration to locally adjust the strain.

[0046]

2a to 2d, other exemplary embodiments of the present invention will now be described in more detail. In these embodiments, embedded strained semiconductor materials are formed in the drain and source regions of the transistor element to be adjacent to the channel The corresponding strain is induced in the zone.

[0047]

2a schematically shows a cross-sectional view of a semiconductor device 200 including a substrate 201 on which a crystalline semiconductor layer 202 is formed.

The substrate 201 may be a bulk silicon substrate or an SOI-like substrate, that is, the substrate 201 may be formed on a buried insulating layer (not shown), and a crystalline semiconductor layer 202 may be formed on the substrate 201.

The crystalline semiconductor layer 202 may be a silicon-based layer, that is, the layer 202 may include at least about 50% silicon.

In addition, the transistor element 250 may be formed in or on the crystalline semiconductor layer 202 in the initial manufacturing stage.

At this stage, the gate electrode 208 can be formed on the layer 202, and can include doped polysilicon or any other suitable material that can be provided on the layer 202, and can be separated by a gate insulating layer 209.

It should be understood that other methods or transistor structures can also be used in combination with the present invention. For example, the gate electrode 208 can represent a substitute or a dummy gate electrode, and the substitute or dummy gate electrode can be removed at a later stage of the process to provide Conductive material with improved electrical characteristics.

The gate electrode 208 can be "encapsulated" by the capping layer 230 and the individual spacer element 231, and the spacer element 231 can be separated from the gate electrode 208 by the individual spacer 232.

For example, the capping layer 230 and the spacer 231 may include any suitable dielectric materials such as silicon nitride, silicon oxynitride, and silicon dioxide, which can be used as etching and growth masks for etching processes and epitaxial growth processes to form embedded strain Semiconductor area.

The liner 232 is typically formed of a material having a high etch selectivity to the spacer 231.

For example, in establishing a complete etching process, a combination of silicon dioxide and silicon nitride can be efficiently used for the liner 232 and the spacer 231.

[0048]

The semiconductor device 200 shown in FIG. 2a can be formed according to the following steps.

After the substrate 201 is manufactured (if an SOI-like substrate is considered, the substrate 201 may include a buried insulating layer formed by high-level wafer bonding technology or other methods), the formation of the gate electrode 208 and the gate insulating layer 209 can be A deposition method and/or an oxidation method are used to form a suitable gate insulating material, and then a suitable gate electrode material is deposited.

Then, according to the established procedures, high-level lithography and etching techniques can be applied to pattern the corresponding layers, thereby forming the gate electrode 208 and the gate insulating layer 209, wherein, during the patterning process, the capping layer 230 Patterning can also be performed, and the capping layer 230 can be used as an anti-reflective coating (ARC), a hard mask layer, and the like.

Next, the liner material can be conformally deposited by plasma-assisted chemical vapor deposition (PECVD), and then the spacer layer is deposited, and then the spacer layer is patterned by an anisotropic etching process, thereby obtaining the spacer 231.

After that, the exposed residual portion of the liner 232 can be removed, and then the device 200 can be subjected to an anisotropic etching process 233 to form individual holes or recesses adjacent to the sealed gate electrode 208.

[0049]

FIG. 2b schematically shows the semiconductor device 200 in a further manufacturing stage, in which a recess or hole 234 is formed after the anisotropic etching process 233 is completed.

In the next step, the device 200 can be subjected to any pretreatment for preparing the device 200 for subsequent selective epitaxial growth processes.

For example, a suitable cleaning process may be implemented to remove contaminants and etching byproducts from the exposed surface of the device 200.

Afterwards, a selective epitaxial growth process 246 may be performed, in which, in an illustrative embodiment, the silicon-containing precursor, the germanium-containing precursor, and atoms having the same valence as silicon and germanium and larger than the covalent radius of germanium are included. Based on the types of precursors, an appropriate deposition environment can be established.

In an illustrative embodiment, a deposition can be generated on the basis of tin hydride (SnH_4) to provide a desired tin concentration in the deposition environment of the process 246.

As mentioned above, typically, in the selective epitaxial growth process, the process parameters such as pressure, temperature, carrier gas type, etc. are selected so that substantially no material is deposited on the surface of the dielectric layer, such as the capping layer 230 and the spacers. The surface of 231 is deposited on the exposed surface of the crystalline layer 202, and the deposited layer is used as a crystallization template, which substantially determines the crystalline structure of the epitaxial growth material.

In this illustrative embodiment, the material grown in at least a part of the recess 234 serves as a strained material, that is, the material should have the same crystalline structure as the basic template of the layer 202 and therefore substantially the same lattice gap. The presence of other atomic species with an increased covalent radius, such as tin, creates a highly strained material region.

In this way, due to the existence of the strained crystalline material, corresponding strain is also generated in the channel region 235 adjacent to the recess 234.

[0050]

As mentioned above, for silicon and germanium, due to the increase in the covalent radius of tin, the significant reduction of non-silicon atoms can be sufficient to obtain the corresponding strained semiconductor material during the epitaxial growth process 246.

Therefore, a moderately low concentration of, for example, tin, in the deposition environment in a concentration range of about 0.1 to 10%, can be regarded as appropriate for generating the required strain.

In other embodiments, on the basis of silicon and at least one other atomic species with an increased covalent radius, such as tin, the deposition environment of process 246 can be established without adding any germanium substantially, so as to improve other electrical characteristics such as PN junction. In terms of leakage current, etc., the effect of the substantial amount of germanium may be considered inappropriate, providing increased design flexibility.

In the epitaxial growth process 236, any suitable method can be used to control the tin and/or germanium concentration and therefore the silicon concentration.

For example, in some cases, because tin has a different diffusion behavior from germanium in the subsequent high-temperature process of the further processing of the device 200, it may be considered appropriate to bring tin atoms closer to the upper surfaces of the drain and source regions.

In other illustrative embodiments, tin can be provided near the area where the metal silicide is subsequently formed, where the content of germanium is significantly increased compared to the need to significantly increase the amount of germanium to produce the same amount of strain, but the subsequent silicidation process can cause significant limitations, the significantly reduced tin The number of atoms can increase the elasticity of producing metal silicides.

In still other embodiments, the final silicon layer may be formed on top of the strained silicon/germanium/tin layer or silicon/tin layer formed by the epitaxial growth process 246.

[0051]

FIG. 2c schematically shows the semiconductor device 200 after the epitaxial growth process 236 is completed.

Therefore, the device 200 includes a recessed strained semiconductor region 236 having a crystalline structure corresponding to the diamond structure of the silicon-based layer 202.

Due to the lattice mismatch, since the natural lattice gap of the crystalline structure in the region 236 is larger than the regular silicon gap, a compressive strain 207 is generated in the channel region 235 to improve the hole mobility during the operation of the transistor 250.

In addition, when a high germanium content is used, since germanium is partially or completely replaced by atomic species with an increased covalent radius, such as tin, the concentration of non-silicon atoms in the region 236 (the concentration is much lower than that previously encountered in conventional devices). Based on the accumulation limit value), a significantly increased strain 207 value can be obtained.

However, as mentioned above, the germanium and/or tin concentration in the region 236 can be varied in the depth direction to meet various device requirements.

For example, in the illustrated embodiment, a specific "overgrowth" can be formed to improve the subsequent silicidation process, thereby reducing the resulting contact resistance.

In addition, an upper region of the epitaxial growth material 236 can be provided, labeled 236A. By correspondingly increasing the tin concentration, the upper region can have a reduced germanium concentration but still provide a high degree of strain. However, the upper region can still have the same ratio The silicon/germanium region of strain 207 has a significantly lower concentration, thereby improving the flexibility in selecting an appropriate refractory metal for the subsequent silicidation process.

It should be understood that during the epitaxial growth process, any other suitable changes in the germanium and/or tin concentration in the region 236 can be produced.

[0052]

Then, after any implantation process for forming the drain and source regions, at least a part of the drain and source regions, when the spacer 231 has an appropriate size to obtain the desired lateral profile, the spacer 231 can be And the capping layer 230 is removed.

In other cases, the spacers 231 and the capping layer 230 can be removed, and the conventional process sequence and the intermediate implantation process can be performed to form spacer elements, so as to obtain the required drain and source regions defined by the design rules Complex side profile.

[0053]

Figure 2d schematically shows the semiconductor device 200 at a further manufacturing stage, in which the transistor 250 is substantially completed.

Therefore, the device 200 includes a sidewall spacer structure 237, which may include a plurality of individual spacer elements separated by individual spacers.

In addition, according to device requirements, the drain and source regions 239 have specific side doping profiles.

In addition, the metal silicide region 238 may be formed on the drain and source regions 239, and the corresponding metal silicide region 239 may be formed in the gate electrode 208.

As a result, due to the strain 207 generated by the region 236, the channel region 235 can be compressively strained, thereby significantly increasing the driving current capability of the transistor 250 (which may be a P-channel transistor).

Due to the provision of atomic species with an increased covalent radius in the region 236, a significant increase in strain 207 can be achieved compared to conventional devices including buried silicon/germanium regions.

[0054]

In addition, by appropriately designing the germanium and/or tin concentration design in the region 236, increased flexibility in forming the metal silicide region 238 can be provided.

For example, by reducing at least the germanium content in the upper region 236A but at the same time increasing the strain by increasing the tin concentration accordingly, a highly conductive nickel silicide can be formed in the region 238.

In this way, a significant increase in performance can be obtained, but at the same time, a high degree of compatibility with the conventional process for forming embedded silicon/germanium semiconductor structures can be maintained, and an additional degree of freedom in design can be obtained.

For this purpose, on the basis of achieving proper and desired introduction of non-silicon atoms, the corresponding epitaxial growth process can be adapted to include the provision of appropriate precursor materials such as tin hydride (SnH_4), in this case by straining the semiconductor region 236 The phase separation and crystal slippage enable the effective control of the generated strain, and substantially no stress release occurs.

[0055]

FIG. 3 schematically shows a cross-sectional view of a semiconductor device 300 according to other embodiments.

The semiconductor device 300 includes a first transistor 350 and a second transistor 360 formed on a substrate 301 based on a crystalline semiconductor layer 302.

Regarding the substrate 302 and the semiconductor layer 302, the same standards as described above with reference to the components 101, 102, 201, and 202 are applied.

In addition, in the described embodiment, the transistors 350 and 360 may have a sealed gate electrode 308 and are formed adjacent to the corresponding raised semiconductor regions 336 and 336A.

In other exemplary embodiments (not shown), the raised semiconductor regions 336 and 336A may not be provided, and only a part of the crystalline semiconductor layer 302 may be formed.

[0056]

The device 300 shown in FIG. 3 can be formed according to the process strategy described above with reference to FIGS. 2a to 2b. However, the transistors 350 and 360 can be represented as transistors that can receive different strains, because these transistors can Transistors in different crystal grain regions or transistors of different conductivity types can be shown.

For example, the first transistor 350 may be a P-channel transistor and the transistor 360 may be an N-channel transistor.

Therefore, in the corresponding etching process of forming individual holes or recesses to accommodate the semiconductor regions 336, 336A, the process uniformity can be improved. This is because when a type of transistor is exposed, the etching process does not require any hard mask. Completely cover another type of transistor.

Similarly, in the subsequent epitaxial growth process, due to any load reduction (which may also be a subject of the prior art), the uniformity across the substrate 301 can be improved. In this process, the first-type transistor is completely covered , And another type of transistor is exposed.

In the corresponding epitaxial growth process for forming the elevated semiconductor regions 336, 336A, a small amount of germanium and/or tin may be introduced to provide, for example, a "basic" strain 307 compatible with the performance of the second transistor 360.

In other illustrative embodiments, when the basic strain 307 is deemed inappropriate, the corresponding hole etching and subsequent epitaxial growth processes can be omitted.

In other cases, transistor 360 may represent a P-channel transistor in a critical device area, such as a static RAM area, which may receive a reduced amount of strain 307, while transistor 350 may require an increased amount of strain.

[0057]

In an illustrative embodiment, an implantation process 320 may be performed. In this process, the first transistor 350 is exposed and the second transistor 360 may be covered with a resist mask 321.

In the implantation process 320, tin can be injected into the region 336 to increase the tin concentration in the region 336. The increased covalent radius of tin produces more efficient lattice distortion, which can lead to an increase in the desired strain.

Because the implant-induced concentration may require a high concentration, such as about 1020 atoms/cm ^3 or higher, when the implantation process 320 is performed, the region 336 may be substantially amorphized.

Therefore, a tempering process can be performed to recrystallize the substantially amorphized region 336 based on the crystallization template 302, thereby forming a highly strained crystal structure in the region 336.

As a result, the initially present strain 307 can be increased to the value 307A, thereby obtaining the increased mobility required for the transistor 350.

After that, the further process described with reference to FIGS. 2a to 2d can be continued to complete the transistors 350 and 360.

[0058]

In other illustrative embodiments, when it is appropriate to use the concentration achieved by the implantation process 320 to generate the strain 307A, the implantation process 320 can be performed without first forming the regions 336 and 336A.

For example, in the region of highly sensitive devices, strain engineering based on strained semiconductor materials may not be appropriate for N-channel transistors, but may require "gentle" strain in the channel region of PMOS transistors.

In this case, the implantation process 320 can be applied before any drain and source regions are formed. In one embodiment, the implantation process 320 can additionally perform a pre-amorphization implantation process to facilitate subsequent introduction of doping to form the drain. And the source area.

In this way, high selectivity and performance improvement can be achieved, and it has a high degree of compatibility with current process technologies, and does not substantially affect the N-channel transistors substantially.

[0059]

Therefore, the present invention provides a strain-forming improvement technique by means of a strained or relaxed semiconductor material. In this technique, an atomic species with a larger covalent radius than germanium, such as tin, is introduced into individual crystalline silicon substrates. The semiconductor layer significantly reduces the risk of stress release caused by aggregation and lattice defects.

In the illustrated embodiment, an epitaxial growth process on a suitable precursor material such as tin hydride (SnH4) can be used to introduce atomic species with an increased covalent radius.

In addition, the use of other techniques such as implantation to introduce atomic species can achieve highly localized strain engineering, thereby providing highly flexible process and product design.

[0060]

The specific embodiments disclosed above are only for illustration. For those skilled in the advantages taught in this specification, it is obvious that the present invention can be modified and practiced in different but equal ways.

For example, the process steps proposed above can be performed in a different order.

In addition, it is not intended to limit the structure or design details shown in this specification, except as described in the claims below.

Obviously, the specific embodiments disclosed above can be changed or modified, and all these changes fall within the scope and spirit of the present invention.

Therefore, the protection sought in this specification is as set forth in the following claims.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS CN101300664A

1.

1、One method includes:

A crystalline structure based on silicon and at least one other atomic species having a covalent radius larger than that of germanium is formed in the crystalline semiconductor layer (104, 236, 336); and

The crystalline structure is used to generate strain (107, 207, 307) in the first region (110, 235, 335) of the semiconductor layer.

2.

2、The method of claim 1, wherein forming the crystalline structure comprises: epitaxially growing the silicon and the at least one other atomic species and depositing the silicon and the at least one other atom At least one of the types.

3.

3、The method of claim 1, wherein forming the crystalline structure comprises implanting the at least one other atomic species into the first portion of the crystalline semiconductor layer, and using the crystalline semiconductor layer as a crystal Template and recrystallize said part.

4.

4、The method of claim 3, further comprising forming a silicon/germanium crystal in the structure, and implanting the at least one other atomic species to adjust the amount of strain in the first region.

5.

5、The method of claim 3, further comprising implanting the at least one other atomic species into the second portion to generate a second strain (307A) in the second region of the crystalline semiconductor layer, the The second strain of is different from the first strain (307).

6.

6、The method of claim 1, further comprising forming a gate electrode (108, 208, 308) on the crystalline semiconductor layer, wherein the crystalline structure is formed with a pair of the gate electrode (108, 208, 308) 308) side offset.

7.

7、The method of claim 6, further comprising forming a recess (234) adjacent to the gate electrode (106, 206, 306), and forming at least a portion (236, 336) of the Crystal structure.

8.

8、A semiconductor device including:

The crystalline semiconductor layer (104, 236, 336) has a first stress inducing zone (335) including silicon and at least one other atomic species having a covalent radius greater than that of germanium.

9.

9、The semiconductor device according to claim 8, further comprising:

Gate electrodes (106, 206, 306) are formed on the crystalline semiconductor layer (104); and

The strained channel region (110, 235, 335), wherein the first stress inducing region is formed in the drain and source regions.

10.

10、The semiconductor device of claim 8, wherein the first stress inducing region includes tin.

11.

11、The semiconductor device of claim 10, wherein the first stress inducing region includes germanium.

12.

12、The semiconductor device according to claim 8, further comprising a second stress inducing region (335), said second stress inducing region comprising silicon and said at least one other atomic species, wherein, in said first The concentration of the at least one other atomic species in the stress inducing zone is different from the concentration of the at least one other atomic species in the second stress inducing zone (335).

[19] 中华人民共和国国家知识产权局

[51] Int. Cl.
H01L 21/20 (2006.01)
H01L 21/205 (2006.01)

[12] 发明专利申请公布说明书

[21] 申请号 200680040454.5

[43] 公开日 2008 年 11 月 5 日

[11] 公开号 CN 101300664A

[22] 申请日 2006.10.23
[21] 申请号 200680040454.5
[30] 优先权
[32] 2005.10.31 [33] DE [31] 102005051994.6
[32] 2006. 8.18 [33] US [31] 11/465,592
[86] 国际申请 PCT/US2006/041559 2006.10.23
[87] 国际公布 WO2007/053381 英 2007.5.10
[85] 进入国家阶段日期 2008.4.28
[71] 申请人 先进微装置公司
地址 美国加利福尼亚州
[72] 发明人 C·施特雷克 V·卡勒特 A·汉克
[74] 专利代理机构 北京纪凯知识产权代理有限公司
代理人 戈 泊

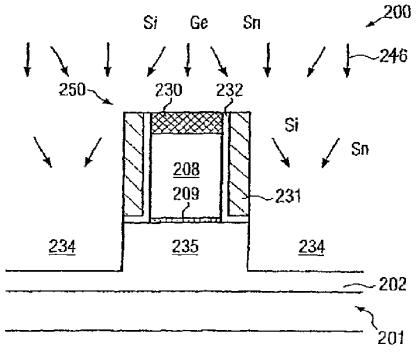
权利要求书 2 页 说明书 16 页 附图 4 页

[54] 发明名称

藉由使用包含具有高共价半径的原子的嵌入半导体层的用于硅基晶体管中工程应变的技术

[57] 摘要

藉由引入具增大共价半径(covalent radius)的原子种类(atomicspecies)，该原子种类可至少部分取代锗，可提供高效率应变机制，在该机制中因锗聚集(conglomeration)与晶格缺陷所引起的应力释放的风险可降低。具有增大半径的原子种类，例如锡，可利用基于氢化锡的外延生长技术来容易引入。



1、一种方法，包括：

在结晶半导体层（104, 236, 336）中形成以硅与至少一种具有共价半径大于锗的共价半径的其他原子种类为基础的结晶结构；以及

使用所述的结晶结构在所述的半导体层的第一区（110, 235, 335）中产生应变（107，207，307）。

2、如权利要求 1 所述的方法，其中，形成所述的结晶结构包括：外延生长所述的硅与所述的至少一种其他原子种类以及沉积所述的硅与所述的至少一种其他原子种类的其中至少之一。

3、如权利要求 1 所述的方法，其中，形成所述的结晶结构包括注入所述的至少一种其他原子种类至所述的结晶半导体层的第一部分中，以及使用所述的结晶半导体层作为结晶模板而再结晶所述的部分。

4、如权利要求 3 所述的方法，还包括在所述的结构中形成硅/锗晶体，以及注入所述的至少一种其他原子种类以调整所述的第一区中的应变量。

5、如权利要求 3 所述的方法，还包括注入所述的至少一种其他原子种类至第二部分中，以在所述的结晶半导体层的第二区中产生第二应变（307A），所述的第二应变与所述的第一应变（307）不同。

6、如权利要求 1 所述的方法，还包括在所述的结晶半导体层上形成栅电极（108，208，308），其中，所述的结晶结构形成有对所述的栅电极（108，208，308）的侧边偏移。

7、如权利要求 6 所述的方法，还包括形成邻接所述的栅电极（108，208，308）的凹陷（234），以及在所述的凹陷内形成至少部分（236，336）的所述的结晶结构。

8、一种半导体器件，包括：

结晶半导体层（104, 236, 336），具有包括硅与至少一种具有共价半径大于锗的共价半径的其他原子种类的第一应力引发区（335）。

9、如权利要求 8 所述的半导体器件，还包括：

栅电极（108, 208, 308），形成在所述的结晶半导体层（104）上；以及

应变沟道区（110, 235, 335），其中，所述的第一应力引发区形成在漏极和源极区中。

10、如权利要求 8 所述的半导体器件，其中，所述的第一应力引发区包括锡。

11、如权利要求 10 所述的半导体器件，其中，所述的第一应力引发区包括锗。

12、如权利要求 8 所述的半导体器件，还包括第二应力引发区（335），所述的第二应力引发区包括硅与所述的至少一种其他原子种类，其中，在所述的第一应力引发区中所述的至少一种其他原子种类的浓度与在所述的第二应力引发区（335）中所述的至少一种其他原子种类的浓度不同。

藉由使用包含具有高共价半径的原子的嵌入半导体层的用于硅基晶体管中工程应变的技术

技术领域

本发明大致关于形成集成电路，且更详细地说，关于藉由使用嵌入硅/锗而形成具有应变沟道区（strained channel region）的不同晶体管类型，以提高电荷载体在晶体管的沟道区中的移动性（mobility）。

背景技术

集成电路的制造，需在给定的芯片区域上，依据特定电路布局形成大量电路元件。大抵上，目前应用许多工艺技术，其中，对于复杂电路诸如微处理器、储存芯片等，CMOS 技术由于在操作速度及/或电力消耗及/或成本效率方面有极优的性能，而为目前最有前景的方法。使用 CMOS 技术制造复杂集成电路时，数百万的晶体管，亦即 N-沟道晶体管与 P-沟道晶体管形成在包含结晶半导体层的衬底上。MOS 晶体管，不管其为 N-沟道晶体管或 P-沟道晶体管，包含所谓 PN 结（junction），是由高度掺杂的漏极与源极区接口所形成，在该漏极与源极区之间设有相反掺杂的沟道区。

沟道区的导电度，亦即导电沟道的驱动电流能力，是由形成在该沟道区上且以薄绝缘层分隔的栅极所控制。导电沟道一旦形成，由于施加适当控制电压在栅电极（gate electrode），沟道区导电度取决于掺杂物浓度、多数电荷载体移动性、以及晶体管宽度方向上沟道区给定延伸时源极与漏极区间距离（亦称为沟道长度）。因此，施加适当控制电压在栅电极，并结合在绝缘层下快速产生导电沟道的能力，整个沟道区导电性实质上决定了 MOS 晶体管的性能。所以，缩短沟道长度使沟道电阻系数降低，对达成提高集成电路操作速度提供了沟道长度的主要设计标准。

然而，晶体管尺寸持续缩小，许多与此有关的问题必须提出，以便不会过度抵消稳定地缩短 MOS 晶体管沟道长度所得的优点。此方面

的一个主要课题为发展增进的光刻技术（photolithography）与蚀刻策略，以便为新一代器件可靠而再现性地制出具关键尺寸的电路元件，例如晶体管的栅电极。再者，漏极与源极区要求在垂直方向与侧边方向具有高精细掺杂物分布（profile），以提供低的片和接触电阻系数（sheet and contact resistivity），以及所欲沟道控制能力。此外，考量漏电流控制，关于栅极绝缘层的 PN 结垂直位置亦为关键设计标准。所以，缩短沟道长度通常亦需要减小关于由栅极绝缘层与沟道区所形成接口的漏极与源极区深度，因而需要精巧注入技术。依据其他方法，外延生长区（称为升高漏极与源极区）形成有对栅电极的特定偏移（offset），以增加该升高漏极与源极区的导电性，同时维持关于栅极绝缘层的浅 PN 结。

因为关键尺寸，亦即晶体管栅极长度持续缩小，所以必须顺应与可能地新开发关于以上所述工艺步骤的高复杂工艺技术，有人提出对给定沟道长度，藉由增加沟道区中电荷载体移动性而亦提高晶体管元件的沟道导电性，藉以提供达成改善性能的可能性，使与未来技术节点的进步可相匹配，并避免或至少延迟许多与器件尺寸缩放（scaling）有关的上述工艺的调适。增加电荷载体移动性的一个有效机制为修改沟道区的晶格结构，例如藉在沟道区附近产生拉伸或压缩应力而在沟道区产生相应应变，使电子与空穴的移动性分别受到修改。例如，在沟道区产生拉伸应变增加电子移动性，而可获得 50%或更高的移动性增加，视拉伸应变大小与方向而定，此移动性增加依序可直接转化成相应导电性提高。另一方面，沟道区的压缩应变可增加空穴移动性，因而提供改善 P 型晶体管性能的可能性。对更进一步世代的器件而言，将应力或应变工程导入集成电路制造中，是极有前景的方法，因为，例如经应变硅（strained silicon）可视为「新」类型半导体材料，其可使快速强大的半导体器件制造成为可能而无需使用昂贵半导体材料，同时许多已建立完备的制造技术仍可使用。

因此，有人提出在沟道区中或在其下导入例如硅/锗层或硅/碳层，以产生拉伸或压缩应力，而可导致相应应变。藉由在沟道区中或在其下导入应力产生层，可相当程度地提高晶体管性能，所以投入相当大努力将形成相应应力层实施在习知与众所公认的 MOS 技术中。例如，

发展其他外延生长技术并加入制造流程中，以在沟道区中或在其下适当位置形成含锗或含碳应力层。

其他方法是应用例如藉由覆盖层（overlaying layer）、间隔件元件等来产生外部应力，以在沟道区内产生所欲应变。然而，藉施加特定外部应力来产生沟道区中应变的工艺，可能遇到外部应力无效率地转化成沟道区中应变的问题。所以，虽然以上所述在沟道区内需要额外应力层的方法，在工艺复杂性方面具有优势，但是应力转移机制的效率可能受该工艺与器件特性所影响，而可能造成减小一种晶体管类型的性能改善。

另一方法是藉由在晶体管漏极与源极区中形成应变硅/锗层，提高 PMOS 晶体管中空穴移动性，其中，经压缩应变的漏极区与源极区在邻接硅沟道区中产生单轴应变。为此目的，PMOS 晶体管的漏极与源极区选择性地凹陷，而 NMOS 晶体管是经遮蔽，然后藉由外延生长使硅/锗层选择性地形成在 PMOS 晶体管中。此技术对 PMOS 晶体管以及因此整个 CMOS 器件的性能提高，提供显著好处。

所以，利用嵌入式半导体材料尤其是硅/锗的工程应变，视所欲功效提供作为应变或松弛层，已证明是种增加高阶硅基晶体管的器件性能的有力方法。然而，结果，个别沟道区所引发的应变程度，取决于基本硅与嵌入半导体化合物间的晶格不匹配量。对硅/锗而言，目前建立的外延生长技术，锗最大浓度限制为约 25%，否则可能发生锗聚集，转而可能导致在相应嵌入半导体化合物材料中不希望的应力解除，由此亦降低个别沟道区的应变。

综观上述情况，对利用嵌入半导体材料来有效增加应变的改善技术，同时实质上避免或至少减少一或多个以上所述问题，实有其需求。

发明内容

以下提出本发明的简单概述，用来初步了解本发明的一些态样。此概述并非本发明的详尽综论，其无意用来验证本发明的关键或重要元件，或用来描绘本发明的范围。其唯一目的是以简化形式呈现一些观念作为稍后更详细说明的引言。

大抵而言，本发明是关于一种用于在结晶半导体层的特定区中产

生应变的技术，为达此目的，在此技术中采用硅基（silicon-based）晶格（亦即具有似钻石晶格结构的晶格）与本身具增大晶格间隙的半导体化合物间的晶格不匹配（lattice mismatch）。对应技术惯用在相当高阶硅基 MOS 晶体管元件中产生应变硅沟道，其中，如前所述，由此机制所得应变量尤其显著受限在可成功使用于目前所建立外延生长技术的有限锗浓度。所以，本发明中，除锗之外可额外使用或是与锗选一使用的方式，可使用于似硅结晶结构中，对键结（bonding）特性具有显著增加共价半径的其他原子种类，藉以使在个别硅基结晶结构中有大幅减少非硅原子数及高度晶体畸变（distortion）成为可能。本发明的例释实施例中，由于相较于硅与锗，锡原子具有相同的原子价（valence），而且亦展现显著较大共价半径，所以锡（Sn）可作为锗的额外添加物或替代物。

依据本发明的一个例释实施例，一种晶体管器件包括衬底，该衬底上形成有具有似钻石结晶结构的结晶半导体层。该结晶半导体层包括应力引发区（stress-inducing region），该应力引发区包含硅与具有与该结晶结构中的硅相同的原子价的其他原子种类，该其他原子种类具有共价半径大于锗的共价半径。此外，该晶体管器件包括形成在该结晶半导体层上的栅电极（gate electrode），以及应变沟道区。

依据本发明的另一例释实施例，一种半导体器件包括结晶半导体层，该结晶半导体层具有包含硅与锡的第一部分，以在该结晶半导体层中形成第一应变区。

依据本发明的又一例释实施例，一种方法包括在结晶半导体层中形成以硅与至少一种具有共价半径大于锗的共价半径的其他原子种类为基础的结晶结构。此外，该方法包括使用该结晶结构以在该半导体层的第一特定区中产生应变。

附图说明

参照附图与以下说明可了解本发明，其中，相似元件符号代表相似元件，且其中：

图 1a 至 1d 概要显示依据本发明的例释实施例，在以硅与以可内建在硅钻石结构中且相较于锗具有增大共价半径的其他原子种类为基

础的结晶半导体层中，形成应变区的不同制造阶段期间的半导体器件的截面图；

图 2a 至 2d 概要显示依据本发明的又一些例释实施例，在形成接收嵌入应变半导体区的晶体管器件以在个别沟道区中产生压缩应变的不同制造阶段期间的截面图；以及

图 3 为依据本发明的另一例释实施例，概要显示半导体器件的截面图，该半导体器件包括接收不同锡量以产生不同应变大小的不同晶体管元件。

本发明可很容易做各种修改与变化，其特定实施例以附图举例的方式显示，并在本文中做详细阐述。然而，应明了，本文中特定实施例的阐述并无意用来限制本发明在所揭示的特定型式，反而是意图用来涵盖所有落在如后附权利要求书所界定本发明精神与范围内的修改、等同与变化。

具体实施方式

以下说明本发明的例释实施例。为清楚起见，并非所有实际施行的特征皆描述在本说明书中。当然，应可理解，在任何此等实际施行的开发中，必须决定许多特定实施例以达成开发者特定目的，诸如依从与系统有关及商业有关的限制，该些目的从一个实施例至另一实施例会有不同。此外，将可理解，此等开发可能复杂且耗时，但对该些了解本发明揭示内容的熟悉此项技术者而言，此等开发实为例行性的工作。

现将参照附图对本发明进行说明。图中各种结构、系统与器件为概要性叙述，仅用在解释，以便不会因熟悉此项技术者所周知的细节而模糊本发明。尽管如此，本说明书仍包含附图，以便用来说明与解释本发明的例释实施例。应明了本文所使用的字与片语，并将该些字与片语解释成具有符合该些字与片语为熟悉该相关领域者所理解的意义。无特别的术语或片语定义，亦即，异于该些熟悉本领域者所理解的通常与习惯意义的定义，隐含在本文术语或片语的一致用法中。当术语或片语意含特殊意义时，亦即，除熟悉本领域者所理解外的其他意义时，此特殊定义将以直接且明确提供该术语或片语特殊定义之下

的定义方式在本说明书中进行说明。

大抵上，本发明专注在利用相较于非应变硅晶体而具有不同晶格间隙的钻石型晶格结构的应变或松弛半导体结构来增进应变引发机制。如前所述，在硅基半导体器件的适当位置内设应变或松弛硅/锗层的机制，提供了有效率工程应变技术，以相应提高电荷载体移动性，尤其是在相当高阶 MOS 晶体管器件的沟道区内。该些技术依赖于外延生长工艺，在此工艺中可形成应变或松弛硅/锗层，视器件需求而定。

此外，最近发展局部选择性外延生长技术，可有效抑制显著材料沉积在介电质表面，然却有效率地沉积硅、硅/锗等于暴露的硅或似硅表面。例如，若硅/锗层沉积在结晶硅层上，则可沉积硅/锗材料，以使具有实质上如底层结晶「模板（template）」一样的晶格间隙，而形成应变硅/锗层，因为相较于纯硅晶体，未受扰乱的硅/锗晶体可有稍微增大的晶格间隙。硅/锗层与硅层的晶格间隙差异取决于锗浓度。所以，产生在硅/锗层的应变量亦取决于锗浓度。然而，如前所述，依目前所用外延生长技术，最大锗浓度可高达约 25 至 30%，但较高的浓度实际上可能导致锗聚集，转而可能导致缺陷率增加，使得初始应变硅/锗层松弛化。

依据本发明，所欲晶格不匹配程度以及因此应变，可在具有比锗显著较大共价半径的原子种类基础上予以调整，其中，在一些例释实施例中，关于似钻石结晶结构中的共价键结结构，所考虑使用的原子种类其原子价实质上与硅或锗相同。在一例释实施例中，具有共价半径 1.04 埃（Å）的锡可作为适当的原子种类。例如，具有共价半径 1.17 埃的硅可与具有共价半径 1.22 埃的锗组合使用，其中，另外可使用一定量的锡以产生显著增大的晶格不匹配。因为硅与锡间共价半径差异显著大于硅与锗间共价半径差异，所以利用减少非硅原子数目可达成对整个晶格结构较显著的作用。如此一来，锗浓度可维持在阈值约 25% 以下，且藉由加入一定量锡仍可得到晶格不匹配提高。

再者，在一些例释实施例中，硅可与锡组合使用而无需添加任何锗，藉此提供适度高程度的晶格修改（lattice modification）有显著减少非硅原子数目。例如，在一些实施例中，除了以外延生长方式引入锡之外，亦考虑利用其他技术例如注入来引入一定量锡，或此二方式择

一使用。尽管如此，但因减少锡原子数目可对晶格畸变产生显著贡献，甚至利用目前注入技术所能达到的原子浓度可充分产生特定应变或至少细调晶格不匹配，所以藉此达到该应变程度。因为离子注入为建立完备的技术，以光刻技术所形成的刻胶掩模（resist mask）为基础，可在室温进行离子注入，因此锡的相应引入可用高度有效率与甚至高度局部方式来达成，藉此提供工艺技术及器件设计额外弹性。例如，可利用目前施行的注入技术来达成浓度约为 1020 锡原子/立方公分，使可进行相应硅/锡或硅/锗/锡结晶结构中应变的有效率调整或控制。

以下详细说明可参考为本发明原理的特定应用，亦即，引入具有增大共价半径的原子种类以在特定结晶半导体区产生应变。然而，应明了，并无意对特定晶体管结构例如似 SOI 晶体管、本体式（bulk）器件、具有升高漏极与源极区的晶体管等做任何限制，除非在实施方式与权利要求书中对此特别限制有做说明。

参照图 1a 至 1d、图 2a 至 2d 与图 3，本发明进一步的例释实施例现将作更详细阐述。

图 1a 概要显示在初期制造阶段时，半导体器件 100 的截面图。半导体器件 100 包括衬底 101，该衬底 101 可表任何带有半导体层 102 的适当衬底，在衬底 101 中或其上可形成电路元件例如晶体管、电容器、电阻器等。例如，衬底 101 可表本体式半导体衬底如硅衬底，或可表任何绝缘衬底如似 SOI 衬底，其中，半导体层 102 可形成在埋入式绝缘层（未图示）上。应明了，虽然本发明结合如典型上以高阶 CMOS 技术，包括具 50 纳米（nm）和甚至更小栅极长度的晶体管所制造的高度缩小化 MOS 晶体管，其具有相当大的优点，但本发明原理亦可应用至较非关键应用上，以便使现有设计可达到显著的性能增加。

半导体层 102 可为硅基结晶半导体层，其中硅基一词是理解成包含硅浓度至少为原子 50%的材料层。在例释实施例中，半导体层 102 可表掺杂硅层，如典型上用于高度复杂集成电路，而该集成电路具有栅极长度在上述特定范围内的晶体管元件的掺杂硅层。在层 102 上可进一步形成实质上结晶层 103，该结晶层 103 可表所谓的缓冲层，在此结晶层中，结晶不匹配以及因此特定原子种类诸如锗、锡等的浓度可逐渐增加，以使在其上形成实质上松弛的应力引发结晶层 104，此应力

引发结晶层可包含至少一个具有共价半径大于锗共价半径的原子种类与硅相组合。在一例释实施例中，应力引发结晶层 104 可包含硅、锗与锡，其中，锗浓度范围可从低于 1%至约 25%，而锡浓度范围可为约 0.1 至 25%。在一些实施例中，可选择锗含量远低于 25%，例如 1 至 10%，而锡含量可选择在约 0.1 至 10%范围内。在又一实施例中，应力引发结晶层 104 可包含硅与锡而实质上无任何锗。

层 104 可表实质上松弛层，具有依层 102 所提供结晶模板的钻石似结构，该结晶模板经缓冲层 103 转移至层 104，然而，其中层 104 晶格间隙可异于层 102 晶格间隙，端视锗与锡浓度而定。

如图 1a 所示，可依据下列工艺形成半导体器件 100。提供衬底 101 后，衬底 101 可表其上形成有层 102 的本体式硅衬底或绝缘层上硅衬底，层 102 厚度可适于外延生长工艺，缓冲层 103 可藉由外延生长工艺 105 予以形成，在此外延工艺 105 中，一或多个非硅种类可用不同浓度进行沉积以形成缓冲层 103。例如，在氢化锗（GeH4）基础上形成硅/锗缓冲层的技术已建立完备，并且当认为在缓冲层 103 中无另外原子种类例如锡是适当时，可用来形成层 103。在其他实施例中，可在其他原子种类例如锡的基础上形成缓冲层 103，缓冲层 103 可藉由以氢化锡（SnH4）作为外延生长工艺 105 的前体来制成，其中，氢化锡可以如氢化锗的相同方式处理。

藉由适当沉积缓冲层 103 的材料，就晶格间隙而言，相应晶格结构可逐渐地自层 102 的基本结晶模板中衍生出来，使得层 104 最后可沉积成相较于层 102 的原始晶格间隙，具有增大晶格间隙而实质上无应变的半导体层，亦即松弛的半导体层。为达此目的，在外延生长工艺 105 中，若有需要，则可提供所欲量的锡及个别量的锗与硅组合，而硅仍为层 104 的主要材料。达成所欲层厚度后，可中断外延生长工艺 105，然后可进行其他外延生长工艺以在层 104 上沉积实质上结晶硅层。在其他实施例中，可修改外延生长工艺 105 以利后续沉积掺杂硅或未掺杂硅，视需求而定，其中，实质上松弛层 104 是作为结晶模板。如此一来，沉积在其上的硅可具有实质上相同的结晶结构，该结晶结构相较于自然结晶硅层例如层 102，为应变结晶结构。因此，可产生特定程度的拉伸应变。

图 1b 概要显示在进一步制造阶段时的半导体器件 100。如图中所示，依据上述外延生长技术在层 104 中形成另一结晶硅层 106。如此一来，层 106 呈现本质拉伸应变，表示为 107，藉以有效率地修改层 106 中电荷载体移动性。此外，层 106 上形成有栅电极 108，并且以栅极绝缘层 109 分隔。栅电极 108 组合栅极绝缘层 109 在层 106 中界定出沟道区 110，如前所述，层 106 呈现拉伸应变 107，藉以增加例如沟道区 110 中电子移动性。结果，相应晶体管元件包括栅电极 108 与沟道区 110 的性能可显著提高，其中在外延生长工艺 105 基础上，拉伸应变 107 程度可有效率地予以调整与控制。因此，利用应力引发结晶层 104 的方式，可提供产生硅基层 106 中拉伸应变的有效率应变产生机制。

图 1c 概要显示依据另一例释实施例的半导体器件 100，在此器件中，在结晶半导体层的特定区域中可产生压缩应变。该实施例中，应力引发结晶层 104 可直接形成在结晶层 102 上，层 102 在外延生长工艺 105 中再次作为结晶模板，因为层 102 的结晶结构在层 104 中实质上维持着，所以该结晶模板现可已组态过，使得层 104 本身生长成实质上应变层，藉以降低其自然晶格间隙，使得沟道区 110 可为压缩应变区，藉以修改空穴移动性，而可利于在沟道区 110 与栅电极 108 基础上形成 P-沟道晶体管。

之后，自如图 1b 或图 1c 中器件 100 开始，在建立完备的形成金氧半晶体管技术基础上，可继续进一步的制造程序，稍后将参照图 2a 至 2d 作更详细的说明。

如前所说明，具有增加共价半径原子种类的适度低浓度，可充分修改产生压缩或拉伸应变所需的相应晶格不匹配，如图 1a 至 1c 所述者。所以，在一些例释实施例中，可使用除外延生长工艺 105 外的额外或可与外延生长工艺 105 择一使用的其他引入原子种类技术，例如扩散或注入。例如，可实施注入工艺以引入例如锡原子进入层 104，藉以增加相应浓度，以及因此引入应变。

图 1d 概要显示包括第一器件区 150 与第二器件区 160 的半导体器件 100 例释实施例，在器件区 150 中可形成有栅电极 108，而在器件区 160 中可在第二栅极绝缘层 119 上形成第二栅电极 118，其中，第二器件区 160 可用注入掩模 121 予以覆盖，掩模 121 可为刻胶型掩模。此

外，半导体器件 100 进行离子注入 120 以局部方式引入锡。例如，在所示实施例中，可假设利用外延生长工艺 105 已形成层 104（参照图 1c 所说明），藉以提供具有本质应变 107 的层 104。藉由在栅电极 108 附近进一步注入锡离子，相应锡浓度可予以增加，其中，可使用高剂量例如 1016 至 1017 离子/平方公分，以在层 104 内提供适度高的额外锡原子浓度。为了获得在层 104 内实质上沉积锡离子的注入能量，而不过度损害「模板层」102，可依据已建立完备的模拟模型来选择工艺 120 的注入参数。

注入工艺 120 完成后，可除去刻胶掩模 121，然后器件 100 可接着进行回火工艺，以使层 104 中受损部分再结晶及实质上在晶格位置放置该注入种类，以重建层 104 中应变晶格。由于沟道区 110 附近锡浓度增加，因而在其内可产生均匀增加的压缩应变，亦藉而造成更有效率地修改电荷载体移动性。

应明了，上述实施例只具有例释性质，可考虑进行许多的修改。例如，以掩模 121 为基础在形成栅电极 108 与 118 之前，可进行注入工艺 120，使得层 104 整个曝光部分可接收增加的锡含量。又一例释实施例中，当以注入工艺 120 引入的锡浓度足够产生所欲应变 107 的程度时，可省略外延生长工艺 105。又一其他例释实施例中，可在硅与锗基础上进行外延生长工艺 105，而注入工艺 120 可用来局部引入锡原子，藉以提供细调最后所得应变的方法。例如，第一与第二器件区 150、160 可表不同晶体管类型的区域，或可表不同晶粒区域，该些器件区有不同应变程度需求。例如，在复杂微处理器的高灵敏度器件区，例如静态 RAM 区，希望没有应变或有相当小的应变；然而在逻辑区，例如 CPU 核心，优选为应力增加，以提高 CPU 核心的运作速度。结果，由于结晶结构上具有增加共价半径的原子种类例如锡的效果提高，注入技术可达到适当的浓度，以便局部调整应变。

参照图 2a 至 2d，本发明的其他例释实施例现将作更详细说明，在该些实施例中，嵌入应变半导体材料形成在晶体管元件的漏极与源极区中，以在邻接沟道区中引发相应应变。

图 2a 概要显示包括衬底 201 且衬底 201 上形成有结晶半导体层 202 的半导体器件 200 截面图。衬底 201 可表本体式硅衬底或似 SOI 衬底，

亦即，衬底 201 可形成在埋入式绝缘层（未图示）上，在衬底 201 上形成有结晶半导体层 202。结晶半导体层 202 可表硅基层，亦即，层 202 可包含至少约 50%硅。此外，在初期制造阶段，晶体管元件 250 可形成在结晶半导体层 202 中或上。在该阶段，栅电极 208 可形成在层 202 上，并可包含掺杂多晶硅或任何其他可设在层 202 上的适当材料，可用栅极绝缘层 209 分隔。应明了，亦可使用其他方法或晶体管结构与本发明相组合，其中，例如栅电极 208 可表示取代品或假栅电极，该取代品或假栅电极可在工艺稍后阶段移除，以提供具提高电气特性的导电性材料。栅电极 208 可由封盖层 230 与个别间隔件元件 231 所「包覆（encapsulated）」，而间隔件元件 231 可用个别衬垫 232 而与栅电极 208 分隔。例如，封盖层 230 与间隔件 231 可包含任何适当介电材料例如氮化硅、氧氮化硅与二氧化硅，可作为蚀刻工艺与外延生长工艺的蚀刻与生长掩模，以形成嵌入应变半导体区。衬垫 232 典型上由对间隔件 231 具有高蚀刻选择性的材料所形成。例如，在建立完备的蚀刻程序上，二氧化硅与氮化硅的组合可有效率地用于衬垫 232 与间隔件 231。

如图 2a 所示的半导体器件 200 可依据下列步骤予以形成。制造衬底 201 后（若考虑似 SOI 衬底，衬底 201 可包括以高阶晶片键结技术或其他方法来形成埋入式绝缘层），栅电极 208 与栅极绝缘层 209 的形成，可利用沉积法及/或氧化法形成适当栅极绝缘材料，接着进行适当栅电极材料的沉积。然后，依据建立完备的程序，可应用高阶平版印刷技术及蚀刻技术来图案化相应的层，藉以形成栅电极 208 与栅极绝缘层 209，其中，在进行图案化工艺时，封盖层 230 亦可进行图案化，该封盖层 230 可作为抗反射涂层（ARC）、硬质掩模层等。下一步，藉由等离子体辅助化学气相沉积（PECVD）可共形地沉积衬垫材料，接着沉积间隔件层，然后以各向异性蚀刻工艺进行间隔件层图案化，因而得到间隔件 231。之后，可移除衬垫 232 经暴露的残留部分，然后器件 200 可进行各向异性蚀刻工艺 233，以形成个别孔洞或凹陷邻接密封栅电极 208。

图 2b 概要显示在进一步制造阶段中的半导体器件 200，其中，在各向异性蚀刻工艺 233 完成后形成凹陷或孔洞 234。下一步，器件 200

可进行任何制备器件 200 的预处理，以便进行后续选择性外延生长工艺。例如，可实施适当清洗工艺以从器件 200 的暴露表面移除污染物与蚀刻副产物。之后，可进行选择性外延生长工艺 246，其中，在一个例释实施例中，在含硅前体、含锗前体以及包括具有如硅与锗相同原子价并比锗共价半径大的原子种类的前体基础上，可建立适当沉积环境。在一个例释实施例中，在氢化锡（SnH4）基础上可产生沉积，以在工艺 246 沉积环境中提供所欲锡浓度。如前所述，典型上，在选择性外延生长工艺中，工艺参数例如压力、温度、载气种类等经选择，以使实质上无材料沉积在介电层表面例如封盖层 230 与间隔件 231 的表面，而是在结晶层 202 的暴露表面上产生沉积，藉而利用此沉积层作为结晶模板，该模板实质上决定了外延生长材料的结晶结构。在该例释实施例中，在凹陷 234 至少一部分中生长的材料供作为应变材料，亦即，该材料应具有如层 202 基本模板一样的结晶结构以及因此实质上一样的晶格间隙，由于锗与其他具有增加共价半径的原子种类例如锡的存在，因而产生高度应变材料区。如此一来，由于应变结晶材料存在，在邻接凹陷 234 处的沟道区 235 中亦产生相应的应变。

如前所述，对硅与锗而言由于锡共价半径增加，非硅原子的显著减少可足够获得在外延生长工艺 246 时的相应应变半导体材料。因此，对产生所需应变而言，沉积环境中浓度范围约 0.1 至 10%的例如锡的适度低浓度，可视为适当。其他实施例中，在硅与至少一个其他具有增加共价半径的原子种类例如锡基础上，可建立工艺 246 的沉积环境，而实质上无加入任何锗，藉此当对其他电气特性例如 PN 结漏电流等而言，锗实质数量的影响也许认为不适当时，提供增加的设计弹性。在外延生长工艺 236 中，可用任何适当方法控制锡及/或锗浓度以及因此硅浓度。例如，一些情况中，因为在器件 200 进一步工艺的后续高温工艺中，锡不同于锗的扩散行为，使锡原子更靠近漏极与源极区上表面，可认为适当。其他例释实施例中，可在后续形成金属硅化物的区域附近提供锡，其中相较于需要显著增加锗含量以产生相同应变量然而对后续硅化工艺可造成显著限制而言，显著减少的锡原子数可增加产生金属硅化物的弹性。又在其他实施例中，可在由外延生长工艺 246 所形成的应变硅/锗/锡层或硅/锡层顶部上形成最终硅层。

图 2c 概要显示外延生长工艺 236 完成后的半导体器件 200。所以，器件 200 包括具有对应于硅基层 202 的钻石结构的结晶结构的凹陷应变半导体区 236。由于晶格不匹配，因区 236 中结晶结构的自然晶格间隙大于规则硅间隙，因此沟道区 235 中产生压缩应变 207，藉以提高晶体管 250 操作时的空穴移动性。此外，当使用高锗含量时，由于锗被具有增加共价半径的原子种类例如锡所部分或完全取代，因此在区 236 中非硅原子浓度（该浓度远低于习知器件中先前所遭遇聚积的限制值）的基础上，可得到显著增加的应变 207 数值。然而，如前所述，区 236 中锗及/或锡浓度在深度方向可变化以符合各种器件需求。例如，在所示实施例中，可形成特定「过度生长」以提高后续硅化工艺，藉以降低产生的接触电阻。此外，可提供外延生长材料 236 的上部区，标示为 236A，藉由相应增加锡浓度，该上部区可具有降低的锗浓度但仍提供高度的应变，然而，该上部区可仍具有比产生相同应变 207 量的硅/锗区显著低的浓度，藉以提高在选择后续硅化工艺的适当难熔金属时的弹性。应明了，在外延生长工艺进行中，可产生区 236 中锗及/或锡浓度的任何其他适当变化。

然后，能在形成漏极与源极区，至少一部分漏极与源极区的任何注入工艺之后，当间隔件 231 具有适当尺寸以得到所欲侧边外形（lateral profile）时，可将间隔件 231 与封盖层 230 移除。其他情况中，可移除间隔件 231 与封盖层 230，以及可进行习知工艺序列以与中间的注入工艺形成间隔件元件，而得到以设计规则所界定漏极与源极区所需的复杂侧边外形。

图 2d 概要显示在进一步制造阶段时的半导体器件 200，其中实质上完成晶体管 250。所以，器件 200 包括侧壁间隔件结构 237，该结构可包括多个个别的间隔件元件用个别衬垫分隔。此外，依据器件需求，漏极与源极区 239 具有特定侧边掺杂外形。此外，金属硅化物区 238 可形成在漏极与源极区 239 上，而相应金属硅化物区 239 可形成在栅电极 208 中。结果，由于区 236 所产生的应变 207，沟道区 235 可予以压缩地应变，藉以显著增加晶体管 250（可为 P-沟道晶体管）的驱动电流能力。由于在区 236 中提供具有增加共价半径的原子种类，相较于包括埋入式硅/锗区的习知器件，可达成应变 207 的显著增加。

此外，藉由适当设计区 236 中的锗及/或锡浓度设计，可提供形成金属硅化物区 238 的增加弹性。例如，藉由降低至少上部区 236A 中锗含量但同时藉由相应地提高锡浓度来增加应变，则高导电性镍硅化物可形成在区 238 中。如此一来，可获得性能显著增加，但同时可维持与形成嵌入硅/锗半导体结构的习知工艺的高度相容性，并可获得在设计方面的额外自由度。为了此目的，在可达成适当与所欲非硅原子的引入基础上，可使相应外延生长工艺适合于包括提供适当前体材料例如氢化锡（SnH4），此情况藉由应变半导体区 236 内的相分离与晶体滑移而使有效率地控制产生的应变，实质上未产生任何应力释放。

图 3 概要显示依据其他实施例的半导体器件 300 的截面图。半导体器件 300 包括形成在衬底 301 上，以结晶半导体层 302 为基础的第一晶体管 350 与第二晶体管 360。关于衬底 302 与半导体层 302，应用如前参照组件 101、102、201 与 202 所述的相同标准。此外，在所述实施例中，晶体管 350、360 可具有密封栅电极 308，并邻接相应升高半导体区 336、336A 而形成。在其他例释实施例中（未图示），可不设升高半导体区 336、336A，并可仅表结晶半导体层 302 的一部分。

如图 3 所示的器件 300，可依据如前参照图 2a 至 2b 所述的工艺策略予以形成，然而，其中，晶体管 350、360 可表示为可接收不同应变大小的晶体管，因为该些晶体管可表在不同晶粒区的晶体管或可表不同导电性类型的晶体管。例如，第一晶体管 350 可表 P-沟道晶体管而晶体管 360 可表 N-沟道晶体管。因此，在形成个别孔洞或凹陷以容设半导体区 336、336A 的相应蚀刻工艺中，可达成工艺均匀性提高，此是由于当暴露一型晶体管时，该蚀刻工艺可不需任何硬质掩模来完全覆盖另一型晶体管。类似情况，在后续外延生长工艺中，由于任何负载作用减少（其亦可能为习知技术的课题），可达成跨越衬底 301 的均匀性的提高，在该工艺中，一型晶体管完全受到覆盖，而另一型晶体管则受到暴露。在形成升高半导体区 336、336A 相应外延生长工艺中，可引入少量锗及/或锡以提供例如与第二晶体管 360 性能相容的「基本」应变 307。其他例释实施例中，当认为基本应变 307 不适当时，可省略相应孔洞蚀刻与后续外延生长工艺。在其他情况中，晶体管 360 可表在关键器件区中例如静态 RAM 区中的 P-沟道晶体管，该区可接收减

少的应变307量，而晶体管350可能需要增加应变量。

在一例释实施例中，可进行注入工艺320，在此工艺中，暴露第一晶体管350而第二晶体管360可用刻胶掩模321覆盖。在注入工艺320中，可将锡注入至区336，藉以增加区336中锡浓度，由于锡增加的共价半径产生更有效率晶格畸变，而可导致所欲的应变增加。因为注入诱发浓度可能需要高浓度例如约1020原子/立方公分或更高，所以进行注入工艺320时，区336可实质上无晶形化。因此，可进行回火工艺以再结晶基于结晶模板302的该实质上无晶形化区336，藉此在区336中形成高度应变晶体结构。结果，可增加初始呈现的应变307至值307A，藉以获得晶体管350所需的移动性增加。之后，可继续实施如前参照图2a至2d所述的进一步工艺以完成晶体管350与360。

其他例释实施例中，当利用注入工艺320所达成浓度去产生应变307A是适当时，可进行注入工艺320而无需先形成区336、336A。例如，在高灵敏器件区，基于应变半导体材料上的应变工程对N-沟道晶体管而言可能不适当，然而可能需要PMOS晶体管的沟道区中的「温和」应变。在此情况，可在形成任何漏极与源极区之前应用注入工艺320，其中，在一实施例中，注入工艺320另外可施行为预先非晶形化注入工艺以便促进后续引入掺杂形成漏极与源极区。如此一来，可达到高选择性效能改善，且对现今工艺技术具有高度相容性，实质上未大幅地影响N-沟道晶体管。

因此，本发明藉由经应变或松弛的半导体材料方式来提供形成应变的改善技术，在此技术中，是将比锗具有更大共价半径的原子种类，例如锡，引入至个别结晶硅基半导体层，藉以显著减少因聚集与晶格缺陷所引起的应力释放风险。在例释实施例中，可利用在适当前体材料例如氢化锡（SnH_4）上的外延生长工艺来引入具有增加共价半径的原子种类。此外，利用其他技术例如注入来引入原子种类，可达到高度定位化的应变工程，藉以提供高弹性的工艺与产品设计。

以上所揭示的特定实施例只用于例释，对该些娴熟本说明书所教示优点的技艺者而言，显然可以不同但均等的方式对本发明进行修改与实践。例如，以上所提出的工艺步骤可以不同的次序予以进行。此外，除如下文权利要求书中所述者外，并无意去限制本说明书所示的

结构或设计细节。所以显然地，以上所揭示的特定实施例可加以变化或修改，而所有该些变化落在本发明的范围与精神内。因此，本说明书所寻求的保护如以下权利要求书中所提出者。

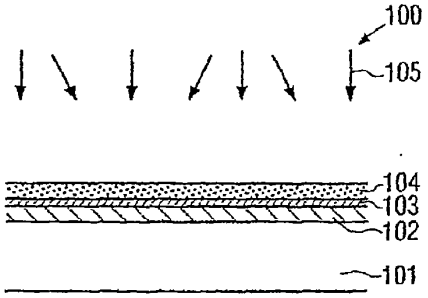


图 1a

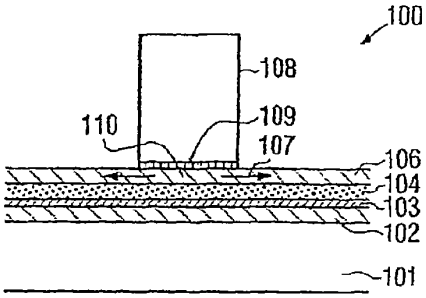


图 1b

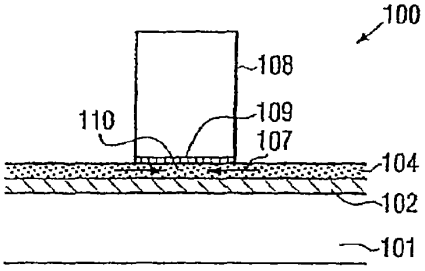


图 1c

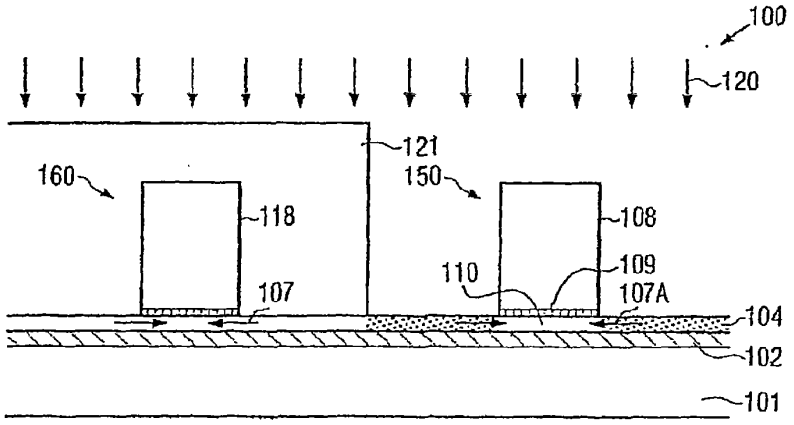


图 1d

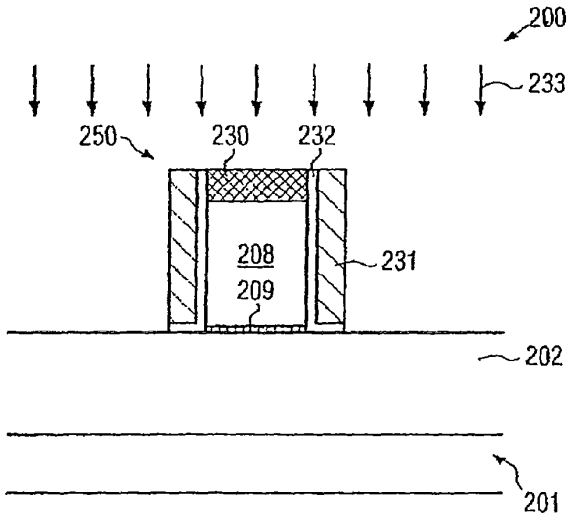

200
233
250
230
232
208
209
231
202
201

图 2a

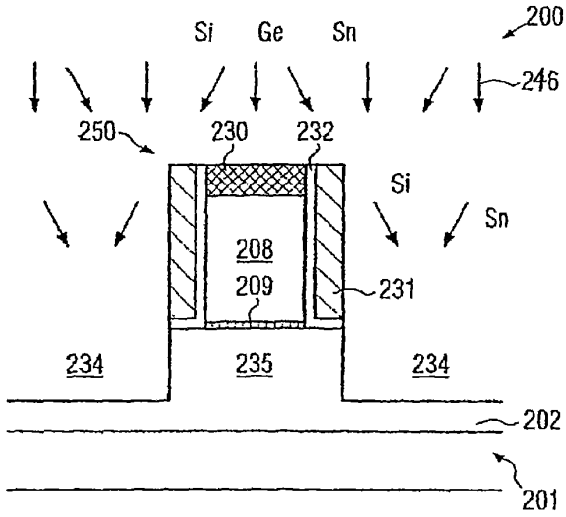

Si
Ge
Sn
200
246
250
230
232
Si
Sn
208
209
231
234
235
234
202
201

图 2b

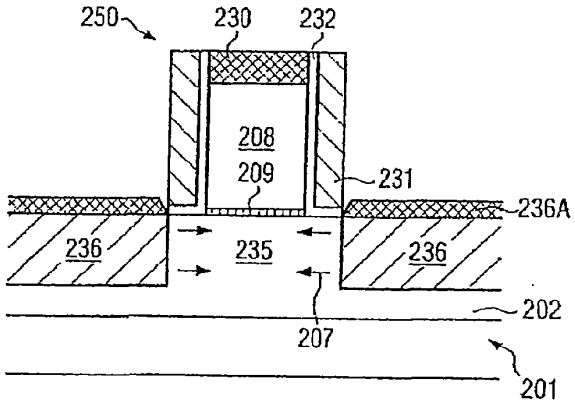

250
230
232
208
209
231
236A
236
235
236
202
207
201

图 2c

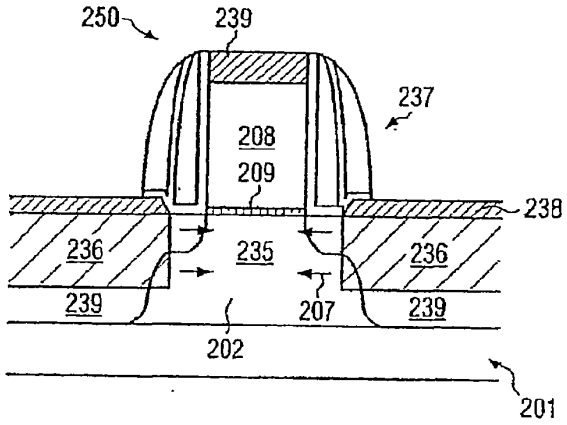

250
239
237
208
209
238
236
235
236
239
207
239
202
201

图 2d

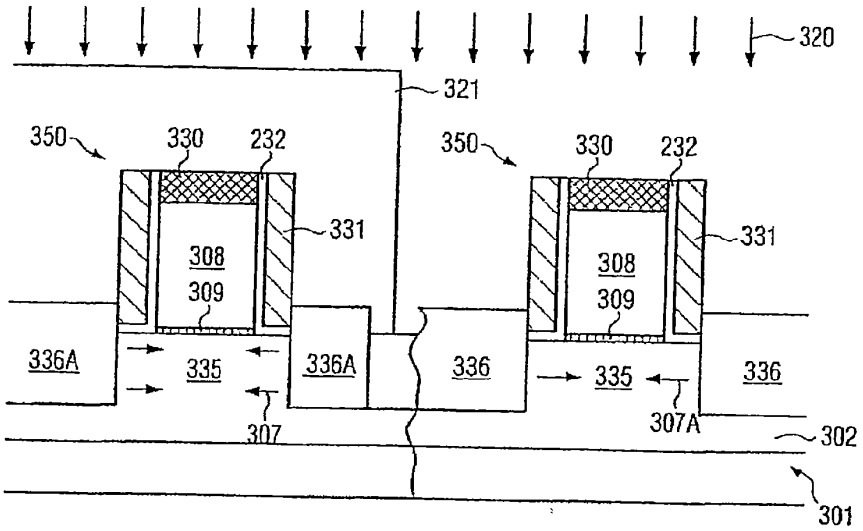


图 3

Espacenet

Bibliographic data: CN101677110 (A) — 2010-03-24

Method for improving transistor performance through reducing the salicide interface resistance

Inventor(s): ANAND MURTHY; BOYAN BOYANOV; GLENN GLASS; THOMAS HOFFMANN ± (MURTHY ANAND, ; BOYANOV BOYAN, ; GLASS GLENN, ; HOFFMANN THOMAS)

Applicant(s): INTEL CORP ± (INTEL CORP)

Classification: - international: *H01L21/28; H01L21/285; H01L21/336; H01L29/45; H01L29/78*

- cooperative: H01L21/28518 (EP, KR, US); H01L21/823807 (EP, US); H01L21/823814 (EP, US); H01L29/0653 (US); H01L29/0847 (US); H01L29/165 (EP, KR, US); H01L29/167 (US); H01L29/36 (US); H01L29/41725 (US); H01L29/6628 (US); H01L29/665 (EP, KR, US); H01L29/6653 (EP, KR, US); H01L29/6656 (EP, KR, US); H01L29/6659 (EP, KR, US); H01L29/66628 (EP, KR, US); H01L29/66636 (EP, KR, US); H01L29/78 (EP, US); H01L29/7833 (EP, KR, US); H01L29/7842 (EP, KR, US); H01L29/7848 (EP, KR, US); Y10S438/933 (EP, US)

Application number: CN200910205003 20041119

Priority number(s): US20030731269 20031208

Also published as: CN101677110 (B) CN100565823 (C) CN1883040 (A) DE112004002409 (B4) DE112004002409 (T5) more

Abstract of CN101677110 (A)

An embodiment of the invention reduces the external resistance of a transistor by utilizing a silicon germanium alloy for the source and drain regions and a nickel silicon germanium self-aligned silicide (i.e., salicide) layer to form the contact surface of the source and drain regions. The interface of the silicon germanium and the nickel silicon germanium silicide has a lower specific contact resistivity based on a decreased metal-semiconductor work function between the silicon germanium and the silicide and the

increased carrier mobility in silicon germanium versus silicon. The silicon germanium may be doped to further tune its electrical properties. A reduction of the external resistance of a transistor equates to increased transistor performance both in switching speed and power consumption.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION CN101677110A

Method for improving transistor performance by reducing salicide interface resistance

[0001]

The patent application for this invention is the international application number PCT/US2004/038986, the international filing date is November 19, 2004, and the application number entering the Chinese national phase is 200480033557. X, a divisional application for an invention patent application entitled "Method for improving transistor performance by reducing salicide interface resistance".

[0002]

Technical field

[0003]

The embodiments of the present invention relate to high-speed semiconductor transistors, and in particular, to improve semiconductor performance through the use of silicon germanium and its improved application methods.

[0004]

Background technique

[0005]

Silicon complementary metal oxide semiconductor (CMOS) technology is the main microelectronic technology.

CMOS provides high reliability, high integration, low power consumption and low cost. For lower frequency applications, CMOS is most likely to remain the main technology. However, the mobility of electrons and holes in silicon limits the range of CMOS devices that can be used in high-speed applications such as radar and mobile communication devices that require high transistor switching speeds.

[0006]

One historical solution has been to use semiconductor compounds to replace elemental semiconductors such as group IV silicon and germanium.

These compounds can be Group II (Zn and Cd), Group III (B, Al, Ga and In), Group IV (C, Si and Ge), Group V (P, As and Sb) and Group VI (S, Se) And Te) the combination of divalent, trivalent and tetravalent elements. Common III-V semiconductors include gallium arsenide (GaAs), gallium phosphide (GaP), and indium phosphide (InP). In particular, gallium arsenide is widely

used as a near-infrared light source and sensor with a 1.43 electron volt (eV) band gap and as a main semiconductor for high-speed electronic devices. Although the speed improvement is better than silicon CMOS devices, GaAs is too costly for most applications. An estimate shows that in 1995, per square millimeter, the cost of silicon CMOS was $0.01 and the cost of GaAs epitaxy was $2.00.

[0007]

An updated method that provides both the speed advantages of GaAs and the better cost efficiency of silicon CMOS uses silicon germanium (strained or unstrained, usually more accurately labeled by Si1-xGex or simply labeled as SiGe) and/ Or strained silicon.

The lattice constant (ie, the interatomic distance) of germanium is 4.2% larger than that of silicon. Silicon germanium also has a larger lattice constant, the extent of which depends on the percentage composition of germanium. When growing silicon on silicon germanium, under suitable conditions, the silicon lattice is elongated at the silicon/silicon germanium interface to match the crystal lattice of silicon germanium. When growing silicon germanium on silicon, the silicon germanium lattice is compressed under appropriate conditions. For each method, there is a critical thickness of the growth layer (silicon or silicon germanium) beyond which the growth layer relaxes when the lattice defects diffuse.

[0008]

There are two reasons why strained silicon and silicon germanium can provide improved speed characteristics for transistors constructed from them.

Compared with elemental silicon, germanium has lower electron effective mass and lower hole effective mass (resulting in higher electron mobility and higher hole mobility). The silicon germanium compound benefits from the increased mobility of the component germanium. In addition, the induced strain (tension and compression, respectively) in silicon or silicon germanium forms an anisotropic structure that changes the conduction band and valence band of the material. When combined with other semiconductor layers with different band gaps (for example, shaped layers), conduction band and valence band discontinuities can be designed to form quantum wells or internal electric fields to accelerate carriers through the shaped layers.

[0009]

It is relatively easy to incorporate silicon germanium deposition into the CMOS process flow.

For example, the larger cost increase is only the addition of silicon germanium epitaxy steps. Assuming that the integration is easier and it is possible to change the band gap with silicon germanium (eg, bulk silicon, bulk silicon germanium, and strain variants of each), it is possible to fabricate the entire system on a silicon or silicon-on-insulator (SOI) substrate Sex is realistic. The integrated system can include fiber optic connections, waveguides, optical detectors, CMOS, heterojunction bipolar transistors, and quantum devices all on the same chip.

[0010]

Simply using strained silicon and/or silicon germanium will not immediately provide a good device.

As with all example changes, the incorporation of strained silicon and silicon germanium into current semiconductor processing flow forms a new set of problems to be solved.

[0011]

Description of the drawings

[0012]

Figure 1a shows a cross-section of the substrate after the formation of the gate and the nitride spacer.

[0013]

Figure 1b shows a cross-section of the substrate after a dielectric film is deposited on the entire surface of the substrate.

[0014]

Figure 1c shows a cross-section of the substrate after the dielectric film is patterned and etched to expose the source and drain regions.

[0015]

Figure 2 shows a cross-section of the substrate after undercut etching of the source and drain regions.

[0016]

Figure 3 shows a cross-section of the substrate after silicon germanium has been deposited in the undercut etched source and drain regions.

[0017]

Figure 4a shows a cross-section of the substrate after depositing a poorly soluble metal.

[0018]

Figure 4b shows a cross-section of the substrate after forming an annealing to form a silicide contact layer on the surface of the silicon germanium source drain region and the gate region.

[0019]

Figure 4c shows the cross section of the substrate after removing unreacted insoluble metal.

[0020]

Figure 5 shows the band structure of p-type silicon to silicon germanium.

[0021]

Figure 6 shows the band structure of p-type silicon in contact with metal.

[0022]

Figure 7 shows the band structure of silicon germanium in contact with metal.

[0023]

FIG. 8 shows a cross section of a substrate representing the external resistance (Rext) of a metal oxide semiconductor transistor.

[0024]

Detailed ways

[0025]

Hereinafter, an embodiment of a method for improving the performance of a transistor will be described.

These embodiments will now be described in detail with reference to the drawings, as shown in the drawings.

Although the embodiments will be described in connection with these drawings, it is not intended to limit them to the drawings disclosed herein.

On the contrary, the intention is to cover all changes, modifications and equivalents within the spirit and scope of the described embodiments, as defined by the appended claims.

[0026]

By using a silicon germanium alloy for the source and drain regions and a nickel silicon germanium salicide (ie, salicide) layer to form the contact surface of the source and drain regions, the embodiment of the present invention reduces The external resistance of the transistor is reduced.

Based on the reduced metal-semiconductor work function between silicon germanium and silicide and the increased carrier mobility of silicon germanium compared to silicon, the interface between silicon germanium and nickel silicon germanium silicide has a lower specific contact resistivity.

The silicon germanium can be doped to further adjust its electrical properties.

The reduction of transistor external resistance is equivalent to the improvement of transistor performance in terms of switching speed and power consumption.

[0027]

1947

The first transistor manufactured in 2009 was germanium.

However, given a narrower band gap of 0.67 eV (compared to 1.11 eV of silicon), a reverse-biased germanium p-n junction exhibits a larger leakage current.

This limits the operating temperature of germanium to below 100°C.

In addition, it is difficult to fabricate a passivation layer, as required by semiconductor processing technology.

For example, germanium oxide is water-soluble and separates at 80°C.

These qualities require an order of magnitude higher cost of electronic-grade germanium than silicon, which actually eliminates element germanium from modern semiconductor technology.

[0028]

However, the use of germanium has advantages over silicon.

For example, at room temperature, germanium has an electron mobility of 3,600 cm 2 /V-s compared to the electron mobility of 1350 cm 2 /V-s of silicon.

Even more surprising is that compared with the hole mobility of silicon of 480 cm2/V-s, the hole mobility of germanium is 1800 cm2/V-s.

Since germanium has an intrinsic carrier concentration of 2.5*1013cm-3 at 300K, silicon has 1.5*1010cm-3, and the sum of conductivity and mobility is proportional to the product of the intrinsic carrier concentration, so germanium has obvious Higher conductivity.

As described further below, the performance of the transistor is related to the external resistance.

Since resistivity is the reciprocal of conductivity, the use of higher conductivity materials increases the performance of the transistor.

Alloying silicon and germanium provides the ability to adjust materials to take advantage of the benefits of each constituent semiconductor.

As described with reference to the embodiments of the present invention, semiconductor alloys of silicon and germanium provide promising improvements in certain semiconductor applications.

[0029]

Figure 1a shows a cross-section of the substrate after various processing steps have begun to form metal oxide semiconductor (MOS) transistors.

Those skilled in the art will recognize what processing steps have been performed, so the description will be omitted.

In the embodiment of the present invention, the transistor is a p-type MOS or PMOS.

The substrate 100 is silicon.

The isolation barrier layer 101 serves as a channel stop to prevent parasitic effects between closely aligned transistors in integrated circuit applications.

The isolation barrier layer 101 may be, for example, a shallow trench isolation (STI) region, which is formed by etching a trench in the substrate 100 and filling the trench with a deposited oxide isolation material.

The gate 102 is formed and patterned on the insulator 104, and the composition of the gate 102 is, for example, polysilicon.

The polysilicon of the gate 102 may be further pre-doped.

On each side of the gate 102, there are sidewall spacers 103 generally composed of silicon nitride.

Each sidewall spacer 103 is used as a hard mask for the subsequent self-alignment processing step.

Those skilled in the art will understand that, for example, the sidewall spacer 103 is a hard mask for lightly doped drain transistor designs that benefit from sidewall isolation or high-dose implantation in other designs, as known in the art. of.

[0030]

Through the processing steps shown in FIG. 1a, the processing is a standard CMOS processing flow well known in the art.

The next processing step for the CMOS process after Figure 1a is to form the source and drain regions of the MOS transistor by doping the source and drain regions by ion implantation.

However, in this regard, the processing of the embodiment of the present invention is different from the standard CMOS processing flow.

In one embodiment of the present invention, silicon germanium is only used for PMOS devices.

Instead of implanting the source and drain regions (ie, the next step in the standard CMOS process flow), cover the exposed surface of the wafer with a dielectric layer such as SiO2 or Si3N4, as shown by the dielectric layer 105 in FIG. 1b.

Use any known photolithography or related patterning techniques to pattern the dielectric layer to expose the source and drain regions of the intended PMOS device, as shown in Figure 1c, and leave the intended NMOS device completely covered.

Subsequently, SF6-based plasma etching selectively removes the exposed silicon substrate 100 material in the source and drain regions of the PMOS device.

This etching is selective in that it removes a large amount of the silicon substrate 100 material at a rate much higher than that of the SiO2 or Si3N4 dielectric layer 105 and the sidewall spacer 103 material used as an etching mask.

Subsequently, the etched source and drain regions are filled with silicon germanium (in one embodiment, silicon germanium doped in situ).

Subsequently, the dielectric layer 105 used as a mask for source and drain region etching and silicon germanium deposition is removed by, for example, HF-based wet etching.

A silicide layer is formed to provide contacts with the source, drain, and gate regions of PMOS and NMOS.

Then, the wafer can undergo the remaining CMOS processing steps to form devices that benefit from embodiments of the invention.

Next, a more specific processing technique of the embodiment of the present invention will be described.

[0031]

Figure 2 shows the cross-section of the substrate of Figure 1c after the undercut etching 201 as described above to remove the silicon of the substrate 100 from the source and drain regions of the PMOS device.

The etched profile allows the substrate 100 material to be removed from under the sidewall spacer 103.

In one embodiment, the undercut etch 201 extends under the gate 102.

The undercut appearance of the undercut etching 201 has a substantial influence on the performance benefits of the embodiment of the present invention.

[0032]

In particular, as shown in FIG. 2, an undercut etching 201 is formed in the substrate 100 laterally along two opposite sidewalls of the gate 102.

In one embodiment, an isotropic etching process is used to form the undercut etching 201.

The isotropic etching not only etches vertically into the substrate but also etches horizontally (laterally) under each sidewall spacer 103 and, in one embodiment, under the gate 102.

Such lateral undercut etching can be generated by using an isotropic dry etching process in, for example, a parallel plate RF plasma etching system using a gas mixture containing SF6 and helium and supporting isotropic process conditions.

These conditions include high voltage and low RF power density.

In one embodiment, processing parameters including a pressure of about 900 mT, a gap of 1.1 cm, an RF power of 100 W, a helium flow rate of 150 sccm, and a SF6 flow rate of 100 sccm are used.

The RF power can vary, for example, in the range of 50W to 200W, and the processing pressure can vary but should be greater than about 500mT.

In one embodiment, the undercut etch 201 has a maximum vertical depth between 100 and 1500 angstroms below the surface of the substrate 100 and is 25 to 200 angstroms horizontally or laterally below the edge of the gate 102 at the interface of the substrate 100/insulator 104. Extends between angstroms.

It is understood that, if necessary, optional processing conditions and etching chemistry (eg, wet etching) can be used to generate other undercut etch 201 geometric structure contours.

[0033]

This etching process not only forms a lateral undercut under each sidewall spacer 103 and, in one embodiment, under the gate 102, but also the etching chemical treatment is highly effective for insulator 104 oxide and sidewall spacer 103 nitride materials. Optional.

In this way, the undercut etching does not damage the material of the insulator and the sidewall spacer 103 and retains the geometric structure of each.

[0034]

The etching chemistry used to form the undercut etching 201 is further slightly oxidized.

The use of an oxidizing etchant makes a portion of the insulator 104 layer exposed during the undercut etching process thicker than the unexposed portion of the insulator 104 layer.

By increasing the thickness of the insulator 104 layer at the edge of the gate 102, the gate edge leakage at the top overlap region of the device can be reduced.

The thicker insulator 104 layer at the edge of the gate 102 helps to increase the breakdown voltage of the device.

[0035]

Another advantage of the undercut etching 201 process is that the etching rate is reduced to between 5 and 30 angstroms per second, so that the etching of the silicon substrate is recessed inward.

With this geometry, when the channel is formed, a larger LMET (metallurgical channel length or physical channel length) is achieved during the off state (low Ioff) of the MOS transistor and at the same time during the on state of the MOS transistor A smaller LMET.

During the on-state, the smaller LMET directly transforms into a smaller channel resistance and correspondingly higher Ion.

[0036]

FIG. 3 shows a cross-section of the substrate of FIG. 2 after the silicon germanium 301 is deposited in the source and drain regions of the undercut etch 201. FIG.

As mentioned above, silicon germanium can be represented by Si1-xGex.

The domain of x is [0,1] ranging from pure silicon to pure germanium, and can be adjusted to adjust the conductivity and band gap according to the needs of the specific device.

In one embodiment, x is approximately between 0.1 and 0.4 (for example, between 10 atomic% and 40 atomic% of germanium in a silicon germanium alloy).

The band gap energy associated with SiGe 301 alloy can be approximated by the following equation:

[0037]

$$Eg(x)=(1.155-0.43x+0.0206x2)eV \text{ For } 0 < x < 0.85 \quad (1)$$

[0038]

$$Eg(x)=(2.010-1.27x)eV \text{ For } 0.85<x<1 \quad (2)$$

[0039]

Therefore, in one embodiment, according to equation (1), the band gap energy of silicon germanium 301 is approximately between 1.11 eV and 0.99 eV, corresponding to 10 atomic% germanium and 40 atomic% germanium, respectively.

[0040]

The silicon germanium 301 is deposited by selective epitaxial deposition, in which the silicon germanium is deposited only on the surface of the larger silicon substrate exposed by the undercut etching 201 and not covered by the dielectric layer 105.

The silicon germanium 301 crystal is not grown on the SiO2 or Si3N4 dielectric layer.

In one embodiment, the deposition technique is pressure-reduced chemical vapor deposition (CVD) epitaxial deposition.

In other embodiments, the deposition technique includes atmospheric CVD epitaxy and ultra-high vacuum CVD epitaxy.

Since the deposited silicon germanium 301 is single crystal, each deposition technique is a special form of vapor phase epitaxy.

[0041]

As mentioned above, in one embodiment, the silicon germanium deposition method is CVD epitaxy.

Environmentally, epitaxy occurs between 600°C and 800°C and under pressure between 10 to 760 Torr.

H2 or He can be used as the carrier gas. .

The silicon source precursor gas may be SiH2Cl, SiH4 or Si2H6.

In one embodiment, GeH4 is a germanium source precursor gas.

HCl or Cl2 can be added as an etchant to increase the material selectivity of the deposition.

In one embodiment, the silicon germanium 301 deposited in the source and drain regions of the undercut etch 201 has a thickness between 500 and 2000 angstroms.

In one embodiment, silicon germanium 301 is deposited to extend on the surface of the substrate 100.

In this way, silicon germanium 301 is formed on and under the surface of the substrate 100 at the same time.

By forming silicon germanium 301 on the surface of the substrate 100, a raised end is formed, and the conductivity of the end is increased.

The increased conductivity improves the performance of the device.

[0042]

The silicon germanium 301 can be further doped to adjust its electrical and chemical properties.

Doping can be performed using various dopants and various doping techniques.

For example, silicon germanium 301 can be doped in situ with p-type impurities to a doping concentration level between 1*1018/cm3 and 3*1021/cm3, with a concentration of about 1*1020cm3 being preferred.

In one embodiment, a PMOS device is formed by using the aforementioned precursor and additional B2H6 precursor gas as a boron dopant source during the epitaxial deposition of the silicon germanium 301, and in-situ doping the silicon germanium 301 with boron during the epitaxy.

The advantage of doping the silicon germanium 301 in situ is that the undercut nature of the undercut etching 201 makes it difficult to dope the silicon germanium 301 after it has been deposited in the area shaded by the sidewall spacers.

As a possible solution for doping the silicon germanium shielded by the sidewall spacers, the angular implantation reduces the short channel performance of the obtained PMOS device.

[0043]

In one embodiment, part of the boron dopant added during the deposition of the silicon germanium 301 is not activated at this time.

That is, after deposition, boron atoms are in the silicon germanium 301 layer but have not yet been substituted into silicon sites in the crystal lattice that can provide holes (ie, lack of electrons).

In one embodiment, the thermal activation of the dopants is delayed until subsequent processing steps, reducing heat accumulation and the resulting diffusion of the dopants to enable the formation of very steep source/drain junctions, thereby improving device performance.

[0044]

As described above, the deposited silicon germanium 301 has a relatively large lattice constant, and its amplitude depends on the atomic percentage of germanium in the silicon germanium 301 alloy.

When deposited on the silicon of the substrate 100, the crystal lattice of the silicon germanium 301 is compressed to accommodate crystal growth.

The compression of the silicon germanium 301 source and drain regions further creates compression in the area of the substrate 100 (ie, the channel of the MOS device) located between the silicon germanium 301 source and drain regions and under the insulator 104 region.

This compression forms an anisotropic atomic structure in the channel region and changes the conduction band and valence band of the channel material.

The compressive stress further reduces the effective mass of holes in the channel region of the substrate 100, thereby increasing the hole mobility.

This increased hole mobility increases the saturation channel current of the obtained MOS transistor, thereby improving device performance.

[0045]

Figures 4a, 4b and 4c show the cross-section of the substrate of Figure 3 during the formation of the silicide layer.

More specifically, this layer is a salicide layer or a salicide layer.

Those skilled in the art will understand that the silicide layer 402 is formed on the silicon germanium 301 by depositing a thin layer of insoluble metal, which in one embodiment uses standard sputtering techniques (ie, physical vapor deposition or PVD), Subsequent processing steps are then used to form metal, silicon and germanium silicide alloys.

The difference between the silicide 403 is that the semiconductor element of the silicide alloy depends on the material composition of the gate 102.

[0046]

Insoluble metals especially include cobalt, titanium and nickel.

In one embodiment, the poorly soluble metal is nickel.

The choice of insoluble metal not only needs to consider the electrical compatibility with the silicon germanium 301 material below, but also the mechanical and chemical compatibility. The silicon germanium 301 material occupies the undercut etch 201 source and drain of the corresponding NMOS device on the same substrate. The electrode region and the exposed source, drain and gate regions.

For example, the silicide layer 402 must be continuous and uniform to help reduce the interface resistance between the silicide layer 402 and the underlying silicon germanium 301.

Nickel tends to react uniformly with both silicon and germanium to form a stable three-Ni (SiGe) phase, while cobalt and titanium preferentially react with silicon and isolate the germanium component of the SiGe 301 alloy.

In addition, compared with nickel silicon germanium silicide, titanium and cobalt-based silicon germanium silicide have reduced thermal stability.

Inappropriate selection of insoluble metals will form an undesirable interface between the silicide and the semiconductor, which will increase the interface resistance independently of other electrically compatible materials.

[0047]

Figure 4a shows the substrate of Figure 3 after blanket deposition of insoluble metal 401.

As described above, in one embodiment, the poorly soluble metal is PVD nickel.

Environmentally, PVD nickel deposition occurs between 20°C and 200°C and under pressures of less than 50 mtorr.

The thickness of nickel is between 50 and 200 angstroms.

After the nickel is deposited, rapid formation annealing is performed between 325° C. and 450° C. in less than or equal to 60 seconds, for example, using a rapid thermal annealing (RTA) equipment.

During the formation annealing, the silicon germanium 301 and the insoluble metal 401 on top of the gate 102 react to form a silicide 402 and a silicide 403, respectively, as shown in FIG. 4b.

When nickel is deposited on the entire exposed surface of the substrate 100, a wet etching chemical composition such as a mixture of hot H2O2 and hot H2SO4 is used to remove unreacted nickel (ie, in the nitride or isolation 101 area deposited on the sidewall spacer 103). On top, nickel that has not reacted with silicon or silicon germanium to form a silicide with its underlying layer) is removed.

The remaining reacted nickel on the top of the silicon germanium 301 source and drain regions and the gate 102 region is then subjected to a final annealing between 400°C and 550°C to complete the formation of nickel silicon germanium silicide 402 and silicide 403, As shown in Figure 4c.

The silicide layer can be further covered with, for example, a titanium nitride cap to prevent the nickel silicon germanium silicide layer 402 and the silicide layer 403 from being oxidized in subsequent processing steps, as is well known in the art.

[0048]

Figures 5 to 7 show how appropriate material selection for poorly soluble metals and source-drain region materials can reduce the physical properties of the corresponding contact resistivity.

Figure 5 shows the energy band diagrams for larger sheets of metal, p-type silicon, and silicon germanium.

The fermi of metal can be labeled as EFm.

The Fermi energy of p-type silicon and silicon germanium are EFSi and EFSiGe, respectively.

As shown in the figure, although it is not necessarily drawn to scale, the conduction band edge ECSiGe of silicon germanium is slightly lower than the conduction band edge ECSi of silicon.

In addition, the valence band edge EVSiGe of silicon germanium is higher than the valence band edge EVSi of silicon, and is proportionally higher based on the percentage composition of germanium in the silicon germanium alloy.

Therefore, the band gap of silicon-germanium alloy is smaller than that of silicon, and its degree depends on the percentage composition of germanium in the germanium alloy, as described in equations (1) and (2).

[0049]

Figure 6 shows the band bending associated with the contact between the poorly soluble metal and p-type silicon.

The size of the energy barrier is worth noting.

With p-type semiconductors, aligning the Fermi level in an equilibrium state requires a positive charge on the metal side and a negative charge on the semiconductor side.

Semiconductors regulate negative charge by generating a depletion region in which ionized acceptors remain uncompensated by holes.

[0050]

Figure 7 shows the band bending associated with the contact between the poorly soluble metal and the silicon germanium 301 alloy.

The magnitude of the energy barrier is worth noting. In this case, pay attention to the relative difference in the energy barrier height of the silicon-germanium alloy when compared with p-type silicon.

In other words, the metal-semiconductor work function is smaller for the metal-silicon germanium 301 contact than for the metal-p-type silicon contact.

The current conduction of the contacts is dominated by tunneling.

The relation of specific contact resistivity is as follows:

[0052]

The significant variables in equation (3) are the metal-semiconductor work function ΦB, the semiconductor doped Nsurf, and the effective carrier mass m^* in the semiconductor.

As mentioned above, the effective mass of holes in the silicon germanium film is 0.34m0 compared to 0.37m0 of silicon, where m0 represents the resting mass of electrons.

[0053]

The specific contact resistivity equation (3) shows that the specific contact resistivity of the metal-semiconductor interface mainly depends on the metal-semiconductor work function, the doping density in the semiconductor, and the effective mass of carriers.

Changing any one of these variables or their combination will affect the specific contact resistivity.

As described above, the use of silicon germanium 301 reduces the work function of the metal semiconductor and reduces the effective mass of carriers.

In one embodiment, silicon germanium is further doped, as described with reference to FIG. 3.

[0054]

The interface between the silicon germanium 301 and the silicide 402 can be further discussed as a metal-semiconductor ohmic contact.

In the beginning, the effect of the energy barrier at the contact between the silicide and the semiconductor must be viewed from the point of view of quantum mechanics.

As is well known in the art, wave-particle duality specifies that an electron is treated as both a particle and a wave to determine its behavior.

The energy barrier formed by the silicide-semiconductor interface can be regarded as a barrier of finite thickness and height.

For a given barrier height and a given barrier width greater than the energy of the incident electron, there is a certain probability that the electron will pass through the barrier and appear on the other side.

This tunneling phenomenon is an important mechanism of electron conduction in solids.

[0055]

More specifically, contact resistivity is a measure of how easily current flows through the metal-semiconductor interface.

If the contact is ohmic, by definition, there is an unhindered transfer of majority carriers from one material to another-in this case between the silicide 402 and the silicon germanium 301.

This can also be expressed as a linear current-voltage characteristic.

In the case of a metal-semiconductor interface, the conduction mechanism is partly dictated by the width of the semiconductor depletion region adjacent to the contact interface.

If the semiconductor is slightly doped (for example, the Fermi energy is neither close to the energy at the edge of the conduction band nor the energy at the edge of the valence band), the depletion zone becomes wide enough to allow electrons to be transferred between the two contact materials. The method is to jump over the barrier through thermionic emission above the maximum value of the barrier.

Or, if the semiconductor is highly doped (the Fermi energy is close to the conduction band edge energy of the n-type and the valence band edge energy of the p-type), the depletion region becomes narrow enough to allow field emission or carrier tunneling as the main The transmission mechanism.

Both field emission and thermionic emission contribute to conduction across the interface and can be adjusted, for example, by material selection and doping.

[0056]

FIG. 8 shows an embodiment of the present invention using, for example, the source and drain regions of silicon germanium 301 with a nickel silicon germanium silicide layer 402.

The external resistance Rext801 is the total series resistance between the source (or drain) contact and the channel of the intrinsic transistor.

The interface resistance between the silicon germanium 301 and the silicide 402 is an important component of the total series resistance.

Rext801 is reduced by using silicon germanium compared to using p-type silicon for the source and drain regions.

In addition, the appropriate selection of the insoluble metal (nickel in one embodiment) of the silicide layer 402 has ensured a chemically and mechanically compatible metal-semiconductor interface, which will not adversely affect Rext801, as described with reference to FIG. 4 .

[0057]

Those skilled in the art will recognize the advantages of the disclosed embodiments, where it reduces the specific contact resistivity between the silicon germanium source and drain regions and their respective silicide contacts by using new material selection and processing techniques .

Since the contact resistivity affects the overall external resistivity of the transistor, the reduction of the contact resistivity contributes to the improvement of the overall performance in the transistor.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS CN101677110A

1.

A type of transistor including:

Gate area

The insulator region under the gate region;

The source region adjacent to the oxide region;

The drain region adjacent to the oxide region;

The source region and the drain region include silicon germanium alloy and nickel silicon germanium silicide layer.

2.

The transistor of claim 1, wherein the source region and the drain region extend laterally under the insulating layer.

3.

3. The transistor of claim 2, wherein the source region and the drain region extend laterally below the gate region.

4.

The transistor of claim 3, wherein the source region and the drain region extend laterally between 25 and 200 angstroms below the gate region.

5.

The transistor of claim 1, wherein the source region and the drain region have a vertical depth between 100 and 1500 angstroms below the surface of the silicon substrate.

6.

The transistor of claim 1, wherein the silicon germanium alloy has a germanium composition between 5% and 50%.

7.

7. The transistor of claim 6, wherein the silicon germanium alloy has a germanium composition between 10% and 40%.

8.

8. The transistor of claim 7, wherein the silicon germanium alloy has a germanium composition between 15% and 30%.

9.

The transistor of claim 1, wherein the silicon germanium alloy is doped.

10.

9. The transistor of claim 9, wherein the silicon germanium is doped in situ during the deposition of the silicon germanium alloy.

11.

The transistor of claim 10, wherein the dopant is boron.

12.

The transistor of claim 11, wherein the source of the dopant is B2H6.

13.

The method of claim 11, wherein the boron has a doping concentration level between 1*1018/cm3 and 3*1021/cm3.

14.

The method of claim 13, wherein the doping concentration level is 1*1020/cm3.

15.

The transistor of claim 1, wherein the nickel silicon germanium silicide layer is self-aligned.

16.

A device for manufacturing transistors, including:

A device for etching source and drain regions in a silicon substrate, wherein the etching has an undercut profile;

A device for depositing silicon germanium alloy in the source region and the drain region;

A device for depositing nickel on the silicon germanium alloy;

A device for forming a nickel silicon germanium silicide layer in the source region and in the drain region, wherein the nickel silicon germanium silicide layer is self-aligned,

A device for annealing the substrate at a temperature between 325°C and 450°C for less than or equal to 60 seconds;

A device for removing excess nickel with hot H2O2 and H2SO4 wet etching chemistry; and

A device for annealing the substrate at a temperature between 400°C and 550°C.

17.

The device of claim 16, wherein the source region and the drain region extend laterally under the insulating layer.

18.

The device of claim 17, wherein the source region and the drain region extend laterally under the gate region.

19.

The device of claim 18, wherein the source region and the drain region extend laterally between 25 and 200 angstroms below the gate region.

20.

The device of claim 16, wherein the source region and the drain region have a vertical depth between 100 and 1500 angstroms below the surface of the silicon substrate.

21.

The apparatus of claim 16, wherein the etching is dry SF6-based.

22.

The device of claim 16, wherein the silicon germanium alloy has a germanium composition of between 5% and 50%.

23.

The device of claim 22, wherein the silicon germanium alloy has a germanium composition between 10% and 40%.

24.

The device of claim 23, wherein the silicon germanium alloy has a germanium composition between 15% and 30%.

25.

The apparatus of claim 16, wherein the deposition of the silicon germanium alloy is vapor phase epitaxy.

26.

The apparatus of claim 16, wherein the deposition of the silicon-germanium alloy is pressure-reduced chemical vapor deposition.

27.

The apparatus of claim 16, wherein the deposition of the silicon-germanium alloy is atmospheric chemical vapor deposition.

28.

The apparatus of claim 16, wherein the deposition of the silicon-germanium alloy is ultra-high vacuum chemical vapor deposition.

29.

The apparatus of claim 16, wherein depositing the silicon germanium alloy further comprises doping the alloy.

30.

The apparatus of claim 29, wherein the doping is performed in situ during the deposition of the silicon germanium alloy.

31.

The device of claim 30, wherein the dopant is boron.

32.

The device of claim 31, wherein the source of the dopant is B2H6.

33.

The device of claim 31, wherein the boron has a doping concentration level between 1*1018/cm3 and 3*1021/cm3.

34.

The device of claim 33, wherein the doping concentration level is 1*1020/cm3.

35.

The apparatus of claim 16, wherein the nickel has a thickness between 50 and 200 angstroms.

[19] 中华人民共和国国家知识产权局

[12] 发明专利申请公布说明书

[21] 申请号 200910205003.8

[51] Int. Cl.
H01L 29/78 (2006.01)
H01L 29/45 (2006.01)
H01L 21/336 (2006.01)
H01L 21/28 (2006.01)

[43] 公开日 2010 年 3 月 24 日

[11] 公开号 CN 101677110A

[22] 申请日 2004.11.19
[21] 申请号 200910205003.8
分案原申请号 200480033557.X
[30] 优先权
[32] 2003.12.8 [33] US [31] 10/731,269
[71] 申请人 英特尔公司
地址 美国加利福尼亚州
[72] 发明人 A·莫西 B·波亚诺夫
G·格拉斯 T·霍夫曼

[74] 专利代理机构 上海专利商标事务所有限公司
代理人 陆 勍

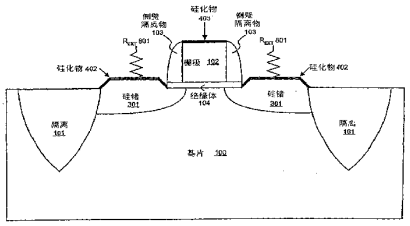
权利要求书 3 页 说明书 10 页 附图 12 页

[54] 发明名称

用于通过减少自对准硅化物界面电阻改善晶体管性能的方法

[57] 摘要

本发明的实施例通过使用用于源极和漏极区的硅锗合金以及镍硅锗自对准硅化物(即，自对准硅化物)层以形成源极区和漏极区的接触表面来减小晶体管的外电阻。 基于硅锗和硅化物之间减少的金属半导体功函数数以及与硅相比硅锗中增加的载流子迁移率，硅锗和镍硅锗硅化物的界面具有较低的比接触电阻。 可对硅锗进行掺杂以进一步调节其电属性。 晶体管的外电阻的减小等同于在切换速度和功耗两方面提高晶体管性能。



1.一种晶体管，包括：

栅极区；

所述栅极区下的绝缘体区；

邻近于氧化物区的源极区；

邻近于氧化物区的漏极区；

其中所述源极区和漏极区包括硅锗合金和镍硅锗硅化物层。

2.如权利要求 1 所述的晶体管，其特征在于，所述源极区和漏极区在绝缘层下横向延伸。

3.如权利要求 2 所述的晶体管，其特征在于，所述源极区和漏极区在栅极区下横向延伸。

4.如权利要求 3 所述的晶体管，其特征在于，所述源极区和漏极区在栅极区下在 25 到 200 埃之间横向延伸。

5.如权利要求 1 所述的晶体管，其特征在于，所述源极区和漏极区在硅基片的表面下具有 100 到 1500 埃之间的垂直深度。

6.如权利要求 1 所述的晶体管，其特征在于，硅锗合金具有 5%到 50%之间的锗组成。

7.如权利要求 6 所述的晶体管，其特征在于，所述硅锗合金具有 10%到 40%之间的锗组成。

8.如权利要求 7 所述的晶体管，其特征在于，所述硅锗合金具有 15%到 30%之间的锗组成。

9.如权利要求 1 所述的晶体管，其特征在于，所述硅锗合金被掺杂。

10.如权利要求 9 所述的晶体管，其特征在于，所述硅锗在硅锗合金沉积期间在原处被掺杂。

11.如权利要求 10 所述的晶体管，其特征在于，掺杂物是硼。

12.如权利要求 11 所述的晶体管，其特征在于，掺杂物的来源是 B_2H_6。

13.如权利要求 11 所述的方法，其特征在于，硼具有 $1*10^{18}/cm^3$ 和 $3*10^{21}/cm^3$ 之间的掺杂浓度水平。

14.如权利要求13所述的方法，其特征在于，所述掺杂浓度水平是 $1*10^{20}/cm^3$。

15.如权利要求1所述的晶体管，其特征在于，所述镍硅锗硅化物层是自对准的。

16.一种制造晶体管的设备，包括：

用于蚀刻硅基片中的源极区和漏极区的装置，其中所述蚀刻具有底切轮廓；

用于在所述源极区中和所述漏极区中沉积硅锗合金的装置；

用于在所述硅锗合金上沉积镍的装置；

用于在所述源极区中和在所述漏极区中形成镍硅锗硅化物层的装置，其中所述镍硅锗硅化物层是自对准的，

用于在325° C和450° C之间的温度下将所述基片退火小于或等于60秒的装置；

用于用热 H_2O_2 和 H_2SO_4 的湿蚀刻化学成分去除过剩的镍的装置；以及

用于在400° C和550° C之间的温度下退火所述基片的装置。

17.如权利要求16所述的设备，其特征在于，所述源极区和漏极区在绝缘层下横向延伸。

18.如权利要求17所述的设备，其特征在于，所述源极区和漏极区在栅极区下横向延伸。

19.如权利要求18所述的设备，其特征在于，所述源极区和漏极区在栅极区下在25到200埃之间横向延伸。

20.如权利要求16所述的设备，其特征在于，所述源极区和漏极区在硅基片的表面下具有100到1500埃之间的垂直深度。

21.如权利要求16所述的设备，其特征在于，所述蚀刻是干 SF_6 基的。

22.如权利要求16所述的设备，其特征在于，硅锗合金具有5%到50%之间的锗组成。

23.如权利要求22所述的设备，其特征在于，所述硅锗合金具有10%到40%之间的锗组成。

24.如权利要求23所述的设备，其特征在于，所述硅锗合金具有15%到30%之间的锗组成。

25.如权利要求 16 所述的设备，其特征在于，所述硅锗合金的沉积是气相外延。

26.如权利要求 16 所述的设备，其特征在于，所述硅锗合金的沉积是减小压力的化学气相沉积。

27.如权利要求 16 所述的设备，其特征在于，所述硅锗合金的沉积是大气化学气相沉积。

28.如权利要求 16 所述的设备，其特征在于，所述硅锗合金的沉积是超高真空化学气相沉积。

29.如权利要求 16 所述的设备，其特征在于，沉积硅锗合金进一步包括掺杂所述合金。

30.如权利要求 29 所述的设备，其特征在于，所述掺杂在沉积硅锗合金期间在原处进行的。

31.如权利要求 30 所述的设备，其特征在于，掺杂物是硼。

32.如权利要求 31 所述的设备，其特征在于，掺杂物的来源是 B_2H_6。

33.如权利要求 31 所述的设备，其特征在于，硼具有 $1*10^{18}/cm^3$ 和 $3*10^{21}/cm^3$ 之间的掺杂浓度水平。

34.如权利要求 33 所述的设备，其特征在于，所述掺杂浓度水平是 $1*10^{20}/cm^3$。

35.如权利要求 16 所述的设备，其特征在于，所述锗具有 50 到 200 埃之间的厚度。

用于通过减少自对准硅化物界面电阻改善晶体管性能的方法

本发明专利申请是国际申请号为 PCT/US2004/038986，国际申请日为 2004 年 11 月 19 日，进入中国国家阶段的申请号为 200480033557.X，名称为“用于通过减少自对准硅化物界面电阻改善晶体管性能的方法”的发明专利申请的分案申请。

技术领域

本发明的实施例涉及高速半导体晶体管，尤其涉及通过使用硅锗和其改进的应用方法来提升半导体性能。

背景技术

硅互补金属氧化物半导体（CMOS）技术是主要的微电子技术。CMOS 提供了高可靠性、高集成度、低功耗和低成本。对于较低频率的应用，CMOS 最可能保持为主要的技术。但是，硅中的电子和空穴迁移率限制了 CMOS 器件可用于诸如需要高晶体管开关速度的雷达和移动通信装置的高速应用的范围。

一个历史上的解决方案是使用半导体化合物代替诸如IV族硅和锗的元素半导体。这些化合物可以是 II 族（Zn 和 Cd）、III 族（B、Al、Ga 和 In）、IV 族（C、Si 和 Ge）、V 族（P、As 和 Sb）和 VI 族（S、Se 和 Te）元素的二价、三价、四价组合。普通的 III-V 半导体包括砷化镓（GaAs）、磷化镓（GaP）和磷化铟（InP）。特别是，砷化镓广泛地用作 1.43 电子伏特（eV）带隙的近红外光源和传感器并用作高速电子器件的主要半导体。尽管速度改善优于硅 CMOS 器件，但 GaAs 对于大多数应用来说是成本过高的。一项估计表明 1995 年的每平方毫米美元，硅 CMOS 成本为$0.01 而 GaAs 外延的成本为$2.00。

一种既提供 GaAs 的速度优势又具有硅 CMOS 的较佳成本效率的更新的方法采用硅锗（应变的或不应变的，通常更精确地由 $Si_{1-x}Ge_x$ 标注或简单地标注为 SiGe）和/或应变硅。锗的晶格常数（即，原子间距）比硅大 4.2%。硅锗也具有较大的晶格常数，其程度取决于锗的百分组成。当在硅锗上生长硅时，在合适的条件下，在

硅/硅锗界面处硅晶格伸长以与硅锗的晶格相匹配。当在硅上生长硅锗时，在适当的条件下硅锗晶格被压缩。对于每种方法，存在生长层（硅或硅锗）的临界厚度，当晶格缺陷扩散时生长层松弛超过该临界厚度。

应变硅和硅锗能对由其构成的晶体管提供改进的速度特征有两个原因。与元素硅相比，锗具有较低的电子有效质量和较低的空穴有效质量（导致较高的电子迁移率和较高的空穴迁移率）。硅锗化合物得益于成分锗的增加的迁移率。此外，硅或硅锗中诱发的应变（分别是拉伸和压缩）形成改变材料的导带和价带的各向异性结构。当与具有不同带隙的其它半导体层（例如，异形层）组合时，可以设计导带和价带不连续以形成量子势阱或内部电场以加速载流子穿过异形层。

可以相对容易地将硅锗沉积结合入 CMOS 工艺流程。例如，较大的成本增加仅仅是硅锗外延步骤的添加。假定集成较容易且可能用硅锗（例如，块硅、块硅锗和每一种的应变变型）来改变带隙，则在一个硅或绝缘衬底硅（SOI）基片上制造整个系统的可能性是现实的。集成系统可包括全部在同一芯片上的光纤连接、波导、光学检测器、CMOS、异质结双极晶体管和量子器件。

简单地使用应变硅和/或硅锗不会立即提供优良的器件。如同所有示例变化，将应变硅和硅锗结合入当前的半导体处理流程形成了要解决的新的一组问题。

附图说明

图 1a 示出了栅极和氮化物隔离物形成之后基片的横截面。

图 1b 示出了在整个基片表面上沉积电介质薄膜后基片的横截面。

图 1c 示出了将电介质薄膜形成图案并蚀刻以露出源极和漏极区之后基片的横截面。

图 2 示出了源极和漏极区底切蚀刻之后基片的横截面。

图 3 示出了在底切蚀刻的源极和漏极区中沉积硅锗之后基片的横截面。

图 4a 示出了沉积难溶金属后基片的横截面。

图 4b 示出了形成退火以便在硅锗源极漏极区和栅极区的表面上形成硅化物接触层之后基片的横截面。

图 4c 示出了去除未反应的难溶金属后基片的横截面。

图 5 示出了 p 型硅比硅锗的能带结构。

图 6 示出了与金属相接触的 p 型硅的能带结构。

图 7 示出了与金属相接触的硅锗的能带结构。

图 8 示出了表示金属氧化物半导体晶体管的外电阻（Rext）的基片的横截面。

具体实施方式

下文将描述用于改善晶体管性能的方法实施例。现在参照附图详细描述这些实施例，如附图中所示的。虽然将联系这些附图来描述实施例，但并非旨在将它们限制于这里所揭示的附图。相反，目的在于覆盖所述实施例的精神和范围内的所有变化、修改和等效物，如所附权利要求书所限定的。

通过使用硅锗合金用于源极和漏极区以及镍硅锗自对准硅化物（即，自对准硅化物）层来形成源极和漏极区的接触表面，本发明的实施例减小了晶体管的外电阻。基于硅锗和硅化物之间减小的金属半导体功函数以及硅锗比硅中增加的载流子迁移率，硅锗和镍硅锗硅化物的界面具有较低的比接触电阻率。可对硅锗掺杂以进一步调整其电属性。晶体管外电阻的降低等同于开关速度和功耗两方面晶体管性能的提升。

1947 年制造的第一个晶体管是锗。但是，给出 0.67 电子伏特的较窄带隙（比之于硅的 1.11 电子伏特），反向偏压的锗 p-n 结呈现较大的漏电流。这将锗的工作温度限制于低于 100° C。此外，很难制造钝化层，如半导体处理技术所需要的。例如，氧化锗是水溶的并在 80° C 时分离。这些品质与同硅相比需要高一个数量级的成本的电子级锗实际上从现代半导体技术中消除了元素锗。

但是，使用锗比硅具有好处。例如，在室温下，与硅的 1350cm^2/V-s 的电子迁移率相比，锗具有 3600cm^2/V-s 的电子迁移率。更惊人的是，与硅的 480cm^2/V-s 的空穴迁移率相比，锗的空穴迁移率是 1800cm^2/V-s。由于 300K 下锗具有 2.5*10^{13}cm-3 的本征载流子浓度的硅具有 1.5*10^{10}cm-3，且传导率与迁移率之和与本征载流子浓度的乘积成比例，所以锗具有明显更高的导电率。如以下进一步描述的，晶体管的性能与外电阻有关。由于电阻率是导电率的倒数，所以使用更高导电率的材料就增加了晶体管的性能。使硅和锗成为合金提供了调节材料的能力以利用每个组成半导体的益处。如参考本发明实施例描述的，硅和锗的半导体合金在某些半导体应用中提供有前途的改进。

图 1a 示出了在开始形成金属氧化物半导体（MOS）晶体管的各种处理步骤后基片的横截面。本领域的熟练技术人员将认识到进行了什么处理步骤，因此省去其说明。在本发明的实施例中，晶体管是 p 型 MOS 或 PMOS。基片 100 是硅。隔离阻挡层 101 用作沟道障碍（stop）以防止集成电路应用中靠近排列的晶体管之间的寄生效应。隔离阻挡层 101 例如可以是浅沟槽隔离（STI）区，它是通过蚀刻基片 100 中的沟槽并用沉积的氧化物隔离材料填充该沟槽而形成的。栅极 102 在绝缘体 104 上形成并形成图案，栅极 102 的组合物例如是多晶硅。栅极 102 的多晶硅可被进一步预掺杂。在栅极 102 的每一侧上，有通常由氮化硅构成的侧壁隔离物 103。每个侧壁隔离物 103 都用作用于后续自对准处理步骤的硬掩膜。本领域的熟练技术人员将理解，例如侧壁隔离物 103 是用于得益于侧壁隔离的轻度掺杂的漏极晶体管设计或其它设计中高剂量植入的硬掩膜，如本领域公知的。

通过图 1a 所示的处理步骤，所述的处理是本领域公知的标准 CMOS 处理流程。图 1a 后用于 CMOS 流程的下一个处理步骤是通过离子植入掺杂源极和漏极区来形成 MOS 晶体管的源极和漏极区。但是，在这点上，本发明实施例的处理不同于标准 CMOS 处理流程。在本发明的一个实施例中，硅锗仅用于 PMOS 器件。代替源极和漏极区植入（即，标准 CMOS 处理流程中的下一个步骤），用例如 SiO_2 或 Si_3N_4 的电介质层覆盖晶片的暴露表面，如图 1b 中的电介质层 105 所示。使用任何已知的光刻或相关图案形成技术将电介质层形成图案，以露出预期 PMOS 器件的源极区和漏极区，如图 1c 所示，并保留预期的 NMOS 器件被完全覆盖。随后，SF_6 基的等离子体蚀刻选择性地去除 PMOS 器件的源极和漏极区中露出的硅基片 100 材料。该蚀刻是选择性的，其中它以远高于用作蚀刻掩膜的 SiO_2 或 Si_3N_4 电介质层 105 和侧壁隔离物 103 材料的速率去除大量硅基片 100 材料。随后，用硅锗（在一实施例中，原位掺杂硅锗）填充被蚀刻的源极和漏极区。随后，例如用基于 HF 的湿法蚀刻去除用作源极和漏极区蚀刻和硅锗沉积的掩膜的电介质层 105。形成硅化物层以提供与 PMOS 和 NMOS 的源极、漏极和栅极区的接触。接着，晶片可经历剩余的 CMOS 处理步骤以形成得益于本发明实施例的器件。接着将描述本发明实施例的更特别的处理技术。

图 2 示出在如以上所介绍的底切蚀刻 201 以从 PMOS 器件的源极和漏极区中去除基片 100 硅之后图 1c 的基片横截面。蚀刻的轮廓使得基片 100 材料从侧壁隔

离物 103 下面去除。在一实施例中，底切蚀刻 201 在栅极 102 下延伸。底切蚀刻 201 的底切外表对于本发明实施例所形成的性能益处有实质性影响。

特别是，如图 2 所示，底切蚀刻 201 形成于基片 100 中横向沿着栅极 102 的两相对侧壁。在一实施例中，使用各向同性的蚀刻工艺来形成底切蚀刻 201。各向同性的蚀刻不仅垂直地蚀刻入基片还水平（横向）地在每个侧壁隔离物 103 下且在一个实施例中在栅极 102 下进行蚀刻。可以通过利用各向同性的干蚀刻工艺在例如使用包含 SF_6 和氦的气体混合化学成分以及支持各向同性的工艺条件的平行板 RF 等离子体蚀刻系统中生成这种横向底切蚀刻。这些条件包括高压和低 RF 功率密度。在一个实施例中，使用包括约 900mT 的压强、1.1cm 的间隙、100W 的 RF 功率、150sccm 的氦流量和 100sccm 的 SF_6 流量的处理参数。RF 功率例如可在 50W 到 200W 的范围内变化，且处理压强可以变化但应大于约 500mT。在一实施例中，底切蚀刻 201 具有基片 100 的表面下 100 到 1500 埃之间的最大垂直深度并在基片 100/绝缘体 104 界面处栅极 102 边缘下水平或横向地在 25 到 200 埃之间延伸。可以理解，如需要，可选的处理条件和蚀刻化学处理（例如，湿法蚀刻）可用于生成其它底切蚀刻 201 几何结构轮廓。

这种蚀刻工艺不仅在每个侧壁隔离物 103 下且在一个实施例中在栅极 102 下形成横向底切，且蚀刻化学处理对于绝缘体 104 氧化物和侧壁隔离物 103 氮化物材料也是高度可选的。这样，底切蚀刻不侵害绝缘体和侧壁隔离物 103 材料且保留了每一个的几何结构。

进一步稍许氧化用于形成底切蚀刻 201 的蚀刻化学成分。利用氧化蚀刻剂使得底切蚀刻处理期间露出的一部分绝缘体 104 层变得比绝缘体 104 层的未暴露部分更厚。通过增加栅极 102 边缘处的绝缘体 104 层的厚度，可以减少器件顶重叠区处的栅极边缘泄漏。栅极 102 边缘处的较厚绝缘体 104 层有助于增加器件的击穿电压。

底切蚀刻 201 处理的另一优点在于蚀刻速率减小到每秒 5 到 30 埃之间，使得硅基片的蚀刻向内凹入。采用这种几何结构，当形成沟道时，在 MOS 晶体管的截止状态（低 I_{off}）期间实现了较大的 L_{MET}（冶金沟道长度或物理沟道长度）同时在 MOS 晶体管的导通状态期间实现了较小的 L_{MET}。导通状态期间较小的 L_{MET} 直接转变为较小的沟道电阻和相应的较高的 I_{on}。

图 3 示出了底切蚀刻 201 源极和漏极区中沉积硅锗 301 后图 2 基片的横截面。

如上所述，硅锗可由 $Si_{1-x}Ge_x$ 表示。x 的域是范围从纯硅到纯锗的[0，1]，并可以调节以按具体器件的需要调整传导率和带隙。在一实施例中，x 约在 0.1 到 0.4 之间（例如，硅锗合金中 10 原子％到 40 原子％的锗之间）。与硅锗 301 合金相关联的带隙能量可由以下等式近似：

$E_g(x)=（1.155-0.43x+0.0206x^2）eV$　　对于 $0<x<0.85$　　（1）

$E_g(x)=（2.010-1.27x）eV$　　对于 $0.85<x<1$　　（2）

因此，在一实施例中，根据等式（1），硅锗 301 的带隙能量约在 1.11eV 到 0.99eV 之间，分别对应于 10 原子％的锗和 40 原子％的锗。

硅锗 301 通过选择性的外延沉积而被沉积，其中硅锗仅沉积于由底切蚀刻 201 露出且电介质层 105 未覆盖的较大硅基片表面上。硅锗 301 晶体不生长于 SiO_2 或 Si_3N_4 电介质层上。在一实施例中，沉积技术是减少压力的化学气相沉积（CVD）外延沉积。在其它实施例中，沉积技术包括大气 CVD 外延和超高真空 CVD 外延。由于沉积的硅锗 301 是单晶的，每种沉积技术都是特殊形式的气相外延。

如上所述，在一实施例中，硅锗沉积法是 CVD 外延。环境上，外延发生于 600°C 到 800°C 之间并在 10 到 760 托之间的压强下。可将 H_2 或 He 用作载体气体。。硅源前体气体可以是 SiH_2Cl、SiH_4 或 Si_2H_6。在一实施例中，GeH_4 是锗源前体气体。可添加 HCl 或 Cl_2 作为蚀刻剂以增加沉积的材料选择性。在一实施例中，底切蚀刻 201 源极和漏极区中沉积的形成的硅锗 301 具有 500 到 2000 埃之间的厚度。在一实施例中，硅锗 301 沉积在基片 100 的表面上延伸。这样，硅锗 301 同时形成于基片 100 的表面之上和之下。通过在基片 100 的表面上形成硅锗 301，形成了上升的末端，增加了该末端的传导率。而该提升的传导率又改善了器件的性能。

硅锗 301 可进一步被掺杂以调节其电气和化学属性。掺杂可利用各种掺杂物并用各种掺杂技术进行。例如，硅锗 301 可以用 p 型杂质原位掺杂到 $1*10^{18}/cm^3$ 和 $3*10^{21}/cm^3$ 之间的掺杂浓度水平，其中约 $1*10^{20}cm^3$ 的浓度是优选的。在一实施例中，形成 PMOS 器件，通过在硅锗 301 外延沉积期间将上述前体和附加的 B_2H_6 前体气体作为硼掺杂物源，在外延期间用硼原位掺杂硅锗 301。原位掺杂硅锗 301 的好处在于底切蚀刻 201 的底切性质使得很难在它已沉积于侧壁隔离物所遮蔽的区域中之后掺杂硅锗 301。作为掺杂由侧壁隔离物所遮蔽的硅锗的一种可能的解决方案，有角度的植入减少了所获得的 PMOS 器件的短沟道性能。

在一实施例中，在硅锗 301 沉积期间添加的硼掺杂物的一部分此时不被激活。即，在沉积后，硼原子处于硅锗 301 层中但仍未替换入可提供空穴（即，缺少电子）的晶格中的硅位点。在一实施例中，掺杂物的热激活被推迟直到后续处理步骤，降低了热积存和所产生的掺杂物扩散以使能形成很陡的源极/漏极结，从而改善器件性能。

如上所述，沉积的硅锗 301 具有较大的晶格常数，其幅度取决于硅锗 301 合金中锗的原子百分比。当沉积于基片 100 硅上时，硅锗 301 的晶格被压缩以适应结晶生长。硅锗 301 源极和漏极区的压缩进一步形成了位于硅锗 301 源极和漏极区之间并在绝缘体 104 区域下的基片 100 区域中的压缩（即，MOS 器件的沟道）。该压缩形成了沟道区中各向异性的原子结构，改变沟道材料的导带和价带。压缩应力进一步减少了基片 100 的沟道区中的空穴有效质量，从而增加了空穴迁移率。该提升的空穴迁移率增加了所获得的 MOS 晶体管的饱和沟道电流，从而改善器件性能。

图 4a、4b 和 4c 示出了硅化物层的形成期间图 3 的基片横截面。更具体地，该层是自对准硅化物层或自对准金属硅化物层。本领域的熟练技术人员将理解，通过沉积难溶金属的薄层而在硅锗 301 上形成硅化物层 402，在一个实施例中这采用标准溅射技术（即，物理气相沉积或 PVD），随后用后续处理步骤形成金属、硅和锗硅化物合金。硅化物 403 不同之处在于硅化物合金的半导体元素取决于栅极 102 的材料成分。

难溶金属尤其包括钴、钛和镍。在一实施例中，难溶金属是镍。难溶金属的选择不仅需要考虑与下面的硅锗 301 材料的电气兼容性还要考虑机械和化学兼容性，该硅锗 301 材料占据了同一基片上相应 NMOS 器件的底切蚀刻 201 源极和漏极区和露出的源极、漏极和栅极区。例如，硅化物层 402 必须是连续的和均匀的，以帮助减少硅化物层 402 和下面的硅锗 301 之间的界面电阻。镍趋于与硅和锗两者均匀地反应，形成稳定的三 Ni(SiGe)相，而钴和钛优先与硅反应并离析硅锗 301 合金的锗组分。此外，与镍硅锗硅化物相比，钛和钴基的硅锗硅化物降低了热稳定性。不合适的难溶金属选择会形成硅化物和半导体之间的不理想界面，会独立于另外电兼容的材料增加界面电阻。

图 4a 示出了在毯状沉积难溶金属 401 后图 3 的基片。如上所述，在一实施例中，难溶金属是 PVD 镍。环境上，PVD 镍沉积发生于 20° C 到 200° C 之间并在

小于 50 毫托的压强下。镍的厚度在 50 到 200 埃之间。镍沉积之后，在 325° C 和 450° C 之间在小于或等于 60 秒内例如使用快速热退火（RTA）设备进行快速形成退火。在形成退火期间，硅锗 301 和栅极 102 顶上的难溶金属 401 反应，以分别形成硅化物 402 和硅化物 403，如图 4b 所示。当镍沉积于基片 100 的整个暴露表面上时，利用例如热 H_2O_2 和热 H_2SO_4 的混合物的湿蚀刻化学成分将未反应的镍（即，在沉积于侧壁隔离物 103 氮化物或隔离 101 区域顶上时未与硅或硅锗反应以形成具有其下面层的硅化物的镍）去除。硅锗 301 源极和漏极区以及栅极 102 区顶上的剩余的反应过的镍随后经受 400° C 和 550° C 之间的最后退火以完成镍硅锗硅化物 402 和硅化物 403 的形成，如图 4c 所示。可以用例如氮化钛盖进一步盖住硅化物层，以防止镍硅锗硅化物层 402 和硅化物层 403 在后续处理步骤中氧化，如本领域公知的。

图 5 到 7 示出了用于难溶金属和源极-漏极区材料的合适的材料选择如何减少相应接触电阻率的物理性质。图 5 示出了较大片金属、p 型硅和硅锗的能带图。金属的费米能被标注为 E_{Fm}。p 型硅和硅锗的费米能分别是 E_{FSi} 和 E_{FSiGe}。如图所示，尽管不必按比例绘制，但硅锗的导带边缘 E_{CSiGe} 稍许低于硅的导带边缘 E_{CSi}。此外，硅锗的价带边缘 E_{VSiGe} 高于硅的价带边缘 E_{VSi}，并基于硅锗合金中锗的百分比组成而成比例地变高。因此，硅锗合金的能带间隙小于硅的能带间隙，其程度取决于锗合金中锗的百分比组成，如参考等式（1）和（2）所介绍的。

图 6 示出了与难溶金属和 p 型硅之间的接触相关联的能带弯曲。能量势垒的大小是值得注意的。采用 p 型半导体，在平衡状态下对准费米能级要求金属侧上的正电荷和半导体侧上的负电荷。半导体通过生成其中保留电离的受主未由空穴补偿的耗尽区来调节负电荷。

图 7 示出了与难溶金属和硅锗 301 合金之间的接触相关联的能带弯曲。能量势垒的大小是值得注意的，在此情况下注意在与 p 型硅相比较时硅锗合金的能量势垒高度中的相对差。换句话说，金属半导体功函数对于金属-硅锗 301 接触比金属-p-型硅接触更小。接触的电流传导由隧穿支配。比接触电阻率关系如下：

$$\rho_c \propto e^{\frac{4\pi\Phi_B}{qh}\sqrt{\frac{m^* \varepsilon}{N_{surf}}}} \qquad (3)$$

等式（3）中的显著的变量是金属-半导体功函数Φ_B，半导体掺杂 N_{surf}，以及

半导体中的有效载流子质量 m*。如上所述，硅锗薄膜中空穴的有效质量是 $0.34m_0$ 比硅的 $0.37m_0$，其中 m_0 表示电子的静止质量。

比接触电阻率等式（3）示出金属-半导体界面的比接触电阻率主要取决于金属-半导体功函数、半导体中的掺杂密度和载流子的有效质量。改变这些变量中的任一个或者它们的组合就会影响比接触电阻率。如上所述，利用硅锗 301 减少了金属半导体功函数并减少了载流子的有效质量。在一实施例中，硅锗被进一步掺杂，如参考图 3 所述的。

硅锗 301 和硅化物 402 之间的界面可作为金属-半导体欧姆接触来进一步讨论。一开始，硅化物和半导体之间的接触处的能量势垒的效果必须从量子力学的观点来看。如本领域公知的，波粒二象性指明电子作为粒子和波两者看待以确定它的行为。硅化物-半导体界面所形成的能量势垒可以被视作有限厚度和高度的势垒。对于大于大于入射电子能量的给定势垒高度和给定势垒宽度，存在一定的概率使得电子穿过势垒并出现于另一侧。这种隧穿现象是固体中电子传导的重要机制。

更具体地，接触电阻率是电流如何容易地流过金属-半导体界面的量度。如果接触是欧姆性的，根据定义，存在从一种材料到另一种材料一本例下在硅化物 402 和硅锗 301 之间的多数载流子的不受阻碍的转移。这也可以表示为线性的电流-电压特征。在金属-半导体界面的情况下，传导机制部分由邻近于接触界面的半导体耗尽区的宽度规定。如果半导体被稍许掺杂（例如，费米能量既不接近于导带边缘能量也不接近于价带边缘能量），耗尽区变得足够宽，使得电子在两个接触材料之间转移的唯一方法是通过势垒最大值以上的热离子发射跃过势垒。或者，如果半导体被高度掺杂（费米能量接近 n 型的导带边缘能量并接近 p 型的价带边缘能量），耗尽区变得足够窄，使得场发射或载流子隧穿作为主要的传导机制。场发射和热离子发射两者都贡献跨界面的传导并可以例如通过材料选择和掺杂来调节。

图 8 示出了使用例如具有镍硅锗硅化物层 402 的硅锗 301 源极和漏极区的本发明实施例。外电阻 R_{ext}801 是源极（或漏极）接触和本征晶体管的沟道之间的总串联电阻。硅锗 301 和硅化物 402 之间的界面电阻是该总串联电阻的重要分量。通过使用硅锗与使用 p 型硅用于源极和漏极区相比减少了 R_{ext}801。此外，硅化物层 402 的难溶金属的合适选择（在一个实施例中是镍）已确保了化学和机械兼容的金属-半导体界面，它不会不利地影响 R_{ext}801，如参考图 4 所述的。

本领域的熟练技术人员将认识到所揭示实施例的优点，其中它通过使用新材料选择和处理技术减少了硅锗源极和漏极区以及它们各自的硅化物接触之间的比接触电阻率。由于接触电阻率影响晶体管的总体外电阻率，所以接触电阻率的减小有助于晶体管中整体性能的提升。

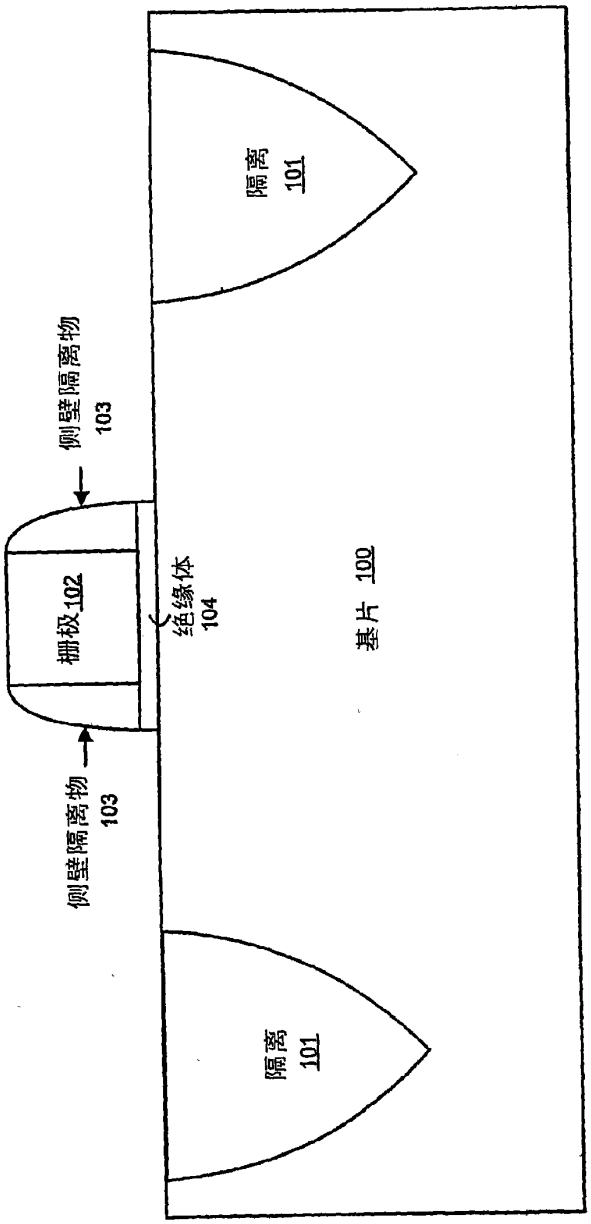


图 1a

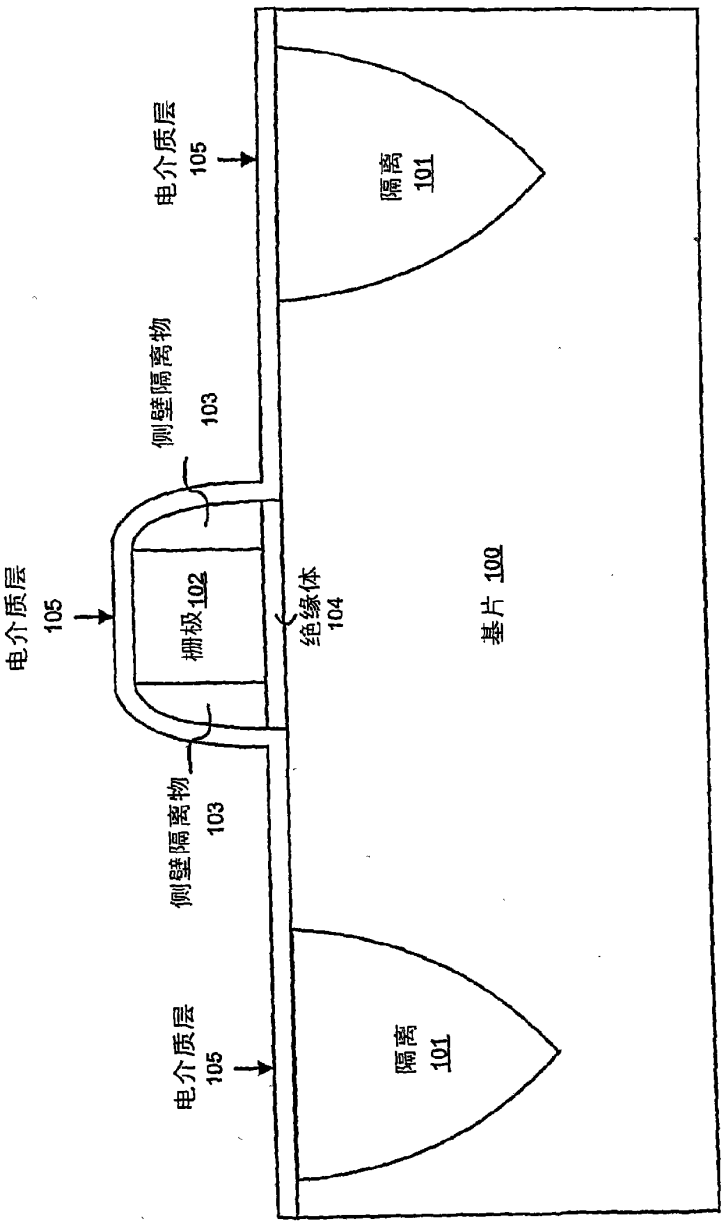

电介质层
105
电介质层
105
隔离
101
侧壁隔离物
103
侧壁隔离物
103
栅极102
绝缘体
104
基片 100
电介质层
105
隔离
101

图 1b

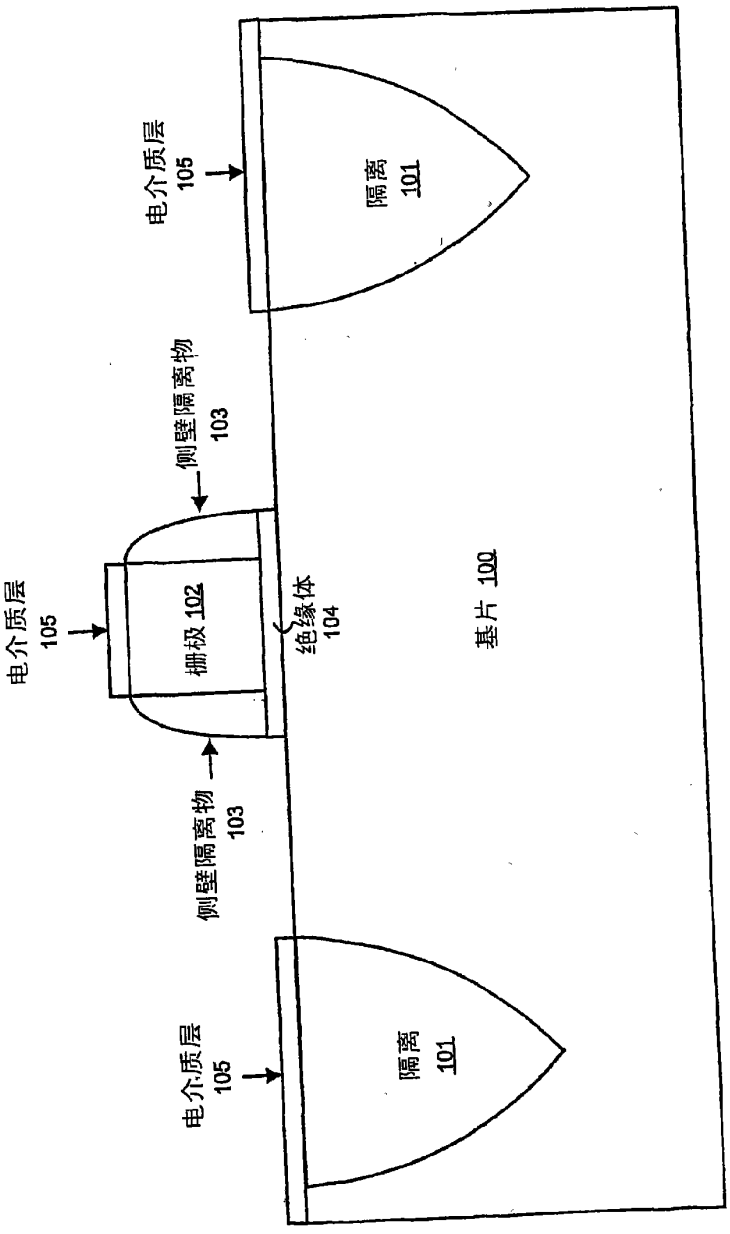

电介质层
105
隔离
101
侧壁隔离物
103
电介质层
105
栅极 102
绝缘体
104
基片 100
侧壁隔离物
103
电介质层
105
隔离
101

图 1C

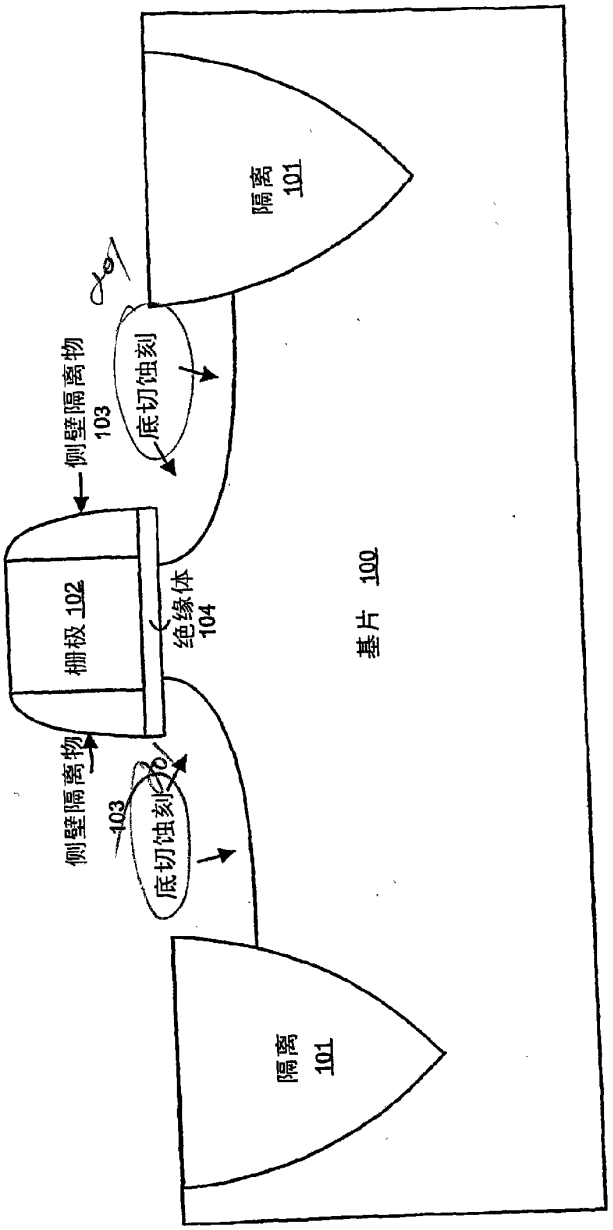

隔离
101
侧壁隔离物
103
底切蚀刻
栅极 102
绝缘体
104
基片 100
侧壁隔离物
103
底切蚀刻
隔离
101

图 2

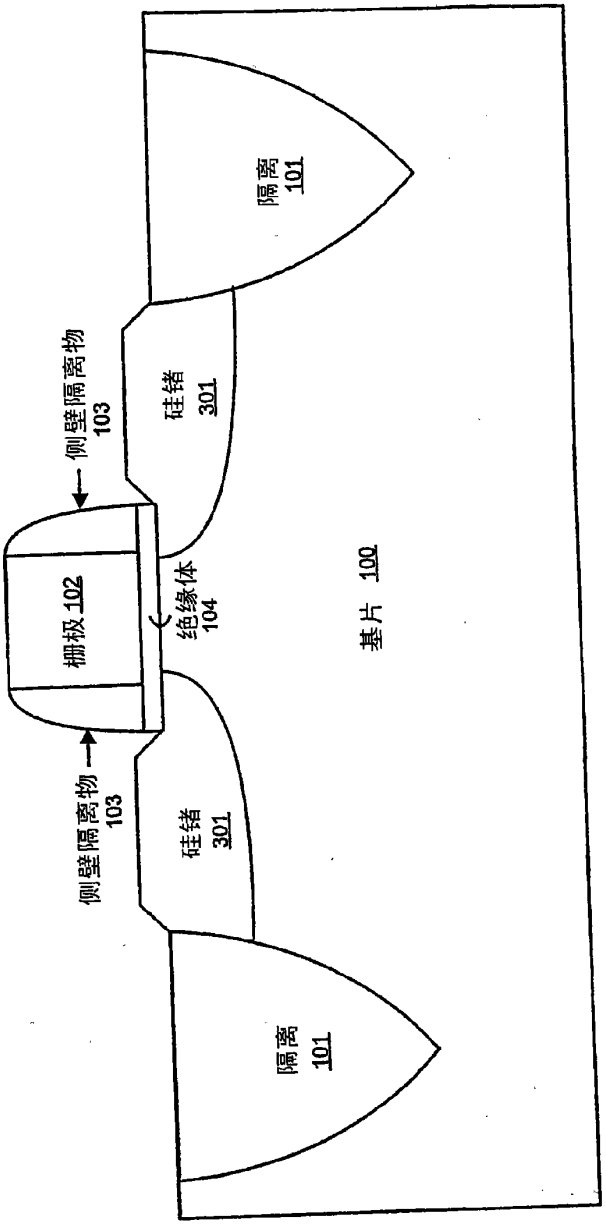

隔离
101
硅锗
301
侧壁隔离物
103
栅极 102
绝缘体
104
基片 100
侧壁隔离物
103
硅锗
301
隔离
101

图 3

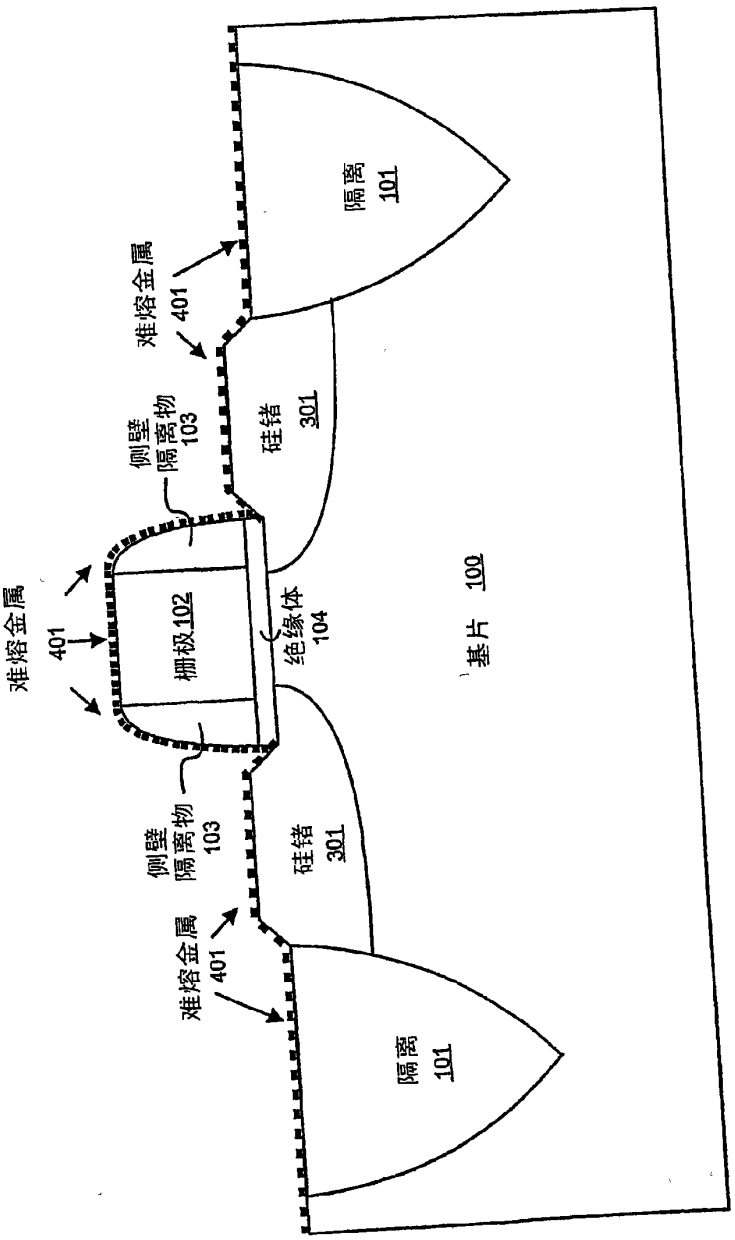

隔离
101
难熔金属
401
侧壁
隔离物
103
硅锗
301
难熔金属
401
栅极102
绝缘体
104
基片 100
侧壁
隔离物
103
硅锗
301
难熔金属
401
隔离
101

图 4a

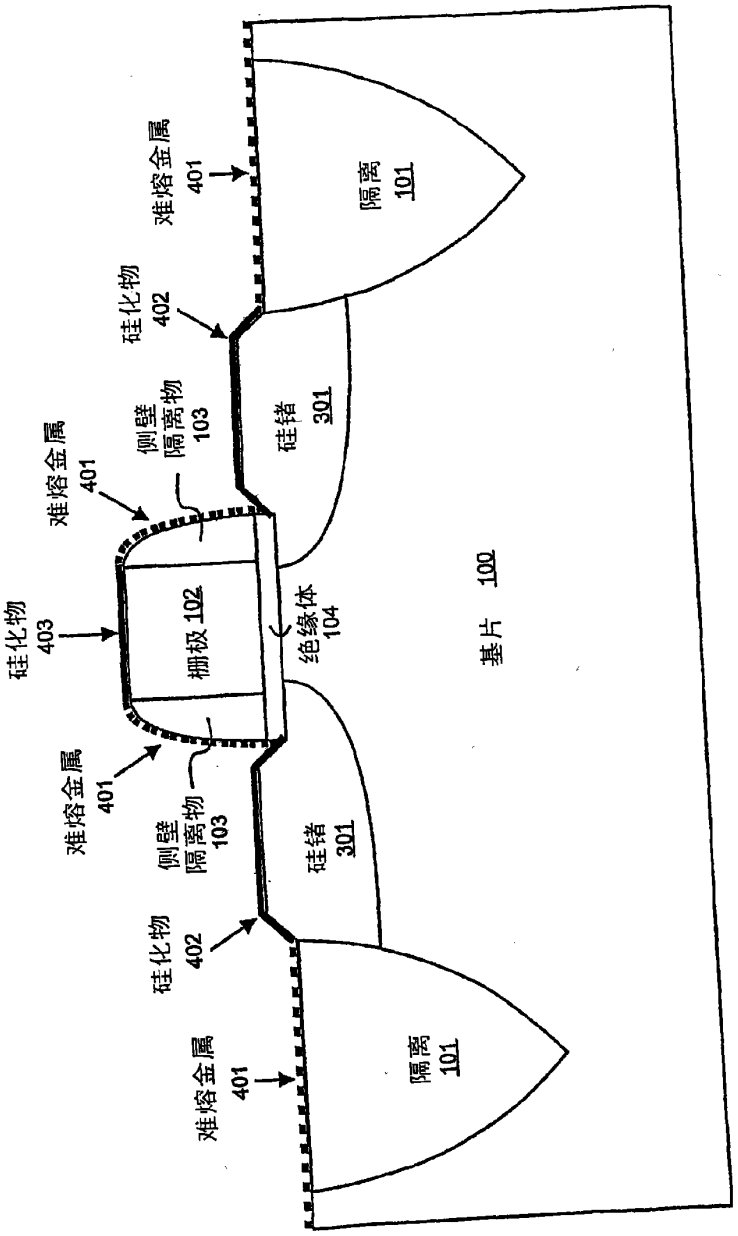

难熔金属
401
硅化物
402
侧壁
隔离物
103
难熔金属
401
硅化物
403
栅极 102
绝缘体
104
难熔金属
401
侧壁
隔离物
103
硅化物
402
难熔金属
401
隔离
101
硅锗
301
硅锗
301
隔离
101
基片 100

图 4b

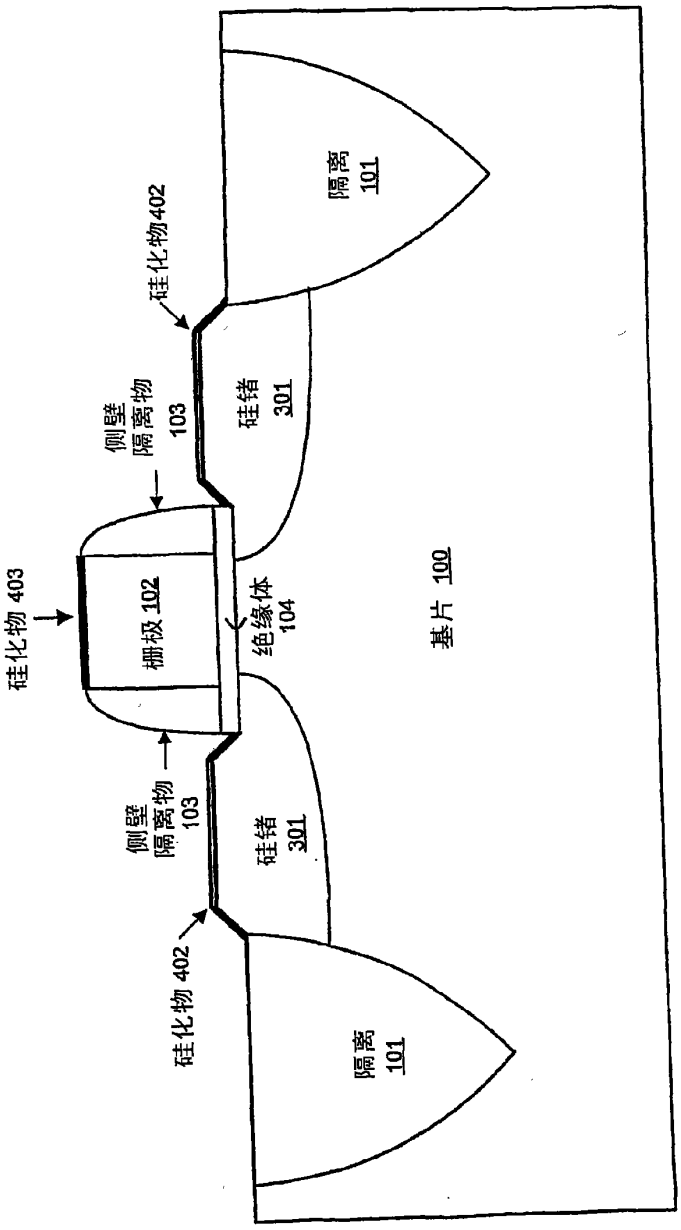

隔离
101
硅化物402
侧壁
隔离物
103
硅锗
301
硅化物 403
栅极 102
绝缘体
104
基片 100
侧壁
隔离物
103
硅锗
301
硅化物 402
隔离
101

图 4c

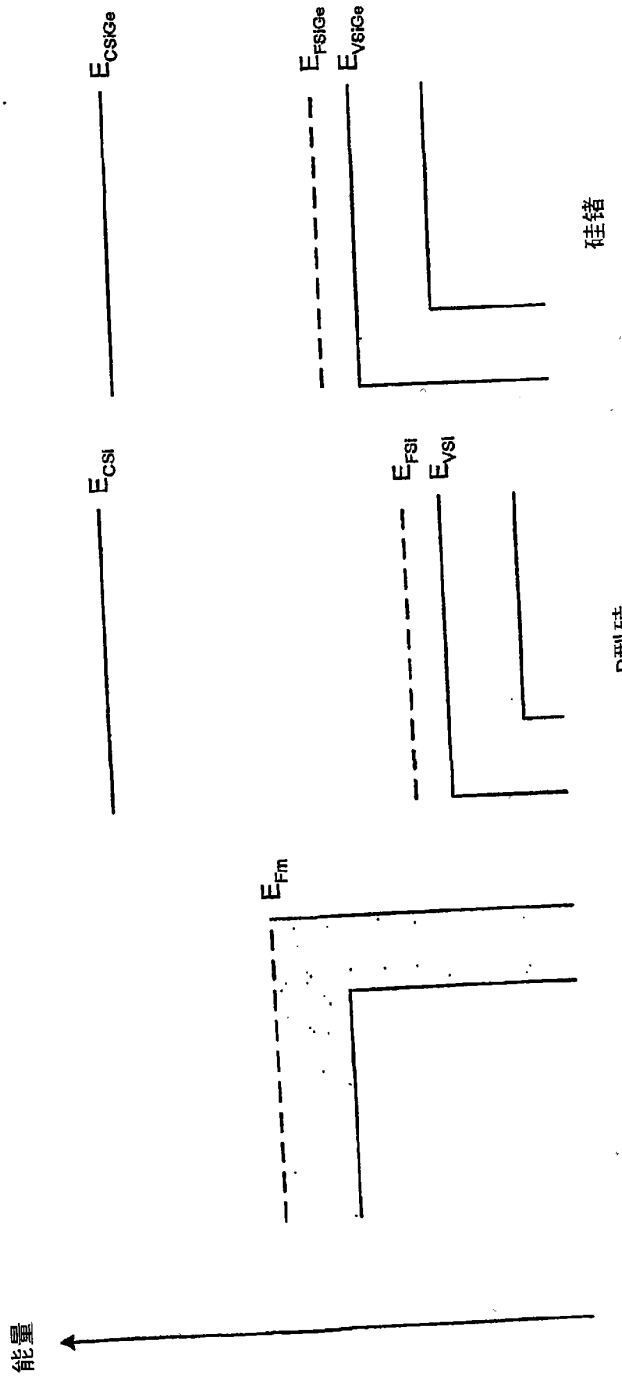


图 5

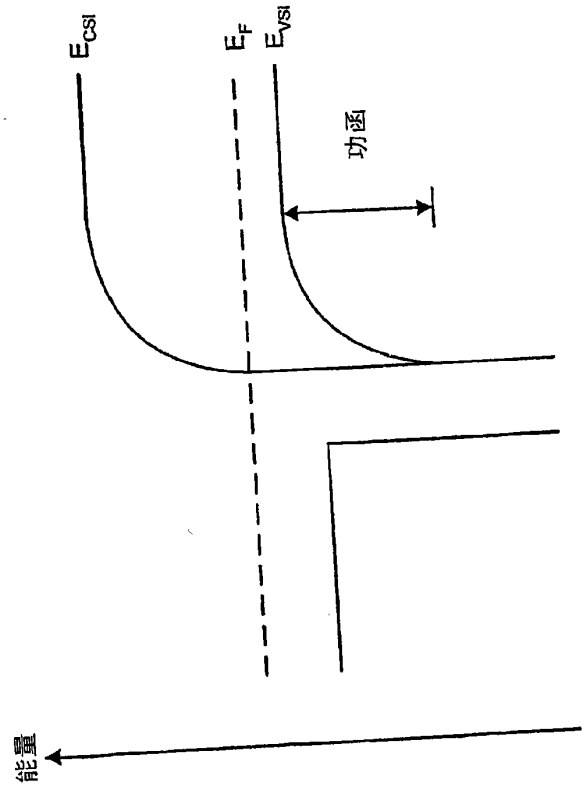


图 6

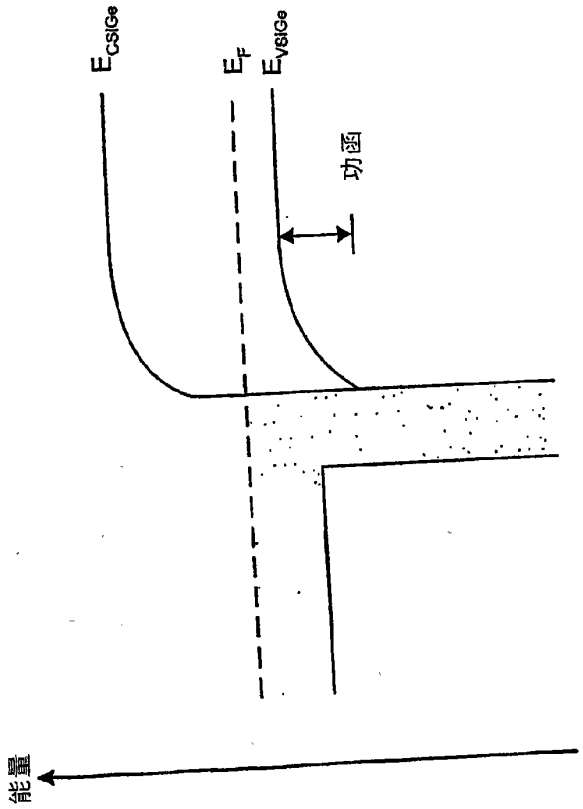


图 7

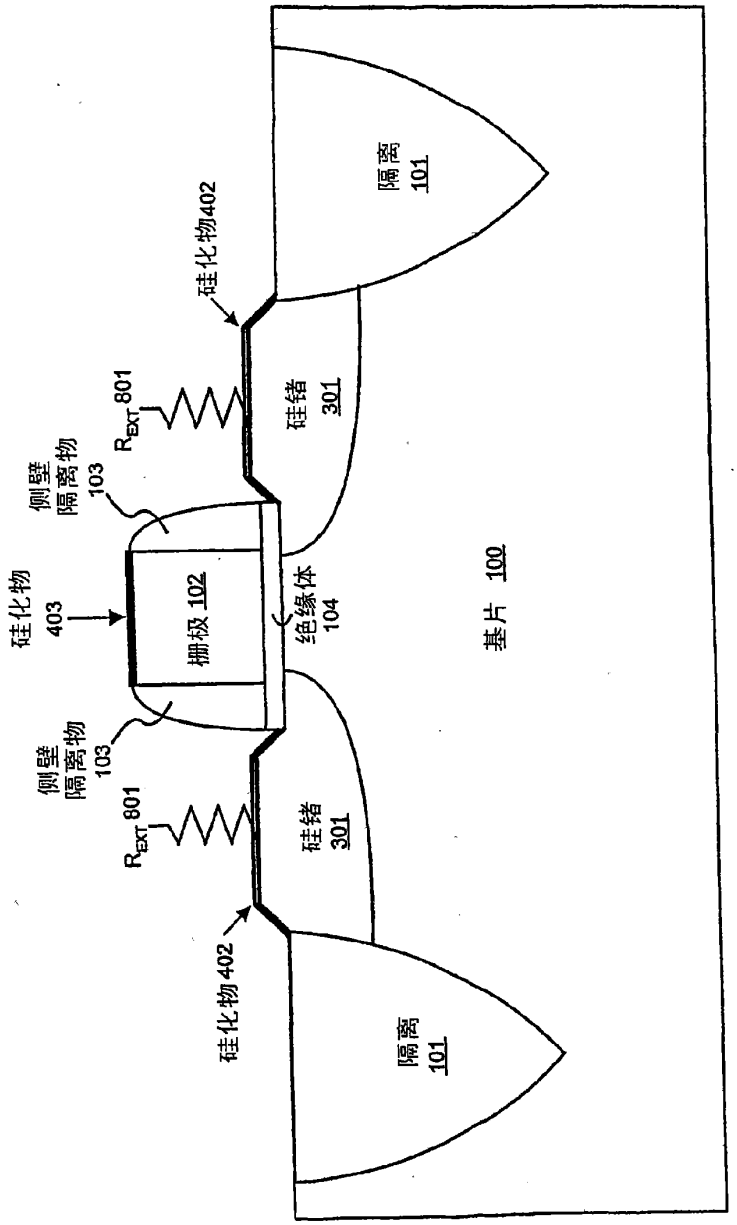

隔离
101
硅化物402
硅锗
301
R_{EXT} 801
侧壁
隔离物
103
硅化物
403
栅极 102
绝缘体
104
基片 100
侧壁
隔离物
103
R_{EXT} 801
硅锗
301
硅化物402
隔离
101

图 8

Espacenet

Bibliographic data: CN102171794 (A) — 2011-08-31

Graded high germanium compound films for strained semiconductor devices

Inventor(s): DANIELLE SIMONELLI; ANAND MURTHY ± (SIMONELLI DANIELLE, ; MURTHY ANAND)

Applicant(s): INTEL CORP ± (INTEL CORP, ; INTEL CORPORATION)

Classification: **- international:** ***H01L21/20; H01L21/336***
- cooperative: **H01L21/02381 (EP, US)**; **H01L21/0245 (EP, US)**; **H01L21/0251 (EP, US)**; **H01L21/02532 (EP, US)**; **H01L21/02579 (EP, US)**; **H01L21/0262 (EP, US)**; **H01L21/02636 (EP, US)**; **H01L21/8238 (KR)**; **H01L29/66636 (EP, US)**; **H01L29/66795 (EP, US)**; **H01L29/7834 (EP, US)**; **H01L29/7848 (EP, US)**; **H01L29/785 (EP, US)**; H01L29/517 (EP, US)

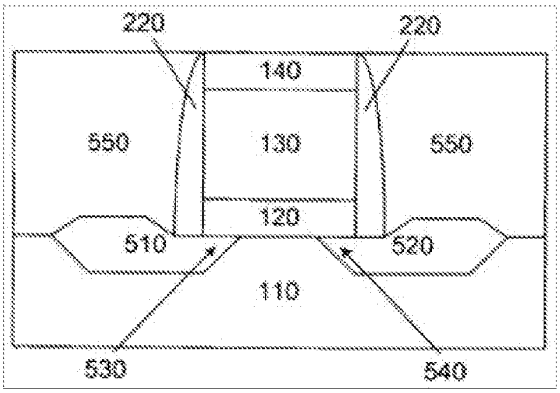
Application number: CN200980139832 20091202

Priority number(s): WO2009US66334 20091202 ; US20080316510 20081211

Also published as: CN102171794 (B) EP2356670 (A2) EP2356670 (A4) JP2012510720 (A) KR20110050713 (A) more

Abstract of CN102171794 (A)

Embodiments of an apparatus and methods for providing a graded high germanium compound region are generally described herein. Other embodiments may be described and claimed.



Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION CN102171794A

Graded high germanium compound film for strained semiconductor device

[0001]

Technical field

[0002]

The field of the invention relates generally to the field of semiconductor integrated circuit manufacturing, and more specifically but not exclusively to planar and three-dimensional complementary metal oxide semiconductor (CMOS) devices containing compound layers with graded germanium content.

[0003]

Background technique

[0004]

In a conventional metal oxide semiconductor (MOS) field effect transistor, the source, channel, and drain structures are constructed adjacent to each other in the same plane.

Typically, the gate dielectric layer is formed on the channel region and the gate electrode is deposited on the gate dielectric layer. The transistor is controlled by applying a voltage to the gate electrode, thereby allowing current to flow through the channel between the source and drain.

[0005]

An alternative to the method of constructing planar MOS transistors is to reduce certain physical barriers to reduce the scale of the planar design.

This alternative method involves constructing a three-dimensional MOS transistor in the form of a multi-gate transistor such as a double-gate field effect transistor (FinFET) or a tri-gate field effect transistor to replace the traditional planar MOS transistor.

[0006]

Three-dimensional transistor designs such as FinFETs and Tri-Gate Field Effect Transistors allow the same number of transistors to be more tightly packaged on a semiconductor chip by using vertical or angled surfaces for the gate.

Tri-gate field effect transistors include three substantially equal-length gates in place on three exposed surfaces of the body, while FinFETs include two equal-length gates in place along each side of a narrow body or fin.

[0007]

Description of the drawings

[0008]

The aforementioned various aspects and many associated advantages of the present invention will become easier to understand, because with reference to the following detailed description in conjunction with the accompanying drawings, these contents become easier to understand, where the same reference numerals denote the same parts in the accompanying drawings. Unless otherwise indicated:

[0009]

Fig. 1 is a cross-sectional view of a planar MOS device showing a gate electrode on a substrate.

[0010]

FIG. 2 is a diagram of the device of FIG. 1 having a spacer structure formed on the side of the gate electrode.

[0011]

3 is a diagram of the device of FIG. 2 after a portion of the substrate has been etched away to form source/drain and source/drain extension cavities.

[0012]

4 is a diagram of the device of FIG. 3 after wet etching the source/drain and source/drain extension cavities.

[0013]

Fig. 5 is a diagram of the device of Fig. 4 after forming source/drain and source/drain extensions.

[0014]

Figure 6 is a diagram of a multi-gate device having a dielectric layer on a multi-gate body.

[0015]

FIG. 7 is a diagram of the device of FIG. 6 after depositing a work function metal layer on a dielectric layer.

[0016]

FIG. 8 is a diagram of the device of FIG. 7 after a protective mask is formed on the work function metal layer.

[0017]

FIG. 9 is a diagram of the device of FIG. 8 after the work function metal layer is anisotropically etched to form a gate electrode.

[0018]

FIG. 10 is a diagram of the device of FIG. 9 after a gate isolation spacer structure is formed on the gate electrode.

[0019]

FIG. 11 is a diagram of the device of FIG. 10 after part of the body is removed to provide a channel region.

[0020]

FIG. 12 is a diagram of the device of FIG. 11 after forming epitaxial source/drain regions.

[0021]

Figure 13 shows a system with a central processing unit containing a graded high germanium compound film.

[0022]

Figure 14 is a diagram of a graded high germanium content silicon-germanium region on a substrate.

[0023]

FIG. 15 is a flowchart illustrating an embodiment of a manufacturing process for forming a strained semiconductor device having a silicon-germanium region with a graded high germanium content.

[0024]

Detailed ways

[0025]

In the various embodiments, various embodiments of an apparatus and method for forming a compound layer with a graded germanium content on a substrate are explained and described.

[0026]

However, those skilled in the relevant art will understand that the various embodiments may be implemented without resorting to one or more specific details or using other alternative and/or additional methods, materials, or components.

In other cases, well-known structures, materials, or operations are not shown or described in detail in order to avoid obscuring various aspects of the various embodiments of the present invention.

Likewise, for ease of explanation, specific numbers, materials, and structures are given to provide a thorough understanding of the present invention.

However, the present invention can be implemented without these specific details.

In addition, it is to be understood that the various embodiments shown in the drawings are illustrative expressions and are not necessarily drawn to scale.

[0027]

Reference throughout this specification to "one embodiment" or "an embodiment" means that a specific feature, structure, material, or characteristic described in conjunction with the embodiment is included in at least one embodiment of the present invention, but does not mean that they appear in each example.

Therefore, the phrases "in one embodiment" or "in an embodiment" appearing in various places in this specification do not necessarily refer to the same embodiment of the present invention.

In addition, in one or more embodiments, multiple specific features, structures, materials, or characteristics may be combined in any suitable manner.

In other embodiments, various additional layers and/or structures may be added and/or the described features may be omitted.

[0028]

Each operation can be expressed as multiple independent operations in turn in a way that is most helpful to the understanding of the present invention.

However, the order of presentation should not be interpreted as implying that these operations must be in a certain order.

Specifically, these operations need not be performed in the order shown.

The described operations can be performed in a different order from the previous embodiment.

In other embodiments, various additional operations can be performed and/or the described operations are omitted.

[0029]

The performance of planar and multi-gate MOS transistors can be improved by using graded high germanium compounds, such as silicon-germanium alloys in the source and drain regions of the transistor.

It will be a pioneering work in the field of semiconductor device manufacturing to provide a method for selectively forming a silicon-germanium material graded high germanium content region with a required crystal structure at a desired film growth rate.

The selective formation of a graded high-germanium content silicon-germanium zone with improved wafer uniformity in layer thickness and germanium concentration is another innovation in the industry.

In addition, it is a pioneering work in the industry to grow graded high germanium concentration silicon-germanium regions at a cost-saving growth rate in a manufacturing environment.

For example, using a strained high germanium compound film including a graded transition layer in the source/drain (S/D) region of a pMOS device can provide a combined effect of reduced contact resistance and improved mobility derived from the strained structure.

More specifically, it will be a pioneering work in the industry to provide a graded transition layer with full strain at or near the theoretical limit of germanium concentration.

These advantages can be derived from the device and method described below.

[0030]

Referring now to the drawings, FIG. 1 is a cross-sectional view of a planar MOS device 100 showing a gate stack 150 on a substrate 110.

The substrate 110 may include bulk silicon optionally having a silicon-on-insulator substructure.

Alternatively, the substrate 110 may include other materials—these materials may be combined with silicon or not—for example: germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or antimony Gallium.

Although some examples of materials that can constitute the substrate 110 are described herein, any material that can serve as a base on which a semiconductor device is constructed falls within the scope of the present invention.

[0031]

In the implementation described herein, the gate stack 150 may include a gate dielectric layer 120 and a sacrificial gate electrode 130.

In other implementations, the gate stack 150 may include a silicon dioxide gate dielectric layer and a polysilicon gate electrode.

The gate dielectric layer 120 may be formed of a material such as silicon dioxide or a high-k dielectric material.

Examples of high-k gate dielectric materials that can be used include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium, Barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

In some embodiments, the thickness of the gate dielectric layer 120 may be between about 5 angstroms and about 50 angstroms.

In other embodiments, the gate dielectric layer 120 may be subjected to additional treatment, such as annealing treatment, to improve the quality of the high-k material.

[0032]

The gate stack 150 may also include a gate hard mask layer 140 that provides certain benefits or uses during processing, such as protecting the gate electrode 130 from subsequent ion implantation processes.

In the implementation of the present invention, the hard mask layer 140 may be formed using materials traditionally used as hard masks, such as traditional dielectric materials.

After the gate stack is formed, an ion implantation process is performed to form the doped portion 210 of the substrate 110 near the gate stack 150, as shown in FIG. 2.

[0033]

FIG. 2 is a diagram of the device of FIG. 1 after forming a doped portion 210 in the substrate 110 and forming a spacer structure 220 on the side of the gate electrode 150.

When exposed to a suitable etchant, the doped portion 210 is etched at a rate higher than the etching rate of the surrounding substrate material.

For the MOS transistor being formed, one of the doped portions 210 will serve as a part of the source region, including the self-aligned epitaxial source extension.

For MOS transistors, another doped portion 210 will serve as a part of the drain region, including a self-aligned epitaxial drain extension.

In the implementation shown, the various regions of the doped portion are located under the gate dielectric layer 120.

In various implementations of the present invention, the size of the doped portion 210, including its depth, can be changed based on the needs of the MOS transistor being formed.

[0034]

The spacer structure 220 may be formed using conventional materials, including but not limited to silicon oxide or silicon nitride.

The width of the spacer structure 220 can be selected based on the design requirements of the MOS transistor being formed.

According to various implementations of the present invention, the width of the spacer structure 220 is not affected by the design constraints imposed by the shaping of the epitaxial source and drain extensions.

[0035]

After the spacer structure 220 is formed on the substrate 110, a dry etching process may be performed to etch the doped portion 210 and etch various parts of the substrate to form a cavity in which source/drain regions and source can be formed. Pole/drain extension.

The etched cavity is located near the gate stack 150.

The etched cavity may be formed at a depth between 50 nm and 1500 nm, which is deeper than the doped region.

Therefore, the etching process will remove the minimum amount of substrate material under the doped portion 210.

[0036]

The dry etching process adopts a complementary etchant prescription to the dopant used in the ion implantation process to increase the etching speed of the doped area.

This allows the etching process to remove the doped regions at a faster rate than other parts of the substrate.

Therefore, by appropriately increasing the etching speed, the etching process can remove almost all materials from the doped portion 210 before the cavity etching is completed.

This includes the portion of the doped region that undercuts the spacer structure and the gate dielectric layer, thereby defining the self-aligned extension structure of the transistor.

Increasing the etching speed of the doped portion 210 allows the etched source and drain extension cavities to undercut the spacer structure and the gate dielectric layer.

[0037]

According to an implementation of the present invention, the dry etching process may use chlorinating agents that occur in the plasma reactor.

In one implementation, the etchant formulation can be composed of a combination of NF3 and Cl2, with argon or helium as the buffer gas or carrier gas.

The flow rate of the activating etchant substance can vary between 50-200 standard cubic centimeters per minute (SCCM), and the flow rate of the carrier gas can vary between 150-400 SCCM.

High-energy plasma can be used at a power in the 700W-1100W range with a low RF bias of less than 100W.

The reactor pressure can vary from about 1 Pascal (Pa) to about 2 Pascals.

[0038]

In another implementation, the etching agent may be composed of a combination of HBr and Cl2.

The flow rate of the etchant material can vary between 40SCCM and 100SCCM.

High-energy plasma can be used at a power ranging from about 800W to about 1000W with a low RF offset of less than 100W.

The reactor pressure can vary from about 0.3 Pascal to about 0.8 Pascal.

In another implementation, the etchant chemistry can be composed of a combination of SF6 and Cl2.

The flow of SF6 can be varied between 3SCCM and 10SCCM and the flow of Cl2 can be varied between 20SCCM and 60SCCM.

High-energy plasma can be used at a power ranging from about 400W to about 900W without RF bias or with an RF bias less than 50W.

In this implementation, the SF6 flow rate and reactor pressure can be kept low to reduce the removal rate and maximize control.

For example, the reactor pressure can range from about 0.1 Pascal to about 0.5 Pascal.

In yet another implementation, the etchant chemistry may be composed of a combination of Ar and Cl2.

Here, the flow rate of the etchant substance can vary between 40 SCCM and 80 SCCM.

The medium energy plasma can be used at a power ranging from about 400W to about 800W with a high RF bias between about 100W and 200W.

The reactor pressure can range from about 1 Pascal to about 2 Pascals.

[0039]

3 is a diagram of the device of FIG. 2 after a portion of the substrate 110 is etched away to form source/drain and source/drain extension cavities.

As shown in the figure, a source region cavity 310 and a drain region cavity 320 are formed.

In addition, the source extension cavity 330 and the drain extension cavity 340 have been formed by etching the doped part 210.

Due to the use of dopant and etchant prescriptions that increase the etching rate of the doped portion 210, the thickness of the spacer structure 220 has the least influence on the etching of the source extension cavity 330 and the drain extension cavity 340.

[0040]

After the dry etching process is completed, a wet etching process may be applied to clean and further etch the source region cavity 310, the source extension cavity 330, the drain region cavity 320, and the drain extension cavity 340.

Conventional wet etching chemistries known in the industry for cleaning silicon and oxide materials can be used.

For example, a wet etching chemistry that can remove silicon along its crystal plane can be used.

[0041]

Wet etching serves at least two purposes.

First, wet etching removes impurities such as carbon, fluorine, chlorofluorocarbons, and oxides such as silicon oxide to provide a clean surface on which subsequent processing can be performed.

Secondly, wet etching removes very thin portions of the substrate along the <111> and <001> crystal planes to provide a smooth surface on which high-quality epitaxial deposition can occur.

The etched away substrate thin layer can be up to 5nm thick and can also remove residual impurities.

As shown in FIG. 4, the wet etching makes the edges of the source region cavity 310, the source extension cavity 330, the drain region cavity 320, and the drain extension cavity 340 follow the <111> and <001> crystals. noodle.

It should also be noted that the source and drain extensions 330, 340 do not have the bullet-like shape that occurs in traditional processing.

[0042]

After the etching process, the source and drain region cavities including the source and drain extensions can be filled with a compound film of, for example, a silicon germanium alloy by a selective epitaxial deposition process.

The epitaxial deposition process is used to form source and drain regions and source and drain extensions in one process.

In some implementations, the silicon alloy may be silicon germanium doped in situ, whereby the silicon germanium doped in situ may be doped with one or more of boron and/or phosphorus.

[0043]

In practice, the lattice spacing of the silicon germanium alloy material deposited in the cavity of the source and drain regions is different from the lattice spacing of the one or more materials used to form the substrate 110.

The difference in lattice spacing causes tensile or compressive stress in the channel region of the MOS transistor. This problem is compounded by the deposition of the high germanium compound alloy in the source extension cavity 330 and the drain extension cavity 340. For outstanding.

[0044]

According to some implementations of the present invention, for PMOS transistors, the source region cavity 310 and the drain region cavity 320 can be filled with a graded silicon germanium alloy, for example, a graded grade obtained according to one of the methods of the embodiment described in FIG. 15 below. Silicon germanium area with high germanium content.

The graded silicon germanium alloy can be deposited epitaxially with a graded germanium concentration ranging from 10 atomic% to 50 atomic %.

In other implementations, the graded germanium-silicon alloy can be further doped with boron in situ.

The boron concentration can vary from 2×1019/cm3-7×1020/cm3.

In this embodiment, the thickness of the graded germanium-silicon alloy can range from 40 angstroms to 1500 angstroms.

[0045]

5 is a diagram of the device of FIG. 4, in which the source region cavity 310 has been filled with the graded high germanium content silicon germanium stack 1400 described further in FIG. 14 to form the source region 510, and the drain region is recessed The cavity 320 has been filled with a graded high germanium content silicon germanium stack 1400 also further described in FIG. 14 to form the drain region 520.

The extension has been filled with a graded high germanium content silicon germanium stack 1400 to form an epitaxial source extension 530 and an epitaxial drain extension 540.

[0046]

As shown in FIG. 5, unlike the conventional source and drain terminal regions that are formed by implantation and diffusion techniques and do not have a clear boundary between the tip region and the channel region, the self-aligned, epitaxial source of the present invention The pole and drain extensions have abrupt boundaries.

Therefore, the interface between the epitaxial source/drain extension and the channel region is clearly and well defined.

One side of the interface is the epitaxially deposited doped silicon material and the other side of the interface is the substrate material constituting the channel region.

The dopants in the epitaxial source/drain extensions remain roughly or completely in the extensions and are not easily diffused into the channel region, thereby allowing the epitaxial source and drain extensions to bring heavily doped silicon materials into To a position very close to the channel region relative to traditional technology.

As understood by those skilled in the art, this in turn allows the gate length to be reduced without shortening the channel region.

[0047]

Forming the epitaxial source and drain extensions relatively close to the channel region also gives the channel greater hydrostatic stress.

This stress increases the strain in the channel, thereby increasing the mobility in the channel and increasing the drive current.

This stress is further amplified by increasing the doping of the epitaxial source and drain extensions, and the doping of the epitaxial source and drain extensions is easily controlled during the epitaxial deposition process of the graded silicon germanium alloy.

[0048]

As known by those skilled in the art, the planar MOS device 100 may undergo further MOS processing, such as replacement gate oxide process, replacement metal gate process, annealing or salicidation process, which can further improve the device and/or Provide the necessary electrical interconnections.

For example, after epitaxial deposition of the source/drain regions and source/drain extensions, an interlayer dielectric layer (ILD) can be deposited and planarized on the device.

The ILD can be formed using materials known to be suitable for the dielectric layer of integrated circuit structures, such as low-k dielectric materials.

These dielectric materials include, but are not limited to, for example, silicon dioxide (SiO2) oxides and carbon-doped oxides (CDO), silicon nitride, organic polymerization such as perfluorocyclobutane or polytetrafluoroethylene Materials, fluorosilicate glass (FSG), and organosilicate or organosilicate glass such as silsesquioxane and siloxane.

The dielectric layer may include holes or other voids to further reduce its dielectric constant.

FIG. 5 shows the ILD layer 550 that has been deposited on the planar MOS device 100.

[0049]

The present invention is not limited to the formation of planar MOS devices containing graded silicon germanium regions with high germanium content.

For example, devices with three-dimensional structures, such as tri-gate devices, can benefit from the aforementioned processes.

6-12 provide explanatory diagrams showing the formation of strain-sensitive source/drain regions in a non-planar device according to an embodiment of the present invention.

[0050]

FIG. 6 is a diagram of the multi-gate device 600 after the multi-gate dielectric layer 610 is deposited on the multi-gate body 620.

The multi-gate transistor in FIG. 6 is a tri-gate transistor with three substantially equal-length gates.

In another embodiment (not shown), the multi-gate transistor is a double-gate field effect transistor (FinFET) with two gates.

The multi-gate dielectric layer 610 may include at least one of silicon oxide or a high-K material.

High-K materials include lanthanum oxide, tantalum oxide, titanium oxide, hafnium oxide, zirconium oxide, lead zirconate titanate, barium strontium titanate, or aluminum oxide.

The multi-gate dielectric layer 610 is deposited on the multi-gate body 620 as a compliant layer using methods known to those skilled in the art, such as plasma enhanced chemical vapor deposition (PECVD), high-density chemical vapor deposition (HDCVD), Molecular organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD) or sputtering.

The multi-gate body 620 may include silicon, germanium, or III-V semiconductors, such as gallium arsenide (GaAs) and indium antimonide (InSb).

The multi-gate body 620 may be formed of an epitaxial layer, a single crystal substrate, or a silicon-on-insulator (SOI) layer.

[0051]

The diagram in FIG. 7 describes the situation of the multi-gate device 600 in FIG. 6 after the work function compliant metal layer 710 is deposited on the multi-gate dielectric layer 610 at a required thickness.

Work function metals are metals with known work functions, which are inherent characteristics of metals expressed in units of electron volts (eV).

In one embodiment, the work function metal layer 710 includes at least one of titanium nitride, tantalum nitride, or other transition metal nitrides.

The work function metal layer thickness is a function of the target threshold voltage (Vt) of the multi-gate device.

[0052]

In one embodiment, the work function metal layer is formed using a direction-sensitive physical vapor deposition (PVD) process.

The work function metal layer 710 deposited using the PVD process is characterized by a microstructure including columnar crystal grains that nucleate on the surface and grow perpendicular to the surface.

In another embodiment, a layering technique including molecular beam epitaxy (MBE), chemical vapor deposition (CVD), electroplating, or evaporation may be used to form the work function metal layer 710 with columnar grains.

[0053]

FIG. 8 shows a state of the multi-gate device 600 of FIG. 7 after a protective mask including a multi-gate electrode 810 such as polysilicon and a hard mask 820 is formed on a part of the work function metal layer 710.

The protective mask is formed by a series of deposition, photolithography, and etching processes well known to those skilled in the art.

The multi-gate electrode 810 may be doped or undoped and the hard mask 820 may include silicon nitride or silicon oxynitride.

[0054]

FIG. 9 shows the situation of the multi-gate device 600 of FIG. 8 after the exposed area of the work function metal layer 710 is anisotropically etched.

The exposed area of the work function metal layer 710 is etched using a wet etching process using a wet etchant containing alkali and oxide.

A suitable wet etching process is selectively designed to etch the work function metal layer 710 without significantly corroding the polysilicon 810 or the hard mask 820.

The base may include at least one of ammonium hydroxide (NH4OH), tetramethylammonium hydroxide (TMAH), or potassium hydroxide (KOH).

The oxide may include at least one of hydrogen peroxide (H2O2) or ozone (O3).

Etching the work function metal layer 710 anisotropically means that the etching rate in the direction perpendicular to the surface is much higher than in the direction parallel to the surface.

Since the etching rate of the work function metal layer 710 in a direction perpendicular to the gate surface is much higher than the etching rate of the work function metal layer 710 in a direction parallel to the gate surface, the work function metal layer 710 is anisotropically etched.

This allows the protected area of the work function metal layer 710 to remain substantially as it is while the exposed area of the work function metal layer 710 is etched away by the wet etchant.

[0055]

FIG. 10 is a diagram of the device of FIG. 9 after a gate insulating spacer structure 1010 is formed near the multi-gate electrode 810.

The gate isolation spacer structure 1010 protects the multi-gate electrode 810, the work function metal layer 710, and the multi-gate dielectric layer 610 in the subsequent processing.

[0056]

FIG. 11 is a diagram of the device of FIG. 10 after removing a portion of the multi-gate body 620 to provide a multi-gate channel region 1110.

FIG. 12 is a diagram of the device of FIG. 11 after the source and drain regions 1210 are epitaxially formed.

The epitaxially formed source/drain region 1210 is formed by using a graded high germanium content silicon germanium film stack.

The epitaxially formed source/drain regions 1210 can use, for example, a graded high-germanium content silicon germanium film laminate made according to one or more methods in the embodiment described in FIG. 15 as further described in FIG. 14 1400 formed.

[0057]

FIG. 13 shows a communication system 1300 having a central processing unit (CPU) 1310 for processing data. The central processing unit 1310 is composed of transistors having a graded high germanium content silicon germanium region according to an embodiment. constitute.

The communication system 1300 may include a motherboard 1320 having a CPU 1310 and a networking interface 1330 coupled to a bus 1340.

More specifically, the CPU 1310 may include a graded silicon germanium region with high germanium content and/or its manufacturing method.

According to the occasion, the communication system 1300 may additionally include other components, including but not limited to volatile and non-volatile memory, graphics processor, digital signal processor, cryptographic processor, chipset, mass storage (such as hard disk, compact disk (CD), digital versatile disc (DVD), etc.) and others.

One or more of these components may also include the previously described graded high germanium content silicon germanium region and/or its manufacturing method.

In various embodiments, the communication system 1300 may be a personal digital assistant (PDA), mobile device, tablet computing device, laptop computing device, desktop computing device, set-top box, entertainment control unit, digital camera, digital video recorder, CD player, DVD player or other similar digital device.

[0058]

FIG. 15 is a flowchart describing one embodiment of a manufacturing process of a strained semiconductor device used to form a graded high germanium content silicon germanium stack 1400 having the crystal structure shown in FIG. 14.

In one embodiment, the graded high germanium content silicon germanium stack 1400 includes a carrier gas such as hydrogen (H2) at a flow rate ranging from 10-40 standard liters per minute (slm) at 10-150 Torr (T A stack is grown on the substrate 110 through an epitaxial deposition process using a deposition tool such as Applied Materials Centura or ASM Epsilon tool under varying pressures between).

[0059]

In step 1500, the bottom layer is preferably selectively formed on the exposed area of the substrate 110.

In one embodiment, the bottom layer is silicon germanium with a relatively low germanium content ranging between 20-25 atomic weight% and deposited for up to 10-30 seconds to provide a final thickness range ranging between Seed layer 1410.

The silicon germanium seed layer 1410 is optionally doped with boron to a concentration in the range of 5.0×1019 atoms/cm3-1.5×1020 atoms/cm3.

The silicon germanium seed layer 1410 may be deposited in a temperature range of 700-800 degrees Celsius (°C) or more preferably between 745-765°C.

In addition, the silicon germanium seed layer 1410 can be formed using a process gas mixture containing hydrogen chloride (HCl), dichlorosilane (DCS), germane (GeH4), and diborane (B2H6), wherein the flow rate of HCl is 20-200 standard cubic meters Centimeters per minute (sccm), the DCS flow rate is between 10-100 sccm, the germane flow rate using 1% germane and hydrogen balance is between 20-200 sccm, and the diborane flow rate is between 10-75 sccm.

[0060]

In step 1510, a transition layer 1420 is selectively formed on the silicon germanium seed layer 1410 to provide a very gentle transition from the base nucleus layer of the silicon germanium seed layer 1410 to the high germanium content layer 1430, for example.

In one embodiment, the lower portion of the transition layer 1420 adjacent to and/or close to the silicon germanium seed layer 1410 may have a germanium content substantially equal to the silicon germanium seed layer 1410 at the silicon germanium seed layer 1410/transition layer 1420 interface, ie 20-25 atomic weight%.

In addition, the transition layer 1420 adjacent to and/or close to the upper part of the high germanium content layer 1430 may have a germanium content substantially equal to the high germanium content layer 1430 at the interface of the transition layer 1420/high germanium content layer 1430, that is, approximately 40-55 atomic weight. %between.

The thickness of the transition layer 420 can vary between and .

[0061]

The transition layer 1420 can be formed by an epitaxial growth process in a dynamic manner in which the processing temperature is gradually decreased from the starting temperature, which is substantially equal to the forming temperature of the silicon germanium seed layer 1410, and varies between 700-800°C or better The ground varies between 745-765°C.

The forming temperature decreases from the starting temperature to the ending temperature in a substantially linear manner.

The termination temperature or the second temperature is approximately 25-100°C lower than the starting temperature or the first temperature in one embodiment, or more preferably approximately 45-55°C lower than the starting temperature or the first temperature.

In one embodiment, the transition layer 1420 is deposited for a period of time varying between 20-60 seconds.

[0062]

The transition layer 1420 is further epitaxially formed by decreasing the flow rate of the gas mixture of DCS, HCl, and GeH4 from a higher flow rate to a lower flow rate during the formation of the transition layer 1420.

If the transition layer 1420 is doped, the diborane flow rate is increased while the transition layer 1420 is formed to provide a boron concentration substantially equal to or greater than 2.0×1020 atoms/cm3 at or near the interface of the transition layer 1420/high germanium content layer 1430 .

In this embodiment, the formation of the transition layer 1420 provides a graded silicon germanium film selectively formed at a growth rate of approximately NER7_/min equal to or less than 2% film relaxation and healthy film morphology.

[0063]

In step 1520, a high germanium content layer 1430 is selectively formed on the transition layer 1420 to provide a strained transistor structure.

In one embodiment, the high germanium content layer 1430 is formed while maintaining the process recipe parameters constant after the final partial formation of the transition layer 1420.

In this embodiment, the high germanium content layer 1430 is formed with a thickness between and the germanium content varies between 40-55 atomic weight %.

The high germanium content layer 1430 can be selectively doped with boron to a concentration of 2.0×1020 atoms/cm3-3.0×1020 atoms/cm3.

[0064]

For the sake of understanding and illustration, the foregoing description of the embodiments of the present invention has been given.

It is not intended to be exhaustive or to limit the invention to the precise form disclosed.

The specification and the following claims include terms, such as left, right, top, bottom, top, bottom, top, bottom, first, second, etc., which are for descriptive purposes only and are not construed as limiting.

For example, the term indicating the relative vertical position refers to the situation where the device side (or active surface) of the substrate or integrated circuit is on the "top" surface of the substrate; the substrate can be in practically any orientation to be in the standard ground coordinate system of the reference Make the "top" side of the substrate lower than the "bottom" side and still fall within the meaning of the term "top".

The term "on" as used herein (including in the claims) does not mean that the first layer "on" on the second layer is directly on or in direct contact with the second layer, unless this is specifically stated There can be a third layer or other structure between the first layer and the second layer on the first layer.

The embodiments of the devices or articles described herein can be manufactured, used, or transported in multiple locations and orientations.

[0065]

Those skilled in the art can understand that many modifications and changes are possible in view of the foregoing teachings.

Those skilled in the art can find many equivalent combinations and substitutions of the components shown in the drawings.

Therefore, the scope of the present invention is not limited by the detailed description, but by the appended claims.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS CN102171794A

1.

A method of forming a crystalline compound film includes:

Selectively form a seed layer with low germanium content;

Selectively forming a transition layer on the low germanium content seed layer, the transition layer being formed while decreasing the processing temperature from the first temperature to the second temperature; and

A high germanium content layer is selectively formed on the transition layer.

2.

The method of claim 1, wherein the transition layer is formed while decreasing the flow rate of dichlorosilane, hydrogen chloride, and germane from a higher flow rate to a lower flow rate.

3.

The method of claim 2, wherein the transition layer is formed while increasing the flow rate of diborane from a lower flow rate to a higher flow rate.

4.

The method of claim 3, wherein the first temperature is selected from a range between 700°C and 800°C.

5.

The method of claim 4, wherein the second temperature is 25-100°C lower than the first temperature.

6.

6. The method of claim 5, wherein the low germanium content seed layer is doped with boron to a concentration in the range of 5.0×1019 atoms/cm3-1.5×1020 atoms/cm3.

7.

7. The method of claim 6, wherein the high germanium content layer is doped with boron to a concentration in the range of 2.0×1020 atoms/cm3-3.0×1020 atoms/cm3.

8.

One method includes:

Forming a gate stack and a pair of spacer structures on the multi-gate body, wherein the spacer structures are formed on laterally opposite sides of the gate stack;

Etching the multi-gate body in a region adjacent to the spacer structure; and

A graded silicon germanium stack with high germanium content is selectively deposited to form source and drain regions directly adjacent to the multi-gate body.

9.

8. The method of claim 8, wherein the graded high germanium content silicon germanium stack is composed of a silicon germanium seed layer, a transition layer and a high germanium content layer.

10.

9. The method of claim 9, wherein the transition layer is formed while decreasing the flow rate of dichlorosilane, hydrogen chloride, and germane from a higher flow rate to a lower flow rate.

11.

The method of claim 10, wherein the transition layer is formed while increasing the flow rate of diborane from a lower flow rate to a higher flow rate.

12.

The method of claim 12, wherein the formation of the transition layer starts at a first temperature selected from a range between 700°C and 800°C.

13.

The method of claim 12, wherein the formation of the transition layer ends at a second temperature selected from a range of 25-100°C lower than the first temperature.

14.

A type of transistor including:

The gate stack formed on the substrate;

Spacer structures formed on laterally opposite sides of the gate stack; and

A source region and a drain region formed on the substrate adjacent to the spacer structure and below the spacer structure, the source region and the drain region including a silicon germanium seed layer, a transition layer, and a high Germanium content layer.

15.

The transistor according to claim 14, wherein the lower part of the transition layer has a germanium content in the range of 20-25 atomic weight% and the upper part of the transition layer has a germanium content in the range of 40-55 atomic weight% The germanium content in the range between.

16.

The transistor according to claim 14, wherein the silicon germanium seed layer is doped with boron to a concentration in the range of 5.0×1019 atoms/cm3-1.5×1020 atoms/cm3.

17.

15. The transistor of claim 15, wherein the high germanium content layer is doped with boron to a concentration in the range of 2.0×1020 atoms/cm3-3.0×1020 atoms/cm3.

18.

The transistor according to claim 15, wherein the thickness of the transition layer is selected from a range between and .

19.

The transistor of claim 18, wherein the thickness of the silicon germanium seed layer is selected from a range between .

20.

The transistor of claim 19, wherein the thickness of the high germanium content layer is selected from a range between .

(19)中华人民共和国国家知识产权局

(12)发明专利申请

(10)申请公布号 CN 102171794 A
(43)申请公布日 2011.08.31

(21)申请号 200980139832.9
(22)申请日 2009.12.02
(30)优先权数据
12/316,510 2008.12.11 US
(85)PCT申请进入国家阶段日
2011.04.01
(86)PCT申请的申请数据
PCT/US2009/066334 2009.12.02
(87)PCT申请的公布数据
WO2010/068530 EN 2010.06.17
(71)申请人 英特尔公司
地址 美国加利福尼亚州
(72)发明人 D·西蒙耐利 A·莫西
(74)专利代理机构 上海专利商标事务所有限公司 31100
代理人 钱慰民
(51)Int.Cl.
H01L 21/20(2006.01)
H01L 21/336(2006.01)

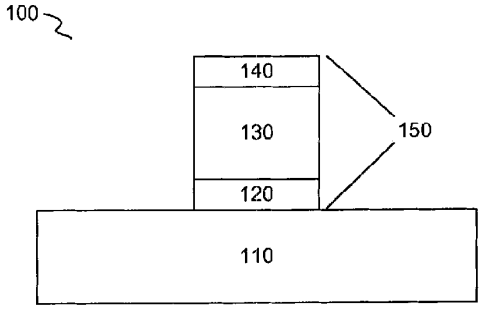
权利要求书 2 页 说明书 8 页 附图 7 页

(54)发明名称

用于应变半导体器件的渐变高锗化合物膜

(57)摘要

本文总体披露了提供渐变的高锗化合物区的装置和方法的实施例。描述和要求保护其它的实施例。



CN 102171794 A

1. 一种形成晶体化合物膜的方法，包括：

选择性地形成低锗含量籽晶层；

在所述低锗含量籽晶层上选择性地形成过渡层，所述过渡层是在将处理温度从第一温度递减至第二温度的同时形成的；以及

在所述过渡层上选择性地形成高锗含量层。

2. 如权利要求 1 所述的方法，其特征在于，所述过渡层是在将二氯硅烷、氯化氢、锗烷流量从较高流量递减至较低流量的同时形成的。

3. 如权利要求 2 所述的方法，其特征在于，所述过渡层是在将乙硼烷流量从较低流量增大至较高流量的同时形成的。

4. 如权利要求 3 所述的方法，其特征在于，所述第一温度是从 700℃和 800℃之间的范围内选择的。

5. 如权利要求 4 所述的方法，其特征在于，所述第二温度比所述第一温度低 25-100℃之间。

6. 如权利要求 5 所述的方法，其特征在于，所述低锗含量籽晶层掺杂硼至 5.0×10^{19} 原子 /cm^3-1.5×10^{20} 原子 /cm^3 之间范围的浓度。

7. 如权利要求 6 所述的方法，其特征在于，所述高锗含量层掺杂硼至 2.0×10^{20} 原子 /cm^3-3.0×10^{20} 原子 /cm^3 之间范围的浓度。

8. 一种方法，包括：

在多栅极本体上形成栅极叠层和一对间隔结构，其中所述间隔结构形成在所述栅极叠层的横向相对两侧上；

在毗邻所述间隔结构的区域蚀刻所述多栅极本体；以及

选择性地沉积渐变的高锗含量的硅锗叠层以形成直接毗邻于所述多栅极本体的源极区和漏极区。

9. 如权利要求 8 所述的方法，其特征在于，所述渐变的高锗含量硅锗叠层由硅锗籽晶层、过渡层和高锗含量层构成。

10. 如权利要求 9 所述的方法，其特征在于，所述过渡层是在将二氯硅烷、氯化氢、锗烷流量从较高流量递减至较低流量的同时形成的。

11. 如权利要求 10 所述的方法，其特征在于，所述过渡层是在将乙硼烷流量从较低流量增大至较高流量的同时形成的。

12. 如权利要求 12 所述的方法，其特征在于，形成所述过渡层开始于从 700℃和 800℃之间的范围内选择的第一温度。

13. 如权利要求 12 所述的方法，其特征在于，形成所述过渡层结束于从比所述第一温度低 25-100℃之间的范围内选择的第二温度。

14. 一种晶体管，包括：

形成在衬底上的栅极叠层；

形成在所述栅极叠层的横向相对两侧上的间隔结构；以及

形成在毗邻于所述间隔结构且在所述间隔结构下方的衬底上的源极区和漏极区，所述源极区和所述漏极区包括硅锗籽晶层、过渡层以及高锗含量层。

15. 如权利要求 14 所述的晶体管，其特征在于，所述过渡层的下部具有在 20-25 原子重

量%之间的范围内的锗含量并且所述过渡层的上部具有在 40-55 原子重量%之间的范围内的锗含量。

16. 如权利要求 14 所述的晶体管，其特征在于，所述硅锗籽晶层掺杂硼至 5.0×10^{19} 原子 /cm^3-1.5×10^{20} 原子 /cm^3 之间范围的浓度。

17. 如权利要求 15 所述的晶体管，其特征在于，所述高锗含量层掺杂硼至 2.0×10^{20} 原子 /cm^3-3.0×10^{20} 原子 /cm^3 之间范围的浓度。

18. 如权利要求 15 所述的晶体管，其特征在于，所述过渡层的厚度是从150Å和450Å之间的范围内选择的。

19. 如权利要求 18 所述的晶体管，其特征在于，所述硅锗籽晶层的厚度是从100Å-300Å之间的范围内选择的。

20. 如权利要求 19 所述的晶体管，其特征在于，所述高锗含量层的厚度是从300Å-600Å之间的范围内选择的。

用于应变半导体器件的渐变高锗化合物膜

技术领域

[0001] 本发明领域总的涉及半导体集成电路制造领域，更具体地但非排它地涉及包含具有渐变锗含量的化合物层的平面和三维互补金属氧化物半导体 (CMOS) 器件。

背景技术

[0002] 在传统金属氧化物半导体 (MOS) 场效应晶体管中，源极、沟道和漏极结构彼此毗邻地构造在同一平面内。典型地，栅极介电层形成在沟道区上并且栅极电极沉积在栅极介电层上。通过将电压施加于栅极电极来控制晶体管，由此使电流流过源极和漏极之间的沟道。

[0003] 采用构造平面 MOS 晶体管的方法的一种替代方法以减轻某些物理势垒来减小平面设计的规模。该替代方法涉及以例如双栅极场效应晶体管 (FinFET) 或三栅极场效应晶体管的多栅极晶体管的形式构建三维 MOS 晶体管以取代传统的平面 MOS 晶体管。

[0004] 例如 FinFET 和三栅极场效应晶体管的三维晶体管设计允许通过对栅极使用垂直或成角度的表面来将同样数量的晶体管更紧密地封装在半导体芯片上。三栅极场效应晶体管包括在本体的三个露出表面上就位的三个基本相等长度的栅极，而 FinFET 包括沿狭窄本体或鳍片各边就位的两个相等长度的栅极。

附图说明

[0005] 本发明前述各个方面和许多伴生的优势将变得更为易懂，因为结合附图参照下面的详细说明，这些内容变得更易于理解，其中相同的标记在各附图中表示相同的部分，除非另有说明：

[0006] 图 1 是示出衬底上的栅极电极的平面 MOS 器件的横截面图。

[0007] 图 2 是图 1 的器件在栅极电极的边上形成有间隔结构的示图。

[0008] 图 3 是图 2 的器件在蚀刻掉一部分衬底以形成源极 / 漏极和源极 / 漏极延伸部凹腔后的示图。

[0009] 图 4 是图 3 的器件在湿蚀刻源极 / 漏极和源极 / 漏极延伸部凹腔后的示图。

[0010] 图 5 是图 4 的器件在形成源极 / 漏极和源极 / 漏极延伸区后的示图。

[0011] 图 6 是在多栅极本体上具有介电层的多栅极器件的示图。

[0012] 图 7 是图 6 的器件在介电层上沉积功函数金属层之后的示图。

[0013] 图 8 是图 7 的器件在功函数金属层上形成保护掩模后的示图。

[0014] 图 9 是图 8 的器件在各向异性地蚀刻功函数金属层以形成栅极电极之后的示图。

[0015] 图 10 是图 9 的器件在栅极电极上形成栅极隔离间隔结构后的示图。

[0016] 图 11 是图 10 的器件在除去部分本体以提供沟道区后的示图。

[0017] 图 12 是图 11 的器件在形成外延源极 / 漏极区后的示图。

[0018] 图 13 示出具有含渐变的高锗化合物膜的中央处理单元的系统。

[0019] 图 14 是衬底上的渐变高锗含量硅 - 锗区的示图。

[0020] 图 15 是表述用来形成具有渐变高锗含量的硅 - 锗区的应变半导体器件的制造工艺的一个实施例的流程图。

具体实施方式

[0021] 在各实施例中，解说和描述了在衬底上形成具有渐变锗含量的化合物层的装置和方法的各实施例。

[0022] 然而，相关领域内技术人员将理解，可不借助一个或多个特定细节或者采用其它替代和 / 或附加的方法、材料或组分来实现各个实施例。在其它情形下，未详细示出或描述公知的结构、材料或操作以避免使本发明各实施例的各个方面晦涩。同样，为便于解释，给出具体的数目、材料和结构以提供对本发明的透彻理解。然而，本发明没有这些具体细节也可实施。此外要理解，附图中示出的各个实施例是解说性表达并且不一定按比例绘制。

[0023] 该说明书中通篇对“一个实施例”或“一实施例”的引用表示结合该实施例描述的具体特征、结构、材料或特性包含在本发明的至少一个实施例中，但不代表它们出现在每个实施例中。因此，本说明书中多处出现的短语“在一个实施例中”或“在一实施例中”不一定指本发明的同一实施例。此外，在一个或多个实施例中，可以任何适宜方式组合多个具体特征、结构、材料或特性。在其它实施例中可加入各个附加层和 / 或结构和 / 或省去所描述的特征。

[0024] 各个操作可以最有助于本发明理解的方式表述为轮流的多个独立操作。然而，表述顺序不应当解释成意指这些操作一定要按照某种顺序。具体地说，这些操作不需要按所表示的顺序进行。所描述的操作可以与前述实施例不同的顺序执行。在其它实施例中可执行各个附加操作和 / 或省去所描述的操作。

[0025] 平面和多栅极 MOS 晶体管的性能可通过采用渐变高锗含量化合物得以改善，例如晶体管的源极区和漏极区中的硅 - 锗合金。提供以合需的膜生长速率选择性地形成具有要求晶体结构的硅 - 锗材料的渐变高锗含量区的方法将会是半导体器件制造领域中的一个创举。选择性地形成在层厚度的晶片均匀性和锗浓度方面有改善的渐变高锗含量硅 - 锗区则是业内的另一创举。此外，使渐变的高锗浓度硅 - 锗区以在制造环境中节约成本的生长速率生长是业内的一个创举。例如，在 pMOS 器件的源极 / 漏极 (S/D) 区中使用包括渐变过渡层的应变高锗化合物膜能提供源自应变结构的接触电阻减小和迁移性提高的组合效果。更具体地，提供在锗浓度的理论极限或其附近具有完全应变的渐变过渡层将是业内的一个创举。这些优点可从下面描述的装置和方法中得出。

[0026] 现在参见附图，图 1 是示出衬底 110 上的栅极叠层 150 的平面 MOS 器件 100 的横截面图。衬底 110 可包括可选择地具有绝缘体上硅 (SOI) 结构的块硅。替代地，衬底 110 可包括其它材料——这些材料可与硅结合或不与硅结合——例如：锗、锑化铟、碲化铅、砷化铟、磷化铟、砷化镓或锑化镓。尽管在此描述了可构成衬底 110 的材料的一些示例，但可充当在其上构建半导体器件的基底的任何材料都落在本发明的范围内。

[0027] 在本文描述的实现中，栅极叠层 150 可包括栅极介电层 120 和牺牲栅极电极 130。在其它实现中，栅极叠层 150 可包括二氧化硅栅极介电层和多晶硅栅极电极。栅极介电层 120 可由例如二氧化硅或高 k 介电材料的材料形成。可采用的高 k 栅极介电材料的示例包括但不局限于，氧化铪、氧化铪硅、氧化镧、氧化镧铝、氧化锆、氧化锆硅、氧化钽、氧化钛、氧

化钡锶钛、氧化钡钛、氧化锶钛、氧化钇、氧化铝、氧化铅钪钽以及铌酸铅锌。在一些实施例中，栅极介电层 120 的厚度可在约 5 埃(Å)至约 50 埃之间。在其它实施例中，可对栅极介电层 120 作附加处理，例如退火处理以提高高 k 材料的质量。

[0028] 栅极叠层 150 也可包括栅极硬掩模层 140，该栅极硬掩模层 140 提供加工过程中的某些益处或用途，例如保护栅极电极 130 免受之后离子注入工艺的影响。在本发明的实现中，该硬掩模层 140 可使用传统用作硬掩模的材料——例如传统介电材料——来形成。在形成栅极叠层后，执行离子注入工艺以形成衬底 110 在栅极叠层 150 附近的掺杂部分 210，如图 2 所示。

[0029] 图 2 是图 1 的器件在衬底 110 中形成掺杂部分 210 并在栅极电极 150 的边上形成间隔结构 220 之后的示图。当暴露于适当的蚀刻剂时，掺杂部分 210 以高于周围衬底材料的蚀刻速率的速率蚀刻。对于正在成形的 MOS 晶体管来说，其中一个掺杂部分 210 将充当源极区的一部分，包括自对准外延源极延伸部。对于 MOS 晶体管来说，另一掺杂部分 210 将充当漏极区的一部分，包括自对准外延漏极延伸部。在所示实现中，掺杂部分的各个区域位于栅极介电层 120 之下。在本发明的各种实现中，掺杂部分 210 的尺寸——包括其深度——可基于正在成形的 MOS 晶体管的需求而改变。

[0030] 间隔结构 220 可使用传统材料形成，包括但不局限于氧化硅或氮化硅。可基于正在成形的 MOS 晶体管的设计需求来选择间隔结构 220 的宽度。根据本发明的各种实现，间隔结构 220 的宽度不受外延源极和漏极延伸部的成形所强加的设计约束的影响。

[0031] 在间隔结构 220 形成在衬底 110 之后，可执行干蚀刻工艺以蚀刻掺杂部分 210 并蚀刻衬底的各个部分以形成凹腔，在所述凹腔中可形成源极 / 漏极区和源极 / 漏极延伸部。经蚀刻的凹腔位于栅极叠层 150 附近。经蚀刻的凹腔可形成在 50nm 和 1500nm 之间的深度，该深度比掺杂区更深。因此蚀刻工艺将去除掺杂部分 210 下面的最少量衬底材料。

[0032] 干蚀刻工艺采用对用于离子注入工艺的掺杂剂作出互补的蚀刻剂处方以增大掺杂区的蚀刻速度。这允许蚀刻工艺以比衬底其它部分更快的速度去除掺杂区。因而，通过适当增加蚀刻速度，蚀刻工艺能在凹腔蚀刻完成前从掺杂部分 210 去除几乎全部材料。这包括对间隔结构和栅极介电层作底切的掺杂区部分，由此限定晶体管的自对准延伸部结构。增大掺杂部分 210 的蚀刻速度允许经蚀刻的源极和漏极延伸部凹腔对间隔结构和栅极介电层形成底切。

[0033] 根据本发明的一种实现，干蚀刻工艺可采用发生在等离子体反应器中的氯化药剂。在一种实现中，蚀刻剂处方可由 NF_3 和 Cl_2 的组合物构成，氩或氦作为缓冲气体或载体气体。活化蚀刻剂物质的流量可在 50-200 标准立方厘米 / 分钟 (SCCM) 之间变动，而载体气体的流量可在 150-400SCCM 之间变动。可在具有小于 100W 的低 RF 偏置的 700W-1100W 范围的功率下采用高能等离子体。反应器压力可在从 1 帕斯卡 (Pa) 左右至 2 帕斯卡左右的范围内变动。

[0034] 在另一实现中，蚀刻药剂可由 HBr 和 Cl_2 的组合构成。蚀刻剂物质的流量可在 40SCCM-100SCCM 之间变动。可在具有小于 100W 的低 RF 偏移的 600W 左右 -1000W 左右范围的功率下采用高能等离子体。反应器压力可从 0.3 帕斯卡左右至 0.8 帕斯卡左右的范围内变动。在另一种实现中，蚀刻剂化学物质可由 SF_6 和 Cl_2 的组合物构成。SF_6 流量可在 3SCCM 和 10SCCM 之间变动并且 Cl_2 流量可在 20SCCM 和 60SCCM 之间变动。可在无 RF 偏置或具有

小于 50W 的 RF 偏置的 400W 左右 -900W 左右范围的功率下采用高能等离子体。在这种实现中，SF_6 流量和反应器压力可保持低以降低去除速率并最大化控制。例如，反应器压力可从 0.1 帕斯卡左右至 0.5 帕斯卡左右的范围内变动。在又一实现中，蚀刻剂化学物质可由 Ar 和 Cl_2 的组合物构成。这里，蚀刻剂物质的流量可在 40SCCM 和 80SCCM 之间变动。可在具有约 100W 和 200W 之间的高 RF 偏置的 400W 左右 -800W 左右范围的功率下采用中等能量等离子体。反应器压力可在从 1 帕斯卡左右至 2 帕斯卡左右的范围内。

[0035] 图 3 是图 2 的器件在蚀刻掉一部分衬底 110 以形成源极 / 漏极和源极 / 漏极延伸部凹腔后的示图。如图所示，形成源极区凹腔 310 和漏极区凹腔 320。此外，已通过蚀刻掺杂部分 210 形成源极延伸物凹腔 330 和漏极延伸物凹腔 340。由于采用增加掺杂部分 210 的蚀刻速率的掺杂剂和蚀刻剂处方，间隔结构 220 的厚度对源极延伸部凹腔 330 和漏极延伸部凹腔 340 的蚀刻具有的影响最小。

[0036] 在干蚀刻工艺完成后，可施加湿蚀刻工艺以清洗并进一步蚀刻源极区凹腔 310、源极延伸部凹腔 330、漏极区凹腔 320 以及漏极延伸部凹腔 340。可采用用于清洗硅和氧化物材料的业内已知传统湿蚀刻化学物质。例如，可采用能沿其晶面去除硅的湿蚀刻化学物质。

[0037] 湿蚀刻为了至少两个目的。首先，湿蚀刻去除例如碳、氟、含氯氟烃和诸如氧化硅的氧化物的杂质以提供可在其上进行后续处理的干净表面。其次，湿蚀沿 <111> 和 <001> 晶面去除很薄部分的衬底以提供在其上可发生高质量外延沉积的光滑表面。蚀刻掉的衬底薄层可高达 5nm 厚并也可去除残留杂质。如图 4 所示，湿蚀刻使源极区凹腔 310、源极延伸物凹腔 330、漏极区凹腔 320 和漏极延伸物凹腔 340 的各边缘遵循 <111> 和 <001> 晶面。还要注意，源极和漏极延伸部 330、340 不具有传统加工中出现的子弹状外形。

[0038] 在蚀刻工艺后，包括源极和漏极延伸部的源极和漏极区凹腔可采用选择性外延沉积工艺以例如硅锗合金的化合物薄膜填充。外延沉积工艺用来在一道工艺中形成源极和漏极区以及源极和漏极延伸部。在一些实现中，硅合金可以是在原处掺杂的硅锗，藉此在原处掺杂的硅锗可用硼和 / 或磷中的一种或多种来掺杂。

[0039] 在实践中，沉积在源极和漏极区凹腔内的硅锗合金材料的晶格间距不同于用来形成衬底 110 的一种或多种材料的晶格间距。晶格间距的差异导致 MOS 晶体管的沟道区内的张应力或压应力，这个问题由于将高锗化合物合金沉积在源极延伸物凹腔 330 和漏极延伸物凹腔 340 中而变得更为突出。

[0040] 根据本发明的一些实现，对于 PMOS 晶体管，源极区凹腔 310 和漏极区凹腔 320 可以渐变的锗硅合金填充，例如根据如下面图 15 中描述的实施例的方法之一得到的渐变高锗含量的硅锗区。渐变锗硅合金可以范围从 10％原子 -50 原子％的渐变锗浓度外延地沉积。在其它实现中，渐变的锗硅合金可进一步在原处以硼掺杂。硼浓度可在从 $2\times10^{19}/cm^3$-$7\times10^{20}/cm^3$ 的范围内变动。在该实施例中，渐变的锗硅合金的厚度可在 40 埃至 1500 埃的范围内变动。

[0041] 图 5 是图 4 器件的示图，其中源极区凹腔 310 已填充有在图 14 中进一步描述的渐变的高锗含量的硅锗叠层 1400 以形成源极区 510，并且漏极区凹腔 320 已填充有同样在图 14 中进一步描述的渐变的高锗含量的硅锗叠层 1400 以形成漏极区 520。延伸部已填充有渐变的高锗含量的硅锗叠层 1400 以形成外延源极延伸部 530 和外延漏极延伸部 540。

[0042] 如图 5 所示，与通过注入和扩散技术形成并在末端 (tip) 区和沟道区之间不具有

明显边界的传统源极和漏极末端区不同，本发明的自对准、外延源极和漏极延伸物具有突变的边界。因此，外延源极 / 漏极延伸部和沟道区之间的界面是清楚和良好界定的。界面的一侧是外延沉积的掺杂硅材料而界面的另一侧是构成沟道区的衬底材料。外延源极 / 漏极延伸部中的掺杂物大致或完全地保留在延伸部内并且不容易扩散入沟道区，由此允许外延源极和漏极延伸部将重掺杂的硅材料带入到相对传统技术非常接近沟道区的位置。如本领域内技术人员理解的那样，这进而允许减小栅极长度而无需缩短沟道区。

[0043] 将外延源极和漏极延伸部形成在相对接近沟道区的位置也给予沟道更大的流体静应力。该应力增加了沟道中的应变，由此提高了沟道中的迁移率并增大驱动电流。该应力通过增大外延源极和漏极延伸部的掺杂而被进一步放大，所述外延源极和漏极延伸部的掺杂在渐变锗硅合金的外延沉积过程中容易得到控制。

[0044] 如本领域内技术人员所知，平面 MOS 器件 100 可能经历进一步 MOS 处理，例如置换栅极氧化物工艺、置换金属栅极工艺、退火或硅化 (salicidation) 工艺，这些工艺可进一步改良器件和 / 或提供必要的电气互连。例如，在源极 / 漏极区和源极 / 漏极延伸部的外延沉积后，层间介电层 (ILD) 可在器件上沉积和平坦化。可使用已知适用于集成电路结构的介电层的材料形成 ILD，例如低 k 介电材料。这些介电材料包括但不局限于，例如二氧化硅 (SiO_2) 的氧化物和掺杂碳的氧化物 (CDO)、氮化硅、例如过氟化环丁烷或聚四氟乙烯的有机聚合物、氟硅酸盐玻璃 (FSG) 以及例如硅倍半氧烷、硅氧烷的有机硅酸盐或有机硅酸盐玻璃。介电层可包括孔或其它空隙以进一步减小其介电常数。图 5 示出已沉积在平面 MOS 器件 100 上的 ILD 层 550。

[0045] 本发明不仅限于包含渐变的高锗含量的硅锗区的平面 MOS 器件的形成。例如，具有三维结构的器件——例如三栅极器件——可从前述工艺中获益。图 6-12 提供表示根据本发明一个实施例的非平面器件内的应变感应源极 / 漏极区的成形的解说图。

[0046] 图 6 是多栅极器件 600 在多栅极本体 620 上沉积多栅极介电层 610 之后的示图。图 6 中的多栅极晶体管是具有三个基本等长度栅极的三栅极晶体管。在另一实施例（未示出）中，多栅极晶体管是具有两个栅极的双栅极场效应晶体管 (FinFET)。多栅极介电层 610 可包括氧化硅或高 K 材料中的至少一种。高 K 材料包括氧化镧、氧化钽、氧化钛、氧化铪、氧化锆、钛酸锆酸铅、钛酸钡锶或氧化铝。多栅极介电层 610 使用本领域内技术人员公知的方法作为顺应层沉积在多栅极本体 620 上，这些方法例如等离子体增强化学气相沉积 (PECVD)、高密度化学气相沉积 (HDCVD)、分子有机化学气相沉积 (MOCVD)、原子层沉积 (ALD) 或溅射。多栅极本体 620 可包括硅、锗或Ⅲ - Ⅴ半导体，例如砷化镓 (GaAs) 和锑化铟 (InSb)。多栅极本体 620 可由外延层、单晶衬底形成，或由绝缘体上硅 (SOI) 层形成。

[0047] 图 7 中的示图描述图 6 中的多栅极器件 600 在将顺应功函数金属层 710 以要求厚度沉积在多栅极介电层 610 上之后的情形。功函数金属是具有已知功函数的金属，该功函数是以电子伏 (eV) 为单位表达的金属的固有特征。在一个实施例中，功函数金属层 710 包括氮化钛、氮化钽或其它过渡性金属氮化物中的至少一个。功函数金属层厚度是多栅极器件的目标阈值电压 (V_t) 的函数。

[0048] 在一个实施例中，功函数金属层是使用方向敏感物理汽相沉积 (PVD) 工艺形成的。使用 PVD 工艺的功函数金属层 710 沉积的特征在于，包含在表面成核并垂直于表面生长的柱状晶粒的微观结构。在另一实施例中，可使用包括分子束外延 (MBE)、化学气相沉积

(CVD)、电镀或蒸镀的分层技术来形成具有柱状晶粒的功函数金属层 710。

[0049] 图 8 示出图 7 的多栅极器件 600 在将包含例如多晶硅的多栅极电极 810 和硬掩模 820 的保护掩模形成在功函数金属层 710 的一部分上后的情形。保护掩模通过本领域内技术人员熟知的一连串沉积、光刻和蚀刻工艺形成。多栅极电极 810 可以是掺杂的或未掺杂的并且硬掩模 820 可包括氮化硅或氧氮化硅。

[0050] 图 9 示出图 8 的多栅极器件 600 在各向异性地蚀刻功函数金属层 710 的露出区之后的情形。功函数金属层 710 的露出区是使用湿蚀刻工艺蚀刻的，所述湿蚀刻工艺利用包含碱和氧化物的湿蚀刻剂。选择性地设计合适的湿蚀刻工艺以蚀刻功函数金属层 710 而不会显著侵蚀多晶硅 810 或硬掩模 820。碱可包括氢氧化铵 (NH_4OH)、氢氧化四甲铵 (TMAH) 或氢氧化钾 (KOH) 中的至少一个。氧化物可包括过氧化氢 (H_2O_2) 或臭氧 (O_3) 中的至少一个。各向异性地蚀刻功函数金属层 710 意味着沿垂直于表面方向的蚀刻速率远高于平行于该表面的方向。由于功函数金属层 710 沿垂直于栅极表面的方向的蚀刻速率远高于功函数金属层 710 沿平行于栅极表面的方向的蚀刻速率，功函数金属层 710 各向异性地被蚀刻。这允许功函数金属层 710 的受保护区基本保持原样同时功函数金属层 710 的露出区被湿蚀刻剂蚀刻掉。

[0051] 图 10 是图 9 的器件在多栅极电极 810 附近形成栅极绝缘间隔结构 1010 后的示图。栅极隔离间隔结构 1010 在后续处理中保护多栅极电极 810、功函数金属层 710 以及多栅极介电层 610。

[0052] 图 11 是图 10 的器件在去除多栅极本体 620 的一部分以提供多栅极沟道区 1110 之后的示图。图 12 是图 11 的器件在外延地形成源极和漏极区 1210 之后的示图。外延形成的源极 / 漏极区 1210 是使用渐变的高锗含量的硅锗膜叠层形成的。外延形成的源极 / 漏极区 1210 可使用根据例如下面在图 15 中描述的实施例中的一个或多个方法制成的如图 14 进一步描述的渐变的高锗含量的硅锗膜叠层 1400 形成。

[0053] 图 13 示出一通信系统 1300，该通信系统 1300 具有用于处理数据的中央处理单元 (CPU)1310，该中央处理单元 1310 由具有根据一个实施例的渐变的高锗含量的硅锗区的晶体管构成。通信系统 1300 可包括具有 CPU 1310 的母板 1320 以及耦合于总线 1340 的联网接口 1330。更具体地，CPU 1310 可包括渐变的高锗含量的硅锗区和 / 或其制造方法。根据场合，通信系统 1300 可另行包括其它组件，包括但不局限于易失和非易失存储器、图形处理器、数字信号处理器、密码处理器、芯片集、海量存储器 (例如硬盘、压缩盘 (CD)、数字多功能盘 (DVD) 等) 及其它。这些组件中的一个或多个还可包括之前描述的渐变的高锗含量的硅锗区和 / 或其制造方法。在各实施例中，通信系统 1300 可以是个人数字助理 (PDA)、移动设备、平板计算设备、膝上计算设备、桌面计算设备、机顶盒、娱乐控制单元、数字相机、数字录像机、CD 播放机、DVD 播放机或其它类似的数字设备。

[0054] 图 15 是描述用来形成具有图 14 所示晶体结构的渐变的高锗含量的硅锗叠层 1400 的应变半导体器件的制造工艺的一个实施例的流程图。在一个实施例中，渐变的高锗含量硅锗叠层 1400 包括使用在 10-40 标准升 / 分钟 (slm) 之间变动的流量的例如氢气 (H2) 的载体气体在 10-150 托 (T) 之间变动的压力下通过外延沉积工艺使用例如 Applied Materials Centura® 或 ASM Epsilon® 工具的沉积工具在衬底 110 上生长的叠层。

[0055] 在步骤 1500，优选将底层选择性地形成在衬底 110 的露出区上。在一个实施例中，

底层是具有在 20-25 原子重量%之间变动的相对低的锗含量并沉积长达 10-30 秒的时间以提供在100Å-300Å之间变动的最终厚度范围的硅锗籽晶层 1410。硅锗籽晶层 1410 可选择地掺杂硼至 5.0×10^{19} 原子 /cm^3-1.5×10^{20} 原子 /cm^3 范围的浓度。硅锗籽晶层 1410 可在 700-800 摄氏度（℃）或更佳地在 745-765℃之间的温度范围内沉积。此外，硅锗籽晶层 1410 可使用包含氯化氢 (HCl)、二氯硅烷 (DCS)、锗烷 (GeH_4) 以及乙硼烷 (B_2H_6) 的工艺气体混合物形成，其中 HCl 流量在 20-200 标准立方厘米 / 分钟 (sccm)，DCS 流量在 10-100sccm 之间，使用 1%锗烷和氢平衡的锗烷流量在 20-200sccm 之间，而乙硼烷流量在 10-75sccm 之间。

[0056] 在步骤 1510，将过渡层 1420 选择性地形成在硅锗籽晶层 1410 上以在例如硅锗籽晶层 1410 的基底晶核层至高锗含量层 1430 之间提供非常缓和的过渡。在一个实施例中，过渡层 1420 毗邻和 / 或靠近硅锗籽晶层 1410 的下部可在硅锗籽晶层 1410/ 过渡层 1420 界面处具有大致等于硅锗籽晶层 1410 的锗含量，即 20-25 原子重量%。此外，过渡层 1420 毗邻和 / 或靠近高锗含量层 1430 的上部可在过渡层 1420/ 高锗含量层 1430 界面处具有大致等于高锗含量层 1430 的锗含量，即大致在 40-55 原子重量%之间。过渡层 420 的厚度可在150Å和450Å之间变动。

[0057] 过渡层 1420 可通过将处理温度从起始温度开始递减的动态方式的外延生长工艺形成，该起始温度基本等于硅锗籽晶层 1410 的成形温度，在 700-800℃之间变动或更佳地在 745-765℃之间变动。成形温度以基本线性方式从起始温度递减至终止温度。终止温度或第二温度在一个实施例中比起始温度或第一温度低大致 25-100℃之间，或更佳地比起始温度或第一温度低大约 45-55℃。在一个实施例中，过渡层 1420 沉积长达 20-60 秒之间变动的时间段。

[0058] 通过在过渡层 1420 成形期间将 DCS、HCl 和 GeH_4 的气体混合物流量从较高流量递减至降低流量而使过渡层 1420 进一步外延地形成。如果掺杂过渡层 1420，则在形成过渡层 1420 的同时增大乙硼烷流量以提供基本等于或大于过渡层 1420/ 高锗含量层 1430 界面处或附近的 2.0×10^{20} 原子 /cm^3 的硼浓度。在该实施例中，过渡层 1420 的成形提供以等于或小于 2%膜松弛和健康膜形态的将近300Å / 分钟的生长速率选择性形成的渐变硅锗膜。

[0059] 在步骤 1520 将高锗含量层 1430 选择性地形成在过渡层 1420 上以提供应变的晶体管结构。在一个实施例中，形成高锗含量层 1430，同时在过渡层 1420 最终部分成形后仍然保持工艺处方参数恒定。该实施例中，高锗含量层 1430 以300Å-600Å之间的厚度形成而锗含量在 40-55 原子重量%之间变动。高锗含量层 1430 可选择性地掺杂硼至 2.0×10^{20} 原子 /cm^3-3.0×1020 原子 /cm^3 之间的浓度。

[0060] 为了解说和阐述，已给出前面对本发明实施例的说明。它不旨在为穷举的或将本发明限定在所披露的精确形式。说明书和后面的权利要求书包括术语，例如左、右、顶、底、上方、下方、上、下、第一、第二等，它们仅为描述目的且不解释为限定。例如，指示相对垂直位置的术语指衬底或集成电路的器件侧（或有效表面）处于该衬底“顶”面的情形；衬底实际上可处于任何方位以在基准的标准地面坐标系中使衬底“顶”侧低于“底”侧并且仍然落在术语“顶”的涵义中。本文中（包括权利要求书中）使用的术语“在……上”不表示在第二层“上”的第一层直接在第二层上或与第二层直接接触，除非这是专门说明的；在第一层和第一层上的第二层之间可以有第三层或其它结构。本文描述的器件或物品的实施例可在

多个位置和方位上制造、使用或运输。

[0061] 本领域内技术人员能理解，许多修正和变化鉴于前面的教义是可能的。本领域内技术人员能发现附图所示各组件的许多等效组合和替代。因此本发明的范围不受该详细说明限制，而是受所附权利要求书限制。

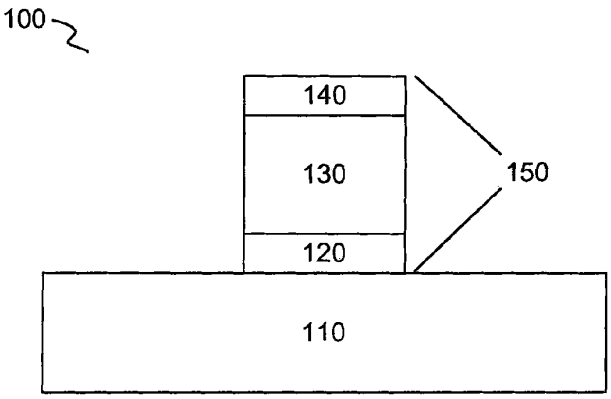

100
140
130
120
150
110

图 1

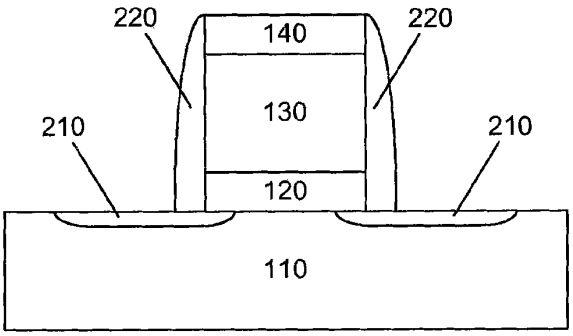

220
140
220
130
210
210
120
110

图 2

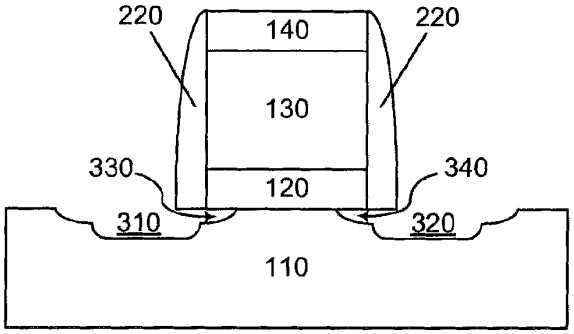

220
140
220
130
330
340
120
310
320
110

图 3

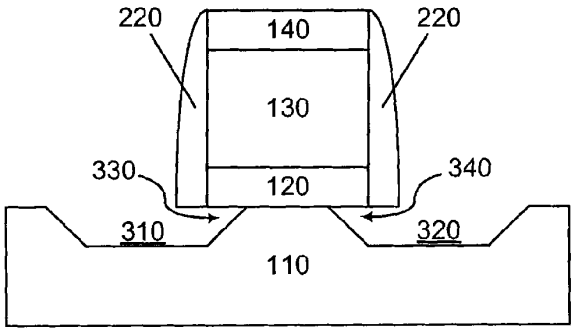

220
140
220
130
330
120
340
310
320
110

图 4

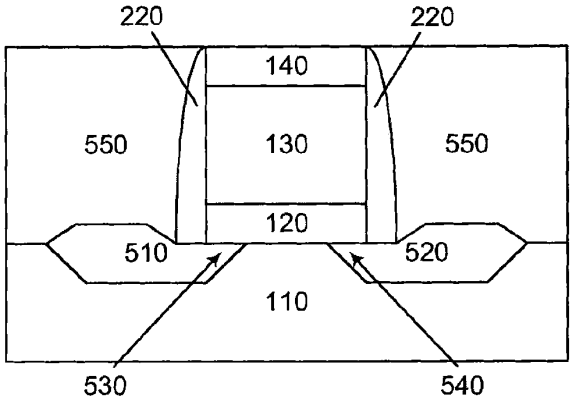

220
220
140
550
130
550
120
510
520
110
530
540

图 5

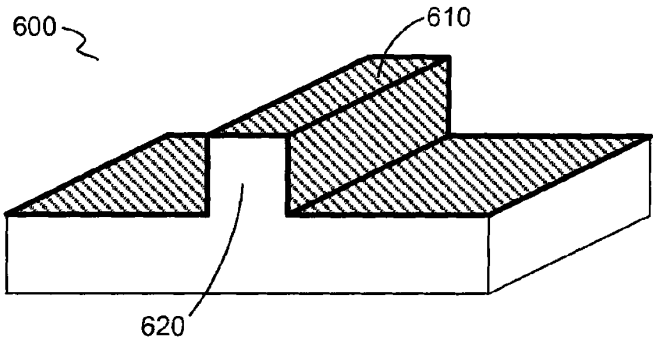

600
610
620

图 6

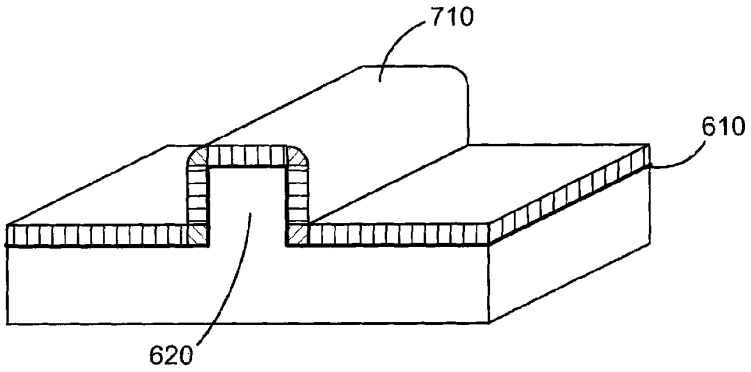


图 7

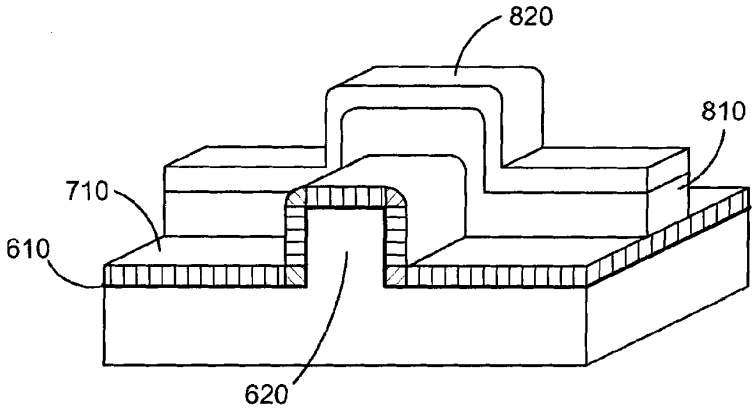


图 8

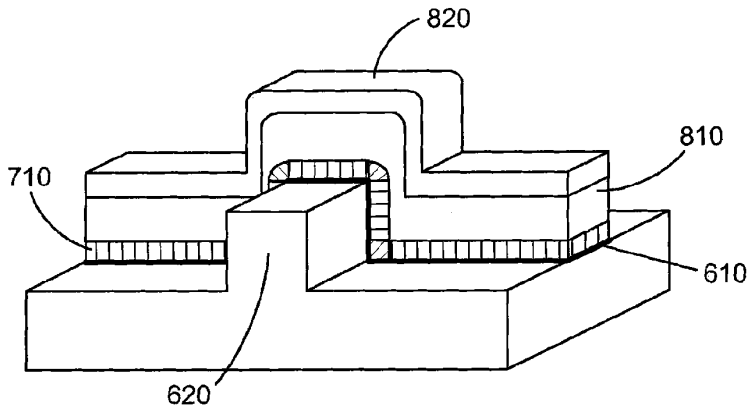


图 9

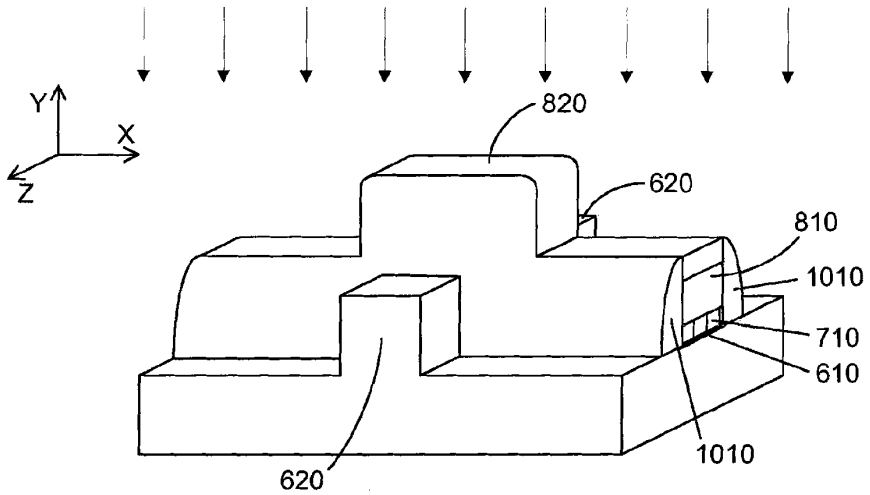


图 10

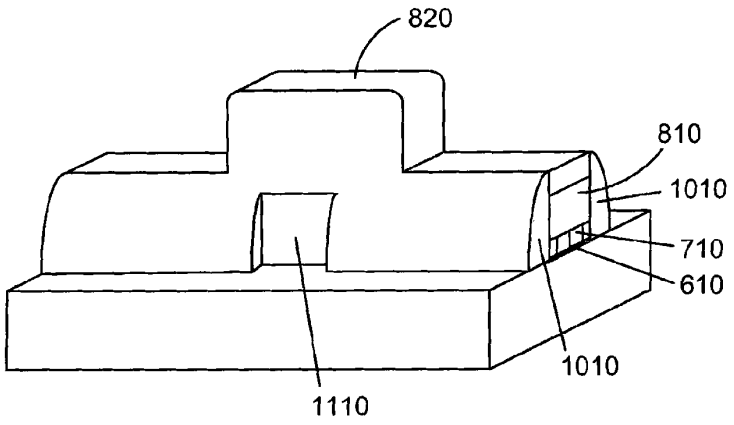

820
810
1010
710
610
1010
1110

图 11

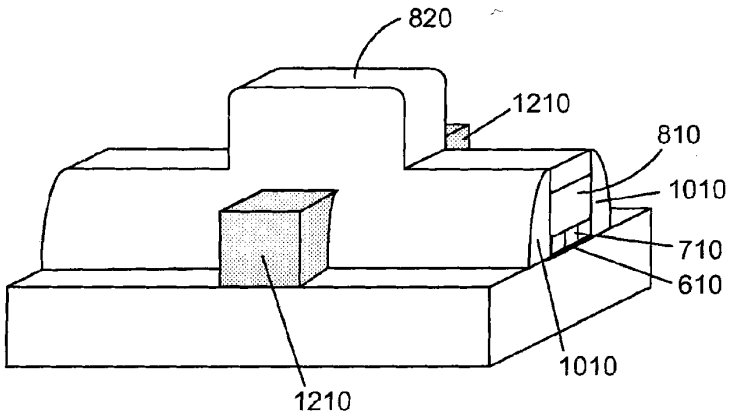

820
1210
810
1010
710
610
1010
1210

图 12

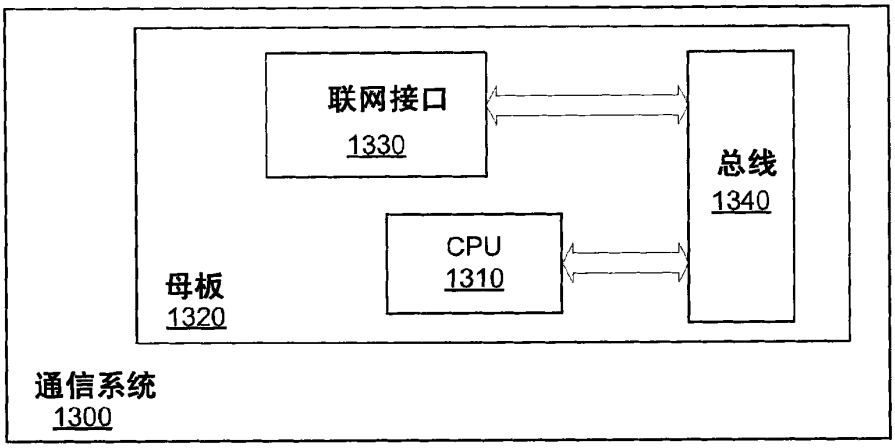

联网接口
1330
总线
1340
CPU
1310
母板
1320
通信系统
1300

图 13

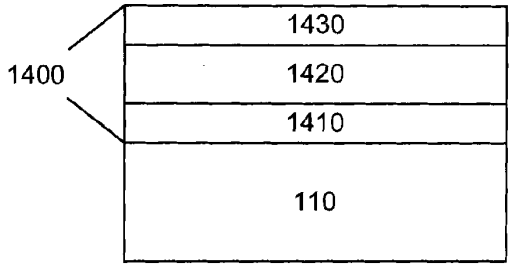

1400
1430
1420
1410
110

图 14

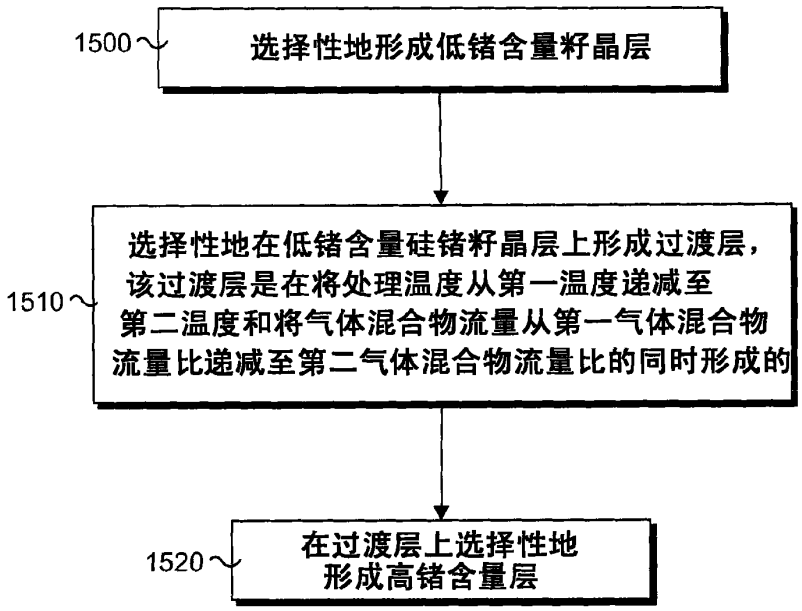

1500
选择性地形成低锗含量籽晶层
选择性地在低锗含量硅锗籽晶层上形成过渡层，该过渡层是在将处理温度从第一温度递减至第二温度和将气体混合物流量从第一气体混合物流量比递减至第二气体混合物流量比的同时形成的
1510
在过渡层上选择性地形成高锗含量层
1520

图 15

Espacenet

Bibliographic data: JP2006013428 (A) — 2006-01-12

MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

Inventor(s): KIM YOUNG SUK; MORI TOSHIFUMI ± (KIM YOUNG SUK, ; MORI TOSHIFUMI)

Applicant(s): FUJITSU LTD ± (FUJITSU LTD)

Classification: - international: ***H01L21/336; H01L21/8238; H01L27/092; H01L29/78; H01L29/786***

- cooperative: **H01L21/823807 (EP, US)**; **H01L21/823814 (EP, US)**; **H01L29/1083 (EP, US)**; **H01L29/6653 (EP, US)**; **H01L29/66628 (EP, US)**; **H01L29/66636 (EP, US)**; **H01L29/7842 (EP, US)**; **H01L29/7848 (EP, US)**; H01L29/165 (EP, US); H01L29/665 (EP, US); H01L29/6656 (EP, US)

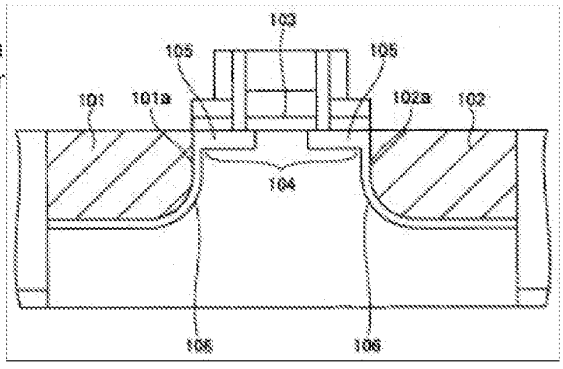
Application number: JP20050046573 20050223 Global Dossier

Priority number(s): JP20040156569 20040526 ; JP20050046573 20050223

Also published as: JP4375619 (B2) US2005266631 (A1) US7407860 (B2)

Abstract of JP2006013428 (A)

PROBLEM TO BE SOLVED: To provide a manufacturing method of a semiconductor device in which p-type and n-type transistors are balanced in operating speed by improving the operating speed of the p-type transistor. ;SOLUTION: A compressive stress applied portion 20 consisting of SiGe film is formed in a source/drain region of a p-MOS region 30a, after that, an impurity is implanted into the p-MOS region 30a and an n-MOS region 30b, and shallow junction regions 22a, 22b and deep junction regions 23a, 23b are formed. A comprehensive working speed of a complementary type semiconductor



device 10 is improved by a balance with respect to an n-MOS transistor 13b in such a way that the impurity of the shallow junction regions 22a, 22b is prevented from diffusing into just beneath a gate insulating film 15 which is caused by a heating when forming the SiGe film, that short channel effect is prevented, and that a hole mobility of channel region of a p-MOS transistor 13a is improved. ;COPYRIGHT: (C) 2006,JPO&NCIPI

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION JP2006013428A

Manufacturing method of semiconductor devices

[0001]

The present invention relates to a method for manufacturing a complementary MIS (Metal Insulator Semiconductor) type semiconductor device in which compression strain is induced in the channel of a p-type transistor.

[0002]

Semiconductor devices have been miniaturized to the minimum processing dimensions in order to achieve high performance such as high-speed operation, low power consumption, and high integration. In the generation with the minimum processing size of 65 nm or less, the technical difficulty of miniaturization becomes extremely high, and the limit of high performance by miniaturization alone is beginning to appear.

[0003]

Therefore, as a high-performance transistor that does not depend on miniaturization, a so-called strained silicon transistor in which distortion is induced in a silicon single crystal in the channel region of a MIS type or MOS type transistor is attracting attention.

A strained silicon transistor forms a Si single crystal film on a SiGe film having a larger lattice constant than a Si single crystal, and induces tensile strain in the Si single crystal film that inherits the lattice constant of the SiGe film to induce a Si single crystal. The electron mobility of the film can be improved. An n-type transistor has been proposed in which such a strained Si single crystal film is used as a channel to improve the operating speed.

[0004]

On the other hand, since the hole mobility (1900 cm2 / (V · s)) in a normal Si single crystal is smaller than the electron mobility (3900 cm2 / (V · s)), a p-type transistor and an n-type transistor are provided. In the complementary semiconductor device, the operating speed of the p-type transistor is slow, so that the overall operating speed of the semiconductor device is slow.

Furthermore, even if the strained silicon substrate is used to increase the speed of operation of the n-type transistor, the operating speed of the entire semiconductor device cannot be improved, which causes problems such as high cost of the strained silicon substrate.

[0005]

Therefore, in order to increase the operating speed of the p-type transistor, as shown in FIG. 1, SiGe films 101 and 102 are formed in the source / drain region of the p-type transistor, and the SiGe films 101 and 102 under the gate oxide film 103. A

semiconductor device has been proposed in which compressive stress is applied to a channel portion (Si single crystal) 104 on the side to improve hole mobility (see Patent Document 1).

米国特許第６６２１１３１号明細書

[0006]

In Patent Document 1, after forming an impurity diffusion region consisting of a shallow junction region 105 and a deep junction region 106 of a p-type transistor, grooves 101a and 102a are formed in the source / drain region, and thermal CVD is formed on the surfaces of the grooves 101a and 102a. SiGe films 101 and 102 are formed by the method.

[0007]

However, after forming the impurity diffusion region, when the SiGe films 101 and 102 are formed, the impurities are diffused by heating to about 740 ° C., and a short channel effect is generated. There is a problem that the roll-off characteristic of is deteriorated.

[0008]

Further, Patent Document 1 does not disclose a specific method for manufacturing a complementary semiconductor device including a p-type transistor and an n-type transistor.

[0009]

An object of the present invention is to provide a method for manufacturing a novel semiconductor device in which the operating speed of a p-type transistor is increased and the operating speed is balanced with that of an n-type transistor.

[0010]

According to one aspect of the present invention, there is a method for manufacturing a semiconductor device including a p-type transistor formed in the first region of the semiconductor substrate and an n-type transistor formed in the second region of the semiconductor substrate. A step of forming a gate laminated body composed of a gate insulating film and a gate electrode on the semiconductor substrate, and in the first region, a first side wall insulating film and a second side wall insulating film are provided on both side surfaces of the gate laminated body. The step of forming the film and the state in which the surface of the semiconductor substrate in the second region is covered with the etching-resistant film, the first side wall insulating film and the second side wall insulating film are used as masks in the first region. A step of forming a groove on the semiconductor substrate outside the second side wall insulating film, a step of forming a compressive stress application portion in the groove, and a first side wall insulating film and a second side wall insulating in the first region. A step of removing the film and an etching-resistant film in the second region, and a step of forming a first bonding region in the first region and the second region using the gate laminate as a mask. A third side wall insulating film is formed on both side surfaces of the gate laminate, and a second junction region is formed in the first region and the second region by using the gate laminate and the third side wall insulating film as a mask. A method for manufacturing a semiconductor device including the process of performing the process is provided.

[0011]

According to another aspect of the present invention, since the impurities are injected to form the first joint region and the second joint region after the compressive stress application portion is formed, the compressive stress application portion is formed. It is possible to prevent impurities, particularly impurities in the first bonding region, from diffusing directly under the gate insulating film due to the heating at the time.

Therefore, by preventing the short-channel effect, increasing the hole mobility in the channel region of the p-type transistor, and increasing the operating speed of the p-type transistor, the complementary semiconductor is balanced with the operating speed of the n-type transistor. The overall operating speed of the device can be increased.

In addition, the drain current of the p-type transistor can be increased, and the characteristics of the p-type transistor can be matched with those of the n-type transistor in terms of drain current.

[0012]

According to another aspect of the present invention, there is a method for manufacturing a semiconductor device including a p-type transistor formed in the first region of the semiconductor substrate and an n-type transistor formed in the second region of the semiconductor substrate. A step of forming a gate laminated body composed of a gate insulating film and a gate electrode on a semiconductor substrate, and forming a first side wall insulating film and a second side wall insulating film on both side surfaces of the gate laminated body, and the same. A step of exposing the surface of the semiconductor substrate outside the second side wall insulating film, a step of forming a resist film covering the second region, and a step of ionizing and irradiating CF4 gas and O2 gas with the first region. The semiconductor substrate is exposed to the outside of the second side wall insulating film while removing the resist film in the second region by ionizing and irradiating the O2 gas in the first surface treatment step of modifying the surface of the semiconductor substrate. A second surface treatment step of forming an oxide film on the surface, a step of exposing the surface of the semiconductor substrate in the first region, and a first side wall insulating film and a second side wall insulating film in the first region. In the first region, a step of forming a groove on the semiconductor substrate outside the second side wall insulating film and a step of forming a compressive stress application portion in the groove using the oxide film of the second region as a mask. A step of removing the first side wall insulating film and the second side wall insulating film and removing the etching resistant film in the second region, and the first region and the second region using the gate laminate as a mask. The first region and the third side wall insulating film are formed on both side surfaces of the gate laminated body, and the gate laminated body and the third side wall insulating film are used as masks. Provided is a method for manufacturing a semiconductor device, which comprises a step of forming a second junction region in the second region.

[0013]

According to another aspect of the present invention, the same effect as that of the above-mentioned invention is obtained, an oxide film is formed on the surface of the semiconductor substrate in the second region by the first surface treatment and the second surface treatment, and the oxide film is formed. On the surface of the first region, an ashing modified film having a lower acidity resistance than the oxide film is formed.

That is, different films having etching selectivity with respect to the hydrofluoric acid aqueous solution are formed on the surfaces of the semiconductor substrates in the first region and the second region.

Therefore, with the surface of the semiconductor substrate in the second region masked by the oxide film, the surface of the semiconductor substrate can be exposed only in the first region by the hydrofluoric acid treatment, and the groove portion in which the compressive stress application portion is formed can be easily formed. ..

[0014]

According to the present invention, it is possible to realize a semiconductor device in which the operating speed of a p-type transistor is increased and the operating speed is balanced with that of an n-type transistor.

[0015]

(First Embodiment) A method for manufacturing a semiconductor device according to the first embodiment of the present invention will be described with reference to FIGS. 2 to 17.

FIG. 2 is a cross-sectional view of a semiconductor device formed by the method for manufacturing a semiconductor device according to the first embodiment of the present invention.

3 to 17 are diagrams showing a manufacturing process of the semiconductor device according to the first embodiment.

[0016]

With reference to FIG. 2, the semiconductor device 10 is composed of a p-MOS transistor 13a and an n-MOS transistor 13b separated by an element separation region 12 formed on the silicon substrate 11.

The p-MOS transistor 13a is compressed from the surface of the silicon substrate 11 in contact with the third side wall insulating film 19 provided on both side surfaces of the gate laminate 18 composed of the gate insulating film 15 and the gate electrode 16, for example, SiGe. The stress applying portion 20 is formed, and the compressive stress applying portion 20 is formed so as

to sandwich the compression strain inducing portion 21 made of Si under the gate laminate 18 and the third side wall insulating film 19 from both sides thereof. ..

Since the SiGe film of the compressive stress application unit 20 has a larger lattice constant than Si, stress is applied in the direction in which the compressive stress application unit 20 sandwiches the channel region, and compressive strain is induced in the channel region.

As a result, the hole mobility in the channel region is improved, and high-speed operation of the p-MOS transistor 13a becomes possible.

[0017]

In the embodiment, the region where the p-MOS transistor 13a is formed is referred to as a p-MOS region 30a, and the region where the n-MOS transistor 13b is formed is referred to as an n-MOS region 30b.

Hereinafter, the manufacturing method of the semiconductor device 10 will be described in detail.

[0018]

3 to 17 are diagrams showing a manufacturing process of the semiconductor device according to the first embodiment.

[0019]

First, in the step of FIG. 3, the element separation region 12 is formed on the silicon substrate 11 by the STI (Shallow Trench Isolation) method.

Specifically, the trench 31-1 is formed by trench etching of the silicon substrate 11, the inner wall of the trench 31-1 is thermally oxidized, the silicon oxide film is filled by the CVD method, and then flattened by the CMP method. The element separation region 12 is formed.

[0020]

The silicon substrate 11 may be a bulk substrate or an SOI (Silicon On Insulator) substrate.

By using the SOI substrate, it is possible to reduce the parasitic capacitance due to the depletion layer generated between the source / drain region formed in the later step and the substrate, and improve the operating speed of the transistor.

Moreover, a known method is used as the STI method.

[0021]

In the step of FIG. 3, further, n-type impurity ions such as As + and P + are implanted in the p-MOS region 30a of the silicon substrate 11 by the ion implantation method, and p-type impurity ions such as B + and BF2 + are implanted in the n-MOS region 30b. Implantation forms an n-type well region 32a and a p-type well region 32b, respectively.

[0022]

Next, in the step of FIG. 4, the silicon natural oxide film (not shown) on the surface of the silicon substrate 11 is removed by HF (fluoric acid) treatment, and the thickness is increased by, for example, a CVD method, a sputtering method, or a thermal oxidation treatment. A 1.2 nm silicon oxide film 15-1 (which later becomes a gate insulating film) is formed.

Specifically, the thermal oxidation treatment is carried out, for example, in an oxygen atmosphere at a temperature of 600 ° C. to 1100 ° C. for 1 minute to 20 minutes to form a silicon oxide film 15-1 having a thickness of 0.5 nm to 3 nm.

[0023]

Instead of the silicon oxide film 15-1, a silicon oxynitride film or a silicon nitride film may be used, or a laminate of these films and a silicon oxide film may be used, and a known insulating film can be used.

[0024]

In the step of FIG. 4, a non-doped polysilicon film 16-1 having a thickness of 100 nm (which later becomes a gate electrode) is further formed on the silicon oxide film 15-1 by a CVD method.

Specifically, for example, by a reduced pressure CVD method, the pressure inside the chamber is heated in the range of 10 Pa to 50 Pa and the substrate temperature is in the range of 600 ° C. to 650 ° C. A polysilicon film 16-1 having a temperature of 20 nm to 200 nm is formed.

A PH3 gas or the like may be mixed to form a P + or B + doped doped polysilicon film.

[0025]

In the step of FIG. 4, a silicon nitride film 33-1 having a thickness of 10 nm to 50 nm (which later becomes a cap layer) is further formed on the polysilicon film 16-1 by a CVD method.

Specifically, for example, the substrate temperature is set to 650 ° C. and the pressure is 20 Pa, and the mixture is formed using dichloromethane gas (flow rate 660 sccm) and ammonia gas (flow rate 870 sccm).

[0026]

Next, in the step of FIG. 5, a resist film (not shown) is formed on the silicon nitride film 33-1 and patterning is performed by a photolithography method to leave a resist film in a region to be a gate laminate.

Next, by the RIE (Reactive Ion Etching) method, the silicon nitride film 33-1, the polysilicon film 16-1 and the silicon oxide film 15-1 are etched using the patterned resist film as a mask, and the cap layer 33 and the gate are etched, respectively. The electrode 16 and the gate insulating film 15 are formed.

The gate length is set in the range of, for example, 10 nm to 90 nm.

[0027]

Next, in the step of FIG. 6, a silicon oxide film 34-1 having a thickness of 10 nm is formed by a CVD method so as to cover the structure of FIG.

Specifically, the substrate temperature is set in the range of 550 ° C. to 700 ° C. using TEOS (tetraethoxysilane) by the thermal CVD method to form a silicon oxide film 34-1 having a thickness of 5 nm to 30 nm.

[0028]

In the step of FIG. 6, a silicon nitride film 35-1 having a thickness of 40 nm is further formed by a CVD method so as to cover the silicon oxide film 34-1.

Specifically, using dichlorosilane gas (flow rate 660 sccm) and ammonia gas (flow rate 870 sccm) by the reduced pressure CVD method, the pressure is set to 20 Pa and the substrate temperature is set to 600 ° C. to 800 ° C., and silicon nitriding having a thickness of 10 nm to 100 nm. It forms a film 35-1.

[0029]

Next, in the step of FIG. 7, the resist film 36 is formed so as to cover the structure of FIG. 6, and the opening 36-1 is formed in the p-MOS region 30a of the resist film 36 by a photolithography method.

[0030]

In the step of FIG. 7, the silicon nitride film 35-1 and the silicon oxide film 34-1 are further anisotropically etched by the RIE method until the surface of the silicon substrate 11 is exposed, and silicon oxidation covering both side surfaces of the gate laminate is performed. A first side wall insulating film 34 made of a film and a second side wall insulating film 35 made of a silicon nitride film are formed on the outside thereof.

Specifically, as the etching gas of the RIE method, for example, hydrofluorocarbon such as difluoromethane (CH2F2) and 1,1-difluoroethane (C2H4F2) is used, and the thickness of the first side wall insulating film 34 is 5 nm to 30 nm. The thickness of the second side wall insulating film 35 is set in the range of 10 nm to 60 nm.

[0031]

Next, in the step of FIG. 8, the surface of the structure of FIG. 7 is covered with a resist film 36 covering the n-MOS region 30b, a cap layer 33 of the p-MOS region 30a, a first side wall insulating film 34, and a second side wall. Using the insulating film 35 as a mask, the surface of the exposed silicon substrate 11 (the region between the second side wall insulating film 35 and the element separation region 12) is anisotropically etched by the RIE method. Form 11-1.

Specifically, for example, hydrogen bromide (HBr) or the like is used as the etching gas of the RIE method, and the depth of the groove portion 11-1 is set to 10 nm to 150 nm.

[0032]

In the step of FIG. 8, the resist film may be removed from the n-MOS region 30b before the anisotropic etching is performed, and the silicon nitride film 35-1 may be used as a mask.

In this case, the thickness of the silicon nitride film 35-1 is preferably set in the range of 10 nm to 100 nm.

[0033]

Next, in the step of FIG. 9, the resist film in the n-MOS region 30b is removed, then the natural oxide film on the surface of the groove 11-1 is removed with an aqueous fluoride solution, and then the silicon nitride film 35 in the n-MOS region 30b is removed. Using the cap layer 33, the first side wall insulating film 34, and the second side wall insulating film 35 of the p-MOS region 30a as masks, the groove portion 11-1 of the structure of FIG. 8 is formed with -1 and the silicon oxide film 34-1. Grind by chemical dry etching method.

[0034]

By using the chemical dry etching method, the groove portion 11-1 is isotropically etched, and the silicon substrate 11 is ground into the inside of both ends of the second side wall insulating film 35.

Specifically, in the chemical dry etching method, hydrogen chloride (HCl) gas or chlorine (Cl2) gas is used to set the pressure in the range of 0.1 Pa to 10000 Pa and the substrate temperature in the range of 600 ° C. to 900 ° C.

The etching amount is set so that the distance X from the end of the gate insulating film to the end of the groove is in the range of 5 nm to 80 nm.

[0035]

Further, in the chemical dry etching method, hydrogen chloride gas or the like causes a chemical reaction with Si to grind the groove surface, so that the impact given to the groove surface can be suppressed as compared with the case of using plasma such as the RIE method. In addition, it is excellent in isotropic grinding.

[0036]

Wet etching may be used instead of the chemical dry etching method.

Since the compression stress application portion 20 is formed in the chamber in the next step, the chemical dry etching method is preferable in terms of handling.

[0037]

Next, in the step of FIG. 10, a SiGe film to be the compressive stress application portion 20 is crystal-grown on the surface of the groove portion 11-2 of the structure of FIG. 9 by the CVD method.

The SiGe film is epitaxially grown on, for example, the (001) plane of Si with the (001) plane as the height direction.

[0038]

Since the SiGe film has a larger lattice constant than Si, the compression strain inducing portion 21 (channel is formed) in which the SiGe film is made of Si.

), A compressive stress is applied so as to sandwich the force from both sides to form a compressive strain in the compressive strain-inducing portion 21.

[0039]

Specifically, the SiGe film is prepared by a reduced pressure thermal CVD method as a raw material gas, SiH2Cl2 (flow rate: 50 to 300 sccm), GeH4 (flow rate: 50 to 300 sccm), SiCH6 (flow rate: 2 to 50 sccm), HCl (flow rate: 2 to 50 sccm). Using each gas of 30 to 300 sccm) and H2 (flow rate: 100 sccm to 100 slm), set the pressure to 100 to 5000 Pa and the substrate temperature to 500 ° C. to 800 ° C., and set the SiGe film to a height corresponding to the surface of the silicon substrate 11. To grow.

By such a step, the SiGe film can be selectively grown only on the surface of the groove where Si is exposed.

[0040]

Since the surface of the gate electrode is covered with the cap layer 33, it is possible to prevent the formation of a SiGe film on the surface of the gate electrode.

[0041]

The composition of the SiGe film is preferably set to a Ge concentration in the range of 1 atomic% to 40 atomic%, and is preferably set to 5 atomic% to 40 atomic%, in terms of epitaxial growth with Si on the groove surface. More preferred.

[0042]

As the Si source gas, SiH4, Si2H6, Si3H8, or Si3Cl6 gas may be used instead of SiH2Cl2 gas, and two or more of these gases may be used.

As the Ge source gas, GeH2Cl2 gas may be used instead of GeH4 gas, or these gases may be mixed and used.

Cl2 gas may be used instead of HCl gas, or may be mixed and used.

Further, it is not necessary to use HCl gas and Cl2 gas.

By adding HCl gas or Cl2 gas, SiGe particles adhering to the surface other than the groove 11-2 can be removed.

[0043]

Further, a so-called raised structure (Elevated S / D) may be formed in which the height of the compressive stress applying portion 20 is grown higher than the surface of the silicon substrate 11.

Further, the compressive stress application portion 20 may be composed of a SiGeC film, and the C (carbon) concentration is preferably set to be larger than 0 atomic% and 2 atomic% or less.

By using the SiGeC film, the thermal stability can be improved as compared with the SiGe film.

When the C concentration exceeds 2 atomic%, the crystallinity of the SiGeC film decreases.

[0044]

Next, in the step of FIG. 11, a resist film (not shown) is formed so as to cover the structure of FIG. 10, an opening is formed in the n-MOS region 30b of the resist film by a photolithography method, and the RIE method is performed. The silicon nitride film 35-1 and the silicon oxide film 34-1 are anisotropically etched until the surface of the silicon substrate 11 is exposed, and the first side wall insulating film made of the silicon oxide film covering both side surfaces of the gate laminate 18 is insulated. A second side wall insulating film 35 made of a film 34 and a silicon nitride film is formed on the outer side of the film 34.

Specifically, the RIE method is performed in the same manner as in the step of FIG.

Then, the resist film is removed.

[0045]

Next, in the step of FIG. 12, the cap layer 33, the second side wall insulating film 35, and the first side wall insulating film 34 of the structure of FIG. 11 are removed by a wet etching method, and a gate laminate is formed on the surface of the silicon substrate 11. Leave.

Specifically, the cap layer 33 made of a silicon nitride film and the second side wall insulating film 35 are removed using, for example, an aqueous phosphoric acid solution, and the first side wall insulating film 34 made of a silicon oxide film is removed using, for example, an aqueous hydrofluoric acid solution.

[0046]

Next, in the step of FIG. 13, a resist film (not shown) is formed so as to cover the structure of FIG. 12, and the n-MOS region 30b of the resist film is opened by a photolithography method.

Next, by the ion implantation method, the gate laminate is used as a mask in the n-MOS region 30b, and the p-type impurities are obliquely injected into the silicon substrates 11 on both sides of the gate laminate 18 with respect to the silicon substrate 11 to form the pocket region 23b. To form.

Specifically, for example, In is used as the p-type impurity, the acceleration energy is 50 keV, and the dose amount is 5 × 1013 cm-2.

[0047]

Further, in the step of FIG. 13, the shallow junction region 22b is formed by implanting n-type impurities into the silicon substrates 11 on both sides of the gate laminate 18 by using the gate laminate as a mask in the n-MOS region 30b by the ion implantation method. ..

Specifically, for example, As + is used as the n-type impurity, the acceleration energy is 5 keV, and the dose amount is 1 × 1015 cm-2.

The pocket region 23b may or may not be formed.

[0048]

Next, in the step of FIG. 14, the resist film 38 of the structure of FIG. 13 is removed, and the resist film 39 in which the p-MOS region 30a opens is formed in the same manner as in the step of FIG.

Next, by the ion implantation method, the gate laminate 18 is used as a mask in the p-MOS region 30a, and n-type impurities are obliquely implanted into the silicon substrates 11 on both sides of the gate laminate 18 to form the pocket region 23a.

Specifically, for example, Sb + is used as the n-type impurity, the acceleration energy is 60 keV, and the dose amount is 5 × 1013 cm-2.

[0049]

Further, in the step of FIG. 14, the gate laminate 18 is used as a mask in the p-MOS region 30a by the ion implantation method, and p-type impurities are implanted into the silicon substrates 11 on both sides of the gate laminate 18 to form a shallow junction region 22a. ..

Specifically, for example, B + is used as the p-type impurity, the acceleration energy is 5 keV, and the dose amount is 1 × 1015 cm-2.

[0050]

Next, in the step of FIG. 15, the resist film 39 of FIG. 14 is removed, and a silicon oxide film (not shown) having a thickness of 80 nm is formed on the surface of the structure by a CVD method.

Specifically, for example, by the thermal CVD method, BTBAS (Bis (Tertiary-butylamino) Silane, C8H22N2Si) gas and O2 gas are used as raw material gases, the pressure is 0.1 Pa to 1000 Pa, and the substrate temperature is 500 ° C to 580 ° C. To form a silicon oxide film.

[0051]

In the step of FIG. 15, the silicon oxide film is further etched (etched back) by the RIE method until the surface of the silicon substrate 11 is exposed, and both side surfaces of the gate laminate 18 of the p-MOS region 30a and the n-MOS region 30b. A third side wall insulating film 19 is formed.

Specifically, as the etching gas of the RIE method, for example, hydrofluorocarbons such as difluoromethane (CH2F2) and 1,1-difluoroethane (C2H4F2) are used.

[0052]

Next, in the step of FIG. 16, a resist film (not shown) is formed so as to cover the structure of FIG. 15, an opening is formed in the p-MOS region 30a of the resist film by a photolithography method, and ion implantation is performed. By the method, the gate laminate 18 and the third side wall insulating film 19 are used as masks in the p-MOS region 30a, and p-type impurities are implanted into the silicon substrates 11 on both sides of the third side wall insulating film 19 to compress the SiGe film. A deep joint region 24a is formed to a position deeper than the bottom of the stress application portion 20, and is designated as a source / drain region 28a.

Specifically, for example, B + is used as the p-type impurity, the acceleration energy is 8 keV, and the dose amount is 5 × 1015 cm-2.

Then, the resist film is removed.

[0053]

In the step of FIG. 16, a resist film 41 is further formed in substantially the same manner as the p-MOS region 30a, an opening 41-1 is formed in the n-MOS region 30b of the resist film by a photolithography method, and ion implantation is performed. By the method, using the gate laminate 18 and the third side wall insulating film as a mask, n-type impurities are implanted into the silicon substrates 11 on both sides of the third side wall insulating film 19 to form a deep bonding region 24b, and a source / drain region 28b is formed. And.

Specifically, for example, As + or P + is used as the n-type impurity, the acceleration energy is 6 keV, and the dose amount is 1 × 1016 cm-2.

[0054]

Next, in the step of FIG. 17, the resist film of the structure 41 in the step of FIG. 16 is removed, and then heat treatment is performed by the RTA (Rapid Thermal Annealing) method to perform shallow bonding regions 22a and 22b and deep bonding regions 24a and 24b. , And activate impurities in the pocket regions 23a, 23b.

[0055]

In the step of FIG. 17, for example, a Ni film, a Ti film, or a Co film having a thickness of 5 nm is formed so as to cover the surface of the structure, and heat treatment is performed to silicide the source / drain regions 28a and 28b. A silicide film 26 such as a NiSi2 film, a TiSi2 film, or a CoSi2 film is formed on the surface of the silicon substrate 11 and the surface of the gate electrode 16.

Next, the Ni film, Ti film, or Co film that has not been silicated is removed.

Although illustration and detailed description will be omitted in the subsequent steps, the structure of FIG. 17 is covered with an interlayer insulating film or the like to form contacts that penetrate the interlayer insulating film and come into contact with the source / drain regions 28a and 28b to provide interlayer insulation. A wiring layer is formed on the film and electrically connected to the contact, and a multi-layer interlayer insulating film, a wiring layer, vertical wiring, and the like are further formed to complete the semiconductor device.

[0056]

In the manufacturing method according to the present embodiment, after forming the compressive stress application portion 20 made of the SiGe film, impurities are injected to form the shallow bonding regions 22a and 22b and the deep bonding regions 23a and 23b. It is possible to prevent impurities, particularly impurities in the shallow bonding regions 22a and 22b, from diffusing directly under the gate insulating film 15 due to heating when forming the SiGe film.

Therefore, the n-MOS transistor is prevented by preventing the short-channel effect, increasing the hole mobility of the compression strain inducing portion 21 (channel region) of the p-MOS transistor 13a, and increasing the operating speed of the p-MOS transistor 13a. By balancing with the operating speed of 13b, the overall operating speed of the complementary semiconductor device 10 can be increased.

Further, the drain current of the p-MOS transistor 13a can be increased, and the characteristics of the drain current can be matched with those of the n-MOS transistor 13b.

[0057]

Further, in the manufacturing method according to the present embodiment, the compressive stress application portion 20 made of the SiGe film is formed in the source / drain region 28a and is separated from the end portion of the gate laminate 18, so that the SiGe film is formed. It is possible to suppress the diffusion of Ge atoms at the interface with the gate insulating film 15 by the heat treatment after the heat treatment, and to suppress the decrease in hole mobility due to the increase in the interface state.

[0058]

Further, in the manufacturing method according to the present embodiment, since the gate electrode 33 is protected by the cap layer 33 when forming the groove portion of the p-MOS region 30a in the steps of FIGS. 7 and 8, the gate electrode 33 of the gate electrode 33 is protected. It is possible to prevent etching of the surface and make the thickness of the gate electrode 33 equal to the thickness of the gate electrode 33 in the n-MOS region 30b.

As a result, the thickness of the third side wall insulating film 19 in the width direction can be formed to be substantially the same in the p-MOS region 30a and the n-MOS region 30b, and the distance between the two deep junction regions 24a and 24b in each region. Can be easily aligned.

As a result, the magnitude of parasitic capacitance can be made uniform.

[0059]

(Second Embodiment) A method for manufacturing a semiconductor device according to a second embodiment of the present invention will be described with reference to FIGS. 18 to 22.

18 to 22 are diagrams showing a manufacturing process of the semiconductor device according to the second embodiment.

In the figure, the same reference numerals are given to the parts corresponding to the parts described above, and the description thereof will be omitted.

[0060]

The second embodiment of the present invention is characterized in that a mask different from that of the first embodiment is used when etching the groove portion forming the compressive stress application portion.

[0061]

First, in the step of FIG. 18, the same steps as the steps of FIGS. 3 to 6 of the first embodiment are performed, and a silicon oxide film covering the surface of the silicon substrate 11, the gate laminate 18, and the cap layer 33 is performed. A structure in which 34-1 and the silicon nitride film 35-1 are deposited is formed.

[0062]

In the step of FIG. 18, the p-MOS region 30a and the n-MOS region 30b are simultaneously anisotropic of the silicon nitride film 35-1 and the silicon oxide film 34-1 by the RIE method until the surface of the silicon substrate 11 is exposed. Etching is performed to form a first side wall insulating film 34 made of a silicon oxide film covering both side surfaces of the gate laminate 18 and a second side wall insulating film 35 made of a silicon nitride film on the outside thereof.

Specifically, as the etching gas of the RIE method, for example, hydrofluorocarbons such as difluoromethane (CH2F2) and 1,1-difluoroethane (C2H4F2) are used.

[0063]

Next, in the step of FIG. 19, a resist film 51 (for example, a thickness of 500 nm) is formed so as to cover the structure of FIG. 18, and an opening is formed in the p-MOS region 30a of the resist film 51 by a photolithography method.

[0064]

In the step of FIG. 19, the surface of the silicon substrate 11 in the p-MOS region 30a is surface-treated using a CF4 gas and an O2 gas as process gases using an ashing device (hereinafter, referred to as "first surface treatment").).

The first surface treatment is performed so that the surface of the silicon substrate 11 in the n-MOS region 30b is not exposed.

By the first surface treatment, the surface serving as the source / drain region of the silicon substrate 11 in the p-MOS region 30a is modified, and the ashing modified film 52 (it is presumed that a fluoride film of Si is formed) is formed. It is formed.

[0065]

Specifically, in the first surface treatment, a parallel plate type plasma ashing device is used, the pressure in the chamber is 100 Pa to 1000 Pa, the CF4 gas flow rate is 4 sccm to 50 sccm, the O2 gas flow rate is 500 sccm to 1000 sccm, and the RF power is 300 W to 300 W. Set to 3000W and perform for about 20 seconds.

CH2F2, C2H4F2, etc. may be used instead of CF4 gas.

The surface of the resist film 51 is etched by surface treatment to reduce the thickness of the resist film 51 to become the resist film 51-1.

[0066]

Next, in the step of FIG. 20, the resist film 15-1 is removed using O2 gas as the process gas using an ashing device, and the surface of the silicon substrate 11 in the p-MOS region 30a and the n-MOS region 30b. Is surface-treated (hereinafter, referred to as "second surface treatment").

By the second surface treatment, the surface of the silicon substrate 11 in the p-MOS region 30a, which is the source / drain region, is further modified to form the ashing modified film 52-1.

Further, the surface of the silicon substrate 11 in the n-MOS region 30b is oxidized to form the silicon oxide film 53.

According to the study by the inventor of the present application, it has been confirmed that the ashing modified film 52 is inferior in hydrofluoric acid resistance to the silicon oxide film 53 and can be removed relatively easily with an aqueous hydrofluoric acid solution.

[0067]

Specifically, in the second surface treatment, the pressure in the chamber was set to 100 Pa to 1000 Pa, the O2 gas flow rate was set to 500 sccm to 1000 sccm, and the RF power was set to 300 W to 3000 W by using the same ashing device as in the step of FIG. Do it for about 20 seconds.

[0068]

Next, in the step of FIG. 21, only the ashing modified film in the p-MOS region 30a is removed by using the hydrofluoric acid aqueous solution to expose the surface of the silicon substrate 11 in the p-MOS region 30a.

At this time, since the silicon oxide film in the n-MOS region 30b is more resistant to acidity than the ashing modified film, the silicon oxide film remains.

[0069]

In the step of FIG. 21, the cap layer 33, the first side wall insulating film 34, the second side wall insulating film 35, and the silicon oxide film 53 of the n-MOS region 30b of the n-MOS region 30b and the p-MOS region 30a are further masked. As in the process of FIG. 8 of the first embodiment, the surface of the silicon substrate 11 of the p-MOS region 30a (the region between the second side wall insulating film 35 and the element separation region 12) is subjected to the RIE method. An anisotropic etching is performed with the above to form a groove portion 11-1 having a depth of, for example, 50 nm.

[0070]

In the step of FIG. 21, the groove portion is isotropically etched by a chemical dry etching method in the same manner as the step of FIG. 9 of the first embodiment.

The groove portion 11-2 is ground to a region inside the second side wall insulating film 35 from both ends.

[0071]

Next, in the step of FIG. 22, a SiGe film to be the compressive stress applying portion 20 is formed on the surface of the groove portion 11-2 of the structure of FIG. 21 by the CVD method in the same manner as the step of FIG. 10 of the first embodiment. Crystal growth.

[0072]

In the step of FIG. 22, a resist film (not shown) is further formed so as to cover the structure, the n-MOS region 30b of the resist film is opened by a photolithography method, and the silicon oxide film 53 is formed on a silicon substrate by the RIE method. Reactive etching is performed until the surface of No. 11 is exposed.

Anisotropic etching is performed in the same manner as in the step of FIG.

Then the resist film is removed.

[0073]

The following steps are the same as those in FIGS. 12 to 17 of the first embodiment, and the semiconductor device shown in FIG. 1 is completed.

[0074]

In the manufacturing method according to the present embodiment, the silicon oxide film 53 is formed on the surface of the silicon substrate 11 in the n-MOS region 30b by the first surface treatment and the second surface treatment, and the silicon oxide film 53 is formed on the surface of the p-MOS region 30a. It forms an ashing modified film 52-1 that is inferior in phosphoric acid resistance to the silicon oxide film 53.

That is, different films having etching selectivity with respect to the hydrofluoric acid aqueous solution are formed on the surfaces of the silicon substrate 11 of the p-MOS region 30a and the n-MOS region 30b.

Therefore, the surface of the silicon substrate can be exposed only in the p-MOS region 30a by the hydrofluoric acid treatment, and the grooves 11-1 and 11-2 can be easily formed.

[0075]

Further, in the manufacturing method according to the present embodiment, the anisotropic etching of the silicon oxide film 34-1 and the silicon nitride film 35-1 is performed simultaneously in the p-MOS region 30a and the n-MOS region 30b, so that they are performed separately. The number of steps can be reduced as compared with the manufacturing method of the first embodiment, and the first side wall insulating film 34 and the second side wall insulating film 35 of the p-MOS region 30a and

the n-MOS region 30b are formed to have substantially the same dimensions. Therefore, the conditions for removing the first side wall insulating film 34 and the second side wall insulating film 35 can be easily set, and the occurrence of uneven removal can be suppressed.

Needless to say, the manufacturing method according to the present embodiment has the same effect as the effect of the manufacturing method according to the first embodiment.

[0076]

(Third Embodiment) A method of manufacturing a semiconductor device according to a third embodiment of the present invention will be described with reference to FIGS. 23 to 29.

23 to 29 are diagrams showing a manufacturing process of the semiconductor device according to the third embodiment.

In the figure, the same reference numerals are given to the parts corresponding to the parts described above, and the description thereof will be omitted.

[0077]

The third embodiment of the present invention differs from the first embodiment in that the shallow joint region has two stages.

[0078]

The method for manufacturing the semiconductor device according to the third embodiment is the same as that of the first embodiment in FIGS. 2 to 14.

That is, in the step of FIG. 13, the shallow junction region 22b is formed by implanting n-type impurities into the silicon substrates 11 on both sides of the gate laminate 18 using the gate laminate as a mask in the n-MOS region 30b by the ion implantation method. Then, in the step of FIG. 14, by the ion implantation method, the gate laminate 18 is used as a mask in the p-MOS region 30a, and p-type impurities are implanted into the silicon substrates 11 on both sides of the gate laminate 18 to form a shallow junction region 22a. do.

The pocket region 23b may or may not be formed.

[0079]

Next, in the step of FIG. 23, the resist film 39 of FIG. 14 is removed, and a silicon oxide film (not shown) having a thickness of 5 to 50 nm is formed on the surface of the structure by a CVD method.

Specifically, for example, by the thermal CVD method, BTBAS (Bis (Tertiary-butylamino) Silane, C8H22N2Si) gas and O2 gas are used as raw material gases, the pressure is 0.1 Pa to 1000 Pa, and the substrate temperature is 500 ° C to 580 ° C. To form a silicon oxide film.

[0080]

In the step of FIG. 23, the silicon oxide film is further etched (etched back) by the RIE method until the surface of the silicon substrate 11 is exposed, and both side surfaces of the gate laminate 18 of the p-MOS region 30a and the n-MOS region 30b. A thin fourth side wall insulating film 60 is formed.

Specifically, as the etching gas of the RIE method, for example, hydrofluorocarbons such as difluoromethane (CH2F2) and 1,1-difluoroethane (C2H4F2) are used.

[0081]

Next, in the step of FIG. 24, a resist film 61 is formed so as to cover the structure of FIG. 23, an opening is formed in the p-MOS region 30a of the resist film 61 by a photolithography method, and an ion implantation method is used. Using the gate laminate 18 and the fourth side wall insulating film 60 as a mask in the p-MOS region 30a, p-type impurities are implanted into the silicon substrates 11 on both sides of the fourth side wall insulating film 60 to apply a compressive stress made of a SiGe film. A slightly deeper joint region 62a is formed up to a slightly deeper position at the bottom of 20.

Specifically, for example, B + is used as the p-type impurity, the acceleration energy is 6 keV, and the dose amount is 2 × 1015 cm-2.

Next, the resist film 61 is removed.

[0082]

Next, in the step of FIG. 25, the resist film 63 is formed in substantially the same manner as the p-MOS region 30a, and the n-MOS region 30b of the resist film 63 is formed with an opening 41-1 by a photolithography method to form an ion. By the implantation method, the gate laminate 18 and the fourth side wall insulating film 60 are used as masks, and n-type impurities are implanted into the silicon substrates 11 on both sides of the fourth side wall insulating film 60 to form a slightly deeper bonding region 24b.

Specifically, for example, As + or P + is used as the n-type impurity, the acceleration energy is 7 keV, and the dose amount is 2 × 1015 cm-2.

Next, the resist film 63 is removed.

[0083]

Next, in the step of FIG. 26, a silicon oxide film (not shown) having a thickness of 30 to 100 nm is formed on the surface of the structure by a CVD method.

Specifically, for example, by the thermal CVD method, BTBAS (Bis (Tertiary-butylamino) Silane, C8H22N2Si) gas and O2 gas are used as raw material gases, the pressure is 0.1 Pa to 1000 Pa, and the substrate temperature is 500 ° C to 580 ° C. To form a silicon oxide film.

[0084]

In the step of FIG. 26, the silicon oxide film is further etched (etched back) by the RIE method until the surface of the silicon substrate 11 is exposed, and both side surfaces of the gate laminate 18 of the p-MOS region 30a and the n-MOS region 30b. A fifth side wall insulating film 64 is formed which further covers both side surfaces of the thin fourth side wall insulating film 60.

Specifically, as the etching gas of the RIE method, for example, hydrofluorocarbons such as difluoromethane (CH2F2) and 1,1-difluoroethane (C2H4F2) are used.

[0085]

Next, in the step of FIG. 27, a resist film 65 is formed so as to cover the structure of FIG. 26, an opening is formed in the p-MOS region 30a of the resist film 65 by a photolithography method, and an ion injection method is used. Using the gate laminate 18, the fourth side wall insulating film 60, and the fifth side wall insulating film 64 as masks in the p-MOS region 30a, p-type impurities are injected into the silicon substrates 11 on both sides of the fifth side wall insulating film 64, and SiGe A deep bonding region 66a is formed deeper than the bottom of the compressive stress applying portion 20 made of a film to form a source / drain region 28a.

Specifically, for example, B + is used as the p-type impurity, the acceleration energy is 8 keV, and the dose amount is 5 × 1015 cm-2.

Next, the resist film 61 is removed.

[0086]

Next, in the step of FIG. 28, the resist film 66 is formed in substantially the same manner as the p-MOS region 30a, and the n-MOS region 30b of the resist film 66 is formed with an opening 41-1 by a photolithography method to form an ion. By the implantation method, the gate laminate 18, the fourth side wall insulating film 60 and the fifth side wall insulating film 64 are used as masks, and n-type impurities are implanted into the silicon substrates 11 on both sides of the fifth side wall insulating film 64 to form a deep bonding region 66b. Is formed into a source / drain region 28b.

Specifically, for example, As + or P + is used as the n-type impurity, the acceleration energy is 6 keV, and the dose amount is 1 × 1016 cm-2.

Next, the resist film 66 is removed.

[0087]

Next, in the step of FIG. 29, the resist film 66 of the structure 41 in the step of FIG. 28 is removed, and then heat treatment is performed by the RTA (Rapid Thermal Annealing) method to perform shallow bonding regions 22a and 22b and slightly deep bonding regions 62a. , 62b, activates impurities in the deep junction regions 66a, 66b.

As a result, the shallow junction regions 22a and 22b and the slightly deeper junction regions 62a and 62b form a p-MOS transistor 13a and an n-MOS transistor 13b having two shallow junction regions.

[0088]

In the step of FIG. 29, for example, a Ni film, a Ti film, or a Co film having a thickness of 5 nm is formed so as to cover the surface of the structure, and heat treatment is performed to silicide the source / drain regions 28a and 28b. A silicide film 26 such as a NiSi2 film, a TiSi2 film, or a CoSi2 film is formed on the surface of the silicon substrate 11 and the surface of the gate electrode 16.

Next, the Ni film, Ti film, or Co film that has not been silicated is removed.

[0089]

(Example) A semiconductor device having a p-MOS transistor 13a and an n-MOS transistor 13b (hereinafter referred to as "Example") was manufactured by the method for manufacturing a semiconductor device according to the first embodiment of the present invention.

[0090]

For comparison, the p-MOS transistor 13a and the n-MOS transistor are manufactured by the same semiconductor device manufacturing method as in the first embodiment except that the compressive stress application portion 20 made of SiGe is not formed on the p-MOS transistor 13a. A semiconductor device having 13b (hereinafter referred to as "comparative example") was manufactured.

[0091]

Various electrical properties were measured for these examples and comparative examples.

The measurement results are shown in FIGS. 30 to 32.

In FIGS. 30 to 32, ● is a measurement point of each embodiment, and ○ is a measurement point of each comparative example.

[0092]

FIG. 30 is a graph showing the relationship between the turn-on current (Ion) and the turn-off current (Ioff) of the p-MOS transistor in each Example and each Comparative Example.

The measurement points of each example are indicated by ●, and the measurement points of comparative examples are indicated by ○.

[0093]

In FIG. 30, when the turn-on currents of the p-MOS transistors having a turn-off current (Ioff) of about 7E-8 [nA / μm] are compared, the comparative example (○) is about 0.35 [mA / μm]. On the other hand, in Example (●), it was about 0.46 [mA / μm], which was found to be improved by about 31% by the present invention.

[0094]

FIG. 31 is a graph showing the relationship between the gate length Lg (SEM) [nm] and the threshold value Vth [V] of the p-MOS transistor in each Example and each Comparative Example.

The measurement points of each example are indicated by ⊗, and the measurement points of comparative examples are indicated by ○.

[0095]

In the case of the embodiment (⊗), in order to form the SiGe film which is the compressive stress applying portion 20, the substrate temperature is set to 500 ° C. to 800 ° C. by the reduced pressure thermal CVD method (see the process of FIG. 10). is required.

On the other hand, the comparative example (◯) does not require such high temperature treatment.

[0096]

As can be seen from FIG. 31, there is no significant difference between the examples and the comparative examples, and it can be seen that the high temperature treatment for forming the SiGe film does not deteriorate the threshold characteristics of the p-MOS transistor.

[0097]

FIG. 32 is a graph showing the relationship between the gate voltage Vg [V] of the p-MOS transistor in each example and each comparative example and the transconductance Gm [mS / mm] when Vdd is 0.02 V.

The measurement points of each example are indicated by ⊗, and the measurement points of comparative examples are indicated by ○.

[0098]

In FIG. 32, when the transconductance of the p-MOS transistors having a gate voltage of −1.0 [V] is compared, the comparative example (◯) is about 560 [mS / mm], whereas the embodiment (⊗).) Was about 800 [mS / mm], which was found to be improved by about 43% by the present invention.

[0099]

(Embodiment of Modification) Although the preferred embodiment of the present invention has been described in detail above, the present invention is not limited to the specific embodiment, and the scope of the present invention described in the claims. Within, various modifications and changes are possible.

[0100]

For example, in the above embodiment, the MOS transistor has been described as an example, but it goes without saying that the manufacturing method of the present invention can be applied to the MIS transistor as well.

For example, as described above, a silicon acid nitride film or a silicon nitride film may be used instead of the silicon oxide film of the gate insulating film, and a high-k material such as Al2O3, Ta2O3, HfO2, ZrO2, perovskite crystal structure may be used. For example, PbTiO3, BaTiO3, Pb (Zr, Ti) O3 and the like may be used.

[0101]

As described in detail above, the features of the present invention can be summarized as follows.

(Appendix 1) A method for manufacturing a semiconductor device including a p-type transistor formed in a first region of a semiconductor substrate and an n-type transistor formed in a second region of the semiconductor substrate, which is on the semiconductor substrate. A step of forming a gate laminated body composed of a gate insulating film and a gate electrode, and a step of forming a first side wall insulating film and a second side wall insulating film on both side surfaces of the gate laminated body in the first region. Then, in a state where the surface of the semiconductor substrate in the second region is covered with an etching resistant film, the second side wall insulating film is used as a mask in the first side wall insulating film and the second side wall insulating film in the first region. A step of forming a groove on the semiconductor substrate outside the film, a step of forming a compressive stress application portion in the groove, and removing the first side wall insulating film and

the second side wall insulating film in the first region. , The step of removing the etching resistant film in the second region, the step of forming the first bonding region in the first region and the second region using the gate laminate as a mask, and the gate lamination. A third side wall insulating film is formed on both side surfaces of the body, and a second bonding region is formed in the first region and the second region using the gate laminate and the third side wall insulating film as masks. A method for manufacturing a semiconductor device, which comprises a process.

(Appendix 2) In the step of forming the first side wall insulating film and the second side wall insulating film, the first insulating film and the second insulating film covering the surface of the semiconductor substrate and the gate laminate are sequentially formed. The step comprises the step of anisotropically etching the first insulating film and the second insulating film in the first region, and in the step of forming the groove, the etching resistant film in the second region is second. The method for manufacturing a semiconductor device according to Appendix 1, wherein the insulating film is the same as above.

(Supplementary Note 3) The method for manufacturing a semiconductor device according to Supplementary note 1, wherein the step of forming the groove portion is a resist film covering the second region.

(Appendix 4) A method for manufacturing a semiconductor device including a p-type transistor formed in a first region of a semiconductor substrate and an n-type transistor formed in a second region of the semiconductor substrate, which is formed on the semiconductor substrate. A step of forming a gate laminate composed of a gate insulating film and a gate electrode, a first side wall insulating film and a second side wall insulating film are formed on both side surfaces of the gate laminated body, and the second side wall insulating film is formed. The step of exposing the outer semiconductor substrate surface of the above, the step of forming a resist film covering the second region, and the step of ionizing and irradiating CF4 gas and O2 gas to modify the surface of the semiconductor substrate in the first region. In the first surface treatment step of quality, the resist film is removed in the second region by ionizing and irradiating the O2 gas, and an oxide film is formed on the surface of the semiconductor substrate exposed to the outside of the second side wall insulating film. A second surface treatment step, a step of exposing the surface of the semiconductor substrate in the first region, and a first side wall insulating film, a second side wall insulating film, and a second region of the first region. A step of forming a groove on the semiconductor substrate outside the second side wall insulating film using the oxide film as a mask, a step of forming a compressive stress application portion in the groove, and a first side wall insulating film in the first region. And the step of removing the etching resistant film in the second region while removing the second side wall insulating film, and the first in the first region and the second region using the gate laminate as a mask. The step of forming the joint region, the third side wall insulating film is formed on both side surfaces of the gate laminate, and the first region and the second side wall insulating film are used as masks of the gate laminate and the third side wall insulating film. A method for manufacturing a semiconductor device, which comprises a step of forming a second junction region in the region of

(Appendix 5) After the step of forming the first joining region in the first region and the second region, and before the step of forming the second joining region, the third is formed on both side surfaces of the gate laminate. A fourth side wall insulating film thinner than the side wall insulating film is formed, and the gate laminate and the fourth side wall insulating film are used as masks in the first region and the second region from the first bonding region. The step of forming a third joining region deeper than the second joining region is further provided, and the step of forming the second joining region in the first region and the second region includes the gate laminate and the said. The third side wall insulating film is formed on both side surfaces of the fourth side wall insulating film, and the first region is masked by the gate laminate, the fourth side wall insulating film, and the third side wall insulating film. A method for manufacturing a semiconductor device, which comprises forming the second junction region in the second region.

(Supplementary Note 6) The step of forming the groove portion comprises a process of performing anisotropic etching on the semiconductor substrate outside the second side wall insulating film and a process of performing isotropic etching. 5. The method for manufacturing a semiconductor device according to any one of 5.

(Appendix 7) The method for manufacturing a semiconductor device according to Appendix 6, wherein the isotropic etching is chemical dry etching using hydrogen chloride gas or chlorine gas.

(Appendix 8) The method for manufacturing a semiconductor device according to Appendix 6, wherein the distance between the end of the groove and the end of the gate laminate is set in the range of 5 nm to 80 nm.

(Supplementary note 9) The step of forming the compressive stress application portion according to any one of Supplementary note 1 to 8, wherein a semiconductor material larger than the lattice constant of the semiconductor constituting the semiconductor substrate is epitaxially grown in the groove portion. The method for manufacturing a semiconductor device according to the description.

(Appendix 10) After the step of forming the gate laminate, a step of forming a cap layer on the gate laminate is further provided, and in the step of forming the groove, the cap layer is used as a mask of the gate laminate. The method for manufacturing a semiconductor device according to any one of Supplementary Provisions 1 to 9, wherein the semiconductor device is manufactured.

(Appendix 11) The method for manufacturing a semiconductor device according to Appendix 10, wherein the step of forming the compressive stress application portion uses the cap layer as a mask of a gate laminate.

(Supplementary Note 12) The method for manufacturing a semiconductor device according to any one of Supplementary note 1 to 11, wherein the semiconductor substrate is a silicon substrate, and the compressive stress applying portion is made of a SiGe film or a SiGeC film.

[0102]

It is sectional drawing of the conventional p-MOS transistor.

It is sectional drawing of the semiconductor device formed by the manufacturing method of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (the 1) of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (the 2) of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (the 3) of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (the 4) of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (the 5) of the semiconductor device which concerns on 1st Embodiment of this invention.

FIG. 6 is a manufacturing process diagram (No. 6) of the semiconductor device according to the first embodiment of the present invention.

FIG. 7 is a manufacturing process diagram (No. 7) of the semiconductor device according to the first embodiment of the present invention.

It is a manufacturing process diagram (8) of the semiconductor device which concerns on 1st Embodiment of this invention.

FIG. 9 is a manufacturing process diagram (No. 9) of the semiconductor device according to the first embodiment of the present invention.

It is a manufacturing process drawing (10) of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (11) of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (12) of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (13) of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (14) of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (15) of the semiconductor device which concerns on 1st Embodiment of this invention.

It is a manufacturing process drawing (the 1) of the semiconductor device which concerns on 2nd Embodiment of this invention.

It is a manufacturing process drawing (the 2) of the semiconductor device which concerns on 2nd Embodiment of this invention.

It is a manufacturing process drawing (the 3) of the semiconductor device which concerns on 2nd Embodiment of this invention.

It is a manufacturing process drawing (the 4) of the semiconductor device which concerns on 2nd Embodiment of this invention.

FIG. 5 is a manufacturing process diagram (No. 5) of the semiconductor device according to the second embodiment of the present invention.

It is a manufacturing process drawing (the 1) of the semiconductor device which concerns on 3rd Embodiment of this invention.

It is a manufacturing process drawing (the 2) of the semiconductor device which concerns on 3rd Embodiment of this invention.

It is a manufacturing process drawing (the 3) of the semiconductor device which concerns on 3rd Embodiment of this invention.

It is a manufacturing process drawing (the 4) of the semiconductor device which concerns on 3rd Embodiment of this invention.

It is a manufacturing process drawing (the 5) of the semiconductor device which concerns on 3rd Embodiment of this invention.

FIG. 6 is a manufacturing process diagram (No. 6) of the semiconductor device according to the third embodiment of the present invention.

It is a manufacturing process diagram (7) of the semiconductor device which concerns on 3rd Embodiment of this invention.

It is a graph which shows the relationship between the turn-on current and the turn-off current of a p-MOS transistor in an Example and a comparative example.

It is a graph which shows the relationship between the gate length and the threshold value of the p-MOS transistor in an Example and a comparative example.

It is a graph which shows the relationship between the gate voltage and the transconductance of a p-MOS transistor in an Example and a comparative example.

Code description

[0103]

10 ... Semiconductor device 11 ... Silicon substrate 11-1, 11-2 ... Groove 12 ... Element separation region 13a ... p-MOS transistor 13b ... n-MOS transistor 15, 15-1 ... Gate insulating film 16 ... Gate electrode 16-1 ... Gate electrode film 18 ... Gate laminate 19 ... Third side wall insulating film 20 ... Compressive stress application portion 21 ... Compressive strain inducing portions 22a, 22b ... Shallow junction regions 23a, 23b ... Pocket regions 24a, 24b ... Deep junction regions 26 ... VDD films 28a, 28b ... Source / drain regions 30a ... p-MOS regions 30b ... n-MOS regions 31-1 ... Trench 32a ... n-type well regions 32b ... p-type well regions 33 ... Cap layers 33-1, 35-1 ... Silicon nitride film 34 ... 1st side wall insulating film 34-1 ... Silicon oxide film 35 ... 2nd side wall insulating film 36, 38, 39, 41, 51, 51-1 ... Resist film 52, 52-1 ... Ashing modification Film 53 ... Silicon oxide film 60 ... Fourth side wall insulating film 61, 63, 65, 66 ... Resist films 62a, 62b ... Slightly deep shallow bonding region 64 ... Fifth side wall insulating film 66a, 66b ... Deep bonding region

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

CLAIMS JP2006013428A

1.

A method for manufacturing a semiconductor device including a p-type transistor formed in a first region of a semiconductor substrate and an n-type transistor formed in a second region of the semiconductor substrate, wherein a gate insulating film is formed on the semiconductor substrate. A step of forming a gate laminated body including the gate electrode and a step of forming a first side wall insulating film and a second side wall insulating film on both side surfaces of the gate laminated body in the first region, and the first. With the surface of the semiconductor substrate in the second region covered with an etching resistant film, the outer side of the second side wall insulating film is covered with the first side wall insulating film and the second side wall insulating film as a mask in the first region. A step of forming a groove in the semiconductor substrate, a step of forming a compressive stress application portion in the groove, and removing the first side wall insulating film and the second side wall insulating film in the first region, and the second side wall insulating film. A step of removing the etching-resistant film in the region of the above, a step of forming a first bonding region in the first region and the second region using the gate laminate as a mask, and both side surfaces of the gate laminate. A step of forming a third side wall insulating film in the first region and forming a second bonding region in the first region and the second region using the gate laminate and the third side wall insulating film as a mask. A method for manufacturing a semiconductor device, which comprises the present invention.

2.

The steps of forming the first side wall insulating film and the second side wall insulating film include a step of sequentially forming a first insulating film and a second insulating film covering the surface of the semiconductor substrate and the gate laminate, and the above-mentioned step. In the step of anisotropically etching the first insulating film and the second insulating film in the first region and forming the groove portion, the etching resistant film in the second region is the second insulating film. The method for manufacturing a semiconductor device according to claim 1, wherein the semiconductor device is provided.

3.

A method for manufacturing a semiconductor device including a p-type transistor formed in the first region of a semiconductor substrate and an n-type transistor formed in the second region of the semiconductor substrate, wherein a gate insulating film and a gate insulating film are formed on the semiconductor substrate. A step of forming a gate laminate composed of gate electrodes, a first side wall insulating film and a second side wall insulating film are formed on both side surfaces of the gate laminate, and a semiconductor outside the second side wall insulating film is formed. A step of exposing the substrate surface, a step of forming a resist film covering the second region, and a first step of ionizing and irradiating CF4 gas and O2 gas to modify the surface of the semiconductor substrate in the first region. 2 The surface treatment step, the step of exposing the surface of the semiconductor substrate in the first region, and the masking of the first side wall insulating film, the second side wall insulating film, and the oxide film in the second region of the first region. As a step of forming a groove on the semiconductor substrate outside the second side wall insulating film, a step of forming a compressive stress application portion in the groove, and the first side wall insulating film and the second side wall insulating film in the first region. A step of removing the side wall

insulating film and the etching resistant film in the second region, and forming a first bonding region in the first region and the second region using the gate laminate as a mask. A third side wall insulating film is formed on both side surfaces of the gate laminate, and the gate laminate and the third side wall insulating film are used as masks in the first region and the second region. A method for manufacturing a semiconductor device, which comprises a step of forming a bonding region of two.

4.

After the step of forming the first bonding region in the first region and the second region, and before the step of forming the second bonding region, the third side wall insulating film is formed on both side surfaces of the gate laminate. A thinner fourth side wall insulating film is formed, and the gate laminate and the fourth side wall insulating film are used as masks in the first region and the second region deeper than the first bonding region. The step of forming a third joining region shallower than the joining region of the above is further provided, and the step of forming the second joining region in the first region and the second region is the gate laminate and the fourth side wall. The third side wall insulating film is formed on both side surfaces of the insulating film, and the first region and the second side wall insulating film are used as masks of the gate laminate, the fourth side wall insulating film, and the third side wall insulating film. A method for manufacturing a semiconductor device, which comprises forming the second junction region in the region.

5.

Any of claims 1 to 4, wherein the step of forming the groove includes a process of performing anisotropic etching on the semiconductor substrate outside the second side wall insulating film and a process of performing isotropic etching. The method for manufacturing a semiconductor device according to item 1.

6.

The method for manufacturing a semiconductor device according to claim 4, wherein the groove portion has a distance between the end portion and the end portion of the gate laminate set in the range of 5 nm to 80 nm.

7.

The semiconductor according to any one of claims 1 to 6, wherein in the step of forming the compressive stress application portion, a semiconductor material larger than the lattice constant of the semiconductor constituting the semiconductor substrate is epitaxially grown in the groove portion. Manufacturing method of the device.

8.

After the step of forming the gate laminate, a step of forming a cap layer on the gate laminate is further provided, and the step of forming the groove is characterized in that the cap layer is used as a mask of the gate laminate. The method for manufacturing a semiconductor device according to any one of claims 1 to 7.

9.

The method for manufacturing a semiconductor device according to claim 8, wherein the step of forming the compressive stress application portion uses the cap layer as a mask of a gate laminate.

10.

The method for manufacturing a semiconductor device according to any one of claims 1 to 9, wherein the semiconductor substrate is a silicon substrate, and the compressive stress applying portion is made of a SiGe film or a SiGeC film.

(19)日本国特許庁(JP)　(12)公開特許公報(A)　(11)特許出願公開番号
特開2006-13428
(P2006-13428A)
(43)公開日　平成18年1月12日(2006.1.12)

(51)Int.Cl.		F I			テーマコード（参考）
H01L 21/8238	(2006.01)	H01L	27/08	321E	5F048
H01L 27/092	(2006.01)	H01L	29/78	301S	5F110
H01L 29/78	(2006.01)	H01L	29/78	616V	5F140
H01L 29/786	(2006.01)	H01L	29/78	616L	
H01L 21/336	(2006.01)	H01L	29/78	613A	

審査請求 未請求　請求項の数 10　ＯＬ　（全 25 頁）

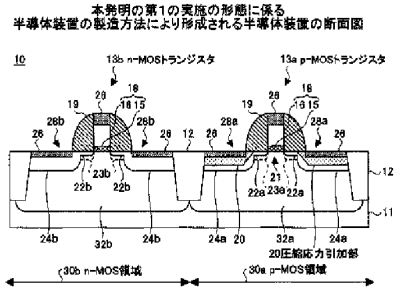
(21)出願番号　特願2005-46573 (P2005-46573)
(22)出願日　平成17年2月23日 (2005.2.23)
(31)優先権主張番号　特願2004-156569 (P2004-156569)
(32)優先日　平成16年5月26日 (2004.5.26)
(33)優先権主張国　日本国(JP)

(71)出願人　000005223
富士通株式会社
神奈川県川崎市中原区上小田中４丁目１番１号
(74)代理人　100087479
弁理士　北野　好人
(74)代理人　100114915
弁理士　三村　治彦
(72)発明者　金　永▲ソク▼
神奈川県川崎市中原区上小田中４丁目１番１号　富士通株式会社内
(72)発明者　森　年史
神奈川県川崎市中原区上小田中４丁目１番１号　富士通株式会社内

最終頁に続く

(54)【発明の名称】半導体装置の製造方法

(57)【要約】
【課題】ｐ型トランジスタの動作速度を高め、ｎ型トランジスタとの動作速度の均衡がとれた半導体装置の製造方法を提供する。
【解決手段】ｐ－ＭＯＳ領域３０ａのソース／ドレイン領域にＳｉＧｅ膜からなる圧縮応力印加部２０を形成し、その後にｐ－ＭＯＳ領域３０ａおよびｎ－ＭＯＳ領域３０ｂに不純物注入を行い、浅い接合領域２２ａ、２２ｂおよび深い接合領域２３ａ、２３ｂを形成する。ＳｉＧｅ膜を形成する際の加熱により浅い接合領域２２ａ、２２ｂの不純物がゲート絶縁膜１５の直下に拡散することを防止し、短チャネル効果を防止すると共に、ｐ－ＭＯＳトランジスタ１３ａのチャネル領域の正孔移動度を高め、ｎ－ＭＯＳトランジスタ１３ｂの動作速度との均衡により、相補型の半導体装置１０の総合的な動作速度を高める。
【選択図】図２



【特許請求の範囲】
【請求項1】
半導体基板の第１の領域に形成されたｐ型トランジスタと、該半導体基板の第２の領域に形成されたｎ型トランジスタからなる半導体装置の製造方法であって、
前記半導体基板上にゲート絶縁膜およびゲート電極からなるゲート積層体を形成する工程と、
前記第１の領域において、前記ゲート積層体の両側面に第１の側壁絶縁膜および第２の側壁絶縁膜を形成する工程と、
前記第２の領域の半導体基板表面を耐エッチング膜により覆った状態で、前記第１の領域において第１の側壁絶縁膜および第２の側壁絶縁膜をマスクとして、該第２の側壁絶縁膜の外側の半導体基板に溝部を形成する工程と、
前記溝部に圧縮応力印加部を形成する工程と、
前記第１の領域において第１の側壁絶縁膜および第２の側壁絶縁膜を除去すると共に、前記第２の領域において耐エッチング膜を除去する工程と、
前記ゲート積層体をマスクとして、前記第１の領域および前記第２の領域に第１の接合領域を形成する工程と、
前記ゲート積層体の両側面に第３の側壁絶縁膜を形成し、前記ゲート積層体および第３の側壁絶縁膜をマスクとして、前記第１の領域および前記第２の領域に第２の接合領域を形成する工程と、
を備えることを特徴とする半導体装置の製造方法。
【請求項2】
前記第１の側壁絶縁膜および第２の側壁絶縁膜を形成する工程は、
前記半導体基板の表面およびゲート積層体を覆う第１の絶縁膜および第２の絶縁膜を順次形成する工程と、
前記第１の領域において第１の絶縁膜および第２の絶縁膜を異方性エッチングする工程からなり、
前記溝部を形成する工程は、前記第２の領域の耐エッチング膜が第２の絶縁膜であることを特徴とする請求項１記載の半導体装置の製造方法。
【請求項3】
半導体基板の第１の領域に形成されたｐ型トランジスタと、該半導体基板の第２の領域に形成されたｎ型トランジスタからなる半導体装置の製造方法であって、
半導体基板上にゲート絶縁膜およびゲート電極からなるゲート積層体を形成する工程と、
前記ゲート積層体の両側面に第１の側壁絶縁膜および第２の側壁絶縁膜を形成すると共に、該第２の側壁絶縁膜の外側の半導体基板表面を露出する工程と、
前記第２の領域を覆うレジスト膜を形成する工程と、
CF_4ガスおよびO_2 ガスを電離すると共に照射して前記第１の領域の半導体基板表面を改質する第１の表面処理工程と、
O_2 ガスを電離すると共に照射して第２の領域においてレジスト膜を除去すると共に、第２の側壁絶縁膜の外側に露出する半導体基板表面に酸化膜を形成する第２の表面処理工程と、
前記第１の領域の半導体基板表面を露出する工程と、
前記第１の領域の第１の側壁絶縁膜、第２の側壁絶縁膜、および第２の領域の酸化膜をマスクとして、第２の側壁絶縁膜の外側の半導体基板に溝部を形成する工程と、
前記溝部に圧縮応力印加部を形成する工程と、
前記第１の領域において第１の側壁絶縁膜および第２の側壁絶縁膜を除去すると共に、前記第２の領域において耐エッチング膜を除去する工程と、
前記ゲート積層体をマスクとして、前記第１の領域および前記第２の領域に第１の接合領域を形成する工程と、

前記ゲート積層体の両側面に第３の側壁絶縁膜を形成し、前記ゲート積層体および第３の側壁絶縁膜をマスクとして、前記第１の領域および前記第２の領域に第２の接合領域を形成する工程と、
を備えることを特徴とする半導体装置の製造方法。
【請求項4】
第１の領域および第２の領域に第１の接合領域を形成する工程の後、第２の接合領域を形成する工程する前に、
前記ゲート積層体の両側面に前記第３の側壁絶縁膜より薄い第４の側壁絶縁膜を形成し、前記ゲート積層体および第４の側壁絶縁膜をマスクとして、前記第１の領域および前記第２の領域に前記第１の接合領域より深く前記第２の接合領域より浅い第３の接合領域を形成する工程を更に有し、
第１の領域および第２の領域に第２の接合領域を形成する工程は、
前記ゲート積層体および前記第４の側壁絶縁膜の両側面に前記第３の側壁絶縁膜を形成し、前記ゲート積層体、前記第４の側壁絶縁膜および前記第３の側壁絶縁膜をマスクとして、前記第１の領域および前記第２の領域に前記第２の接合領域を形成する
を備えることを特徴とする半導体装置の製造方法。
【請求項5】
前記溝部を形成する工程は、
第２の側壁絶縁膜の外側の半導体基板を異方性エッチングを行う処理と、
等方性エッチングを行う処理からなる
ことを特徴とする請求項１乃至４のいずれか１項に記載の半導体装置の製造方法。
【請求項6】
前記溝部は、その端部とゲート積層体の端部との距離を５ｎｍ～８０ｎｍの範囲に設定することを特徴とする請求項４記載の半導体装置の製造方法。
【請求項7】
前記圧縮応力印加部を形成する工程は、前記溝部に半導体基板を構成する半導体の格子定数よりも大きな半導体材料をエピタキシャル成長させることを特徴とする請求項１乃至６のいずれか１項に記載の半導体装置の製造方法。
【請求項8】
前記ゲート積層体を形成する工程の後に、該ゲート積層体上にキャップ層を形成する工程をさらに備え、
前記溝部を形成する工程は、キャップ層をゲート積層体のマスクとすることを特徴とする請求項１乃至７のいずれか１項に記載の半導体装置の製造方法。
【請求項9】
前記圧縮応力印加部を形成する工程は、前記キャップ層をゲート積層体のマスクとすることを特徴とする請求項８記載の半導体装置の製造方法。
【請求項10】
前記半導体基板がシリコン基板であり、前記圧縮応力印加部がＳｉＧｅ膜あるいはＳｉＧｅＣ膜からなることを特徴とする請求項１乃至９のいずれか１項に記載の半導体装置の製造方法。
【発明の詳細な説明】
【技術分野】
【0001】
本発明は、ｐ型トランジスタのチャネルに圧縮歪みを誘起した相補型のＭＩＳ（Metal Insulator Semiconductor）型の半導体装置の製造方法に関する。
【背景技術】
【0002】
半導体装置は、高速動作、低消費電力化、高集積化等の高性能化のため、最小加工寸法の微細化が図られてきた。最小加工寸法が６５ｎｍ以下の世代では、微細化の技術的困難性が極めて高くなり、また、微細化のみによる高性能化に限界が見え始めている。
【0003】

そこで、微細化によらない高性能トランジスタとして、ＭＩＳ型あるいはＭＯＳ型トランジスタのチャネル領域のシリコン単結晶に歪みを誘起させた、いわゆる歪みシリコントランジスタが注目されている。歪みシリコントランジスタは、Ｓｉ単結晶よりも格子定数の大きいＳｉＧｅ膜上にＳｉ単結晶膜を形成し、ＳｉＧｅ膜の格子定数を引き継いだＳｉ単結晶膜に引っ張り歪みを誘起させることにより、Ｓｉ単結晶膜の電子移動度を向上することができる。このような歪みＳｉ単結晶膜をチャネルとして使用し、動作速度を向上したｎ型トランジスタが提案されている。

【0004】

一方、通常のＳｉ単結晶中の正孔移動度（１９００ｃｍ^2／（Ｖ・ｓ））は電子移動度（３９００ｃｍ^2／（Ｖ・ｓ））よりも小さいので、ｐ型トランジスタとｎ型トランジスタを備えた相補型の半導体装置では、ｐ型トランジスタの動作速度が遅いため、半導体装置の全体の動作速度が遅くなる。ましてや、歪みシリコン基板を使用してｎ型トランジスタの高速動作化を図っても、半導体装置全体の動作速度の向上が図れず、歪みシリコン基板の高コスト等の問題が生ずる。

【0005】

そこで、ｐ型トランジスタの動作速度を高めるために、図１に示すように、ｐ型トランジスタのソース／ドレイン領域にＳｉＧｅ膜１０１，１０２を形成し、ＳｉＧｅ膜１０１，１０２によりゲート酸化膜１０３の下側のチャネル部（Ｓｉ単結晶）１０４に圧縮応力を印加して正孔移動度を向上させる半導体装置が提案されている（特許文献１参照）。r/>

【特許文献1】米国特許第６６２１１３１号明細書

【発明の開示】

【発明が解決しようとする課題】

【0006】

特許文献１では、ｐ型トランジスタの浅い接合領域１０５と深い接合領域１０６からなる不純物拡散領域を形成した後に、ソース／ドレイン領域に溝１０１ａ，１０２ａを形成し、溝１０１ａ、１０２ａの表面に熱ＣＶＤ法によりＳｉＧｅ膜１０１，１０２を形成する。

【0007】

しかしながら、不純物拡散領域を形成した後に、ＳｉＧｅ膜１０１，１０２を形成する際に７４０℃程度に加熱されることによって不純物が拡散し短チャネル効果が生じ、特にゲート長が１００ｎｍ以下のトランジスタでは閾値電圧のロールオフ特性が悪化するという問題がある。

【0008】

また、上記特許文献１では、ｐ型トランジスタとｎ型トランジスタからなる相補型の半導体装置の具体的な製造方法については開示されていない。

【0009】

本発明の目的は、ｐ型トランジスタの動作速度を高め、ｎ型トランジスタとの動作速度の均衡がとれた新規な半導体装置の製造方法を提供することである。

【課題を解決するための手段】

【0010】

本発明の一観点によれば、半導体基板の第１の領域に形成されたｐ型トランジスタと、該半導体基板の第２の領域に形成されたｎ型トランジスタからなる半導体装置の製造方法であって、前記半導体基板上にゲート絶縁膜およびゲート電極からなるゲート積層体を形成する工程と、前記第１の領域において、前記ゲート積層体の両側面に第１の側壁絶縁膜および第２の側壁絶縁膜を形成する工程と、前記第２の領域の半導体基板表面を耐エッチング膜により覆った状態で、前記第１の領域において第１の側壁絶縁膜および第２の側壁絶縁膜をマスクとして、該第２の側壁絶縁膜の外側の半導体基板に溝部を形成する工程と、前記溝部に圧縮応力印加部を形成する工程と、前記第１の領域において第１の側壁絶縁膜および第２の側壁絶縁膜を除去すると共に、前記第２の領域において耐エッチング膜を

除去する工程と、前記ゲート積層体をマスクとして、第１の領域および第２の領域に第１の接合領域を形成する工程と、前記ゲート積層体の両側面に第３の側壁絶縁膜を形成し、前記ゲート積層体および第３の側壁絶縁膜をマスクとして、第１の領域および第２の領域に第２の接合領域を形成する工程と、を備える半導体装置の製造方法が提供される。

【0011】

本発明の他の観点によれば、圧縮応力印加部を形成した後で第１の接合領域および第２の接合領域を形成するための不純物注入を行っているので、圧縮応力印加部を形成する際の加熱により不純物、特に第１の接合領域の不純物がゲート絶縁膜の直下に拡散することを防止できる。したがって、短チャネル効果を防止する共に、ｐ型トランジスタのチャネル領域の正孔移動度を高め、ｐ型トランジスタの動作速度を高めることにより、ｎ型トランジスタの動作速度との均衡により、相補型の半導体装置の総合的な動作速度を高めることができる。また、ｐ型トランジスタのドレイン電流を増加することができ、ドレイン電流の点でもｎ型トランジスタと特性を揃えることができる。

【0012】

本発明の他の観点によれば、半導体基板の第１の領域に形成されたｐ型トランジスタと、該半導体基板の第２の領域に形成されたｎ型トランジスタからなる半導体装置の製造方法であって、半導体基板上にゲート絶縁膜およびゲート電極からなるゲート積層体を形成する工程と、前記ゲート積層体の両側面に第１の側壁絶縁膜および第２の側壁絶縁膜を形成すると共に、該第２の側壁絶縁膜の外側の半導体基板表面を露出する工程と、前記第２の領域を覆うレジスト膜を形成する工程と、ＣＦ4ガスおよびO2ガスを電離すると共に照射して前記第１の領域の半導体基板表面を改質する第１の表面処理工程と、O2ガスを電離すると共に照射して第２の領域においてレジスト膜を除去すると共に、第２の側壁絶縁膜の外側に露出する半導体基板表面に酸化膜を形成する第２の表面処理工程と、前記第１の領域の半導体基板表面を露出する工程と、前記第１の領域の第１の側壁絶縁膜、第２の側壁絶縁膜、および第２の領域の酸化膜をマスクとして、第２の側壁絶縁膜の外側の半導体基板に溝部を形成する工程と、前記溝部に圧縮応力印加部を形成する工程と、前記第１の領域において第１の側壁絶縁膜および第２の側壁絶縁膜を除去すると共に、前記第２の領域において耐エッチング膜を除去する工程と、前記ゲート積層体をマスクとして、第１の領域および第２の領域に第１の接合領域を形成する工程と、前記ゲート積層体の両側面に第３の側壁絶縁膜を形成し、前記ゲート積層体および第３の側壁絶縁膜をマスクとして、第１の領域および第２の領域に第２の接合領域を形成する工程と、を備えることを特徴とする半導体装置の製造方法が提供される。

【0013】

本発明の他の観点によれば、上述した発明と同様の効果を奏すると共に、第１の表面処理および第２の表面処理により第２の領域の半導体基板の表面に酸化膜を形成すると共に、第１の領域の表面に、酸化膜よりも耐フッ酸性の劣るアッシング改質膜を形成する。すなわち、フッ酸水溶液に対するエッチング選択性を有する異なる膜を第１の領域と第２の領域の半導体基板の表面に形成する。したがって、第２の領域の半導体基板表面を酸化膜によりマスクした状態で、フッ酸処理により第１の領域だけを半導体基板表面を露出でき、圧縮応力印加部が形成される溝部を容易に形成できる。

【発明の効果】

【0014】

本発明によれば、ｐ型トランジスタの動作速度を高め、ｎ型トランジスタとの動作速度の均衡がとれた半導体装置が実現できる。

【発明を実施するための最良の形態】

【0015】

（第１の実施の形態）

本発明の第１の実施の形態に係る半導体装置の製造方法について、図２乃至図１７を用いて説明する。図２は、本発明の第１の実施の形態に係る半導体装置の製造方法により形成される半導体装置の断面図である。図３乃至図１７は、第１の実施の形態に係る半導体

装置の製造工程を示す図である。

【0016】

図２を参照するに、半導体装置１０は、シリコン基板１１に形成された素子分離領域１２により離隔されたｐ－ＭＯＳトランジスタ１３ａとｎ－ＭＯＳトランジスタ１３ｂから構成されている。ｐ－ＭＯＳトランジスタ１３ａは、ゲート絶縁膜１５とゲート電極１６からなるゲート積層体１８の両側面に設けられた第３側壁絶縁膜１９が接するシリコン基板１１の表面から外側に、例えばＳｉＧｅからなる圧縮応力印加部２０が形成され、圧縮応力印加部２０は、ゲート積層体１８および第３側壁絶縁膜１９の下側のＳｉからなる圧縮歪み誘起部２１を、その両側から挟むように形成されている。圧縮応力印加部２０のＳｉＧｅ膜は、Ｓｉよりも格子定数が大きいことから、圧縮応力印加部２０がチャネル領域を挟む方向に応力を印加し、チャネル領域に圧縮歪みが誘起される。その結果、チャネル領域の正孔移動度が向上し、ｐ－ＭＯＳトランジスタ１３ａの高速動作が可能となる。

【0017】

なお、実施の形態では、ｐ－ＭＯＳトランジスタ１３ａが形成される領域をｐ－ＭＯＳ領域３０ａ、ｎ－ＭＯＳトランジスタ１３ｂが形成される領域をｎ－ＭＯＳ領域３０ｂと呼ぶ。以下、半導体装置１０の製造方法を詳細に説明する。

【0018】

図３～図１７は、第１の実施の形態に係る半導体装置の製造工程を示す図である。

【0019】

最初に、図３の工程では、シリコン基板１１にＳＴＩ（Shallow Trench Isolation）法により素子分離領域１２を形成する。具体的には、シリコン基板１１のトレンチエッチングによりトレンチ３１－１を形成し、トレンチ３１－１の内壁の熱酸化、ＣＶＤ法によるシリコン酸化膜の充填を行い、次いでＣＭＰ法による平坦化を行い、素子分離領域１２を形成する。

【0020】

なお、シリコン基板１１は、バルク基板でもＳＯＩ（Silicon On Insulator）基板でもよい。ＳＯＩ基板を用いることにより、後の工程で形成されるソース／ドレイン領域と基板との間に生じる空乏層による寄生容量を低減して、トランジスタの動作速度を向上することができる。また、ＳＴＩ法は公知の方法を用いる。

【0021】

図３の工程では、さらに、イオン注入法によりシリコン基板１１のｐ－ＭＯＳ領域３０ａにAs^+、P^+などのｎ型不純物イオンを打込み、ｎ－ＭＯＳ領域３０ｂにB^+、BF_2^+などのｐ型不純物イオンを打込み、それぞれｎ型ウェル領域３２ａ、ｐ型ウェル領域３２ｂを形成する。

【0022】

次いで、図４の工程では、シリコン基板１１の表面のシリコン自然酸化膜（図示せず）をＨＦ（ふっ酸）処理により除去し、ＣＶＤ法、スパッタ法、あるいは熱酸化処理により、例えば厚さが１．２ｎｍのシリコン酸化膜１５－１（後にゲート絶縁膜となる）を形成する。具体的には、熱酸化処理は、例えば酸素雰囲気中で６００℃～１１００℃の温度で１分間～２０分間行い、０．５ｎｍ～３ｎｍの厚さのシリコン酸化膜１５－１を形成する。

【0023】

なお、シリコン酸化膜１５－１の代わりに、シリコン酸窒化膜やシリコン窒化膜でもよく、さらにこれらの膜とシリコン酸化膜との積層体でもよく、公知の絶縁膜を用いることができる。

【0024】

図４の工程では、さらに、シリコン酸化膜１５－１上に、ＣＶＤ法により、厚さ１００ｎｍのノンドープのポリシリコン膜１６－１（後にゲート電極となる）を形成する。具体的には、例えば減圧ＣＶＤ法により、チャンバー内圧力を１０Ｐａ～５０Ｐａ、基板温度を６００℃～６５０℃の範囲で加熱して、モノシランガスを流量５０ｓｃｃｍ～３００ｓ

ｃｃｍ、５分間～６０分間流して、厚さ２０ｎｍ～２００ｎｍのポリシリコン膜１６－１を形成する。PH_3ガス等を混合して、P^+やB^+をドープしたドープトポリシリコン膜を形成してもよい。

【0025】

図４の工程では、さらに、ポリシリコン膜１６－１上に、ＣＶＤ法により、厚さ１０ｎｍ～５０ｎｍのシリコン窒化膜３３－１（後にキャップ層となる）を形成する。具体的には、例えば基板温度を６５０℃、圧力２０Ｐａに設定して、ジクロロシランガス（流量６６０ｓｃｃｍ）およびアンモニアガス（流量８７０ｓｃｃｍ）を用いて形成する。

【0026】

次いで、図５の工程では、シリコン窒化膜３３－１上にレジスト膜（図示せず）を形成し、フォトリソグラフィ法によりゲート積層体となる領域のレジスト膜を残すパターニングを行う。次いでＲＩＥ（Reactive Ion Etching）法により、パターニングされたレジスト膜をマスクとしてシリコン窒化膜３３－１、ポリシリコン膜１６－１およびシリコン酸化膜１５－１をエッチングして、各々、キャップ層３３、ゲート電極１６、ゲート絶縁膜１５を形成する。ゲート長は、例えば１０ｎｍ～９０ｎｍの範囲に設定する。

【0027】

次いで、図６の工程では、図５の構造体を覆うように、ＣＶＤ法により厚さ１０ｎｍのシリコン酸化膜３４－１を形成する。具体的には、熱ＣＶＤ法によりＴＥＯＳ（tetraeth oxy silane）を用いて基板温度を５５０℃～７００℃の範囲に設定して、厚さ５ｎｍ～３０ｎｍのシリコン酸化膜３４－１を形成する。

【0028】

図６の工程ではさらに、シリコン酸化膜３４－１を覆うように、ＣＶＤ法により厚さ４０ｎｍのシリコン窒化膜３５－１を形成する。具体的には、減圧ＣＶＤ法によりジクロロシランガス（流量６６０ｓｃｃｍ）およびアンモニアガス（流量８７０ｓｃｃｍ）を用いて、圧力２０Ｐａ、基板温度を６００℃～８００℃に設定して、厚さ１０ｎｍ～１００ｎｍのシリコン窒化膜３５－１を形成する。

【0029】

次いで、図７の工程では、図６の構造体を覆うようにレジスト膜３６を形成し、フォトリソグラフィ法によりレジスト膜３６のｐ－ＭＯＳ領域３０ａに開口部３６－１を形成する。

【0030】

図７の工程ではさらに、ＲＩＥ法によりシリコン窒化膜３５－１およびシリコン酸化膜３４－１をシリコン基板１１の表面が露出するまで異方性エッチングを行い、ゲート積層体の両側面を覆うシリコン酸化膜からなる第１側壁絶縁膜３４と、その外側にシリコン窒化膜からなる第２側壁絶縁膜３５が形成される。具体的には、ＲＩＥ法のエッチングガスとしては、例えば、ジフルオロメタン（CH_2F_2）、１，１－ジフルオロエタン（$C_2H_4F_2$）等のハイドロフルオロカーボンを用い、第１側壁絶縁膜３４の厚さを５ｎｍ～３０ｎｍ、第２側壁絶縁膜３５の厚さを１０ｎｍ～６０ｎｍに範囲に設定する。

【0031】

次いで、図８の工程では、図７の構造体の表面を、ｎ－ＭＯＳ領域３０ｂを覆うレジスト膜３６と、ｐ－ＭＯＳ領域３０ａのキャップ層３３、第１側壁絶縁膜３４、および第２側壁絶縁膜３５をマスクとして、露出するシリコン基板１１の表面（第２側壁絶縁膜３５と素子分離領域１２との間の領域）をＲＩＥ法により異方性エッチングを行い、例えば５０ｎｍの深さの溝部１１－１を形成する。具体的には、ＲＩＥ法のエッチングガスとしては、例えば、臭化水素（ＨＢｒ）等を用い、溝部１１－１の深さを１０ｎｍ～１５０ｎｍに設定する。

【0032】

なお、図８の工程では、ｎ－ＭＯＳ領域３０ｂは、異方性エッチングを行う前にレジスト膜を除去し、シリコン窒化膜３５－１をマスクとしてもよい。この場合は、シリコン窒化膜３５－１の厚さは１０ｎｍ～１００ｎｍの範囲に設定することが好ましい。

【0033】
次いで、図９の工程では、ｎ－ＭＯＳ領域３０ｂのレジスト膜を除去し、次いで、溝部１１－１の表面の自然酸化膜をフッ酸水溶液で除去後、ｎ－ＭＯＳ領域３０ｂのシリコン窒化膜３５－１およびシリコン酸化膜３４－１と、ｐ－ＭＯＳ領域３０ａのキャップ層３３、第１側壁絶縁膜３４、および第２側壁絶縁膜３５をマスクとして、図８の構造体の溝部１１－１をケミカルドライエッチング法により研削する。
【0034】
ケミカルドライエッチング法を用いることにより、等方的に溝部１１－１をエッチングして、第２側壁絶縁膜３５の両端よりも内側に入り込んだシリコン基板１１まで研削される。具体的には、ケミカルドライエッチング法は、塩化水素（ＨＣｌ）ガスあるいは塩素（Cl_2）ガスを用いて、圧力を０．１Ｐａ～１００００Ｐａ、基板温度を６００℃～９００℃の範囲に設定する。エッチング量は、ゲート絶縁膜の端部から溝部の端部との距離Ｘが５ｎｍ～８０ｎｍの範囲になるように設定する。
【0035】
また、ケミカルドライエッチング法は、塩化水素ガス等がＳｉと化学反応を起こして溝部表面が研削されるので、ＲＩＥ法等のプラズマを用いる場合よりも溝部表面に与える衝撃を抑制することができ、また、研削の等方性に優れている。
【0036】
なお、ケミカルドライエッチング法の替わりにウエットエッチングを用いてもよい。次の工程における圧縮応力印加部２０の形成はチャンバー内で行われるので、ハンドリングの点でケミカルドライエッチング法の方が好ましい。
【0037】
次いで、図１０の工程では、図９の構造体の溝部１１－２の表面にＣＶＤ法により圧縮応力印加部２０となるＳｉＧｅ膜を結晶成長させる。ＳｉＧｅ膜は、例えばＳｉの（００１）面上に（００１）面を高さ方向としてエピタキシャル成長させる。
【0038】
ＳｉＧｅ膜はＳｉよりも格子定数が大きいので、ＳｉＧｅ膜がＳｉからなる圧縮歪み誘起部２１（チャネルが形成される。）に対して両側から挟むように圧縮応力を印加し、圧縮歪み誘起部２１に圧縮歪みを形成する。
【0039】
ＳｉＧｅ膜は、具体的には、減圧熱ＣＶＤ法により、原料ガスとして、SiH_2Cl_2（流量：５０～３００ｓｃｃｍ）、GeH_4（流量：５０～３００ｓｃｃｍ）、$SiCH_6$（流量：２～５０ｓｃｃｍ）、ＨＣｌ（流量：３０～３００ｓｃｃｍ）、およびH_2（流量：１００ｓｃｃｍ～１００ｓｌｍ）の各ガスを用いて、圧力１００～５０００Ｐａ、基板温度を５００℃～８００℃に設定し、シリコン基板１１の表面と一致する高さまでＳｉＧｅ膜を成長させる。このような工程により、Ｓｉが露出した溝部表面にのみＳｉＧｅ膜を選択的に成長させることができる。
【0040】
なお、ゲート電極の表面はキャップ層３３に覆われているので、ゲート電極表面のＳｉＧｅ膜の形成を防止できる。
【0041】
ＳｉＧｅ膜の組成は、溝部表面のＳｉとのエピタキシャル成長の点で、Ｇｅ濃度が１原子％～４０原子％の範囲に設定されることが好ましく、５原子％～４０原子％に設定されることがさらに好ましい。
【0042】
なお、Ｓｉソースガスとして、SiH_2Cl_2ガスの替わりにSiH_4、Si_2H_6、Si_3H_8、またはSi_3Cl_6ガスを用いてもよく、これらのガスを２種以上用いてもよい。Ｇｅソースガスとして、GeH_4ガスの替わりにGeH_2Cl_2ガスを用いてもよく、これらのガスを混合して用いてもよい。ＨＣｌガスの替わりにCl_2ガスを用いてもよく、混合して用いてもよい。また、ＨＣｌガスおよびCl_2ガスを用いなくともよい。ＨＣｌガ

スあるいはCl_2ガスを添加することで、溝部１１－２以外の表面に付着したＳｉＧｅ粒子を除去することができる。

【0043】

また、圧縮応力印加部２０の高さをシリコン基板１１の表面よりも高く成長させた、いわゆるせり上げた構造（Elevated S/D）としてもよい。さらに、圧縮応力印加部２０はＳｉＧｅＣ膜から構成されてもよく、Ｃ（炭素）濃度が０原子％よりも大きく、かつ２原子％以下に設定することが好ましい。ＳｉＧｅＣ膜を用いることによりＳｉＧｅ膜よりも熱安定性を高めることができる。Ｃ濃度が２原子％を超えるとＳｉＧｅＣ膜の結晶性が低下する。

【0044】

次いで、図１１の工程では、図１０の構造体を覆うように、レジスト膜（図示せず）を形成し、フォトリソグラフィ法によりレジスト膜のｎ－ＭＯＳ領域３０ｂに開口部を形成し、ＲＩＥ法により、シリコン窒化膜３５－１およびシリコン酸化膜３４－１をシリコン基板１１の表面が露出するまで異方性エッチングを行い、ゲート積層体１８の両側面を覆うシリコン酸化膜からなる第１側壁絶縁膜３４と、その外側にシリコン窒化膜からなる第２側壁絶縁膜３５が形成される。ＲＩＥ法は、具体的には、図７の工程と同様に行う。次いで、レジスト膜を除去する。

【0045】

次いで、図１２の工程では、ウエットエッチング法により、図１１の構造体のキャップ層３３、第２側壁絶縁膜３５、および第１側壁絶縁膜３４を除去し、シリコン基板１１の表面にゲート積層体を残す。具体的には、シリコン窒化膜からなるキャップ層３３および第２側壁絶縁膜３５は例えばリン酸水溶液、シリコン酸化膜からなる第１側壁絶縁膜３４は、例えばフッ酸水溶液を用いて除去する。

【0046】

次いで、図１３の工程では、図１２の構造体を覆うように、レジスト膜（図示せず）を形成し、フォトリソグラフィ法によりレジスト膜のｎ－ＭＯＳ領域３０ｂを開口する。次いで、イオン注入法により、ｎ－ＭＯＳ領域３０ｂにゲート積層体をマスクとして、ゲート積層体１８の両側のシリコン基板１１に、シリコン基板１１に対して斜めにｐ型不純物を注入してポケット領域２３ｂを形成する。具体的には、ｐ型不純物としては、例えばＩｎを用い、加速エネルギーを５０ｋｅＶ、ドーズ量を$5\times10^{13}cm^{-2}$とする。

【0047】

図１３の工程ではさらに、イオン注入法により、ｎ－ＭＯＳ領域３０ｂにゲート積層体をマスクとして、ゲート積層体１８の両側のシリコン基板１１にｎ型不純物を注入して浅い接合領域２２ｂを形成する。具体的には、ｎ型不純物としては、例えばAs^+を用い、加速エネルギーを５ｋｅＶ、ドーズ量を$1\times10^{15}cm^{-2}$とする。なお、ポケット領域２３ｂは形成してもよく、形成しなくてもよい。

【0048】

次いで、図１４の工程では、図１３の構造体のレジスト膜３８を除去し、図１３の工程と同様にしてｐ－ＭＯＳ領域３０ａが開口するレジスト膜３９を形成する。次いで、イオン注入法により、ｐ－ＭＯＳ領域３０ａにゲート積層体１８をマスクとして、ゲート積層体１８の両側のシリコン基板１１に斜めにｎ型不純物を注入してポケット領域２３ａを形成する。具体的には、ｎ型不純物としては、例えばＳｂ+を用い、加速エネルギーを６０ｋｅＶ、ドーズ量を$5\times10^{13}cm^{-2}$とする。

【0049】

図１４の工程ではさらに、イオン注入法によりｐ－ＭＯＳ領域３０ａにゲート積層体１８をマスクとして、ゲート積層体１８の両側のシリコン基板１１にｐ型不純物を注入して浅い接合領域２２ａを形成する。具体的には、ｐ型不純物としては、例えばB^+を用い、加速エネルギーを５ｋｅＶ、ドーズ量を$1\times10^{15}cm^{-2}$とする。

【0050】

次いで、図１５の工程では、図１４のレジスト膜３９を除去し、構造体の表面にＣＶＤ

法により厚さ８０ｎｍのシリコン酸化膜（図示せず）を形成する。具体的には、例えば熱ＣＶＤ法により、原料ガスとして、ＢＴＢＡＳ（Bis(Tertiary-butylamino)Silane、$C_8H_{22}N_2Si$）ガスとO_2ガスを用いて、圧力０．１Ｐａ～１０００Ｐａ、基板温度を５００℃～５８０℃に設定し、シリコン酸化膜を形成する。

【0051】

図１５の工程では、さらに、ＲＩＥ法によりシリコン酸化膜をシリコン基板１１の表面が露出するまでエッチング（エッチバック）し、ｐ－ＭＯＳ領域３０ａおよびｎ－ＭＯＳ領域３０ｂのゲート積層体１８の両側面を覆う第３側壁絶縁膜１９が形成される。具体的には、ＲＩＥ法のエッチングガスとしては、例えば、ジフルオロメタン（CH_2F_2）、１，１－ジフルオロエタン（$C_2H_4F_2$）等のハイドロフルオロカーボンを用いる。

【0052】

次いで、図１６の工程では、図１５の構造体を覆うように、レジスト膜（図示せず）を形成し、フォトリソグラフィ法によりレジスト膜のｐ－ＭＯＳ領域３０ａに開口部を形成し、イオン注入法により、ｐ－ＭＯＳ領域３０ａにゲート積層体１８および第３側壁絶縁膜１９をマスクとして、第３側壁絶縁膜１９の両側のシリコン基板１１にｐ型不純物を注入して、ＳｉＧｅ膜からなる圧縮応力印加部２０の底よりも深い位置まで深い接合領域２４ａを形成し、ソース／ドレイン領域２８ａとする。具体的には、ｐ型不純物としては、例えばB^+を用い、加速エネルギーを８ｋｅＶ、ドーズ量を$5\times10^{15}cm^{-2}$とする。次いで、レジスト膜を除去する。

【0053】

図１６の工程では、さらに、ｐ－ＭＯＳ領域３０ａと略同様にして、レジスト膜４１を形成し、フォトリソグラフィ法によりレジスト膜のｎ－ＭＯＳ領域３０ｂを開口部４１－１を形成し、イオン注入法により、ゲート積層体１８および第３側壁絶縁膜をマスクとして、第３側壁絶縁膜１９の両側のシリコン基板１１にｎ型不純物を注入して深い接合領域２４ｂを形成し、ソース／ドレイン領域２８ｂとする。具体的には、ｎ型不純物としては例えばAs^+またはP^+を用い、加速エネルギーを６ｋｅＶ、ドーズ量を$1\times10^{16}cm^{-2}$とする。

【0054】

次いで、図１７の工程では、図１６の工程の構造体４１のレジスト膜を除去し、次いで、ＲＴＡ（Rapid Thermal Annealing）法により熱処理を行い、浅い接合領域２２ａ，２２ｂ、深い接合領域２４ａ，２４ｂ、およびポケット領域２３ａ，２３ｂの不純物を活性化する。

【0055】

図１７の工程ではさらに、構造体の表面を覆うように、例えば厚さ５ｎｍのＮｉ膜、Ｔｉ膜、あるいはＣｏ膜を形成し、加熱処理を行ってシリサイド化し、ソース／ドレイン領域２８ａ，２８ｂのシリコン基板１１の表面、およびゲート電極１６の表面に$NiSi_2$膜、$TiSi_2$膜、$CoSi_2$膜などのシリサイド膜２６を形成する。次いで、シリサイド化しなかったＮｉ膜、Ｔｉ膜、あるいはＣｏ膜を除去する。この後の工程は図示および詳しい説明を省略するが、図１７の構造体を層間絶縁膜等により覆い、層間絶縁膜を貫通しソース／ドレイン領域２８ａ，２８ｂと接触するコンタクトを形成し、層間絶縁膜上に配線層を形成してコンタクトと電気的に接続し、さらに多層の層間絶縁膜や配線層、垂直配線等を形成し、半導体装置が完成する。

【0056】

本実施の形態に係る製造方法では、ＳｉＧｅ膜からなる圧縮応力印加部２０を形成した後で浅い接合領域２２ａ，２２ｂおよび深い接合領域２３ａ，２３ｂを形成するための不純物注入を行っているので、ＳｉＧｅ膜を形成する際の加熱により不純物、特に浅い接合領域２２ａ、２２ｂの不純物がゲート絶縁膜１５の直下に拡散することを防止できる。したがって、短チャネル効果を防止する共に、ｐ－ＭＯＳトランジスタ１３ａの圧縮歪み誘起部２１（チャネル領域）の正孔移動度を高め、ｐ－ＭＯＳトランジスタ１３ａの動作速度を高めることにより、ｎ－ＭＯＳトランジスタ１３ｂの動作速度との均衡により、相補

型の半導体装置１０の総合的な動作速度を高めることができる。また、ｐ－ＭＯＳトランジスタ１３ａのドレイン電流を増加することができ、ドレイン電流の点でもｎ－ＭＯＳトランジスタ１３ｂと特性を揃えることができる。

【0057】

また、本実施の形態に係る製造方法では、ＳｉＧｅ膜からなる圧縮応力印加部２０は、ソース／ドレイン領域２８ａに形成し、ゲート積層体１８の端部から離隔されているので、ＳｉＧｅ膜を形成した後の熱処理によりゲート絶縁膜１５との界面にＧｅ原子が拡散することを抑制し、界面準位の増加による正孔移動度の低下を抑制できる。

【0058】

また、本実施の形態に係る製造方法では、図7および図8の工程においてｐ－ＭＯＳ領域３０ａの溝部を形成する際にキャップ層３３によりゲート電極３３が保護されているので、ゲート電極３３の表面のエッチングを防止してゲート電極３３の厚さをｎ－ＭＯＳ領域３０ｂのゲート電極３３の厚さと揃えることができる。その結果、ｐ－ＭＯＳ領域３０ａとｎ－ＭＯＳ領域３０ｂとで、第３側壁絶縁膜１９の幅方向の厚さをほぼ同一に形成でき、各々の領域の２つの深い接合領域２４ａ，２４ｂの距離を容易に揃えることができる。その結果、寄生容量の大きさを揃えることができる。

【0059】

（第２の実施の形態）

本発明の第２の実施の形態に係る半導体装置の製造方法について、図１８乃至図２２を用いて説明する。図１８乃至図２２は、第２の実施の形態に係る半導体装置の製造工程を示す図である。図中、先に説明した部分に対応する部分には同一の参照符号を付し、説明を省略する。

【0060】

本発明の第２の実施の形態は、圧縮応力印加部を形成する溝部をエッチングする際に、第１の実施の形態とは異なるマスクを用いる点に特徴がある。

【0061】

最初に、図１８の工程では、第１の実施の形態の図３～図６の工程と同様の工程を行い、シリコン基板１１の表面、ゲート積層体１８、およびキャップ層３３を覆うシリコン酸化膜３４－１およびシリコン窒化膜３５－１が堆積した構造体を形成する。

【0062】

図１８の工程ではさらに、ｐ－ＭＯＳ領域３０ａとｎ－ＭＯＳ領域３０ｂを同時に、ＲＩＥ法によりシリコン窒化膜３５－１およびシリコン酸化膜３４－１をシリコン基板１１の表面が露出するまで異方性エッチングを行い、ゲート積層体１８の両側面を覆うシリコン酸化膜からなる第１側壁絶縁膜３４と、その外側にシリコン窒化膜からなる第２側壁絶縁膜３５を形成する。具体的には、ＲＩＥ法のエッチングガスとしては、例えば、ジフルオロメタン（CH_2F_2）、１，１－ジフルオロエタン（$C_2H_4F_2$）等のハイドロフルオロカーボンを用いる。

【0063】

次いで、図１９の工程では、図１８の構造体を覆うようにレジスト膜５１（例えば厚さ５００ｎｍ）を形成し、フォトリソグラフィ法によりレジスト膜５１のｐ－ＭＯＳ領域３０ａに開口部を形成する。

【0064】

図１９の工程ではさらに、アッシング装置を用い、プロセスガスとしてCF_4ガスとO_2ガスを使用してｐ－ＭＯＳ領域３０ａのシリコン基板１１の表面を表面処理する（以下、「第１表面処理」と呼ぶ）。第１表面処理はｎ－ＭＯＳ領域３０ｂのシリコン基板１１の表面が露出しない程度に行う。第１表面処理により、ｐ－ＭＯＳ領域３０ａのシリコン基板１１のソース／ドレイン領域となる表面が改質され、アッシング改質膜５２（Ｓｉのフッ化物膜が形成されていると推定される）が形成される。

【0065】

第１表面処理は、具体的には、平行平板型プラズマアッシング装置を用いて、チャンバ

ー内の圧力を１００Ｐａ～１０００Ｐａ、CF_4ガス流量を４ｓｃｃｍ～５０ｓｃｃｍ、O_2ガス流量を５００ｓｃｃｍ～１０００ｓｃｃｍ、ＲＦ電力３００Ｗ～３０００Ｗに設定し、２０秒程度行う。なお、CF_4ガスの代わりに、CH_2F_2、$C_2H_4F_2$等を用いてもよい。なお、レジスト膜５１は、表面処理により表面がエッチングされて厚さが減少してレジスト膜５１－１となる。

【0066】

次いで、図２０の工程では、アッシング装置を用いて、プロセスガスとしてO_2ガスを使用してレジスト膜１５－１を除去すると共に、ｐ－ＭＯＳ領域３０ａおよびｎ－ＭＯＳ領域３０ｂのシリコン基板１１の表面を表面処理する（以下、「第２表面処理」と呼ぶ）。第２表面処理により、ｐ－ＭＯＳ領域３０ａのシリコン基板１１のソース／ドレイン領域となる表面がさらに改質されてアッシング改質膜５２－１が形成される。また、ｎ－ＭＯＳ領域３０ｂのシリコン基板１１の表面が酸化され、シリコン酸化膜５３が形成される。本願発明者の検討によれば、アッシング改質膜５２は、シリコン酸化膜５３よりも耐フッ酸性が劣り、フッ酸水溶液により比較的容易に除去できることが確認されている。

【0067】

第２表面処理は、具体的には、図１９の工程と同様のアッシング装置を用いて、チャンバー内の圧力を１００Ｐａ～１０００Ｐａ、O_2ガス流量を５００ｓｃｃｍ～１０００ｓｃｃｍ、ＲＦ電力３００Ｗ～３０００Ｗに設定し、２０秒程度行う。

【0068】

次いで、図２１の工程では、フッ酸水溶液を用いて、ｐ－ＭＯＳ領域３０ａのアッシング改質膜のみを除去し、ｐ－ＭＯＳ領域３０ａのシリコン基板１１の表面を露出させる。この際、ｎ－ＭＯＳ領域３０ｂのシリコン酸化膜は、アッシング改質膜よりも耐フッ酸性に優れるのでシリコン酸化膜は残留する。

【0069】

図２１の工程ではさらに、ｎ－ＭＯＳ領域３０ｂおよびｐ－ＭＯＳ領域３０ａのキャップ層３３、第１側壁絶縁膜３４、および第２側壁絶縁膜３５、ｎ－ＭＯＳ領域３０ｂのシリコン酸化膜５３をマスクとして、第１の実施の形態の図８の工程と同様にして、ｐ－ＭＯＳ領域３０ａのシリコン基板１１の表面（第２側壁絶縁膜３５と素子分離領域１２との間の領域）をＲＩＥ法により異方性エッチングを行い、例えば５０ｎｍの深さの溝部１１－１を形成する。

【0070】

図２１の工程ではさらに、第１の実施の形態の図９の工程と同様にして、溝部をケミカルドライエッチング法により等方的にエッチングを行う。溝部１１－２は第２側壁絶縁膜３５の両端よりも内側に入り込んだ領域まで研削される。

【0071】

次いで、図２２の工程では、第１の実施の形態の図１０の工程と同様にして、図２１の構造体の溝部１１－２の表面にＣＶＤ法により圧縮応力印加部２０となるＳｉＧｅ膜を結晶成長させる。

【0072】

図２２の工程ではさらに、構造体を覆うようにレジスト膜（図示せず）を形成し、フォトリソグラフィ法によりレジスト膜のｎ－ＭＯＳ領域３０ｂを開口し、ＲＩＥ法によりシリコン酸化膜５３をシリコン基板１１の表面が露出するまで異方性エッチングを行う。異方性エッチングは図７の工程と同様に行う。次いでレジスト膜を除去する。

【0073】

以下の工程は、第１の実施の形態の図１２～図１７と同様の工程を行い、図１に示す半導体装置が完成する。

【0074】

本実施の形態に係る製造方法では、第１表面処理および第２表面処理によりｎ－ＭＯＳ領域３０ｂのシリコン基板１１の表面にシリコン酸化膜５３を形成すると共に、ｐ－ＭＯＳ領域３０ａの表面に、シリコン酸化膜５３よりも耐フッ酸性の劣るアッシング改質膜５

２－１を形成する。すなわち、フッ酸水溶液に対するエッチング選択性を有する異なる膜をｐ－ＭＯＳ領域３０ａとｎ－ＭＯＳ領域３０ｂのシリコン基板１１の表面に形成する。したがって、フッ酸処理によりｐ－ＭＯＳ領域３０ａだけをシリコン基板表面を露出でき、溝部１１－１、１１－２を容易に形成できる。

【0075】

また、本実施の形態に係る製造方法では、シリコン酸化膜３４－１およびシリコン窒化膜３５－１の異方性エッチングをｐ－ＭＯＳ領域３０ａとｎ－ＭＯＳ領域３０ｂを同時に行うので、それぞれ別に行う第１の実施の形態の製造方法よりも工程数を低減でき、また、ｐ－ＭＯＳ領域３０ａとｎ－ＭＯＳ領域３０ｂの第１側壁絶縁膜３４と第２側壁絶縁膜３５をほぼ同じ寸法に形成できるので、第１側壁絶縁膜３４と第２側壁絶縁膜３５を除去する際の条件の設定が容易となり除去むらの発生を抑制できる。なお、本実施の形態に係る製造方法は、第１の実施の形態に係る製造方法の効果と同様の効果を奏することはいうまでもない。

【0076】

（第３の実施の形態）

本発明の第３の実施の形態に係る半導体装置の製造方法について、図２３乃至図２９を用いて説明する。図２３乃至図２９は、第３の実施の形態に係る半導体装置の製造工程を示す図である。図中、先に説明した部分に対応する部分には同一の参照符号を付し、説明を省略する。

【0077】

本発明の第３の実施の形態は、浅い接合領域が２段である点が第１の実施の形態とは異なる。

【0078】

第３の実施の形態に係る半導体装置の製造方法は、図２乃至図１４までは第１の実施の形態と同じである。すなわち、図１３の工程において、イオン注入法により、ｎ－ＭＯＳ領域３０ｂにゲート積層体をマスクとして、ゲート積層体１８の両側のシリコン基板１１にｎ型不純物を注入して浅い接合領域２２ｂを形成し、図１４の工程において、イオン注入法によりｐ－ＭＯＳ領域３０ａにゲート積層体１８をマスクとして、ゲート積層体１８の両側のシリコン基板１１にｐ型不純物を注入して浅い接合領域２２ａを形成する。なお、ポケット領域２３ｂは形成してもよく、形成しなくてもよい。

【0079】

次いで、図２３の工程では、図１４のレジスト膜３９を除去し、構造体の表面にＣＶＤ法により厚さ５～５０ｎｍのシリコン酸化膜（図示せず）を形成する。具体的には、例えば熱ＣＶＤ法により、原料ガスとして、ＢＴＢＡＳ（Bis(Tertiary-butylamino)Silane、$C_8H_{22}N_2Si$）ガスとO_2ガスを用いて、圧力０．１Ｐａ～１０００Ｐａ、基板温度を５００℃～５８０℃に設定し、シリコン酸化膜を形成する。

【0080】

図２３の工程では、さらに、ＲＩＥ法によりシリコン酸化膜をシリコン基板１１の表面が露出するまでエッチング（エッチバック）し、ｐ－ＭＯＳ領域３０ａおよびｎ－ＭＯＳ領域３０ｂのゲート積層体１８の両側面を覆う薄い第４側壁絶縁膜６０が形成される。具体的には、ＲＩＥ法のエッチングガスとしては、例えば、ジフルオロメタン（CH_2F_2）、１，１－ジフルオロエタン（$C_2H_4F_2$）等のハイドロフルオロカーボンを用いる。

【0081】

次いで、図２４の工程では、図２３の構造体を覆うように、レジスト膜６１を形成し、フォトリソグラフィ法によりレジスト膜６１のｐ－ＭＯＳ領域３０ａに開口部を形成し、イオン注入法により、ｐ－ＭＯＳ領域３０ａにゲート積層体１８および第４側壁絶縁膜６０をマスクとして、第４側壁絶縁膜６０の両側のシリコン基板１１にｐ型不純物を注入して、ＳｉＧｅ膜からなる圧縮応力印加部２０の底の少し深い位置まで少し深い接合領域６２ａを形成する。具体的には、ｐ型不純物としては、例えばB^+を用い、加速エネルギーを６ｋｅＶ、ドーズ量を$2\times10^{15}\ cm^{-2}$とする。次いで、レジスト膜６１を除去する

。

【0082】

次いで、図２５の工程では、ｐ－ＭＯＳ領域３０ａと略同様にして、レジスト膜６３を形成し、フォトリソグラフィ法によりレジスト膜６３のｎ－ＭＯＳ領域３０ｂを開口部４１－１を形成し、イオン注入法により、ゲート積層体１８および第４側壁絶縁膜６０をマスクとして、第４側壁絶縁膜６０の両側のシリコン基板１１にｎ型不純物を注入して少し深い接合領域２４ｂを形成する。具体的には、ｎ型不純物としては例えばAs^+またはP^+を用い、加速エネルギーを７ｋｅＶ、ドーズ量を2×10^{15}ｃｍ$^{-2}$とする。次いで、レジスト膜６３を除去する。

【0083】

次いで、図２６の工程では、構造体の表面にＣＶＤ法により厚さ３０～１００ｎｍのシリコン酸化膜（図示せず）を形成する。具体的には、例えば熱ＣＶＤ法により、原料ガスとして、ＢＴＢＡＳ（Bis(Tertiary-butylamino)Silane、$C_8H_{22}N_2Si$）ガスとO_2ガスを用いて、圧力０．１Ｐａ～１０００Ｐａ、基板温度を５００℃～５８０℃に設定し、シリコン酸化膜を形成する。

【0084】

図２６の工程では、さらに、ＲＩＥ法によりシリコン酸化膜をシリコン基板１１の表面が露出するまでエッチング（エッチバック）し、ｐ－ＭＯＳ領域３０ａおよびｎ－ＭＯＳ領域３０ｂのゲート積層体１８の両側面を覆う薄い第４側壁絶縁膜６０の両側面を更に覆う第５側壁絶縁膜６４が形成される。具体的には、ＲＩＥ法のエッチングガスとしては、例えば、ジフルオロメタン（CH_2F_2）、１，１－ジフルオロエタン（$C_2H_4F_2$）等のハイドロフルオロカーボンを用いる。

【0085】

次いで、図２７の工程では、図２６の構造体を覆うように、レジスト膜６５を形成し、フォトリソグラフィ法によりレジスト膜６５のｐ－ＭＯＳ領域３０ａに開口部を形成し、イオン注入法により、ｐ－ＭＯＳ領域３０ａにゲート積層体１８、第４側壁絶縁膜６０および第５側壁絶縁膜６４をマスクとして、第５側壁絶縁膜６４の両側のシリコン基板１１にｐ型不純物を注入して、ＳｉＧｅ膜からなる圧縮応力印加部２０の底より深い位置まで深い接合領域６６ａを形成し、ソース／ドレイン領域２８ａとする。具体的には、ｐ型不純物としては、例えばB^+を用い、加速エネルギーを８ｋｅＶ、ドーズ量を5×10^{15}ｃｍ$^{-2}$とする。次いで、レジスト膜６１を除去する。

【0086】

次いで、図２８の工程では、ｐ－ＭＯＳ領域３０ａと略同様にして、レジスト膜６６を形成し、フォトリソグラフィ法によりレジスト膜６６のｎ－ＭＯＳ領域３０ｂを開口部４１－１を形成し、イオン注入法により、ゲート積層体１８、第４側壁絶縁膜６０および第５側壁絶縁膜６４をマスクとして、第５側壁絶縁膜６４の両側のシリコン基板１１にｎ型不純物を注入して深い接合領域６６ｂを形成し、ソース／ドレイン領域２８ｂとする。具体的には、ｎ型不純物としては例えばAs^+またはP^+を用い、加速エネルギーを６ｋｅＶ、ドーズ量を1×10^{16}ｃｍ$^{-2}$とする。次いで、レジスト膜６６を除去する。

【0087】

次いで、図２９の工程では、図２８の工程の構造体４１のレジスト膜６６を除去し、次いで、ＲＴＡ（Rapid Thermal Annealing）法により熱処理を行い、浅い接合領域２２ａ，２２ｂ、少し深い接合領域６２ａ、６２ｂ、深い接合領域６６ａ，６６ｂの不純物を活性化する。これにより、浅い接合領域２２ａ，２２ｂと、少し深い接合領域６２ａ、６２ｂにより、2段の浅い接合領域を有するｐ－ＭＯＳトランジスタ１３ａとｎ－ＭＯＳトランジスタ１３ｂが形成される。

【0088】

図２９の工程ではさらに、構造体の表面を覆うように、例えば厚さ５ｎｍのＮｉ膜、Ｔｉ膜、あるいはＣｏ膜を形成し、加熱処理を行ってシリサイド化し、ソース／ドレイン領域２８ａ，２８ｂのシリコン基板１１の表面、およびゲート電極１６の表面に$NiSi_2$

膜、ＴｉＳｉ$_2$膜、ＣｏＳｉ$_2$膜などのシリサイド膜２６を形成する。次いで、シリサイド化しなかったＮｉ膜、Ｔｉ膜、あるいはＣｏ膜を除去する。

【0089】

（実施例）

本発明の第１の実施の形態に係る半導体装置の製造方法によりｐ－ＭＯＳトランジスタ１３ａとｎ－ＭＯＳトランジスタ１３ｂを有する半導体装置（以下「実施例」という）を製造した。

【0090】

比較のために、ｐ－ＭＯＳトランジスタ１３ａにＳｉＧｅからなる圧縮応力印加部２０を形成しない点以外は、第１の実施の形態と同じ半導体装置の製造方法によりｐ－ＭＯＳトランジスタ１３ａとｎ－ＭＯＳトランジスタ１３ｂを有する半導体装置（以下「比較例」という）を製造した。

【0091】

これら実施例および比較例について様々な電気的特性を測定した。その測定結果を図３０乃至図３２に示す。図３０乃至図３２において、●は各実施例の測定点であり、○は各比較例の測定点である。

【0092】

図３０は、各実施例および各比較例におけるｐ－ＭＯＳトランジスタのターンオン電流（Ｉon）とターンオフ電流（Ｉoff）の関係を示すグラフである。各実施例の測定点を●で示し、比較例の測定点を○で示す。

【0093】

図３０において、ターンオフ電流（Ｉoff）が約7Ｅ－８［ｎＡ／μｍ］であるｐ－ＭＯＳトランジスタのターンオン電流を比較すると、比較例(○)は約０．３５［ｍＡ／μｍ］であるのに対し、実施例(●)は約０．４６［ｍＡ／μｍ］となり、本発明により約３１％改善されたことがわかった。

【0094】

図３１は、各実施例および各比較例におけるｐ－ＭＯＳトランジスタのゲート長Ｌｇ（ＳＥＭ）［ｎｍ］と閾値Ｖｔｈ［Ｖ］の関係を示すグラフである。各実施例の測定点を●で示し、比較例の測定点を○で示す。

【0095】

実施例(●)の場合には、圧縮応力印加部２０であるＳｉＧｅ膜を形成するために、減圧熱ＣＶＤ法により基板温度を５００℃～８００℃とする高温処理（図１０の工程を参照）が必要である。これに対し、比較例(○)ではそのような高温処理を必要としない。

【0096】

図３１からわかるように実施例と比較例とでは有意な相違がなく、ＳｉＧｅ膜を形成するための高温処理がｐ－ＭＯＳトランジスタの閾値特性を劣化させていないことがわかる。

【0097】

図３２は、各実施例および各比較例におけるｐ－ＭＯＳトランジスタのゲート電圧Ｖｇ［Ｖ］と、Ｖｄｄが０．０２Ｖの際の相互コンダクタンスＧｍ［ｍＳ／ｍｍ］の関係を示すグラフである。各実施例の測定点を●で示し、比較例の測定点を○で示す。

【0098】

図３２において、ゲート電圧が－１．０［Ｖ］であるｐ－ＭＯＳトランジスタの相互コンダクタンスを比較すると、比較例(○)は約５６０［ｍＳ／ｍｍ］であるのに対し、実施例(●)は約８００［ｍＳ／ｍｍ］となり、本発明により約４３％改善されたことがわかった。

【0099】

（変形の実施の形態）

以上本発明の好ましい実施の形態について詳述したが、本発明は係る特定の実施の形態に限定されるものではなく、特許請求の範囲に記載された本発明の範囲内において、種々

の変形・変更が可能である。

【0100】

例えば、上記実施の形態においてはＭＯＳトランジスタを例に説明したが、ＭＩＳトランジスタにも本発明の製造方法を適用できることはいうまでもない。例えば、上述したように、ゲート絶縁膜のシリコン酸化膜の代わりに、シリコン酸窒化膜、シリコン窒化膜を用いてもよく、ｈｉｇｈ－ｋ材料、例えば、Al_2O_3、Ta_2O_3、HfO_2、ZrO_2、ペロブスカイト結晶構造を有する金属酸化物、例えば$PbTiO_3$、$BaTiO_3$、Ｐｂ（Ｚｒ，Ｔｉ）O_3等を用いてもよい。

【0101】

以上詳述したように、本発明の特徴をまとめると以下の通りとなる。

（付記１）

半導体基板の第１の領域に形成されたｐ型トランジスタと、該半導体基板の第２の領域に形成されたｎ型トランジスタからなる半導体装置の製造方法であって、

前記半導体基板上にゲート絶縁膜およびゲート電極からなるゲート積層体を形成する工程と、

前記第１の領域において、前記ゲート積層体の両側面に第１の側壁絶縁膜および第２の側壁絶縁膜を形成する工程と、

前記第２の領域の半導体基板表面を耐エッチング膜により覆った状態で、前記第１の領域において第１の側壁絶縁膜および第２の側壁絶縁膜をマスクとして、該第２の側壁絶縁膜の外側の半導体基板に溝部を形成する工程と、

前記溝部に圧縮応力印加部を形成する工程と、

前記第１の領域において第１の側壁絶縁膜および第２の側壁絶縁膜を除去すると共に、前記第２の領域において耐エッチング膜を除去する工程と、

前記ゲート積層体をマスクとして、前記第１の領域および前記第２の領域に第１の接合領域を形成する工程と、

前記ゲート積層体の両側面に第３の側壁絶縁膜を形成し、前記ゲート積層体および第３の側壁絶縁膜をマスクとして、前記第１の領域および前記第２の領域に第２の接合領域を形成する工程と、

を備えることを特徴とする半導体装置の製造方法。

（付記２）

前記第１の側壁絶縁膜および第２の側壁絶縁膜を形成する工程は、

前記半導体基板の表面およびゲート積層体を覆う第１の絶縁膜および第２の絶縁膜を順次形成する工程と、

前記第１の領域において第１の絶縁膜および第２の絶縁膜を異方性エッチングする工程からなり、

前記溝部を形成する工程は、前記第２の領域の耐エッチング膜が第２の絶縁膜であることを特徴とする付記１記載の半導体装置の製造方法。

（付記３）

前記溝部を形成する工程は、前記第２の領域を覆うレジスト膜であることを特徴とする付記１記載の半導体装置の製造方法。

（付記４）

半導体基板の第１の領域に形成されたｐ型トランジスタと、該半導体基板の第２の領域に形成されたｎ型トランジスタからなる半導体装置の製造方法であって、

半導体基板上にゲート絶縁膜およびゲート電極からなるゲート積層体を形成する工程と、

前記ゲート積層体の両側面に第１の側壁絶縁膜および第２の側壁絶縁膜を形成すると共に、該第２の側壁絶縁膜の外側の半導体基板表面を露出する工程と、

前記第２の領域を覆うレジスト膜を形成する工程と、

CF_4ガスおよびO_2 ガスを電離すると共に照射して前記第１の領域の半導体基板表面を改質する第１の表面処理工程と、

O_2 ガスを電離すると共に照射して第２の領域においてレジスト膜を除去すると共に、第２の側壁絶縁膜の外側に露出する半導体基板表面に酸化膜を形成する第２の表面処理工程と、

前記第１の領域の半導体基板表面を露出する工程と、

前記第１の領域の第１の側壁絶縁膜、第２の側壁絶縁膜、および第２の領域の酸化膜をマスクとして、第２の側壁絶縁膜の外側の半導体基板に溝部を形成する工程と、

前記溝部に圧縮応力印加部を形成する工程と、

前記第１の領域において第１の側壁絶縁膜および第２の側壁絶縁膜を除去すると共に、前記第２の領域において耐エッチング膜を除去する工程と、

前記ゲート積層体をマスクとして、前記第１の領域および前記第２の領域に第１の接合領域を形成する工程と、

前記ゲート積層体の両側面に第３の側壁絶縁膜を形成し、前記ゲート積層体および第３の側壁絶縁膜をマスクとして、前記第１の領域および前記第２の領域に第２の接合領域を形成する工程と、

を備えることを特徴とする半導体装置の製造方法。

（付記５）

第１の領域および第２の領域に第１の接合領域を形成する工程の後、第２の接合領域を形成する工程する前に、

前記ゲート積層体の両側面に前記第３の側壁絶縁膜より薄い第４の側壁絶縁膜を形成し、前記ゲート積層体および第４の側壁絶縁膜をマスクとして、前記第１の領域および前記第２の領域に前記第１の接合領域より深く前記第２の接合領域より浅い第３の接合領域を形成する工程を更に有し、

第１の領域および第２の領域に第２の接合領域を形成する工程は、

前記ゲート積層体および前記第４の側壁絶縁膜の両側面に前記第３の側壁絶縁膜を形成し、前記ゲート積層体、前記第４の側壁絶縁膜および前記第３の側壁絶縁膜をマスクとして、前記第１の領域および前記第２の領域に前記第２の接合領域を形成する

を備えることを特徴とする半導体装置の製造方法。

（付記６）

前記溝部を形成する工程は、

第２の側壁絶縁膜の外側の半導体基板を異方性エッチングを行う処理と、

等方性エッチングを行う処理からなる

ことを特徴とする付記１乃至５のいずれか１項に記載の半導体装置の製造方法。

（付記７）

前記等方性エッチングは、塩化水素ガスあるいは塩素ガスを用いたケミカルドライエッチングであることを特徴とする付記６記載の半導体装置の製造方法。

（付記８）

前記溝部は、その端部とゲート積層体の端部との距離を５ｎｍ～８０ｎｍの範囲に設定することを特徴とする付記６記載の半導体装置の製造方法。

（付記９）

前記圧縮応力印加部を形成する工程は、前記溝部に半導体基板を構成する半導体の格子定数よりも大きな半導体材料をエピタキシャル成長させることを特徴とする付記１乃至８のいずれか１項に記載の半導体装置の製造方法。

（付記１０）

前記ゲート積層体を形成する工程の後に、該ゲート積層体上にキャップ層を形成する工程をさらに備え、

前記溝部を形成する工程は、キャップ層をゲート積層体のマスクとすることを特徴とする付記１乃至９のいずれか１項に記載の半導体装置の製造方法。

（付記１１）

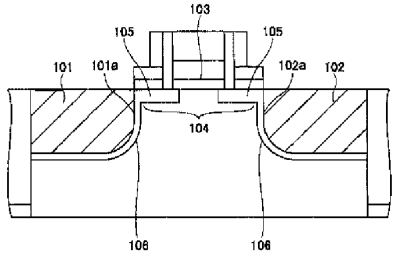
前記圧縮応力印加部を形成する工程は、前記キャップ層をゲート積層体のマスクとすることを特徴とする付記１０記載の半導体装置の製造方法。

（付記１２）
　前記半導体基板がシリコン基板であり、前記圧縮応力印加部がＳｉＧｅ膜あるいはＳｉＧｅＣ膜からなることを特徴とする付記１乃至１１のいずれか１項に記載の半導体装置の製造方法。
【図面の簡単な説明】
【0102】
【図1】従来のｐ－ＭＯＳトランジスタの断面図である。
【図2】本発明の第１の実施の形態に係る半導体装置の製造方法により形成される半導体装置の断面図である。
【図3】本発明の第１の実施の形態に係る半導体装置の製造工程図（その１）である。
【図4】本発明の第１の実施の形態に係る半導体装置の製造工程図（その２）である。
【図5】本発明の第１の実施の形態に係る半導体装置の製造工程図（その３）である。
【図6】本発明の第１の実施の形態に係る半導体装置の製造工程図（その４）である。
【図7】本発明の第１の実施の形態に係る半導体装置の製造工程図（その５）である。
【図8】本発明の第１の実施の形態に係る半導体装置の製造工程図（その６）である。
【図9】本発明の第１の実施の形態に係る半導体装置の製造工程図（その７）である。
【図10】本発明の第１の実施の形態に係る半導体装置の製造工程図（その８）である。
【図11】本発明の第１の実施の形態に係る半導体装置の製造工程図（その９）である。
【図12】本発明の第１の実施の形態に係る半導体装置の製造工程図（その１０）である。
【図13】本発明の第１の実施の形態に係る半導体装置の製造工程図（その１１）である。
【図14】本発明の第１の実施の形態に係る半導体装置の製造工程図（その１２）である。
【図15】本発明の第１の実施の形態に係る半導体装置の製造工程図（その１３）である。
【図16】本発明の第１の実施の形態に係る半導体装置の製造工程図（その１４）である。
【図17】本発明の第１の実施の形態に係る半導体装置の製造工程図（その１５）である。
【図18】本発明の第２の実施の形態に係る半導体装置の製造工程図（その１）である。
【図19】本発明の第２の実施の形態に係る半導体装置の製造工程図（その２）である。
【図20】本発明の第２の実施の形態に係る半導体装置の製造工程図（その３）である。
【図21】本発明の第２の実施の形態に係る半導体装置の製造工程図（その４）である。
【図22】本発明の第２の実施の形態に係る半導体装置の製造工程図（その５）である。
【図23】本発明の第３の実施の形態に係る半導体装置の製造工程図（その１）である。
【図24】本発明の第３の実施の形態に係る半導体装置の製造工程図（その２）である。
【図25】本発明の第３の実施の形態に係る半導体装置の製造工程図（その３）である。
【図26】本発明の第３の実施の形態に係る半導体装置の製造工程図（その４）である。
【図27】本発明の第３の実施の形態に係る半導体装置の製造工程図（その５）である。
【図28】本発明の第３の実施の形態に係る半導体装置の製造工程図（その６）である。
【図29】本発明の第３の実施の形態に係る半導体装置の製造工程図（その７）である。
【図30】実施例および比較例におけるｐ－ＭＯＳトランジスタのターンオン電流とターンオフ電流の関係を示すグラフである。
【図31】実施例および比較例におけるｐ－ＭＯＳトランジスタのゲート長と閾値の関係を示すグラフである。
【図32】実施例および比較例におけるｐ－ＭＯＳトランジスタのゲート電圧と相互コンダクタンスの関係を示すグラフである。
【符号の説明】
【0103】
　１０…半導体装置
　１１…シリコン基板
　１１－１、１１－２…溝部
　１２…素子分離領域
　１３ａ…ｐ－ＭＯＳトランジスタ
　１３ｂ…ｎ－ＭＯＳトランジスタ

１５、１５－１…ゲート絶縁膜
１６…ゲート電極
１６－１…ゲート電極膜
１８…ゲート積層体
１９…第３側壁絶縁膜
２０…圧縮応力印加部
２１…圧縮歪み誘起部
２２ａ，２２ｂ…浅い接合領域
２３ａ，２３ｂ…ポケット領域
２４ａ，２４ｂ…深い接合領域
２６…シリサイド膜
２８ａ，２８ｂ…ソース／ドレイン領域
３０ａ…ｐ－ＭＯＳ領域
３０ｂ…ｎ－ＭＯＳ領域
３１－１…トレンチ
３２ａ…ｎ型ウェル領域
３２ｂ…ｐ型ウェル領域
３３…キャップ層
３３－１，３５－１…シリコン窒化膜
３４…第１側壁絶縁膜
３４－１…シリコン酸化膜
３５…第２側壁絶縁膜
３６，３８，３９，４１，５１，５１－１…レジスト膜
５２，５２－１…アッシング改質膜
５３…シリコン酸化膜
６０…第４側壁絶縁膜
６１、６３、６５、６６…レジスト膜
６２ａ、６２ｂ…少し深い浅い接合領域
６４…第５側壁絶縁膜
６６ａ、６６ｂ…深い接合領域

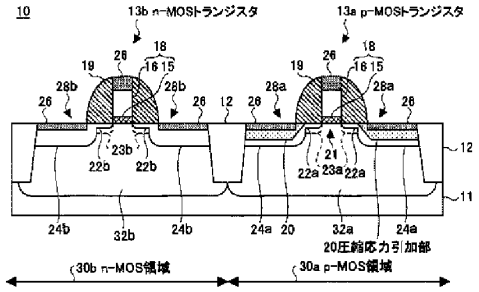
【図1】

従来のp－MOSトランジスタの断面図



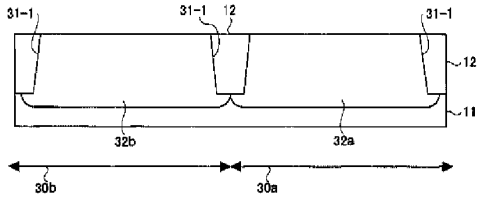
【図2】

本発明の第１の実施の形態に係る
半導体装置の製造方法により形成される半導体装置の断面図



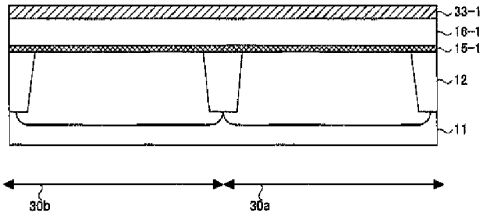
【図3】

本発明の第１の実施の形態に係る半導体装置の製造工程図（その１）



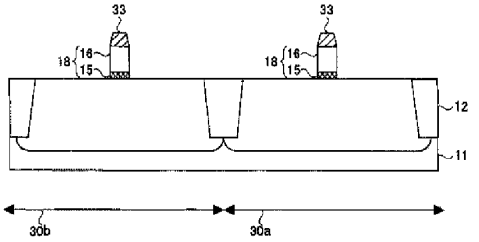
【図4】

第１の実施の形態に係る半導体装置の製造工程図（その２）



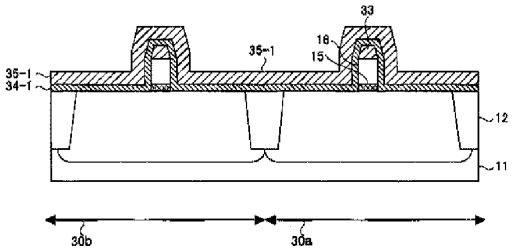
【図5】

第１の実施の形態に係る半導体装置の製造工程図（その３）



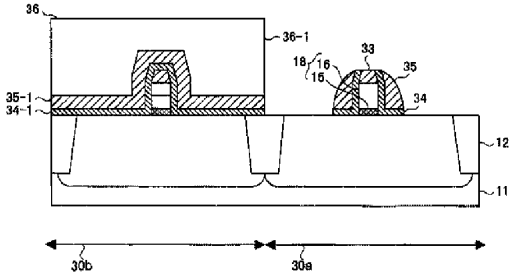
【図6】

第１の実施の形態に係る半導体装置の製造工程図（その４）



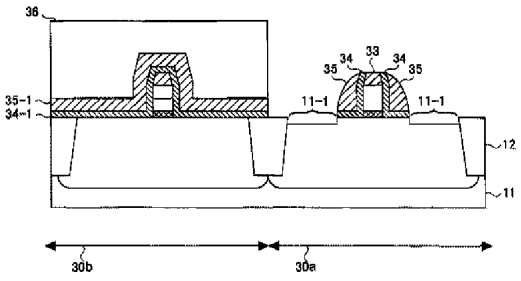
【図7】

第１の実施の形態に係る半導体装置の製造工程図（その５）



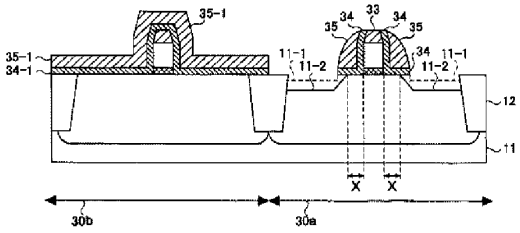
【図8】

第１の実施の形態に係る半導体装置の製造工程図（その６）



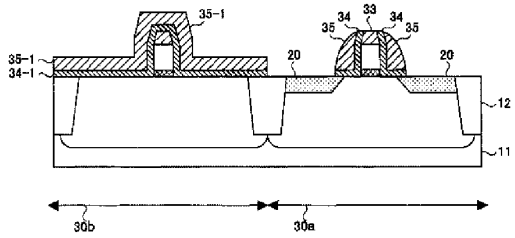
【図9】

第1の実施の形態に係る半導体装置の製造工程図(その7)



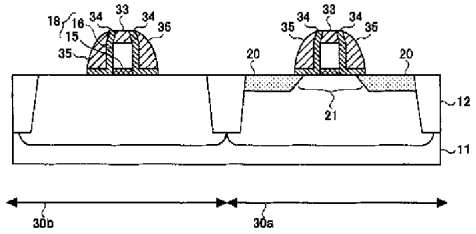
【図10】

第1の実施の形態に係る半導体装置の製造工程図(その8)



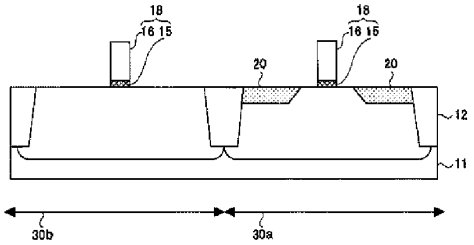
【図11】

第1の実施の形態に係る半導体装置の製造工程図(その9)



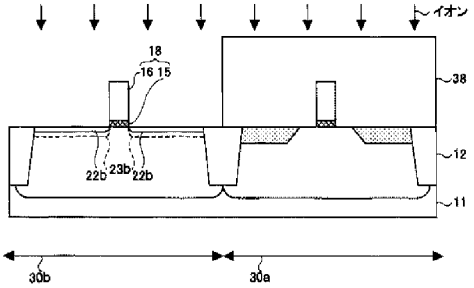
【図12】

第1の実施の形態に係る半導体装置の製造工程図(その10)



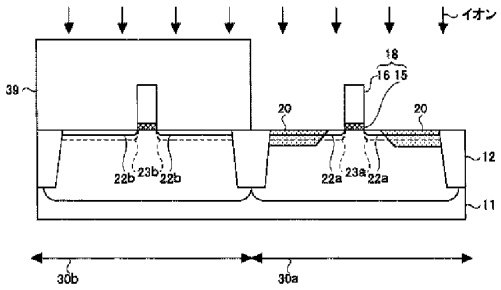
【図13】

第1の実施の形態に係る半導体装置の製造工程図(その11)



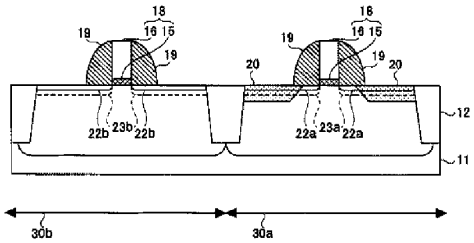
【図14】

第1の実施の形態に係る半導体装置の製造工程図(その12)



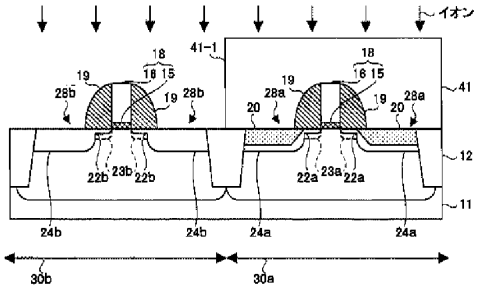
【図15】

第1の実施の形態に係る半導体装置の製造工程図(その13)



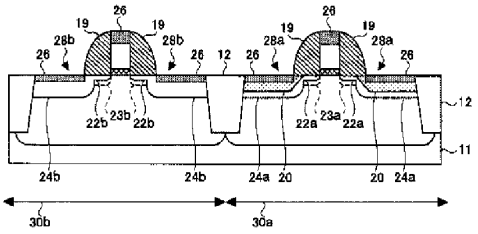
【図16】

第1の実施の形態に係る半導体装置の製造工程図(その14)



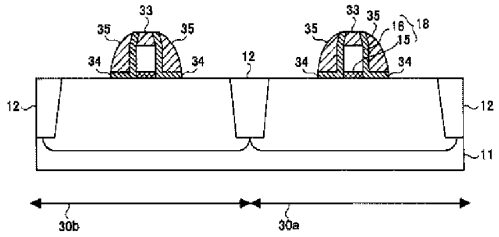
【図17】

第１の実施の形態に係る半導体装置の製造工程図（その１５）



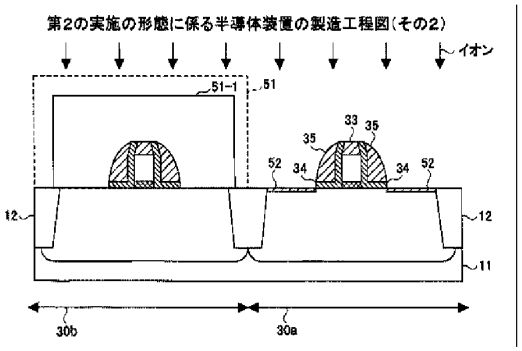
【図18】

本発明の第２の実施の形態に係る半導体装置の製造工程図（その１）



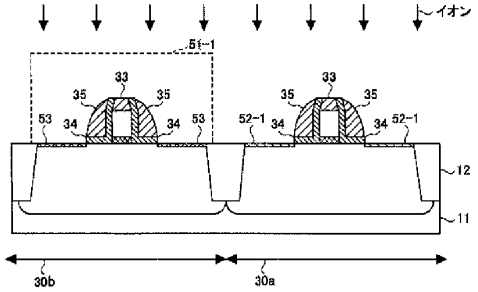
【図19】

第２の実施の形態に係る半導体装置の製造工程図（その２）



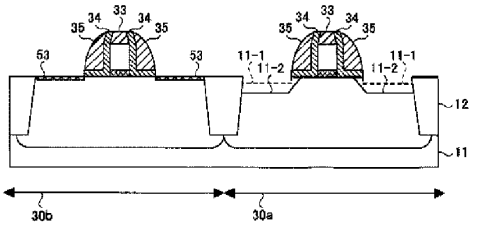
【図20】

第２の実施の形態に係る半導体装置の製造工程図（その３）



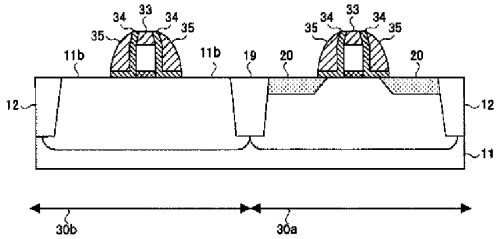
【図21】

第２の実施の形態に係る半導体装置の製造工程図（その４）



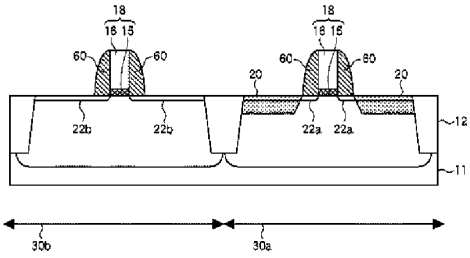
【図22】

第２の実施の形態に係る半導体装置の製造工程図（その５）



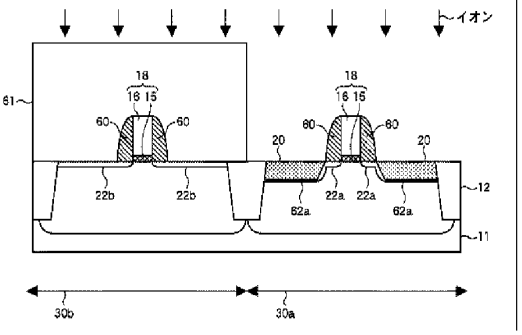
【図23】

本発明の第３の実施の形態に係る半導体装置の製造工程図（その１）



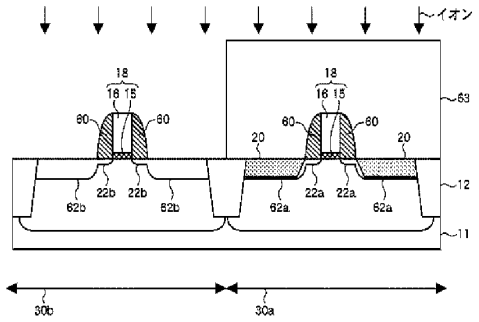
【図24】

本発明の第３の実施の形態に係る半導体装置の製造工程図（その２）



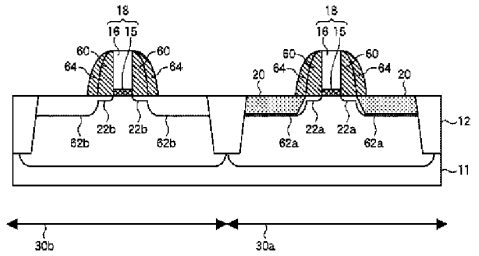
【図25】

本発明の第3の実施の形態に係る半導体装置の製造工程図(その3)



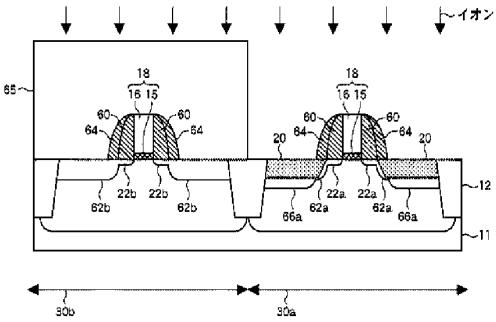
【図26】

本発明の第3の実施の形態に係る半導体装置の製造工程図(その4)



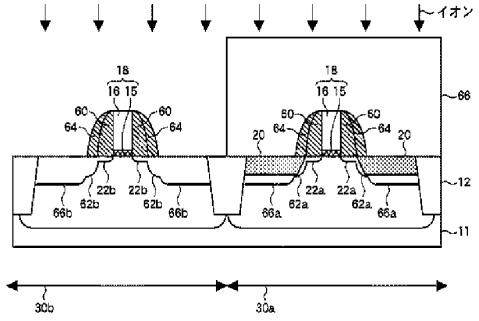
【図27】

本発明の第3の実施の形態に係る半導体装置の製造工程図(その5)



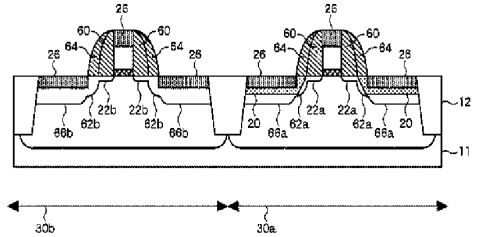
【図28】

本発明の第3の実施の形態に係る半導体装置の製造工程図(その6)



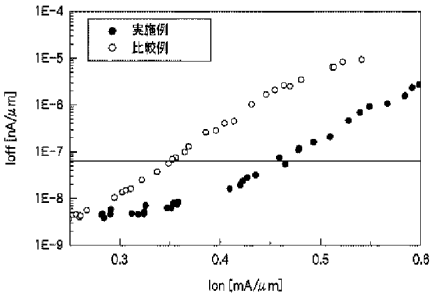
【図29】

本発明の第3の実施の形態に係る半導体装置の製造工程図(その7)



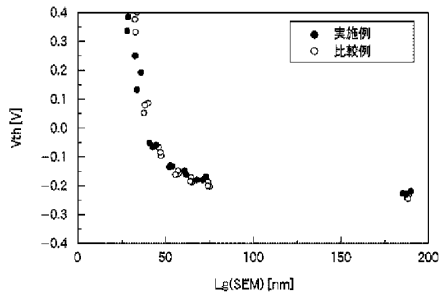
【図30】

p-MOSトランジスタのターンオン電流とターンオフ電流の関係を示すグラフ



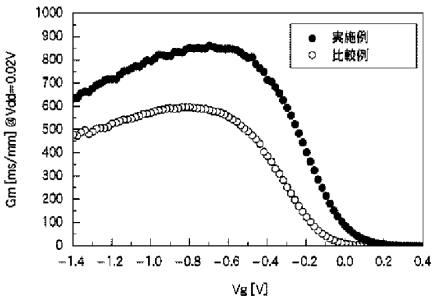
【図31】

p-MOSトランジスタのゲート長と閾値の関係を示すグラフ



【図32】

p-MOSトランジスタのゲート電圧と相互コンダクタンスの関係を示すグラフ



Ｆターム(参考)	5F048	AC03	BA01	BA16	BA19	BB05	BB08	BC06	BC15	BC18	BE03
		BF06	BF16	BG13	DA25	DA27	DA30				
	5F110	AA01	BB04	CC02	EE05	EE09	EE14	EE32	EE45	FF01	FF02
		FF03	FF04	FF09	FF23	FF28	FF29	GG28	GG32	GG52	HJ01
		HJ04	HJ06	HJ13	HJ14	HJ23	HK05	HK08	HK32	HK41	HM02
		NN65	QQ08	QQ11							
	5F140	AA01	AB03	AC01	AC28	AC36	BA01	BC06	BD01	BD06	BD07
		BD09	BD11	BD12	BD13	BE03	BE07	BE09	BE10	BF04	BF11
		BF18	BG08	BG09	BG12	BG28	BG34	BG38	BG52	BG53	BG54
		BH06	BH14	BH21	BH27	BH35	BJ01	BJ08	BK02	BK08	BK09
		BK10	BK13	BK14	BK18	BK21	BK34	CB04	CF04		