semiconductor material layer comprising the having a third concentration level of a doping material, the third concentration level of the doping material being higher than the second concentration level of the doping material;

A method of forming a semiconductor device.

11.

The method of claim 10,

wherein the doping material is one or more of the group V elements.

12.

The method of claim 11,

wherein the doping material is boron, and the first concentration level of the doping material is from about 5e19 atoms/cm3 to about 2e20 atoms/cm3.

13.

12. The method of claim 11,

wherein the second concentration level of the doping material is from about 2e20 atoms/cm3 to about 5e20 atoms/cm3.

14.

12. The method of claim 11,

wherein the third concentration level of the doping material is in a range from about 5e20 atoms/cm3 to 1e21 atoms/cm3.

15.

a first layer of semiconductor material in the recess of the source region and a second layer of semiconductor material in the recess of the drain region, each of the first and second semiconductor material layers having an atomic concentration of the first element and a second layer of semiconductor material formed using a stressor material having a first ratio between the atomic concentrations of the two elements and having a first concentration level of a doping material, wherein the first element is silicon;

a third layer of semiconductor material overlying the first layer of semiconductor material, and a fourth layer of semiconducting material overlying the second layer of semiconducting material, each of the third layer of semiconductor material and the fourth layer of semiconductor material being an atom of the first element a second ratio between a concentration and an atomic concentration of the second element, wherein the second ratio is higher than the first ratio, and wherein each of the third semiconductor material layer and the fourth semiconductor material layer has a second concentration of the doping material. level, wherein the second concentration level of the doping material is higher than the first concentration level of the doping material; and

a fifth layer of semiconductor material overlying the third layer of semiconductor material, and a sixth layer of semiconducting material overlying the fourth layer of semiconductor material, each of the fifth layer of semiconductor material and the sixth layer of semiconducting material being an atom of the first element a third ratio between the concentration and the atomic concentration of the second element, wherein the third ratio is lower than the second ratio, each of the fifth semiconductor material layer and the sixth semiconductor material layer having a third concentration of the doping material level, wherein the third concentration level of the doping material is higher than the second concentration level of the doping material;

semiconductor device.

16.

The method of claim 15,

The stressor material is an alloy of silicon and germanium, and the second element is germanium.

17.

16. The method of claim 15,

The doping material is one or more of the group V elements.

18.

The method of claim 17,

A first ratio between the atomic concentration of the first element and the atomic concentration of the second element is about 2.3:1.

19.

18. The method of claim 17,

the doping material is boron, the first concentration level of the doping material is from about 5e19 atoms/cm3 to about 2e20 atoms/cm3, and the second concentration level of the doping material is from about 2e20 atoms/cm3 to 5e20 atoms/cm3 and the third concentration level of the doping material is in a range from about 5e20 atoms/cm3 to 1e21 atoms/cm3.

20.

18. The method of claim 17,

and a second ratio between the atomic concentration of the first element and the atomic concentration of the second element is about 3.0:1.

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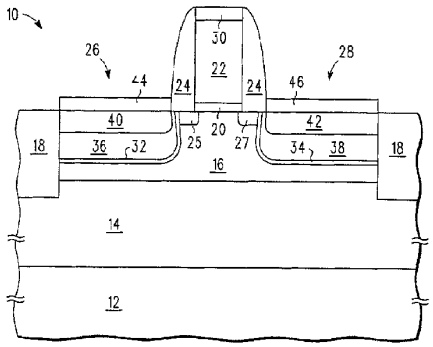
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(57) 요 약

반도체 디바이스(10)를 형성하는 방법은, 반도체 디바이스의 소스 영역에 리세스(26)를 형성하고 드레인 영역에 리세스(28)를 형성하는 단계를 포함한다. 이 방법은 또한 소스 영역에서의 리세스(26)에 제1 반도체 물질층(32)을 형성하고 드레인 영역에서의 리세스(28)에 제2 반도체 물질층(34)을 형성하는 단계를 포함하며, 제1 반도체 물질층(32)과 제2 반도체 물질층(34) 각각은 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제1 비율을 갖고 도핑 물질의 제1 농도 레벨을 가지는 스트레서 물질을 이용하여 형성되고, 제1 엘리먼트는 실리콘이다. 이 방법은 또한 제1 엘리먼트와 제2 엘리먼트의 상이한 원자 농도 간의 비율을 갖게 하는 식으로 제1 반도체 물질층(32)과 제2 반도체 물질층(34) 위에 깔리는 추가의 반도체 물질층들(36, 38, 40, 42)을 형성하는 단계를 포함한다.

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특허청구의 범위

청구항 1

반도체 디바이스를 형성하는 방법으로서,

상기 반도체 디바이스의 소스 영역에 리세스(recess)를 형성하고 드레인 영역에 리세스를 형성하는 단계;

상기 소스 영역에서의 리세스에 제1 반도체 물질층(semiconductor material layer)을 형성하고 상기 드레인 영역에서의 리세스에 제2 반도체 물질층을 형성하는 단계 - 상기 제1 반도체 물질층과 상기 제2 반도체 물질층 각각은 제1 엘리먼트의 원자 농도(atomic concentration)와 제2 엘리먼트의 원자 농도 간의 제1 비율을 갖고 도핑 물질의 제1 농도 레벨(a first level of concentration of a doping material)을 갖는 스트레서 물질(stressor material)을 이용하여 형성되고, 상기 제1 엘리먼트는 실리콘일 - ;

상기 제1 반도체 물질층 위에 깔리는 제3 반도체 물질층을 형성하고 상기 제2 반도체 물질층 위에 깔리는 제4 반도체 물질층을 형성하는 단계 - 상기 제3 반도체 물질층과 상기 제4 반도체 물질층 각각은 상기 제1 엘리먼트의 원자 농도와 상기 제2 엘리먼트의 원자 농도 간의 제2 비율을 가지고, 상기 제2 비율은 상기 제1 비율보다 높고, 상기 제3 반도체 물질층과 상기 제4 반도체 물질층 각각은 상기 도핑 물질의 제2 농도 레벨을 가지고, 상기 도핑 물질의 제2 농도 레벨은 상기 도핑 물질의 제1 농도 레벨보다 높음 - ; 및

상기 제3 반도체 물질층 위에 깔리는 제5 반도체 물질층을 형성하고 상기 제4 반도체 물질층 위에 깔리는 제6 반도체 물질층을 형성하는 단계 - 상기 제5 반도체 물질층과 상기 제6 반도체 물질층 각각은 상기 제1 엘리먼트의 원자 농도와 상기 제2 엘리먼트의 원자 농도 간의 제3 비율을 가지고, 상기 제3 비율은 상기 제2 비율보다 낮고, 상기 제5 반도체 물질층과 상기 제6 반도체 물질층 각각은 상기 도핑 물질의 제3 농도 레벨을 가지고, 상기 도핑 물질의 제3 농도 레벨은 상기 도핑 물질의 제2 농도 레벨보다 높음 - 를 포함하는

반도체 디바이스의 형성 방법.

청구항 2

제1항에 있어서,

상기 스트레서 물질은 실리콘과 게르마늄의 합금이고, 상기 제2 엘리먼트는 게르마늄인 반도체 디바이스의 형성 방법.

청구항 3

제1항에 있어서,

상기 도핑 물질은 V족 엘리먼트(a group V element) 중 하나 또는 그 이상인 반도체 디바이스의 형성 방법.

청구항 4

제3항에 있어서,

상기 제1 엘리먼트의 원자 농도와 상기 제2 엘리먼트의 원자 농도 간의 제1 비율은 약 2.3:1인 반도체 디바이스의 형성 방법.

청구항 5

제3항에 있어서,

상기 도핑 물질은 붕소이고, 상기 도핑 물질의 제1 농도 레벨은 약 5e19 atoms/cm^3으로부터 약 2e20 atoms/cm^3까지인 반도체 디바이스의 형성 방법.

청구항 6

제3항에 있어서,

상기 제1 엘리먼트의 원자 농도와 상기 제2 엘리먼트의 원자 농도 간의 제2 비율은 약 3.0:1인 반도체 디바이스의 형성 방법.

청구항 7

제3항에 있어서,

상기 도핑 물질은 붕소이고, 상기 도핑 물질의 제2 농도 레벨은 약 2e20 atoms/cm^3으로부터 5e20 atoms/cm^3까지인 반도체 디바이스의 형성 방법.

청구항 8

제3항에 있어서,

상기 제1 엘리먼트의 원자 농도와 상기 제2 엘리먼트의 원자 농도 간의 제3 비율은 약 2.3:1인 반도체 디바이스의 형성 방법.

청구항 9

제3항에 있어서,

상기 도핑 물질은 붕소이고, 상기 도핑 물질의 제3 농도 레벨은 약 5e20 atoms/cm^3으로부터 1e21 atoms/cm^3까지의 범위 내인 반도체 디바이스의 형성 방법.

청구항 10

반도체 디바이스를 형성하는 방법으로서,

상기 반도체 디바이스의 소스 영역에 리세스를 형성하고 드레인 영역에 리세스를 형성하는 단계;

상기 소스 영역에서의 리세스에 제1 반도체 물질층을 형성하고 상기 드레인 영역에서의 리세스에 제2 반도체 물질층을 형성하는 단계 - 상기 제1 반도체 물질층과 상기 제2 반도체 물질층 각각은 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제1 비율을 갖는 스트레서 물질을 이용하여 형성되고, 상기 제1 엘리먼트는 실리콘이고, 상기 제1 반도체 물질층과 상기 제2 반도체 물질층 각각은 도핑 물질의 제1 농도 레벨을 가짐 - ;

상기 제1 반도체 물질층 위에 깔리는 제3 반도체 물질층을 형성하고 상기 제2 반도체 물질층 위에 깔리는 제4 반도체 물질층을 형성하는 단계 - 상기 제3 반도체 물질층과 상기 제4 반도체 물질층 각각은 상기 도핑 물질의 제2 농도 레벨을 가지고, 상기 도핑 물질의 제2 농도 레벨은 상기 도핑 물질의 제1 농도 레벨보다 높음 - ; 및

상기 제3 반도체 물질층 위에 깔리는 제5 반도체 물질층을 형성하고 상기 제4 반도체 물질층 위에 깔리는 제6 반도체 물질층을 형성하는 단계 - 상기 제5 반도체 물질층과 상기 제6 반도체 물질층 각각은 상기 도핑 물질의 제3 농도 레벨을 가지고, 상기 도핑 물질의 제3 농도 레벨은 상기 도핑 물질의 제2 농도 레벨보다 높음 - 를 포함하는

반도체 디바이스의 형성 방법.

청구항 11

제10항에 있어서,

상기 도핑 물질은 V족 엘리먼트 중 하나 또는 그 이상인 반도체 디바이스의 형성 방법.

청구항 12

제11항에 있어서,

상기 도핑 물질은 붕소이고, 상기 도핑 물질의 제1 농도 레벨은 약 5e19 atoms/cm^3으로부터 약 2e20 atoms/cm^3까지인 반도체 디바이스의 형성 방법.

청구항 13

제11항에 있어서,

상기 도핑 물질의 제2 농도 레벨은 약 2e20 atoms/cm^3으로부터 5e20 atoms/cm^3까지인 반도체 디바이스의 형성

방법.

청구항 14

제11항에 있어서,

상기 도핑 물질의 제3 농도 레벨은 약 5e20 atoms/cm^3으로부터 1e21 atoms/cm^3까지의 범위 내인 반도체 디바이스의 형성 방법.

청구항 15

소스 영역의 리세스에서의 제1 반도체 물질층과, 드레인 영역의 리세스에서의 제2 반도체 물질층 - 상기 제1 반도체 물질층과 상기 제2 반도체 물질층 각각은 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제1 비율을 가지며 도핑 물질의 제1 농도 레벨을 가지는 스트레서 물질을 이용하여 형성되고, 상기 제1 엘리먼트는 실리콘임 - ;

상기 제1 반도체 물질층 위에 깔리는 제3 반도체 물질층과, 상기 제2 반도체 물질층 위에 깔리는 제4 반도체 물질층 - 상기 제3 반도체 물질층과 상기 제4 반도체 물질층 각각은 상기 제1 엘리먼트의 원자 농도와 상기 제2 엘리먼트의 원자 농도 간의 제2 비율을 가지고, 상기 제2 비율은 상기 제1 비율보다 높고, 상기 제3 반도체 물질층과 상기 제4 반도체 물질층 각각은 상기 도핑 물질의 제2 농도 레벨을 가지고, 상기 도핑 물질의 제2 농도 레벨은 상기 도핑 물질의 제1 농도 레벨보다 높음 - ; 및

상기 제3 반도체 물질층 위에 깔리는 제5 반도체 물질층과, 상기 제4 반도체 물질층 위에 깔리는 제6 반도체 물질층 - 상기 제5 반도체 물질층과 상기 제6 반도체 물질층 각각은 상기 제1 엘리먼트의 원자 농도와 상기 제2 엘리먼트의 원자 농도 간의 제3 비율을 가지고, 상기 제3 비율은 상기 제2 비율보다 낮고, 상기 제5 반도체 물질층과 상기 제6 반도체 물질층 각각은 상기 도핑 물질의 제3 농도 레벨을 가지고, 상기 도핑 물질의 제3 농도 레벨은 상기 도핑 물질의 제2 농도 레벨보다 높음 - 을 포함하는

반도체 디바이스.

청구항 16

제15항에 있어서,

상기 스트레서 물질은 실리콘과 게르마늄의 합금이고, 상기 제2 엘리먼트는 게르마늄인 반도체 디바이스.

청구항 17

제15항에 있어서,

상기 도핑 물질은 V족 엘리먼트 중 하나 또는 그 이상인 반도체 디바이스.

청구항 18

제17항에 있어서,

상기 제1 엘리먼트의 원자 농도와 상기 제2 엘리먼트의 원자 농도 간의 제1 비율은 약 2.3:1인 반도체 디바이스.

청구항 19

제17항에 있어서,

상기 도핑 물질은 붕소이고, 상기 도핑 물질의 제1 농도 레벨은 약 5e19 atoms/cm^3으로부터 약 2e20 atoms/cm^3까지이고, 상기 도핑 물질의 제2 농도 레벨은 약 2e20 atoms/cm^3으로부터 5e20 atoms/cm^3까지이고, 상기 도핑 물질의 제3 농도 레벨은 약 5e20 atoms/cm^3으로부터 1e21 atoms/cm^3까지의 범위 내인 반도체 디바이스.

청구항 20

제17항에 있어서,

상기 제1 엘리먼트의 원자 농도와 상기 제2 엘리먼트의 원자 농도 간의 제2 비율은 약 3.0:1인 반도체 디바이스.

명 세 서

기 술 분 야

<1> 본 출원은 일반적으로 집적 회로에 관한 것으로, 보다 구체적으로는 다층 소스/드레인 스트레서(multi-layer source/drain stressor)를 갖는 집적 회로에 관한 것이다.

배 경 기 술

<2> N 채널 및 P 채널 트랜지스터의 성능을 개선하는 방안들 중 한가지는 그 채널에 스트레인(strain)을 도입하는 것이다. 이러한 스트레인을 도입하는 방안들 중 한가지로는 소스/드레인 위치들로부터 반도체 물질을 제거하고 상이한 조성으로 이루어진 반도체 물질을 에피택셜 재성장(regrow)시키는 것이다. 예컨대, 초기의 반도체 물질과 이에 따른 채널이 순수 실리콘(just silicon)인 경우에, P 채널 성능을 개선하는 한가지 방안은 그 채널에 압축 스트레스를 가하는 소스/드레인 영역들에서 실리콘과 게르마늄의 조합(SiGe)을 재성장시키는 것이다. 이 방안의 어려움들 중 한가지는, 가해지는 스트레스의 양이 게르마늄의 농도에 의존하는데, 그 게르마늄의 농도를 증가시키면 결함(defect)의 형성을 야기하여 가해지는 스트레스를 줄일 수 있다는 것이다. 또한, 기술의 발전에 수반하여 디바이스 치수가 작아짐에 따라, 쇼트 채널(short channel) 트랜지스터들에 대해 양호한 성능 특성을 유지해야 한다는 한가지 중대한 도전에 직면해 있다.

<3> 따라서, 채널에 스트레스를 제공하기 위해 소스/드레인들을 재성장시키는 방안을 개선하는 것이 필요하다.

발명의 상세한 설명

<12> 일 측면에 있어서, 게이트에 인접한 소스/드레인 영역들은 제거되고 상이한 반도체 조합의 다층(multiple layers)을 이용하여 재성장된다. 일 실시예에서, 반도체 조합은 실리콘과 게르마늄의 합금(SiGe)이다. 제1 층은 제1 농도의 게르마늄을 갖고 제1 농도의 붕소로 도핑된다. 제1 층의 성장은 결함들이 발생하기 전에 종료된다. 제1 후속 층은 제2 두께(제2 두께는 제1 두께보다 큼)에 도달할 때까지 결함들을 갖지 않을 감소된 게르마늄 농도에서 성장된다. 이러한 제1 후속 층은 결함들 없이 성장되고 제1 농도의 붕소보다는 큰 농도의 제2 농도의 붕소로 붕소-도핑된다. 그 후, 제2 후속 층이 제1 후속 층에 비해 증가된 게르마늄 농도에서 성장되며 거의 어떠한 결함들도 존재하지 않도록 하기 위해 충분히 작은(low) 두께로 성장된다. 붕소 도핑은 제2 후속 층에서 한층 증가된다. 따라서, 제1 후속 층은 제1 층과 제2 후속 층의 높은 게르마늄 농도 층들에 비해 결함에 대한 걱정을 없애준다. 붕소는 쇼트 채널의 역효과를 피하기 위해 채널로부터의 거리가 증가함에 따라 증가된다. 이에 대해서는, 다음의 설명과 도면들에서 추가로 설명한다.

<13> 도 1에는, 반도체 기판(12), 기판 위의 절연층(14), 절연층(14) 위의 반도체 영역(16), 반도체 영역(16)을 둘러싸는 트렌치 절연 영역(18), 반도체 영역(16) 중앙부 위에 깔리는 게이트(22), 게이트(22)를 둘러싸는 측벽 스페이서(24), 게이트(22) 위의 절연 캡(30), 게이트(22)와 반도체 영역(16) 사이의 게이트 유전체, 반도체 영역(16)의 상면에서 게이트(22)의 한쪽에 인접한 소스/드레인 연장부(source/drain extension : 25), 및 반도체 영역(16)의 상면에서의 게이트(22)의 다른쪽 상의 소스/드레인 연장부(27)를 포함하는 반도체 디바이스(10)가 도시되어 있다. 소스/드레인 연장부들(25 및 27) 사이의 영역으로, 반도체 영역(16)의 상면을 따라 게이트(22) 아래 영역이 채널 역할을 할 것이다. 이러한 도 1의 구조는, 게이트(22)를 형성하고, 임플란트(implant)를 수행하여 소스/드레인 연장부들(25 및 27)을 형성하고, 측벽 스페이서(24)를 형성하며, 트렌치 절연 영역(18), 게이트(22), 캡(30) 및 측벽 스페이서(24)를 마스크로서 이용하여 반도체 영역(16)의 일부를 제거함으로써 결과적으로 한쪽에서 게이트(22)에 인접한 개구(26)와 다른쪽에서 게이트(22)에 인접한 개구(28)가 되게 하는 것에 기인한다. 이 에칭은 개구들(26 및 28)의 일부가 측벽 스페이서(24) 아래에 있는 식의 등방성, 바람직하게는 건식 등방성 에칭(dry isotropic etch)일 수 있다. 이 에칭이 일어나는 동안, N 채널 트랜지스터들은 마스크 오프(mask off)되고 이에 따라 에칭되지 않는다. 측벽 스페이서는 이방성 에칭이 뒤따르는 등방성 퇴적(conformal deposition)에 의해 형성되는 하나의 물질로서 도시되어 있지만, 복수 층에 형성될 수도 있고 라이너(liner)를 포함할 수도 있다. 대안으로는, 하나 또는 그 이상의 측벽 스페이서보다는 간단히 라이너로서 측벽 스페이서가 형성될 수도 있다. 일례로는, 질화물 스페이서와 반도체 영역(16) 사이뿐만 아니라 질화물 스페이서와 게이트(22) 사이에 산화물 라이너를 갖는 질화물 스페이서가 있다. 이 예에서의 반도체 영역(16)은, 반

도체 물질로서, 백그라운드 도핑 및 할로겐 임플란트(halo implant)와 같은 다른 도핑들을 가질 수 있는 순수 실리콘이다. 이러한 원리는 다른 반도체 물질들에도 또한 적용될 수 있다. 절연층(14)으로부터 게이트 유전체(20)로의 반도체 영역(16)의 두께는 예를 들어 약 500 옹스트롬(Angstrom)이다. 개구들(26 및 28)의 깊이는 예를 들어 350 옹스트롬이다. 기판(12), 절연층(14) 및 반도체 영역의 조합은 통상적으로 SOI(semiconductor on insulator) 기판으로 지칭되는 것을 형성한다. 절연층(14)은 통상적으로 BOX(buried oxide)로 지칭된다. 이 프로세스는 절연층이 존재하지 않는 벌크 실리콘 기판에도 효과적일 수 있다. 트렌치 절연 영역(18)은 트랜지스터를 전기적으로 분리시키거나 또는 트렌치 절연 영역(18)이 둘러싸고 있는 트랜지스터들을 전기적으로 분리시킨다.

<14> 도 2에는, 개구(26)에서 반도체 영역(16) 상에 반도체층(32)을 에피택셜 성장시키고, 개구(28)에서 반도체 영역(16) 상에 반도체층(34)을 에피택셜 성장시킨 후의 반도체 디바이스(10)가 도시되어 있다. 반도체층들(32 및 34)은 이 예에서 약 50 옹스트롬의 두께이고 붕소-도핑된 SiGe이다. Ge의 농도는 약 30%(atomic percent)이다. 이는 2.3:1의 Si:Ge 비율이다. 이 예에서의 붕소 도핑은 약 5e19($5x10^{19}$) atoms/cc(atoms per cubic centimeter)로부터 약 2e20($2x10^{20}$) atoms/cc까지이다. 30% 게르마늄에서, 반도체층들(32 및 34)은 결함들의 발생없이 순수 실리콘 상에 직접 50 옹스트롬까지 성장될 수 있다. 결함들은 그들이 존재하는 층을 느슨(relax)하게 하는 경향이 있기 때문에 결함들을 피하는 것이 중요하다. 결함들이 발생하면, 이는 채널들에 대해 스트레스를 발생시키려는 층들의 성장의 주요 목적을 좌절시킨다. 제1 성장된 층들(층들(32 및 34))에서의 비교적 높은 Ge%는 쇼트 채널 디바이스 제어를 향상시키기 위해 채널 영역으로의 불순물의 확산을 늦출 때 중요하다. 그 이유는 불순물(예를 들면, 붕소)의 확산성이, Si에서 보다도, 높은 Ge%를 갖는 SiGe에서 상당히 감소되기 때문이다. 약 5e19 atoms/cc로부터 2e20 atoms/cc까지의 붕소 농도는 채널로의 붕소의 확산을 한층 더 줄여 쇼트 채널 효과를 감소시키는 비교적 낮은 농도이다. 또한 에피택셜 성장에 붕소를 포함시킴으로써, 임플란트가 필요하지 않게 한다. 임플란트는, 또한 느슨함을 야기하므로 바람직하게는 피해야 하는 타입의 결함들을 발생시키는 경향이 있다. 층(32)의 두께는 위쪽으로의 성장이 측면으로의 성장보다 빠른 경향이 있기 때문에 측면 및 수직 방향에서 균일하지 않을 수도 있다.

<15> 도 3에는, 반도체층(32) 상에 반도체층(36)을 에피택셜 성장시키고, 반도체층(34) 상에 반도체층(38)을 에피택셜 성장시킨 후의 반도체 디바이스(10)가 도시되어 있다. 반도체층들(36 및 38)은 이 예에서 약 250 옹스트롬이고 또한 붕소-도핑된 SiGe이다. 이 층에서, 게르마늄 함유량(content)은 약 25%(3:1의 Si:Ge 비율)이고, 붕소 농도는 약 2e20/cc로부터 5e20/cc까지이다. 게르마늄 농도에서의 이러한 감소는 결함들을 발생시키지 않고 스트레서 막 두께의 증가를 지원한다. 붕소 농도에서의 증가는 도전성을 증가시키기 위한 것이지만, 또한 그 채널로부터 기인하는 쇼트 채널 문제점들의 발생 위험을 줄인다. 측면 성장은 그 성장이 지속됨에 따라 작아지고, 측면 방향에서의 반도체층들(36 및 38)의 두께는 위쪽 방향에서의 250 옹스트롬 성장보다도 훨씬 작다.

<16> 도 4에는, 반도체층(36) 상에 반도체층(40)을 에피택셜 성장시키고, 반도체층(38) 상에 반도체층(42)을 에피택셜 성장시킨 후의 반도체 디바이스(10)가 도시되어 있다. 반도체층들(40 및 42)은 이 예에서 약 300 옹스트롬이고 또한 붕소-도핑된 SiGe이다. 이 층에서, 게르마늄 함유량은 약 30%이고, 붕소 농도는 약 5e20/cc로부터 1e21/cc까지이다. 게르마늄 농도에서의 이러한 증가는 발생되는 스트레스를 증가시키고, 반도체층들(40 및 42)은 이들이 순수 Si 대신에 SiGe 상에서 성장되기 때문에 반도체층들(32 및 34)보다 두꺼울 수 있으며, 또한 반도체층들(40 및 42)의 상부는 악영향을 발생시키지 않고 결함들을 가질 수 있는데, 이는 그 상부가 후속 단계에서 금속 합금으로 변환되기 때문이다. 상단 층들(40 및 42)에서의 증가된 Ge 및 붕소 농도는 접촉 저항을 감소시킨다.

<17> 도 5에는, 반도체층들(40 및 42)의 상부를 금속 게르마늄 실리사이드층들(44 및 46)로 변환한 후의 반도체 디바이스(10)가 도시되어 있다. 소스/드레인 영역의 상부의 실리사이드로의 이러한 변환은 접촉부들(contacts)의 형성시 흔한 일이다. 상단 층들(40 및 42)에서의 증가된 Ge 및 붕소 농도는 실리사이드-반도체 계면에서의 접촉 저항을 감소시킨다. 반도체에 게르마늄이 존재하면, 금속 실리사이드 합금은 결과적으로 실리콘과 게르마늄을 포함하게 된다. 궁극적으로는 금속화 프로세스에서 소모되어 금속 게르마늄 실리사이드층들(44 및 46)을 형성하는 반도체층들(40 및 42)에서의 어떤 결함들도 역효과를 발생시키지 않는다.

<18> 도 6에는, 절연층(14)의 상단으로부터 반도체층들(40 및 42)의 상면으로의 붕소 농도의 증가를 보여주는 그래프가 도시되어 있다. 반도체층(16)과의 계면에서의 붕소 농도의 계단형 변화(abrupt change)는, 접합 커패시턴스를 감소시킬뿐만 아니라 PN 접합에 걸쳐 누설을 감소시키는데 보다 나은 계단형 PN 접합(abrupt PN junction)을 발생시키기 때문에 이롭다.

<19> 도 7에는, 절연층(14)의 상단으로부터 반도체층들(40 및 42)의 상면으로의 게르마늄 농도의 변화를 보여주는 그래프가 도시되어 있다. 이 스케일은 제로에서 시작하지는 않지만, 초기의 높은 농도, 감소된 중간 농도 및 최종의 높은 농도를 보여주고 있다. 이는 작은 결함들을 갖는 스트레서에서 높은 스트레스의 원하는 결과를 달성하는데 효과적인 방식이다.

<20> 따라서, 다층에서의 게르마늄의 농도를 바꿈으로써, 결함들의 발생 위험을 줄이면서 스트레서가 보다 큰 스트레스를 제공하게 할 수 있다. 이것의 유효성은 게르마늄의 농도와 선택된 두께 모두에 좌우된다. 게르마늄의 농도가 증가함에 따라, 특히 30%를 넘는 농도에 대해서는 그 두께가 감소될 필요가 있을 것이다. 더 높은 농도가 사용되는 경우에는, 게르마늄의 농도를 바꾸려는 추가의 층들을 제공하는 것이 이로울 수 있다. 또한, 층들이 추가될 때 붕소의 농도를 증가시킴으로써, 양호한 도전성을 얻으면서 쇼트 채널 효과의 위험을 감소시킨다.

<21> 이하, 반도체 디바이스를 형성하는 방법에 대해 설명한다. 이 방법은, 반도체 디바이스의 소스 영역에 리세스(recess)를 형성하고 드레인 영역에 리세스를 형성하는 단계; 소스 영역에 제1 반도체 물질을 형성하고 드레인 영역의 리세스에 제2 반도체 물질층을 형성하고, 제3 반도체 물질 및 제5 반도체 물질을 형성하는 단계; 제1 반도체 물질층 위에 깔리는 제3 반도체 물질층을 형성하고 제2 반도체 물질층 위에 깔리는 제4 반도체 물질층을 형성하는 단계; 및 제3 반도체 물질층 위에 깔리는 제5 반도체 물질층을 형성하고 제4 반도체 물질층 위에 깔리는 제6 반도체 물질층을 형성하는 단계를 포함한다. 제1 및 제2 반도체 물질층을 형성하는 단계는, 또한 제1 반도체 물질층과 제2 반도체 물질층 각각이 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제1 비율을 갖고 도핑 물질의 제1 농도 레벨(a first level of concentration of a doping material)을 가지는 스트레서 물질(stressor material)을 이용하여 형성되고, 제1 엘리먼트가 실리콘인 것을 특징으로 한다. 제3 및 제4 반도체 층들을 형성하는 단계는, 또한 제3 반도체 물질층과 제4 반도체 물질층 각각이 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제2 비율을 가지고, 제2 비율이 제1 비율보다 높고, 제3 반도체 물질층과 제4 반도체 물질층 각각이 도핑 물질의 제2 농도 레벨을 가지고, 도핑 물질의 제2 농도 레벨이 도핑 물질의 제1 농도 레벨보다 높은 것을 특징으로 한다. 제5 및 제6 반도체 물질층들을 형성하는 단계는, 또한 제5 반도체 물질층과 제6 반도체 물질층 각각이 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제3 비율을 가지고, 제3 비율이 제2 비율보다 낮고, 제5 반도체 물질층과 제6 반도체 물질층 각각이 도핑 물질의 제3 농도 레벨을 가지고, 도핑 물질의 제3 농도 레벨이 도핑 물질의 제2 농도 레벨보다 높은 것을 특징으로 한다. 이 방법은, 또한 스트레서 물질이 실리콘과 게르마늄의 합금이고, 제2 엘리먼트가 게르마늄인 것을 특징으로 한다. 이 방법은, 또한 도핑 물질이 주기율표의 V족 엘리먼트 중 하나 또는 그 이상인 것을 특징으로 한다. 이 방법은, 또한 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제1 비율이 약 2.3:1인 것을 특징으로 한다. 이 방법은, 또한 도핑 물질이 붕소이고, 도핑 물질의 제1 농도 레벨이 약 5e19 atoms/cm^3으로부터 약 2e20 atoms/cm^3까지인 것을 특징으로 한다. 이 방법은, 또한 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제2 비율이 약 3.0:1인 것을 특징으로 한다. 이 방법은, 또한 도핑 물질이 붕소이고, 도핑 물질의 제2 농도 레벨이 약 2e20 atoms/cm^3으로부터 5e20 atoms/cm^3까지인 것을 특징으로 한다. 이 방법은, 또한 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제3 비율이 약 2.3:1인 것을 특징으로 한다. 이 방법은, 또한 도핑 물질이 붕소이고, 도핑 물질의 제3 농도 레벨이 약 5e20 atoms/cm^3으로부터 1e21 atoms/cm^3까지의 범위내인 것을 특징으로 한다.

<22> 또한, 반도체 디바이스의 소스 영역에 리세스를 형성하고 드레인 영역에 리세스를 형성하는 단계; 소스 영역에서의 리세스에 제1 반도체 물질층을 형성하고 드레인 영역에서의 리세스에 제2 반도체 물질층을 형성하는 단계; 제1 반도체 물질층 위에 깔리는 제3 반도체 물질층을 형성하고 제2 반도체 물질층 위에 깔리는 제4 반도체 물질층을 형성하는 단계; 및 제3 반도체 물질층 위에 깔리는 제5 반도체 물질층을 형성하고 제4 반도체 물질층 위에 깔리는 제6 반도체 물질층을 형성하는 단계를 포함하는 반도체 디바이스의 형성 방법에 대해 설명한다. 제1 및 제2 반도체 물질층들을 형성하는 단계는, 또한 제1 반도체 물질층과 제2 반도체 물질층 각각이 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제1 비율을 갖는 스트레서 물질을 이용하여 형성되고, 제1 엘리먼트가 실리콘이고, 제1 반도체 물질층과 제2 반도체 물질층 각각이 도핑 물질의 제1 농도 레벨을 갖는 것을 특징으로 한다. 제3 및 제4 반도체 물질층들을 형성하는 단계는, 또한 제3 반도체 물질층과 제4 반도체 물질층 각각이 도핑 물질의 제2 농도 레벨을 가지고, 도핑 물질의 제2 농도 레벨이 도핑 물질의 제1 농도 레벨보다 높은 것을 특징으로 한다. 제5 및 제6 반도체 물질층들을 형성하는 단계는, 또한 제5 반도체 물질층과 제6 반도체 물질층 각각이 도핑 물질의 제3 농도 레벨을 가지고, 도핑 물질의 제3 농도 레벨이 도핑 물질의 제2 농도 레벨보다 높은 것을 특징으로 한다. 이 방법은, 또한 도핑 물질이 주기율표의 V족 엘리먼트 중 하나 또는 그 이상

인 것을 특징으로 한다. 이 방법은, 또한 도핑 물질이 붕소이고, 도핑 물질의 제1 농도 레벨이 약 5e19 atoms/cm^3으로부터 약 2e20 atoms/cm^3까지인 것을 특징으로 한다. 이 방법은, 또한 도핑 물질의 제2 농도 레벨이 약 2e20 atoms/cm^3으로부터 5e20 atoms/cm^3까지인 것을 특징으로 한다. 이 방법은, 또한 도핑 물질의 제3 농도 레벨이 약 5e20 atoms/cm^3으로부터 1e21 atoms/cm^3까지의 범위 내인 것을 특징으로 한다.

<23> 또한, 소스 영역의 리세스에서의 제1 반도체 물질층과, 드레인 영역의 리세스에서의 제2 반도체 물질층; 제1 반도체 물질층 위에 깔리는 제3 반도체 물질층과, 제2 반도체 물질층 위에 깔리는 제4 반도체 물질층; 및 제3 반도체 물질층 위에 깔리는 제5 반도체 물질층과, 제4 반도체 물질층 위에 깔리는 제6 반도체 물질층을 포함하는 반도체에 대해 설명한다. 제1 및 제2 반도체 물질층들은, 또한 제1 반도체 물질층과 제2 반도체 물질층 각각이 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제1 비율을 가지며 도핑 물질의 제1 농도 레벨을 가지는 스트레서 물질을 이용하여 형성되고, 제1 엘리먼트가 실리콘인 것을 특징으로 한다. 제3 및 제4 반도체 물질층들은, 또한 제3 반도체 물질층과 제4 반도체 물질층 각각이 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제2 비율을 가지고, 제2 비율이 제1 비율보다 높고, 제3 반도체 물질층과 제4 반도체 물질층 각각이 도핑 물질의 제2 농도 레벨을 가지고, 도핑 물질의 제2 농도 레벨이 도핑 물질의 제1 농도 레벨보다 높은 것을 특징으로 한다. 제5 및 제6 반도체 물질층들은, 또한 제5 반도체 물질층과 제6 반도체 물질층 각각이 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제3 비율을 가지고, 제3 비율이 제2 비율보다 낮고, 제5 반도체 물질층과 제6 반도체 물질층 각각이 도핑 물질의 제3 농도 레벨을 가지고, 도핑 물질의 제3 농도 레벨이 도핑 물질의 제2 농도 레벨보다 높은 것을 특징으로 한다. 반도체 디바이스는, 또한 스트레서 물질이 실리콘과 게르마늄의 합금이고, 제2 엘리먼트가 게르마늄인 것을 특징으로 한다. 반도체 디바이스는, 또한 도핑 물질이 주기율표의 V족 엘리먼트 중 하나 또는 그 이상인 것을 특징으로 한다. 반도체 디바이스는, 또한 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제1 비율이 약 2.3:1인 것을 특징으로 한다. 반도체 디바이스는, 또한 도핑 물질이 붕소이고, 도핑 물질의 제1 농도 레벨이 약 5e19 atoms/cm^3으로부터 약 2e20 atoms/cm^3까지이고, 도핑 물질의 제2 농도 레벨이 약 2e20 atoms/cm^3으로부터 5e20 atoms/cm^3까지이며, 도핑 물질의 제3 농도 레벨이 약 5e20 atoms/cm^3으로부터 1e21 atoms/cm^3까지의 범위 내인 것을 특징으로 한다. 반도체 디바이스는, 또한 제1 엘리먼트의 원자 농도와 제2 엘리먼트의 원자 농도 간의 제2 비율이 약 3.0:1인 것을 특징으로 한다.

<24> 본 명세서에서는 특정한 실시예들을 참조하여 본 발명에 대해 설명하였지만, 다음의 청구범위에 개시된 바와 같은 본 발명의 범주를 벗어나지 않고서 다양한 수정 및 변경들을 행할 수 있다. 예컨대, P 채널 트랜지스터들에 스트레스를 추가하기 보다는, 소스/드레인 스트레서들을 제공하는 것과 유사한 방식으로 N 채널 트랜지스터들의 채널들에 신장 스트레스(tensile stress)를 가함으로써 N 채널 트랜지스터들에 스트레스를 추가할 수도 있다. 이는 결함의 발생을 피하면서 탄화 실리콘(silicon carbon)을 재성장시키고 상이한 층들에서 탄소의 농도를 바꿈으로써 원하는 스트레스를 제공하는 것에 의해 달성될 수 있다. 또한, P 채널 트랜지스터들에 대해 붕소 불순물을 증가시키는 것과 유사한 방식으로 층들에 N 채널 불순물을 증가시키는 것이 이로울 수 있다. 이는 불순물이 비소인 경우에 비소의 낮은 확산 속도로 인해 덜 필요할 수도 있지만, 여전히 몇몇 이점이 존재한다. 따라서, 본 명세서와 도면들은 국한적인 의미라기보다는 예시적인 의미로 간주되어야 하며, 이러한 변형들 모두는 본 발명의 범주 내에 포함되는 것으로 의도되어 진다. 본 명세서에서 특정한 실시예들과 관련하여 설명하였던 문제점들의 어떤 해결방안들, 이점들 또는 이익들은 본 청구범위의 어느 청구항 또는 모든 청구항들의 결정적이거나 필요하거나 또는 본질적인 특징 또는 구성요소로서 해석되는 것으로 의도되지는 않는다.

<25> 더욱이, 본 명세서에서 사용된 "한"("a" 또는 "an")과 같은 용어는 하나보다는 하나 또는 그 이상의 것으로 규정된다. 또한, 본 청구범위에서 "적어도 하나" 및 "하나 또는 그 이상"과 같은 도입구(introductory phrase)들의 사용은, 동일한 청구항이 "하나 또는 그 이상" 또는 "적어도 하나"와 같은 도입구들 및 "한"과 같은 부정 관사들을 포함하는 경우에도, "한"과 같은 부정 관사들에 의한 다른 청구항 구성요소의 도입이 이러한 도입된 청구항 구성요소를 포함하는 임의의 특정한 청구항을 하나의 이러한 구성요소만을 포함하는 발명들로 제한하고자 하는 것으로 해석되어서는 안된다. 이는 정관사에 대해서도 동일하게 적용된다.

<26> 달리 언급되지 않는다면, "제1" 및 "제2"와 같은 용어들은 이러한 용어들이 나타내는 구성요소들 간의 임의 구별을 위해 사용되었다. 따라서, 이러한 용어들은 그 구성요소들의 시간적인 또는 다른 우선 순위를 나타내려는 것으로 의도되지는 않는다.

도면의 간단한 설명

<4> 본 발명은 유사한 참조부호가 유사한 구성요소들을 나타내고 있는 첨부 도면들에 의해 예를 드는 식으로 도해되어 있지만, 이러한 첨부 도면들에만 국한되는 것은 아니다. 이러한 도면들에서의 구성요소들은 간결하고 명확하게 도시되어 있으며 반드시 일정한 비율로 스케일링되어 있는 것은 아니다.

<5> 도 1은 본 발명의 일 실시예에 따른 프로세싱 단계에서의 반도체 디바이스의 단면도.

<6> 도 2는 후속 프로세싱 단계에서의 도 1의 반도체 디바이스의 단면도.

<7> 도 3은 후속 프로세싱 단계에서의 도 2의 반도체 디바이스의 단면도.

<8> 도 4는 후속 프로세싱 단계에서의 도 3의 반도체 디바이스의 단면도.

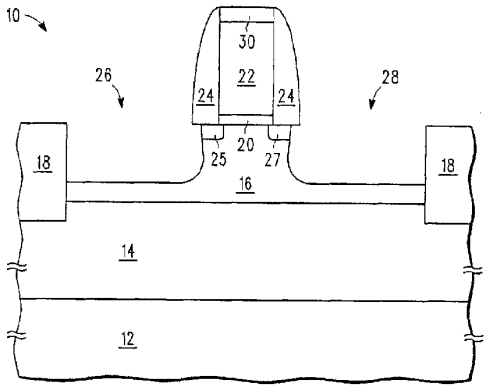
<9> 도 5는 후속 프로세싱 단계에서의 도 4의 반도체 디바이스의 단면도.

<10> 도 6은 에피택셜 성장 영역들을 포함하는 도 5의 반도체 디바이스의 반도체 영역에서의 붕소의 상대 농도를 보여주는 그래프.

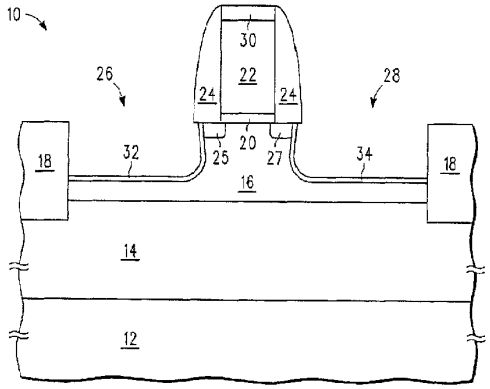
<11> 도 7은 도 5의 반도체 디바이스의 반도체 영역에서의 게르마늄의 상대 농도를 보여주는 그래프.

도면

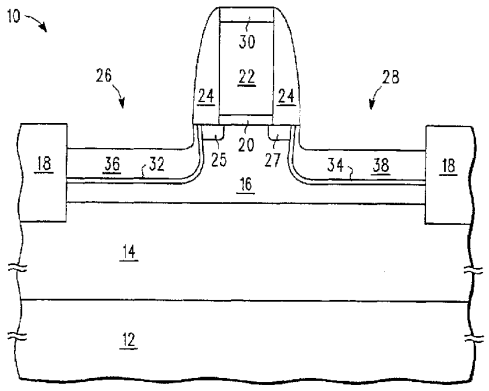
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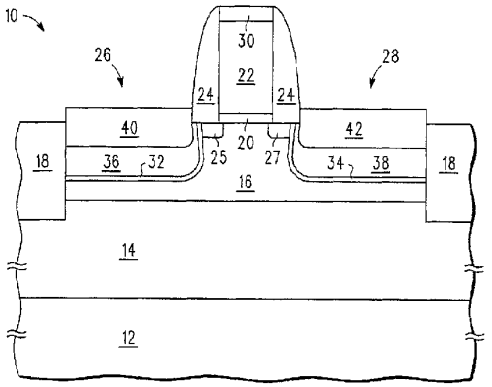
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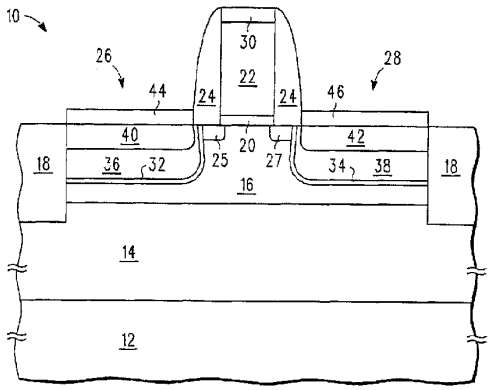
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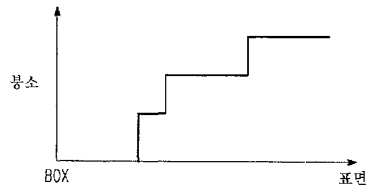
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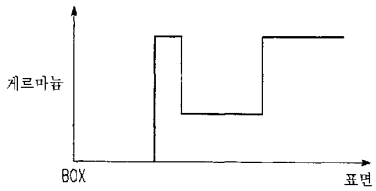
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도면6



도면7



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Strained fin FETs structure and method

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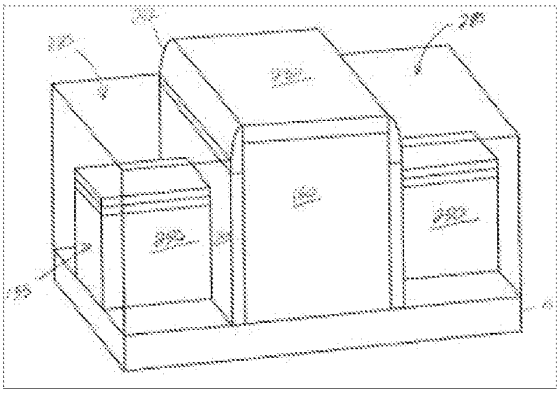
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Abstract of TW200304703 (A)

A method and structure for a transistor that includes an insulator and a silicon structure on the insulator. The silicon structure includes a central portion and Fins extending from ends of the central portion. A first gate is positioned on a first side of the central portion of the silicon structure. A strain-producing layer could be between the first gate and the first side of the central portion of the silicon structure and a second gate is on a second side of the central portion of the silicon structure.



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Description: TW200304703 (A) — 2003-10-01

Strained fin FETs structure and method

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BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention generally relates to the field of semiconductor manufacturing and, more specifically, to a method for forming double-gated field effect transistors.

[0003] 2. Description of the Related Art

[0004] The need to remain cost and performance competitive in the production of semiconductor devices has caused continually increasing device density in integrated circuits. To facilitate the increase in device density, new technologies are constantly needed to allow the feature size of these semiconductor devices to be reduced.

[0005] The push for ever-increasing device densities is particularly strong in complementary metal oxide semiconductor (CMOS) technologies, such as the in the design and fabrication of field effect transistors (FETs). FETs are used in almost all types of integrated circuit design (i.e., microprocessors, memory, etc.). Unfortunately, increased device density in CMOS FETs often results in degradation of performance and/or reliability.

[0006] One type of FET that has been proposed to facilitate increased device density is a double gated field effect transistor. Double gated FETs use two gates, one on each

side of the body to facilitate scaling of CMOS dimensions while maintaining acceptable performance. In particular, the use of the double gate increases the gate area, which allows the transistor to have better current control without increasing the gate length of the device. As such, the double gated FET is able to have the current control of a larger transistor without requiring the device space of the larger transistor.

[0007] Unfortunately, several difficulties arise in the design and fabrication of double gated CMOS transistors. First, the relative dimensions of a double gated transistor are such that it is difficult to reliably fabricate one that has reliable performance and minimum feature size. Second, the threshold voltage of a double gated transistor is highly dependent upon the material used for the two gates. In particular, current fabrication techniques have generally resulted in a double gated transistor that has either too high a threshold voltage or too low a threshold voltage. For example, if the gates are doped the same polarity as the source, the threshold voltage will generally be near zero. Conversely, if the gates are doped the opposite polarity of the source, then the threshold voltage will be approximately one volt. Neither result is desirable in most CMOS applications.

[0008] Thus, there is a need for improved device structures and methods of fabrication of double gated CMOS devices that provide improved threshold voltage of the resulting double gated CMOS without overly increasing fabrication complexity.

[0009] Physical strain on the channel material in FET can improve carrier mobility. Strain induced on planar p-type metal oxide semiconductor field effect transistor (MOSFET) devices has been shown to increase hole mobility in excess of 30%. This invention provides these advantages to thin semiconductor bodies that are vertically arranged on a substrate; as such, the invention combines greater channel control with greater carrier mobility.

SUMMARY OF THE INVENTION

[0010] The asymmetric strained Fin Field effect transistor has an insulator and a semiconductor structure on the insulator. The structure includes a central portion and first and second ends extending from the central portion. A first gate is positioned on a first side of the central portion of the structure, a strain-producing layer between the first gate and the first side of the central portion of the structure, and a second gate on a second side of the central portion of the structure. The insulator is a buried oxide layer and the central portion of the structure is silicon. The strain-producing layer has a sufficient concentration of germanium to produce strain within the central portion to enhance carrier mobility without producing sufficient dislocations to reduce overall performance of the transistor. The first and second ends are source and drain regions, respectively. The concentration of germanium is between 10% and 40%. The different gates may be doped differently to adjust VT. The gates may also be doped similarly.

[0011] The symmetric strained Fin field effect transistor has an insulator and a semiconductor structure on the insulator. The structure is a Fin body having a central portion having silicon and silicon germanium and end portions comprising silicon. A first gate is positioned on a first side of the central portion of the silicon structure and a second gate is on a second side of the central portion of the structure. The first gate and the second gate may again be doped similarly or differently (as with the asymmetric strained situation).

[0012] The method of forming a transistor includes forming a silicon layer on an insulator, etching a first portion of the silicon layer to create a first opening, depositing a first gate in the first opening and etching a second portion of the silicon layer to create a second opening opposite the first opening. After the etching of the second portion, the silicon layer has a silicon structure on the insulator having a central portion and Fins extending from ends of the central portion. The invention forms a strain-producing layer upon a portion of the silicon structure facing the second opening which forms a second gate in the second opening, and removes the first gate and the second gate from all portions of the silicon structure except from the central portion.

[0013] The method of forming an asymmetric strained Fin field effect transistor includes forming a silicon layer on an insulator, etching a first portion of the silicon layer to create a first opening, depositing a first gate in the first opening, etching a second portion of the silicon layer to create a second opening opposite the first opening. After the etching of the second portion, the silicon layer has a silicon structure on the insulator having a central portion and Fins extending from ends of the central portion. The invention forms a silicon germanium layer upon a portion of the silicon structure facing the second opening, forms a second gate doped differently or similarly to the first gate in the second opening and removes the first gate and the second gate from all portions of the silicon structure except the central portion.

[0014] The method of forming strained Fin field effect transistors includes forming a silicon structure on an insulator, forming stress on one or both sides of the silicon structure, having a central portion and Fins extending from ends of the central portion, depositing a first gate and a second gate on sides of the silicon structure, and removing the first gate and the second gate from all portions of the silicon structure except the central portion.

[0015] Physical strain on the channel material in FETs can improve carrier mobility.

[0016] Strain induced on planar p-type metal oxide semiconductor field effect transistor (MOSFET) devices has been shown to increase hole mobility in excess of 30%. This invention provides these advantages to thin semiconductor bodies that are vertically arranged on a substrate; and, as such, the invention combines greater channel control with greater carrier mobility.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment(s) of the invention with reference to the drawings, in which:

[0018] FIGS. 1-20, 22, 24 and 25 are cross-sectional views of a first embodiment of a FET structure produced utilizing a method according to a first embodiment of the invention;

[0019] FIGS. 21, 23, and 26-28 are perspective views of the first embodiment of FET structure produced utilizing the method according to the first embodiment of the invention;

[0020] FIGS. 29-31 are cross-sectional views of the second embodiment of a FET structure produced utilizing a method in accordance with a second embodiment of the

invention;

[0021] FIG. 32 is a flowchart illustrating a sequence of steps in accordance with the first embodiment of the invention; and

[0022] FIG. 33 is a flowchart illustrating a sequence of steps in accordance with the second embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0023] This invention relates to enhanced Fin FET devices and builds strain into such devices. The present invention is implemented using a "Fin" type FET double gated structure. In a Fin FET type structure, the double gates are formed on each side of the body, with the body being disposed horizontally between the gates. The invention produces a Fin FET that has a channel body that is strained through the operation of a silicon germanium layer. Processing is started on a wafer that is built, potentially through wafer bonding, to include a silicon bulk wafer on the bottom, a relatively thick bottom oxide layer and a relaxed SiGe layer on top. A thin Fin is then etched out of the SiGe, stopping on the BOX layer. A thin layer of epitaxial silicon can then be grown onto the Fin. Due to the difference in the crystalline lattice constant of Silicon and SiGe, the epitaxial layer will grow under strained conditions. The invention can be included in symmetrical or asymmetrical gate workfunction Fin FET devices.

[0024] While the invention is described above with respect to an asymmetric strained Fin FET, it is equally applicable to a symmetric strained Fin FET. More specifically, as shown in FIGS. 29-31, the processing necessary to create a strained symmetric strained Fin FET in accordance with a second embodiment of the invention starts with a SOI structure having a SiGe layer 300 above and insulator 10 (this is shown in FIG. 29). The SiGe layer 300 is selectively patterned, as shown in FIG. 30. Then, a silicon layer 315 is grown on the SiGe layer 300 to create a strained structure. A thermal oxide 320 is then grown on the silicon layer 315. Next, the gate conductors (e.g., polysilicon) 310 are deposited, planarized, and patterned to form the gates surrounding the body structure 155. In one embodiment, the gate conductors 310 have the same doping concentration and material makeup. However, in a different embodiment, the gate electrodes 310 can be made asymmetric with, for example, an ion implant, to result in an asymmetric gate workfunction Fin FET with strain. More specifically, in the asymmetric gate arrangement, the gate conductors 310 would have different doping concentrations or utilize different dopants. Processing proceeds to complete the structure shown in FIGS. 18-28, as discussed above.

[0025] An important feature of the invention is that it provides strain within many different forms of Fin FETs. One of the strained Fin FET embodiments shown in FIGS. 1-28 utilizes an SOI arrangement to formed a strained Fin FET that has either symmetric or asymmetric gate conductors. Alternatively, as explained with respect to FIG. 15, if the oxide 150 is omitted, a dynamic threshold Fin FET is formed. To the contrary, the embodiment shown in FIGS. 29-31 utilizes a SiGe-OI (silicon germanium over insulator) in place of the SOI structure shown in FIGS. 1-28. In a similar manner, the SiGe-OI structure can be formed as an asymmetric gate or symmetric gate structure depending upon the doping of the gate conductors. The forgoing embodiments are merely illustrative of the invention and the invention is not limited to these specific embodiments. Instead, the embodiments shown above are merely examples and one ordinarily skilled in the art would understand that many different

types of Fin FETs would achieve beneficial results by including the inventive strain structure.

[0026] The formation of a Fin FET according to a first embodiment of the invention is shown in FIGS. 1-28. Processing begins as shown FIG. 1 where a silicon over an insulator (SOI) structure includes an insulator 10 such as a buried oxide layer with an overlying silicon layer 11. A placeholder layer 12 (such as a nitride, etc.) is deposited over the silicon layer 11. This structure is then patterned using well-known conventional patterning processes, as shown in FIG. 2, to remove a portion 20 of the placeholder layer 12. A subsequent etching step removes any corresponding portion 30 of the silicon layer 11 not protected by the placeholder 12, as shown in FIG. 3.

[0027] In FIG. 4, an oxidation process grows a gate oxide layer 40 on the silicon 11. Next, polysilicon 50 is deposited over the structure, as shown FIG. 5. The polysilicon 50 is of one dopant type (e.g., N+ doped polysilicon, etc.). In FIG. 6, the structure is planarized using, for example, a chemical mechanical polishing (CMP) process to form planar layer 60. FIG. 7 illustrates an oxidation process in which the doped polysilicon 50 oxidizes at a faster rate than the placeholder material 12. Therefore, the oxide layer 70 over the polysilicon 50 is thicker than the oxide layer 71 over the placeholder layer 12.

[0028] The oxide layers 70, 71 are etched at a controlled rate, as shown in FIG. 8. Once the placeholder layer 12 is exposed, the etching process is stopped. This removes all the oxide from the upper surface of the placeholder layer 12, while leaving some oxide 70 above the polysilicon layer 50. Next, in FIG. 9, the placeholder layer 12 is removed using a selected etching process, leaving the upper portion 90 of the silicon 11 exposed.

[0029] In FIG. 10, a hard mask 100 (such as TEOS, etc.) is conformally deposited over the upper layers of the structure. Then, as shown in FIG. 11, a directional anisotropic etch is used to remove the hard mask 100 from all horizontal surfaces 110, yet allow the hard mask 100 to remain upon the vertical surfaces of the polysilicon 50 and the oxide 70. In FIG. 12, the silicon 11 is patterned to remove the portion 120. Only the portion beneath the hard mask 100 remains after the patterning process.

[0030] FIG. 13 illustrates the growth of selective SiGe 130. While SiGe is used in this example, the invention is not limited to such material composition. Any substance which will present a lattice mismatch with the silicon will produce stress and would be useful with the invention. More specifically, the structure is heated in a complex having Ge, which causes the SiGe 130 to grow from the silicon 11. This builds strain into the already-formed silicon channel 11. The resulting Si layer is strained due to the lattice mismatch between the SiGe and the smaller lattice constant silicon layer. Physical strain on the channel material in an FET can improve carrier mobility. Strain induced on planar p-type metal oxide semiconductor field effect transistor (MOSFET) devices has been shown to increase hole mobility in excess of 30%. This is because the strain splits the conduction and valence bands and raises the energy of the low mobility ellipsoids, depopulating them of holes.

[0031] At the same time, excessive amounts of germanium will produce misfit dislocations that will degrade device performance. The inventors have found the optimal range of the content to be 10% to 40% germanium.

[0032] Strain is induced on conventional planar devices by use of Shallow Trench Isolation (STI) techniques. In a Fin FET, however, there is no process analogous to STI, as the buried insulator layer 10 (BOX) provides the device isolation. The invention overcomes this problem by using Silicon Germanium (SiGe) and silicon sidewall films to generate this strain on the Fin FET channel.

[0033] In FIG. 14, the oxide 70 is removed from the upper surface 141 of the polysilicon 50. This also reduces the height 142 of the hard mask 100 and forms a step 140 in the insulator 10. Another thermal oxidation step forms an oxide 150 over the SiGe 130 surface, as shown in FIG. 15. Alternatively, the formation of the oxide 150 could be omitted to form a dynamic threshold Fin FET. In the embodiment without the oxide 150 (the dynamic threshold (DT) Fin FET) the strained Fin FET DT CMOS devices are formed with body tied to gate. This structure, including the silicon 11, gate oxide 40, hard mask 100, oxide 150, and SiGe 130, is referred to hereinafter as the "body" and is identified in the drawings as item 155 in order to simplify the description and illustration.

[0034] Next, in FIG. 16, a second polysilicon 160, that may be doped differently or similarly to the first polysilicon 50, is deposited over the entire structure. The structure is again planarized, forming a planar upper surface 170, as shown in FIG. 17. Since the first polysilicon 50 was an N+ doped polysilicon, the second polysilicon 160 is preferably a P+ polysilicon. However, the first and second polysilicon could be the same for symmetric gate devices. The two types of polysilicon could be substituted for one another, or for other types of doping now known or developed in the future. The important point is that the polysilicon regions 50, 160 existing on opposite sides of the body 155 are doped differently for asymmetric structures. The polysilicon 50, 160 could be Germanium doped or any other conductor. Utilizing differently-doped polysilicon on opposite sides of the silicon channel structure 11 creates an asymmetric gate Fin FET.

[0035] Various electrically conducting materials have associated with them a built-in electrical potential, often referred to as a fermi level, which, along with externally applied voltage, determines the relative affinity of the conductor for electrons (or holes). In a metal, the fermi level is intrinsic to the material while in a semiconductor, such as silicon, this fermi level can be adjusted to values between the valence band and conduction band by introduction of impurities which supply excess holes or electrons. In the asymmetric double gated Fin FET, the two gate electrodes 50, 160 are doped with opposite polarity, with one gate being doped N-type and the other gate being doped P-type. Thus, the two gate electrodes 50, 160 have different fermi levels and, hence, one gate electrode (the strong gate, the n-gate for nFETs) has a greater affinity for the inversion carriers while the other electrode (the weak gate, the p-gate for nFETs) has a lesser affinity for the inversion carriers. As a result, the inversion channel will form in the semiconductor body at a location nearer the "strong" gate. Thus, both gate electrodes contribute to the inversion potential, leading to a relatively low threshold voltage (e.g., between 0 and 0.5 volts).

[0036] In the embodiment being illustrated and discussed, the structure is an asymmetric Fin FET device, the silicon 11 is only etched on one side 30, and the placeholder 12 above the remaining silicon 11 is left in place. The invention grows selective single-crystal SiGe 130 on the exposed half of the Fin structure (on the side opposite the gate oxide). However, the invention is also applicable to symmetric Fin FETs, as shown later.

[0037] Processing proceeds, as shown in FIG. 18, with the deposition or growth of an

intrinsic silicon layer 180. Then, in FIG. 19, another insulator hard mask 190 (such as TEOS, etc.) is deposited over the intrinsic silicon 18 and patterned using conventional patterning techniques to remove portions 200, as shown in FIG. 20. The same structure is shown in perspective view in FIG. 21. The polysilicon electrodes 50, 160 and intrinsic silicon 180 are patterned using the hard mask 190, as shown in FIG. 22 (and in perspective view in FIG. 23). The hard mask 190 is then removed from area 220, as shown in FIG. 24. The patterning of the gates 50, 160 preferably removes all the gate polysilicon down to the buried oxide layer 10 and is done using a directional etch that is selective to the nitride or oxide. Thus, the patterning does not remove the portions of the body 155 that are protected by the previously-formed hard mask 100. The patterning leaves a portion of polysilicon 50 and polysilicon 160, which defines the two gates of the double gated transistor. A buffered HF clean up is performed, followed by a thermal reoxidation designed to grow oxide on all the exposed silicon surfaces. This preferably forms a thin (50 angstrom) film of oxide that provides good interface when the gate meets the body.

[0038] The invention then performs well-known, conventional source, drain, and halo implants in the transistor. Preferably, these implants are made into all four directions of the exposed portions (Fins 250) of the body 155 to ensure that a uniform implant is made into both sides of the body. In particular, both the source and drain implants are made from both sides of the Fins 250 of the body 155. Then, another implant is made, with different implant energies and angles, to form the halo implants in the body 155 that improve short channel effects. The halo implants are performed at higher energies and at angles more acute with respect to the Fin 250 in order to assure placement of the halo dopant further under the gate electrodes 50, 160 than the source/drain dopants.

[0039] Next, the invention deposits a dielectric 240 of thickness greater than the height of the combined gate electrodes 50, 160 and hardmask 232, covering the entire gate electrodes 50, 160 and exposed Fins 250, as shown in FIG. 25. This dielectric is then planarized and partially recessed until a portion of the hardmask232 and gate electrodes 50, 160, but not any of the source/drain Fin region, is exposed, as shown in FIG. 25. As shown in FIG. 26, the dielectric 240 is etched to cover only the sides of the gates 50, 160 and sidewall spacers 242 are formed on the edges of the gates above the dielectric 240. This is preferably done using a conformal deposition of a dielectric material, followed by a directional etch. The sidewall spacers 242 are preferably formed of a nitride. The dielectric 240, sidewall spacers 242, and hardmask 232 are used to mask a directional etch and thereby remove the oxides 40, 150, except in areas adjacent the gates. The hardmask 232, the sidewall spacers 242, and the sidewall portions 240 combine to effectively isolate the gate 50, 160 from the source and drain 250 contacts 280, as shown in FIG. 27. Preferably, the source and drain contacts 280 comprise a patterned conductive material. Next, as shown in FIG. 28, the intrinsic silicon layer 180 is silicided using conventional, well-known silicide processes, forming silicide layer 230.

[0040] In FIG. 32, a flow chart summarizing this first embodiment of the invention is shown. First, in item 320, the invention forms a silicon layer 11 on an insulator 10. Then, in item 321, the invention creates a first opening 30. In item 322, the invention grows a first oxide layer 40 on the silicon layer 11. Next, in item 323, the invention deposits a first gate 50 in the first opening. In item 324, the invention etches the silicon layer 11 to create a silicon structure 155 having a central portion and Fins. The invention forms a strain-producing layer 130 in item 325. Next, in item 326, the

invention grows a second oxide layer 150 on the strain-producing layer 130. In item 327, the invention forms a second gate 160 in the second opening 140. Then, in item 328, the invention removes the first gate and second gate from all portions of the silicon structure except the central portion. In item 329, the invention dopes the Fins 250 such that the Fins 250 comprise source and drain regions. Lastly, in item 330, the invention forms source and drain contacts 280 over source and drain regions.

[0041] In operation, a voltage within the gates 50, 160 changes the conductivity of the region of the semiconducting silicon 11 that is covered by the gates 50, 160. This operation either makes or breaks an electrical connection between the source and drain Fins 250. Therefore, the device can be used as an electrical switch to perform logical operations.

[0042] As mentioned above, one important feature of the invention is the SiGe layer 130 that remains as a permanent part of the body 155. More specifically, such a feature builds strain into the silicon channel 11. Physical strain on the channel material in an FET can improve carrier mobility.

[0043] While the invention is described above with respect to an asymmetric strained Fin FET, it is equally applicable to a symmetric strained Fin FET. More specifically, as shown in FIGS. 29-31, the processing necessary to create a strained symmetric strained Fin FET in accordance with a second embodiment of the invention starts with a SOI structure having a SiGe layer 300 above an insulator 10 (this is shown in FIG. 29). The SiGe layer 300 is selectively patterned, as shown in FIG. 30. Then, a silicon layer 315 is grown on the SiGe layer 300 to create a strained structure. A thermal oxide 320 is then grown on the silicon layer 315. Next, the gate conductors (e.g., polysilicon) 310 are deposited, planarized, and patterned to form the gates surrounding the body structure 155. In one embodiment, the gate conductors 310 have the same doping concentration and material makeup. However, in a different embodiment, the gate electrodes 310 can be made asymmetric with, for example, an ion implant to result in an asymmetric gate workfunction Fin FET with strain. More specifically, in the asymmetric gate arrangement, the gate conductors 310 would have different doping concentrations or utilize different dopants. Processing proceeds to complete the structure shown in FIGS. 18-28, as discussed above.

[0044] An important feature of the invention is that it provides strain within many different forms of Fin FETs. One of the strained Fin FET embodiments shown in FIGS. 1-28 utilizes an SOI arrangement to form a strained Fin FET that has either symmetric or asymmetric gate conductors. Alternatively, as explained with respect to FIG. 15, if the oxide 150 is omitted, a dynamic threshold Fin FET is formed. To the contrary, the embodiment shown in FIGS. 29-31 utilizes a SiGe-OI (silicon germanium over insulator) in place of the SOI structure shown in FIGS. 1-28. In a similar manner, the SiGe-OI structure can be formed as an asymmetric gate or symmetric gate structure, depending upon the doping of the gate conductors. The forgoing embodiments are merely illustrative of the invention and the invention is not limited to these specific embodiments. Instead, the embodiments shown above are merely examples and one ordinarily skilled in the art would understand that many different types of FinFETs would achieve beneficial results by including the inventive strain structure.

[0045] In FIG. 33, a flow chart for constructing a symmetric strained Fin field effect transistor, in accordance with a second embodiment of the invention, is shown. First, in item 331, the method forms a silicon germanium layer 300 on an insulator 10. Next, in

item 332, the method etches a silicon germanium layer to create a silicon structure that has a central portion and Fins 250. In item 333, the method grows an oxide layer 320 on silicon structure 300. In item 334, the method deposits gates on sides of the silicon structure. Next, in item 336, the method removes the first gate and second gate from all portions of the silicon structure except the central portion. In item 337, the method dopes the Fins 250 such that the Fins 250 are source and drain regions. Lastly, in item 338, the method forms source and drain contacts 280 over source and drain regions.

[0046] As mentioned above, the SiGe layer 130 builds strain into the already-formed silicon channel 11. Physical strain on the channel material in FET can improve carrier mobility. Strain induced on planar p-type metal oxide semiconductor field effect transistor (MOSFET) devices has been shown to increase hole mobility up to 30%. This invention provides these advantages to thin semiconductor bodies that are vertically arranged on a substrate; and as such, the invention combines greater channel control with greater carrier mobility.

[0047] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims. For example, while the invention has been taught with reference to a particular method of forming vertical semiconductor bodies, other methods of producing discrete semiconductor bodies on a substrate could be used (e.g., silicon islands on a SOI substrate). Moreover, while SiGe is taught as the primary material to induce the requisite strain in the channel region, other materials could be used. Finally, the invention is applicable to other semiconductors (e.g., Group III-IV semiconductors such as gallium arsenide).

Espacenet

Claims: TW200304703 (A) — 2003-10-01

Strained fin FETs structure and method

Claims not available for TW200304703 (A)
Claims of corresponding document: US2003178677 (A1)

A high quality text as facsimile in your desired language may be available amongst the following family members:

EP1488462 (A2) JP2005521258 (A) KR20040094702 (A) US2003178677 (A1) WO03081640 (A2) US2003178681 (A1) US2003201458 (A1)

- Original claims
- Claims tree

The EPO does not accept any responsibility for the accuracy of data and information originating from other authorities than the EPO; in particular, the EPO does not guarantee that they are complete, up-to-date or fit for specific purposes.

What is claimed is:

1. A transistor comprising:
an insulator;
a semiconductor structure on said insulator, wherein said structure includes a central portion and first and second ends extending from said central portion;
a first gate positioned on a first side of said central portion of said structure;
a strain-producing layer between said first gate and said first side of said central portion of said structure; and
a second gate on a second side of said central portion of said structure.

2. The transistor in claim 1, wherein said insulator comprises a buried oxide layer.

3. The transistor in claim 1, wherein said central portion of said structure comprises silicon.

4. The transistor in claim 1, wherein said strain-inducing layer has a sufficient concentration of germanium to produce strain within said central portion to enhance carrier mobility, without producing sufficient dislocations to reduce overall performance of said transistor.

5. The transistor in claim 1, wherein said first and second ends comprise source and drain regions, respectively.

6. The transistor in claim 4, wherein said concentration of germanium is between 10% and 40%.

7. The transistor in claim 1, wherein said first gate and said second gate are doped differently.

7. The transistor in claim 1, wherein said first gate and said second gate are doped similarly.

8. An asymmetric strained Fin field effect transistor comprising:
an insulator;
a semiconductor structure on said insulator, wherein said structure includes a central portion and Fins extending from ends of said central portion;
a first gate positioned on a first side of said central portion of said structure;
a strain-inducing layer between said first gate and said first side of said central portion of said silicon structure; and
a second gate on a second side of said central portion of said silicon structure,
wherein said first gate and said second gate are doped differently.

9. The transistor in claim 8, wherein said insulator comprises a buried oxide layer.

10. The transistor in claim 8, wherein said central portion of said silicon structure comprises silicon.

11. The transistor in claim 8, wherein said strain-inducing layer comprises silicon germanium.

12. The transistor in claim 11, wherein said silicon germanium has a sufficient concentration of germanium to produce strain within said central portion to enhance carrier mobility, without producing sufficient dislocations to reduce overall performance of said Fin field effect transistor.

13. The transistor in claim 11, wherein said concentration of germanium is between 10% and 40%.

14. The transistor in claim 8, wherein said Fins comprise source and drain regions.

15. A symmetric strained Fin field effect transistor comprising:
an insulator;
a semiconductor structure on said insulator, wherein said structure comprises a Fin body having a central portion comprising silicon and silicon germanium; and end portions comprising silicon;
a first gate positioned on a first side of said central portion of said silicon structure; and
a second gate on a second side of said central portion of said structure,
wherein said first gate and said second gate are doped similarly.

16. The transistor in claim 15, wherein said insulator comprises a buried oxide layer.

17. The transistor in claim 15, wherein said silicon germanium has a sufficient concentration of germanium to produce strain within said central portion to enhance carrier mobility, without producing sufficient dislocations to reduce overall performance of said Fin field effect transistor.

18. The transistor in claim 17, wherein said concentration of germanium is between 10% and 40%.

19. A method of forming a transistor comprising:
forming a silicon layer on an insulator;
etching a first portion of said silicon layer to create a first opening;
depositing a first gate in sad first opening;
etching a second portion of said silicon layer to create a second opening opposite said first opening, wherein after said etching of said second portion, said silicon layer comprises a silicon structure on said insulator having a central portion and Fins extending from ends of said central portion;
forming a strain-producing layer upon a portion of said silicon structure facing said second opening;
forming a second gate in said second opening; and
removing said first gate and said second gate from all portions of said silicon structure except said central portion.

20. The method in claim 19, further comprising doping said Fins such that said Fins comprise source and drain regions.

21. The method in claim 19, wherein said silicon germanium has a sufficient concentration of germanium to produce strain within said central portion to enhance carrier mobility, without producing sufficient dislocations to reduce overall performance of said Fin field effect transistor.

22. The method in claim 20, wherein said concentration of germanium is between 10% and 40%.

23. A method of forming an asymmetric strained Fin field effect transistor comprising:
forming a silicon layer on an insulator;
etching a first portion of said silicon layer to create a first opening;
depositing a first gate in said first opening;
etching a second portion of said silicon layer to create a second opening opposite said first opening, wherein after said etching of said second portion, said silicon layer comprises a silicon structure on said insulator having a central portion and Fins extending from ends of said central portion;
forming a silicon germanium layer upon a portion of said silicon structure facing said second opening;
forming a second gate in said second opening, wherein said first gate and said second gate are doped differently; and
removing said first gate and said second gate from all portions of said silicon structure except said central portion.

24. The method in claim 23, further comprising doping said Fins such that said Fins comprise source and drain regions.

25. The method in claim 23, wherein said silicon germanium has a sufficient concentration of germanium to produce strain within said central portion to enhance carrier mobility, without producing sufficient dislocations to reduce overall performance of said Fin field effect transistor.

26. The method in claim 24, wherein said concentration of germanium is between 10% and 40%.

27. A method of forming strained Fin field effect transistor comprising:
forming a silicon structure on an insulator;
forming stress on one side of said silicon structure, having a central portion and Fins extending from ends of said central portion;
depositing a first gate and a second gate on sides of said silicon structure; and
removing said first gate and said second gate from all portions of said silicon structure except said central portion.

28. The method in claim 27, wherein said first gate and said second gate are doped similarly.

29. The method in claim 27, wherein said first gate and said second gate are doped differently.

30. The method in claim 28, further comprising doping said Fins such that said Fins comprise source and drain regions.

31. The method in claim 27, wherein said silicon germanium has a sufficient concentration of germanium to produce strain within said central portion to enhance carrier mobility, without producing sufficient dislocations to reduce overall performance of said Fin field effect transistor.

32. The method in claim 31, wherein said concentration of germanium is between 10% and 40%.

33. A method of forming a transistor comprising:
forming a silicon germanium layer on an insulator;
etching said silicon germanium layer to create a central portion and Fins extending from ends of said central portion;
growing a strained silicon layer on said silicon germanium layer;
growing a thermal oxide on said strained silicon layer; and
growing gate conductors on said thermal oxide.

34. The method in claim 33, further comprising doping said Fins such that said Fins comprise source and drain regions.

35. The method in claim 33, wherein said silicon germanium has a sufficient concentration of germanium to produce strain within said strained silicon layer to enhance carrier mobility, without producing sufficient dislocations to reduce overall performance of said transistor.

36. The method in claim 35, wherein said concentration of germanium is between 10% and 40%.

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發明專利說明書

200304703

一、發明名稱	中文	應變鰭式場效電晶體結構及方法
	英文	STRAINED FIN FETS STRUCTURE AND METHOD
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發明專利說明書

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一、本案已向

國家(地區)申請專利	申請日期	案號	主張專利法第二十四條第一項優先權
美國 US	2002/03/19	10/101,807	有

二、□主張專利法第二十五條之一第一項優先權:

申請案號:

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日期:

三、主張本案係符合專利法第二十條第一項□第一款但書或□第二款但書規定之期間

日期:

四、□有關微生物已寄存於國外:

寄存國家:

寄存機構:

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寄存日期:

寄存號碼:

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寄存機構:

寄存日期:

無

寄存號碼:

□熟習該項技術者易於獲得,不須寄存。

五、發明說明（1）

一、【發明所屬之技術領域】

本發明係關於半導體之製造領域，更具體而言，係關於一種形成雙閘極場效電晶體。

二、【先前技術】

半導體元件生產上之成本與性能競爭，導致了積體電路內元件密集度之不斷增長。為加速元件密集度之增長，常常需由新技術達成?少半導體元件之特徵尺寸(feature size)。

元件密集度之增長趨勢，著重體現於互補式金氧半導體（CMOS）技術，如場效應電晶體（FETs）之設計及製造。場效應電晶體幾乎應用於所有類型之積體電路設計中（如，微處理器，記憶體等等）。然而，不幸的是，互補式金氧半導體場效應電晶體（CMOS FETs）上元件密集度的不斷增長，常常導致其性能和/或可靠性之下降。

一種有助於元件密集度的增長之場效應電晶體型式，即為雙閘極場效應電晶體。雙閘極場效應電晶體使用兩閘極，於其主體之每一側各具有一閘極，以便其在保持可接受之性能的前提下，有助於比例縮放CMOS尺寸。具體而言，雙閘極之使用增大了閘極區域，此在未增加元件之閘極長度的前提下，使電晶體具有更佳之電流控制。因此，雙閘極場效應電晶體能進行更大電晶體之電流控制，?並

五、發明說明（2）

不需要更大電晶體之元件空間。

不幸地是，在雙閘極場效應電晶體之設計和製造中發生了一些困難。首先，雙閘極場效應電晶體之相對尺寸關係，使其很難可靠地製造成為具有可靠性能與最小化特徵尺寸的電晶體。其次，雙閘極場效應電晶體之起始電壓很大程度上與兩閘極之材質有關。具體來說，目前的製造技術一般導致雙閘極場效應電晶體，或具有過分高的起始電壓，或具有過分低的起始電壓。例如，若閘極摻雜與源極相同的極性，則起始電壓一般接近於零。相反地，若閘極摻雜與源極相反之極性，則起始電壓近似一伏特。大多數互補式金氧半導體（CMOS）之應用中並不期望有此類結果發生。

因此，提供改良式元件結構及雙閘極場效應電晶體元件之製造方法，用以改善雙閘極場效應電晶體之起始電壓，而不過份增加製造之複雜性是必要的。

場效應電晶體之通道材質上的物理應變可提高載子遷移率(mobility)。平面的p型之金氧半導體場效應電晶體元件上所產生之應變，經顯示電洞遷移率增加且超過30%以上。本發明提供此類優點於垂直安置於基板上的薄型半導體主體，如此，本發明獲得更大的載子遷移率的同時，亦可達到更大之通道控制。

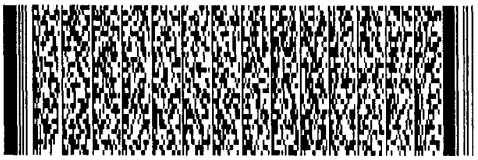
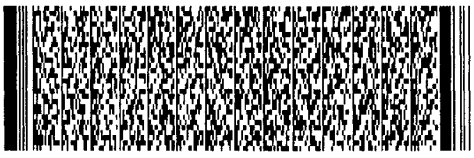
五、發明說明 (3)

三、【發明內容】

非對稱應變鰭式場效電晶體係具有一絕緣體和位於絕緣體上的半導體結構。此結構包括一中心部分及自此中心部分延伸之第一和第二端面。一第一閘極係位於此結構之中心部分之第一側上，一應變產生層(strain-producing layer)係介於第一閘極與此結構之中心部分之第一側之間，且一第二閘極係位於此結構之中心部分之第二側之上。絕緣層係為一埋氧化層(buried oxide layer)，而此結構之中心部分係為矽。應變產生層具有足夠的鍺濃度，在不產生足夠之差排降低電晶體整體性能的條件下，於中心部分內產生應變，以提高載子遷移率。第一和第二端分別為源極和汲極區域。而鍺濃度係介於10%與40%之間。不同之閘極可以不同的方式摻雜，以調節起始電壓(VT)。閘極亦可以相同的方式摻雜。

對稱應變鰭式場效電晶體係具有一絕緣體和位於絕緣體上的半導體結構。此結構係為一鰭式主體，其具有含矽和矽化鍺的中心部分及含矽的端部。一第一閘極係位於矽結構之中心部分的第一側上，而一第二閘極係位於矽結構之中心部分的第二側上。第一和第二閘極可再度以相同的方式或不同的方式摻雜（類似於非對稱應變情形）。

形成電晶體之方法係包含於絕緣層上形成一矽層，蝕

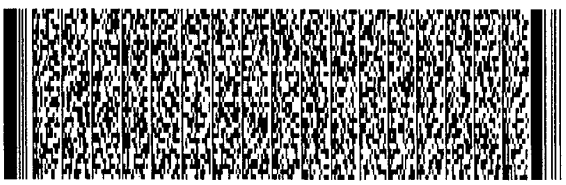



五、發明說明（4）

刻此矽層之第一部分，以形成一第一開口。於此第一開口內沈積第一閘極，且蝕刻此矽層之第二部分，以形成相對於第一開口之一第二開口。蝕刻此第二部分後，此矽層係包含位於絕緣層上的一矽結構，且此矽結構具有一中心部分和以自該中心部分之複數個端延伸之複數個鰭。本發明係於面對第二開口之部分矽結構上形成一應變產生層。於第二開口內形成一第二閘極，且自矽結構除中心部分外之所有部分，去除第一和第二閘極。

形成非對稱應變鰭式場效電晶體之方法包括於絕緣層上形成一矽層，蝕刻此矽層之第一部分，以形成一第一開口。於此第一開口內沈積一第一閘極，蝕刻此矽層之第二部分，以形成相對第一開口之一第二開口。蝕刻第二部分後，此矽層包含位於絕緣層上的一矽結構，此矽結構係具有一中心部分及以自中心部分之複數個端延伸之複數個鰭。本發明於面對第二開口之部分矽結構上形成一矽化鍺層。於第二開口內，形成以不同或相同於第一閘極之摻雜方式的一之第二閘極，且自此矽結構除中心部分外之所有部分，去除此第一和第二閘極。

形成應變鰭式場效電晶體之方法包含於絕緣層上形成一矽結構，形成應力（stress）於矽結構之一側或兩側上。此矽結構具有一中心部分及以自中心部分之複數個端延伸之複數個鰭。於矽結構之側邊上沈積一第一閘極和一



五、發明說明 (5)

第二閘極，且自此矽結構除中心部分外之所有部分，去除第一閘極和第二閘極。

於場效電晶體之通道材質上的物理應變，可提高載子遷移率。平面p型之金氧半導體場效電晶體元件上所產生的應變，經顯示其電洞遷移率已增加且超過30%。本發明於垂直方式設置於基板上的薄半導體主體提供此類優點，且因此，本發明係於達成更大載子遷移率的同時，亦獲得了更大的通道控制。

四、【實施方式】

本發明係關於增強型之鰭式場效電晶體元件，且使應變建立於此類元件內。本發明使用"鰭式"型("Fin" type)場效應雙閘極結構加以實施。此鰭式場效應電晶體型結構中，雙閘極係形成於此主體之每一側邊上，且此主體水平設置於閘極之間。本發明提供之鰭式場效電晶體透過矽化鍺層之運作，而使其通道主體受應變。製程過程係於一晶圓上開始進行，可能地經結合，以包含底部之一矽主體晶圓(silicon bulk wafer)、相對較厚之底部氧化層和頂部之疏鬆（relaxed）矽化鍺層。薄形鰭則在矽化鍺層上蝕刻出來，且停止於埋氧化層（BOX）層上。一磊晶矽薄層則成長於此鰭上。由於矽和矽化鍺之矽晶格常數有所不同，故磊晶矽層將在應變的條件下成長。本發明可包括具有對稱或非對稱閘極功函數的鰭式場效電晶體。

五、發明說明（6）

本發明以上所述係針對非對稱應變鰭式場效電晶體而言，但亦可同等應用於對稱之應變鰭式場效電晶體。具體而言，如圖29-31所示，本發明第二實施例之形成對稱應變鰭式場效電晶體之製程中，其係以絕緣層10上方具有矽化鍺層300之矽絕緣層結構(SOI)上開始進行（圖29所示）。矽化鍺層300係選擇性地進行圖案化，如圖30所示。接著，在矽化鍺層300上成長一矽層315，以形成應變結構。熱氧化層320則成長於矽層315上。隨後，閘極導體310（如多晶矽）被沈積，平坦化且圖案化，以形成圍繞此主體結構155之閘極。於一實施例中，閘極導體310係具有相同之摻雜濃度和材質構成。然而，另一實施例中，閘極電極310可以如離子植入的方式，非對稱地加以形成，以便產生具有非對稱閘極功函數且帶有應變之鰭式場效電晶體。具體而言，非對稱閘極之設置中，其閘極導體310可具有不同之摻雜濃度或可利用不同之摻雜物。此製程一直進行，直至完成如上所述且如圖18-28所示之結構。

本發明之一重要特徵在於，其於許多不同形式之鰭式場效電晶體內提供應變。如圖1-28所示，應變鰭式場效電晶體之一實施例係利用絕緣體上具有矽（SOI）之結構的設置，以形成具有對稱或非對稱閘極導體之應變鰭式場效電晶體。或者，亦可參考圖15之說明，若略去氧化層150，則形成一動態起始之鰭式場效電晶體(dynamic

五、發明說明 (7)

threshold FinFET)。相反地，圖29-31所示之實施例係利用絕緣層上覆蓋矽化鍺（SiGe-OI）的結構，用以替代圖1-28所示之絕緣層上具有矽(SOI)之結構。同樣方式下，此SiGe-OI之結構依據閘極導體之摻雜，可形成非對稱閘極或對稱閘極結構。以上實施例僅用以說明本發明，而本發明並非局限於此些具體實施例。相反地，以上所述之實施例只作為例子而已，熟此技藝者應該理解的是，各種不同類型之鰭式場效電晶體可藉由包含本發明之應變結構，以達成所述之優點。

本發明之第一實施例中，鰭式場效電晶體之形成過程如圖1-28所示。如圖1所示，開始進行製程過程。此處，絕緣層上具有矽（SOI）之結構包括如埋氧化層之一絕緣層10，且其為一矽層11覆蓋。矽層11上沈積一佔位層12（placeholder layer，如氮化層等）。此結構則使用習知之傳統圖案化製程，進行圖案化，如圖2所示，以去除佔位層12之一部分20。而後續之蝕刻步驟，則去除未被佔位層12所保護之矽層11之任何對應的部分30，如圖3所示。

圖4中，氧化過程係於矽層11上成長一閘極氧化層40。接著，多晶矽50則被沈積於此結構上，如圖5所示。多晶矽50係為一種摻雜質類型（如，N+摻雜之多晶矽等）。圖6中，使用例如化學機械研磨(chemical

五、發明說明 (8)

mechanical polishing)製程，平坦化此結構，以便形成平坦層60。圖7顯示一氧化製程，於其中此經摻雜之多晶矽層50以更快於佔位材質層12的速率，加以氧化。因此，多晶矽50上之氧化層70較佔位層12上之氧化層71為厚。

氧化層70、71以可控制之速率加以蝕刻，如圖8所示。一旦佔位層12被暴露，則停止蝕刻製程。此去除自佔位層12之上表面之所有氧化物，而同時保留一些多晶矽層上的氧化物70。接著，圖9中，佔位層12藉使用一選擇性蝕刻製程加以去除之，而使矽層11之上部分90暴露。

圖10中，一硬遮罩100（如TEOS等等），係共形地沈積於此結構之上層上。接著，如圖11所示，使用一方向性之非等向蝕刻製程，以去除所有水平表面110之硬遮罩100，並使此硬遮罩100保留於多晶矽50和氧化層70之垂直表面上。圖12中，圖案化矽層11，以去除120部分。此圖案化過程後，僅硬遮罩100之下方部分留存下來。

圖13係示意選擇性矽化鍺層130之成長。此例中應用了矽化鍺層，但本發明並不局限於此種材料組合。任何若與矽呈現晶格失配而產生應變之材質，亦可用於本發明中。更具體而言，此結構在含有鍺之複合物(complex)內加熱，使得矽化鍺130自矽層11成長。此使已成型之矽通道11內建立了應變。成效後之矽層，由於矽化鍺與更小晶

五、發明說明 (9)

格常數的矽層之間的晶格失配而受到應變。場效電晶體之通道材料上的物理應變，則可提高載子遷移率。平面p型之金氧半導體場效電晶體上所產生之應變，經顯示可提高其電洞遷移率且達30%以上。這是因為應變分離了導帶與價帶，且提高低遷移率橢圓體(ellipsoid)之能量，因而可將其電洞減少。

同時，若鍺過量，則會產生不恰當之差排，導致元件性能之降低。發明者發現最佳鍺濃度之範圍係介於10%至40%之間。

傳統之平面元件藉使用淺溝渠隔離（STI）技術，產生應變。然而，鰭式場效電晶體中，並沒有類似淺溝渠隔離之製程，而由埋氧化層10（BOX）提供元件隔離。本發明藉使用矽化鍺（SiGe）和矽側壁薄膜，以於鰭式場效電晶體之通道上產生應變的方式來克服上述之問題。

圖14中，自多晶矽50之上表面141去除氧化層70。此亦可降低硬遮罩層100之高度142，且於絕緣體10內形成階梯140。另一熱氧化步驟，係於矽化鍺130之表面上形成氧化層150，如圖15所示。或者，亦可略去氧化層150的形成，以便形成動態起始鰭式場效電晶體。於未包含有氧化層150之實施例中（此即為動態起始（DT）鰭式場效電晶體），則應變鰭式場效電晶體之動態起始CMOS元件形成

五、發明說明（10）

後，其主體係連接閘極。此結構以下將其稱作為"主體"，且圖中為簡化描述和說明，而標示為符號155，其包括矽層11，閘極氧化層40，硬遮罩層100，氧化層150和矽化鍺130。

接著，圖16中，第二多晶矽160可以不同或相同於第一多晶矽50之方式摻雜，係沈積於整個結構上。此結構將再次被平坦化，形成平坦的上表面170，如圖17所示。倘若第一多晶矽50為N+摻雜之多晶矽，則第二多晶矽160較佳為P+多晶矽。然而，對於對稱閘極元件而言，第一和第二多晶矽可為相同。兩種類型之多晶矽可互相替代，或亦可替代為目前所知或將來研發之其他類型。重點在於，對非對稱結構而言，位於主體155之相對側之多晶矽區域50、160係以不同之方式摻雜。多晶矽50、160可為鍺摻雜或其他導體。經不同方式摻雜之多晶矽係設置於矽通道結構11之相對兩側上時，則為非對稱閘極鰭式場效電晶體。

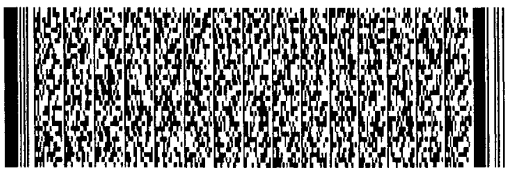
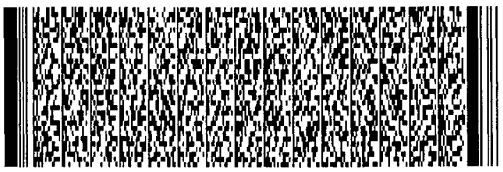
各種導電材料係與內建的電位有關，電位常為費米能階(Fermi level)，即其與外部供應電壓相連，用以確定以電子（或電洞）為導體之相對親合力(affinity)。在金屬中，費米能階係為材質所固有，而半導體中，如矽材質，費米能階可藉由引入不純物之方式提供過量電洞或電子，使費米能階之值可調節於價帶與導電帶之間。而在非對稱之雙極閘極鰭式場效電晶體中，兩個閘極電極50、

五、發明說明（11）

160摻雜相反之極性，以一閘極摻雜N型，而另一閘極摻雜P型。因此，兩個閘極電極50、160具有不同之費米能階，因而，一閘極電極（強閘極，n型場效電晶體為n閘極）對反轉載子(inversion carrier)具有較大之親和力。而另一電極（弱閘極，n型場效電晶體為p閘極）對反轉載子則具有較小之親和力。因此，反轉通道將在半導體主體內，接近"強"閘極處形成。因而，兩個閘極電極都促使反轉電位形成，其導致一相對低的起始電壓（如，介於0伏與0.5伏之間）。

以下說明及所述之實施例中，此結構為非對稱之鰭式場效電晶體元件，矽層(silicon layer)11僅在一側30上加以蝕刻，而位於餘下之矽層11上方的佔位層12則被適當地保留下來。本發明係於暴露之一半鰭結構之上方（於閘極氧化層之相對側上），成長選擇性單晶矽化鍺層130。然而，本發明亦可應用於對稱之鰭式場效電晶體，如下文所述。

製程繼續進行，如圖18所示，其以沈積或成長一本徵矽層180。接著，圖19中，另一絕緣硬遮罩190（如TEOS等）係沈積於本徵矽層18上，且藉使用傳統圖案化技術加以圖案化，以去除部分200，如圖20所示。相同之結構參見圖21所示之透視圖。多晶矽電極50，160和本徵矽層180係使用硬遮罩190，以進行圖案化，如圖22所示（且可參

五、發明說明（12）

考圖23之透視圖）。硬遮罩層190則從區域220中加以去除，如圖24所示。閘極50，160之圖案化較佳為，去除掉所有的閘極多晶矽，直至到達埋氧化層10，且使用方向性蝕刻，其對氮化層或氧化層具有選擇性，以完成圖案化。因此，此圖案化未去除由先前形成之硬遮罩100所保護之部分主體155。圖案化係保留了部分之多晶矽50和部分之多晶矽160，此定義為雙閘極電晶體之兩個閘極。進行一緩衝氟化氫(HF)清潔製程，接著熱氧化，以於所有暴露之矽表面層上成長氧化層。此較佳為形成一氧化層薄膜（50埃），其用以在閘極接觸主體時，提供良好之介面。

本發明接著進行電晶體內，熟知且傳統之源極，汲極和環（halo）之植入。較佳為，此些植入由暴露之部分主體155（即鰭250）所有的四個方向植入，以確保均勻植入此主體之兩側。具體來說，源極和汲極之植入係從主體155之鰭250之兩側進行。接著，進行另一植入，此植入以不同之植入能量和角度進行，以於主體155內形成環（halo）植入，以改善短通道效應。環植入係以更高之能量和與鰭250相關之更小之銳角進行，以確保環摻雜較源極/汲極摻雜更位於閘極電極50，160之下方。

接著，本發明沈積一介電層240，其厚度大於所組合之閘極電極50，160和硬遮罩層232之高度，且其覆蓋了整個閘極電極50，160和暴露之鰭250，如圖25所示。此介電

五、發明說明 (13)

層然後被平坦化，且部分加以凹化，直至部分之硬遮罩232和閘極電極50，160被暴露，而不暴露任何源極/汲極之鰭區，如圖25所示。圖26中，介電層240被加以蝕刻，以僅僅覆蓋閘極電極50，160之側邊，且側壁間隙壁242形成於介電層240上方之閘極邊上。而進行此製程之較佳為，於共形(conformal)沈積介電材料後，進行方向性蝕刻。側壁間隙壁242較佳為由氮化物形成。介電層240，側壁間隙壁242和硬遮罩層232係用於遮罩一方向性蝕刻，且隨後去除氧化層40，150，並保留鄰接閘極的區域。硬遮罩層232，側壁間隙壁242和側壁部分240係組合以有效地自源極及汲極250和接觸280隔離閘極50，160，如圖27所示。較佳為，此源極和汲極接觸280係包含一圖案化導電材料。接著，如圖28所示，本徵矽層180藉使用傳統且熟知之金屬矽化製程，形成金屬矽化層(silicide)230。

圖32係為概述本發明之第一實施例之一流程圖表。首先，步驟320中，本發明於絕緣層10上形成矽層11。其次，步驟321中，本發明產生第一開口30。步驟322中，本發明於此矽層11上成長第一氧化層40。接著，步驟323中，本發明於第一開口內沈積第一閘極50。步驟324中，本發明蝕刻矽層11，以形成具有中心部分和鰭之矽結構155。本發明於步驟325中，形成一應變產生層130。接著，步驟326中，本發明於應變產生層130上成長第二氧化層150。步驟327中，本發明在第二開口140內形成第二閘

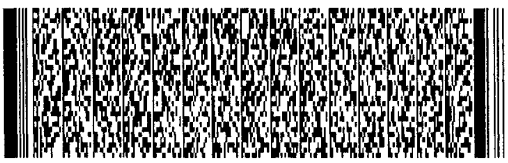
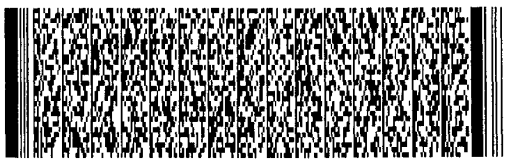
五、發明說明（14）

極160。然後，步驟328中，本發明自矽結構除中心部分外之所有部分，去除此第一閘極和第二閘極。步驟329中，本發明摻雜鰭250，使得鰭250包含源極和汲極區域。最後，步驟330中，本發明於源極和汲極區域上，形成源極和汲極接觸280。

操作中，閘極50，160內的電壓，則改變由閘極50，160覆蓋之半導體矽層11之區域的導電能力。此操作可進行，或可中斷源極和汲極鰭250之間的電連接。因此，此元件可作為一種電開關，以執行邏輯操作。

如上所述，本發明之一重要特徵為，矽化鍺層130係保留下來，以作為主體155之一永久部分。更具體而言，此特徵使應變形成於矽通道11。場效電晶體內之通道材料之物理應變，可提高載子遷移率。

本發明以上所述係針對非對稱應變鰭式場效電晶體，而此亦可同等應用於對稱應變鰭式場效電晶體。更具體而言，如圖29-31，本發明第二實施例形成應變對稱鰭式場效電晶體之製程中，其係以絕緣層10之上具有矽化鍺層300之SOI結構上開始形成（圖29所示）。矽化鍺層300係選擇性地加以圖案化，如圖30所示。接著，矽層315成長於矽化鍺層300上，以形成一應變結構。而熱氧化層320則成長於矽層315上。接著，閘極導體310（如多晶矽）被沈

五、發明說明 (15)

積，平坦化且圖案化，以形成圍繞主體結構155之閘極。一實施例中，閘極導體310係具有相同之摻雜濃度和材料構成。然而，另一不同之實施例中，閘極電極310可以如離子植入的方式非對稱地加以設置，形成帶有應變之非對稱閘極功函數鰭式場效電晶體。更具體而言，非對稱閘極之設置中，閘極導體310可具有不同之摻雜濃度，或利用不同之摻雜物。如上所述，製程一直進行，直至如圖18-28所示之結構完成。

本發明之一重要特徵在於，其於各種不同形式之鰭式場效電晶體內提供應變。圖1-28所示為應變鰭式場效電晶體之一實施例，其係利用SOI結構設置，以形成具對稱或非對稱閘極導體之應變鰭式場效電晶體。或者，參考圖15之說明，如略去氧化層150，則形成動態起始鰭式場效電晶體。相反地，圖29-31所示之實施例，係利用SiGe-OI（絕緣層上具有矽化鍺）代替如圖1-28所示之SOI結構。同樣的方式下，SiGe-OI結構根據閘極導體之摻雜，可形成非對稱或對稱閘極結構。以上之實施例僅示意性地說明本發明，且本發明並不局限於此些具體實施例。相反地，以上所示之實施例僅作為例子而已，熟此技藝者應該理解的是，許多不同類型之鰭式場效電晶體可藉由包含本發明之應變結構，而達成所欲之益處。

圖33係為本發明第二實施例形成對稱應變鰭式場效電

五、發明說明（16）

晶體之流程圖表。首先，步驟331中，此方法於絕緣層10上形成矽化鍺層300。接著，步驟332中，此方法蝕刻一矽化鍺層，以形成具有中心部分和複數個鰭250之矽結構。步驟333中，此方法係於矽結構300上成長一氧化層320。步驟334，此方法於矽結構之側邊上沈積閘極。接著，步驟336中，此方法自矽結構除中心部分外之所有部分，去除第一閘極和第二閘極。步驟337中，此方法摻雜鰭250，使得鰭250係為源極和汲極區域。最後，步驟338中，此方法於源極和汲極區域之上方，形成源極和汲極接觸280。

如上所述，矽化鍺層130住入應變於已成形之矽通道11內。場效電晶體內通道材料上之物理應變，可提高其載子遷移率。平面p型之金氧半導體場效電晶體元件所產生之應變經顯示，其遷移率提高且達至30%。本發明提供此些優點給垂直設置於基板上之薄半導主體。如此，本發明可達成更大之載子遷移率的同時，亦獲得了更大之通道控制。

當本發明以較佳實施例加以描述，熟此技藝者應該意識到的是，本發明可於所附申請專利範圍之精神與範疇內做修改。例如，當本發明以一具體方法形成垂直半導體主體時，亦可使用其他於基板上產生分離半導體主體之方法（如，SOI基板上之矽島）。而且，矽化鍺雖作為基本材料，亦可使用其他之材料，以於通道區域內產生必要之應

五、發明說明 (17)

變。最後，本發明可應用於其他半導體中（例如，諸如砷化鎵之Ⅲ-Ⅴ族半導體）。

圖式簡單說明

五、【圖示簡單說明】

本發明之前述和其他目的、優點及特徵清楚地指明於下述之較佳實施例之詳細說明和圖示部分：

圖1-20、22、24和25係為使用本發明第一實施例之方法所產生之第一實施例之場效電晶體之截面示意圖；

圖21、23和26-28係為使用本發明第一實施例之方法所產生之第一實施例之場效電晶體之透視圖；

圖29-31係為使用本發明第二實施例之方法所產生之第二實施例之場效電晶體之截面示意圖；

圖32係為本發明之第一實施例之步驟流程圖；及

圖33係為本發明之第二實施例之步驟流程圖。

圖示元件符號說明

10	絕緣層	11	矽層
12	佔位層	20	部分之佔位層
30	矽層之相應部分	40	閘極氧化層
50	閘極	60	平坦層
70	氧化層	71	氧化層
90	矽層之上部分	100	硬遮罩
110	硬遮罩之水平表面	120	部分
130	矽化鍺層	140	階梯
141	多晶矽之上表面	150	第二氧化層
155	主體結構	160	第二多晶矽
170	平坦的上表面	180	本徵矽層

圖式簡單說明

190 絕緣硬遮罩	200 部分
220 區域	230 金屬矽化層
240 介電層	242 側壁間隙壁
250 鰭	280 源極和汲極接觸
300 矽化鍺層	310 閘極導體
315 矽層	320 熱氧化層

四、中文發明摘要 （發明名稱：應變鰭式場效電晶體結構及方法）

一種電晶體結構及方法，其包括一絕緣層和位於此絕緣層上的一矽結構。此矽結構包括一中心部分及自此中心部分延伸之複數個鰭。一第一閘極係位於此矽結構之中心部分之第一側上。一應變產生層可位於第一閘極與此矽結構之中心部分之第一側之間，且一第二閘極係位於此矽結構之中心部分之第二側上。

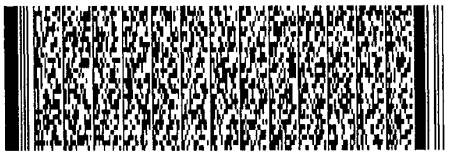
五、（一）、本案代表圖為：圖 28

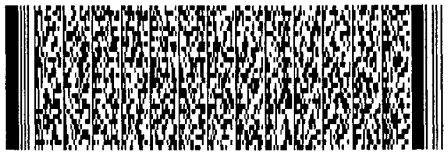
（二）、本案代表圖之元件代表符號簡單說明：

10	絕緣層	50	閘極
155	主體結構	160	第二多晶矽
230	金屬矽化層		

六、英文發明摘要 （發明名稱：STRAINED FIN FETS STRUCTURE AND METHOD）

A method and structure for a transistor that includes an insulator and a silicon structure on the insulator. The silicon structure includes a central portion and Fins extending from ends of the central portion. A first gate is positioned on a first side of the central portion of the silicon structure. A strain-producing layer could be between the first gate and the first side of





四、中文發明摘要　（發明名稱：應變鰭式場效電晶體結構及方法）

六、英文發明摘要　（發明名稱：STRAINED FIN FETS STRUCTURE AND METHOD）

the central portion of the silicon structure and a second gate is on a second side of the central portion of the silicon structure.



六、申請專利範圍

1. 一種電晶體包含：

一絕緣層；

一半導體結構，係位於該絕緣層上，其中該結構包括一中心部分，及自該中心部分延伸之一第一端和一第二端；

一第一閘極，係位於該結構之該中心部分之一第一側上；

一應變產生層，係介於該第一閘極與該結構之中心部分之第一側之間；以及

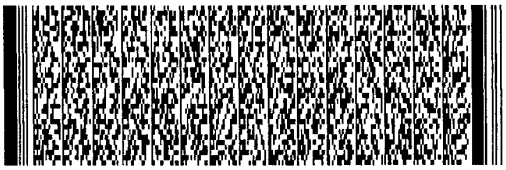
一第二閘極，係位於該結構之中心部分之一第二側上。

2. 如申請專利範圍第1項所述之電晶體，其中該絕緣層包含一埋氧化層。

3. 如申請專利範圍第1項所述之電晶體，其中該結構之中心部分係包含矽。

4. 如申請專利範圍第1項所述之電晶體，其中該應變產生層具有一充分之鍺濃度，且於未產生充分之差排，降低該電晶體整體性能的條件下，於該中心部分內產生應變，以提高載子遷移率。

5. 如申請專利範圍第1項所述之電晶體，其中該第一端和



六、申請專利範圍

第二端分別包含源極和汲極區域。

6. 如申請專利範圍第4項所述之電晶體，其中該鍺濃度係介於10%與40%之間。

7. 如申請專利範圍第1項所述之電晶體，其中該第一閘極和該第二閘極係不同地摻雜。

8. 如申請專利範圍第1項所述之電晶體，其中該第一閘極和該第二閘極係相同地摻雜。

9. 一種非對稱應變鰭式場效電晶體，包含：

一絕緣層；

一半導體結構，係位於該絕緣層上，其中該結構包括一中心部分和複數個鰭，該複數個鰭以自該中心部分之複數個端處延伸；

一第一閘極，係位於該結構之中心部分之一第一側上；

一應變產生層，係介於該第一閘極與該矽結構之中心部分之第一側之間；以及

一第二閘極，係位於該矽結構之中心部分之一第二側上；

其中該第一閘極和第二閘極係不同地摻雜。

六、申請專利範圍

10. 如申請專利範圍第9項所述之電晶體，其中該絕緣層包含一埋氧化層。

11. 如申請專利範圍第9項所述之電晶體，其中該矽結構之中心部分係包含矽。

12. 如申請專利範圍第9項所述之電晶體，其中該應變產生層係包含矽化鍺。

13. 如申請專利範圍第12項所述之電晶體，其中該矽化鍺具有一充分之鍺濃度，且於未產生充分之差排，降低該鰭式場效電晶體之整體性能的條件下，於該中心部分內產生應變，以提高載子遷移率。

14. 如申請專利範圍第13項所述之電晶體，其中該鍺濃度係介於10%與40%之間。

15. 如申請專利範圍第9項所述之電晶體，其中該複數個鰭包含源極和汲極區域。

16. 一種對稱之應變鰭式場效電晶體，包含：

一絕緣層；

一半導體結構，係位於該絕緣層上，其中該結構包括一鰭主體和複數個端部分，該鰭主體具有含矽和矽化鍺之

六、申請專利範圍

一中心部分，該複數個端部分係包含矽；

一第一閘極，係位於該矽結構之中心部分之一第一側上；及

一第二閘極，係位於該矽結構之中心部分之一第二側上；

其中該第一閘極和第二閘極係相同地摻雜。

17. 如申請專利範圍第16項所述之電晶體，其中該絕緣層包含一埋氧化層。

18. 如申請專利範圍第16項所述之電晶體，其中該矽化鍺具有一充分之鍺濃度，且於未產生充分之差排，降低該鰭式場效電晶體之整體性能的條件下，於該中心部分內產生應變，以提高載子遷移率。

19. 如申請專利範圍第18項所述之電晶體，其中該鍺濃度係介於10%與40%之間。

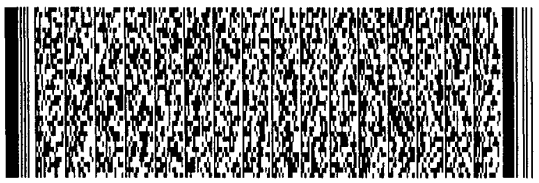
20. 一種形成一電晶體之方法，包含：

形成一矽層於一絕緣層上；

蝕刻該矽層之一第一部分，以形成一第一開口；

沈積一第一閘極於該第一開口內；

蝕刻該矽層之一第二部分，以形成相對於該第一開口之一第二開口，其中蝕刻該第二部分後，該矽層包含一矽



六、申請專利範圍

結構，該矽結構係位於該絕緣層上，且具有一中心部分和自該中心部分之複數個端延伸之複數個鰭；

形成一應變產生層於面對該第二開口之該矽結構之一部分；

形成一第二閘極於該第二開口內；及

自該矽結構除該中心部分外之所有部分，去除該第一閘極和該第二閘極。

21. 如申請專利範圍第20項所述之方法，進一步包含摻雜該複數個鰭，使得該些鰭包含源極和汲極區域。

22. 如申請專利範圍第20項所述之方法，其中該矽化鍺具有一充分之鍺濃度，且於未產生充分之差排，降低該鰭式場效電晶體之整體性能的條件下，於該中心部分內產生應變，以提高載子遷移率。

23. 如申請專利範圍第22項所述之方法，其中該鍺濃度係介於10%與40%之間。

24. 一種形成一非對稱應變鰭式場效電晶體之方法包含：

形成一矽層於一絕緣層上；

蝕刻該矽層之一第一部分，以形成一第一開口；

沈積一第一閘極於該第一開口內；

蝕刻該矽層之一第二部分，以形成相對於該第一開口

六、申請專利範圍

之一第二開口，其中蝕刻該第二部分後，該矽層包含一矽結構，該矽結構係位於該絕緣層上，且具有一中心部分及自該中心部分之複數個端延伸之複數個鰭；

形成一矽化鍺層於面對該第二開口之該矽結構之一部分上；

形成一第二閘極於該第二開口內，其中該第一閘極和該第二閘極係不同地摻雜；及

自該矽結構除該中心部分外之所有部分，去除該第一閘極和該第二閘極。

25. 如申請專利範圍第24項所述之方法，進一步包含摻雜該複數個鰭，使得該些鰭包含源極和汲極區域。

26. 如申請專利範圍第24項所述之方法，其中該矽化鍺具有一充分之鍺濃度，且於未產生充分之差排，降低該鰭式場效電晶體之整體性能的條件下，於該中心部分內產生應變，以提高載子遷移率。

27. 如申請專利範圍第26項所述之方法，其中該鍺濃度係介於10%與40%之間。

28. 一種形成應變鰭式場效電晶體之方法包含：

形成一矽結構於一絕緣層上；

於該矽結構之一側邊上形成應力（stress），該矽結

六、申請專利範圍

構具有一中心部分及以自該中心部分之複數個端延伸之複數個鰭；

沈積一第一閘極和一第二閘極於該矽結構之複數個側上；及

自該矽結構除該中心部分外之所有部分，去除該第一閘極和該第二閘極。

29. 如申請專利範圍第28項所述之方法，其中該第一閘極和第二閘極係相同地摻雜。

30. 如申請專利範圍第28項所述之方法，其中該第一閘極和第二閘極係不同地摻雜。

31. 如申請專利範圍第29項所述之方法，進一步包含摻雜該複數個鰭，使得該些鰭包含源極和汲極區域。

32. 如申請專利範圍第28項所述之方法，其中該矽化鍺具有一充分之鍺濃度，且於未產生充分之差排，降低該鰭式場效電晶體之整體性能的條件下，於該中心部分內產生應變，以提高載子遷移率。

33. 如申請專利範圍第32項所述之方法，其中該鍺濃度係介於10%與40%之間。

六、申請專利範圍

34. 一種形成一電晶體之方法，包含：

形成一矽化鍺層於一絕緣層上；

蝕刻該矽化鍺層，以形成一中心部分及以自該中心部分之複數個端延伸之複數個鰭；

成長一應變矽層於該矽化鍺層上；

成長一熱氧化層於該應變矽層上；及

成長複數個閘極導體於該熱氧化層上。

35. 如申請專利範圍第34項所述之方法，進一步包含摻雜該複數個鰭，使得該些鰭包含源極和汲極區域。

36. 如申請專利範圍第34項所述之方法，其中該矽化鍺具有一充分之鍺濃度，且於未產生充分之差排，降低該電晶體之整體性能的條件下，於該中心部分內產生應變，以提高載子遷移率。

37. 如申請專利範圍第36項所述之方法，其中該鍺濃度係介於10%與40%之間。

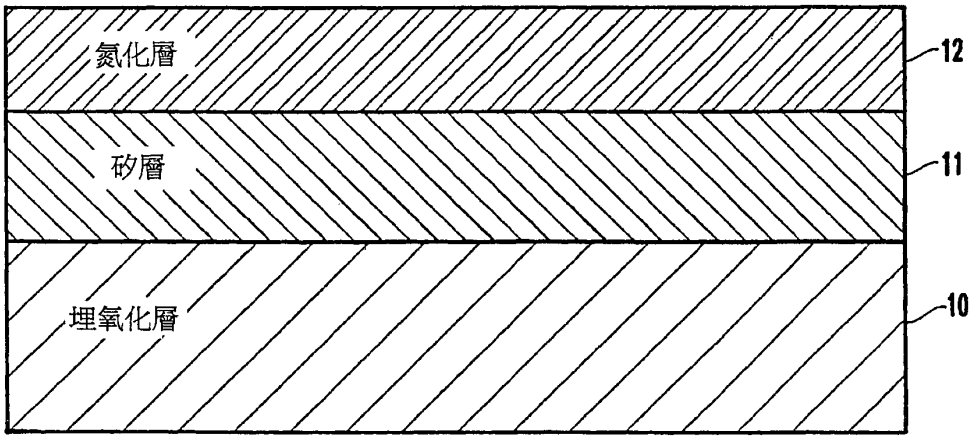


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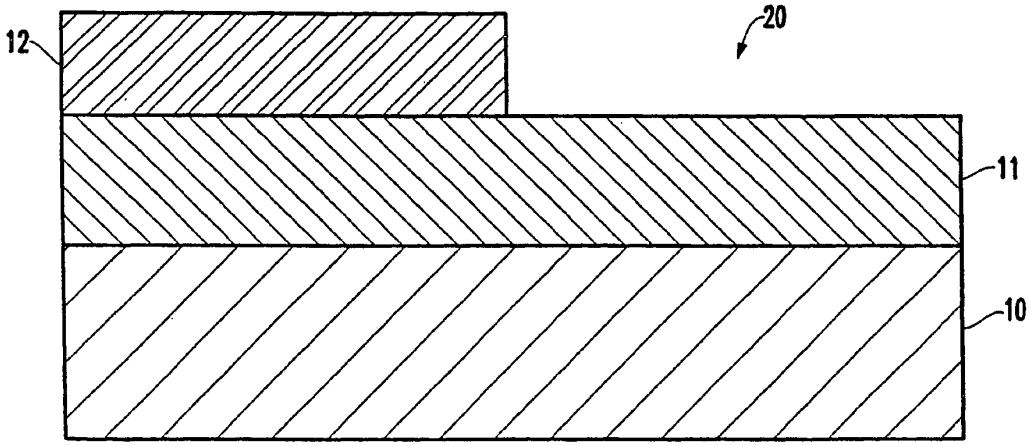


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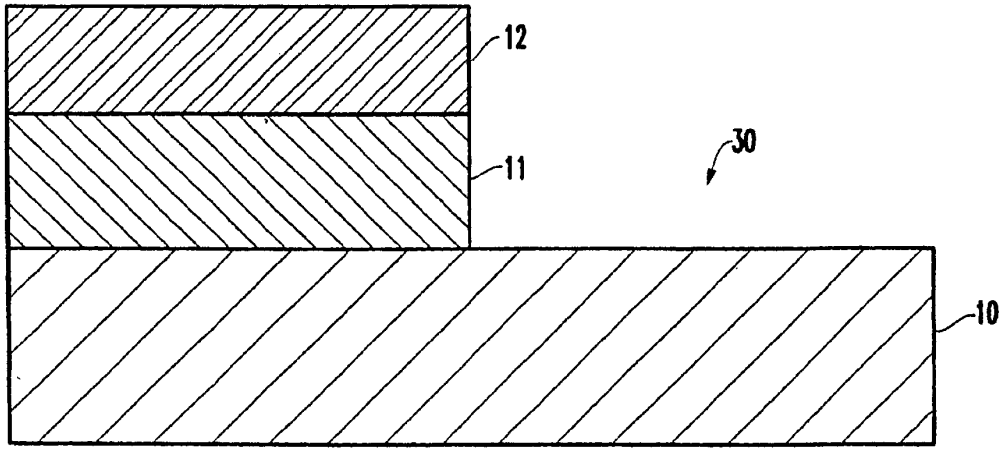


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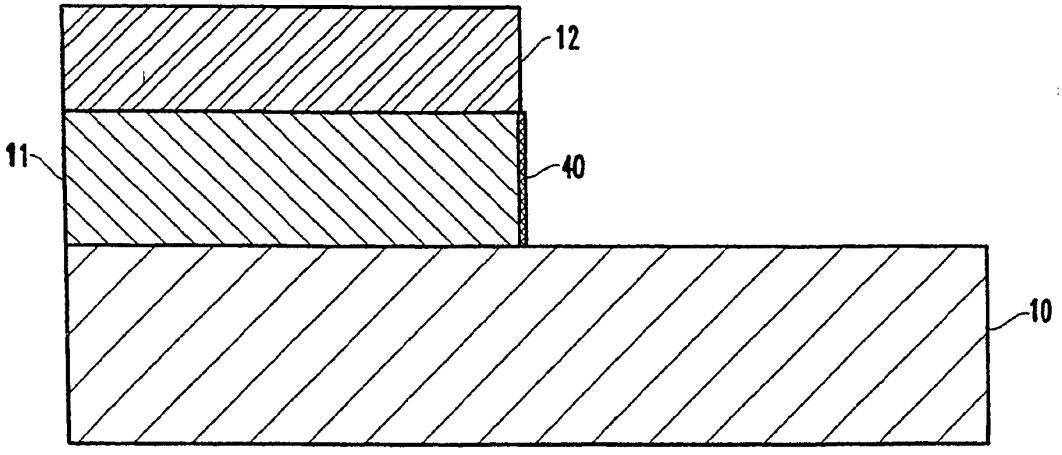


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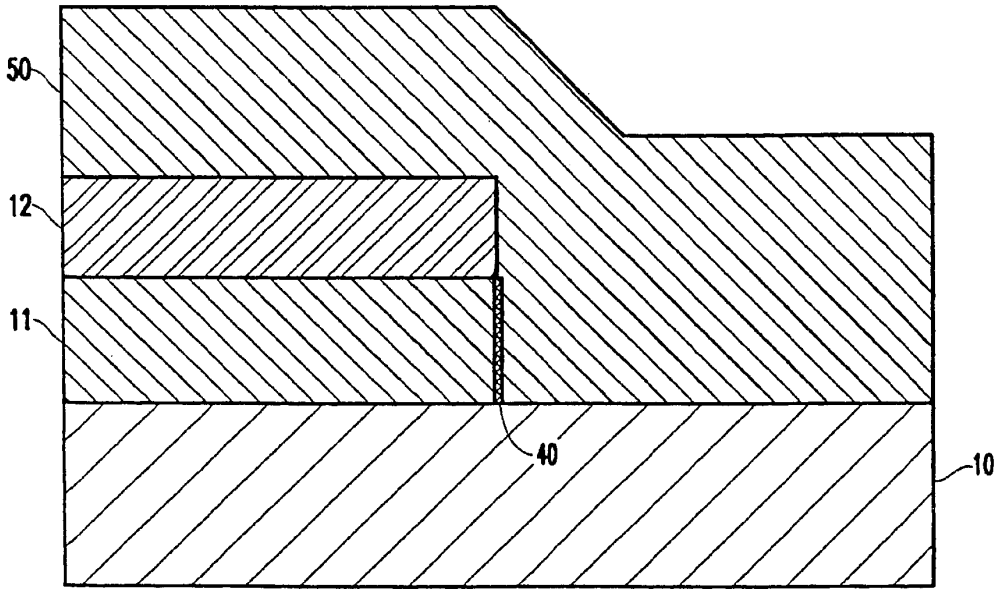


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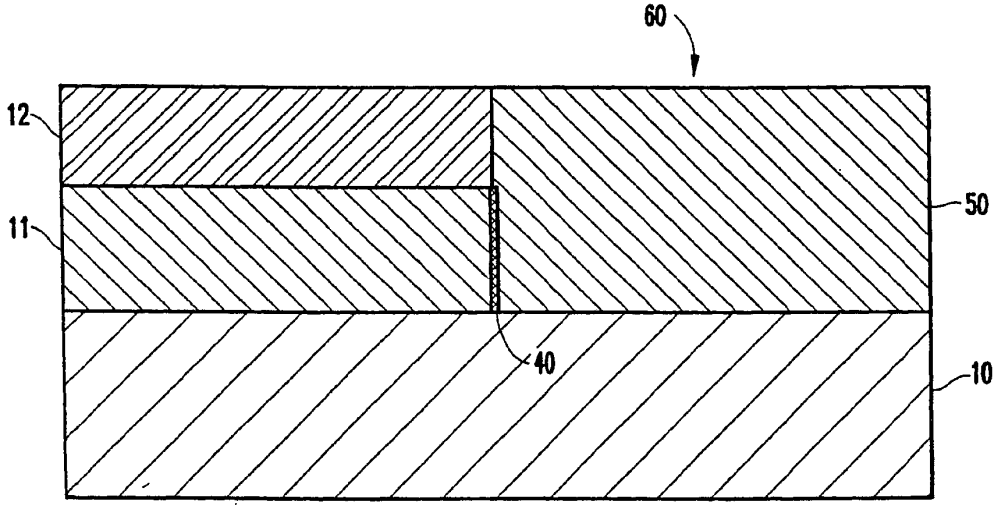


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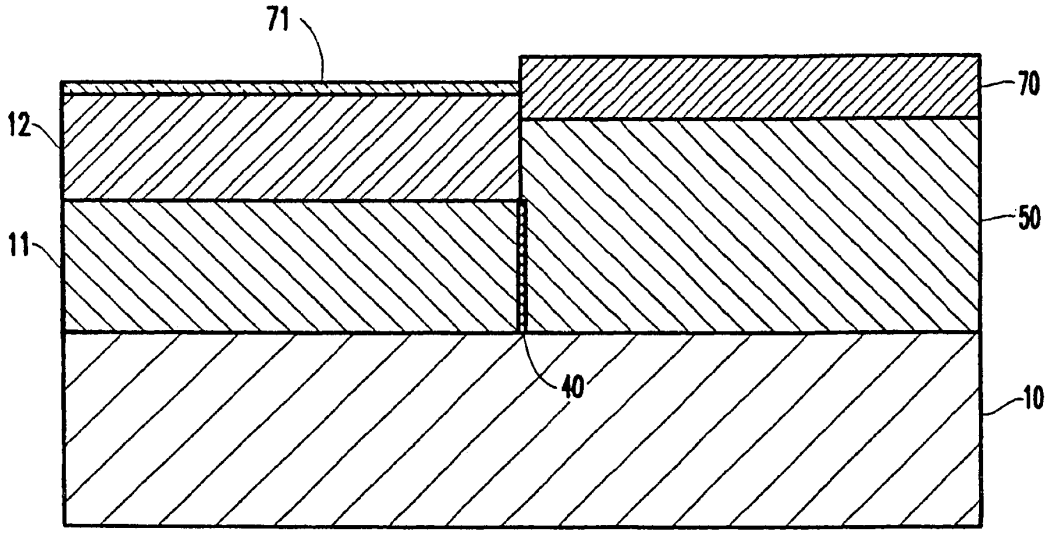


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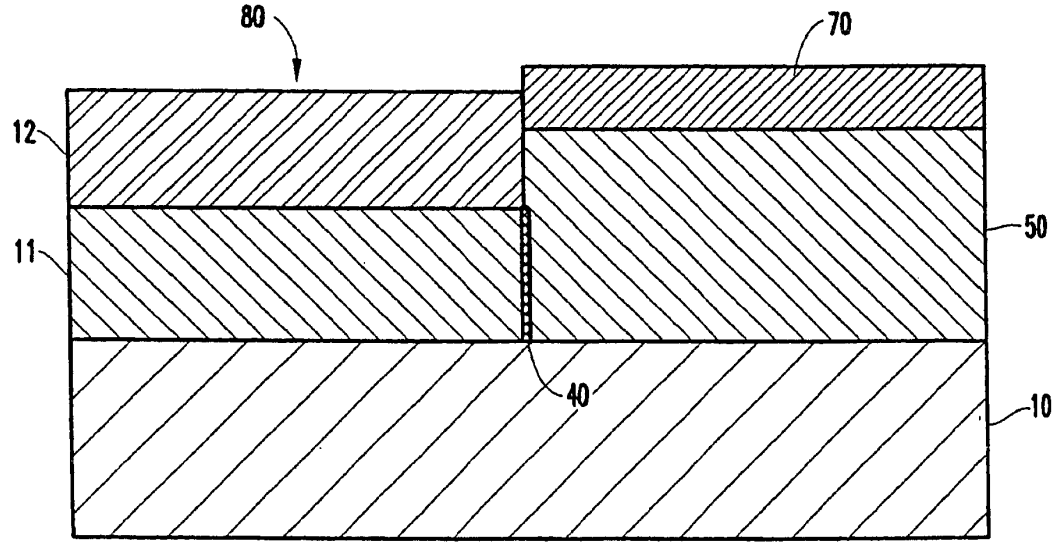


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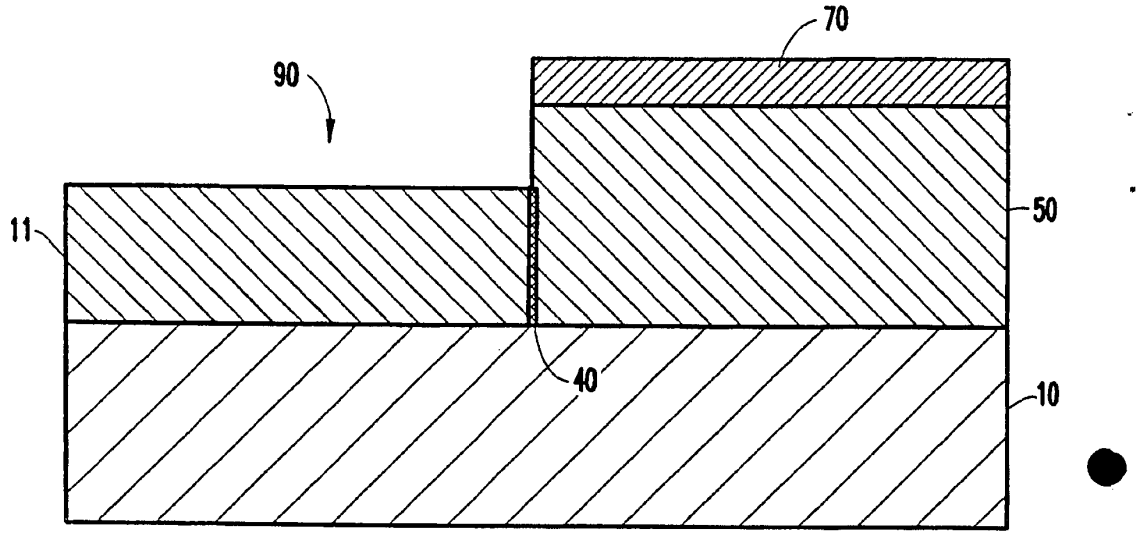


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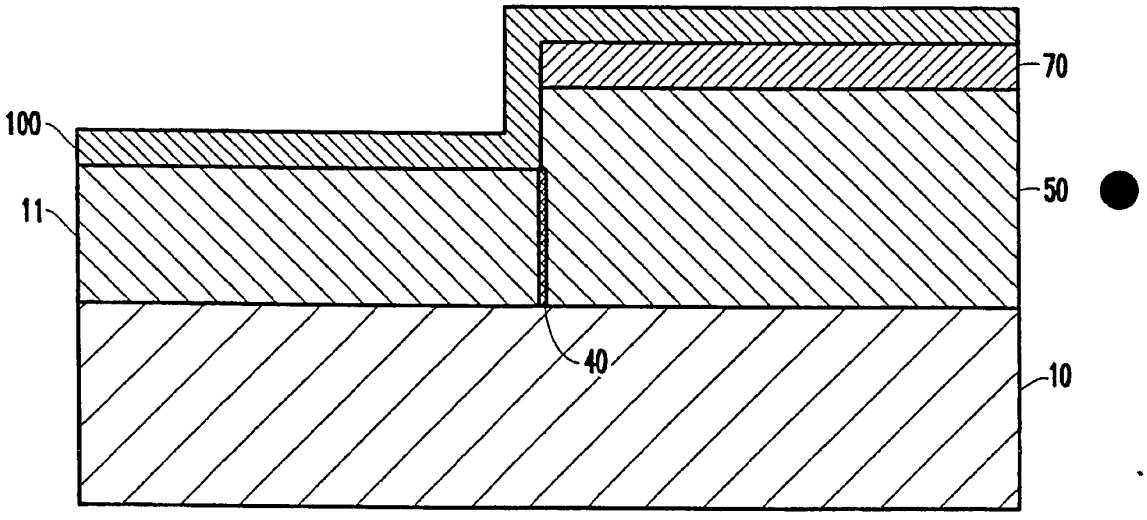


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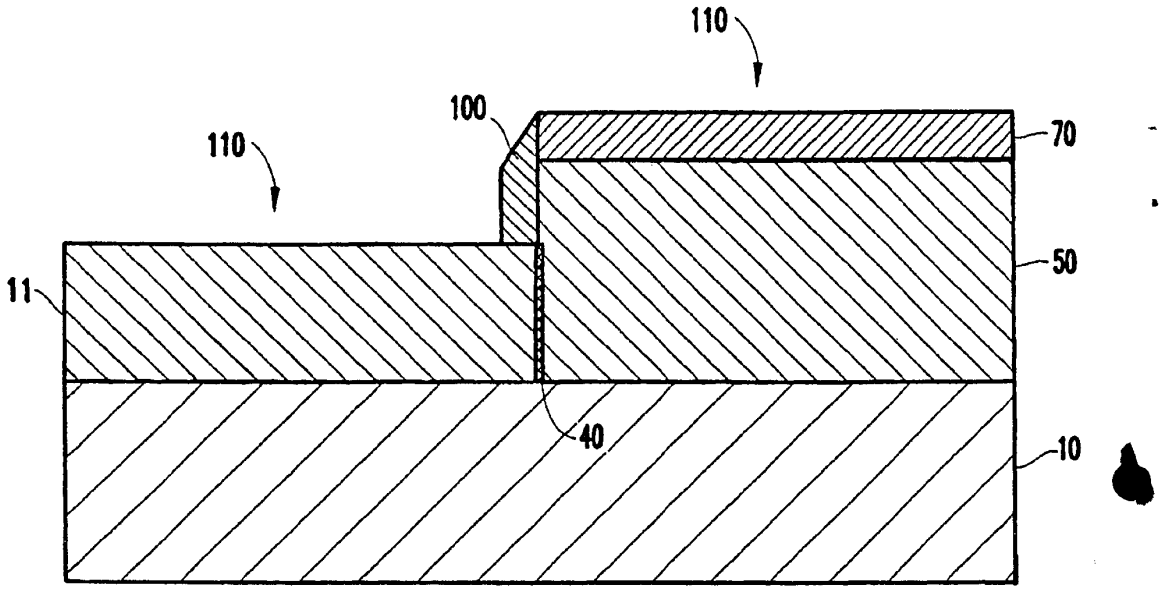


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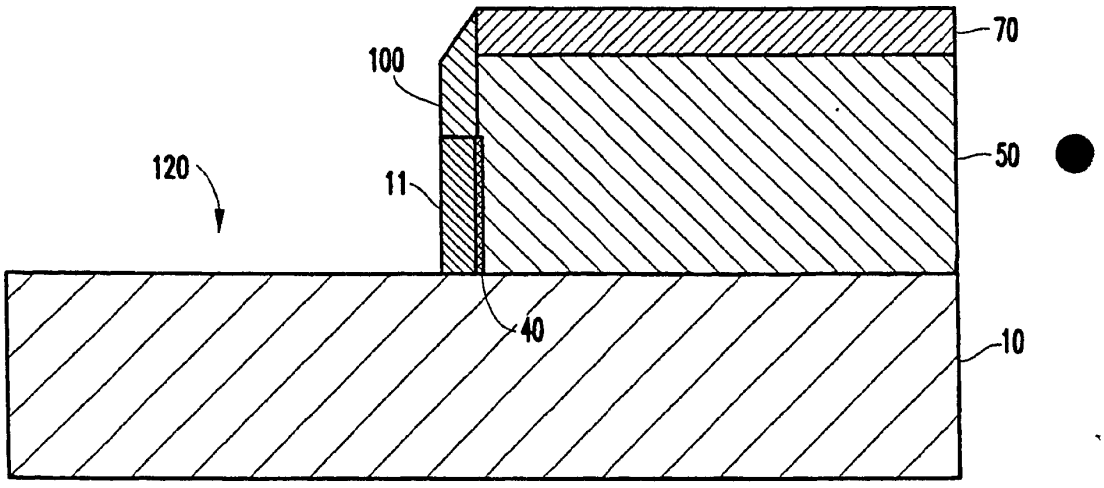


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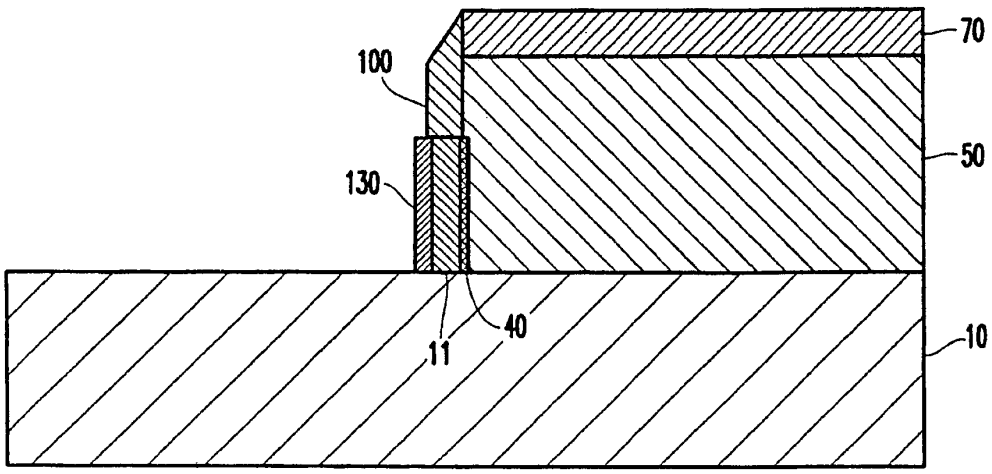


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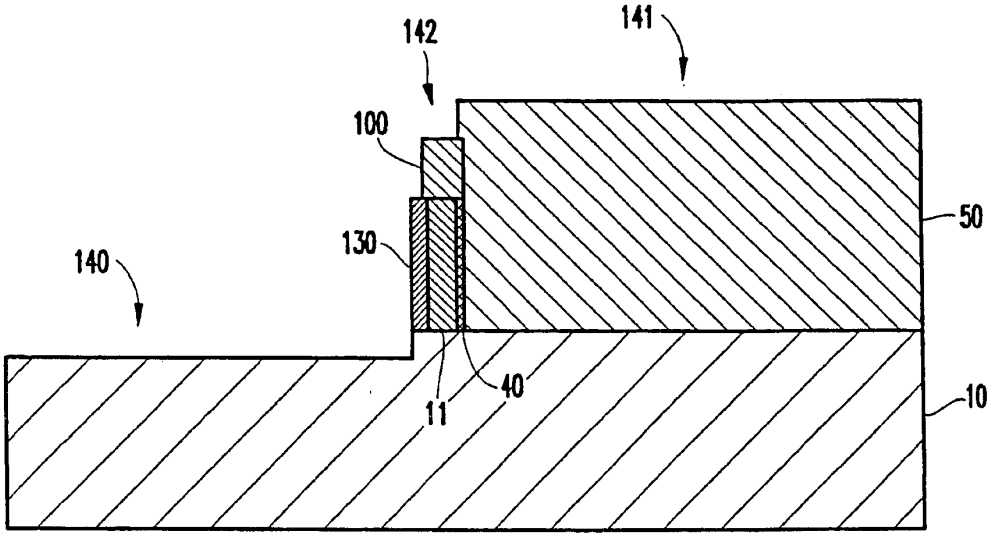


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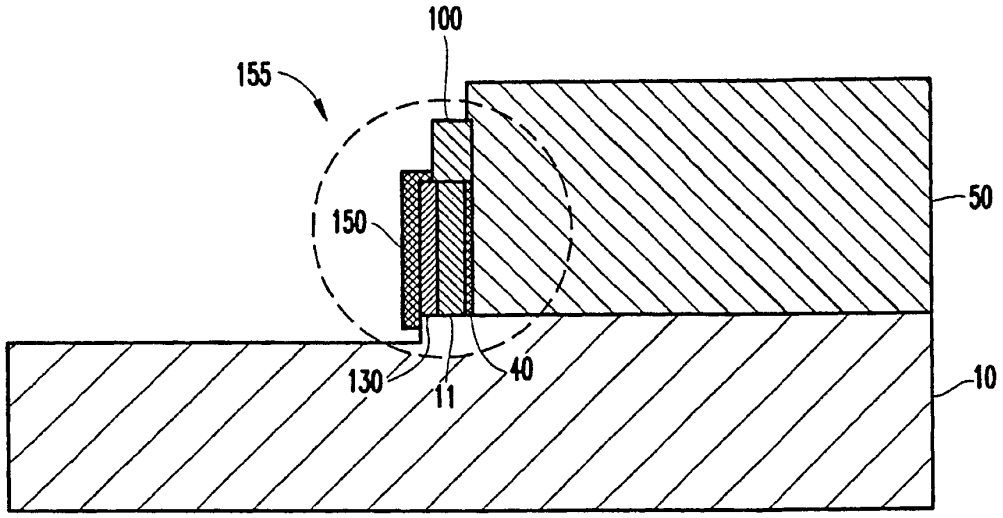


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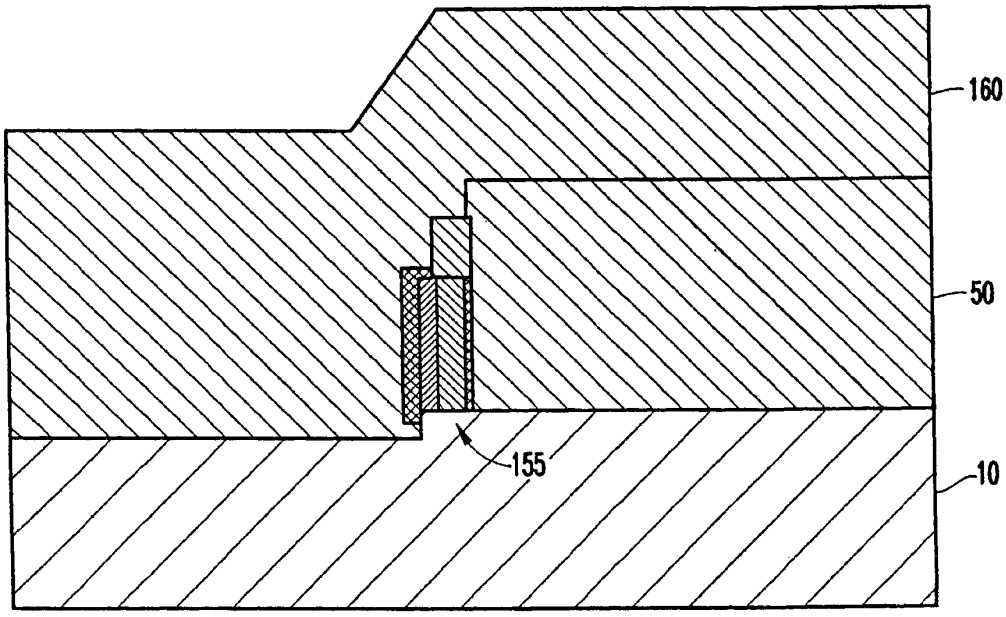


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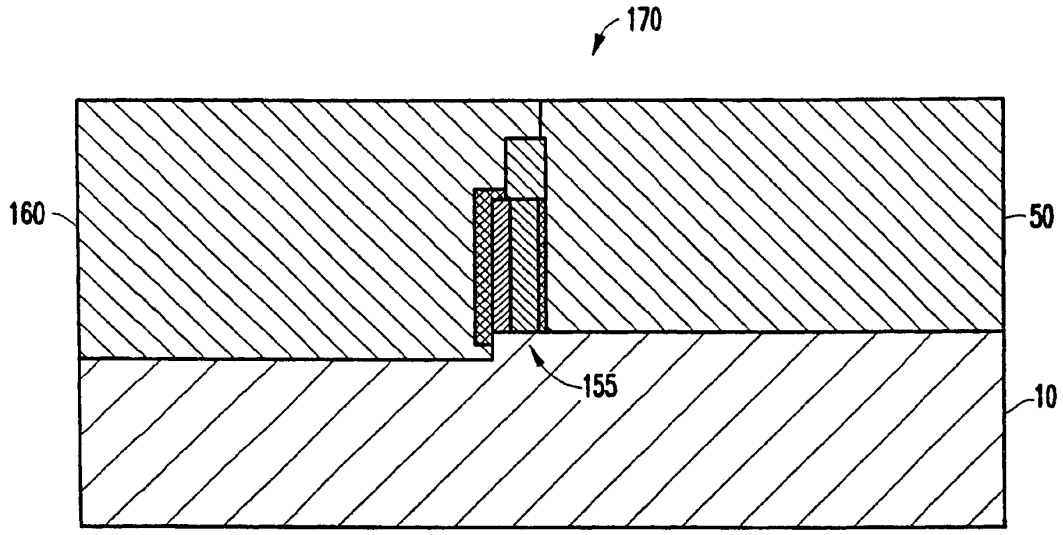


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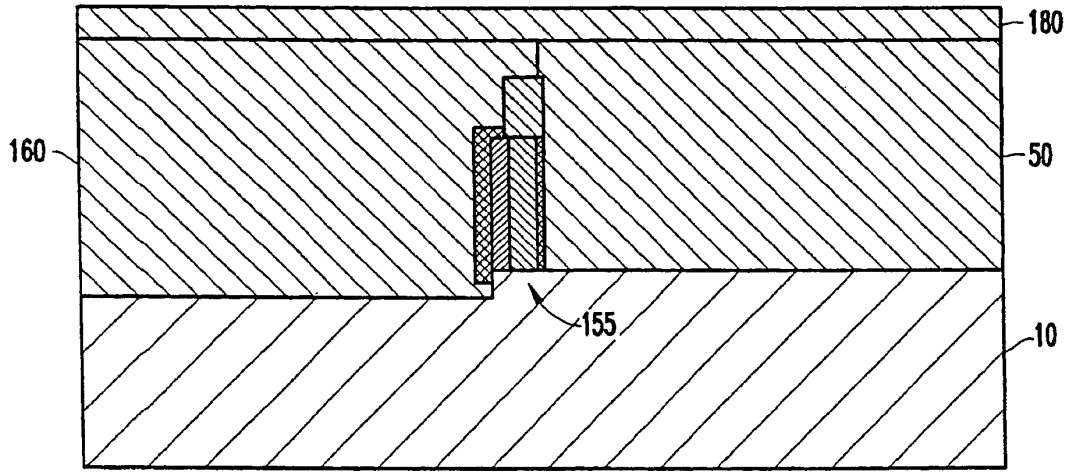


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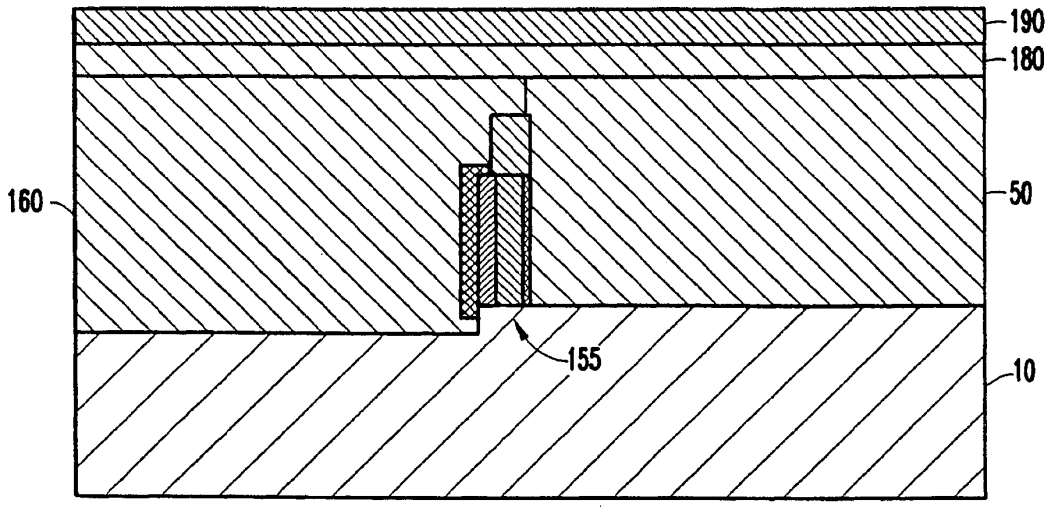


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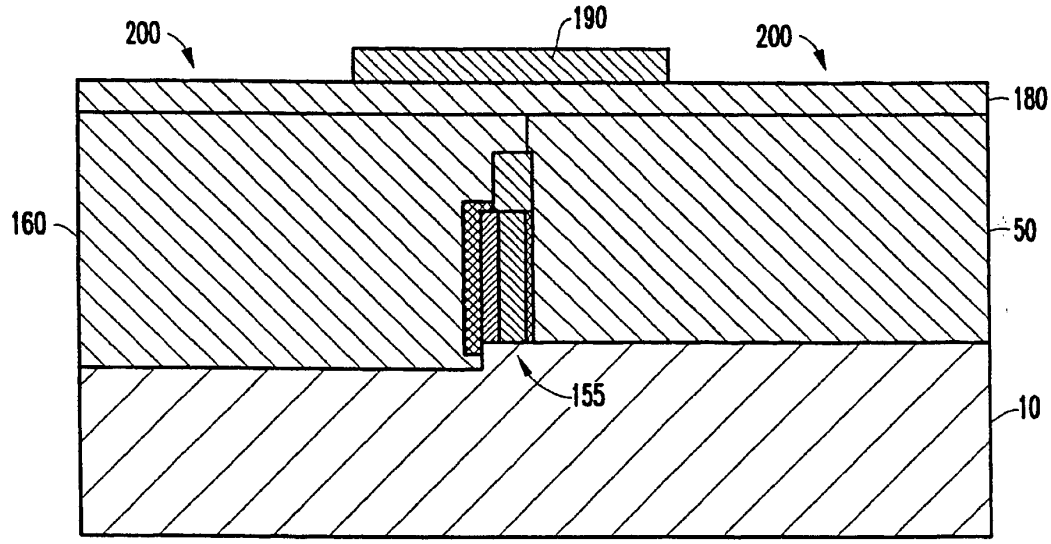


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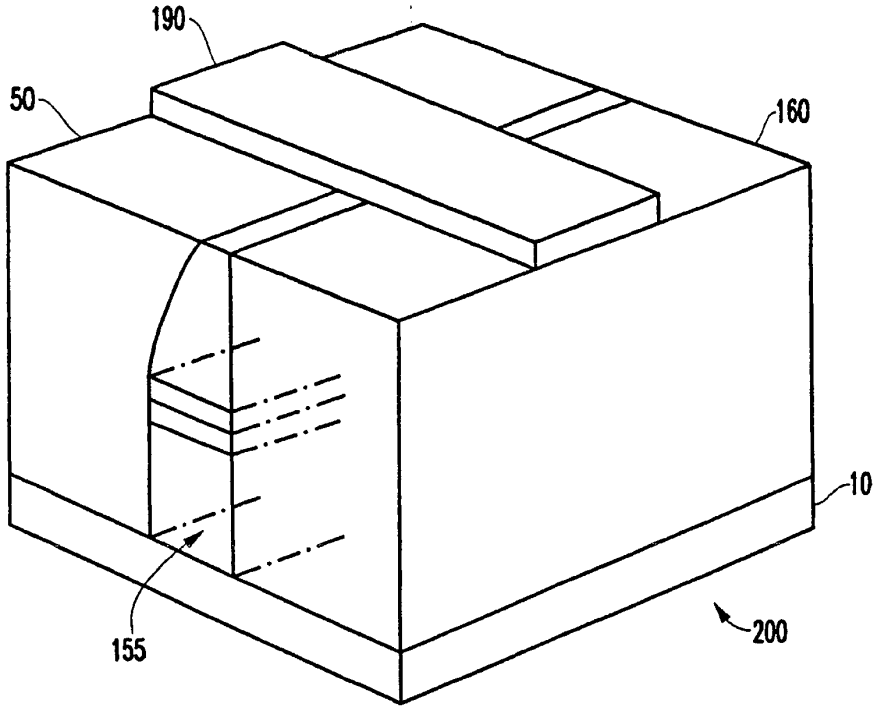


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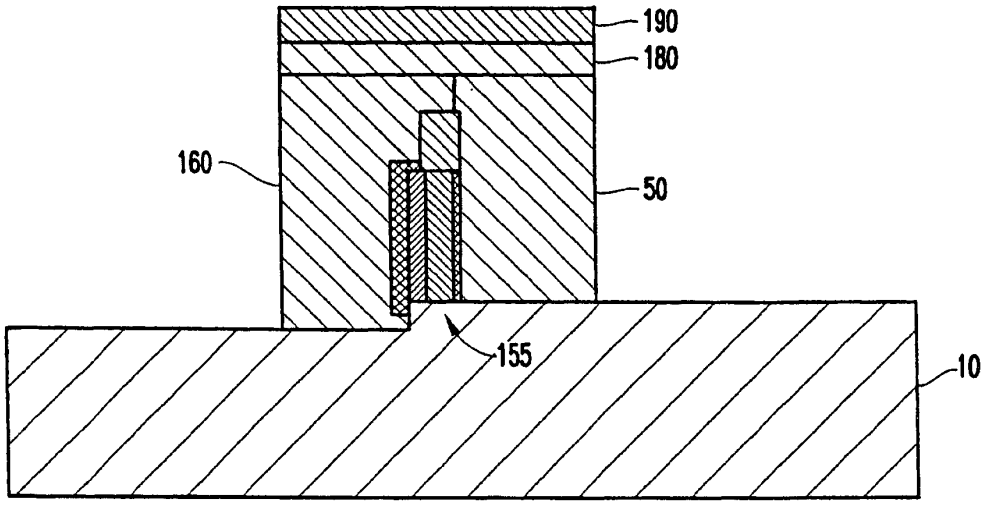


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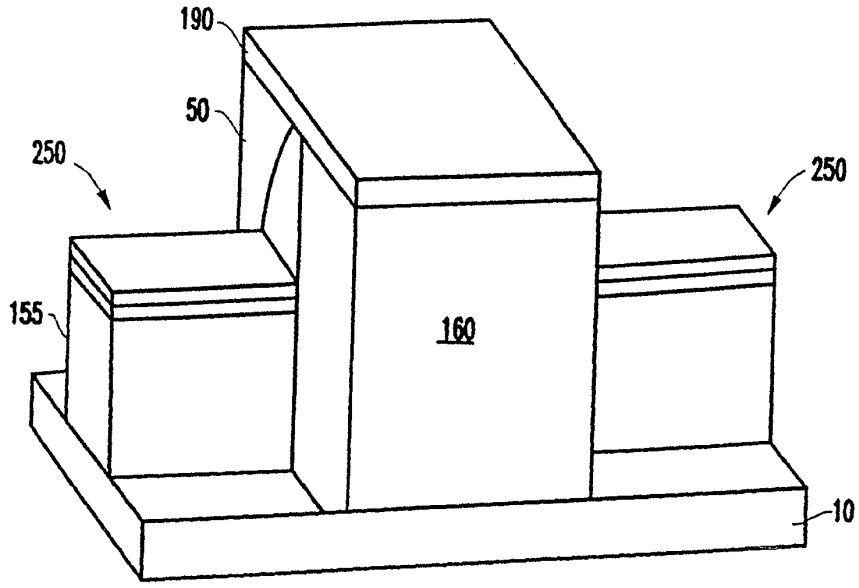


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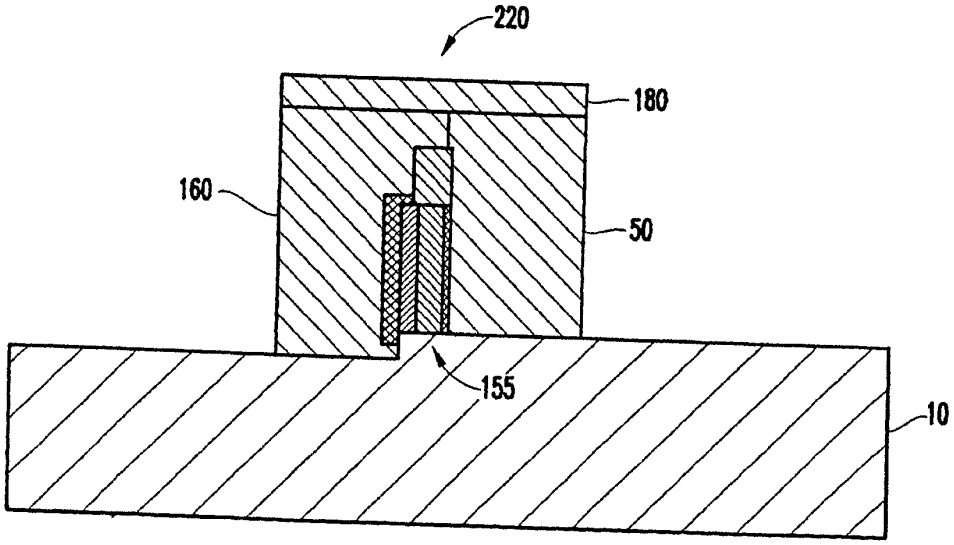


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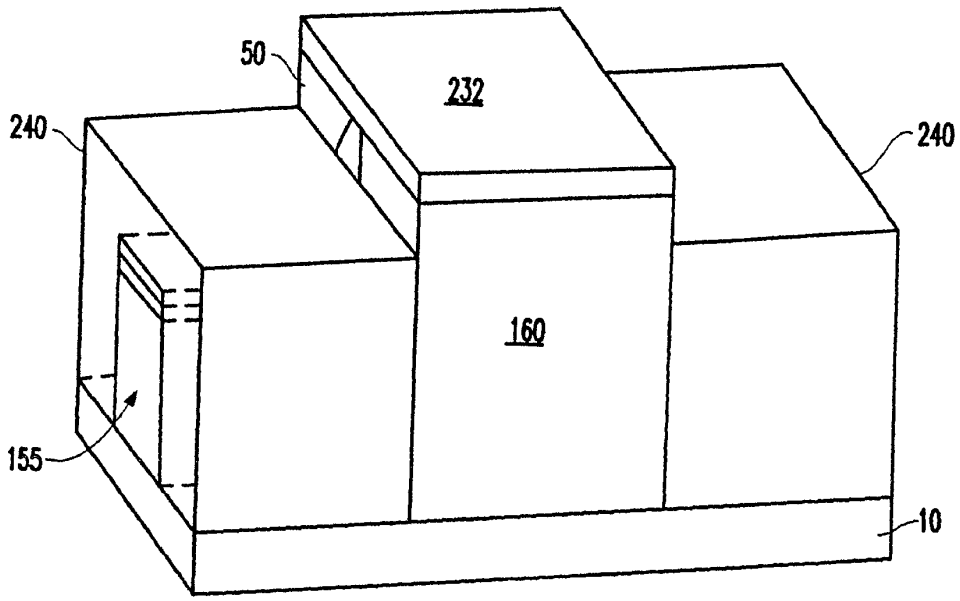


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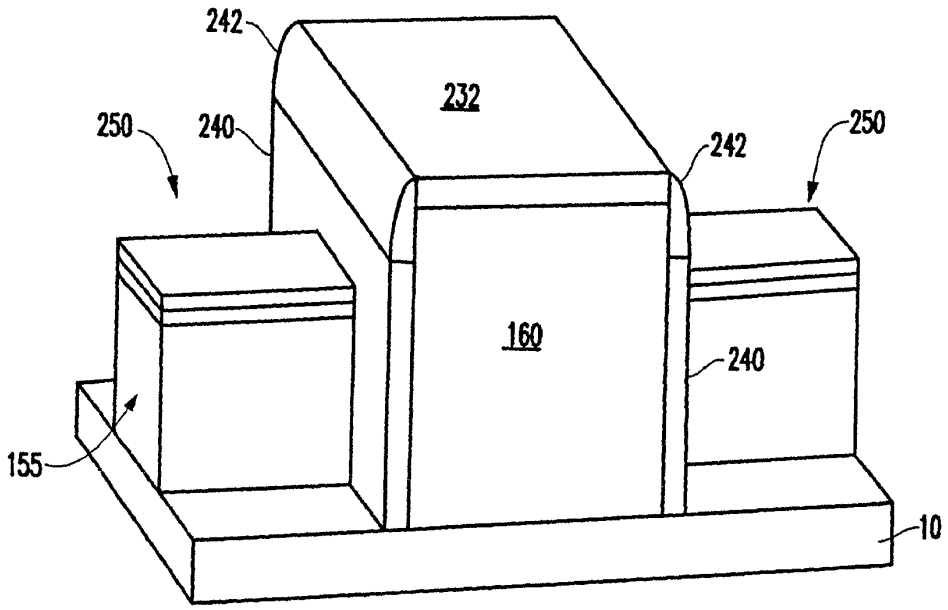


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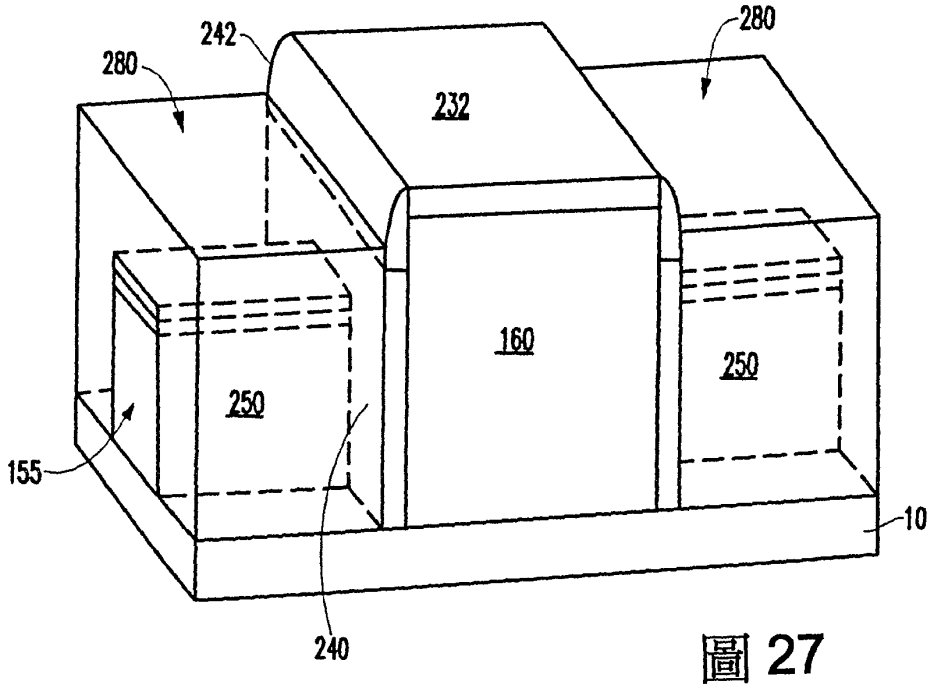


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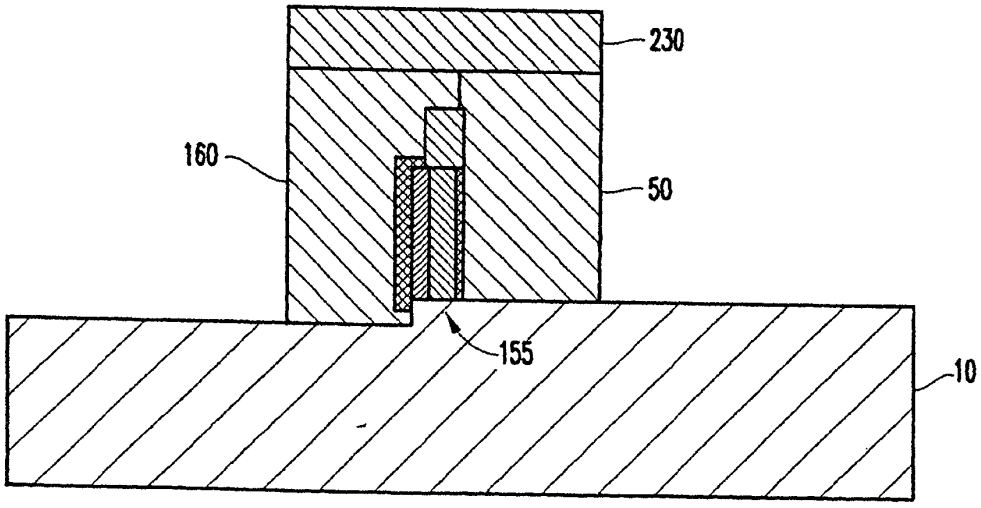


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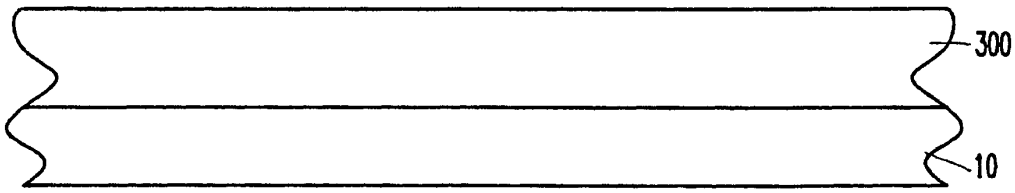


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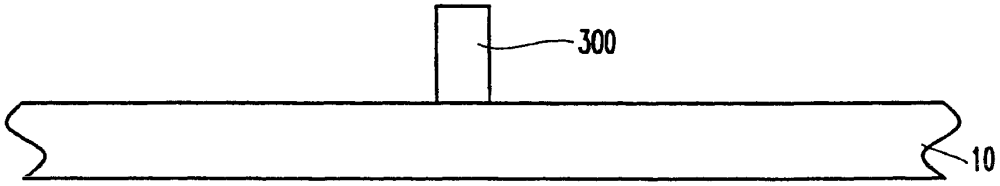


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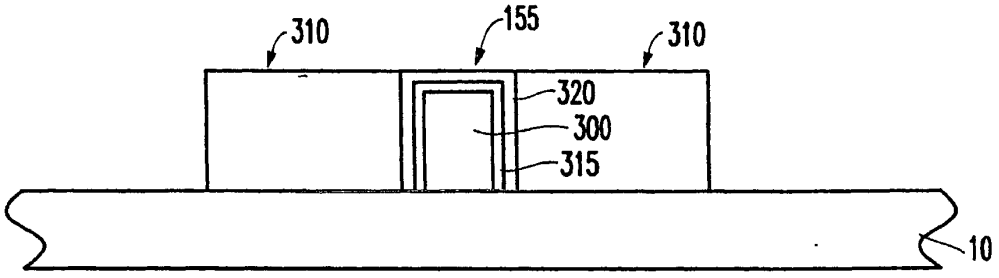


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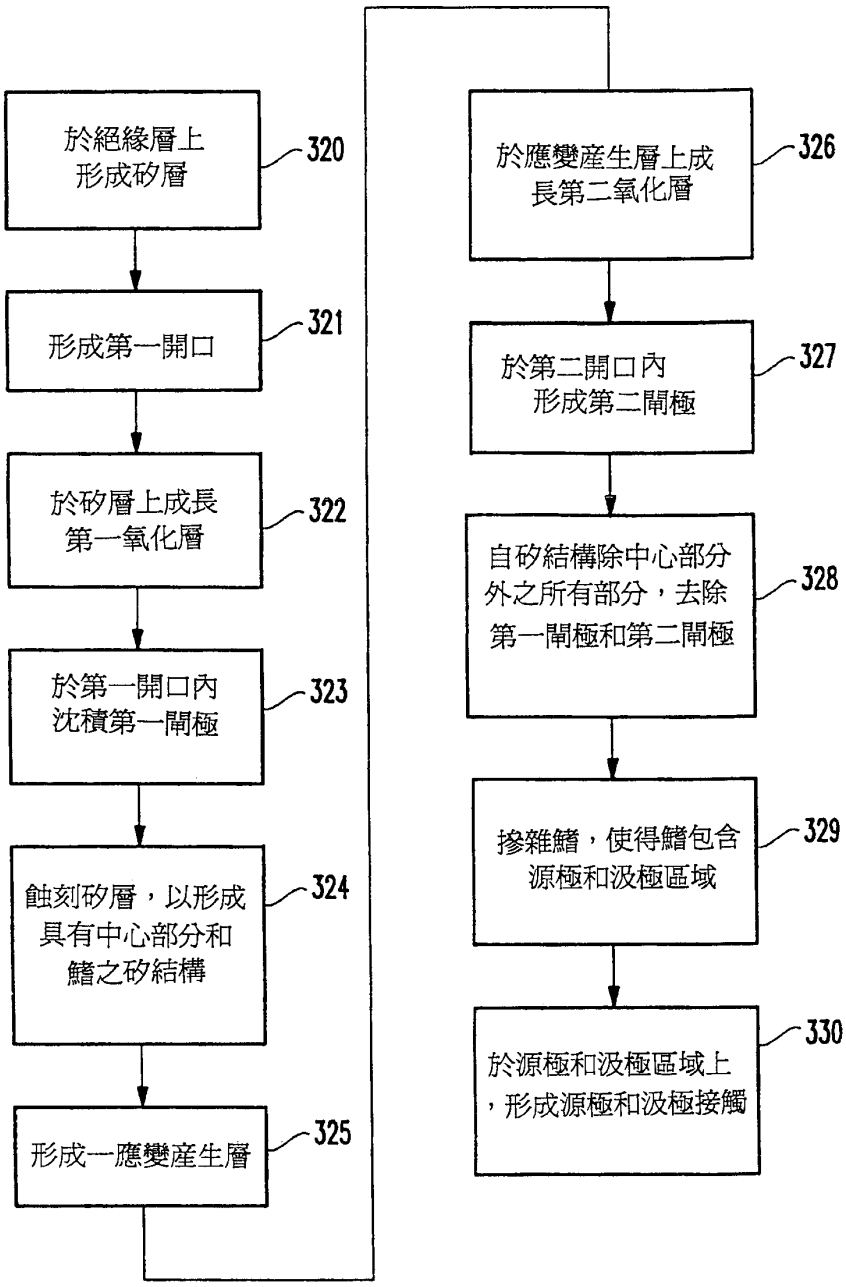

於絕緣層上形成矽層
320
形成第一開口
321
於矽層上成長第一氧化層
322
於第一開口內沈積第一閘極
323
蝕刻矽層，以形成具有中心部分和鰭之矽結構
324
形成一應變產生層
325
於應變產生層上成長第二氧化層
326
於第二開口內形成第二閘極
327
自矽結構除中心部分外之所有部分，去除第一閘極和第二閘極
328
摻雜鰭，使得鰭包含源極和汲極區域
329
於源極和汲極區域上，形成源極和汲極接觸
330

圖 32

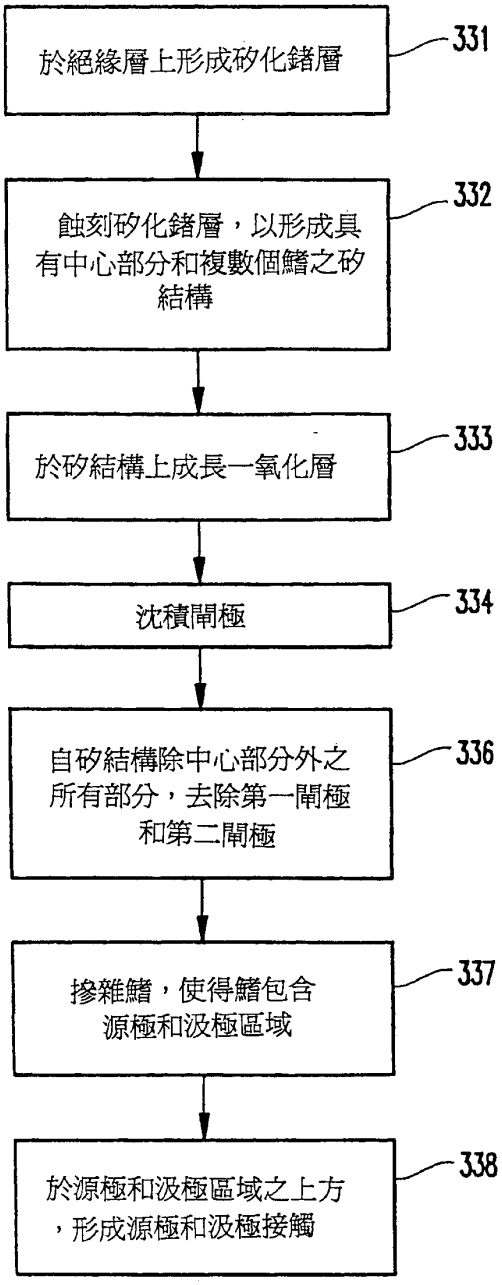

於絕緣層上形成矽化鍺層
331
蝕刻矽化鍺層，以形成具有中心部分和複數個鰭之矽結構
332
於矽結構上成長一氧化層
333
沈積閘極
334
自矽結構除中心部分外之所有部分，去除第一閘極和第二閘極
336
摻雜鰭，使得鰭包含源極和汲極區域
337
於源極和汲極區域之上方，形成源極和汲極接觸
338

圖 33

Espacenet

Bibliographic data: TWI690084 (B) — 2020-04-01

Column iv transistors for pmos integration

Inventor(s): GLASS GLENN [US]; MURTHY ANAND [US] ± (GLASS, GLENN, ; MURTHY, ANAND)

Applicant(s): INTEL CORP [US] ± (INTEL CORPORATION)

Classification: **- international:** ***H01L21/28; H01L29/78***
- cooperative: H01L21/02532 (US); H01L21/28512 (EP, CN, US); H01L21/28525 (US); H01L21/3215 (US); H01L21/76831 (KR, US); H01L23/535 (US); H01L27/092 (US); H01L27/0924 (US); H01L29/06 (CN); H01L29/0603 (CN); H01L29/0615 (US); H01L29/0676 (US); H01L29/0847 (US); H01L29/086 (US); H01L29/165 (EP, CN, US); H01L29/167 (US); H01L29/36 (US); H01L29/41791 (US); H01L29/42356 (KR); H01L29/4236 (KR); H01L29/42392 (EP, US); H01L29/45 (EP, CN, US); H01L29/456 (US); H01L29/4966 (EP, CN, US); H01L29/66409 (CN); H01L29/66477 (CN, US); H01L29/66545 (EP, CN, US); H01L29/6659 (US); H01L29/66628 (EP, CN, US); H01L29/66636 (EP, CN, US); H01L29/66681 (US); H01L29/66795 (CN); H01L29/66931 (US); H01L29/7785 (US); H01L29/78 (CN, US); H01L29/7802 (KR); H01L29/7816 (US); H01L29/7833 (US); H01L29/7848 (EP, CN, US); H01L29/785 (EP, CN, US); H01L29/7851 (US)

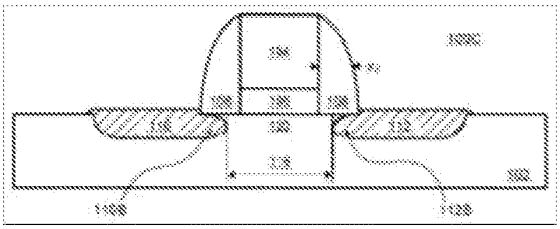
Application number: TW20180102233 20121218

Priority number(s): WO2011US66129 20111220 ; US20100975278 20101221

Also published as: CN103270597 (A) CN103270597 (B) CN103270598 (A) CN103270598 (B) CN103270599 (A) more

Abstract of TW201824567 (A)

Techniques are disclosed for forming column IV transistor devices having source/drain regions with high concentrations of germanium, and exhibit reduced parasitic resistance relative to conventional devices. In some example embodiments, the source/drain regions each includes a thin p-type silicon or germanium or SiGe deposition with the remainder of the source/drain material deposition being p-type germanium or a germanium alloy (e.g., germanium: tin or other suitable strain inducer, and having a germanium content of at least 80 atomic % and 20 atomic % or less other components). In some cases, evidence of strain relaxation may be observed in the germanium rich cap layer, including misfit dislocations and/or threading dislocations and/or twins. Numerous transistor configurations can be used, including both planar and non-planar transistor structures (e.g., FinFETs and nanowire transistors), as well as strained and unstrained channel structures.



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DESCRIPTION TWI690084B

Column IV transistors for PMOS integration

[00003]

The present invention relates to group IV transistors for PMOS integration.

[00004]

The increased performance of circuit devices (including transistors, diodes, resistors, capacitors, and other passive or active electronic devices formed on semiconductor substrates) is generally the main consideration in the process of designing, manufacturing, and operating these devices. factor. For example, in the design and manufacturing or formation of metal oxide semiconductor (MOS) transistor semiconductor devices (such as those used in complementary metal oxide semiconductor (CMOS)), it is usually desirable to minimize the contact (Also called the parasitic resistance of the external resistance Rext). The reduced Rext enables the design of the same transistor to have a higher current.

[00005]

300···Substrate

[00006]

302···Gate Dielectric Layer

[00007]

304···Gate electrode

[00008]

306···Selective hard mask

[00009]

310···Interstitial Wall

[00010]

312···pit

[0011]

312A···Top area

[0012]

313···lining

[0013]

314···pit

[0014]

314A···Top area

[0015]

315···lining

[0016]

318···Cover

[0017]

318A···The top of the source

[0018]

320···Cover

[0019]

320A···Dip pole top

[0020]

322···Insulator layer

[0021]

324···High-k gate dielectric layer

[0022]

325···Reduced contact resistance metal

[0023]

326···Metal gate electrode

[0024]

329···Contact plug metal

[00025]

400···Substrate

[00026]

410···fin

[00027]

420···STI layer

[00028]

430···Gate dielectric material

[00029]

440···Gate electrode

[00030]

450···Hard mask

[00031]

460···Interstitial Wall

[00032]

470···Groove

[00033]

480···Epitaxial liner

[00034]

490···Epitaxial source/drain cap layer

[00035]

510···Nanowire

[00036]

511···Material

[00037]

580···lining

[00038]

590···Cover

[00039]

1000···Computer system

[00040]

1002···motherboard

[00041]

1004···processor

[00042]

1006···Communication chip

[00043]

Fig. 1 schematically depicts the resistor components of a typical MOS transistor including the source and drain top regions; Fig. 2 is a method for forming a group IV transistor according to a specific embodiment of the present invention; Figs. 3A to 3F describes the structure formed by implementing the method of FIG. 2 according to various specific embodiments of the present invention; each of FIGS. 4A to 4G shows a perspective view of a FinFET transistor structure formed according to a specific embodiment of the present invention; FIG. 5A Each of and 5B shows a perspective view of a nanowire transistor structure formed according to an embodiment of the present invention; and FIG. 6 depicts a structure of one or more transistors according to an embodiment of the present invention. The implemented computing system.

[00044]

It should be understood that the drawings are not necessarily drawn to scale or intended to limit the present invention to the specific configuration shown.

For example, although some graphics generally show straight lines, right angles, and smooth surfaces, in view of the limitations of the real world on the processing equipment and technology used, the actual implementation of the transistor structure may have less perfect straight lines and /Or right angles, and some features may have surface topology or be uneven.

In short, the diagrams are only provided to show the example structure.

[00005]

300···Substrate

[00006]

302···Gate Dielectric Layer

[00007]

304···Gate electrode

[00008]

306···Selective hard mask

[00009]

310···Interstitial Wall

[00010]

312···pit

[00011]

312A···Top area

[00012]

313···lining

[00013]

314···pit

[00014]

314A···Top area

[00015]

315···lining

[00016]

318···Cover

[00017]

318A···The top of the source

[00018]

320···Cover

[00019]

320A···Dip pole top

[00020]

322···Insulator layer

[00021]

324···High-k gate dielectric layer

[00022]

325···Reduced contact resistance metal

[00023]

326···Metal gate electrode

[00024]

329···Contact plug metal

[00025]

400···Substrate

[00026]

410···fin

[00027]

420···STI layer

[00028]

430···Gate dielectric material

[00029]

440···Gate electrode

[00030]

450···Hard mask

[00031]

460···Interstitial Wall

[00032]

470···Groove

[00033]

480···Epitaxial liner

[00034]

490···Epitaxial source/drain cap layer

[00035]

510···Nanowire

[00036]

511···Material

[00037]

580···lining

[00038]

590···Cover

[00039]

1000···Computer system

[00040]

1002···motherboard

[00041]

1004···processor

[00042]

1006···Communication chip

[Content and Implementation of the Invention]

Overview

Structure and methodology

Non-planar configuration

Example system

[00045]

The disclosed technology is used to form a group IV transistor device that has source/drain regions with high germanium concentration and exhibits reduced parasitic resistance compared to conventional devices.

In some exemplary embodiments, each of the source/drain regions of the resulting transistor structure includes a thin p-type silicon or germanium or silicon germanium (SiGe) liner, and the source/drain material The remainder of is p-type germanium or germanium alloy, which includes, for example, germanium and tin, and has a germanium content of at least 80 atomic percent (and other components of 20 atomic percent or less, such as tin and/or other suitable strain inducers .

In some cases, evidence of strain relaxation can be observed in this germanium-rich layer, which includes misalignment and/or penetration.

According to the present invention, many transistor configurations and suitable manufacturing procedures will be obvious, including both planar and non-planar transistor structures (such as fin field effect transistors and nanowire transistors), as well as strained and unstrained channels structure.

The technology of the present invention is particularly suitable for realizing p-type MOS (PMOS) devices, but other transistor configurations can also benefit.

[00046]

As explained above, generally, the increase of the drive current in the transistor can be achieved by reducing the external resistance (Rext) of the device.

However, the performance of the PMOS transistor is a function of the resistance of various components in the device, as shown with reference to FIG. 1.

The channel resistance R1 can be adjusted via carrier mobility, which is a function of compressive strain in the channel.

The external resistance Rext of the device includes a top resistance R2 (the top region is also called a source/drain extension), a source/drain resistance R3, and a contact resistance R4 (metal to semiconductor).

All these segmented resistors have a material component (such as energy barrier across the interface, carrier concentration and mobility), geometric components (such as length, width, etc.), and dynamic electrical load components (current crowding).

[00047]

Therefore, according to some specific embodiments of the present invention, a p-type thin liner layer and a high content of germanium (with a very high p-type dopant concentration) are used to replace the general silicon or SiGe alloy materials in the source/drain regions The system minimizes the external resistance components (R2, R3, and R4).

In addition, by introducing highly compressively strained materials, the channel hole mobility is maximized or increased, thereby reducing the channel resistance (R1).

The static effect of the reduced channel, top, source/drain, and contact resistance is an improved transistor current at a given voltage (relative to the critical voltage Vt, or V-Vt).

[00048]

In some example cases, the thin liner layer is p-type doped silicon or germanium or SiGe alloy, and is generally less than 50% of the total source/drain deposition layer thickness.

The thickness of the remaining source/drain deposition layer is generally greater than 50% of the total source/drain deposition layer thickness, and may be, for example, p-type doped germanium or a germanium alloy, such as germanium:tin or germanium:tin: x (wherein x is, for example, silicon or other trace components or artificial products based on process/diffusion), germanium having at least 80 atomic percent and other components of 20 atomic percent or less (such as tin and/or any other suitable strain inducer and / Or other minor unintentional ingredients).

In some special such exemplary embodiments, the thickness ratio of the source/drain liner layer to the high-concentration germanium cap layer is about 1:5 or less (wherein the liner layer constitutes the total source/drain deposition layer About 20% of the thickness or less).

In some such example cases, the thickness of the liner is one to several monolayers.

[00049]

This technology can be used to form transistor devices in any number of devices and systems.

In some embodiments, such as CMOS devices with both n-type MOS (NMOS) and PMOS transistors, selectivity can be achieved in various ways.

In a specific embodiment, for example, deposition on the NMOS source/drain location can be avoided by shielding the NMOS region during the PMOS deposition process.

In other specific embodiments, the selectivity may include natural selection.

For example, although boron-doped germanium is formed on p-type SiGe (or silicon) source/drain, it is not formed on the surface of an insulator (such as silicon dioxide (SiO2) or silicon nitride (SiN)); It is also not generated on exposed heavily phosphorus-doped silicon in, for example, n-type regions.

[00050]

The techniques provided herein can be used to improve device resistance in any number of transistor structures and configurations, including planar, flush or raised source/drain, non-planar (such as nanowire transistors and Fin transistors, such as double-gate and triple-gate transistor structures), and strained and unstrained channel structures.

The source/drain regions may be recessed (for example, using an etching process) or non-recessed (for example, formed on the top surface of the substrate).

In addition, the transistor device can optionally include source and drain tip regions, which are designed to reduce the overall resistance of the transistor and improve the short channel effect (SCE) at the same time, but such tip regions are not necessary.

The transistor device may further include any number of gate configurations, such as polycrystalline gates, high-k dielectric metal gates, alternative metal gate (RMG) process gates, or any other gate structure.

Any number of structural features can be used with the low resistance transistor technology described herein.

[00051]

According to some embodiments, a transmission electron microscope (TEM) cross section perpendicular to the gate line or the outline of a secondary ion mass spectrometer (SIMS) can be used to show the germanium concentration in the structure, because the epitaxial alloy of silicon and SiGe The profile can be easily distinguished from the high germanium concentration profile.

In the case of some such silicon-containing substrates, by discarding the general requirement for maintaining strain (without drain) of the source/drain region, the lattice dimension between the source/drain filling material and the silicon channel The mismatch can increase by at least 2X for pure germanium, and the germanium-tin alloy can increase even more.

In the case where the dislocation occurs in the germanium-rich cap layer, although not 100% of the strain can be transferred to the channel, the post-deposition heat treatment can be used to provide a clear transistor performance (current at a given V-Vt) The gain, even for relaxed films (as described herein), is controlled by the relative strain of SiGe.

It will be understood that relaxation generally means that the film may have misalignment, but can also refer to a plastic relaxation mechanism including the formation and propagation of misalignment.

The procedure of elastic relaxation becomes possible in non-planar configurations (such as FinFETs (such as triple-gate) and nanostructures, where the strained material is not completely restricted by the substrate.

Therefore, the in-plane lattice constant has greater flexibility to expand or contract without being affected by the substrate, and the process does not require the formation and propagation of dislocation rows.

In this article, the term relaxation is used in the sense of plastic relaxation rather than elastic relaxation.

The alloys using tin or other suitable strain inducers to form the high-concentration germanium cap layer described herein can be selectively used to increase the strain in the channel region, thereby further reducing the overall device through the reduction of the resistance R1 in FIG. 1 resistance.

It will be understood that although defect-free pure germanium is ideal, it is generally difficult to grow defect-free for deposition on, for example, silicon substrates or even SiGe substrates with 50 atomic percent germanium.

However, unexpectedly, if the performance of a general fully strained SiGe layer is compared with such a germanium-rich layer with certain defects (such as dislocation and/or penetration), the defective germanium-rich layer will perform better. good.

It will be understood that this result is generally not intuitive because it violates the traditional understanding of films.

In any case, although some specific embodiments of the present invention may include lack of lattice features (such as misalignment, penetration, and twinning (defects are caused by changes in the orientation of the crystal lattice across the twin plane)) The germanium-rich cap layer of, but other specific embodiments may include a germanium-rich cap layer having one or more of these characteristics.

[00052]

FIG. 2 shows a method for forming a group IV transistor according to an embodiment of the present invention.

3A to 3F illustrate exemplary structures formed by implementing the method of FIG. 2 according to various specific embodiments of the present invention.

One or more of these transistors can be formed in, for example, the manufacture of processors, communication chips, or memory chips.

Such integrated circuits can then be used in various electronic devices and systems.

[00053]

An example method includes forming one or more gate stacks on a semiconductor substrate, where MOS devices can be formed on the substrate (202).

MOS devices may include, for example, PMOS transistors, or both NMOS and PMOS transistors (e.g., CMOS devices).

FIG. 3A shows an exemplary structure generated, which in this case includes a PMOS transistor formed on a substrate 300.

It can be seen that the gate stack is formed on the channel region and includes a gate dielectric layer 302, a gate electrode 304, and a selective hard mask 306.

The spacer 310 is formed adjacent to the gate stack.

[00054]

The gate dielectric 302 can be, for example, any suitable oxide, such as silicon dioxide (SiO 2) or a high-k gate dielectric material.

For example, examples of high-k gate dielectric materials include hafnium oxide, hafnium silica, lanthanum oxide, lanthanum oxide, zirconium oxide, zirconium oxide, tantalum oxide, titanium oxide, barium strontium oxide, and barium titanium oxide. , Strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum and scandium lead oxide, and zinc lead niobate.

In some embodiments, when a high-k material is used, an annealing process can be performed on the gate dielectric layer 302 to improve its quality.

In some specific exemplary embodiments, the high-k gate dielectric 302 may have a thickness ranging from 5 Å to 100 Å (for example, 10 Å).

In other embodiments, the gate dielectric 302 may have a thickness of a monolayer of oxide material.

Generally, the thickness of the gate dielectric 302 should be sufficient to electrically isolate the gate electrode 304 from the source and drain contacts.

In some embodiments, an additional process, such as an annealing process, may be performed on the high-k gate dielectric 302 to improve the quality of the high-k material.

[00055]

The material of the gate electrode 304 may be, for example, polysilicon, silicon nitride, carbide, or a metal layer (for example, tungsten, titanium nitride, tantalum, tantalum nitride), but other suitable gate electrode materials may also be used.

In some embodiments, the material of the gate electrode 304 can be a sacrificial layer removed later in the replacement metal gate (RMG) process, and the thickness thereof is in the range of about 10 Å to 500 Å (for example, 100 Å).

[00056]

The selective gate hard mask layer 306 can be used to provide certain benefits or use during the manufacturing process, for example, to protect the gate electrode 304 from subsequent etching and/or implantation processes.

The hard mask layer 306 can be formed using general hard mask materials, such as silicon dioxide, silicon nitride, and/or conventional insulator materials.

[00057]

The gate stack can be formed by a conventional method or by using any suitable customized technology (for example, a conventional patterning process to etch away part of the gate electrode and gate dielectric layer to form the gate electrode and gate dielectric layer shown in FIG. 2A Gate stack).

Each of the gate dielectric 302 and the gate electrode 304 material can be formed, for example, using a conventional deposition process, such as chemical vapor deposition (CVD), molecular layer deposition (ALD), spin-on deposition (SOD), Or physical vapor deposition (PVD).

Other deposition techniques may also be used. For example, the gate dielectric 302 and gate electrode 304 materials may be thermally grown.

It can be understood from the content of this specification that any number of other suitable materials, geometries, or formation processes may be used to implement specific embodiments of the present invention to provide the low-resistance transistor devices or structures described herein.

[00058]

The spacer 310 may be formed of, for example, a conventional material, such as silicon oxide, silicon nitride, or other suitable spacer materials.

The width of the spacer 310 can generally be selected based on the design requirements of the transistor to be formed.

However, according to some specific embodiments, the width of the spacer 310 is not limited by the design caused by the formation of the source and drain top regions. It is assumed that there is sufficiently high p-type doping in the source/drain top regions. Germanium content (eg boron-doped germanium) or SiGe alloy liner.

[00059]

Any number of suitable substrates can be used to implement the substrate 300, including bulk substrates, semiconductor-on-insulator substrates (XOI, where X is a semiconductor material, such as silicon, germanium, or germanium-rich silicon), and multilayer structures, including Those substrates on which fins or nanowires can be formed before the subsequent gate patterning process.

In some specific examples, the substrate 300 is a bulk substrate of germanium or silicon or SiGe, or germanium or silicon or SiGe on an oxide substrate.

Although a few examples of materials that can form the substrate 300 are described herein, other suitable materials that can be used as the basis for building low-resistance transistor devices are also within the spirit and scope of the claimed invention.

[00060]

3A, after the formation of one or more gate stacks, the method continues with some selective processing, in this exemplary embodiment includes etching the source/drain regions (204) of the transistor structure, and removing Masks (if any) of any NMOS source/drain regions of the structure (206).

It will be understood that the source/drain regions need not be recessed or otherwise etched.

In this case, the source/drain material can be formed on the substrate 300 without any etching.

According to some embodiments, although this non-recessed source/drain region will not affect the channel resistance, a double-layer source/drain structure with a thin liner layer and a high germanium content cap layer can still be implemented to provide low contact resistance.

It will be further understood that not all specific embodiments include n-type regions.

In some example cases, for example, the manufactured circuit may only include PMOS devices.

In this type of example case, no n-type source/drain regions need to be unmasked.

When n-type regions appear, any suitable masking technique can be used to protect the n-type regions during p-type processing.

[00061]

In an exemplary embodiment where the source/drain regions are etched, source/drain cavities 312/314 are generated, as shown in FIG. 3A.

The cavities effectively define the location of the source/drain regions.

It can be further seen that the substrate 300 has not only been etched to produce the source/drain cavities 31223/314, but also the individual top regions 312A/314A of the undercut gate dielectric 302 have been produced.

The cavities 312/314 and their respective top regions 312A/314A can be formed in a conventional manner using any number of suitable processes.

In some example cases, this includes ion implantation to highly dope the portion of the substrate 300 adjacent to the gate stack, followed by annealing to drive the dopants into the substrate 300 to improve the expected source/drain region. Etching rate.

Then, a dry etching process can be used to etch the doped regions of the substrate 300 to form the cavities 312/314 and their respective top regions 312A/314A.

After the dry etching process is completed, wet etching can be used, for example, to clean and further etch the cavities 312/314 and their respective top regions 312A/314A.

This type of wet etching can be performed using conventional or customized wet etching chemicals, which can be used to remove contaminants, such as carbon, fluorine, chlorofluorocarbon, and oxides (such as silicon oxide), to provide subsequent processing options. A clean surface implemented on it.

In addition, assuming a single crystal silicon surface, wet etching can also be used to remove thin portions of the substrate 300 along the <111> and <001> crystal planes to provide a smooth surface where high-quality epitaxial deposition can occur. .

In some exemplary cases, the thin portion of the substrate 300 that is etched and removed can be as high as 5 nm thick, and can remove residual contaminants.

Wet etching generally causes the edges of the cavities 312/314 and individual top regions 312A/314A to be along the <111> and <001> crystal planes.

[00062]

With further reference to FIG. 2, the method continues to deposit a p-type silicon or germanium or SiGe liner layer 313/315 on the p-type source/drain region (208), and then deposits a p-type germanium or germanium alloy on the liner layer 313/315 In the p-type source/drain region (210).

Each of these depositions can be achieved, for example, using selective epitaxial deposition, but any suitable deposition process can be used.

Referring to FIG. 3B, it can be seen that the p-type silicon or germanium or SiGe liner layer 313/315 is deposited in the cavity 312/314 and its respective top regions 312A/314A.

In addition, as shown in FIG. 3C, the cavity 312/314 and its respective top regions 312A/314A are further filled to provide a thick cap layer 318/320 of p-type germanium or germanium alloy on the p-type liner layer 313/315 .

It will be understood that examples of p-type dopants include, for example, boron, gallium, or any other suitable p-type dopants, and the claimed invention is not intended to be limited to any particular one.

[00063]

According to some specific example embodiments where the substrate 300 is a silicon or SiGe bulk substrate, or a semiconductor-on-insulator substrate (XOI, where X is silicon or SiGe), the source and drain cavities 312/314 and their respective tops The regions 312A/314A are filled with in-situ boron-doped silicon or SiGe to form the corresponding liner layer 313/315, and then further filled with in-situ boron-doped germanium or germanium-rich alloy to form a capping layer 318/320.

In other exemplary embodiments where the substrate 300 is a germanium bulk substrate or a germanium-on-insulation substrate, the source and drain cavities 312/314 and their respective top regions 312A/314A may be rich in germanium doped with boron in situ The alloy (eg germanium: tin) is filled to form the corresponding liner layer 313/315, and then the germanium-rich alloy doped with in-situ boron is further filled to form the cap layer 318/320.

It can be understood from the content of this specification that the individual germanium or p-type dopant concentration of the liner layer 313/315 and the cap layer 318/320 may vary according to factors such as: the composition of the substrate 300, the lattice matching/compatibility The use of gradual changes, and the overall ideal thickness of the total source/drain deposition.

It can be understood from the content of this specification that many material systems and p-type doping configurations can be implemented.

[00064]

For example, in certain exemplary embodiments with silicon or germanium or SiGe substrates, the germanium content of the liner layer 311/3315 may be in the range of 20 atomic percent to 100 atomic percent, and the boron concentration may be in the range of 1E20 cm-3 to 1E20 cm-3. In the range of 2E21cm-3.

According to some embodiments, in order to avoid the mismatch between the crystal lattice and the underlying silicon-containing substrate, the germanium concentration of the liner layer 313/315 may be gradually changed.

For example, in one such embodiment, the liner layer 313/315 may be a gradual change of boron-doped SiGe layer, which has a gradual change from a reference concentration compatible with the underlying silicon or SiGe substrate 300 to 100 A germanium concentration of atomic percent (or close to 100 atomic percent, for example, more than 90 atomic percent, 95 atomic percent, or 98 atomic percent).

In a specific such embodiment, the germanium concentration ranges from 40 atomic percent or less to more than 98 atomic percent.

The boron concentration in the liner layer 313/315 may be fixed at a high level or may be gradually changed, for example.

For example, the boron concentration in the liner layer 313/315 may gradually change from a reference concentration equal to or compatible with the underlying substrate 300 to an ideal high concentration (for example, more than 1E20cm-3, 2E20cm-3, or 5E20cm-3).)and.

In certain such specific embodiments, the boron-doped germanium cap layer 318/320 has a boron concentration exceeding 1E20 cm-3 (for example, exceeding 2E20 cm-3 or 2E21 cm-3 or higher).

The boron concentration in the cap layer 318/320 can be gradually changed in a manner similar to that described with reference to the liner layer 313/315.

More generally, the boron concentration can be adjusted as needed to provide the required conductivity level, which can be understood according to the content of this specification.

For example, the germanium concentration of the cap layer 318/320 can be fixed at 100 atomic percent.

Or, according to the content of this specification, it can be understood that the germanium concentration of the cap layer 318/320 can be gradually changed from a low to a high concentration (for example, from 20 atomic percent to 100 atomic percent) to take into account the liner layer 313/315 and the cap layer 318/ The lattice mismatch between the ideal peak germanium concentration of 320.

In other specific embodiments, the cap layer 318/320 may be implemented by a germanium alloy, where the mixture may be, for example, up to 80 atomic percent of germanium and up to 20 atomic percent of alloy material (which is tin in some specific embodiments).

It should be noted that it will be understood that the tin concentration (or other alloy materials) can also be gradually changed.

In this case, when the tin concentration in the cap layer 318/320 is in the range of 3 to 8 atomic percent, the channel strain will increase (the equilibrium atomic percent of the cap layer 318/320 is essentially germanium and any gradient material).

Despite the relaxation, the lattice constant is still relatively large, and sufficient strain can be applied to adjacent channels.

Other suitable tin concentrations are obvious, as are other suitable strain inducers.

[00065]

It should be noted that when a pure germanium substrate is used, the liner layer 313/315 can be realized by germanium and does not need to be changed gradually.

In some such cases, the germanium concentration of the liner layer 313/315 may be fixed (for example, 100 atomic percent) and the cap layer 318/320 may be made of a germanium alloy (for example, germanium:tin, or the aforementioned other suitable germanium alloy) accomplish.

As explained above, the germanium concentration (or tin or other alloy material concentration) in the cap layer 318/320 can be gradually changed to produce a desired channel strain.

In some such cases, it should be further noted that the germanium liner layer 313/315 can be effectively integrated with the germanium alloy cap layer 318/320 or can be an undetectable component deposited in the source/drain region.

[00066]

Regarding the gradual change, it should be noted that the compatibility used herein does not need to overlap in the concentration level (for example, the germanium concentration of the underlying substrate 300 can be 0 to 20 atomic percent, and the initial The germanium concentration can be 30 to 40 atomic percent).

In addition, as used herein, the term "fixed" in relation to the concentration level means a relatively constant concentration level (for example, the lowest concentration level in a layer is 10% of the highest concentration level in the layer).

In a more general sense, a fixed concentration level means the lack of deliberately changing concentration levels.

[00067]

The thickness of the liner layer 313/315 and the cap layer 318/320 can also vary with the following factors: the composition of the substrate 300, the use of gradual changes in lattice matching/compatibility, and the overall ideal of total source/drain deposition thickness.

Generally, in the case where the liner layer 313/315 is configured to have a gradually changing germanium content to provide compatibility with the substrate 300 that does not have or has a low germanium content, the liner layer 313/315 may be thicker.

In other cases, when the substrate 300 is a germanium substrate or contains a relatively high concentration of germanium, the liner layer 313/315 does not need to be changed gradually, so it can be relatively thin (for example, one to several monolayers).

In other cases, when the substrate 300 does not contain or has a relatively low germanium content, the liner layer 313/315 may be implemented by a relatively thin silicon layer or a low germanium content material layer, and the germanium content of the cap layer 318/320 may depend on the phase. Capacitive needs change gradually.

In any such case, the liner layer 313/315 generally constitutes less than 50% of the total source/drain deposition layer thickness, and the remaining source/drain deposition layer thickness is generally greater than 50% of the total source/drain deposition layer thickness. The thickness of the polar deposition layer.

According to some such exemplary embodiments, when the liner layer 313/315 does not change gradually, the thickness ratio of the liner layer 313/315 to the cap layer 318/320 is about 2:5 or less (that is, the liner layer constitutes the total source /About 40% or less of the thickness of the drain deposition layer).

In some specific such embodiments, the thickness ratio of the liner layer 313/315 to the cap layer 318/320 is about 1:5 or less (that is, the liner layer constitutes about the thickness of the total source/drain deposition layer). 20% or less).

In a specific example of this type, the thickness of the liner layer 313/315 is in the range of 1 to several monolayers to about 10 nanometers, and the total source/drain deposition layer thickness is 50 to 500 nanometers. Scope.

According to this description, it is clear that there are many source/drain liner and cap layer geometries and material configurations.

[00068]

It will be understood from the content of this specification that specific embodiments of the invention may implement any number of other transistor features.

For example, the channel may be strained or unstrained, and the source/drain region may or may not include a top region formed between the corresponding source/drain region and the channel region.

In this sense, regardless of whether the transistor structure has a strained or unstrained channel, or has a source/drain top region or no source/drain top region, it is not particularly relevant to the various embodiments of the present invention, and so The claimed invention is not intended to be limited to any specific such structural features.

Conversely, any number of transistor structures and types, especially those with p-type or n-type and p-type source/drain transistor regions, will be used with the liner and height described herein. Benefit from the double-layer source/drain configuration of the germanium concentration cap layer.

[00069]

The deposition (206 and 210) can be performed using a CVD process or other suitable deposition techniques.

For example, the deposition of 208 and 210 can be performed in a CVD reactor, an LPCVD reactor, or an ultra-high vacuum CVD (UHVCVD).

In some exemplary cases, the reactor temperature may fall between 600° C. and 800° C., and the reactor pressure may fall between 1 to 760 Torr, for example.

The carrier gas may, for example, include hydrogen or helium, which has an appropriate flow rate, for example, between 10 and 50 SLM.

In some specific embodiments, a germanium source precursor gas (for example, GeH4 diluted in H2 (for example, GeH4 may be diluted to 1-20%)) may be used to perform the deposition.

For example, diluted GeH4 can be used at a concentration of 1% and a flow rate ranging from 50 to 300 SCCM.

For in-situ doping of boron, diluted B2H6 can be used (for example, B2H6 can be diluted to 1-20% in H2).

For example, diluted B2H6 can be used at a concentration of 3% and a flow rate ranging from 10 to 100 SCCM.

In some example cases, an etchant may be added to increase the selectivity of the deposition.

For example, HCl or Cl2 with a flow rate ranging, for example, between 50 to 300 SCCM can be added.

[00070]

According to the content of this specification, various changes in the source/drain double-layer structure will be obvious.

For example, in some embodiments, the liner layer 313/315 is implemented by epitaxially deposited boron-doped SiGe, which can be one or more layers with germanium in the range of 30 to 70 atomic percent or more. concentration.

As explained above, the germanium concentration of the SiGe underlayer can be fixed or gradually changed to increase from the reference (close to the substrate 300) to a high level (for example, more than 50 atomic percent, close to the reference concentration of the germanium concentration of the cap layer 318/320) , Germanium continues to gradually change to 100 atomic percent).

In some such specific embodiments, the boron concentration may exceed 1E20cm-3, such as higher than 5E20cm-3 or 2E21cm-3, and may also be gradually changed to increase from a baseline close to the substrate 300 to a high level (for example, more than 1E20cm- 3 or 2E20cm-3 or 3E20cm-3, etc., close to the cover layer 318/320).

In the specific embodiment where the germanium concentration of the boron-doped SiGe liner layer 313/315 is fixed, a thin gradual change buffer can be used to better connect the liner layer 313/315 and the boron-doped cap layer 318/320.

It should be noted that the buffer can be an intermediate layer or integrated into the composition of the cover layer 318/320.

For the purpose of this disclosure, the buffer can be regarded as part of the cover layer 318/320.

According to some specific exemplary embodiments, the thickness of the boron-doped SiGe deposition layer (or collection of layers) 313/315 can be, for example, in the range of a few monomolecular layers to 50 nanometers, and the layer (or collection of layers) 318/ 320 may have a thickness ranging, for example, from 51 to 500 nanometers, but other specific embodiments may have other liner and cap thicknesses, which will be apparent from the content of this specification.

In some specific embodiments, it should be noted that the cavities 312/314 can be generated under the spacer during the cyclic deposition-etching process, and these cavities 312/314 can also be backfilled by an epitaxial cap layer (which can be, for example, it has the same composition as the boron-doped germanium cap layer 318/320).

[00071]

In view of the content of this specification, it will be better understood that the combination of high germanium concentration (for example, more than 50 atomic percent and up to pure germanium) and high boron concentration (for example, more than 1E20cm-3) (as discussed herein) can be used to mainly realize the PMOS circuit The source and drain regions of the crystal device (R3 in FIG. 1) and their respective top regions (R2 in FIG. 1) have higher conductivity.

In addition, as explained above, because the diffusion of boron in the high-germanium component layer is sufficiently suppressed compared to the low-germanium component layer, despite the high doping concentration in the deposited stressor film, when compared with the same p-type The lower germanium composition layer of dopant type and doping level can achieve less unfavorable SCE degradation by subsequent thermal annealing.

The higher germanium concentration at the contact surface (which results in the lower contact resistance R4 in Figure 1) also enables the barrier height to be reduced.

In some exemplary embodiments, germanium concentrations in excess of 80 atomic percent and up to pure germanium (100 atomic percent) can be used to achieve this benefit.

However, it should be noted that pure germanium is not necessary.

For example, certain embodiments may have a germanium concentration in excess of 90 or 95 atomic percent (but not pure).

[00072]

With reference to FIG. 3C, it can be further seen that forming the source/drain tips 318A/320A in the region relatively close to the channel also exerts a relatively large hydrostatic stress on the channel.

This stress increases the strain in the channel, thereby increasing the mobility in the channel and increasing the drive current.

In the case of a silicon-containing substrate, this stress can be further amplified by increasing the germanium concentration of the source/drain top 318A/320A, and in the case of a germanium substrate, it can be amplified by increasing the tin concentration.

This is an improvement to the diffusion-based process, in which the tip area generally does not include the strain on the channel area.

[00073]

Once the source and drain regions are filled according to specific embodiments of the present invention, various conventional MOS processes can be implemented to complete the fabrication of MOS transistors, such as alternative gate oxide processes, alternative metal gate processes, annealing, and The metal silicide deposition process can further modify the transistor and/or provide the necessary electrical interconnections.

For example, after epitaxial deposition on the source/drain regions and their respective tops, with further reference to Figure 2, the method can continue to remove any masks from the n-type regions and treat these regions as needed (if applicable, for example in the CMOS process) (212), an insulator is deposited on the transistor (214), and then the insulator layer is planarized in the usual way.

The insulator layer may use conventional materials suitable for the insulator layer of integrated circuit structures, such as low-k dielectric (insulator) materials.

This insulator material includes, for example, oxides (such as silicon dioxide (SiO_2) and carbon doped oxide (CDO)), silicon nitride, organic polymers (such as octafluorocyclobutane, polytetrafluoroethylene), fluorosilicone glass (FSG), and organosilicate (such as semisiloxane, siloxane, or organosilicate glass).

In some example configurations, the insulator layer may include pores or other holes to further reduce its dielectric constant.

FIG. 3D depicts an example of depositing the insulator layer 322 and then planarizing it to the hard mask 306.

[00074]

With reference to FIG. 3D', it can be further seen that some embodiments of the present invention use an alternative metal gate process, and the method may include using a conventional etching process to remove the gate stack (including high-k gate dielectric Layer 302, sacrificial gate electrode 304, and hard mask layer 306).

In another implementation, only the sacrificial gate 304 is removed.

If the gate dielectric 302 is removed, the method may include depositing a new gate dielectric layer to the trench opening.

Any suitable high-k dielectric material (as described above) can be used here, such as hafnium oxide.

The same deposition process can also be used.

The gate dielectric 302 can be used instead of, for example, to solve any damage that occurs in the initial gate dielectric layer during the application of dry and wet etching processes, and/or with high-k or other ideal gates Dielectric materials to replace low-k or sacrificial dielectric materials.

The method can then continue to deposit the metal gate electrode layer into the trench and on the gate dielectric layer.

A conventional metal deposition process can be used to form the metal gate electrode layer, such as CVD, ALD, PVD, electroless plating, or electroplating.

The metal gate electrode layer may include, for example, p-type work function metals, such as ruthenium, palladium, cobalt, nickel, and conductive metal oxides (such as ruthenium oxide).

In some example configurations, two or more metal gate electrode layers can be deposited.

For example, a work function metal can be deposited, followed by a suitable metal gate electrode filler metal, such as aluminum.

FIG. 3D' depicts an example high-k gate dielectric layer 324 and metal gate electrode 326 according to a specific embodiment of the present invention, which have been deposited into the trench opening.

It should be noted that if necessary, this RMG procedure can be implemented at different points in the manufacturing process.

[00075]

With further reference to FIG. 2, after forming the insulator layer 322 (and any required pre-contact formation RMG process), the method continues to etch to form source/drain contact trenches (216).

Any suitable dry and/or wet etching process can be used.

FIG. 3E shows the source/drain contact trenches after etching is completed according to an exemplary embodiment.

[00076]

Next, the method continues to deposit the contact resistance reducing metal and annealing (218), and then deposit the source/drain contact plugs (220).

Figure 3F shows the contact resistance reducing metal 325, which in some embodiments includes silver, nickel, aluminum, titanium, gold, gold-germanium, nickel-platinum, or nickel-aluminum, and/or other such resistance reducing metals Or alloy.

Figure 3F further shows the contact plug metal 329, which in some embodiments includes aluminum or tungsten, however, any suitable conductive contact metal or alloy can be used, such as silver, nickel-platinum or nickel-aluminum or nickel and aluminum. Other alloys, or titanium, use conventional deposition processes.

The metallization of the source/drain contacts can, for example, use a germanium process (generally, the deposition of the contact metal and subsequent annealing).

For example, other alloys with nickel, aluminum, nickel-platinum or nickel-aluminum or nickel and aluminum, or germanization of titanium (with or without germanium pre-amorphous implantation) can be used to form low-resistance germanides.

The boron-doped germanium cap layer 318/320 allows metal-germanide formation (e.g., nickel-germanium).

Germanium allows significantly lower Schottky-barrier height and improved contact resistance than traditional metal-silicide systems.

For example, conventional transistors generally use a source/drain SiGe epitaxy process, and the germanium concentration ranges from 30 to 40 atomic percent.

This conventional system exhibits a Rext value of about 140 ohm-micron, which is limited by the epitaxial/silicide interface resistance, which is high and may hinder future gate pitch scaling.

Certain embodiments of the present invention allow a significant improvement of Rext in PMOS devices (for example, 2x or better improvement, such as Rext of about 70 ohm-micron or lower), which can better support PMOS device scaling.

Therefore, compared to conventional transistors, a transistor with a source/drain structure configured as a double-layer source/drain structure as described herein can exhibit a relatively lower Rext value.

[00077]

Non-planar architectures can be implemented, for example, using fin transistors or nanowire configurations.

FinFET is a transistor built around a thin strip of semiconductor material (generally called a fin).

Transistors include standard field-effect transistor (FET) nodes, including gates, gate dielectrics, source regions, and drain regions.

The conduction channel of the device is located under the gate dielectric and on/inside the outside of the fin.

In particular, the current flows along the two side walls of the fin (the side perpendicular to the substrate plane) and also along the top of the fin (the side parallel to the substrate plane).

Because the conduction channels of this configuration are mainly located in three different outer, planar areas along the fin, this FinFET design is sometimes called a three-gate FinFET.

Other types of FinFET configurations can also be used, such as so-called dual-gate FinFETs, where the conduction channels are mainly located only along the two sidewalls of the fin (not along the top of the fin).

[00078]

4A to 4G each show a perspective view of a FinFET transistor structure formed according to a specific embodiment of the present invention.

It will be understood that the previous discussion regarding FIGS. 2 to 3F can also be applied here.

It can be seen that the exemplary non-planar configuration shown in FIG. 4A is implemented in a fin structure and includes a substrate 400 having a semiconductor body or fin 410 extending from the substrate 400 through a shallow trench isolation (STI) layer 420.

The substrate may be silicon, germanium, or SiGe, for example.

[00079]

FIG. 4B shows the gate electrodes 440 formed on the three surfaces of the fin 410 to form three gate electrodes (hence the tri-gate device).

The gate dielectric material 430 is formed between the fin 410 and the gate electrode 440, and the hard mask 450 is formed on the top of the gate electrode 440.

Figure 4C depicts the resulting structure after deposition of insulating material and subsequent etching (which leaves a coating of insulator material on all vertical surfaces to form spacers 460).

[00080]

4D depicts the structure produced after the additional etching process, which eliminates excess insulation/spacer material from the sidewalls of the fin 410, and only leaves the spacer 460 on the opposite sidewall of the gate electrode 440.

FIG. 4E depicts the structure produced after the recess is etched, which removes the fin 410 in the source/drain region of the substrate 400 to form a recess 470.

It should be noted that other embodiments may have no grooves (for example, the source/drain regions are aligned with the STI layer 420).

[00081]

4F depicts the structure produced after the growth of the epitaxial liner 480, which can be thin, p-type and contain a substantial portion of silicon (such as silicon or SiGe with 70 atomic percent silicon), or pure germanium (such as A separation layer of germanium, or an undetectable layer integrated into or included in the composition of the cap layer 318/320).

FIG. 4G depicts the structure produced after the epitaxy source/drain cap layer 490 is grown, which may be p-type and mainly contain germanium, but may contain less than 20 atomic percent of tin or other suitable alloy materials, as described above Explained.

According to the content of this specification, it will be understood that conventional manufacturing processes and forming techniques can be used to manufacture the FinFET transistor structure with a double-layer source/drain structure described herein.

[00082]

It will be further understood that it should be noted that the alternative to the three-gate configuration shown is a double-gate structure, which includes a dielectric/isolation layer on top of the fin 410.

It should also be noted that the exemplary shapes of the liner layer 480 and the cap layer 490 constituting the source/drain region shown in FIG. 4G are not intended to limit the claimed invention to any specific source/drain type or formation process. And according to the content of this specification, other source/drain shapes are obvious and easy to know (for example, circular, square or rectangular source/drain regions can be implemented).

[00083]

FIG. 5A shows a perspective view of a nanowire transistor structure formed according to an embodiment of the present invention.

Nanowire transistors (sometimes called wrap-around gate FETs) are similarly configured as fin-based transistors, but nanowires are used instead of fins, and the gate material generally surrounds all sides of the channel area .

According to specific designs, some nanowire transistors have, for example, four equivalent gates.

Figure 5A depicts a nanowire channel architecture with two nanowires 510, however other embodiments may have any number of wires.

The nanowire 510 may be implemented by, for example, p-type silicon or germanium or SiGe nanowire.

It can be seen that one nanowire 510 is formed or provided in the recess of the substrate 400, and the other nanowires 510 are equivalently floating on the source/drain material double-layer structure including the liner layer 580 and the cap layer 590 middle.

As with the fin configuration, it should be noted that the source/drain nanowire 510 (such as a relatively thin silicon or germanium or SiGe liner layer and a relatively thick The high-concentration germanium cap layer).

Alternatively, the double-layer structure may be formed around the initially formed nanowire 510, as shown in the figure (wherein the liner 580 is formed around the nanowire 510, and the cap layer 590 is then formed around the liner 580).

Figure 5B also depicts a nanowire configuration with multiple nanowires 510, but in this example, it can be understood from the content of this specification that in the nanowire formation process, the inactive material 511 is not removed from the individual nanowires. Inter-removal, which can be implemented using various conventional techniques.

Therefore, one nanowire 510 is formed in the recess of the substrate 400, and the other nanowire 510 is equivalently located on the top of the material 511.

It should be noted that the nanowire 510 acts through the channel, but the 511 material does not.

It can be seen that the double-layer source/drain structure of the liner layer 580 and the cap layer 590 surrounds all other exposed surfaces of the nanowire 510.

[00084]

FIG. 6 depicts a computing system 1000 implemented by configuring one or more transistor structures according to exemplary embodiments of the present invention.

It can be seen that the computing system 1000 contains a motherboard 1002.

The motherboard 1002 may include some components, including but not limited to a processor 1004 and at least one communication chip 1006, each of which may be physically and electrically coupled to the motherboard 1002 or integrated therein.

It will be understood that the main board 1002 can be, for example, any printed circuit board, whether it is a main board, a daughter board mounted on the main board, or a board of only the system 1000, or the like.

Depending on its application, the computing system 1000 may include one or more other components, which may or may not be physically and electrically coupled to the motherboard 1002.

These other components may include but are not limited to volatile memory (such as DRAM), non-volatile memory (such as ROM), graphics processor, digital signal processor, cryptographic processor, chipset, antenna, display, touch screen Display, touch screen controller, battery, audio codec, video codec, power amplifier, global positioning system (GPS) device, compass, accelerometer, gyroscope, speaker, camera, mass storage device (such as hard disk) Driver, compact disc (CD), digital versatile disc (DVD), etc.).

Any component included in the computing system 1000 may include one or more transistor structures described herein (for example, having a double-layer source/drain structure, which includes a relatively thin p-type silicon or germanium or SiGe liner layer and a relatively thin Thick p-type high germanium content cap layer).

These transistor structures can be used, for example, to implement on-board processor caches or memory arrays.

In some embodiments, multiple functions can be integrated into one or more chips (for example, it should be noted that the communication chip 1006 can be part of the processor 1004 or integrated into the processor 1004).

[00085]

The communication chip 1006 is a wireless communication that enables data transfer to and from the computing system 1000.

"Wireless" and its derivatives can be used to describe circuits, devices, systems, methods, technologies, communication channels, etc., which can communicate data through the use of modulated electromagnetic radiation through non-solid media.

This term does not mean that the related device does not contain any wires, but it may not be included in some specific embodiments.

The communication chip 1006 can implement any number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long-term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, its derivatives, and any other wireless protocols designated as 3G, 4G, 5G or higher.

The computing system 1000 may include a plurality of communication chips 1006.

For example, the first communication chip 1006 can be dedicated to short-range wireless communication, such as Wi-Fi and Bluetooth, and the second communication chip 1006 can be dedicated to longer-range wireless communication, such as GPS, EDGE, GPRS, CDMA , WiMAX, LTE, Ev-DO and others.

[00086]

The processor 1004 of the computing system 1000 includes an integrated circuit die packaged in the processor 1004.

In some embodiments of the present invention, the integrated circuit die of the processor includes a built-in memory circuit, which is implemented with one or more transistor structures (such as PMOS or CMOS) described herein.

The term "processor" can refer to any device or part of a device that processes, for example, electronic data from a register and/or memory and converts the electronic data into something else that can be stored in the register and/or memory Electronic data.

[00087]

The communication chip 1006 may also include an integrated circuit die packaged in the communication chip 1006.

According to some such exemplary embodiments, the integrated circuit die of the communication chip includes one or more circuits (such as on-chip processors or memory) implemented in one or more transistor structures described herein.

According to the content of this specification, it should be noted that the multi-standard wireless capabilities can be directly integrated into the processor 1004 (for example, the functions of any chip 1006 are integrated into the processor 1004 instead of having a separate communication chip).

In addition, it should be noted that the processor 1004 may be a chipset with this wireless capability.

In short, any number of processors 1004 and/or communication chips 1006 can be used.

Similarly, any chip or chip set can have multiple functions integrated therein.

[00088]

In various implementations, the computing system 1000 can be a laptop computer, a light-saving laptop, a notebook computer, a smart phone, a tablet computer, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, Server, printer, scanner, monitor, set-top box, entertainment control unit, digital camera, mobile music player, or digital video recorder.

In a further implementation, the system 1000 may be any other electronic device that processes data or uses the low-resistance transistor devices described herein (such as PMOS and CMOS circuits).

[00089]

Many specific embodiments will be apparent, and the features described herein can be combined in any number of configurations.

An exemplary embodiment of the present invention provides a transistor device.

The device includes a substrate with a channel region, a gate electrode on the channel region, and a source/drain region formed on or in the substrate and adjacent to the channel region.

Each of the source and drain regions has a total thickness, which includes a p-type liner layer of silicon or germanium or silicon germanium and a p-type cap layer with a germanium concentration exceeding 80 atomic percent, wherein the liner layer is less than the total thickness 50% of it.

In some cases, the device is one of planar, FinFET, or nanowire PMOS transistors.

In some cases, the device further includes metal-germanide source/drain contacts.

In some cases, the thickness ratio of the liner layer thickness to the cap layer thickness is 2:5 or less (the liner layer is 40% or less of the total thickness).

In some cases, the ratio of the thickness of the lining layer to the thickness of the cap layer is 1:5 or less (the lining layer is 20% or less of the total thickness).

In some cases, each of the liner layers has a thickness ranging from about 1 monolayer to 10 nanometers, and each of the cap layers has a thickness ranging from about 50 nanometers to 500 nanometers.

In some cases, at least one of the liner layer and/or the cap layer has at least one of the gradually changing concentrations of germanium and/or the p-type dopant.

For example, in some cases, at least one of the liner layers has a germanium concentration, which gradually changes from a reference concentration compatible with the substrate to a high concentration exceeding 50 atomic percent.

In one such case, the high concentration is more than 90 atomic percent.

In some cases, at least one of the liner layers has a p-type dopant concentration, which gradually changes from a reference concentration compatible with the substrate to a high concentration exceeding 1E20 cm-3.

In one such case, the p-type dopant of one or more underlayers is boron.

In some cases, at least one of the cap layers has a germanium concentration exceeding 95 atomic percent.

In some cases, at least one of the cap layers has a germanium concentration that gradually changes from a reference concentration compatible with the corresponding liner layer to a high concentration exceeding 80 atomic percent.

In some cases, at least one of the cap layers has a p-type dopant concentration that gradually changes from a reference concentration compatible with the corresponding liner layer to a high concentration exceeding 1E20 cm-3.

In some cases, the p-type dopant of one or more cap layers is boron.

In some cases, at least one of the cap layers further contains tin.

Many changes will be obvious.

For example, in some example cases, the substrate is a silicon-containing substrate.

In some such cases, the p-type liner layer contains silicon or silicon germanium.

In other example cases, the substrate is a germanium substrate.

In some such cases, the p-type liner is p-type germanium.

In some examples of such cases, each liner is included in the composition of the corresponding cap layer (so that different and independent liners may not be distinguishable from different and independent cap layers).

In some cases, at least one of the cap layers further includes misalignment and/or penetration and/or twin crystals, while in other cases, the cap layer has no misalignment, penetration, and Twin crystals.

Another embodiment of the present invention includes an electronic device having a printed circuit board, wherein the printed circuit board has an integrated circuit including one or more transistor devices of various definitions in this paragraph.

In one such case, the integrated circuit includes at least one of a communication chip and/or a processor.

In some cases, the electronic device is a computing device.

[00090]

Other embodiments of the present invention provide an integrated circuit.

The circuit includes a substrate (such as silicon, SiGe, or germanium) having a channel region, a gate electrode on the channel region, a source/drain region formed on or in the substrate and adjacent to the channel region, and Metal germanide source and drain contacts.

Each of the source and drain regions has a total thickness, which includes a p-type liner layer of silicon or germanium or silicon germanium and a p-type cap layer with a germanium concentration exceeding 80 atomic percent, where the liner layer is the total thickness 40% or less.

In some cases, the thickness ratio of the thickness of the lining layer to the thickness of the cap layer is 1:5 or lower.

In some cases, at least one of the cap layers further contains tin.

[00091]

Another embodiment of the present invention provides a method for forming a transistor device.

The method includes providing a substrate with a channel region, providing a gate electrode on the channel region, and providing source and drain regions formed on or in the substrate and adjacent to the channel region.

Each of the source and drain regions has a total thickness, which includes a p-type liner layer of silicon or germanium or silicon germanium and a p-type cap layer with a germanium concentration exceeding 80 atomic percent, wherein the liner layer is less than the total thickness 50% of it.

In some cases, the method includes providing source and drain contacts of the metal germanide.

In some cases, the thickness ratio of the lining layer thickness to the cap layer thickness is 2:5 or lower.

In some cases, at least one of the liner layer and/or the cap layer has at least one of the gradually changing concentrations of germanium and/or the p-type dopant.

In some cases, at least one of the cap layers further contains tin (or other suitable strain inducers).

[00092]

In the foregoing, the description of the exemplary specific embodiments of the present invention has been provided for the purpose of illustration and description.

This is not intended to be exhaustive or to limit the invention to the precise form disclosed.

According to the contents of this manual, many modifications and changes are possible.

For example, although some embodiments of the present invention utilize in-situ boron doping of germanium, other embodiments may use intrinsic germanium, which is subsequently deposited with p-type dopants and an annealing process to provide The required p-type doping concentration.

In addition, some embodiments may include source and drain regions fabricated as described herein, but still use traditional processes (such as implantation and annealing) to form the top of the source and drain regions.

In this embodiment, the tip may have a lower germanium and/or p-type dopant concentration than the main source and drain regions, which may be acceptable in certain applications.

In other embodiments, only the top of the source and drain regions can be configured to have high germanium and p-type dopant concentrations, and the main part of the source and drain regions can have conventional or lower germanium. / Concentration of dopants.

The scope of the present invention is not intended to be limited to this detailed description, but is limited by the scope of the attached patent application.

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1.

An integrated circuit device comprising: a semiconductor body including at least one of silicon and germanium; at least a gate structure on the semiconductor body, the gate structure including a gate electrode and the semiconductor body and the gate A gate dielectric between the electrodes; a source structure or a drain structure adjacent to the semiconductor body, the source structure or the drain structure comprising a first part and a second part, the first part comprising at least one of silicon and germanium , And the second part includes p-type dopants, germanium, and tin. The second part has a germanium concentration exceeding 80 atomic percent and a tin concentration ranging from 1 to 20 atomic percent, wherein the first portion is larger than the second Part is thin; and a contact structure on the second part of the source structure or the drain structure.

11.

Such as the device of the first item in the scope of patent application, wherein the p-type dopant is gallium.

21.

Such as the device of the first item in the scope of patent application, wherein the tin concentration is in the range of 3 to 8 atomic percent.

31.

For example, in the device of the first item of the scope of the patent application, in addition to the p-type dopant, the second part is mainly composed of germanium and tin.

41.

Such as the device of item 4 in the scope of patent application, wherein the tin concentration is in the range of 3 to 8 atomic percent.

51.

Such as the device of the first item in the scope of patent application, where the second part also contains silicon.

61.

For example, in the device of item 6 of the scope of patent application, in addition to the p-type dopant, the second part is mainly composed of germanium, silicon, and tin.

71.

Such as the device of item 7 in the scope of patent application, wherein the tin concentration is in the range of 3 to 8 atomic percent.

81.

Such as the device of the first item in the scope of patent application, wherein the semiconductor body is mainly composed of germanium or silicon and germanium, and the first part of the source structure or the drain structure is mainly composed of silicon or silicon and germanium.

91.

For example, the device of the 9th item of the scope of patent application further includes a germanium substrate, wherein the semiconductor body is a part of the substrate or is different from the substrate.

101.

Such as the device of any one of items 1-10 in the scope of patent application, wherein the semiconductor body includes a fin or a nanowire.

111.

An integrated circuit device comprising: a semiconductor body including at least one of silicon and germanium; a gate structure on a plurality of sides of the semiconductor body, the gate structure including a gate electrode and a gate electrode on the semiconductor body and The gate dielectric between the gate electrodes; the source structure or the drain structure adjacent to the semiconductor body, the source structure or the drain structure comprising a first part and a second part, the first part comprising silicon and germanium At least one, and the second part contains p-type dopants and germanium, the second part has a germanium concentration exceeding 80 atomic percent, wherein the first part is thinner than the second part, and wherein the first part is in the second part Between the two parts and the semiconductor body, and wherein the second part includes one or more differential rows, the one or more differential rows include misaligned rows, penetrating rows, or originating from crystals straddling the twin crystal planes. At least one of the changed defects in the grid orientation; and the contact structure on the second part of the source structure or the drain structure.

121.

Such as the device of item 12 of the scope of patent application, wherein the second part further contains tin, and the tin concentration ranges from 3 to 8 atomic percent.

131.

For example, in the device of item 12 of the scope of patent application, in addition to the p-type dopant, the second part is mainly composed of germanium.

141.

For example, in the device of item 12 of the scope of patent application, in addition to the p-type dopant, the second part is mainly composed of germanium and silicon.

151.

Such as the device of the 12th patent application, wherein the semiconductor body is mainly composed of silicon, and the first part of the source structure or the drain structure is mainly composed of silicon or silicon and germanium.

161.

Such as the device of the 12th patent application, wherein the semiconductor body is mainly composed of germanium, and the first part of the source structure or the drain structure is mainly composed of silicon or silicon and germanium.

171.

Such as the device of any one of items 12-17 of the scope of patent application, wherein the semiconductor body includes a fin and the gate structure is on three sides of the fin.

181.

Such as the device of any one of items 12-17 in the scope of the patent application, wherein the one or more shifts include at least one shift shift.

191.

Such as the device of any one of items 12-17 in the scope of the patent application, wherein the one or more differential rows include at least one penetration differential row.

201.

Such as the device of any one of items 12-17 in the scope of the patent application, wherein the one or more difference rows include at least one defect originating from a change in the orientation of the crystal lattice across the twin crystal plane.

211.

An integrated circuit device comprising: a semiconductor nanowire, which contains at least one of silicon and germanium; a gate structure surrounding the semiconductor nanowire, the gate structure including a gate electrode and a gate electrode on the semiconductor nanowire and The gate dielectric between the gate electrodes; the source structure or the drain structure adjacent to the semiconductor nanowire, the source structure or the drain structure comprising a first part and a second part, the first part comprising silicon and At least one of germanium, and the second part includes p-type dopants and germanium, the second part has a germanium concentration exceeding 80 atomic percent, wherein the first part is thinner than the second part, and the first part is Between the second part and the semiconductor nanowire, and wherein the second part includes one or more differential rows, the one or more differential rows include misaligned rows, penetrating rows, or originating from across double At least one of the defects in the crystal lattice orientation of the crystal plane; and the contact structure on the second part of the source structure or the drain structure.

221.

For example, in the device of the 22nd patent application, the semiconductor nanowire is mainly composed of silicon, and the first part of the source structure or the drain structure is mainly composed of silicon or silicon and germanium.

231.

Such as the device of the 22nd patent application, in which the semiconductor nanowire is mainly composed of germanium, and the first part of the source structure or the drain structure is mainly composed of silicon or silicon and germanium.

241.

For example, the device of the 22nd patent application, wherein the semiconductor nanowire is mainly composed of silicon and germanium, and the first part of the source structure or the drain structure is mainly composed of silicon or silicon and germanium.

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(56)參考文獻：

US	5089872B	US	20050130454A1
US	20050130454A1	US	20090075029A1
WO	2010014246A1		

林庭宇(學位論文)，矽奈米線場效電晶體之研究，2009 年 08 月 05 日
審查人員：黃本立
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(54)名稱

用於ＰＭＯＳ整合之第ＩＶ族電晶體

(57)摘要

所揭露之技術係用以形成第 IV 族電晶體裝置，其具有高鍺濃度之源極/汲極區域，且相對傳統裝置表現出降低的寄生電阻。在某些範例具體實施例中，源極/汲極區域之每一者包括薄的 p 型矽或鍺或矽鍺沉積，且源極/汲極材料沉積的剩餘物為 p 型鍺或鍺合金(例如鍺：錫或其他適合的應變誘導物，且具有至少 80 原子百分比的鍺含量及 20 原子百分比或更低的其他成分)。在某些情況中，應變鬆弛的證據可於富含鍺的蓋層中觀察到，包括錯位差排及/或穿透差排及/或雙晶。可使用許多電晶體組態，包括平面及非平面電晶體結構兩者(例如鰭式場效電晶體及奈米線電晶體)、以及應變及非應變通道結構。

Techniques are disclosed for forming column IV transistor devices having source/drain regions with high concentrations of germanium, and exhibit reduced parasitic resistance relative to conventional devices. In some example embodiments, the source/drain regions each includes a thin p-type silicon or germanium or SiGe deposition with the remainder of the source/drain material deposition being p-type germanium or a germanium alloy (e.g., germanium: tin or other suitable strain inducer, and having a germanium content of at least 80 atomic % and 20 atomic % or less other components). In some cases, evidence of strain relaxation may be observed in the germanium rich cap layer, including misfit dislocations and/or threading dislocations and/or twins. Numerous transistor configurations can be used, including both planar and non-planar transistor structures (e.g., FinFETs and nanowire transistors), as well as strained and unstrained channel structures.

指定代表圖：

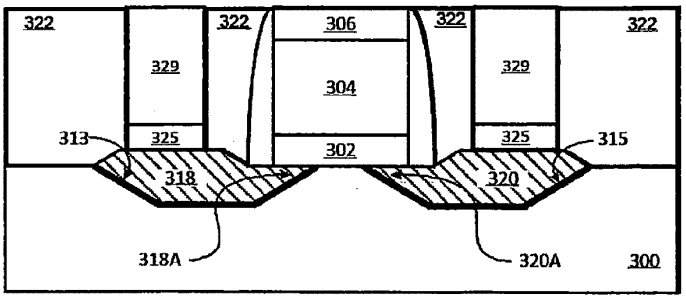


圖3F

符號簡單說明：

300・・・基板

302・・・閘極介電層

304・・・閘極電極

306・・・選擇性硬式遮罩

313・・・襯層

315・・・襯層

318・・・蓋層

318A・・・源極頂端

320・・・蓋層

320A・・・汲極頂端

322・・・絕緣體層

325・・・接觸電阻降低金屬

329・・・接觸插塞金屬

發明專利說明書

（本說明書格式、順序，請勿任意更動）

【發明名稱】(中文/英文)

用於 PMOS 整合之第 IV 族電晶體

Column IV transistors for PMOS integration

【技術領域】

本發明係關於用於 PMOS 整合之第 IV 族電晶體。

【先前技術】

電路裝置（包括電晶體、二極體、電阻、電容、及形成於半導體基板上的其他被動或主動電子裝置）增加的效能一般爲在設計、製造、及操作這些裝置的過程中所要考量的主要因素。舉例來說，在金屬氧化物半導體（MOS）電晶體半導體裝置（例如在互補式金屬氧化物半導體（CMOS）中所使用者）的設計及製造或形成過程中，通常欲最小化關聯於接觸（亦稱作外部電阻 Rext）的寄生電阻。降低的 Rext 能使相同電晶體的設計有更高的電流。

【圖式簡單說明】

圖 1 示意地描述包括源極及汲極頂端區域之一典型 MOS 電晶體之電阻的構件；

圖 2 爲根據本發明之一具體實施例之用以形成第 IV 族電晶體之方法；

圖 3A 至 3F 根據本發明之各種具體實施例描述實施圖 2 之方法所形成之結構；

圖 4A 至 4G 之每一者顯示根據本發明之一具體實施例所形成之 FinFET 電晶體結構的透視圖；

圖 5A 及 5B 之每一者顯示根據本發明之一具體實施例所形成之奈米線電晶體結構的透視圖；以及

圖 6 描述根據本發明之一具體實施例之以一或多個電晶體結構所實施之計算系統。

應理解，圖式未必是以等比例繪出或是意圖限制本發明於所示的特定組態。舉例來說，雖然某些圖式一般係顯示直線、直角、及平滑表面，但鑒於真實世界對所使用之處理設備及技術的限制，電晶體結構的實際實作可能具有較不完美的直線及/或直角，且某些特徵可能具有表面拓撲或是不平滑。簡言之，圖式僅被提供來顯示範例結構。

【發明內容及實施方式】

所揭露之技術係用以形成第 IV 族電晶體裝置，其具有高鍺濃度之源極/汲極區域，且相對傳統裝置表現出降低的寄生電阻。在某些範例具體實施例中，所產生之電晶體結構之源極/汲極區域之每一者包括薄的 p 型矽或鍺或矽鍺（SiGe）襯層，且源極/汲極材料的剩餘物為 p 型鍺或鍺合金，其包括例如鍺及錫，且具有至少 80 原子百分比的鍺含量（及 20 原子百分比或更低的其他成分，例如錫及/或其他適合的應變誘導物。在某些情況中，應變鬆

弛的證據可於此富含鍺之層中觀察到，其包括錯位差排及/或穿透差排。根據本發明，許多電晶體組態以及合適的製造程序將爲顯而易見，其包括平面及非平面電晶體結構兩者（例如鰭式場效電晶體及奈米線電晶體）、以及應變及非應變通道結構。本發明技術特別適於實現 p 型 MOS（PMOS）裝置，然而其他電晶體組態亦可受益。

概述

如前文所解釋，一般可藉由降低裝置外部電阻（Rext）而達成電晶體中增加的驅動電流。然而，PMOS 電晶體效能爲裝置內各種構件電阻的函數，如參照圖 1 所示。通道電阻 R1 可經由載子遷移率（其爲通道內壓縮應變的函數）而調節。裝置的外部電阻 Rext 包括頂端電阻 R2（頂端區域亦稱作源極/汲極延伸）、源極/汲極電阻 R3、及接觸電阻 R4（金屬至半導體）。所有這些分段電阻具有一材料構件（例如橫跨介面的能量屏障、載子濃度及遷移率）、幾何構件（例如長度、寬度等）、及動態電性負載構件（電流擁擠）。

因此，根據本發明某些具體實施例，以 p 型薄襯層及高含量的鍺（具有非常高的 p 型摻雜物濃度）來取代源極/汲極區域中的一般矽或 SiGe 合金材料係最小化外部電阻構件（R2、R3、及 R4）。此外，藉由引入高度壓縮應變的材料，通道電洞遷移率係最大化或增加，因而降低通道電阻（R1）。降低的通道、頂端、源極/汲極及接觸電阻

的靜影響爲在一給定電壓下（相對臨界電壓 V_t，即 $V-V_t$）之改善的電晶體電流。

在某些範例情況中，薄襯層爲 p 型摻雜矽或鍺或 SiGe 合金，且一般小於總源極/汲極沉積層厚度的 50%。剩餘的源極/汲極沉積層厚度一般大於總源極/汲極沉積層厚度的 50%，且可例如爲 p 型摻雜鍺或鍺合金，例如鍺：錫或鍺：錫：x（其中 x 例如爲矽或其他微量的成分或基於製程/擴散的人爲產物），具有至少 80 原子百分比的鍺及 20 原子百分比或更少的其他成分（例如錫及/或任何其他合適的應變誘導物及/或其他微量無意的成分）。在某些特殊的此類範例具體實施例中，源極/汲極襯層與高濃度鍺蓋層的厚度比爲約 1：5 或更低（其中襯層構成總源極/汲極沉積層厚度之約 20%或更低）。在某些此類範例情況中，襯層的厚度爲一到數個單分子層。

本技術可用以形成電晶體裝置於任何數量的裝置及系統。在某些具體實施例中，例如具有 n 型 MOS（NMOS）及 PMOS 電晶體兩者的 CMOS 裝置，可由各種方式來達成選擇性。在一具體實施例中，舉例來說，在 NMOS 源極/汲極位置上的沉積可藉由在 PMOS 沉積過程中將 NMOS 區域屏蔽而避免。在其他具體實施例中，選擇性可包括自然選擇。舉例來說，雖然硼摻雜鍺生成於 p 型 SiGe（或矽）源極/汲極上，但其並不生成於絕緣體表面（例如二氧化矽（SiO2）或氮化矽（SiN））上；其亦不生成於例如 n 型區域中的暴露重度磷摻雜矽上。

本文中所提供的技術可用以改善在任何數量的電晶體結構及組態中的裝置電阻，其包括平面、平齊式或抬升式源極/汲極、非平面（例如奈米線電晶體及鰭式電晶體，例如雙閘極及三閘極電晶體結構）、以及應變及非應變通道結構。源極/汲極區域可爲凹陷（例如使用蝕刻製程）或非凹陷（例如形成於基板的頂表面）。此外，電晶體裝置可選擇性地包括源極及汲極頂端區域，其係設計以例如降低電晶體的整體電阻，同時改善短通道效應（SCE），但此類頂端區域並非必需。電晶體裝置可更包括任何數量的閘極組態，例如多晶閘極、高 k 介電質金屬閘極、替換性金屬閘極（RMG）製程閘極、或任何其他閘極結構。任何數量的結構特徵可與本文所述的低電阻電晶體技術一同使用。

根據某些具體實施例，垂直於閘極線或二次離子質譜儀（SIMS）輪廓的穿透式電子顯微鏡（TEM）橫截面可用以顯示結構中的鍺濃度，因爲矽及 SiGe 的磊晶合金的輪廓可容易地與高鍺濃度輪廓區別。在某些此類含矽基板的情況中，藉由捨棄用以維持應變（無差排）源極/汲極區域的一般需求，源極/汲極填充材料及矽通道之間的晶格維度不匹配對純鍺而言可增加至少 2X，鍺-錫合金可增加更多。在差排出現於富含鍺之蓋層的情況中，雖然不是100%的應變都能夠轉移至通道，但後沉積熱處理可用以提供明確的電晶體效能（在給定 $V-V_t$ 處的電流）增益，即使是鬆弛薄膜（如本文所述），其係相對應變 SiGe 控

制。將理解到，鬆弛一般係表示薄膜可能具有錯位差排，但也可指包括差排形成及傳播的可塑鬆弛機制。彈性鬆弛的程序在非平面組態（例如 FinFET（如三閘極）及奈米結構中變得可能，其中應變材料並未完全受到基板的限制。因此，平面內晶格常數具有更大的彈性來擴張或縮小，而不受基板的影響，且此程序不需錯位差排的形成及傳播。在本文中，鬆弛一詞係用於可塑鬆弛的意義上而非用於彈性鬆弛的意義上。使用錫或其他合適應變誘導物以形成本文所述之高濃度鍺蓋層的合金可選擇性地用以增加通道區域中的應變，藉此透過圖 1 中電阻 R1 的降低而更降低整體的裝置電阻。將理解到，雖然無缺陷的純鍺爲理想的，但對例如矽基板或甚至具有 50 原子百分比鍺之 SiGe 基板上的沉積通常難以無缺陷地成長。然而，意外地，若比較一般完全應變 SiGe 層與具有某些缺陷（例如具有錯位及/或穿透差排）之此類富含鍺層的效能，則有缺陷的富含鍺層將表現較佳。將理解到，此結果一般並不直觀，因爲其違背了傳統對薄膜的了解。無論如何，雖然本發明的某些具體實施例可能包括缺少晶格特徵（例如錯位差排、穿透差排及雙晶（缺陷係源於橫跨雙晶平面之晶格方位中的改變））的富含鍺蓋層，但其他具體實施例可包括具有一或多個此類特徵的富含鍺蓋層。

結構及方法學

圖 2 爲根據本發明之一具體實施例之用以形成第 IV

族電晶體之方法。圖 3A 至 3F 根據本發明之各種具體實施例描述實施圖 2 之方法所形成之範例結構。一或多個此類電晶體可形成於例如處理器、通訊晶片或記憶體晶片的製造中。此類積體電路可接著用於各種電子裝置及系統中。

範例方法包括形成一或多個閘極堆疊於半導體基板上，其中 MOS 裝置可形成於基板上（202）。MOS 裝置可包含例如 PMOS 電晶體、或 NMOS 及 PMOS 電晶體兩者（例如 CMOS 裝置）。圖 3A 顯示所產生的一範例結構，其在此情況中包括形成於基板 300 上之 PMOS 電晶體。可看出閘極堆疊係形成於通道區域之上，且包括閘極介電層 302、閘極電極 304、及選擇性硬式遮罩 306。間隙壁 310 係鄰接閘極堆疊而形成。

閘極介電質 302 可例如爲任何適合的氧化物，例如二氧化矽（SiO_2）或高 k 閘極介電質材料。舉例來說，高 k 閘極介電質材料的範例包括氧化鉿、氧化矽鉿、氧化鑭、氧化鋁鑭、氧化鋯、氧化矽鋯、氧化鉭、氧化鈦、氧化鈦鋇鍶、氧化鈦鍶、氧化鈦鋇、氧化釔、氧化鋁、氧化鉭鈧鉛、及鈮酸鋅鉛。在某些具體實施例中，當使用高 k 材料時，可在閘極介電層 302 上實行退火程序以改善其品質。在某些特定範例具體實施例中，高 k 閘極介電質 302 可具有範圍在 5Å 至 100Å 厚的厚度（例如 10Å）。在其他具體實施例中，閘極介電質 302 可具有一單分子層氧化材料的厚度。一般來說，閘極介電質 302 的厚度應足以將閘極

電極 304 與源極及汲極接觸電性地隔離。在某些具體實施例中，可於高 k 閘極介電質 302 上執行額外的程序，例如退火程序，以改善高 k 材料的品質。

閘極電極 304 的材料可例如爲多晶矽、氮化矽、碳化物、或金屬層（例如鎢、氮化鈦、鉭、氮化鉭），然而也可使用其他合適的閘極電極材料。在某些具體實施例中，閘極電極 304 材料可爲稍後在替換性金屬閘極（RMG）製程移除的一犧牲層，其厚度在約 10Å 至 500Å（例如 100Å）的範圍。

選擇性閘極硬式遮罩層 306 可用以在製造過程中提供某些益處或使用，例如保護閘極電極 304 免於後續的蝕刻及/或佈植製程。硬式遮罩層 306 可使用一般的硬式遮罩材料形成，例如二氧化矽、氮化矽、及/或習知的絕緣體材料。

閘極堆疊可由習知方式形成或使用任何合適的客製化技術形成（例如習知的圖案化製程以蝕刻除去部份的閘極電極及閘極介電質層，以形成圖 2A 所示的閘極堆疊）。閘極介電質 302 及閘極電極 304 材料之每一者可例如使用習知的沉積製程而形成，例如化學汽相沉積（CVD）、分子層沉積（ALD）、旋塗沉積（SOD）、或物理汽相沉積（PVD）。也可使用其他沉積技術，舉例來說，閘極介電質 302 及閘極電極 304 材料可爲熱成長。根據本說明書內容可理解到，可使用任何數量的其他合適材料、幾何、或形成製程來實施本發明的具體實施例，以提供本文所述的

低電阻電晶體裝置或結構。

間隙壁 310 可例如使用習知的材料而形成，例如氧化矽、氮化矽、或其他合適的間隙壁材料。間隙壁 310 的寬度一般可基於所形成電晶體的設計需求而選擇。然而，根據某些具體實施例，間隙壁 310 的寬度並不受到源極及汲極頂端區域之形成所造成的設計限制，其假設在源極/汲極頂端區域有足夠高的 p 型摻雜鍺含量（例如摻雜硼的鍺）或 SiGe 合金襯層。

可使用任何數量的合適基板來實施基板 300，包括塊狀基板、絕緣層上半導體基板（XOI，其中 X 爲半導體材料，例如矽、鍺、或富含鍺的矽）、及多層結構，包括在隨後閘極圖案化製程之前可形成鰭式或奈米線於其上的那些基板。在某些特定範例情況中，基板 300 爲鍺或矽或 SiGe 塊狀基板、或是鍺或矽或 SiGe 於氧化物基板上。雖然本文描述了可形成基板 300 之材料的幾個範例，但可作爲建立低電阻電晶體裝置於其上之基礎的其他合適材料也在所主張之本發明的精神及範疇。

再參考圖 3A，在形成一或多個閘極堆疊後，方法繼續某些選擇性的處理，在此範例具體實施例中包括蝕刻電晶體結構的源極/汲極區域（204），以及去除結構之任何 NMOS 源極/汲極區域的遮罩（若有的話）（206）。將理解到，源極/汲極區域不需爲凹陷或以其他方式蝕刻。在此情況中，源極/汲極材料可形成於基板 300 上而不需任何蝕刻。根據某些具體實施例，雖然此非凹陷源極/汲極

區域將不影響通道電阻，仍可實施具有薄襯層及高鍺含量蓋層的雙層源極/汲極結構，以提供低接觸電阻。更將理解到，並非所有具體實施例都包括 n 型區域。在某些範例情況中，舉例來說，所製造的電路可僅包括 PMOS 裝置。在此類範例情況中，無 n 型源極/汲極區域要被去除遮罩。當出現 n 型區域，可使用任何適合的遮罩技術，以在 p 型處理過程中保護 n 型區域。

在源極/汲極區域被蝕刻的範例具體實施例中，產生源極/汲極凹洞 312/314，如圖 3A 所示。凹洞有效地定義源極/汲極區域的位置。可進一步看出，基板 300 不僅已被蝕刻而產生源極/汲極凹洞 312/314，也產生了底切閘極介電質 302 之其個別的頂端區域 312A/314A。凹洞 312/314 及其個別的頂端區域 312A/314A 可使用任何數量的合適製程而以習知方式形成。在某些範例情況中，這包括離子佈植以高度地摻雜鄰接閘極堆疊之部份的基板 300，接著退火以驅使摻雜物更進入基板 300，以改善預期源極/汲極區域的蝕刻速率。接著，可使用乾蝕刻製程來蝕刻基板 300 的摻雜區域，以形成凹洞 312/314 及其個別的頂端區域 312A/314A。在完成乾蝕刻製程後，可例如使用濕蝕刻以清潔及進一步地蝕刻凹洞 312/314 及其個別的頂端區域 312A/314A。此類濕蝕刻可使用習知或客製的濕蝕刻化學劑而實行，其可用以移除污染物，例如碳、氟、氟氯碳、及氧化物（例如氧化矽），以提供後續製程可實施於其上的乾淨表面。此外，假設一單晶矽表面，濕

蝕刻也可用以沿<111>及<001>結晶面來移除薄的部份基板 300，以提供平滑表面，其中高品質磊晶沉積可發生於其上。在某些範例情況中，被蝕刻移除之薄的部份基板 300 可例如高達 5 奈米厚，且可移除殘留的污染物。濕蝕刻一般會造成凹洞 312/314 及其個別頂端區域 312A/314A 的邊緣沿著<111>及<001>結晶面。

進一步參考圖 2，方法繼續沉積 p 型矽或鍺或 SiGe 襯層 313/315 於 p 型源極/汲極區域（208），且接著在襯層 313/315 之上沉積 p 型鍺或鍺合金於 p 型源極/汲極區域中（210）。這些沉積之每一者可例如使用選擇性磊晶沉積而實現，然而可使用任何合適的沉積製程。參考圖 3B 可看出，p 型矽或鍺或 SiGe 襯層 313/315 係沉積於凹洞 312/314 及其個別頂端區域 312A/314A 中。此外，如圖 3C 所示，凹洞 312/314 及其個別頂端區域 312A/314A 係進一步地填充以提供 p 型鍺或鍺合金的厚蓋層 318/320 於 p 型襯層 313/315 之上。將理解到，p 型摻雜物的範例包括例如硼、鎵、或任何其他合適的 p 型摻雜物，且所主張之本發明並不意欲受限於任何特定一種。

根據基板 300 爲矽或 SiGe 塊狀基板、或絕緣層上半導體基板（XOI，其中 X 爲矽或 SiGe）之某些特定範例具體實施例，源極及汲極凹洞 312/314 及其個別頂端區域 312A/314A 係以原位硼摻雜之矽或 SiGe 填充，藉以形成對應的襯層 313/315，並接著以原位硼摻雜之鍺或富含鍺的合金進一步填充，以形成蓋層 318/320。在基板 300 爲

鍺塊狀基板或絕緣層上鍺基板的其他範例具體實施例中，源極及汲極凹洞 312/314 及其個別頂端區域 312A/314A 可以原位硼摻雜之富含鍺的合金（例如鍺：錫）填充，藉以形成對應的襯層 313/315，並接著以原位硼摻雜之富含鍺合金進一步填充，以形成蓋層 318/320。根據本說明書內容可理解到，襯層 313/315 及蓋層 318/320 的個別鍺或 p 型摻雜物濃度可根據例如以下因素而變化：基板 300 的組成、晶格匹配/相容性之漸次變化的使用、以及總源極/汲極沉積的整體理想厚度。根據本說明書內容可理解到，可實施許多材料系統及 p 型摻雜組態。

舉例來說，在具有矽或鍺或 SiGe 基板的某些範例具體實施例中，襯層 313/315 的鍺含量可在 20 原子百分比至 100 原子百分比的範圍中，且硼濃度在 $1E20cm^{-3}$ 至 $2E21cm^{-3}$ 的範圍中。根據某些具體實施例，爲避免晶格與底下的含矽基板不匹配，襯層 313/315 的鍺濃度可漸次變化。舉例來說，在一此類具體實施例中，襯層 313/315 可爲一漸次變化的硼摻雜 SiGe 層，其具有從相容於底下矽或 SiGe 基板 300 之一基準濃度漸次變化至 100 原子百分比（或接近 100 原子百分比，例如超過 90 原子百分比或 95 原子百分比或 98 原子百分比）的鍺濃度。在一特定的此類具體實施例中，鍺濃度的範圍從 40 原子百分比或更低到超過 98 原子百分比。襯層 313/315 內的硼濃度可例如固定在一高位準或者可漸次變化。舉例來說，襯層 313/315 內的硼濃度可從等於或相容於底下基板 300 之一

基準濃度漸次變化到一理想高濃度（例如，超過 $1E20cm^{-3}$、$2E20cm^{-3}$、或 $5E20cm^{-3}$）而。在某些此類具體實施例中，硼摻雜鍺蓋層 318/320 具有超過 $1E20cm^{-3}$（例如超過 $2E20cm^{-3}$ 或 $2E21cm^{-3}$ 或更高）的硼濃度。此蓋層 318/320 中的硼濃度可以類似於參照襯層 313/315 所描述的方式漸次變化。更一般地來說，硼濃度可依需要調整，以提供所需的傳導率等級，其可根據本說明書內容而理解。舉例來說，蓋層 318/320 的鍺濃度可固定於 100 原子百分比。或者，根據本說明書內容可理解到，蓋層 318/320 的鍺濃度可從低至高濃度（例如從 20 原子百分比至 100 原子百分比）漸次變化，以考量到襯層 313/315 與蓋層 318/320 之理想峰值鍺濃度之間的晶格不匹配。在其他具體實施例中，蓋層 318/320 可由鍺合金來實施，其中混合物可例如爲高達 80 原子百分比的鍺以及高達 20 原子百分比的合金材料（其在某些具體實施例中爲錫）。需注意，將理解到，錫濃度（或其他合金材料）也可漸次變化。在一此情況中，當蓋層 318/320 中的錫濃度範圍在 3 至 8 原子百分比，通道應變將增加（蓋層 318/320 之平衡原子百分比實質爲鍺及任何梯度材料）。儘管鬆弛，晶格常數仍舊相對爲大，且能夠施予足夠的應變於鄰接的通道。其他合適的錫濃度爲顯而易見，其他合適的應變誘導物亦是。

需注意，使用純鍺基板下，襯層 313/315 可由鍺來實現且不需漸次變化。在某些此類情況中，襯層 313/315 的鍺濃度可爲固定（例如 100 原子百分比）且蓋層 318/320

可由鍺合金（例如鍺：錫、或前述之其他合適的鍺合金）來實現。如前文所解釋，蓋層 318/320 中的鍺濃度（或錫或其他合金材料濃度）可漸次變化以產生理想的通道應變。在某些此類的情況中，需進一步注意，鍺襯層 313/315 可有效地與鍺合金蓋層 318/320 整合或可爲源極/汲極區域沉積之一無法偵測的組件。

有關漸次變化，需注意到本文中所使用的相容性並不需要在濃度等級上重疊（舉例來說，底下基板 300 的鍺濃度可爲 0 至 20 原子百分比，且襯層 313/315 的初始鍺濃度可爲 30 至 40 原子百分比）。此外，如本文所使用，有關濃度等級的「固定」一詞意指相對不變的濃度等級（例如層中最低濃度等級爲在該層內之最高濃度等級的 10%）。在更一般的意義上，固定的濃度等級係意指缺乏故意的漸次變化濃度等級。

襯層 313/315 及蓋層 318/320 的厚度也可隨以下因素而變化：基板 300 的組成、晶格匹配/相容性之漸次變化的使用、以及總源極/汲極沉積的整體理想厚度。一般來說，在襯層 313/315 組態爲具有漸次變化的鍺含量以提供與不具有或具有低鍺含量之基板 300 的相容性的情況下，襯層 313/315 可較厚。在其他情況中，當基板 300 爲鍺基板或者含有相對高濃度的鍺，襯層 313/315 不需漸次變化，因此可相對較薄（例如一至數個單分子層）。在其他情況中，當基板 300 不含或具有相對低的鍺含量，襯層 313/315 可由相對薄的矽層或低鍺含量材料層來實施，且

蓋層 318/320 的鍺含量可依相容性所需而漸次變化。在任何此類情況中，襯層 313/315 一般構成少於 50%的總源極/汲極沉積層厚度，且剩餘的源極/汲極沉積層厚度一般大於 50%的總源極/汲極沉積層厚度。根據某些此類範例具體實施例，當襯層 313/315 未漸次變化，襯層 313/315 對蓋層 318/320 的厚度比爲約 2：5 或更低（即襯層構成總源極/汲極沉積層厚度的約 40%或更低）。在某些特定的此類具體實施例中，襯層 313/315 對蓋層 318/320 的厚度比爲約 1：5 或更低（即襯層構成總源極/汲極沉積層厚度的約 20%或更低）。在一此類特定範例情況中，襯層 313/315 的厚度在 1 至數個單分子層到約 10 奈米的範圍中，且總源極/汲極沉積層厚度在 50 至 500 奈米的範圍。根據本說明內容可清楚有許多源極/汲極襯層及蓋層幾何及材料組態。

根據本說明書內容將理解到，本發明具體實施例可實施任何數量的其他電晶體特徵。舉例來說，通道可爲應變或非應變，且源極/汲極區域可包括或不包括形成於對應源極/汲極區域及通道區域之間的頂端區域。從這個意義來說，不論電晶體結構具有應變或非應變通道、或具有源極/汲極頂端區域或不具源極/汲極頂端區域，都與本發明各種具體實施例不特別相關，且所主張之本發明並不意欲受限於任何特定之此類結構特徵。相反地，任何數量的電晶體結構及種類，特別是那些具有 p 型或 n 型及 p 型兩者之源極/汲極電晶體區域的結構，將從使用具有本文所述

之襯層及高鍺濃度蓋層之雙層源極/汲極組態而受益。

可使用 CVD 製程或其他合適的沉積技術來進行沉積（208 及 210）。舉例來說，208 及 210 的沉積可於 CVD 反應器、LPCVD 反應器、或超高真空 CVD（UHVCVD）中實行。在某些範例情況中，反應器溫度可例如落於 600℃至 800℃之間，且反應器壓力可例如落於 1 至 760 托耳之間。載子氣體可例如包括氫或氮，其具有適當的流速，例如在 10 至 50 SLM 之間。在某些特定具體實施例中，可使用鍺源前驅物氣體（例如在 H_2 中稀釋的 GeH_4（舉例來說，GeH_4 可稀釋爲 1-20%））來實行沉積。舉例來說，稀釋的 GeH_4 可在 1%濃度及流速範圍在 50 至 300 SCCM 之間使用。針對硼的原位摻雜，可使用稀釋的 B_2H_6（例如 B_2H_6 可在 H_2 中稀釋爲 1-20%）。舉例來說，稀釋的 B_2H_6 可在 3%濃度及流速範圍在 10 至 100 SCCM 之間使用。在某些範例情況中，可加入蝕刻劑，以增加沉積的選擇性。舉例來說，可加入流速範圍在例如 50 至 300 SCCM 之間的 HCl 或 Cl_2。

根據本說明書內容，源極/汲極雙層結構上的各種變化將爲顯而易見。舉例來說，在某些具體實施例中，襯層 313/315 係由磊晶沉積的硼摻雜 SiGe 所實施，其可爲一或多層且具有範圍在 30 至 70 原子百分比或更高的鍺濃度。如前文所解釋，此 SiGe 襯層的鍺濃度可爲固定或漸次變化，以從基準（接近基板 300）增加至高位準（例如超過 50 原子百分比，接近蓋層 318/320 之鍺濃度的基準濃度，

鍺持續漸次變化至 100 原子百分比）。在某些此類具體實施例中的硼濃度可超過 1E20 cm^{-3}，例如高於 5E20 cm^{-3} 或 2E21 cm^{-3}，且亦可漸次變化以從接近基板 300 的基準增加至高位準（例如超過 1E20 cm^{-3} 或 2E20 cm^{-3} 或 3E20 cm^{-3} 等，接近蓋層 318/320）。在硼摻雜 SiGe 襯層 313/315 的鍺濃度爲固定的具體實施例中，可使用薄的漸次變化緩衝以較佳地連接襯層 313/315 與硼摻雜蓋層 318/320。需注意，此緩衝可爲一中間層或整合至蓋層 318/320 的成分中。爲了此揭露的目的，此緩衝可視爲蓋層 318/320 的部份。根據某些特定範例具體實施例，硼摻雜 SiGe 沉積層（或層的集合）313/315 的厚度可例如在數單分子層至 50 奈米的範圍，而層（或層的集合）318/320 可具有範圍在例如 51 至 500 奈米的厚度，然而其他具體實施例可具有其他的襯層及蓋層厚度，其根據本說明書內容將爲顯而易見的。在某些具體實施例中，需注意到凹洞 312/314 可在循環的沉積-蝕刻製程過程中產生於間隙壁底下，且這些凹洞 312/314 也可由磊晶蓋層回填（其可例如具有與硼摻雜鍺蓋層 318/320 相同的成分）。

鑒於本說明書內容將更理解到，高鍺濃度（例如超過 50 原子百分比且高達純鍺）及高硼濃度（例如超過 1E20cm^{-3}）的組合（如本文所討論）可用以主要地實現在 PMOS 電晶體裝置中之源極及汲極區域（圖 1 中的 R3）以及其個別的頂端區域（圖 1 中的 R2）中較高的傳導率。此外，如前文所解釋，因爲相對於低鍺成分層，硼擴散在

高鍺成分層中係足夠地被抑制，儘管在沉積應力源薄膜中的高摻雜濃度，當相較於具有相同 p 型摻雜物種類及摻雜等級之較低鍺成分層，可以後續的熱退火實現較少不利的 SCE 退化。在接觸表面的較高鍺濃度（其造成圖 1 中的較低接觸電阻 R4）也致能了阻障高度降低。在某些範例具體實施例中，可使用超過 80 原子百分比以及高達純鍺（100 原子百分比）的鍺濃度來達成此益處。然而，需注意到純鍺並非必須。舉例來說，某些具體實施例可具有超過 90 或 95 原子百分比（但不是純的）的鍺濃度。

參考圖 3C 可進一步看出，在相對靠近通道區域中形成源極/汲極頂端 318A/320A 亦施予較大的流體靜力應力於通道上。此應力增加通道內的應變，藉此而增加通道中的遷移率並增加驅動電流。在含矽基板的情況中，此應力可進一步藉由增加源極/汲極頂端 318A/320A 的鍺濃度而放大，而在鍺基板的情況中可藉由增加錫濃度而放大。這是對擴散爲基礎的製程的改善，其中頂端區域一般不包括應變於通道區域上。

一旦根據本發明具體實施例填充源極及汲極區域，可實行各種習知的 MOS 製程以完成 MOS 電晶體的製造，例如替代性閘極氧化物製程、替代性金屬閘極製程、退火、及矽化金屬沉積製程，其可進一步更改電晶體及/或提供必需的電性互連。舉例來說，在源極/汲極區域與其個別頂端的磊晶沉積後，進一步參考圖 2，方法可繼續從 n 型區域移除任何遮罩並依所需處理這些區域（若可應用，例

如在 CMOS 製程）（212），且沉積絕緣體於電晶體之上（214），且接著以一般的做法平面化該絕緣體層。絕緣體層可使用習知適用於積體電路結構之絕緣體層的材料，例如低 k 介電質（絕緣體）材料。此絕緣體材料包括例如氧化物（如二氧化矽（SiO2）及碳摻雜氧化物（CDO））、氮化矽、有機聚合物（例如八氟環丁烷、聚四氟乙烯）、氟矽玻璃（FSG）、及有機矽酸鹽（例如半矽氧烷、矽氧烷、或有機矽酸鹽玻璃）。在某些範例組態中，絕緣體層可包括細孔或其他孔洞，以進一步降低其介電質常數。圖 3D 描述沉積絕緣體層 322 並接著將其平面化至硬式遮罩 306 的一範例。

參考圖 3D'可進一步看出，本發明的某些具體實施例使用一替代性金屬閘極製程，且方法可包括使用習知的蝕刻製程移除閘極堆疊（包括高 k 閘極介電質層 302、犧牲閘極電極 304、及硬式遮罩層 306）。在另一實施中，僅移除犧牲閘極 304。若移除閘極介電質 302，則方法可包括沉積新的閘極介電質層至溝渠開口。在此可使用任何合適的高 k 介電質材料（如前文所描述），例如氧化鉿。也可使用相同的沉積製程。可使用閘極介電質 302 的取代，以例如解決在乾式及濕式蝕刻製程的應用過程中發生在最初閘極介電質層的任何損壞，及/或以高 k 或其他理想的閘極介電質材料來取代低 k 或犧牲介電質材料。方法接著可繼續沉積金屬閘極電極層至溝渠中及閘極介電質層之上。可使用習知的金屬沉積製程以形成金屬閘極電極層，

例如 CVD、ALD、PVD、無電電鍍、或電鍍。金屬閘極電極層可包括例如 p 型功函數金屬，例如釕、鈀、鈷、鎳、及導電金屬氧化物（例如氧化釕）。在某些範例組態中，可沉積二或更多金屬閘極電極層。舉例來說，可沉積功函數金屬，接著沉積合適的金屬閘極電極填充金屬，例如鋁。圖 3D'描述根據本發明一具體實施例之一範例高 k 閘極介電質層 324 以及金屬閘極電極 326，其已沉積至溝渠開口中。需注意，若需要的話，此 RMG 程序可在製程中的不同時間點實行。

進一步參考圖 2，在形成絕緣體層 322 後（及任何所需的預先接觸形成 RMG 製程），方法繼續蝕刻以形成源極/汲極接觸溝渠（216）。可使用任何合適的乾式及/或濕式蝕刻製程。圖 3E 顯示根據一範例具體實施例之在完成蝕刻後的源極/汲極接觸溝渠。

接著，方法繼續沉積接觸電阻降低金屬及退火（218），接著沉積源極/汲極接觸插塞（220）。圖 3F 顯示接觸電阻降低金屬 325，其在某些具體實施例中包括銀、鎳、鋁、鈦、金、金-鍺、鎳-鉑、或鎳-鋁、及/或其他此類電阻降低金屬或合金。圖 3F 更顯示接觸插塞金屬 329，其在某些具體實施例中包括鋁或鎢，然而可使用任何合適的導電接觸金屬或合金，例如銀、鎳-鉑或鎳-鋁或鎳及鋁的其他合金、或鈦，其使用習知的沉積製程。源極/汲極接觸的金屬化可例如使用鍺化製程（一般來說，接觸金屬的沉積及後續的退火）。舉例來說，可使用具有

鎳、鋁、鎳-鉑或鎳-鋁或鎳及鋁的其他合金、或鈦的鍺化（包含或不包含鍺預非晶佈植）來形成低電阻鍺化物。硼摻雜鍺蓋層 318/320 允許金屬-鍺化物形成（例如鎳-鍺）。鍺化物允許比傳統金屬-矽化物系統明顯較低的蕭特基-阻障高度及改善的接觸電阻。舉例來說，傳統的電晶體一般使用源極/汲極 SiGe 磊晶製程，其鍺濃度的範圍在 30 至 40 原子百分比。此傳統的系統展現約 140 歐姆-微米的 Rext 值，受限於磊晶/矽化物介面電阻，其爲高且可能阻礙未來的閘極節距縮放。本發明的某些具體實施例允許 PMOS 裝置中 Rext 的顯著改善（例如 2x 或更佳的改善，例如約 70 歐姆-微米或更低的 Rext），其可較佳地支援 PMOS 裝置縮放。因此，相較於傳統的電晶體，具有組態爲如本文所述之雙層源極/汲極結構之源極/汲極的電晶體可展現相對較低的 Rext 值。

非平面組態

非平面架構可例如使用鰭式電晶體或奈米線組態而實施。FinFET 爲圍繞一半導體材料薄條（一般稱作鰭）而建立的電晶體。電晶體包括標準場效電晶體（FET）節點，包括閘極、閘極介電質、源極區域、及汲極區域。裝置的傳導通道位在閘極介電質底下、鰭的外側之上/之內。特別地，電流沿鰭的兩側壁（垂直基板平面之側）流動，也沿鰭的頂部（平行基板平面之側）流動。因爲此組態的傳導通道主要位在沿鰭的三個不同的外部、平面區

域，此一 FinFET 設計有時稱作三閘極 FinFET。其他類型的 FinFET 組態也可使用，例如所謂的雙閘極 FinFETs，其中傳導通道主要僅位於沿鰭的兩側壁（沒有沿著鰭的頂部）。

圖 4A 至 4G 之每一者顯示根據本發明一具體實施例形成之 FinFET 電晶體結構的透視圖。將理解到，前文有關圖 2 至圖 3F 的討論同樣可用於此處。可看出，圖 4A 所示之範例非平面組態係以鰭式結構來實施，包括基板 400，其具有半導體本體或鰭 410 從基板 400 延伸通過淺溝渠隔離（STI）層 420。基板可例如爲矽、鍺、或 SiGe。

圖 4B 顯示形成於鰭 410 之三個表面之上的閘極電極 440，以形成三個閘極（因此爲三閘極裝置）。閘極介電質材料 430 係形成於鰭 410 與閘極電極 440 之間，且硬式遮罩 450 係形成於閘極電極 440 的頂部。圖 4C 描述在沉積絕緣材料及後續蝕刻（其留下絕緣體材料之覆層於所有垂直表面上，以形成間隙壁 460）後所產生的結構。

圖 4D 描述在額外蝕刻處理後所產生的結構，其從鰭 410 的側壁消除了多餘的絕緣/間隙壁材料，而僅留下間隙壁 460 在閘極電極 440 的相對側壁。圖 4E 描述在凹槽蝕刻後所產生的結構，其移除了基板 400 之源極/汲極區域中的鰭 410，從而形成凹槽 470。需注意，其他具體實施例可無凹槽（例如源極/汲極區域與 STI 層 420 對齊）。

圖 4F 描述在磊晶襯層 480 生長後所產生的結構，其

可爲薄、p 型並含相當大部份的矽（例如矽或具有 70 原子百分比矽的 SiGe）、或爲純鍺（例如鍺的分隔層、或整合至或包含於蓋層 318/320 的成分中之不可偵測層）。圖 4G 描述在成長磊晶源極/汲極蓋層 490 後所產生的結構，其可爲 p 型且主要包含鍺，但可包含少於 20 原子百分比的錫或其他合適的合金材料，如前文所解釋。根據本說明書內容將可理解到，可使用習知的製程及形成技術以製造本文所述之具有雙層源極/汲極結構 FinFET 電晶體結構。

將進一步理解到，需注意，所示三閘極組態的替代物爲雙閘極架構，其包括介電質/隔離層於鰭 410 的頂部。更需注意，構成圖 4G 所示之源極/汲極區域之襯層 480 及蓋層 490 的範例外形並不意欲限制所主張之本發明於任何特定的源極/汲極種類或形成製程，且根據本說明書內容，其他源極/汲極外形爲顯而易知的（例如可實施圓形、方形或矩形源極/汲極區域）。

圖 5A 顯示根據本發明一具體實施例而形成之奈米線電晶體結構的透視圖。奈米線電晶體（有時稱作環繞式閘極 FET）係類似地組態爲以鰭爲基礎的電晶體，但使用奈米線來代替鰭，且閘極材料一般圍繞通道區域的所有側。根據特定的設計，某些奈米線電晶體具有例如四個等效閘極。圖 5A 描述具有兩個奈米線 510 的奈米線通道架構，然而其他具體實施例可具有任何數量的線。奈米線 510 可由例如 p 型矽或鍺或 SiGe 奈米線來實施。可看出，一奈

米線 510 係形成或提供於基板 400 的凹陷處，且其他奈米線 510 係等效地漂浮在包含襯層 580 及蓋層 590 的源極/汲極材料雙層結構中。如同鰭式組態，需注意可由本文所述之源極/汲極材料的雙層結構取代源極/汲極中的奈米線 510（例如相對薄的矽或鍺或 SiGe 襯層以及相對厚的高濃度鍺蓋層）。或者，雙層結構可形成於最初所形成之奈米線 510 周圍，如圖所示（其中襯層 580 係形成於奈米線 510 周圍，且蓋層 590 接著形成於襯層 580 的周圍）。圖 5B 也描述具有多個奈米線 510 的奈米線組態，但在此範例中，根據本說明書內容可理解，在奈米線形成過程中，非活性材料 511 沒有從個別的奈米線之間移除，其可使用各種習知的技術來實行。因此，一奈米線 510 係形成於基板 400 的凹陷處，而另一奈米線 510 係等效地位於材料 511 的頂部。需注意，奈米線 510 通過通道而作用，但 511 材料則無。可看出，襯層 580 及蓋層 590 的雙層源極/汲極結構係圍繞奈米線 510 的所有其他暴露表面。

範例系統

圖 6 描述一計算系統 1000，其係以根據本發明範例具體實施例而組態之一或多個電晶體結構而實施。可看出，計算系統 1000 內含一主機板 1002。主機板 1002 可包括一些組件，其包括但不限於處理器 1004 及至少一通訊晶片 1006，其每一者可物理地及電性地耦合至主機板 1002，或是整合於其中。將理解到，主機板 1002 可例如

爲任何印刷電路板，不論是主板、架設於主板上的子板、或僅系統 1000 的板等。根據其應用，計算系統 1000 可包括一或多個其他組件，其可或可不物理及電性地耦合至主機板 1002。這些其他組件可包括但不限於揮發性記憶體（如 DRAM）、非揮發性記憶體（如 ROM）、圖形處理器、數位信號處理器、密碼處理器、晶片組、天線、顯示器、觸控螢幕顯示器、觸控螢幕控制器、電池、音頻編解碼器、視頻編解碼器、功率放大器、全球定位系統（GPS）裝置、羅盤、加速度計、陀螺儀、揚聲器、相機、大量儲存裝置（如硬碟驅動、光碟（CD）、數位多功能光碟（DVD）等）。計算系統 1000 所包括的任何組件可包括一或更多本文所述的電晶體結構（例如具有雙層源極/汲極結構，其包含相對薄的 p 型矽或鍺或 SiGe 襯層及相對較厚的 p 型高鍺含量蓋層）。這些電晶體結構可用以例如實施機載處理器快取或記憶體陣列。在某些具體實施例中，多重函數可整合至一或多個晶片（例如，需注意通訊晶片 1006 可爲處理器 1004 的部份或整合至處理器 1004）。

通訊晶片 1006 係致能往返計算系統 1000 之資料轉移的無線通訊。「無線」及其衍生物可用以描述電路、裝置、系統、方法、技術、通訊通道等，其可透過經由非固態媒體之調節電磁輻射的使用來通訊資料。此術語不表示相關裝置不含任何電線，然而其在某些具體實施例中可能不含。通訊晶片 1006 可實現任何數量的無線標準或協

定，包括但不限於 Wi-Fi（IEEE 802.11 家族）、WiMAX（IEEE 802.16 家族）、IEEE 802.20、長期進化（LTE）、Ev-DO、HSPA+、HSDPA+、HSUPA+、EDGE、GSM、GPRS、CDMA、TDMA、DECT、藍牙、其衍生物、以及指定爲 3G、4G、5G 或更高之任何其他無線協定。計算系統 1000 可包括複數個通訊晶片 1006。舉例來說，第一通訊晶片 1006 可專用於較短範圍的無線通訊，例如 Wi-Fi 及藍芽，而第二通訊晶片 1006 可專用於較長範圍無線通訊，例如 GPS、EDGE、GPRS、CDMA、WiMAX、LTE、Ev-DO 及其他。

計算系統 1000 的處理器 1004 包括封裝於處理器 1004 之內的積體電路晶粒。在本發明某些具體實施例中，處理器的積體電路晶粒包括內建記憶體電路，其以一或多個本文所述之電晶體結構（如 PMOS 或 CMOS）所實施。「處理器」一詞可指任何裝置或一裝置的部份，其處理例如來自暫存器及/或記憶體的電子資料並轉換電子資料爲可儲存於暫存器及/或記憶體的其他電子資料。

通訊晶片 1006 也可包括封裝於通訊晶片 1006 內的積體電路晶粒。根據某些此類範例具體實施例，通訊晶片的積體電路晶粒包括以一或多個本文所述之電晶體結構所實施的一或多個電路（例如晶片上處理器或記憶體）。根據本說明書內容將理解到，需注意，多重標準無線能力可直接整合至處理器 1004（例如任何晶片 1006 的功能係整合至處理器 1004 中，而非具有獨立的通訊晶片）。此外，

需注意，處理器 1004 可爲具有此無線能力的晶片組。簡言之，可使用任何數量的處理器 1004 及/或通訊晶片 1006。同樣地，任一晶片或晶片組可具有多個功能整合於其中。

在各種實施中，計算系統 1000 可爲膝上型電腦、輕省筆電、筆記型電腦、智慧型手機、平板電腦、個人數位助理（PDA）、超行動 PC、行動電話、桌上型電腦、伺服器、印表機、掃描器、監視器、機上盒、娛樂控制單元、數位相機、行動音樂播放器、或數位視頻記錄器。在進一步的實施中，系統 1000 可爲處理資料或使用本文所述之低電阻電晶體裝置（如 PMOS 及 CMOS 電路）的任何其他電子裝置。

許多具體實施例將爲明顯的，且本文所述的特徵可結合於任何數量的組態中。本發明一範例具體實施例提供一電晶體裝置。裝置包括具有通道區域的基板、在通道區域之上的閘極電極、及形成於基板之上或之中且鄰接通道區域的源極/汲極區域。源極及汲極區域之每一者具有一總厚度，其包含矽或鍺或矽鍺的一 p 型襯層以及具有鍺濃度超過 80 原子百分比的一 p 型蓋層，其中襯層小於總厚度的 50%。在某些情況中，裝置爲平面、FinFET、或奈米線 PMOS 電晶體之其中一者。在某些情況中，裝置更包括金屬-鍺化物源極/汲極接觸。在某些情況中，襯層厚度對蓋層厚度的厚度比爲 2：5 或更低（襯層爲總厚度的 40%或更低）。在某些情況中，襯層厚度對蓋層厚度的厚度比爲

1：5 或更低（襯層爲總厚度的 20%或更低）。在某些情況中，襯層之每一者具有範圍在約 1 單分子層至 10 奈米的一厚度，且蓋層之每一者具有範圍在約 50 奈米至 500 奈米的一厚度。在某些情況中，襯層及/或蓋層之其中至少一者具有鍺及/或 p 型摻雜物之一漸次變化濃度之至少一者。舉例來說，在某些情況中，襯層之其中至少一者具有一鍺濃度，其從相容於基板之一基準濃度至超過 50 原子百分比之一高濃度而漸次變化。在一此類情況中，高濃度係超過 90 原子百分比。在某些情況中，襯層之其中至少一者具有一 p 型摻雜物濃度，其從相容於基板之一基準濃度至超過 $1E20cm^{-3}$ 之一高濃度而漸次變化。在一此類情況中，一或多個襯層之 p 型摻雜物爲硼。在某些情況中，蓋層之其中至少一者具有超過 95 原子百分比之一鍺濃度。在某些情況中，蓋層之其中至少一者具有從相容於對應襯層之一基準濃度至超過 80 原子百分比之一高濃度而漸次變化的一鍺濃度。在某些情況中，蓋層之其中至少一者具有從相容於對應襯層之一基準濃度至超過 $1E20cm^{-3}$ 之一高濃度而漸次變化的一 p 型摻雜物濃度。在某些情況中，一或多個蓋層之 p 型摻雜物爲硼。在某些情況中，蓋層之其中至少一者更包含錫。許多變化將爲顯而易見的。舉例來說，在某些範例情況中，基板爲含矽基板。在某些此類情況中，p 型襯層包含矽或矽鍺。在其他範例情況中，基板爲鍺基板。在某些此類情況中，p 型襯層爲 p 型鍺。在某些範例的此類情況中，每一襯層係包括在對應蓋

層的成分中（使得不同及獨立的襯層可能無法與不同及獨立的蓋層區別）。在某些情況中，蓋層之其中至少一者更包含錯位差排及/或穿透差排及/或雙晶，而在其他情況中，蓋層無錯位差排、穿透差排、及雙晶。本發明的另一具體實施例包括具有一印刷電路板的一電子裝置，其中印刷電路板具有包括此段落中各種不同定義之一或多個電晶體裝置的一積體電路。在一此類情況中，積體電路包含一通訊晶片及/或一處理器之其中至少一者。在某些情況中，電子裝置爲一計算裝置。

本發明的其他具體實施例提供一積體電路。電路包括一基板（如矽、SiGe、或鍺），其具有通道區域、於通道區域之上的閘極電極、形成於基板之上或之中且鄰接通道區域的源極/汲極區域、以及金屬鍺化物源極及汲極接觸。源極及汲極區域之每一者具有一總厚度，其包含矽或鍺或矽鍺的一 p 型襯層以及具有鍺濃度超過 80 原子百分比的一 p 型蓋層，其中襯層爲總厚度的 40%或更低。在某些情況中，襯層厚度對蓋層厚度的厚度比爲 1：5 或更低。在某些情況中，蓋層之其中至少一者更包含錫。

本發明的另一具體實施例提供用以形成電晶體裝置的一方法。方法包括提供具有一通道區域的一基板、提供在通道區域之上的一閘極電極、以及提供形成於基板之上或之中且鄰近通道區域的源極及汲極區域。源極及汲極區域之每一者具有一總厚度，其包含矽或鍺或矽鍺的一 p 型襯層以及具有鍺濃度超過 80 原子百分比的一 p 型蓋層，其

中襯層小於總厚度的 50%。在某些情況中，方法包括提供金屬鍺化物之源極及汲極接觸。在某些情況中，襯層厚度對蓋層厚度的厚度比爲 2：5 或更低。在某些情況中，襯層及/或蓋層之其中至少一者具有鍺及/或 p 型摻雜物之一漸次變化濃度之至少一者。在某些情況中，蓋層之其中至少一者更包含錫（或其他合適的應變誘導物）。

前文中已提出本發明範例具體實施例的描述作爲說明及描述目的。這並不意圖爲詳盡的或限制本發明於所揭露的精確形式。根據本說明書內容，許多修改及變化是可能的。舉例來說，雖然本發明某些具體實施例利用鍺的原位硼摻雜，但其他具體實施例可使用本質鍺，其在沉積後係接著受到 p 型摻雜物佈植及退火製程以提供所需的 p 型摻雜濃度。此外，某些具體實施例可包括如本文所述而製造的源極及汲極區域，但仍使用傳統製程（例如佈植及退火）來形成源極及汲極區域的頂端。在此具體實施例中，頂端可具有比主要源極及汲極區域低的鍺及/或 p 型摻雜物濃度，其在某些應用中是可接受的。在其他具體實施例中，只有源極及汲極區域的頂端可組態爲具有高鍺及 p 型摻雜物濃度，而源極及汲極區域的主要部份可具有傳統或較低的鍺/摻雜物濃度。本發明的範疇並不意欲受限於此詳細的說明內容，而是由後附之申請專利範圍所限制。

【符號說明】

300：基板

302：閘極介電層

304：閘極電極

306：選擇性硬式遮罩

310：間隙壁

312：凹洞

312A：頂端區域

313：襯層

314：凹洞

314A：頂端區域

315：襯層

318：蓋層

318A：源極頂端

320：蓋層

320A：汲極頂端

322：絕緣體層

324：高 k 閘極介電質層

325：接觸電阻降低金屬

326：金屬閘極電極

329：接觸插塞金屬

400：基板

410：鰭

420：STI 層

430：閘極介電質材料

440：閘極電極

450：硬式遮罩

460：間隙壁

470：凹槽

480：磊晶襯層

490：磊晶源極/汲極蓋層

510：奈米線

511：材料

580：襯層

590：蓋層

1000：計算系統

1002：主機板

1004：處理器

1006：通訊晶片

I690084

發明摘要

【發明名稱】(中文/英文)

用於 PMOS 整合之第 IV 族電晶體

Column IV transistors for PMOS integration

【中文】

所揭露之技術係用以形成第 IV 族電晶體裝置，其具有高鍺濃度之源極/汲極區域，且相對傳統裝置表現出降低的寄生電阻。在某些範例具體實施例中，源極/汲極區域之每一者包括薄的 p 型矽或鍺或矽鍺沉積，且源極/汲極材料沉積的剩餘物爲 p 型鍺或鍺合金（例如鍺：錫或其他適合的應變誘導物，且具有至少 80 原子百分比的鍺含量及 20 原子百分比或更低的其他成分）。在某些情況中，應變鬆弛的證據可於富含鍺的蓋層中觀察到，包括錯位差排及/或穿透差排及/或雙晶。可使用許多電晶體組態，包括平面及非平面電晶體結構兩者（例如鰭式場效電晶體及奈米線電晶體）、以及應變及非應變通道結構。

【英文】

Techniques are disclosed for forming column IV transistor devices having source/drain regions with high concentrations of germanium, and exhibit reduced parasitic resistance relative to conventional devices. In some example embodiments, the source/drain regions each includes a thin p-type silicon or germanium or SiGe deposition with the remainder of the source/drain material deposition being p-type germanium or a germanium alloy (e.g., germanium:tin or other suitable strain inducer, and having a germanium content of at least 80 atomic % and 20 atomic % or less other components). In some cases, evidence of strain relaxation may be observed in the germanium rich cap layer, including misfit dislocations and/or threading dislocations and/or twins. Numerous transistor configurations can be used, including both planar and non-planar transistor structures (e.g., FinFETs and nanowire transistors), as well as strained and unstrained channel structures.

【代表圖】

【本案指定代表圖】：第(3F)圖。

【本代表圖之符號簡單說明】：

300：基板

302：閘極介電層

304：閘極電極

306：選擇性硬式遮罩

313：襯層

315：襯層

318：蓋層

318A：源極頂端

320：蓋層

320A：汲極頂端

322：絕緣體層

325：接觸電阻降低金屬

329：接觸插塞金屬

【本案若有化學式時，請揭示最能顯示發明特徵的化學式】：無

申請專利範圍

1.一種積體電路裝置，包含：

半導體本體，其包含矽和鍺之至少一者；

至少在該半導體本體之上的閘極結構，該閘極結構包括閘極電極和在該半導體本體及該閘極電極之間的閘極介電質；

鄰近該半導體本體的源極結構或汲極結構，該源極結構或汲極結構包括第一部分和第二部分，該第一部分包含矽和鍺之至少一者，且該第二部分包含 p 型摻雜物、鍺、及錫，該第二部分具有超過 80 原子百分比的鍺濃度以及範圍在 1 至 20 原子百分比的錫濃度，其中該第一部分比該第二部分薄；以及

在該源極結構或汲極結構之該第二部分上的接觸結構。

2.如申請專利範圍第 1 項之裝置，其中該 p 型摻雜物是鎵。

3.如申請專利範圍第 1 項之裝置，其中該錫濃度範圍在 3 至 8 原子百分比。

4.如申請專利範圍第 1 項之裝置，其中除了該 p 型摻雜物以外，該第二部分主要由鍺和錫組成。

5.如申請專利範圍第 4 項之裝置，其中該錫濃度範圍在 3 至 8 原子百分比。

6.如申請專利範圍第 1 項之裝置，其中該第二部分還包含矽。

7.如申請專利範圍第 6 項之裝置，其中除了該 p 型摻雜物以外，該第二部分主要由鍺、矽、和錫組成。

8.如申請專利範圍第 7 項之裝置，其中該錫濃度範圍在 3 至 8 原子百分比。

9.如申請專利範圍第 1 項之裝置，其中該半導體本體主要由鍺或矽和鍺組成，且該源極結構或汲極結構之該第一部分主要由矽或矽和鍺組成。

10.如申請專利範圍第 9 項之裝置，更包含鍺基板，其中該半導體本體是該基板的一部分或與該基板不同。

11.如申請專利範圍第 1-10 項之任一項的裝置，其中該半導體本體包含鍺或奈米線。

12.一種積體電路裝置，包含：

半導體本體，其包含矽和鍺之至少一者；

在該半導體本體之多個側邊上的閘極結構，該閘極結構包括閘極電極和在該半導體本體及該閘極電極之間的閘極介電質；

鄰近該半導體本體的源極結構或汲極結構，該源極結構或汲極結構包括第一部分和第二部分，該第一部分包含矽和鍺之至少一者，且該第二部分包含 p 型摻雜物和鍺，該第二部分具有超過 80 原子百分比的鍺濃度，其中該第一部分比該第二部分薄，且其中該第一部分在該第二部分與該半導體本體之間，且其中該第二部分包括一或多個差排，該一或多個差排包括錯位差排、穿透差排、或源於橫跨雙晶平面之晶格方位中的改變的缺陷之其中至少一者；

以及

在該源極結構或汲極結構之該第二部分上的接觸結構。

13.如申請專利範圍第 12 項之裝置，其中該第二部分還包含錫，該錫濃度範圍在 3 至 8 原子百分比。

14.如申請專利範圍第 12 項之裝置，其中除了該 p 型摻雜物以外，該第二部分主要由鍺組成。

15.如申請專利範圍第 12 項之裝置，其中除了該 p 型摻雜物以外，該第二部分主要由鍺和矽組成。

16.如申請專利範圍第 12 項之裝置，其中該半導體本體主要由矽組成，且該源極結構或汲極結構之該第一部分主要由矽或矽和鍺組成。

17.如申請專利範圍第 12 項之裝置，其中該半導體本體主要由鍺組成，且該源極結構或汲極結構之該第一部分主要由矽或矽和鍺組成。

18.如申請專利範圍第 12-17 項之任一項的裝置，其中該半導體本體包含鰭且該閘極結構在該鰭的三個側邊上。

19.如申請專利範圍第 12-17 項之任一項的裝置，其中該一或多個差排包括至少一個錯位差排。

20.如申請專利範圍第 12-17 項之任一項的裝置，其中該一或多個差排包括至少一個穿透差排。

21.如申請專利範圍第 12-17 項之任一項的裝置，其中該一或多個差排包括至少一個源於橫跨雙晶平面之晶格方位中的改變的缺陷。

22.一種積體電路裝置，包含：

半導體奈米線，其包含矽和鍺之至少一者；

圍繞該半導體奈米線的閘極結構，該閘極結構包括閘極電極和在該半導體奈米線及該閘極電極之間的閘極介電質；

鄰近該半導體奈米線的源極結構或汲極結構，該源極結構或汲極結構包括第一部分和第二部分，該第一部分包含矽和鍺之至少一者，且該第二部分包含 p 型摻雜物和鍺，該第二部分具有超過 80 原子百分比的鍺濃度，其中該第一部分比該第二部分薄，且其中該第一部分在該第二部分與該半導體奈米線之間，且其中該第二部分包括一或多個差排，該一或多個差排包括錯位差排、穿透差排、或源於橫跨雙晶平面之晶格方位中的改變的缺陷之其中至少一者；以及

在該源極結構或汲極結構之該第二部分上的接觸結構。

23.如申請專利範圍第 22 項之裝置，其中該半導體奈米線主要由矽組成，且該源極結構或汲極結構之該第一部分主要由矽或矽和鍺組成。

24.如申請專利範圍第 22 項之裝置，其中該半導體奈米線主要由鍺組成，且該源極結構或汲極結構之該第一部分主要由矽或矽和鍺組成。

25.如申請專利範圍第 22 項之裝置，其中該半導體奈米線主要由矽和鍺組成，且該源極結構或汲極結構之該第

一部分主要由矽或矽和鍺組成。

圖式

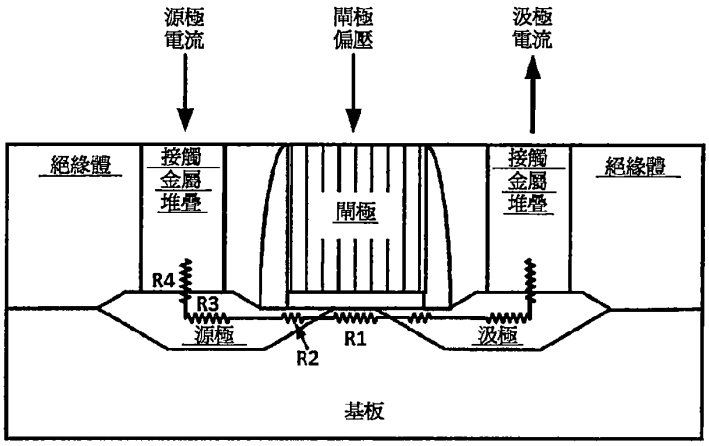


圖1

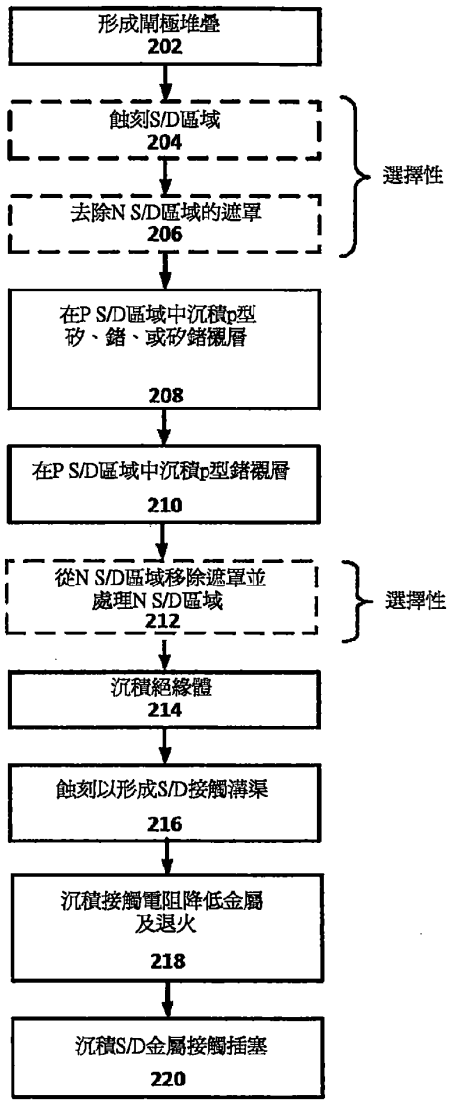

形成閘極堆疊
202
蝕刻S/D區域
204
去除N S/D區域的遮罩
206
選擇性
在P S/D區域中沉積p型
矽、鍺、或矽鍺襯層
208
在P S/D區域中沉積p型鍺襯層
210
從N S/D區域移除遮罩並
處理N S/D區域
212
選擇性
沉積絕緣體
214
蝕刻以形成S/D接觸溝渠
216
沉積接觸電阻降低金屬
及退火
218
沉積S/D金屬接觸插塞
220

圖2

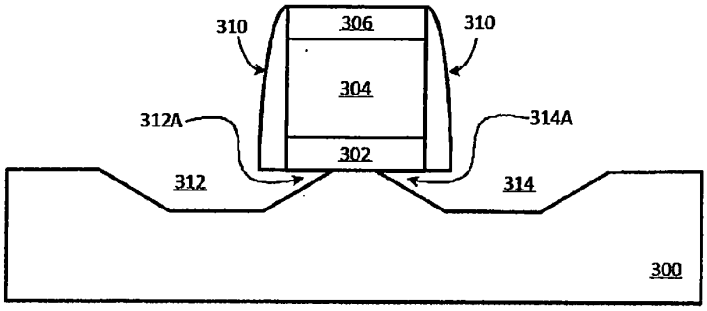

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312A
314A
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圖3A

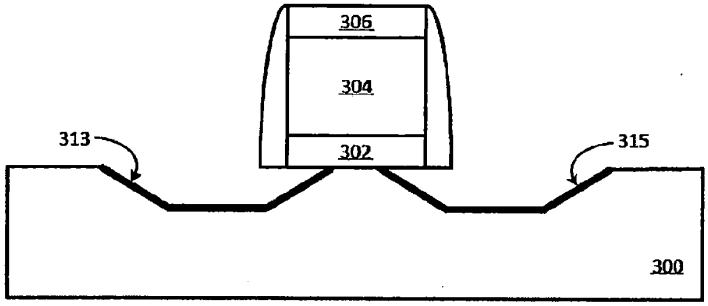

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圖3B

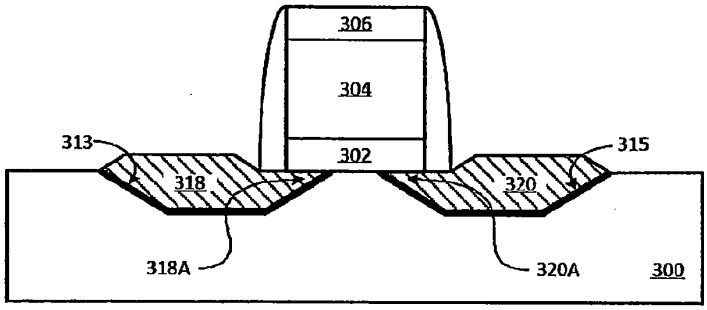

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318A
320A
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圖3C

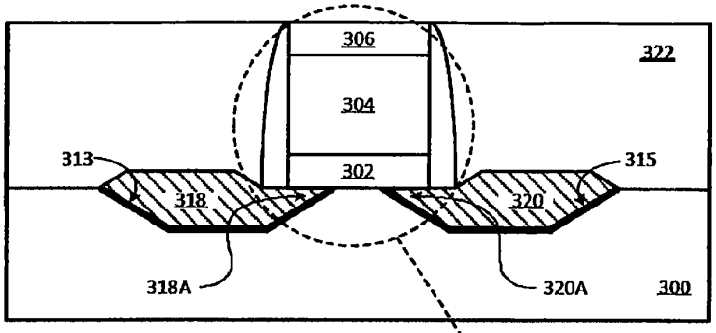


圖 3D

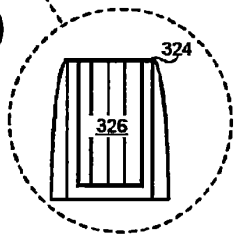


圖 3D'

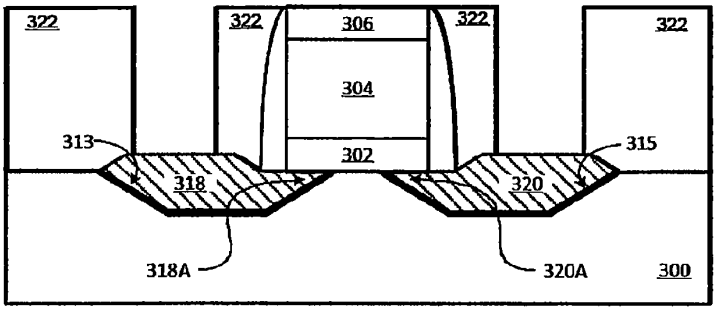


圖 3E

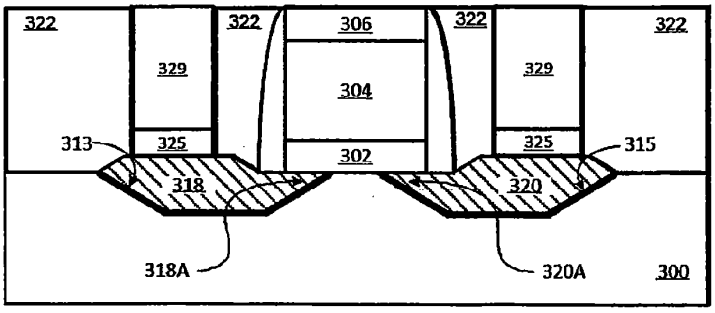


圖 3F

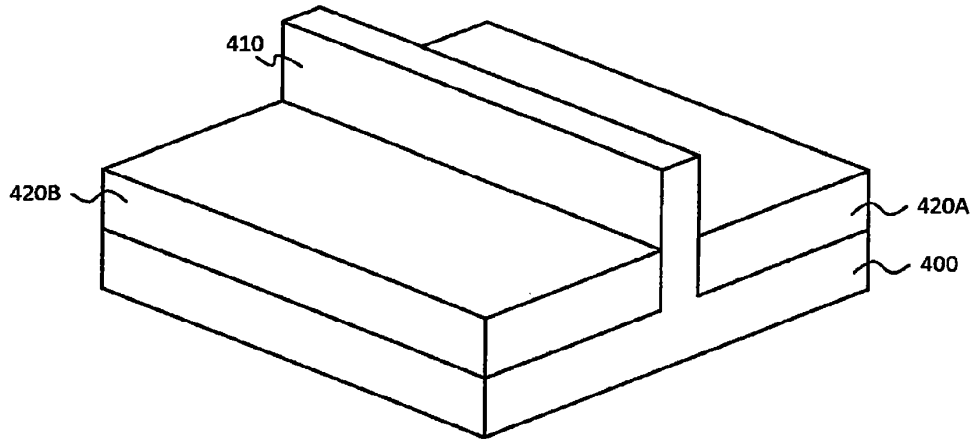


圖4A

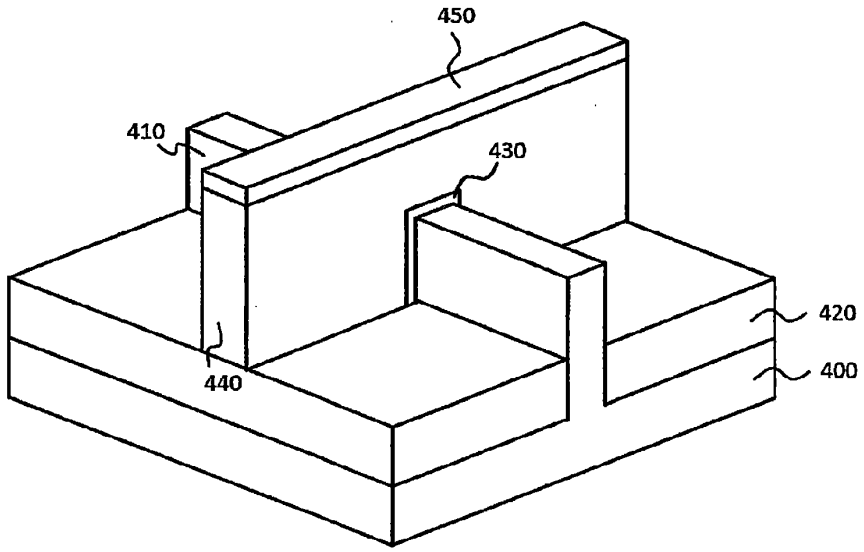


圖4B

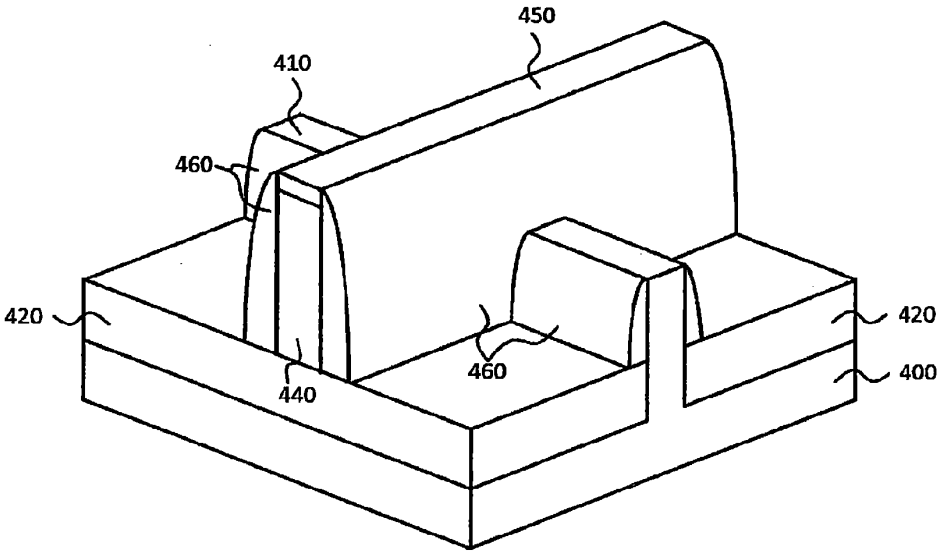


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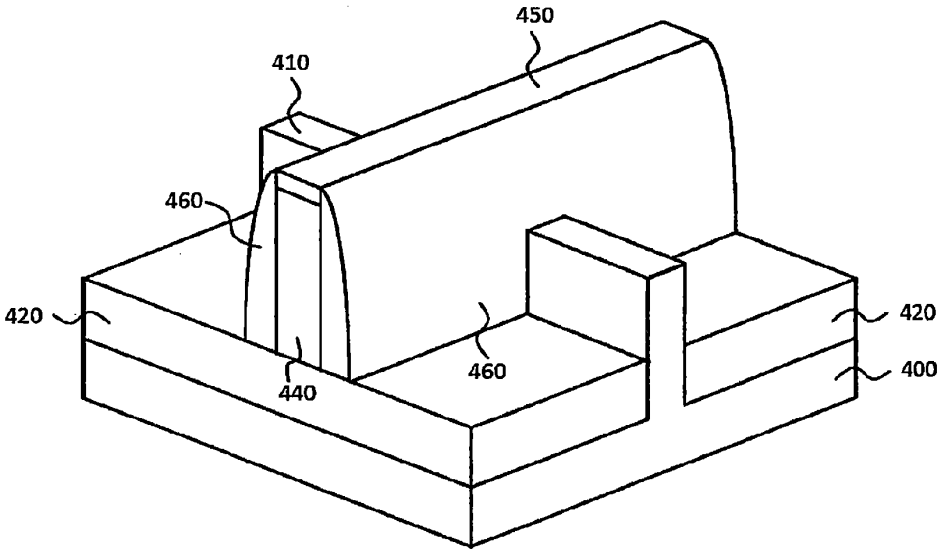


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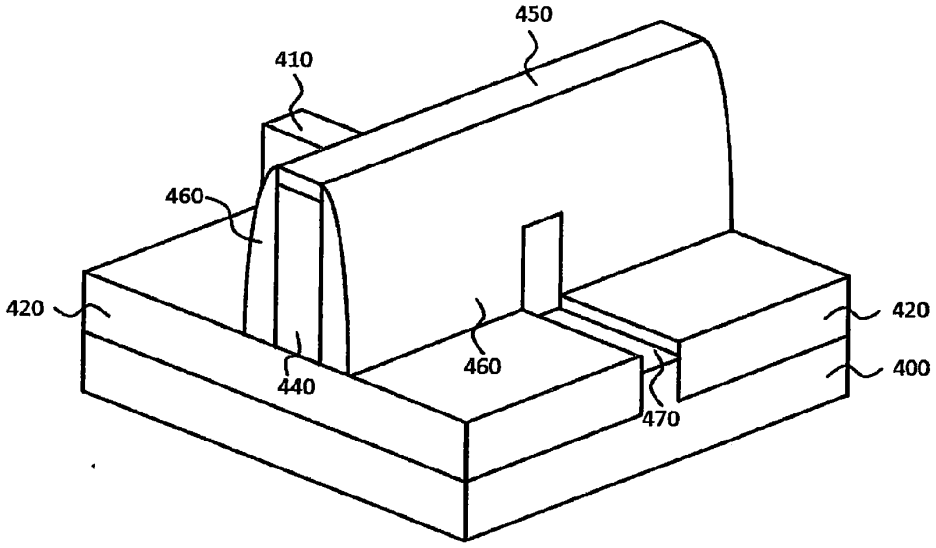

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圖4E

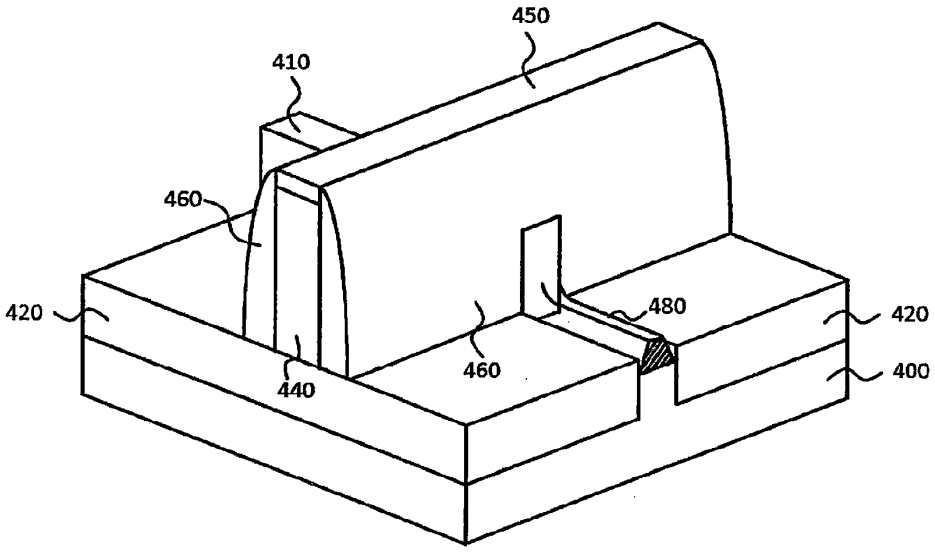

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圖4F

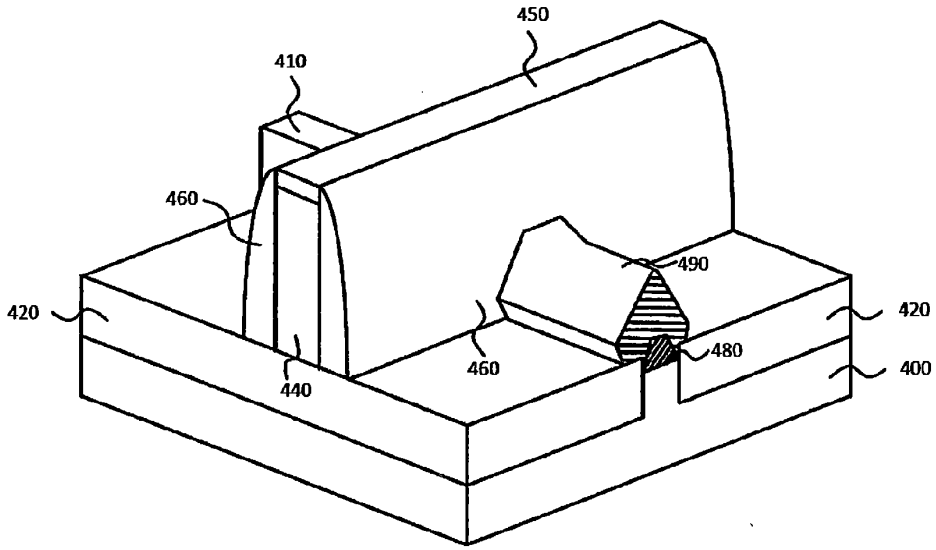

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圖4G

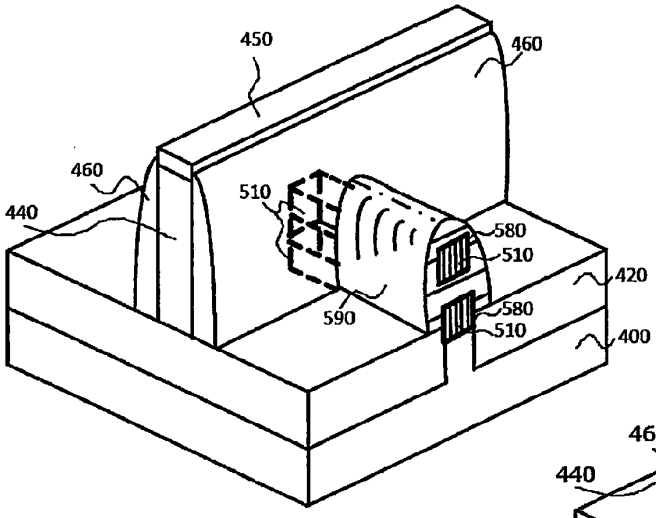
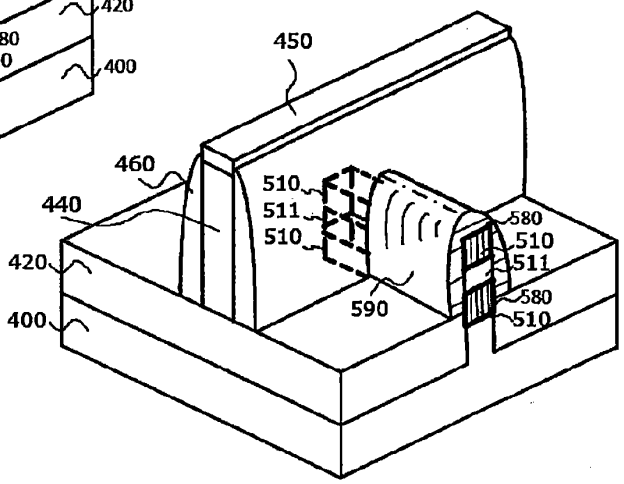

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圖5A

圖5B


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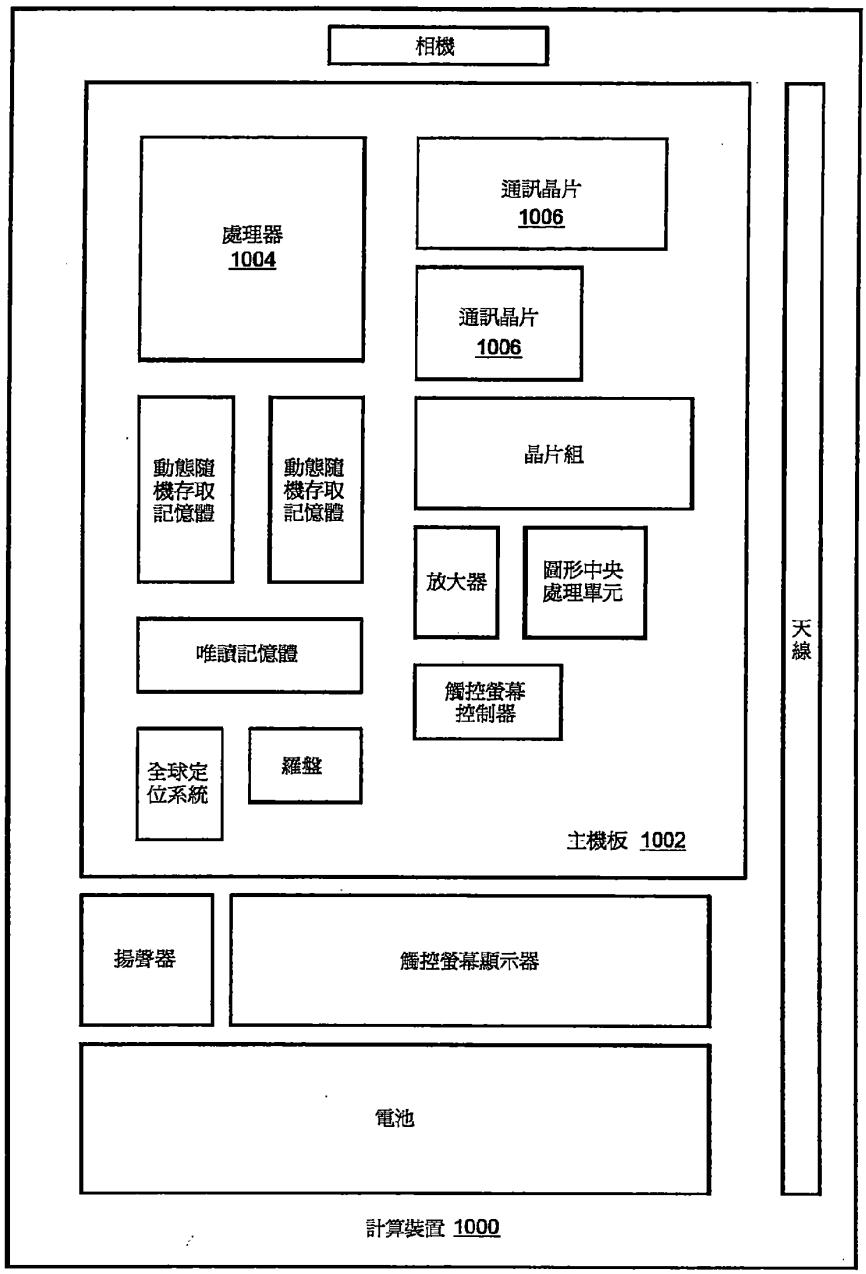

相機
處理器
1004
通訊晶片
1006
通訊晶片
1006
晶片組
動態隨機存取記憶體
動態隨機存取記憶體
放大器
圖形中央處理單元
唯讀記憶體
觸控螢幕控制器
全球定位系統
羅盤
主機板 1002
天線
揚聲器
觸控螢幕顯示器
電池
計算裝置 1000

圖6

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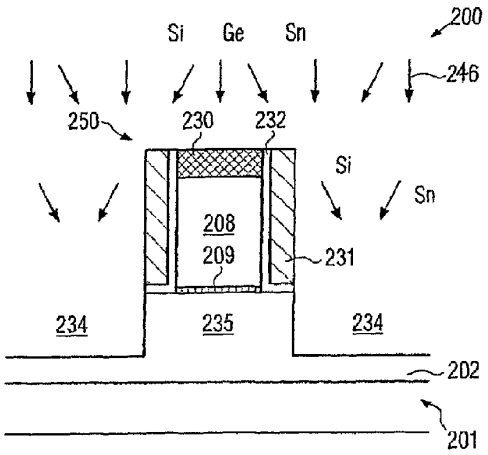
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(54) Title: TECHNIQUE FOR STRAIN ENGINEERING IN SI-BASED TRANSISTORS BY USING EMBEDDED SEMICONDUCTOR LAYERS INCLUDING ATOMS WITH HIGH COVALENT RADIUS



(57) Abstract: By incorporating an atomic species of increased covalent radius, which may at least partially substitute germanium, a highly efficient strain mechanism may be provided, in which the risk of stress relief due to germanium conglomeration and lattice defects may be reduced. The atomic species of increased radius, such as tin, may be readily incorporated by epitaxial growth techniques on the basis of tin hydride.

WO 2007/053381 A1

TECHNIQUE FOR STRAIN ENGINEERING IN SI-BASED TRANSISTORS BY USING EMBEDDED SEMICONDUCTOR LAYERS INCLUDING ATOMS WITH HIGH COVALENT RADIUS

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

Generally, the present invention relates to the formation of integrated circuits, and, more particularly, to the formation of different transistor types having strained channel regions by using embedded silicon/germanium to enhance charge carrier mobility in the channel region of a MOS transistor.

2. DESCRIPTION OF THE RELATED ART

The fabrication of integrated circuits requires the formation of a large number of circuit elements on a given chip area according to a specified circuit layout. Generally, a plurality of process technologies are currently practiced, wherein, for complex circuitry, such as microprocessors, storage chips and the like, CMOS technology is currently the most promising approach due to the superior characteristics in view of operating speed and/or power consumption and/or cost efficiency. During the fabrication of complex integrated circuits using CMOS technology, millions of transistors, *i.e.*, N-channel transistors and P-channel transistors, are formed on a substrate including a crystalline semiconductor layer. A MOS transistor, irrespective of whether an N-channel transistor or a P-channel transistor is considered, comprises so-called PN junctions that are formed by an interface of highly doped drain and source regions with an inversely doped channel region disposed between the drain region and the source region.

The conductivity of the channel region, *i.e.*, the drive current capability of the conductive channel, is controlled by a gate electrode formed above the channel region and separated therefrom by a thin insulating layer. The conductivity of the channel region upon formation of a conductive channel, due to the application of an appropriate control voltage to the gate electrode, depends on the dopant concentration, the mobility of the majority charge carriers, and, for a given extension of the channel region in the transistor width direction, on the distance between the source and drain regions, which is also referred to as channel length. Hence, in combination with the capability of rapidly creating a conductive channel below the insulating layer upon application of the control voltage to the gate electrode, the overall conductivity of the channel region substantially determines the performance of MOS transistors. Thus, the reduction of the channel length, and associated therewith the reduction of the channel resistivity, renders the channel length a dominant design criterion for accomplishing an increase in the operating speed of the integrated circuits.

The continuing shrinkage of the transistor dimensions, however, involves a plurality of issues associated therewith that have to be addressed so as to not unduly offset the advantages obtained by steadily decreasing the channel length of MOS transistors. One major problem in this respect is the development of enhanced photolithography and etch strategies to reliably and reproducibly create circuit elements of critical dimensions, such as the gate electrode of the transistors, for a new device generation. Moreover, highly sophisticated dopant profiles, in the vertical direction as well as in the lateral direction, are required in the drain and source regions to provide low sheet and contact resistivity in combination with a desired channel controllability. In addition, the vertical location of the PN junctions with respect to the gate insulation layer also represents a critical design criterion in view of leakage current control. Hence, reducing the channel length usually also requires reducing the depth of the drain and source regions with respect to the interface formed by the gate insulation layer and the channel region, thereby requiring sophisticated implantation techniques. According to other approaches, epitaxially grown regions are formed with a specified offset to the gate electrode, which are referred to as raised drain and source regions, to provide increased conductivity of the raised drain and source regions, while at the same time maintaining a shallow PN junction with respect to the gate insulation layer.

Since the continuous size reduction of the critical dimensions, *i.e.*, the gate length of the transistors, necessitates the adaptation and possibly the new development of highly complex process techniques concerning the above-identified process steps, it has been proposed to also enhance the channel conductivity of the transistor elements by increasing the charge carrier mobility in the channel region for a given channel length, thereby offering the potential for achieving a performance improvement that is comparable with the advance to a future technology node, while avoiding or at least postponing many of the above process adaptations associated with device scaling. One efficient mechanism for increasing the charge carrier mobility is the modification of the lattice structure in the channel region, for instance by creating tensile or compressive stress in the vicinity of the channel region to produce a corresponding strain in the channel region, which results in a modified mobility for electrons and holes, respectively. For example, creating tensile strain in the channel region increases the mobility of electrons, wherein, depending on the magnitude and direction of the tensile strain, an increase in mobility of 50% or more may be obtained, which, in turn, may directly translate into a corresponding increase in the conductivity. On the other hand, compressive strain in the channel region may increase the mobility of holes, thereby providing the potential for enhancing the performance of P-type transistors. The introduction of stress or strain engineering into integrated circuit fabrication is an extremely promising approach for further device

generations, since, for example, strained silicon may be considered as a "new" type of semiconductor material, which may enable the fabrication of fast powerful semiconductor devices without requiring expensive semiconductor materials, while many of the well-established manufacturing techniques may still be used.

Consequently, it has been proposed to introduce, for instance, a silicon/germanium layer or a silicon/carbon layer in or below the channel region to create tensile or compressive stress that may result in a corresponding strain. Transistor performance may be considerably enhanced by the introduction of stress-creating layers in or below the channel region, and therefore significant efforts have been made to implement the formation of corresponding stress layers into the conventional and well-approved MOS technique. For instance, additional epitaxial growth techniques have been developed and implemented into the process flow to form the germanium or carbon-containing stress layers at appropriate locations in or below the channel region.

In other approaches, external stress created by, for instance, overlaying layers, spacer elements and the like is used in an attempt to create a desired strain within the channel region. However, the process of creating the strain in the channel region by applying a specified external stress may suffer from an inefficient translation of the external stress into strain in the channel region. Hence, although providing advantages in terms of process complexity over the above-discussed approach requiring additional stress layers within the channel region, the efficiency of the stress transfer mechanism may depend on the process and device specifics and may result in a reduced performance gain for one type of transistors.

In another approach, the hole mobility in PMOS transistors is enhanced by forming a strained silicon/germanium layer in the drain and source regions of the transistors, wherein the compressively strained drain and source regions create uniaxial strain in the adjacent silicon channel region. To this end, the drain and source regions of the PMOS transistors are selectively recessed, while the NMOS transistors are masked and subsequently the silicon/germanium layer is selectively formed in the PMOS transistor by epitaxial growth. This technique offers significant advantages in view of performance gain of the PMOS transistor and thus of the entire CMOS device.

Thus, strain engineering by means of embedded semiconductor materials, especially of silicon/germanium, provided as strained or relaxed layers depending on the desired effect, has proven to be a powerful means in increasing the device performance of advanced silicon-based transistors. It turns out, however, that the degree of strain induced in the respective channel regions depends on the amount of lattice mismatch between the basic silicon and the embedded semiconductor compound. For silicon/germanium, a maximum concentration of germanium for currently established epitaxial growth techniques is limited to

approximately 25%, since otherwise germanium conglomeration may occur, which in turn may result in a non-desired stress relief in the corresponding embedded semiconductor compound material, thereby also reducing the strain in the respective channel region.

In view of the above-described situation, there exists a need for an improved technique that enables efficiently increasing strain by embedded semiconductor materials, while substantially avoiding or at least reducing one or more of the above-identified problems.

SUMMARY OF THE INVENTION

The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an exhaustive overview of the invention. It is not intended to identify key or critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is discussed later.

Generally, the present invention is directed to a technique for creating strain in specified regions of a crystalline semiconductor layer, in which a lattice mismatch between a silicon-based lattice, *i.e.*, a lattice having a diamond-like lattice structure, and a semiconductor compound having per se an increased lattice spacing is taken advantage of for this purpose. A corresponding technology is conventionally used for creating strained silicon channels in highly advanced silicon-based MOS transistor elements, wherein, as previously explained, the amount of strain obtained by this mechanism is, among others, significantly restricted by the limited germanium concentration that may be successfully used in currently established epitaxial growth techniques. Therefore, in the present invention, additionally or alternatively to germanium, a further atomic species may be used that has a significantly increased covalent radius with respect to the boding characteristics within a silicon-like crystalline structure, thereby enabling a high degree of crystal distortion with a significantly reduced amount of non-silicon atoms in the respective silicon-based crystalline structure. In illustrative embodiments of the present invention, tin (Sn) may be used as an addition or a substitute for germanium as tin atoms have the same valence compared to silicon and germanium and also exhibit a significantly larger covalent radius.

According to one illustrative embodiment of the present invention, a transistor device comprises a substrate having formed thereon a crystalline semiconductor layer having a diamond-like crystalline structure. The crystalline semiconductor layer comprises a stress-inducing region comprised of silicon and a further atomic species having the same valence as silicon in the crystalline structure and having a covalent radius that is greater

than a covalent radius of germanium. Moreover, the transistor device comprises a gate electrode formed above the crystalline semiconductor layer and a strained channel region.

According to another illustrative embodiment of the present invention, a semiconductor device comprises a crystalline semiconductor layer having a first portion comprising silicon and tin to form a first strained region in the crystalline semiconductor layer.

In accordance with still another illustrative embodiment of the present invention, a method comprises forming, in a crystalline semiconductor layer, a crystalline structure on the basis of silicon and at least one further atomic species having a covalent radius that is greater than a covalent radius of germanium. Moreover, the method comprises using the crystalline structure to create strain in a first specified region of the semiconductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figures 1a-1d schematically show cross-sectional views of a semiconductor device during various manufacturing stages in forming a strained region in a crystalline semiconductor layer on the basis of silicon and a further species that may be built into the diamond structure of silicon and has an increased covalent radius compared to germanium, according to illustrative embodiments of the present invention;

Figures 2a-2d schematically show cross-sectional views during various manufacturing stages in forming a transistor device receiving an embedded strained semiconductor region for creating compressive strain in a respective channel region in accordance with further illustrative embodiments of the present invention; and

Figure 3 schematically illustrates a cross-sectional view of a semiconductor device comprising different transistor elements that receive a different amount of tin for creating a different magnitude of strain in accordance with still another illustrative embodiment of the present invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present invention will now be described with reference to the attached figures. Various structures, systems and devices are schematically depicted in the drawings for purposes of explanation only and so as to not obscure the present invention with details that are well known to those skilled in the art. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present invention. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, *i.e.*, a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, *i.e.*, a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

Generally, the present invention contemplates an enhanced strain-inducing mechanism by means of strained or relaxed semiconductor structures having a diamond-type lattice structure with a different lattice spacing compared to a non-strained silicon crystal. As previously explained, the mechanism of providing a strained or relaxed silicon/germanium layer within appropriate locations of a silicon-based semiconductor device provides an efficient strain engineering technique so as to correspondingly enhance the charge carrier mobility, especially within channel regions of highly advanced MOS transistor devices. These techniques rely on epitaxial growth processes, during which a strained or relaxed silicon/germanium layer may be formed, depending on the device requirements.

Moreover, recently, local selective epitaxial growth techniques have been developed which may effectively suppress a significant material deposition on dielectric surfaces, while efficiently depositing silicon, silicon/germanium and the like on exposed silicon or silicon-like surfaces. For example, if a silicon/germanium

layer is deposited on a crystalline silicon layer, the silicon/germanium material may be deposited so as to have substantially the same lattice spacing as the underlying crystalline "template" so that a strained silicon/germanium layer is formed, since an undisturbed silicon/germanium crystal may have a somewhat enlarged lattice spacing compared to a pure silicon crystal. The difference in lattice spacing of a silicon/germanium layer and a silicon layer depends on the germanium concentration. Therefore, the amount of strain created in the silicon/germanium layer also depends on the germanium concentration. As previously explained, however, in currently used epitaxial growth techniques, a maximum germanium concentration may range up to approximately 25-30%, whereas a higher concentration may actually result in a germanium conglomeration, which in turn may result in an increased defect rate and thus relaxation of the initially strained silicon/germanium layer.

According to the present invention, a desired degree of lattice mismatch and thus strain may be adjusted on the basis of an atomic species having a significantly larger covalent radius compared to germanium, wherein, in some illustrative embodiments, the valence of the atomic species under consideration is substantially identical to silicon or germanium with respect to a covalent bonding structure in a diamond-like crystalline structure. In one illustrative embodiment, tin, having a covalent radius of 1.40 Å, may be used as a suitable atomic species. For example, silicon having a covalent radius of 1.17 Å may be used in combination with germanium having a covalent radius of 1.22 Å, wherein, additionally, a certain amount of tin may be incorporated to create a significantly enlarged lattice mismatch. Since the difference in covalent radius between silicon and tin is significantly higher compared to the difference in radius between silicon and germanium, a more pronounced effect on the overall lattice structure may be achieved with a reduced number of non-silicon atoms. Consequently, the germanium concentration may be kept well below a critical value of approximately 25% while an enhanced lattice mismatch may still be obtained by adding a certain amount of tin.

Furthermore, in some illustrative embodiments, silicon may be used in combination with tin, without adding any germanium, thereby providing a moderately high degree of lattice modification with a significantly reduced number of non-silicon atoms. For example, in some embodiments, it is contemplated to incorporate a certain amount of tin by other techniques such as implantation in addition or alternatively to the incorporation of tin by means of epitaxial growth. Since a reduced number of tin atoms may nevertheless significantly contribute to a lattice distortion, even atomic concentrations achievable by currently used implantation techniques may be sufficient to create a specified strain or at least to fine tune the lattice mismatch and thus the degree of strain achieved thereby. Since ion implantation is a well-established technique, which may be performed at room

temperature on the basis of resist masks formed by photolithography, a corresponding incorporation of tin may be accomplished in a highly efficient and even a highly local fashion, thereby providing additional flexibility in process techniques and device design. For example, a concentration of approximately 10^{20} tin atoms/cm^3, which may be achievable by presently performed implantation techniques, may enable an efficient adjustment or control of strain in a corresponding silicon/tin or silicon/germanium/tin crystalline structure.

In the following detailed description, it may be referred to specific applications of the principles of the present invention, *i.e.*, the incorporation of an atomic species having an enlarged covalent radius so as to create strain in a specified crystalline semiconductor region. It should be appreciated, however, that any restriction to specific transistor architectures, such as SOI-like transistors, bulk devices, transistors having raised drain and source regions and the like, are not intended unless such specific restrictions are explicitly set forth in the detailed description as well as in the appended claims.

With reference to Figures 1a-1d, 2a-2d and 3, further illustrative embodiments of the present invention will now be described in more detail. Figure 1a schematically shows a cross-sectional view of a semiconductor device 100 at an early manufacturing stage. The semiconductor device 100 comprises a substrate 101, which may represent any appropriate substrate for carrying a semiconductor layer 102, in and on which circuit elements, such as transistors, capacitors, resistors and the like, may be formed. For example, the substrate 101 may represent a bulk semiconductor substrate, such as a silicon substrate, or may represent any insulating substrate, such as an SOI-like substrate, wherein the semiconductor layer 102 may be formed on a buried insulation layer (not shown). It should be appreciated that, although the present invention is highly advantageous in combination with highly scaled MOS transistors as are typically fabricated in advanced CMOS technologies including transistors having a gate length of 50 nm and even less, the principles of the present invention may also be applied to less critical applications so that, for existing designs, a significant performance increase may be achieved.

The semiconductor layer 102 may be a silicon-based crystalline semiconductor layer, wherein the term silicon-based is to be understood as a material layer comprising silicon with a concentration of at least atomic 50%. In illustrative embodiments, the semiconductor layer 102 may represent a doped silicon layer as is typically used for highly complex integrated circuits having transistor elements with a gate length in the above specified range. A further substantially crystalline layer 103 may be formed on the layer 102 and may represent a so-called buffer layer, in which the crystalline mismatch and thus the concentration of a specific atomic species such as germanium, tin, and the like may gradually increase to allow for the formation of a substantially relaxed

stress-inducing crystalline layer 104 thereon, which may comprise at least one atomic species in combination with silicon that has a covalent radius that is greater than that of germanium. In one illustrative embodiment, the stress-inducing layer 104 may be comprised of silicon, germanium and tin, wherein a concentration of germanium may range from less than 1% to approximately 25%, while a concentration of tin may range from approximately 0.1-25%. In some embodiments, the germanium content may be selected to be well below 25%, for instance 1-10%, while the tin content may be selected within a range of approximately 0.1-10%. In still other embodiments, the stress-inducing layer 104 may be comprised of silicon and tin substantially without any germanium.

The layer 104 may represent a substantially relaxed layer having a diamond-like structure according to the crystalline template provided by the layer 102 which is transferred via the buffer layer 103 into the layer 104, wherein, however, the lattice spacing of the layer 104 may differ from that of the layer 102 depending on the concentration of germanium and tin.

The semiconductor device 100 as shown in Figure 1a may be formed in accordance with the following processes. After providing the substrate 101, which may represent a silicon bulk substrate or an SOI substrate having formed thereon the layer 102, the thickness of which may be adapted by an epitaxial growth process, the buffer layer 103 may be formed by an epitaxial growth process 105, in which one or more non-silicon species may be deposited with varying concentrations so as to form the buffer layer 103. For example, the formation of silicon/germanium buffer layers on the basis of germanium hydride (GeH_4) is well established and may be used for forming the layer 103 when no additional atomic species, such as tin, is considered appropriate in the buffer layer 103. In other embodiments, the buffer layer 103 may be formed on the basis of a further atomic species such as tin, which may be accomplished by providing tin hydride (SnH_4) as a precursor for the epitaxial growth process 105, wherein tin hydride may be handled in a similar fashion as germanium hydride.

By appropriately depositing the material of the buffer layer 103, a corresponding lattice structure may increasingly deviate from the basic crystalline template of the layer 102 in terms of lattice spacing so that finally the layer 104 may then be deposited as a substantially unstrained, *i.e.*, relaxed, semiconductor layer with an increased lattice spacing compared to the original lattice spacing of the layer 102. For this purpose, during the epitaxial growth process 105, a desired amount of tin and, if desired, a respective amount of germanium may be provided in combination with the silicon, which still represents the majority of the material in the layer 104. After a desired layer thickness is achieved, the epitaxial growth process 105 may be discontinued and a further epitaxial growth process may be performed so as to deposit a substantially crystalline silicon layer above the

layer 104. In other embodiments, the epitaxial growth process 105 may be modified to subsequently deposit silicon, doped or undoped, depending on device requirements, wherein the substantially relaxed layer 104 acts as a crystalline template. Consequently, the silicon deposited thereon may have substantially the same crystalline structure, which represents a strained crystalline structure compared to a natural crystalline silicon layer, such as the layer 102. Consequently, a certain degree of tensile strain may be generated.

Figure 1b schematically shows the semiconductor device 100 in a further advanced manufacturing stage. As is shown, a further crystalline silicon layer 106 is formed in the layer 104 in accordance with the above-described epitaxial growth technique. Consequently, the layer 106 exhibits intrinsic tensile strain, indicated as 107, thereby efficiently modifying the charge carrier mobility in the layer 106. Moreover, a gate electrode 108 is formed above the layer 106 and is separated therefrom by a gate insulation layer 109. The gate electrode 108 in combination with the gate insulation layer 109 defines a channel region 110 within the layer 106, which, as previously explained, exhibits the tensile strain 107, thereby increasing, for instance, the mobility of electrons in the channel region 110. Consequently, the performance of a corresponding transistor element including the gate electrode 108 and the channel region 110 may be significantly enhanced, wherein the degree of tensile strain 107 may be efficiently adjusted and controlled on the basis of the epitaxial growth process 105. Consequently, by means of the stress-inducing layer 104, an efficient strain-creating mechanism may be provided for generating tensile strain in the silicon-based layer 106.

Figure 1c schematically shows the semiconductor device 100 in accordance with another illustrative embodiment, in which compressive strain may be generated in a specified region of a crystalline semiconductor layer. In this embodiment, the stress-inducing layer 104 may be directly formed on the crystalline layer 102, which again acts as a crystalline template during the epitaxial growth process 105, which may now have been configured such that the layer 104 is itself grown as a substantially strained layer, since the crystalline structure of the layer 102 is substantially maintained within the layer 104, thereby reducing its natural lattice spacing so that the channel region 110 may be a compressively strained region, thereby modifying the mobility of holes, which may be advantageous in forming a P-channel transistor on the basis of the channel region 110 and the gate electrode 108.

Thereafter, starting from the device 100 as shown in Figure 1b or in Figure 1c, the further manufacturing process may be continued on the basis of well-established techniques for forming MOS transistors, which will be described in more detail later on with reference to Figures 2a-2d.

As previously explained, a moderately low concentration of the atomic species having the increased covalent radius may suffice so as to modify a corresponding lattice mismatch required for the generation of compressive or tensile strain, as is explained with reference to Figures 1a-1c. Thus, in some illustrative embodiments, additionally or alternatively to the epitaxial growth process 105, other techniques for incorporating the atomic species, such as diffusion and implantation, may be used. For example, an implantation process may be performed to introduce, for instance, tin atoms into the layer 104, thereby increasing the corresponding concentration and thus the induced strain.

Figure 1d schematically shows an illustrative embodiment in which the semiconductor device 100 comprises a first device region 150, in which the gate electrode 108 may be formed, while, in a second device region 160, a second gate electrode 118 may be formed on a second gate insulation layer 119, wherein the second device region 160 may be covered by an implantation mask 121, which may be provided in the form of a resist mask. Moreover, the semiconductor device 100 is subjected to an ion implantation 120 for introducing tin in a local fashion. For example, in the embodiment shown, it may be assumed that the layer 104 has been formed by the epitaxial growth process 105, as explained with reference to Figure 1c, thereby providing the layer 104 with an intrinsic strain 107. By further implanting tin ions in the vicinity of the gate electrode 108, the corresponding tin concentration may be increased, wherein a high dose, such as 10^{16} to 10^{17} ions/cm^2 may be used to provide a moderately high additional concentration of tin atoms within the layer 104. The implantation parameters of the process 120 may be selected on the basis of well-established simulation models in order to obtain an implantation energy for substantially depositing the tin ions within the layer 104 without unduly damaging the "template layer" 102.

After the completion of the implantation process 120, the resist mask 121 may be removed and the device 100 may be subjected to an anneal process for re-crystallizing damaged portions in the layer 104 and for substantially placing the implanted species at lattice sites to rebuild the strained lattice in the layer 104. Due to the increased tin concentration in the vicinity of the channel region 110, an even increased compressive strain may be generated therein, thereby also causing a more efficient modification of the charge carrier mobility.

It should be appreciated that the above-described embodiment is only of an illustrative nature and a variety of modifications may be considered. For instance, the implantation process 120 may be performed prior to the formation of the gate electrodes 108 and 118 on the basis of the mask 121, so that the entire exposed portion of the layer 104 may receive the increased tin contents. In still other illustrative embodiments, the epitaxial growth process 105 may be omitted when the tin concentration incorporated by the implantation

process 120 is considered sufficient for generating the desired degree of strain 107. In still other illustrative embodiments, the epitaxial growth process 105 may be performed on the basis of silicon and germanium and the implantation process 120 may be used to locally introduce tin atoms, thereby providing a means for fine tuning the finally obtained strain. For example, the first and second device regions 150, 160 may represent regions for different transistor types or may represent different die regions, in which a different degree of strain is required. For instance, in highly sensitive device regions of complex microprocessors, such as static RAM areas, none or a significantly reduced strain may be desirable, while, in logic areas, such as a CPU core, an increased degree of stress may be preferable to enhance operating speed of the CPU core. Consequently, due to the enhanced effect of the atomic species, such as tin, having the increased covalent radius, on the crystalline structure, a concentration achievable by implantation techniques may be appropriate so as to locally adjust the strain.

With reference to Figures 2a-2d, further illustrative embodiments of the present invention will now be described in more detail in which an embedded strained semiconductor material is formed in drain and source regions of a transistor element to induce a corresponding strain in the adjacent channel region.

Figure 2a schematically shows in a cross-sectional view a semiconductor device 200 comprising a substrate 201 having formed thereon a crystalline semiconductor layer 202. The substrate 201 may represent a bulk silicon substrate or an SOI-like substrate, *i.e.*, the substrate 201 may have formed thereon a buried insulating layer (not shown) above which is formed the crystalline semiconductor layer 202. The semiconductor layer 202 may represent a silicon-based layer, *i.e.*, the layer 202 may at least comprise approximately 50% silicon. Moreover, a transistor element 250 at an early manufacturing stage may be formed in and above the crystalline semiconductor layer 202. In this stage, a gate electrode 208 may be formed above the layer 202 and may be comprised of doped polysilicon, or any other appropriate material may be provided above the layer 202 and may be separated therefrom by a gate insulation layer 209. It should be appreciated that other approaches and transistor architectures may also be used in combination with the present invention, in which, for example, the gate electrode 208 may represent a replacement or dummy gate electrode, which may be removed in a later stage of manufacture to provide a conductive material of enhanced electrical characteristics. The gate electrode 208 may be "encapsulated" by a capping layer 230 and respective spacer elements 231, which may be separated from the gate electrode 208 by a respective liner 232. For instance, the capping layer 230 and the spacer 231 may be comprised of any appropriate dielectric material, such as silicon nitride, silicon oxynitride and silicon dioxide, which may be used as an etch and growth mask in an etch process and an epitaxial growth process for the formation of an embedded strained semiconductor region. The liner 232 is typically formed of a material

having a high etch selectivity with respect to the spacer 231. For instance, a combination of silicon dioxide and silicon nitride for the liner 232 and the spacer 231 may be efficiently used on the basis of well-established etch recipes.

The semiconductor device 200 as shown in Figure 2a may be formed in accordance with the following processes. After manufacturing the substrate 201, which may include advanced wafer bond techniques or other methods of forming a buried insulation layer, if SOI-like substrates are considered, the gate electrode 208 and the gate insulation layer 209 may be formed by deposition and/or oxidation for forming an appropriate gate insulation material, followed by the deposition of an appropriate gate electrode material. Thereafter, advanced lithography and etch techniques may be applied in accordance with well-established recipes to pattern the corresponding layers, thereby forming the gate electrode 208 and the gate insulation layer 209, wherein, during the patterning process, the capping layer 230 may also be patterned, which may have been used as an anti-reflective coating (ARC) layer, a hard mask layer and the like. Next, a liner material may be conformally deposited on the basis of plasma enhanced chemical vapor deposition (PECVD) followed by the deposition of a spacer layer, which is then patterned by an anisotropic etch process, thereby obtaining the spacer 231. Thereafter, the exposed residuals of the liner 232 may be removed and then the device 200 may be subjected to an anisotropic etch process 233 for forming a respective cavity or recess adjacent to the encapsulated gate electrode 208.

Figure 2b schematically shows the semiconductor device 200 in a further advanced manufacturing stage, wherein a recess or cavity 234 is formed after the completion of the anisotropic etch process 233. Next, the device 200 may be subjected to any pretreatments for preparing the device 200 for a subsequent selective epitaxial growth process. For instance, appropriate cleaning processes may be performed to remove contaminants and etch byproducts from exposed surfaces of the device 200. Thereafter, a selective epitaxial growth process 246 may be performed, wherein, in one illustrative embodiment, an appropriate deposition atmosphere may be established on the basis of a silicon-containing precursor material, a germanium-containing precursor material, and a precursor including an atomic species having the same valence as silicon and germanium and exhibiting an increased covalent radius compared to germanium. In one illustrative embodiment, the deposition ambient may be created on the basis of tin hydride (SnH_4) to provide a desired concentration of tin within the deposition atmosphere of the process 246. As previously explained, typically, in selective epitaxial growth processes, the process parameters, such as pressure, temperature, type carrier gases and the like, are selected such that substantially no material is deposited on dielectric surfaces, such as surfaces

of the capping layer 230 and the spacers 231, while a deposition is obtained on exposed surfaces of the crystalline layer 202, thereby using this layer as a crystalline template, which substantially determines the crystalline structure of the epitaxially grown material. In this illustrative embodiment, the material grown within at least a portion of the recess 234 is to be provided as a strained material, *i.e.*, the material should exhibit the same crystalline structure and, thus, substantially the same lattice spacing as the basic template of the layer 202, which results in a highly strained material region due to the presence of germanium and a further atomic species having an increased covalent radius, such as tin. Consequently, due to the presence of strained crystalline material, a corresponding strain is also created in a channel region 235 located adjacent to the recess 234.

As previously explained, due to the enhanced covalent radius of tin with respect to silicon and germanium, a significantly reduced amount of non-silicon atoms may be sufficient to achieve a corresponding strained semiconductor material during the epitaxial growth process 246. Consequently, a moderately low concentration of, for instance, tin within the deposition atmosphere in the range of approximately 0.1-10% may be considered appropriate for creating the required strain. In other embodiments, the deposition atmosphere of the process 246 may be established on the basis of silicon and the at least one further atomic species having the increased covalent radius, such as tin, substantially without adding any germanium, thereby providing enhanced design flexibility when the influence of a substantial amount of germanium may be considered inappropriate with respect to other electrical characteristics, such as leakage current of PN junctions and the like. During the epitaxial growth process 236, a concentration of tin and/or germanium and thus of silicon may be controlled in any appropriate manner. For example, in some cases, it may be appropriate to locate the tin atoms more closely to an upper surface of the drain and source regions still to be formed due to a different diffusion behavior of tin compared to germanium in subsequent high temperature processes in the further processing of the device 200. In other illustrative embodiments, the tin may be provided in the vicinity of areas in which a metal silicide is to be subsequently formed, wherein the significantly reduced amount of tin atoms may provide increased flexibility in creating the metal silicide, compared to a corresponding device that would require a significantly increased germanium content for creating the same amount of strain, which may, however, impose significant restrictions with respect to the subsequent silicidation process. In still other embodiments, a final silicon layer may be formed on top of the strained silicon/germanium/tin layer or the silicon/tin layer formed by the epitaxial growth process 246.

Figure 2c schematically shows the semiconductor device 200 after the completion of the epitaxial growth process 236. Hence, the device 200 comprises a recessed strained semiconductor region 236 having a

crystalline structure that corresponds to the diamond-structure of the silicon-based layer 202. Due to the lattice mismatch, as the natural lattice spacing of the crystalline structure in the region 236 is larger than a regular silicon spacing, a compressive strain 207 is generated in the channel region 235, thereby providing an enhanced mobility for holes during the operation of the transistor 250. Moreover, due to the partial or complete substitution of germanium by an atomic species having an enlarged covalent radius, such as tin, a significantly increased value for the strain 207 may be obtained on the basis of a concentration of non-silicon atoms in the region 236 that is well below a limit for conglomeration, as is previously encountered in conventional devices, when a high germanium content is used. However, as previously explained, the germanium and/or tin concentration within the region 236 may vary in the depth direction to account for various device requirements. For instance, in the embodiment shown, a specific "overgrowth" may have been formed to enhance a subsequent silicidation process, thereby reducing the resulting contact resistance. Moreover, an upper region of the epitaxially grown material 236, indicated as 236A, may be provided, which may have a reduced germanium concentration while still providing a high degree of strain by correspondingly increasing the tin concentration, which may, however, still be significantly less compared to a silicon/germanium region producing the same amount of strain 207, thereby allowing enhanced flexibility in selecting appropriate refractory metals for the subsequent silicidation process. It should be appreciated that any other appropriate variation in the germanium and/or tin concentration within the region 236 may be created during the preceding epitaxial growth process.

Thereafter, the spacers 231 and the capping layer 230 may be removed, possibly after any implantation processes for forming drain and source regions, when the spacers 231 have appropriate dimensions for obtaining the desired lateral profile, at least of a part of the drain and the source regions. In other cases, the spacers 231 and the capping layer 230 may be removed and a conventional process sequence may be carried out to form spacer elements with intermediate implantation processes for obtaining the required complex lateral profiling of the drain and source region defined by design rules.

Figure 2d schematically shows the semiconductor device 200 at an advanced manufacturing stage, in which the transistor 250 is substantially finished. Thus, the device 200 comprises a sidewall spacer structure 237, which may include a plurality of individual spacer elements separated by respective liners. Moreover, a drain and source region 239 has a specified lateral dopant profile in accordance with device requirements. Moreover, metal silicide regions 238 may be formed on the drain and source regions 239 and a corresponding metal silicide region 239 may be formed in the gate electrode 208. Consequently, the channel region 235 may be compressively strained due to the strain 207 created by the region 236, thereby significantly enhancing the drive

current capability of the transistor 250, which may represent a P-channel transistor. Due to the provision of the atomic species having the increased covalent radius in the region 236, a significant increase of the strain 207 may be achieved compared to conventional devices including an embedded silicon/germanium region.

Moreover, by appropriately designing the germanium and/or tin concentration in the region 236, an enhanced flexibility in forming the metal silicide regions 238 may be provided. For example, a highly conductive nickel silicide may be formed in the region 238 by reducing the germanium content at least in the upper portion 236A while nevertheless providing enhanced strain by correspondingly increasing the tin concentration. Consequently, a significant gain in performance may be obtained while nevertheless a high degree of compatibility with conventional processes for forming embedded silicon/germanium semiconductor structures may be maintained and an additional freedom in the design may be obtained. For this purpose, a corresponding epitaxial growth process may be adapted to include the provision of appropriate precursor material such as tin hydride (SnH_4), on the basis of which an appropriate and desired incorporation of non-silicon atoms may be achieved, which allows efficient control of the created strain substantially without creating any stress relief by phase segregation and crystal slips inside the strained semiconductor region 236.

Figure 3 schematically shows a cross-sectional view of a semiconductor device 300 in accordance with still other embodiments. The semiconductor device 300 comprises a first transistor 350 and second transistor 360 formed above a substrate 301 on the basis of a crystalline semiconductor layer 302. With respect to the substrate 302 and the semiconductor layer 302, the same criteria apply as previously explained with reference to the components 101, 102, 201 and 202. Moreover, in the embodiment illustrated, the transistors 350, 360 may have encapsulated gate electrodes 308 and formed adjacent thereto corresponding raised semiconductor regions 336, 336A. In other illustrative embodiments (not shown), the raised regions 336, 336A may not be provided and may merely represent a portion of the crystalline semiconductor layer 302.

The device 300 as shown in Figure 3 may be formed in accordance with a process strategy as is previously described with reference to Figures 2a-2b, wherein, however, the transistors 350, 360 may represent transistors that may receive a different magnitude of strain, since these transistors may represent transistors at different die regions or may represent transistors of different conductivity type. For example, the first transistor 350 may represent a P-channel transistor while the transistor 360 may represent an N-channel transistor. Consequently, during a corresponding etch process for forming respective cavities or recesses to accommodate the semiconductor regions 336, 336A, an enhanced process uniformity may be achieved since the etch process may not require any hard masks to completely cover one transistor type, while exposing the other. Similarly, in

the subsequent epitaxial growth process, an enhanced degree of uniformity may be achieved across the substrate 301 due to the reduction of any loading effects that may also be an issue in conventional techniques, in which one transistor type is to be completely covered while the other type is exposed. During the corresponding epitaxial growth process for forming the raised semiconductor regions 336, 336A, a small amount of germanium and/or tin may be incorporated to provide a "basic" strain 307 that is compatible with the performance of, for instance, the second transistor 360. In other illustrative embodiments, when the basic strain 307 is considered inappropriate, a corresponding cavity etch and a subsequent epitaxial growth process may be omitted. In other cases, the transistor 360 may represent a P-channel transistor in a critical device region, such as a static RAM area, which may receive a reduced amount of strain 307, while the transistor 350 may require an increased strain.

In one illustrative embodiment, an implantation process 320 may be performed, during which the first transistor 350 is exposed while the second transistor 360 may be covered by a resist mask 321. During the implantation 320, tin may be implanted into the region 336, thereby increasing the tin concentration therein, which may lead to a desired increase of strain due to the increased covalent radius of tin generating a lattice distortion more efficiently. Since a high concentration in terms of implantation induced concentrations may be required, such as approximately 10^{20} atoms/cm^3 or even more, the region 336 may be substantially amorphized during the implantation 320. Consequently, an anneal process may be performed to re-crystallize the substantially amorphized portion 336 on the basis of the crystalline template 302, thereby forming a highly strained crystal structure in the region 336. As a consequence, the initially present strain 307 may be increased to a value 307A to thereby obtain the required mobility gain in the transistor 350. Thereafter, the further processing for completing the transistors 350 and 360 may be continued as is previously described with reference to Figures 2a-2d.

In other illustrative embodiments, the implantation process 320 may be performed without a preceding formation of the regions 336, 336A, when the creation of the strain 307A obtained by a concentration achieved by the implantation 320 is considered appropriate. For example, in highly sensitive device regions, a strain engineering on the basis of a strained semiconductor material may not be inappropriate for N-channel transistors, while a "mild" strain in the channel region of PMOS transistors may be desirable. In this situation, the implantation sequence 320 may be applied prior to the formation of any drain and source regions, wherein, in one embodiment, additionally the implantation 320 may be performed as a pre-amorphization implantation to enhance the subsequent dopant introduction for forming the drain and source regions. Consequently, a highly

selective performance improvement may be achieved with a high degree of compatibility with existing process techniques substantially without grossly affecting the N-channel transistors.

As a result, the present invention provides an improved technique for the formation of strain by means of strained or relaxed semiconductor material in that an atomic species, such as tin, having greater covalent radius compared to germanium is incorporated into respective crystalline silicon-based semiconductor layers, thereby significantly reducing the risk for stress relief due to conglomeration and lattice defects. In illustrative embodiments, the atomic species having the increased covalent radius may be incorporated by an epitaxial growth process on the basis of an appropriate precursor material, such as tin hydride (SnH_4). Moreover, by incorporating the atomic species by other techniques, such as implantation, a highly localized strain engineering may be accomplished, thereby offering high flexibility for process and product design.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

forming, in a crystalline semiconductor layer (104, 236, 336), a crystalline structure on the basis of silicon and at least one further atomic species having a covalent radius that is greater than a covalent radius of germanium; and

using said crystalline structure to create strain (107, 207, 307) in a first region (110, 235, 335) of said semiconductor layer.

2. The method of claim 1, wherein forming said crystalline structure comprises at least one of epitaxially growing said silicon and said at least one further atomic species and depositing said silicon and said at least one further atomic species.

3. The method of claim 1, wherein forming said crystalline structure comprises implanting said at least one further atomic species into a first portion of said crystalline semiconductor layer and re-crystallizing said portion using said crystalline semiconductor layer as a crystalline template.

4. The method of claim 3, further comprising forming a silicon/germanium crystal in said structure and implanting said at least one further atomic species to adjust the amount of strain in said first region.

5. The method of claim 3, further comprising implanting said at least one further atomic species into a second portion so as to create a second strain (307A) in a second region of said crystalline semiconductor layer, said second strain differing from said first strain (307).

6. The method of claim 1, further comprising forming a gate electrode (108, 208, 308) above said crystalline semiconductor layer, wherein said crystalline structure is formed with a lateral offset to said gate electrode (108, 208, 308).

7. The method of claim 6, further comprising forming a recess (234) adjacent to said gate electrode (108, 208, 308) and forming at least a portion (236, 336) of said crystalline structure within said recess.

8. A semiconductor device, comprising:

a crystalline semiconductor layer (104, 236, 336) having a first stress-inducing region (335) comprising silicon and at least one further atomic species having a covalent radius that is greater than a covalent radius of germanium.

9. The semiconductor device of claim 8, further comprising:

a gate electrode (108, 208, 308) formed above said crystalline semiconductor layer (104); and

a strained channel region (110, 235, 335), wherein said first stress-inducing region is formed in a drain and source region.

10. The semiconductor device of claim 8, wherein said first stress-inducing region comprises tin.

11. The semiconductor device of claim 10, wherein said first stress-inducing region comprises germanium.

12. The semiconductor device of claim 8, further comprising a second stress-inducing region (335) comprising silicon and the least one further atomic species, wherein a concentration of the at least one further atomic species in the first stress-inducing region is different than a concentration of the at least one further atomic species in the second stress-inducing region (335).

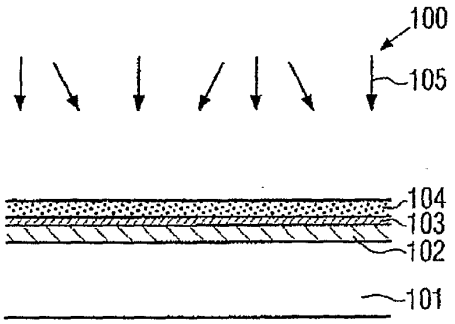


FIG. 1a

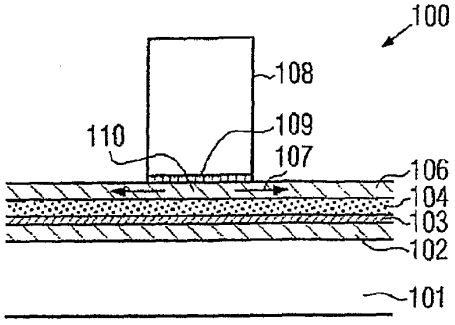


FIG. 1b

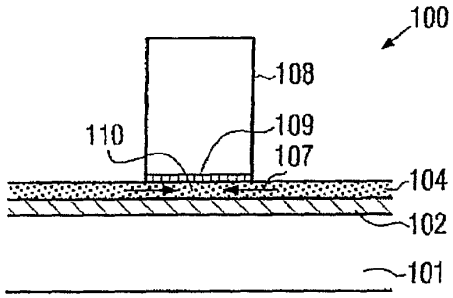


FIG. 1c

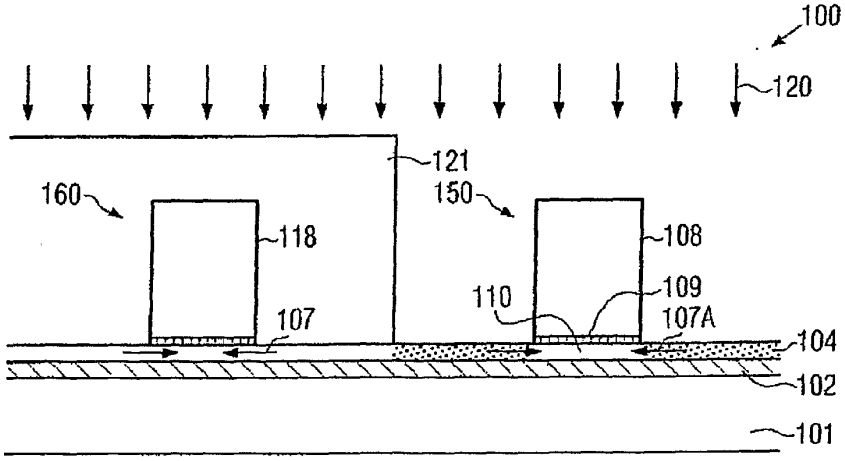


FIG. 1d

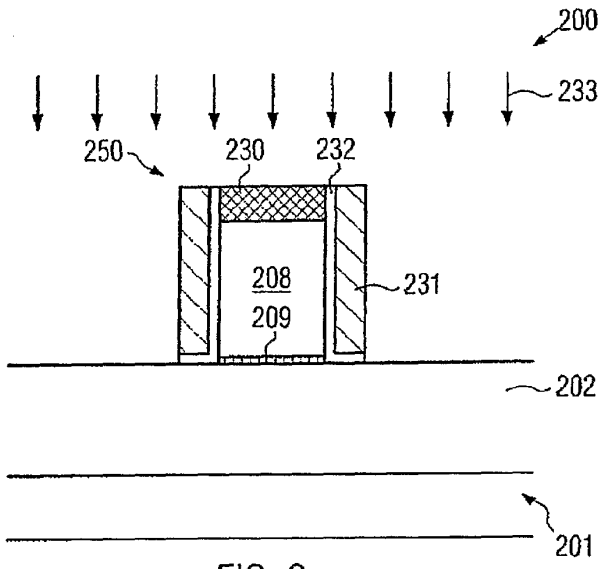

200
233
250
230
232
208
209
231
202
201

FIG. 2a

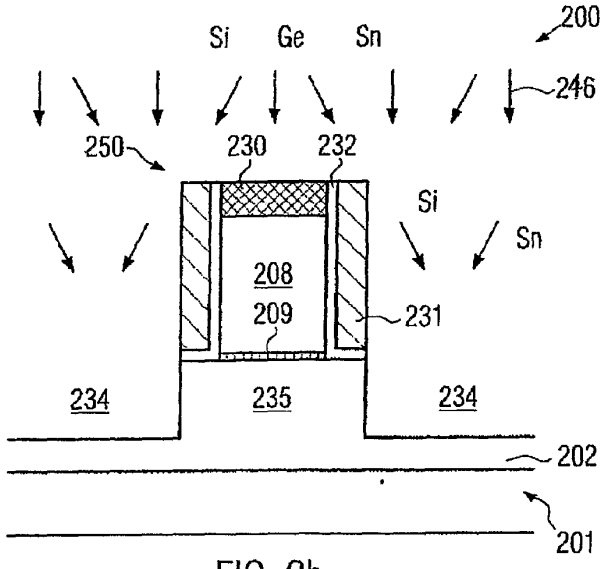

Si
Ge
Sn
200
246
250
230
232
Si
Sn
208
209
231
234
235
234
202
201

FIG. 2b

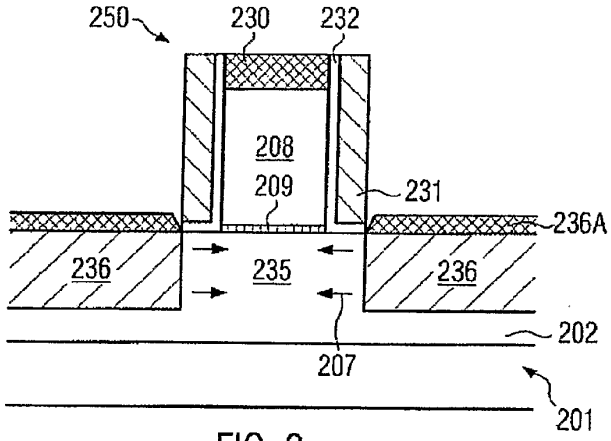

250
230
232
208
209
231
236A
236
235
236
202
207
201

FIG. 2c

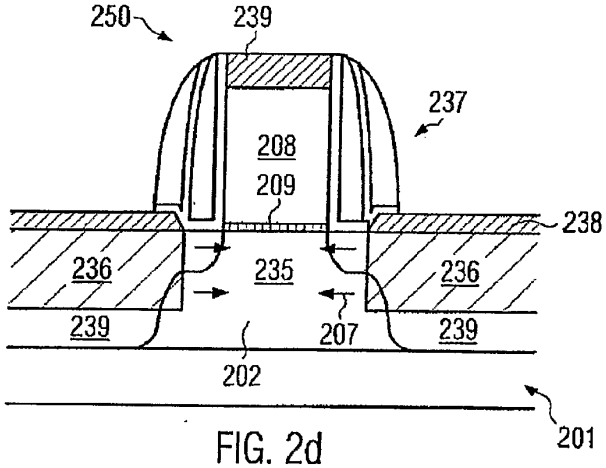

250
239
237
208
209
238
236
235
236
239
207
239
202
201

FIG. 2d

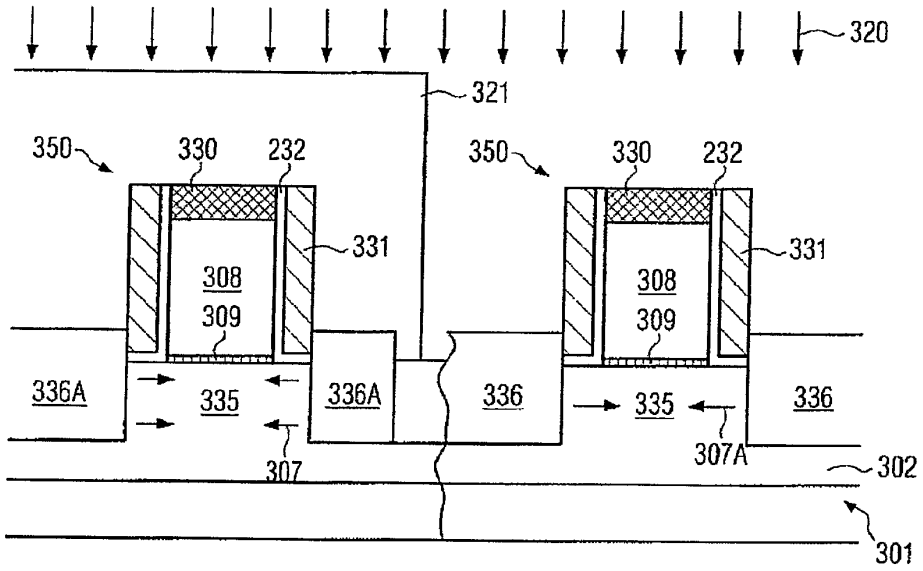

320
321
350
330
232
331
308
309
336A
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FIG. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/041559

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/20 H01L21/205

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/070053 A1 (SADAKA MARIAM G [US] ET AL) 31 March 2005 (2005-03-31) the whole document	1-12
X	WO 2005/015609 A (UNIV ARIZONA [US]; KOUVETAKIS JOHN [US]; BAUER MATTHEW [US]; TOLLE JOH) 17 February 2005 (2005-02-17) paragraphs [0022] - [0048]	1-12

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 March 2007	19/03/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Wolff, Gerhard

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/041559

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KOBAYASHI ET AL: "Synthesis of metastable group-IV alloy semiconductors by ion implantation and ion-beam-induced epitaxial crystallization" APPLIED SURFACE SCIENCE, ELSEVIER, AMSTERDAM, NL, vol. 100-101, 2 July 1996 (1996-07-02), pages 498-502, XP005296582 ISSN: 0169-4332 1. Introduction, 2. Experimental	1-12
X	KOUVETAKIS J ET AL: "New IR semiconductors in the Si-Ge-Sn system" GROUP IV PHOTONICS, 2004. FIRST IEEE INTERNATIONAL CONFERENCE ON HONG KONG, CHINA 29 SEPT.-1 OCT. 2004, PISCATAWAY, NJ, USA,IEEE, US, 29 September 2004 (2004-09-29), pages 55-57, XP010782182 ISBN: 0-7803-8474-1 the whole document	1-12
X	"Pseudomorphic Si1-xSnx alloy films grown by molecular beam epitaxy on Si" APPLIED PHYSICS LETTERS, AIP, AMERICAN INSTITUTE OF PHYSICS, MELVILLE, NY, US, vol. 67, no. 16, 16 October 1995 (1995-10-16), pages 2287-2289, XP012013788 ISSN: 0003-6951 abstract	1-12
X	"Band-edge photoluminescence from pseudomorphic Si0.96Sn0.04 alloy" APPLIED PHYSICS LETTERS, AIP, AMERICAN INSTITUTE OF PHYSICS, MELVILLE, NY, US, vol. 68, no. 22, 27 May 1996 (1996-05-27), pages 3105-3107, XP012015378 ISSN: 0003-6951 page 3105	1-12

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/041559

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005070053 A1	31-03-2005	US 2005070056 A1	31-03-2005
		US 2005070057 A1	31-03-2005
WO 2005015609 A	17-02-2005	WO 2005001902 A2	06-01-2005
		WO 2004114368 A2	29-12-2004

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(54) **Title:** MULTI-LAYER SOURCE/DRAIN STRESSOR

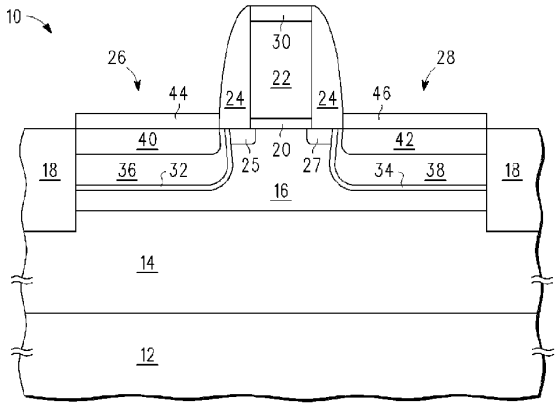


FIG. 5

(57) **Abstract:** A method for forming a semiconductor device (10) includes forming a recess (26) in a source region and a recess (28) in a drain region of the semiconductor device. The method further includes forming a first semiconductor material layer (32) in the recess (26) in the source region and a second semiconductor material layer (34) in the recess (28) in the drain region, wherein each of the first semiconductor material layer (32) and the second semiconductor material layer (38) are formed using a stressor material having a first ratio of an atomic concentration of a first element and an atomic concentration of a second element, wherein the first element is silicon and a first level of concentration of a doping material. The method further includes forming additional semiconductor material layers (36, 38, 40, 42) overlying the first semiconductor material layer (32) and the second semiconductor material layer (34) that have a different ratio of the atomic concentration of the first element and the second element.

WO 2008/100687 A1

MULTI-LAYER SOURCE/DRAIN STRESSOR

Background

Field

[0001] This disclosure relates generally to integrated circuits, and more specifically, to integrated circuits having a multi-layer source/drain stressor.

Related Art

[0002] One of the techniques for improving N channel and P channel transistor performance is by introducing strain to the channel. One of the techniques to introduce strain is to remove semiconductor material from the source/drain locations and regrowing a semiconductor material epitaxially which is of a different composition. For example, one approach for improving P channel performance, where the initial semiconductor material and thus the channel is just silicon, is regrowing a combination of silicon and germanium (SiGe) in the source/drain regions which exerts a compressive stress on the channel. One of the difficulties is that the amount of stress being exerted is dependent on the germanium concentration but increasing the germanium concentration can cause the formation of defects which then causes a reduction in the stress being exerted. In addition, as the device dimension shrinks during the technology evolution, one critical challenge is to maintain good performance characteristics for short channel transistors.

[0003] Thus, there is a need for improving on the technique for regrowing the source/drains to provide stress to the channel.

Brief Description of the Drawings

[0004] The present invention is illustrated by way of example and is not limited by the accompanying figures, in which like references indicate similar elements. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

[0005] FIG. 1 is a cross section of a semiconductor device at a stage in processing according to an embodiment of the invention;

[0006] FIG. 2 is a cross section of the semiconductor device of FIG. 1 at a subsequent stage in processing;

[0007] FIG. 3 is a cross section of the semiconductor device of FIG. 2 at a subsequent stage in processing;

[0008] FIG. 4 is a cross section of the semiconductor device of FIG. 3 at a subsequent stage in processing;

[0009] FIG. 5 is a cross section of the semiconductor device of FIG. 4 at a subsequent stage in processing;

[0010] FIG. 6 is a graph showing relative boron concentration in a semiconductor region, which includes epitaxially grown regions, of the semiconductor device of FIG. 5; and

[0011] FIG. 7 is a graph showing relative germanium concentration in the semiconductor region of the semiconductor device of FIG. 5.

Detailed Description

[0012] In one aspect, source/drains regions adjacent to a gate are removed and regrown using multiple layers of a different semiconductor combination. In one embodiment the semiconductor combination is an alloy of silicon and germanium (SiGe). The first layer has a first concentration of germanium and is doped with a first concentration of boron. Growth of the first layer is terminated before defects begin occurring. A first subsequent layer is grown at reduced germanium concentration which would not have defects until a second thickness is reached in which the second thickness is greater than the first thickness. The first subsequent layer is grown without defects and is boron-doped to a second concentration of boron greater than the first concentration of boron. A second subsequent layer is then grown at increased germanium concentration compared to the first subsequent layer and which is grown to a sufficiently low thickness so that there are substantially no defects. The boron doping is further increased in the second subsequent layer. Thus, the first subsequent layer provides defect relief against the high germanium concentration layers of the first layer and the second subsequent layer. The boron is increased as distance from the channel is increased to avoid adverse short channel effects. This is further explained in the following description and the drawings.

[0013] Shown in FIG. 1 is a semiconductor device 10 comprising a semiconductor substrate 12, an insulating layer 14 over substrate 12, a semiconductor region 16 over insulating layer 14, a trench isolation region 18 surrounding semiconductor region 16, a gate 22 overlying a center portion semiconductor region 16, a sidewall spacer 24 surrounding gate 22, an insulating cap 30 over gate 22, a gate dielectric between gate 22 and semiconductor region 16, a source/drain extension 25 adjacent to one side of gate 22 in a top surface of semiconductor region 16, and a source/drain extension 27 on the other side of gate 22 on the top surface of semiconductor region 16. The region between source/drain

extensions 25 and 27, which is along the top surface of semiconductor region 16 and under gate 22, will function as a channel. This structure of FIG. 1 arises from forming gate 22, performing an implant to form source/drain extensions 25 and 27, forming sidewall spacer 24, and removing portions of semiconductor 16 using trench isolation region 18, gate 22, cap 30, and sidewall spacer 24 as a mask to result in an opening 26 adjacent to gate 22 on one side and opening 28 adjacent to gate 22 on the other side. This etch can be isotropic, preferably a dry isotropic etch, so that portions of openings 26 and 28 are under sidewall spacer 24. While this etch is occurring the N channel transistors are masked off and thus are not etched. Sidewall spacer is shown as one material formed by a conformal deposition followed by an anistropic etch but it may be formed in several layers and may include a liner. As an alternative It may be formed simply as a liner rather than one or more sidewall spacers. One example is a nitride spacer with an oxide liner between the nitride spacer and gate 22 as well as between the nitride spacer and semiconductor region 16. Semiconductor region 16 in this described example is just silicon, as the semiconductor material, that may have background doping and other dopings such as a halo implant. The principles described may have applicability with other semiconductor materials as well. An exemplary thickness for semiconductor region 16 from insulating layer 14 to gate dielectric 20 is about 500 Angstroms. An exemplary depth for openings 26 and 28 is 350 Angstroms. The combination of substrate 12, insulating layer 14, and semiconductor region makes up what is commonly called an SOI (semiconductor on insulator) substrate. Insulating layer 14 is commonly referred to as a BOX (buried oxide). This process may also be effective for a bulk silicon substrate in which the insulating layer is not present. Trench isolation 18 provides electrical isolation for the transistor or transistors that it surrounds.

[0014] Shown in FIG. 2 is semiconductor device 10 after epitaxially growing a semiconductor layer 32 on semiconductor region 16 in opening 26 and semiconductor layer 34 on semiconductor region 16 in opening 28. Semiconductor layers 32 and 34 are about 50 Angstroms thick in this example and are boron-doped SiGe. The concentration of Ge is about 30 atomic percent (%). This is a Si to Ge ratio of 2.3 to 1. The boron doping in this example is from about 5e19 (5×10^{19}) atoms per cubic centimeter (atoms/cc) to about 2e20 (2×10^{20}) atoms/cc. At 30% germanium, semiconductor layers 32 and 34 can be grown to 50 Angstroms directly on just silicon without developing defects. Avoiding defects is important because defects tend to relax the layer where they are. If that occurs, that defeats the primary purpose of growing the layers of generating stress on the channel. The relatively high Ge% in the first grown layers (layers 32 and 34) is important in retarding dopant diffusion into the channel region to improve short channel device control. The reason is that dopant (e.g., Boron) diffusivity is significantly reduced in SiGe with high Ge% than in Si. The

boron concentration of about 5e19 atoms/cc to 2e20 atoms/cc is a relatively low concentration that further reduces the boron diffusing into the channel to reduce short channel effects. Also by including boron in the epitaxial growth, this avoids the need for implanting. Implanting also tends to generate the type of defects that cause relaxation so is preferably avoided. The thickness of layer 32 may not be uniform in the lateral and vertical directions because the upward growth tends to be faster than lateral growth.

[0015] Shown in FIG. 3 is semiconductor device 10 after epitaxially growing a semiconductor layer 36 on semiconductor layer 32 and epitaxially growing a semiconductor layer 38 on semiconductor layer 34. Semiconductor layers 36 and 38 are, in this example, about 250 Angstroms and are also boron-doped SiGe. In this layer the germanium content is about 25 % (Si to Ge ratio of 3 to 1) and the boron concentration is from about 2e20/cc to 5e20/cc. This reduction in germanium concentration supports the increase of stressor film thickness without generating defects. The increase in boron concentration is for increasing conductivity but the risk in generating short channel problems is reduced by being further from the channel. The lateral growth is low as the growth continues so the thickness of semiconductor layers 36 and 38 in the lateral direction is much less than the 250 Angstrom growth in the upward direction.

[0016] Shown in FIG. 4 is semiconductor device 10 after epitaxially growing a semiconductor layer 40 on semiconductor layer 36 and epitaxially growing a semiconductor layer 42 on semiconductor layer 38. Semiconductor layers 40 and 42 are, in this example, about 300 Angstroms and are also boron-doped SiGe. In this layer the germanium content is about 30 % and the boron concentration is from about 5e20/cc to 1e21/cc. This increase in germanium concentration increases the stress that is generated and can be thicker than semiconductor layers 32 and 34 because they are grown on SiGe instead of just Si, and further, the upper portion of semiconductor layers 40 and 42 can have defects without causing adverse affects because the upper portion is converted to a metal alloy in a subsequent step. The increased Ge and boron concentrations at top layers 40 and 42 reduces contact resistance.

[0017] Shown in FIG. 5 is semiconductor device 10 after converting the upper portion of semiconductor layers 40 and 42 to metal germanium silicide layers 44 and 46. This conversion of a top portion of source/drain region to a silicide is a common practice for forming contacts. The increased Ge and boron concentrations at top layers 40 and 42 reduces contact resistance at the silicide-semiconductor interface. With germanium present in the semiconductor, the resulting metal silicide alloy includes silicon and germanium. Any

defects in semiconductor layers 40 and 42 that are ultimately consumed in the metallization process to form metal germanium silicide layers 44 and 46 do not cause adverse effects.

[0018] Shown in FIG. 6 is a graph showing the increase in boron concentration from the top of insulating layer 14 to the top surface of semiconductor layers 40 and 42. The abrupt change in boron concentration at the interface with semiconductor layer 16 is beneficial because it causes an abrupt PN junction which is better for reducing leakage across the PN junction as well as reducing junction capacitance.

[0019] Shown in FIG. 7 is a graph showing the changes in germanium concentration from the top of insulating layer 14 to the top surface of semiconductor layers 40 and 42. The scale does not begin at zero but shows the initial high concentration, the reduced intermediate concentration, and the final high concentration. This is an efficient way of achieving the desired result of high stress in the stressor with low defects.

[0020] Thus, it is seen that by altering the concentration of germanium in multiple layers it is possible to have the stressor provide a greater stress while reducing the risk of generating defects. The effectiveness is dependent both the germanium concentration and the thicknesses chosen. As the germanium concentration rises the thickness will need to be reduced, especially for concentrations over 30%. If higher concentration is used, it may be beneficial to provide additional layers of alternating germanium concentration. Further, by increasing the boron concentration as the layers are added the risk of short channel effects are reduced while obtaining good conductivity.

[0021] Thus described is a method for forming a semiconductor device. The method comprises forming a recess in a source region and a recess in a drain region of the semiconductor device, forming a first semiconductor material in the source region and second semiconductor material layer in the recess of the drain region, a third semiconductor material, and a fifth semiconductor material, forming a third semiconductor material layer overlying the first semiconductor material layer and a fourth semiconductor material layer overlying the second semiconductor material layer, and forming a fifth semiconductor material layer overlying the third semiconductor material layer and a sixth semiconductor material layer overlying the fourth semiconductor material layer. The step of forming the first and second semiconductor material layer is further characterized by each of the first semiconductor material layer and the second semiconductor material layer being formed using a stressor material having a first ratio of an atomic concentration of a first element and an atomic concentration of a second element, wherein the first element is silicon and a first level of concentration of a doping material. The step of forming the third and fourth

semiconductor layers is further characterized by each of the third semiconductor material layer and the fourth semiconductor material layer having a second ratio of the atomic concentration of the first element and the atomic concentration of the second element, wherein the second ratio is higher than the first ratio and wherein each of the third semiconductor material layer and the fourth semiconductor material layer have a second level of concentration of the doping material, wherein the second level of concentration of the doping material is higher than the first level of concentration of the doping material. The step of forming the fifth and sixth semiconductor material layers is further characterized by each of the fifth semiconductor material layer and the sixth semiconductor material layer having a third ratio of the atomic concentration of the first element and the atomic concentration of the second element, wherein the third ratio is lower than the second ratio and wherein each of the fifth semiconductor material layer and the sixth semiconductor material layer have a third level of concentration of the doping material, wherein the third level of concentration of the doping material is higher than the second level of concentration of the doping material. The method may be further characterized by the stressor material bieing an alloy of silicon and germanium such that the second element is germanium. The method may be further characterized by the doping material being one or more of a group V element in the periodic table. . The method may be further characterized by the first ratio of the atomic concentration of the first element to the atomic concentration of the second element being about 2.3 to 1. The method may be further characterized by the doping material being boron and the first level of concentration of the doping material being from about 5e19 atoms per cm^3 to about 2e20 atoms per cubic centimeter. The method may be further characterized by the second ratio of the atomic concentration of the first element to the atomic concentration of the second element being about 3.0 to 1. The method may be further characterized by the doping material being boron and the second level of concentration of the doping material being from about 2e20 atoms per cm^3 to 5e20 atoms per cubic centimeter. . The method may be further characterized by the third ratio of the atomic concentration of the first element to the atomic concentration of the second element being about 2.3 to 1. The method may be further characterized by the doping material being boron and the third level of concentration of the doping material being in a range from about 5e20 atoms per cm^3 to 1e21 atoms per cm^3.

[0022] Also described is a method for forming a semiconductor device comprising forming a recess in a source region and a recess in a drain region of the semiconductor device, forming a first semiconductor material layer in the recess in the source region and a second semiconductor material layer in the recess in the drain region, forming a third semiconductor material layer overlying the first semiconductor material layer and a fourth

semiconductor material layer overlying the second semiconductor material layer, and forming a fifth semiconductor material layer overlying the third semiconductor material layer and a sixth semiconductor material layer overlying the fourth semiconductor material layer. The step of forming the first and second semiconductor material layers is further characterized by each of the first semiconductor material layer and the second semiconductor material layer being formed using a stressor material having a first ratio of an atomic concentration of a first element and an atomic concentration of a second element, wherein the first element is silicon and wherein each of the first semiconductor material layer and the second semiconductor material layer have a first level of concentration of a doping material. The step of forming the third and fourth semiconductor material layers is further characterized by each of the third semiconductor material layer and the fourth semiconductor material layer have a second level of concentration of the doping material, wherein the second level of concentration of the doping material is higher than the first level of concentration of the doping material. The step of forming the fifth and sixth semiconductor material layers is further characterized by each of the fifth semiconductor material layer and the sixth semiconductor material layer having a third level of concentration of the doping material, wherein the third level of concentration of the doping material is higher than the second level of concentration of the doping material. The method may be further characterized by the doping material being one or more of a group V element in the periodic table. The method may be further characterized by the doping material being boron and the first level of concentration of the doping material being from about 5e19 atoms per cm^3 to about 2e20 atoms per cm^3. The method may be further characterized by the second level of concentration of the doping material is from about 2e20 atoms per cm^3 to 5e20 atoms per cm^3. The method may be further characterized by the third level of concentration of the doping material being in a range from about 5e20 atoms per cm^3 to 1e21 atoms per cm^3.

[0023] Also described is a semiconductor comprising a a first semiconductor material layer in a recess in a source region and a second semiconductor material layer in a recess in a drain region; a third semiconductor material layer overlying the first semiconductor material layer and a fourth semiconductor material layer overlying the second semiconductor material layer; and a fifth semiconductor material layer overlying the third semiconductor material layer and a sixth semiconductor material layer overlying the fourth semiconductor material layer. The first and second semiconductor material layers are further characterized by each of the first semiconductor material layer and the second semiconductor material layer using a stressor material having a first ratio of an atomic concentration of a first element and an atomic concentration of a second element and a first level of concentration of a doping

material, wherein the first element is silicon. The third and fourth semiconductor material layers being further characterized by each of the third semiconductor material layer and the fourth semiconductor material layer having a second ratio of the atomic concentration of the first element and the atomic concentration of the second element, wherein the second ratio is higher than the first ratio and wherein each of the third semiconductor material layer and the fourth semiconductor material layer have a second level of concentration of the doping material, wherein the second level of concentration of the doping material is higher than the first level of concentration of the doping material. The fifth and sixth semiconductor material layers being further characterized by each of the fifth semiconductor material layer and the sixth semiconductor material layer having a third ratio of the atomic concentration of the first element and the atomic concentration of the second element, wherein the third ratio is lower than the second ratio and wherein each of the fifth semiconductor material layer and the sixth semiconductor material layer have a third level of concentration of the doping material, wherein the third level of concentration of the doping material is higher than the second level of concentration of the doping material. The semiconductor device may be further characterized by the stressor material being an alloy of silicon and germanium such that the second element is germanium. . The semiconductor device may be further characterized by the doping material being one or more of a group V element in the periodic table. The semiconductor device may be further characterized by the first ratio of the atomic concentration of the first element to the atomic concentration of the second element being about 2.3 to 1. The semiconductor device may be further characterized by the doping material being boron and the first level of concentration of the doping material being from about 5e19 atoms per cm^3 to about 2e20 atoms per cm^3, the second level of concentration of the doping material being from about 2e20 atoms per cm^3 to 5e20 atoms per cm^3, and the third level of concentration of the doping material being in a range from about 5e20 atoms per cm^3 to 1e21 atoms per cm^3. The semiconductor device may be further characterized by the second ratio of the atomic concentration of the first element to the atomic concentration of the second element being about 3.0 to 1.

[0024] Although the invention is described herein with reference to specific embodiments, various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, rather than adding stress to P channel transistors, stress may be added to N channel transistors by exerting tensile stress on the channels of the N channel transistors in a similar manner of providing source/drain stressors. This may be achievable by regrowing silicon carbon and altering the concentration of carbon in different layers to provide the desired stress while avoiding defect creation. Further it may be beneficial to increase the N channel dopant in

layers as well analogous to increasing the boron dopant for the P channel transistors. Although this may be less necessary for the case where the dopant is arsenic, due to its lower rate of diffusion, there may still some benefit. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention. Any benefits, advantages, or solutions to problems that are described herein with regard to specific embodiments are not intended to be construed as a critical, required, or essential feature or element of any or all the claims.

[0025] Furthermore, the terms “a” or “an,” as used herein, are defined as one or more than one. Also, the use of introductory phrases such as “at least one” and “one or more” in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles.

[0026] Unless stated otherwise, terms such as “first” and “second” are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements.

CLAIMS

What is claimed is:

1. A method for forming a semiconductor device comprising:
forming a recess in a source region and a recess in a drain region of the semiconductor device;
forming a first semiconductor material layer in the recess in the source region and a second semiconductor material layer in the recess in the drain region, wherein each of the first semiconductor material layer and the second semiconductor material layer are formed using a stressor material having a first ratio of an atomic concentration of a first element and an atomic concentration of a second element, wherein the first element is silicon and a first level of concentration of a doping material;
forming a third semiconductor material layer overlying the first semiconductor material layer and a fourth semiconductor material layer overlying the second semiconductor material layer, wherein each of the third semiconductor material layer and the fourth semiconductor material layer have a second ratio of the atomic concentration of the first element and the atomic concentration of the second element, wherein the second ratio is higher than the first ratio and wherein each of the third semiconductor material layer and the fourth semiconductor material layer have a second level of concentration of the doping material, wherein the second level of concentration of the doping material is higher than the first level of concentration of the doping material; and
forming a fifth semiconductor material layer overlying the third semiconductor material layer and a sixth semiconductor material layer overlying the fourth semiconductor material layer, wherein each of the fifth semiconductor material layer and the sixth semiconductor material layer have a third ratio of the atomic concentration of the first element and the atomic concentration of the second element, wherein the third ratio is lower than the second ratio and wherein each of the fifth semiconductor material layer and the sixth semiconductor material layer have a third level of concentration of the doping material, wherein the third level of concentration of the doping material is higher than the second level of concentration of the doping material.

2. The method of claim 1, wherein the stressor material is an alloy of silicon and germanium such that the second element is germanium.

3. The method of claim 1, wherein the doping material is one or more of a group V element.

4. The method of claim 3, wherein the first ratio of the atomic concentration of the first element to the atomic concentration of the second element is about 2.3 to 1.

5. The method of claim 3, wherein the doping material is boron and the first level of concentration of the doping material is from about 5e19 atoms per cm^3 to about 2e20 atoms per cubic centimeter.

6. The method of claim 3, wherein the second ratio of the atomic concentration of the first element to the atomic concentration of the second element is about 3.0 to 1.

7. The method of claim 3, wherein the doping material is boron and the second level of concentration of the doping material is from about 2e20 atoms per cm^3 to 5e20 atoms per cubic centimeter.

8. The method of claim 3, wherein the third ratio of the atomic concentration of the first element to the atomic concentration of the second element is about 2.3 to 1.

9. The method of claim 3, wherein the doping material is boron and the third level of concentration of the doping material is in a range from about 5e20 atoms per cm^3 to 1e21 atoms per cm^3.

10. A method for forming a semiconductor device comprising:

forming a recess in a source region and a recess in a drain region of the semiconductor device;

forming a first semiconductor material layer in the recess in the source region and a second semiconductor material layer in the recess in the drain region, wherein each of the first semiconductor material layer and the second semiconductor material layer are formed using a stressor material having a first ratio of an atomic concentration of a first element and an atomic concentration of a second element, wherein the first element is silicon and wherein each of the first semiconductor material layer and the second semiconductor material layer have a first level of concentration of a doping material;

forming a third semiconductor material layer overlying the first semiconductor material layer and a fourth semiconductor material layer overlying the second

semiconductor material layer, wherein each of the third semiconductor material layer and the fourth semiconductor material layer have a second level of concentration of the doping material, wherein the second level of concentration of the doping material is higher than the first level of concentration of the doping material; and

forming a fifth semiconductor material layer overlying the third semiconductor material layer and a sixth semiconductor material layer overlying the fourth semiconductor material layer, wherein each of the fifth semiconductor material layer and the sixth semiconductor material layer have a third level of concentration of the doping material, wherein the third level of concentration of the doping material is higher than the second level of concentration of the doping material.

11. The method of claim 10, wherein the doping material is one or more of a group V element.

12. The method of claim 11, wherein the doping material is boron and the first level of concentration of the doping material is from about 5e19 atoms per cm^3 to about 2e20 atoms per cm^3.

13. The method of claim 11, wherein the second level of concentration of the doping material is from about 2e20 atoms per cm^3 to 5e20 atoms per cm^3.

14. The method of claim 11, wherein the third level of concentration of the doping material is in a range from about 5e20 atoms per cm^3 to 1e21 atoms per cm^3.

15. A semiconductor device comprising:

a first semiconductor material layer in a recess in a source region and a second semiconductor material layer in a recess in a drain region, wherein each of the first semiconductor material layer and the second semiconductor material layer are formed using a stressor material having a first ratio of an atomic concentration of a first element and an atomic concentration of a second element and a first level of concentration of a doping material, wherein the first element is silicon;

a third semiconductor material layer overlying the first semiconductor material layer and a fourth semiconductor material layer overlying the second semiconductor material layer, wherein each of the third semiconductor material layer and the

fourth semiconductor material layer have a second ratio of the atomic concentration of the first element and the atomic concentration of the second element, wherein the second ratio is higher than the first ratio and wherein each of the third semiconductor material layer and the fourth semiconductor material layer have a second level of concentration of the doping material, wherein the second level of concentration of the doping material is higher than the first level of concentration of the doping material; and

a fifth semiconductor material layer overlying the third semiconductor material layer and a sixth semiconductor material layer overlying the fourth semiconductor material layer, wherein each of the fifth semiconductor material layer and the sixth semiconductor material layer have a third ratio of the atomic concentration of the first element and the atomic concentration of the second element, wherein the third ratio is lower than the second ratio and wherein each of the fifth semiconductor material layer and the sixth semiconductor material layer have a third level of concentration of the doping material, wherein the third level of concentration of the doping material is higher than the second level of concentration of the doping material.

16. The semiconductor device of claim 15, wherein the stressor material is an alloy of silicon and germanium such that the second element is germanium.

17. The semiconductor device of claim 15, wherein the doping material is one or more of a group V.

18. The semiconductor device of claim 17, wherein the first ratio of the atomic concentration of the first element to the atomic concentration of the second element is about 2.3 to 1.

19. The semiconductor device of claim 17, wherein the doping material is boron and the first level of concentration of the doping material is from about 5e19 atoms per cm^3 to about 2e20 atoms per cm^3, the second level of concentration of the doping material is from about 2e20 atoms per cm^3 to 5e20 atoms per cm^3, and the third level of concentration of the doping material is in a range from about 5e20 atoms per cm^3 to 1e21 atoms per cm^3.

20. The semiconductor device of claim 17, wherein the second ratio of the atomic concentration of the first element to the atomic concentration of the second element is about 3.0 to 1.

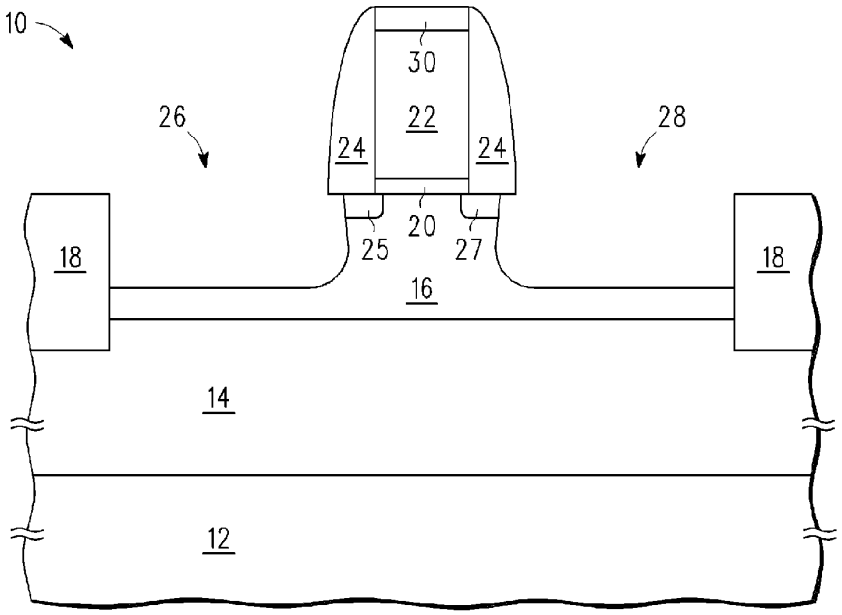

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FIG. 1

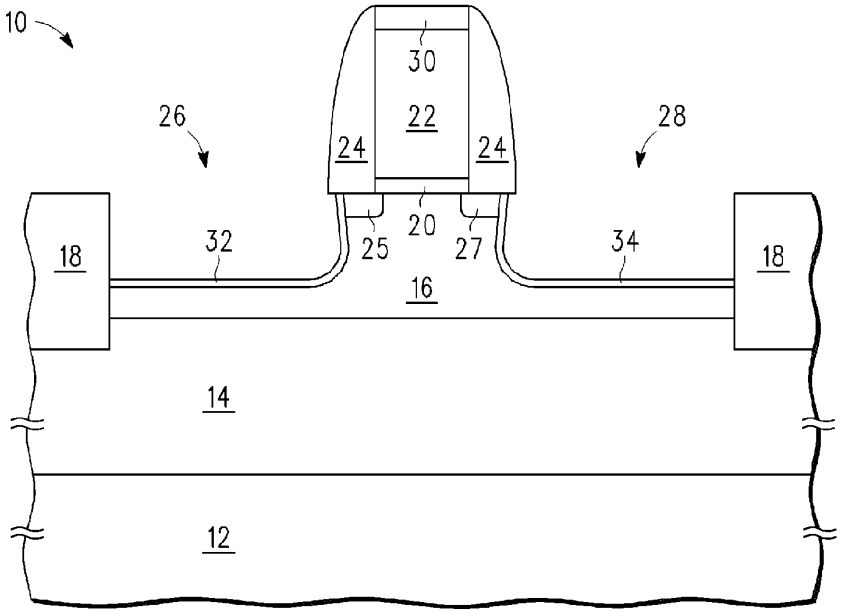

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FIG. 2

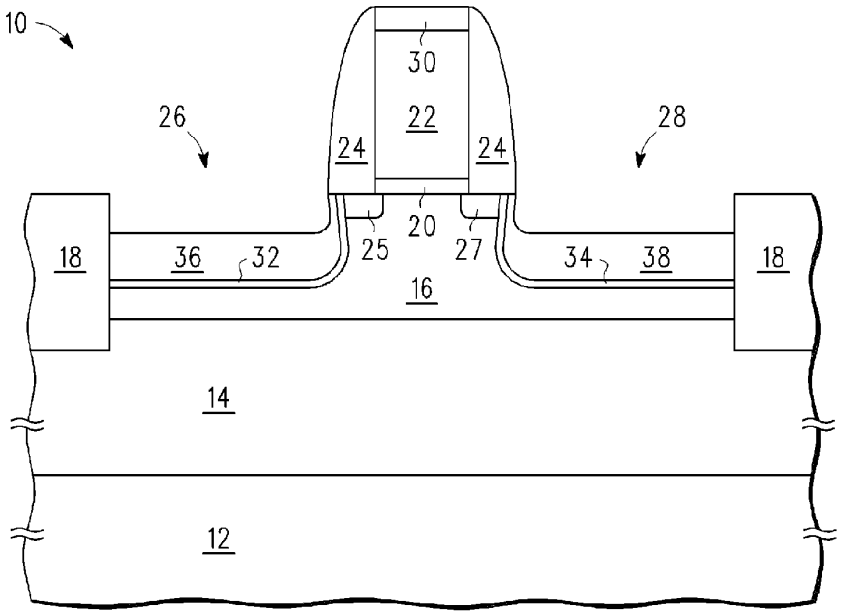

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FIG. 3

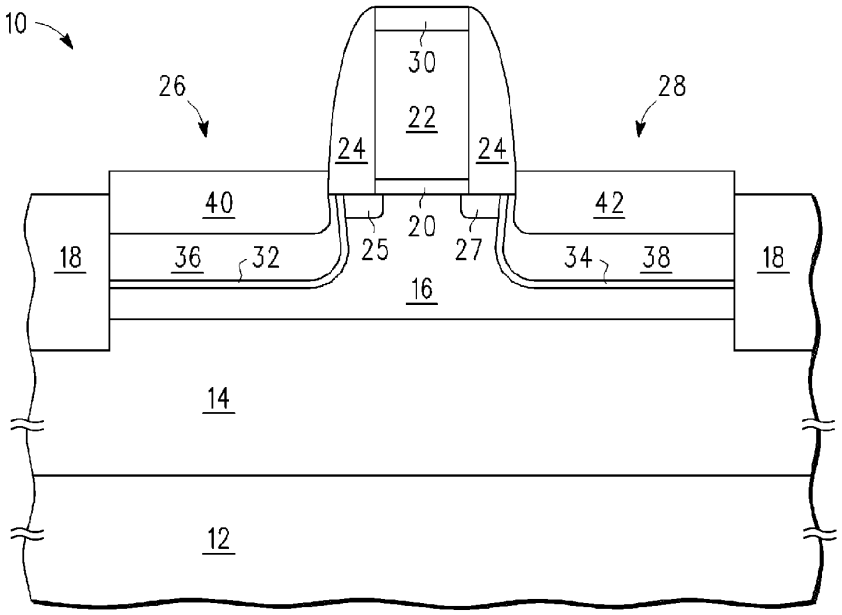

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FIG. 4

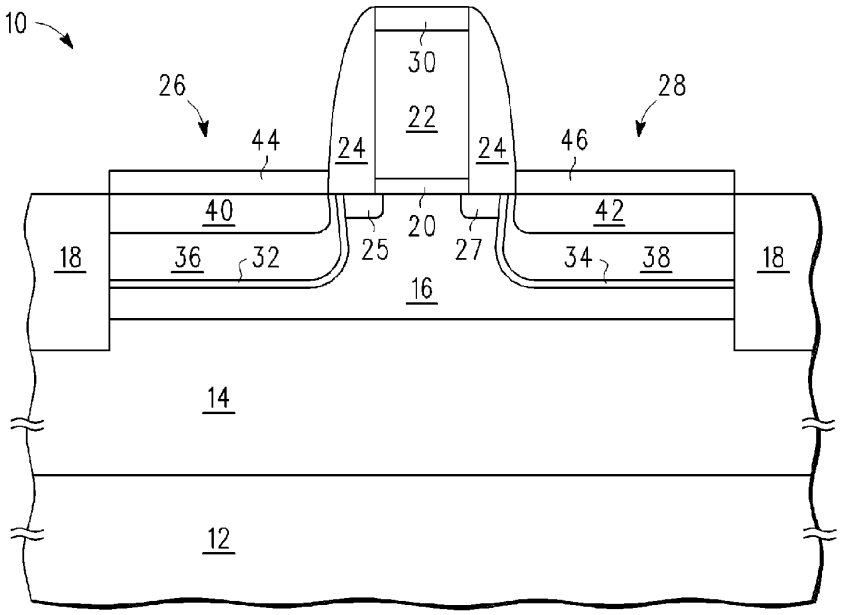


FIG. 5

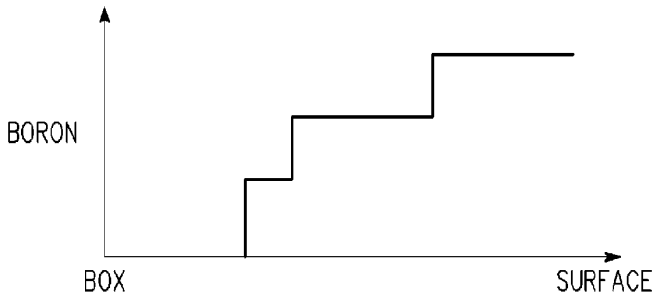


FIG. 6

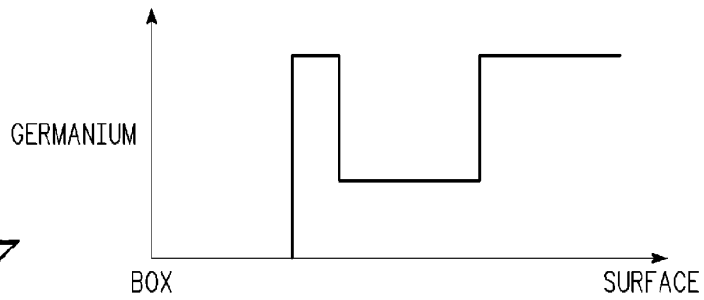


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/051841

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 8: H01L21/20, H01L 21/336, H01L29/76, H01L 29/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Utility models and applications for Utility models since 1975
Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKIPASS(KIPO internal) "Keyword: multi-layer stressor, source/drain stressor, and recess"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2005-124837 A1 (KONINKLIJKE PHILIPS ELECTRONICS N. V. et al.) 29 December 2005 See Abstract; Page 5, Line 24 - Page 8, Line 13; Claims 1 - 15; Figures 1 - 4.	1 - 20
A	JP 2007-036205 A (FUJITSU LTD.) 08 February 2007 See Abstract; Paragraph [0015] - Paragraph [0209]; Claims 1 - 10; Figures 3 - 39.	1 - 20
A	US 2006-0065914 A1 (CHEN, H. et al.) 30 March 2006 See Abstract; Paragraph [0012] - Paragraph [0036]; Claims 1 - 30; Figures 1 - 11.	1 - 20
A	US 2007-0004123 A1 (BOHR, M. T. et al.) 04 January 2007 See Abstract; Paragraph [0014] - Paragraph [0039]; Claims 1 - 20; Figures 2 - 9.	1 - 20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 MAY 2008 (29.05.2008)	**29 MAY 2008 (29.05.2008)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer KIM, JU SIK Telephone No. 82-42-481-8265

Form PCT/ISA/210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2008/051841

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO2005124837A1	29.12.2005	CN1969373A	23.05.2007
		EP01759404A1	07.03.2007
		JP20503083	31.01.2008
		KR1020070032692	22.03.2007
		US20070246742A1	25.10.2007
JP2007036205A	08.02.2007	CN1885556A	27.12.2006
		KR1020060134772	28.12.2006
		TW278115B	01.04.2007
		US2006289856A1	28.12.2006
		US2007012913A1	18.01.2007
US20060065914A1	30.03.2006	CN101032018A	05.09.2007
		EP1805796A1	11.07.2007
		KR1020070053300	23.05.2007
		US2006292779AA	28.12.2006
		US7135724BB	14.11.2006
		WO2006039377A1	13.04.2006
US20070004123A1	04.01.2007	KR1020080015891	20.02.2008
		WO2007005817A1	11.01.2007

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31 July 2009 (31.07.2009)

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(74) Agent: **DRAKE, Paul, S.**; Advanced Micro Devices, Inc., 7171 Southwest Parkway, Mail Stop B100.3.341, Austin, TX 78735 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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Published:

— *with international search report (Art. 21(3))*

(54) Title: PERFORMANCE ENHANCEMENT IN PMOS AND NMOS TRANSISTORS ON THE BASIS OF SILICON/CARBON MATERIAL

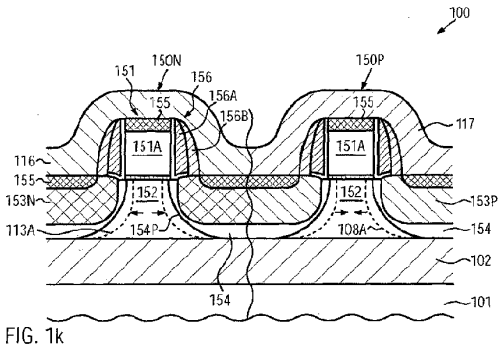


FIG. 1k

(57) Abstract: A silicon/germanium material and a silicon/carbon material may be provided in transistors of different conductivity type (150P, 150N) on the basis of an appropriate manufacturing regime without unduly contributing to overall process complexity. Furthermore, appropriate implantation species may be provided through exposed surface areas of the cavities (103P, 103N) prior to forming the corresponding strained semiconductor alloy (153), thereby additionally contributing to enhanced overall transistor performance. In other embodiments a silicon/carbon material may be formed in a P-channel transistor (150P) and an N-channel transistor (150N), while the corresponding tensile strain component may be overcompensated for by means of a stress memorization technique in the P-channel transistor. Thus, the advantageous effects of the carbon species, such as enhancing overall dopant profile of P-channel transistors, may be combined with an efficient strain component while enhanced overall process uniformity may also be accomplished.

WO 2010/014246 A1

PERFORMANCE ENHANCEMENT IN PMOS AND NMOS TRANSISTORS ON THE BASIS OF SILICON/CARBON MATERIAL

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

Generally, the present disclosure relates to integrated circuits, and, more particularly, to the formation of different transistor types having strained channel regions by using an embedded strain-inducing material to enhance charge carrier mobility in the channel regions.

2. DESCRIPTION OF THE RELATED ART

Integrated circuits have found a widespread applicability in many fields due to the continuous increase of functions that may be provided on a given chip area. Integrated circuits are composed of numerous individual circuit components, such as transistors, wherein several million or even several hundred million individual transistors may be provided in complex devices. Generally, a plurality of process technologies are currently practiced, wherein, for complex circuitry, such as microprocessors, storage chips and the like, CMOS technology is currently the most promising approach due to the superior characteristics in view of operating speed and/or power consumption and/or cost efficiency. During the fabrication of complex integrated circuits using CMOS technology, millions of transistors, *i.e.*, N-channel transistors and P-channel transistors, are formed on a substrate including a crystalline semiconductor layer. A MOS transistor, irrespective of whether an N-channel transistor or a P-channel transistor is considered, comprises so-called PN junctions that are formed by an interface of highly doped drain and source regions with an inversely doped channel region disposed between the drain region and the source region. The conductivity of the channel region, *i.e.*, the drive current capability of the conductive channel, is controlled by a gate electrode formed near to the channel region and separated therefrom by a thin insulating layer. The conductivity of the channel region, upon formation of a conductive channel due to the application of an appropriate control voltage to the gate electrode, depends on the dopant concentration, the mobility of the charge carriers and, for a given extension of the channel region in the transistor width direction, on the distance between the source and drain regions, which is also referred to as channel length. Thus, the reduction of the channel length, and associated therewith the reduction of the channel resistivity, renders the channel length a dominant design criterion for accomplishing an increase in the operating speed of the integrated circuits.

The continuing shrinkage of the transistor dimensions, however, involves a plurality of issues associated therewith that have to be addressed so as to not unduly offset the advantages obtained by steadily decreasing the channel length of MOS transistors. One major problem in this respect is the development of enhanced photolithography and etch strategies to reliably and reproducibly create circuit elements of critical dimensions, such as the gate electrode of the transistors, for a new device generation. Moreover, highly sophisticated dopant profiles, in the vertical direction as well as in the lateral direction, are required in the drain and source regions to provide low sheet and contact resistivity in combination with a desired channel controllability.

The continuous size reduction of the critical dimensions, *i.e.*, the gate length of the transistors, necessitates the adaptation and possibly the new development of highly complex process techniques concerning the above-identified process steps. It has, therefore, been proposed to enhance the channel conductivity of the transistor elements by increasing the charge carrier mobility in the channel region for a given channel length, thereby offering the potential for achieving a performance improvement that is comparable with the advance to a future technology node while avoiding or at least postponing many of the above process adaptations associated with device scaling. One efficient mechanism for increasing the charge carrier mobility is the modification of the lattice structure in the channel region, for instance by creating tensile or compressive stress in the vicinity of the channel region to produce a corresponding strain in the channel region, which results in a modified mobility for electrons and holes, respectively. For example, creating tensile strain in the channel region having a standard (100) surface orientation may increase the mobility of electrons, which, in turn, may directly translate into a corresponding increase in the conductivity. On the other hand, compressive strain in the channel region may increase the mobility of holes, thereby providing the potential for enhancing the performance of P-type transistors. The introduction of stress or strain engineering into integrated circuit fabrication is an extremely promising approach for further device generations, since, for example, strained silicon may be considered as a "new" type of semiconductor material, which may enable the fabrication of fast powerful semiconductor devices without requiring expensive semiconductor materials, while many of the well-established manufacturing techniques may still be used.

In one approach, the hole mobility of PMOS transistors is enhanced by forming a strained silicon/germanium layer in the drain and source regions of the transistors, wherein the compressively strained drain and source regions create uniaxial strain in the adjacent silicon channel region. To this end, the drain and source regions of the PMOS transistors are selectively recessed, while the NMOS transistors are masked, and subsequently the silicon/germanium layer is selectively formed in the PMOS transistor by epitaxial growth. Thus, complex manufacturing steps, such as etch processes, the formation of appropriate etch and growth masks and selective epitaxial growth techniques have to be incorporated into the CMOS process flow.

In other approaches, silicon/carbon material may be used for NMOS transistors to create a desired lattice mismatch specifically in the channel regions of the NMOS transistors, which may frequently be accomplished by ion implantation of carbon into the drain and source regions. However, the performance gain for transistors of different conductivity type on the basis of silicon/carbon alloys may lead to an even more complex process flow, as the various steps for the formation of respective strain layers may have to be appropriately integrated in the complex manufacturing flow, which may result in a less pronounced performance gain than expected.

The present disclosure is directed to various methods and devices that may avoid, or at least reduce, the effects of one or more of the problems identified above.

SUMMARY OF THE INVENTION

The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an exhaustive overview of the invention. It is not intended to identify key or critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is discussed later.

Generally, the present disclosure relates to techniques and semiconductor devices which enable the manufacture of differently strained semiconductor materials embedded into drain and source areas, wherein at least a semiconductor alloy may be used having a natural lattice constant that is less compared to a natural lattice constant of silicon. For example, in some illustrative aspects disclosed herein, a silicon/carbon alloy may be used in combination

with a further semiconductor alloy, such as a silicon/germanium alloy, to provide different types of strain for transistors of different conductivity type, while nevertheless providing an efficient manufacturing strategy, for instance with respect to using appropriate etch stop and spacer layers and/or incorporating appropriate implantation species prior to forming the corresponding semiconductor alloys. Hence, the advantages of each of the different semiconductor alloys may be taken advantage of while not unduly contributing to additional process complexity compared to conventional strategies in which usually a single strain-inducing semiconductor alloy may be used. In other illustrative aspects disclosed herein, a semiconductor material, such as silicon/carbon, which may typically be employed for enhancing characteristics of N-channel transistors, may also be provided in P-channel transistors in combination with sophisticated stress memorization techniques, thereby obtaining a desired type of strain in the P-channel transistors while at the same time enabling enhanced overall manufacturing efficiency and additional gain in transistor performance due to the positive effects of the carbon species in the drain and source areas of the P-channel transistor.

One illustrative method disclosed herein relates to forming a strained semiconductor material in a first transistor of a first conductivity type and a second transistor of a second conductivity type. The method comprises forming a stack of layers above a first gate electrode structure of the first transistor and a second gate electrode structure of the second transistor, wherein the first and second gate electrode structures comprise a respective cap layer and wherein the stack of layers comprises a spacer layer and an etch stop layer formed above the spacer layer. The method additionally comprises forming a mask above the second transistor by using the etch stop layer and forming a first spacer element at the first gate electrode structure from the spacer layer. Moreover, first cavities are formed in drain and source areas of the first transistor on the basis of the first spacer element and a first strained semiconductor material is formed in the first cavities. The method further comprises forming second cavities in drain and source areas of the second transistor on the basis of the second spacer element formed from the spacer layer. Finally, the method comprises forming a second strained semiconductor material in the second cavities, wherein the first and second strained semiconductor materials have a different material composition.

A further illustrative method disclosed herein comprises forming first cavities adjacent to a first gate electrode structure of a first transistor and second cavities adjacent to a

second gate electrode structure of a second transistor, wherein the first and second transistors are of different conductivity type. The method further comprises forming a semiconductor material in the first and second cavities, wherein the semiconductor material has a first type of strain. Moreover, lattice damage is created in the semiconductor material selectively in the first transistor to form a substantially relaxed semiconductor material. Furthermore, the method comprises re-crystallizing the substantially relaxed semiconductor material in a strained state that corresponds to a second type of strain that is opposite to the first type of strain.

One illustrative semiconductor device disclosed herein comprises a first transistor comprising a silicon/carbon alloy in drain and source regions wherein the first transistor comprises a channel region exhibiting a first strain component along a channel length direction. The semiconductor device further comprises a second transistor comprising a silicon/carbon alloy in drain and source regions thereof, wherein the second transistor comprises a channel region exhibiting a second strain component along a channel length direction wherein the first and second strain components are of opposite type.

BRIEF DESCRIPTION OF THE DRAWINGS

The disclosure may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figures 1a-1k schematically illustrate cross-sectional views of a semiconductor device including transistors of different conductivity type during various manufacturing stages, wherein a different type of strained semiconductor materials may be provided on the basis of a sophisticated manufacturing flow including enhanced masking regimes, possibly in combination with the incorporation of dopant species, non-doping species and the like, for enhancing overall transistor characteristics, according to illustrative embodiments; and

Figures 2a-2h schematically illustrate cross-sectional views of a semiconductor device during various manufacturing stages in forming transistor elements with different strain components by using a common semiconductor alloy, such as silicon/carbon, according to further illustrative embodiments.

While the subject matter disclosed herein is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION

Various illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present subject matter will now be described with reference to the attached figures. Various structures, systems and devices are schematically depicted in the drawings for purposes of explanation only and so as to not obscure the present disclosure with details that are well known to those skilled in the art. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present disclosure. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, *i.e.*, a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, *i.e.*, a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

Generally, the present disclosure relates to manufacturing techniques and related semiconductor devices in which field effect transistors of different conductivity type may receive a strained semiconductor material in the drain and/or source regions in order to provide a desired magnitude and/or type of strain in the corresponding channel regions of these transistors. For this purpose, in some illustrative embodiments, different semiconductor alloys may be used, such as silicon/germanium and silicon/carbon, on the basis of an appropriate manufacturing regime in which both materials may be embedded into the drain and source areas of the corresponding transistors by using an appropriately designed layer stack including a spacer layer and an etch stop layer. Furthermore, overall transistor performance for at least one type of transistor may be enhanced by incorporating any desired type of implantation species, such as dopants, non-doping species and the like, prior to forming a respective strained semiconductor material by epitaxial growth techniques. In this case, the electronic characteristics of the drain and source regions may be enhanced on the basis of the additional implantation species, which may be incorporated without creating additional implantation-induced damage, since the implantation process may be performed prior to growing the strained semiconductor material. Consequently, for N-channel transistors, a reduced source/drain junction resistance may be obtained due to a specifically optimized dopant profile. Furthermore, floating body effects in silicon-on-insulator (SOI) transistors may be reduced due to the presence of higher leakage currents of the corresponding PN junctions, which may, therefore, reduce charge carrier accumulation in the body region of the SOI transistors. A corresponding adjustment of the PN junction characteristics may also be accomplished by incorporating an appropriate implantation species prior to actually forming the strained semiconductor material. Additionally, the electron mobility may be enhanced due to the embedded silicon/carbon alloy in the drain and source areas of the N-channel transistor. Similarly, in P-channel transistors, a reduced source and drain resistance may be obtained due to the lower intrinsic resistivity of the silicon/germanium material, and also leakage currents through the PN junctions may be adjusted to a moderately high value, depending on the overall transistor characteristics, thereby also reducing charge carrier accumulation in SOI transistors. Finally, the increased hole mobility in the channel region caused by the embedded silicon/germanium alloy may additionally contribute to the overall enhanced device performance. Furthermore, since both strain-inducing semiconductor materials may be incorporated at a moderately early manufacturing stage, additional strain-inducing mechanisms may be implemented into the overall manufacturing flow substantially without requiring additional process steps. For example, strain-inducing spacer elements

and/or strain-inducing dielectric cap layers may be provided in order to further enhance strain in at least one type of transistor.

In other illustrative embodiments disclosed herein, a highly efficient manufacturing sequence may be used in incorporating a silicon/carbon material into transistors of different conductivity type, wherein additional strain-inducing mechanisms may also be used, for instance, in the P-channel transistor to overcompensate for any negative effect of the silicon/carbon material, while at the same time taking advantage of the characteristics of carbon with respect to acting as a diffusion hindering species, which may thus provide dopant profiles of enhanced accuracy in the P-channel transistor. Consequently, in combination with the enhanced electronic characteristics of the drain and source regions of the P-channel transistor and the overcompensated strain component, a significant enhancement of the P-channel transistor may be achieved, wherein, for SOI architectures, reduced floating body effects may also be achieved, while the N-channel transistor may exhibit reduced source/drain junction resistance in combination with increased electron mobility in the channel region due to the embedded silicon/carbon alloy. Also, in this case, charge carrier accumulation in the floating body of SOI N-channel transistors may be reduced by providing PN junctions of increased leakage currents due to the presence of the carbon species.

Figure 1a schematically illustrates a cross-sectional view of a semiconductor device 100, which may comprise a first transistor 150P and a second transistor 150N at an early manufacturing stage. The semiconductor device 100 may comprise a substrate 101, which may represent any appropriate carrier material for forming thereabove a semiconductor layer 103, such as a silicon-based layer, the electronic characteristics of which may be locally adapted by generating a specific type of strain for the first and second transistors 150P, 150N. The semiconductor layer 103 may represent a silicon-based layer, *i.e.*, a semiconductor material including a significant amount of silicon, wherein other components, such as germanium, carbon, dopant species and the like, may also be present. Furthermore, in the embodiment shown, a buried insulating layer 102 may be positioned between the substrate 101 and the semiconductor layer 103, thereby defining an SOI architecture, wherein it should be appreciated that, in other device areas of the device 100, a bulk configuration may be provided, depending on the overall device requirements. It should be noted that the principles disclosed herein may be very advantageous with respect to an SOI architecture, since efficient strain-inducing mechanisms may be provided in combination with additional

measures for reducing charge carrier accumulation, which may generally improve performance of SOI transistors with respect to floating body effects and hysteresis effects, *i.e.*, a threshold variation depending on the "switching history" of a corresponding transistor element. In other illustrative embodiments, the principles disclosed herein may also be advantageously applied to a bulk configuration, *i.e.*, a configuration in which a thickness of the semiconductor layer 103 may be greater than a depth of drain and source regions still to be formed in the transistors 150P, 150N.

Furthermore, appropriate active regions may be defined in the semiconductor layer 103 on the basis of appropriate isolation structures, such as shallow trench isolations (not shown), which may also be provided between the transistors 150P, 150N. Furthermore, the transistors 150P, 150N may comprise a gate electrode structure 151 which may include, in this manufacturing stage, an electrode material 151A, which is formed on a gate insulation layer 151B, which separates the electrode material 151A from a channel region 152. The gate electrode material 151A may represent any appropriate material, such as polysilicon and the like, which may even be replaced by a material of enhanced conductivity in a later manufacturing stage, depending on the overall process and device requirements. Similarly, the gate insulation layer 151B may be comprised of any appropriate dielectric material, such as silicon dioxide-based materials, silicon nitride, silicon oxynitride, high-k dielectric materials, such as hafnium oxide, zirconium oxide and the like. Furthermore, the gate electrode structures 151 may include a cap layer 151C which may be comprised of silicon nitride and the like. Furthermore, the semiconductor device 100 may comprise a layer stack 104 that is formed above the transistors 150P, 150N and, in the embodiment shown, may comprise a first layer or spacer layer 104A, above which may be provided a second layer or etch stop layer 104B. In one illustrative embodiment, the spacer layer 104A may be comprised of silicon nitride while the etch stop layer 104B may be formed of silicon dioxide. Thus, in the embodiment shown, the spacer layer 104A and the cap layer 151C may be comprised of material having similar characteristics with respect to a subsequent etch process so that these components may be removed during a common etch sequence. Furthermore, the etch stop layer 104B may have a thickness that is sufficient to provide the desired etch stop capabilities during an etch process for locally providing an etch and growth mask above the transistor 150N. For example, the etch stop layer 104B may be provided with a thickness of approximately 20-50 nm or even more, when provided in the form of a silicon dioxide material. On the other hand, the spacer layer 104A may be provided with an appropriate thickness in a

highly conformal manner in order to adjust a desired offset during an etch process for forming cavities in the semiconductor layer 103 in a later manufacturing stage. For instance, a thickness of the spacer layer 104A may range from approximately 1-20 nm in sophisticated applications in which a gate length, *i.e.*, the horizontal extension of the gate electrode material 151A in Figure 1a, may be approximately 50 nm and less, such as 30 nm and less. It should be appreciated, however, that an increased thickness may be selected if an increased offset may be required during the further processing.

The semiconductor device 100 as shown in Figure 1a may be formed on the basis of the following processes. After forming respective isolation structures (not shown) and defining corresponding basic dopant profiles for the transistors 150P, 150N in the semiconductor layer 103, the gate electrode structure 151 may be formed by well-established techniques, which may include oxidation and/or deposition of a gate dielectric material followed by the deposition of the gate electrode material 151A and material of the cap layer 151C. The corresponding material stack may be patterned by sophisticated lithography and etch techniques. Next, the stack 104 may be formed, for instance, by depositing the spacer layer 104A, for instance using thermally activated chemical vapor deposition (CVD) techniques, wherein, if required, a thin oxide layer may be formed by oxidation on exposed areas of the gate electrode material 151A and the semiconductor layer 103. Thereafter, the etch stop layer 104B may be formed, by instance, by CVD and the like, wherein material density and thickness of the etch stop layer 104B may be selected such that the desired etch stop capabilities may be obtained. Thereafter, a mask material (not shown) may be deposited, for instance by plasma assisted CVD, thermally activated CVD and the like, which may be subsequently patterned by photolithography and appropriate selective etch techniques.

Figure 1b schematically illustrates the semiconductor device 100 with a mask 105 that covers the second transistor 150N while exposing the first transistor 150P, *i.e.*, the layer stack 104 formed thereabove. The mask 105 may represent, in one illustrative embodiment, a hard mask, for instance comprised of silicon nitride or any other appropriate material, which may be etched selectively to the etch stop layer 104B. In other illustrative embodiments, any other appropriate material, such as a resist material, may be selectively formed above the second transistor 150N and may be used for patterning the layer stack 104 in the first transistor 150P.

Figure 1c schematically illustrates the semiconductor device 100 during an etch sequence 106, which may comprise a first etch step for selectively removing the etch stop layer 104B, which may be accomplished on the basis of well-established etch techniques, for instance by using hydrofluoric acid (HF), and thereafter an anisotropic etch step may be performed to etch the spacer layer 104A selectively to material of the semiconductor layer 103, while, in other cases, a thin oxide layer (not shown) may be provided to act as an etch stop material during the anisotropic etch process. Hence, after the etch process 106, a sidewall spacer 104S may be formed on sidewalls of the gate electrode structure 151, wherein a width of the spacer 104S is substantially determined by the initial layer thickness of the spacer layer 104A and the conditions of the etch sequence 106. In the embodiment shown, a certain degree of material erosion may also occur in the mask 105, as indicated by the dashed line, if the spacer layer 104A and the mask 105 are comprised of materials having a similar etch behavior or may be comprised of substantially the same material. In other illustrative embodiments, the mask 105 may represent a resist material, at least during the first etch step of the sequence 106 for selectively removing the etch stop layer 104B above the first transistor 150P. Thereafter, if required, the resist mask may be removed and the anisotropic etch step of the sequence 106 may be performed on the basis of a selective etch recipe, wherein the etch stop layer 104B may protect the remaining portion of the layer 104A above the second transistor 150N.

Figure 1d schematically illustrates the semiconductor device 100 in a further advanced manufacturing stage, in which a further etch process 107 may be performed to obtain recesses or cavities 103P adjacent to the gate electrode structure 151 in the semiconductor layer 103 of the first transistor 150P. The etch process 107 may be performed on the basis of well-established etch recipes, such as isotropic recipes, anisotropic recipes or a combination thereof, depending on the desired shape and size of the cavities 103P. For example, a plurality of etch chemistries are available for removing silicon material selectively with respect to silicon nitride material, oxide material and the like which may be used for forming the cavities 103P. During the etch process 107, respective process parameters, such as plasma power, pressure, the type and amount of polymer materials for controlling a horizontal removal rate and the like, may be selected such that a desired shape of the cavities 103P may be obtained. For example, an offset of the cavities 103P from the channel region 152 may be substantially determined by the width of the spacer 104S. If a more or less pronounced degree of under-etching may be desired, the process parameters and/or the etch

chemistry may be appropriately selected, for example, from the beginning of the etch process 107 or at a certain phase of the process, depending on the desired overall size and shape of the cavities 103P. In the embodiment shown, the mask 105 may protect the layer stack 104 formed above the second transistor 150N. In other cases, the mask 105 may have been removed in an earlier manufacturing stage, if provided as a resist material and the like, so that, in this case, the etch stop layer 104B may reliably protect the spacer layer 104A.

In some illustrative embodiments, after the etch process 107 and prior to or after the removal of the mask 105, one or more implantation processes 108 may be performed to incorporate one or more implantation species 108A through exposed surface portions of the cavity 103P. For example, the one or more implantation processes 108 may comprise one or more steps performed on the basis of a non-zero tilt angle, which is to be understood as a non-zero angle with respect to a normal of the semiconductor layer 103 or the buried insulating layer 102. Consequently, any desired implantation species may be incorporated, wherein the positioning of the implantation species 108A may be controlled by the process parameters of the one or more implantation processes 108, such as energy, dose, tilt angle, type of implantation species and the like. In some illustrative embodiments, the implantation species 108A may comprise a dopant species, for instance for counter-doping material of the layer 103 with respect to drain and source areas to be formed in a later manufacturing stage on the basis of a strained semiconductor material to be filled into the cavities 103P. Moreover, in other illustrative embodiments, the implantation species 108A may comprise a dopant for defining at least a portion of drain and source regions, such as an extension region to avoid additional implantation steps in a later manufacturing stage after providing a strained semiconductor material in the cavities 103P. In other illustrative embodiments, respective drain and source extension regions may have been formed in an early manufacturing stage, for instance prior to or after the deposition of the spacer layer 104A, depending on the initial layer thickness thereof. In still other illustrative embodiments, the implantation species 108A may comprise corresponding components, such as nitrogen, carbon and the like, which may result in a reduced diffusion activity of a corresponding dopant species, such as boron, which may be provided in a later manufacturing stage. In this manner, the finally obtained PN junctions of the drain and source regions may be defined with enhanced accuracy on the basis of one or more components of the implantation species 108A. Moreover, the degree of leakage currents through the PN junctions still to be formed may also be adjusted on the basis of the implantation species 108A, thereby enabling a highly efficient stabilization of

threshold voltage of the transistor 150P with respect to floating body effects. During the implantation process 108, undue incorporation of the implantation species 108A into the gate electrode material 151A may be suppressed or at least reduced by the spacers 104S and the cap layer 151C. In other embodiments, in which the mask 105 may have been removed at an earlier manufacturing stage, the corresponding shadowing effect during a tilted implantation step of the process 108 may be reduced.

Figure 1e schematically illustrates the semiconductor device 100 during a selective epitaxial growth process 109, which may be performed on the basis of well-established process recipes in order to deposit a semiconductor alloy selectively on exposed surfaces of the cavities 103P (Figure 1d) while substantially avoiding significant material deposition on dielectric surface areas. For example, during the growth process 109, silicon/germanium may be deposited with a desired fraction of germanium so that, upon growing on the silicon layer 103, a strained state may be obtained, the magnitude of which may be determined on the fraction of germanium. For example, approximately 15-35 atomic percent germanium may be incorporated into the silicon/germanium alloy in order to form a strained semiconductor material 153P. It should be appreciated that, in other illustrative embodiments, in addition or alternatively to germanium, other atomic species having a greater covalent radius compared to silicon may be used, such as tin, which may also be incorporated into the material 153P. In this case, a significantly reduced fraction of non-silicon material may be incorporated, while nevertheless providing a desired difference of the natural lattice constant of the material 153P with respect to the surrounding template material of the layer 103. In some illustrative embodiments, during the growth process 109, a dopant species may also be incorporated into the material 153P, such as boron, so that further implantation processes may be avoided or may at least be reduced with respect to the implantation dose, thereby also maintaining implantation-induced damage of the material 153P at a low level. Thereafter, the further processing may be continued by removing the mask 105, which may be accomplished by well-established selective etch recipes, for instance using hot phosphoric acid, thereby efficiently removing the mask 105 when comprised of silicon nitride, selectively to the etch stop layer 104B, while also removing the spacers 104S and the cap layer 151C in the transistor 150P.

Figure 1f schematically illustrates the semiconductor device 100 after the above-described process sequence. Moreover, the device 100 is exposed to an etch ambient 110

designed to selectively remove the exposed etch stop layer 104B, while maintaining the spacer layer 104A. For this purpose, well-established selective etch recipes, for instance on the basis of hydrofluoric acid (HF), may be used. Thereafter, a further etch process may be performed in order to anisotropically etch the exposed spacer layer 104A, as is also explained with reference to the etch process 106 (Figure 1c).

Figure 1g schematically illustrates the semiconductor device 100 after the above-described process sequence and with a further mask 111 that covers the first transistor 150P, while the second transistor 150N has the gate electrode structure 151 that now comprises spacer elements 104R due to the previously performed anisotropic etch process. The mask 111 may be comprised of silicon nitride or any other material that is compatible with the further processing.

Figure 1h schematically illustrates the semiconductor device 100 during an etch process 112, which may be performed on the basis of similar process parameters as the etch process 107 (Figure 1d). That is, process parameters and etch chemistries of the etch process 112 may be selected in accordance with a desired size and shape of cavities 103N created adjacent to the gate electrode structure 151, wherein the spacers 104R protect the sidewalls thereof and also define an offset of the cavities 103N with respect to the channel region 152, similarly as is discussed above when referring to the first transistor 150P. Consequently, the size and shape of the cavities 103N may be adjusted independently from a size and shape of the corresponding cavities 103P (Figure 1d). Furthermore, in some illustrative embodiments, an implantation process or sequence 113 may be performed to incorporate one or more implantation species 113A through exposed surface portions of the cavities 103N. Also, in this case, the implantation process 113 may include one or more implantation steps with a non-zero tilt angle so as to appropriately position the one or more implantation species 113A. For instance, a counter-doped region may be formed, a dopant species may be incorporated or any other implantation species, such as non-doping species in the form of carbon, nitrogen and the like, may be incorporated to adjust the overall electronic characteristics, for instance in view of leakage currents and the like, as is also previously discussed with reference to the transistor 150P, wherein it should be appreciated that, due to the different conductivity type of the transistors 150N and 150P, the implantation process 113 may differ from the corresponding process 108 (Figure 1d) with respect to implantation parameters and implantation species.

Figure 1i schematically illustrates the semiconductor device 100 during a further selective epitaxial growth process 114 designed to deposit a strained semiconductor material 153N. In a further illustrative embodiment, the semiconductor material 153N may comprise a silicon/carbon alloy, which has a natural constant that is less than the lattice constant of silicon, thereby growing in a tensile strained state which may thus result in a tensile strain in the adjacent channel region 152. For example, an appropriate fraction of carbon material may be incorporated into the silicon material of the deposition ambient 114, for instance one to several atomic percent, depending on the desired degree of tensile stress and other electronic characteristics of drain and source regions to be formed in the second transistor 150N. Furthermore, as previously indicated, an appropriate dopant species, that is, an N-type species, may be incorporated into the material 153N during the growth process 114 so as to avoid further implantation processes or reduce at least the degree of ion bombardment during subsequent implantation processes for defining the finally desired dopant profile for the second transistor 150N. After the selective epitaxial growth process 114, an etch process, for instance on the basis of hot phosphoric acid and the like, may be performed in order to remove the mask 111 and the spacers 104R and the cap layer 151C.

Figure 1j schematically illustrates the semiconductor device 100 after the above-described process sequence. Hence, the gate electrode structures 151 of both transistors 150P, 150N may be exposed prior to the further processing of the device 100, while, in other embodiments, as indicated by the dashed line, a protection layer 115, such as a silicon dioxide layer and the like, may be provided prior to performing additional manufacturing processes for completing the transistors 150P, 150N.

Figure 1k schematically illustrates the semiconductor device 100 in a further advanced manufacturing stage. As illustrated, drain and source regions 154 may be formed adjacent to the channel region 152, wherein the drain and source regions 154 may comprise at least a portion of the strained semiconductor materials 153P, 153N, respectively. That is, depending on the device requirements, the strained materials 153N, 153P may be positioned entirely within the drain and source regions 154, as shown, which may be accomplished by incorporating a high concentration of the corresponding dopant species and performing an anneal process for initiating a diffusion of the dopant species. In other cases, a portion of the PN junctions 154P may extend through the strained semiconductor material, at least in one of

the transistors 150P, 150N. It should be appreciated that, as previously discussed with reference to the implantation processes 108 (Figure 1d) and 113 (Figure 1h), the additional implant species 108A and/or 110A may be present so as to adjust the overall transistor characteristics, for instance in view of leakage of the PN junctions 154P, the dopant gradient, for instance by reducing the overall diffusivity of dopant species, such as boron, which may thus result in an enhanced confinement of the dopant species and thus of the drain and source regions 154 for the transistor 150P, which may represent a P-channel transistor.

Furthermore, the semiconductor device 100 may comprise a spacer structure 156 formed adjacent to the gate electrode material 151A, wherein the spacer structure 156 may comprise a plurality of individual spacer elements 156A, 156B, depending on the overall process and device requirements. For instance, the drain and source regions 154, at least for one of the transistors 150P, 150N, may be adjusted on the basis of additional implantation processes, during which the corresponding spacer elements 156A, 156B may act as implantation masks. In other illustrative embodiments, additional implantation processes may be substantially avoided after forming the strained semiconductor materials 153P, 153N, respectively, thereby also maintaining lattice damage in these materials at a low level. In this case, the spacer structure 156 may be provided to act as a mask for forming metal silicide regions 155 in a self-aligned manner. In some illustrative embodiments, the spacer structure 156 may comprise a high intrinsic stress level, which may be appropriate for enhancing performance of one of the transistors 150P, 150N. For example, the spacer structure 156 may have a high tensile stress level, thereby providing additional strain in the channel region 152 of the transistor 150N. On the other hand, a negative influence of the internal stress level in the transistor 150P may be overcompensated for by additional stress-inducing mechanisms, such as strain-inducing dielectric layers 116 and 117, which may be provided with high internal tensile stress and compressive stress, respectively. For instance, silicon nitride may be deposited with high internal stress levels, depending on the corresponding process parameters of a plasma enhanced CVD technique. For example, stress levels up to 1 GPa and higher for a tensile silicon nitride material may be obtained, while stress levels of up to 2 GPa and higher may be accomplished for a compressively stressed silicon nitride material. Consequently, by providing a high internal compressive stress level in the layer 117, any tensile internal stress of the spacer structure 156 in the transistor 150P may be compensated for. In other illustrative embodiments, a compressive stress level may be established in the

spacer structures 156, when a further pronounced performance gain may be desired in the transistor 150P.

The semiconductor device 100 as shown in Figure 1k may be formed on the basis of the following processes. The drain and source regions 154 may be formed, for instance, by ion implantation for forming shallow drain and source extension regions (not shown), wherein implantation-induced damage of the materials 153P, 153N may be less pronounced. In other cases, as previously discussed, corresponding extension regions may have been formed prior to growing the materials 153P, 153N, respectively. If required, further implantation processes may be performed to incorporate additional dopant species and/or the corresponding dopant species may have been incorporated during the growth processes for the materials 153P, 153N. Furthermore, appropriate anneal processes may be performed in order to establish the desired dopant profile for the drain and source regions 154, wherein also the corresponding implantation species 113A (Figure 1h), 108A (Figure 1d) may enable a more precise control of the finally obtained electronic characteristics. Thereafter, the metal silicide regions 155 may be formed in accordance with well-established techniques, wherein the spacer structure 156 may be used as a silicidation mask. Subsequently, the layers 116 and 117 may be deposited, wherein one or both of the layers may have a high intrinsic stress level, as explained above, which may be accomplished on the basis of respective patterning regimes in which one of the layers 116, 117 may be deposited and may subsequently be removed from above one of the transistors 150P, 150N, followed by the deposition of the other one of the layers 116, 117 and the removal thereof from the other one of the transistors 150P, 150N.

As a consequence, the strained semiconductor materials 153P, 153N may be formed on the basis of selective epitaxial growth techniques, wherein appropriate mask and etch stop layers, such as the layers 104A, 104B (Figure 1a) may be used, possibly in combination with the incorporation of appropriate implantation species, such as species 113A (Figure 1h), 108A (Figure 1d), and may provide enhanced electronic characteristics and strain conditions, as is also previously explained.

With reference to Figures 2a-2h, embodiments will be described in which a strained semiconductor material of reduced natural lattice constant compared to silicon may be

provided in transistors of different conductivity type to obtain performance enhancement of both types of transistors.

Figure 2a schematically illustrates a semiconductor device 200 comprising a substrate 201, a buried insulating layer 202 and a semiconductor layer 203. Furthermore, gate electrode structures 251 of a first transistor 250P and a second transistor 250N of different conductivity type are formed above the semiconductor layer 203. The gate electrode structures 251 may comprise a gate electrode material 251A, a gate insulation layer 251B and a cap layer 251C. With respect to the components described so far, the same criteria apply as previously explained with reference to the semiconductor device 100. Furthermore, a spacer layer 204 is formed on the gate electrode structures 251, wherein the spacer layer 204 may have an appropriate thickness for adjusting an offset of cavities to be formed in the layer 203 in a later manufacturing stage. The semiconductor device 200 as shown in Figure 2a may be formed on the basis of the same process techniques as previously described with reference to the device 100.

Figure 2b schematically illustrates the semiconductor device 200 with spacer elements 204S formed on sidewalls of the gate electrode structures 251, which may be accomplished on the basis of well-established etch techniques, as previously explained, wherein, if required, a thin etch stop liner (not shown), for instance in the form of silicon dioxide, may be provided, for instance, by oxidation of exposed surface portions of the gate electrode material 251A and the semiconductor layer 203.

Figure 2c schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage. As illustrated, the device 200 is exposed to an etch ambient of an etch process 207 for forming cavities 203P and 203N in the transistors 250P, 250N, respectively. The etch process 207 may be performed on the basis of well-established etch chemistries exhibiting a moderately high selectively with respect to the material of the spacers 204S and the cap layer 251C so as to not unduly remove material of the gate electrode materials 251A. Since the etch process 207 may be performed simultaneously for the transistors 250P, 250N, generally the overall process uniformity may be enhanced due to the absence of etch masks. Consequently, the across-substrate uniformity, for instance with respect to a depth of the corresponding cavities 203P, 203N may be enhanced. Moreover, any additional lithography steps for individually providing the cavities 203P, 203N may be

avoided. In some illustrative embodiments, starting from the device 200 as shown in Figure 2a, the etch sequence for defining the spacers 204S and forming the cavities 203P, 203N may be performed as an *in situ* process, *i.e.*, within the same process chamber, while appropriately adapting the etch chemistry during the various phases of the common etch process. After the etch process 207, the device 200 may be prepared for the deposition of a strain-inducing semiconductor material, which may include respective cleaning processes and the like.

Figure 2d schematically illustrates the semiconductor device 200 during a selective epitaxial growth process 209, which may be designed to deposit a semiconductor alloy 253, for instance in the form of a silicon/carbon alloy, which may be grown on the silicon-based template material of the layer 203 with a tensile strain level. With respect to corresponding process parameters of the process 209, similar criteria apply as previously explained with reference to the semiconductor device 100. It should be appreciated that, also during the selective epitaxial growth process 209, enhanced overall process uniformity may be achieved, due to the absence of extended mask regions, in which a deposition of the material 253 may not be desired. Furthermore, the material 253 may be deposited in a substantially non-doped state since the corresponding drain and source regions may require a different type of dopant species for the transistors 250P, 250N, respectively. Thus, a tensile strain component may be induced in channel regions 252 of transistors 250P, 250N, wherein the tensile strain component 252T may be directed along the channel length direction, that is, in Figure 2d, the horizontal direction.

Figure 2e schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage. As shown, the device 200 may be exposed to an ion bombardment 208, wherein the second transistor 250N may be masked by an appropriate mask 210, such as a resist mask, while the transistor 250P is exposed. In some illustrative embodiments, as shown, the spacers 204S and the cap layers 251C may have been removed prior to forming the mask 210, while, in other cases, the gate electrode structures 251 may still be encapsulated by the spacers 204S and the cap layers 251C (not shown). Maintaining the cap layer 251C during the ion bombardment 208 may reduce the penetration of the corresponding species into the gate electrode material 251A, if deemed inappropriate. In the embodiment shown, the ion bombardment 208 may be performed with the spacers 204S removed, wherein, if desired, offset spacers of reduced width (not shown) may be provided on sidewalls of the gate electrode materials 251A. Consequently, during the ion bombard-

ment 208, the crystalline structure of portions of the semiconductor layer 203 and of the previously grown semiconductor alloy 253 may be heavily damaged or substantially amorphized. For this purpose, any appropriate implantation species may be used, such as xenon, germanium, silicon, krypton and the like. It should be appreciated that appropriate implantation parameters for the bombardment 208 may readily be determined on the basis of well-established simulation programs, experiments and the like. Consequently, the material 253 may be relaxed, thereby forming a substantially relaxed semiconductor alloy 253P. In addition, the semiconductor material adjacent to the gate electrode material 251A may also be heavily damaged or amorphized, depending on a width of a corresponding offset spacer, if provided.

Figure 2f schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage. As illustrated, a stress-inducing material layer 218, for instance comprised of silicon nitride, nitrogen-containing silicon carbide and the like, may be formed above the first and second transistors 250P, 250N, which may have a high intrinsic compressive stress level of one or more GPa or even higher. For example, as previously explained with reference to the layers 116, 117 (Figure 1k), silicon nitride material may be formed so as to have a high compressive stress level by selecting appropriate deposition parameters. Thus, the layer 218 may induce a moderately high compressive stress level in the previously relaxed material 253P and thus in the channel region 252 of the transistor 250P. Similarly, temporarily, the strain component in the channel region 252 of the transistor 250N may be compensated or even over-compensated by the stress-inducing layer 218. Furthermore, the device 200 is subjected to an anneal process 219 designed to re-crystallize the heavy lattice damage created in the material 253P and adjacent to the channel region 252 of the first transistor 250P. For example, any appropriate anneal technique, such as rapid thermal anneal, laser-based or flashlight-based anneal techniques, may be used in which an efficient re-crystallization may occur. Due to the presence of the highly stressed layer 218, the material 253P and any material of the layer 203 adjacent thereto may re-grow in a highly compressively stressed state, thereby preserving the compressive strain component in the channel region 252 of the first transistor 250P. It should be appreciated that, due to the strained state of the re-crystallized material 253P, the corresponding compressive strain component 252C may be maintained in the channel region 252, even after removal of the layer 218. Techniques in which a substantially amorphized semiconductor material may be

re-grown in the presence of a stressed cap layer may frequently be referred to as stress memorization techniques.

Figure 2g schematically illustrates the semiconductor device 200 after the removal of the stress-inducing cap layer 218. It should be appreciated that an appropriate etch stop material may be provided along with the stress-inducing layer 218, if desired, in order to enhance the removal process. In other cases, the layer 218 may be removed on the basis of highly selective etch recipes, in which, for instance, silicon nitride material may be removed selectively with respect to silicon-based material. Consequently, in the transistor 250N, the tensile strain component 252T may be re-established due to the removal of the "external" strain-inducing source in the form of the layer 218, while the compressive strain component 252C in the transistor 250P may still be present due to the previously strained re-crystallization of the material 253P and material adjacent thereto, which may have also been amorphized during the process 208 (Figure 2e). On the basis of the device configuration as shown in Figure 2g, the further processing may be continued, for instance, by using well-established process techniques.

Figure 2h schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage in which drain and source regions 254 may be formed within the semiconductor layer 203, wherein at least a portion of the drain and source regions 254 may comprise the strain-inducing material 253 in the transistor 250N and the strain-inducing material 253P in the transistor 250P. Furthermore, a corresponding sidewall spacer structure 256 may be provided on sidewalls of the gate electrode structures 251, wherein, as is also previously explained with reference to the device 100, the spacer structure 256 may comprise any appropriate number of individual spacer elements in order to appropriately define the lateral and vertical dopant profile of the drain and source regions 254. Furthermore, metal silicide regions 255 may be formed in the drain and source regions and the gate electrode materials 251A.

The semiconductor device 200 as shown in Figure 2h may be formed on the basis of well-established process techniques, wherein the drain and source regions 254 may be created on the basis of the spacer structure 256 by means of ion implantation. In the transistor 250P, typically boron may act as a dopant species, wherein, however, due to the presence of an additional species, such as carbon, in the material 253P, enhanced doping profiles may be

obtained due to the diffusion hindering effect of the carbon species with respect to the boron species. That is, the PN junction at the transistor 250P, as indicated by 254P, may be defined in accordance with the corresponding implantation steps such that a significant length thereof may be within the semiconductor alloy 253P. Thus, upon annealing the device 200, the diffusion hindering effect of the carbon species may provide increased "confinement" of the boron species at least within the material 253P. Consequently, in addition to the compressive strain component 252C, the enhanced dopant gradient at the PN junction 254P, at least within the region 253P, may contribute to reduced junction resistance, which may also result in enhanced transistor performance. Furthermore, the presence of the carbon species in the transistors 250P, 250N may result in an increased leakage current of the respective PN junctions, which may thus provide an efficient mechanism for removing accumulated charges between the drain and source regions 254 during operation of the transistors 250P, 250N, as previously explained. Furthermore, as also previously explained with reference to the device 100, additional strain-inducing mechanisms may be implemented, for instance by providing highly stressed spacer elements in the spacer structure 256 and/or positioning stress-inducing layers, such as the layers 116, 117 (Figure 1k) above the transistors 250P, 250N so as to further enhance the overall strain components in these transistors.

As a result, the present disclosure provides semiconductor devices and methods of forming the same in which strained semiconductor materials, such as silicon/germanium and the like on the one hand and silicon/carbon on the other hand, may be incorporated in the drain and source regions on the basis of a highly efficient manufacturing flow, possibly in combination with additional implant species for further enhancing the overall transistor characteristics so that dopant profiles in combination with increased strain levels may be accomplished. In other cases, a semiconductor material having a natural lattice constant less than a silicon-based material may be used in transistors of different conductivity types, wherein a negative influence of the corresponding initially provided strain component may be overcompensated for by applying a stress memorization technique. Consequently, enhanced overall process uniformity may be achieved due to enhanced conditions during etching the respective cavities and depositing the semiconductor alloy, while at the same time dopant profile characteristics as well as leakage current behavior may be enhanced in both the P-channel transistor and the N-channel transistor, thereby also contributing to enhanced overall device characteristics.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

WHAT IS CLAIMED:

1. A method of forming a strained semiconductor material in a first transistor (150P) of a first conductivity type and a second transistor (150N) of a second conductivity type, the method comprising:

forming a stack of layers above a first gate electrode structure of said first transistor (150P) and a second gate electrode structure of said second transistor (150N), said first and second gate electrode structures comprising a respective cap layer (15K), said stack of layers comprising a spacer layer (104A) and an etch stop layer (104B) formed above said spacer layer (104A);

forming a mask above (105) said second transistor (150N) and above said etch stop layer (104B);

forming a first spacer element (104S) at said first gate electrode structure from said spacer layer (104A); forming first cavities (103P) in drain and source areas of said first transistor (150P) using said first spacer element (104S) as a mask;

forming a first strained semiconductor material (153P) in said first cavities (103P);

forming second cavities (103N) in drain and source areas of said second transistor (150N) using a second spacer element (104R) formed from said spacer layer (104A) as a mask; and

forming a second strained semiconductor material (153N) in said second cavities, (103N) said first and second strained semiconductor materials (153P, 153N) having a different material composition.

2. The method of claim 1, further comprising introducing one or more first implantation species into exposed surface portions of said first cavities (103P).

3. The method of claim 2, wherein said one or more first implantation species comprises a non-doping species for modifying a diffusion behavior of a dopant species of drain and source regions of said first transistor (150P).

4. The method of claim 2, wherein said one or more first implantation species comprises a dopant species for forming drain and source regions of said first transistor (150P).

5. The method of claim 1, further comprising introducing one or more second implantation species into exposed surface portions of said second cavities (103N).

6. The method of claim 5, wherein said one or more second implantation species comprises a non-doping species.

7. The method of claim 5, wherein said one or more second implantation species comprises a dopant species for forming drain and source regions of said second transistor (150N).

8. The method of claim 1, further comprising forming one or more stress-inducing spacer elements on sidewalls of said first and second gate electrode structures after forming said first and second strained semiconductor materials (153P,153N).

9. The method of claim 1, further comprising forming a first strain inducing layer above said first transistor (150P) and forming a second strain inducing layer above said second transistor, (150N) wherein said first and second strain inducing layers induce a different type of strain in channel regions of said first and second transistors.

10. The method of claim 1, wherein said first strained semiconductor material (153P) comprises a silicon/germanium alloy and said second strained semiconductor material (153N) comprises a silicon/carbon alloy.

11. A method, comprising:

forming first cavities (203P) adjacent to a first gate electrode structure of a first transistor (250P) and second cavities (203N) adjacent to a second gate electrode structure of a second transistor (250N) , said first and second transistors being of different conductivity type;

forming a semiconductor material (253) in said first and second cavities (203P, 203N), said semiconductor material (253) having a first type of strain;

creating lattice damage in said semiconductor material (253) selectively in said first transistor (250P) to form a substantially relaxed semiconductor material; and

re-crystallizing said substantially relaxed semiconductor material in a strained state, said strained state corresponding to a second type of strain that is opposite to said first type of strain.

12. The method of claim 11, wherein re-crystallizing said substantially relaxed semiconductor material comprises forming a strain-inducing material layer (218) above said first transistor (250P) and annealing said substantially relaxed semiconductor material in the presence of said strain-inducing material layer.

13. The method of claim 12, wherein said semiconductor material comprises a silicon/carbon alloy.

14. The method of claim 11, wherein said first and second cavities are formed in a common etch process.

15. The method of claim 11, further comprising forming a first strain-inducing layer above metal silicide regions of said first transistor (250P) and forming a second strain-inducing layer on metal silicide regions of said second transistor, (250N) wherein said first and second strain-inducing layers generate a different type of strain.

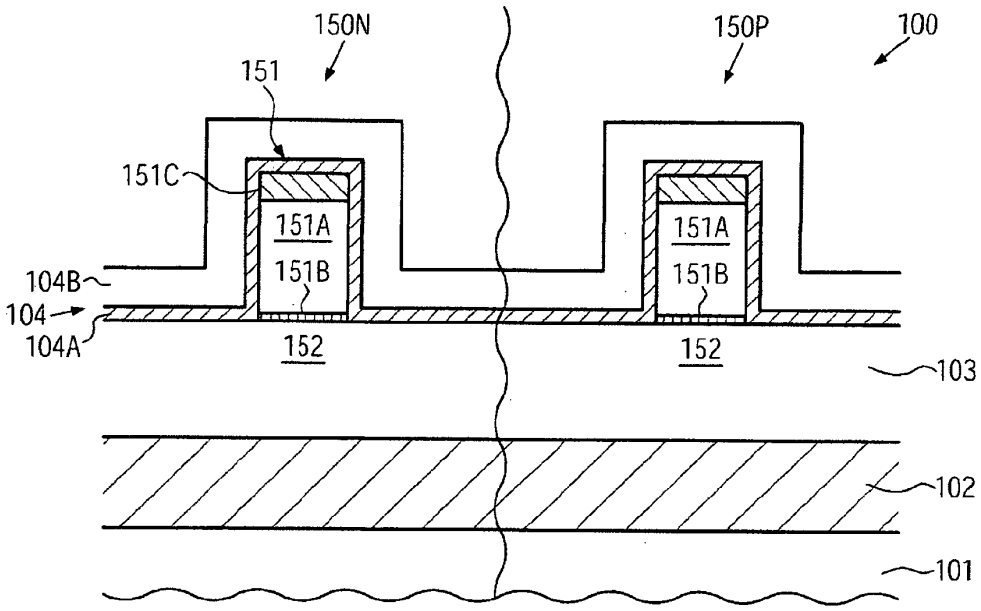

150N
150P
100
151
151C
151A
151B
104B
104
104A
152
152
103
102
101

FIG. 1a

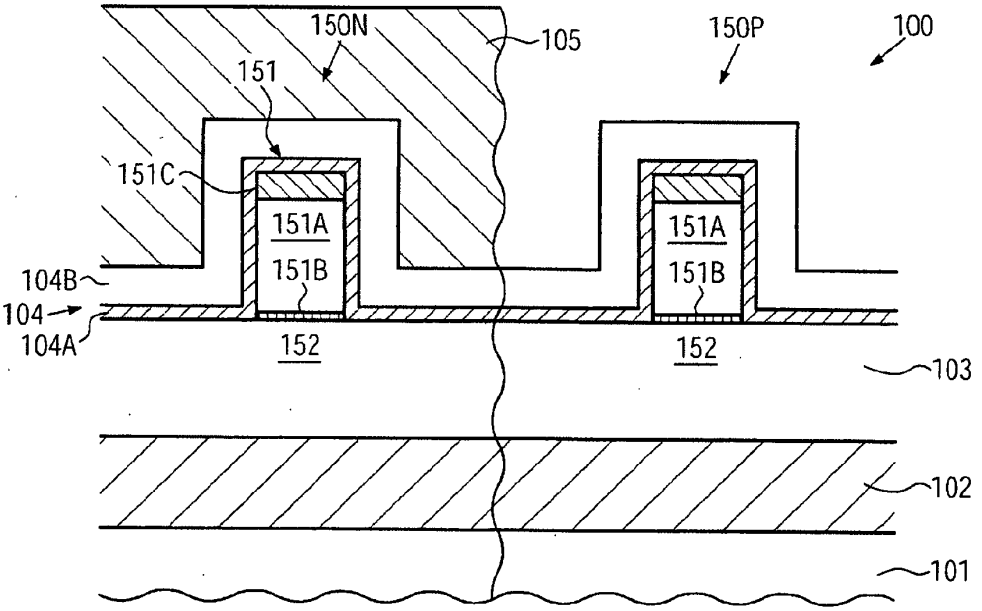

150N
105
150P
100
151
151C
151A
151B
104B
104
104A
152
152
103
102
101

FIG. 1b

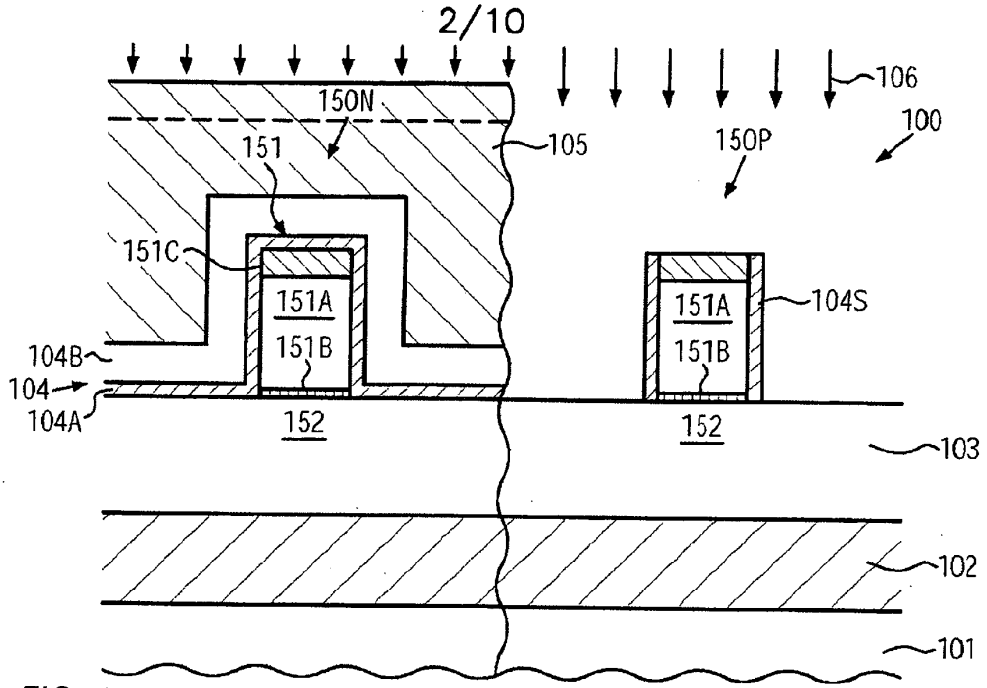

106
150N
100
151
105
150P
151C
151A
151B
104S
104B
104
104A
152
152
103
102
101

FIG. 1c

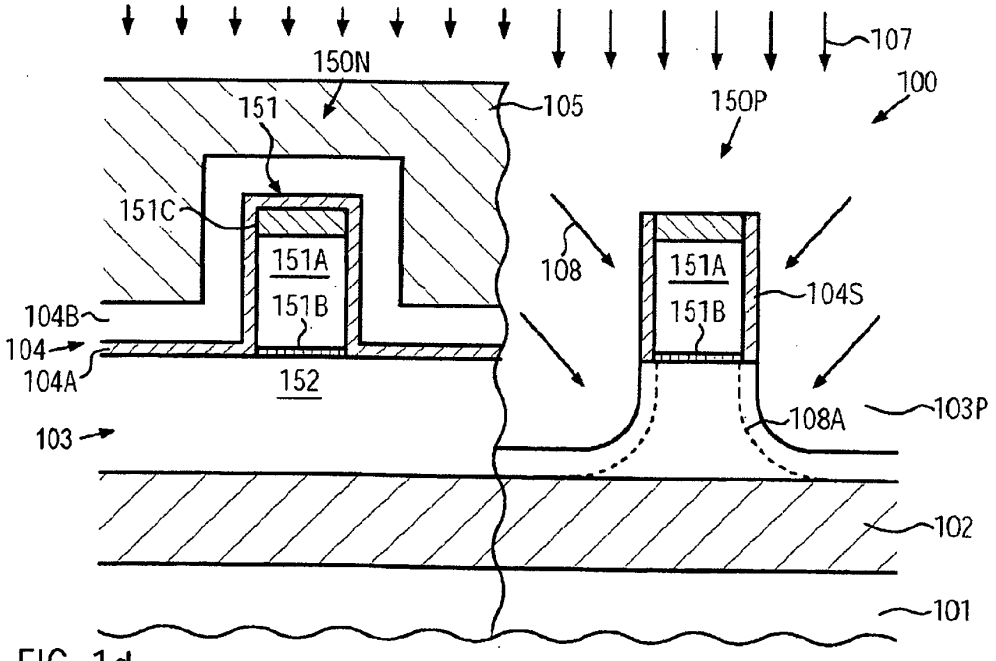

107
150N
100
151
105
150P
151C
151A
151B
108
104S
104B
104
104A
152
108A
103P
103
102
101

FIG. 1d

3/10

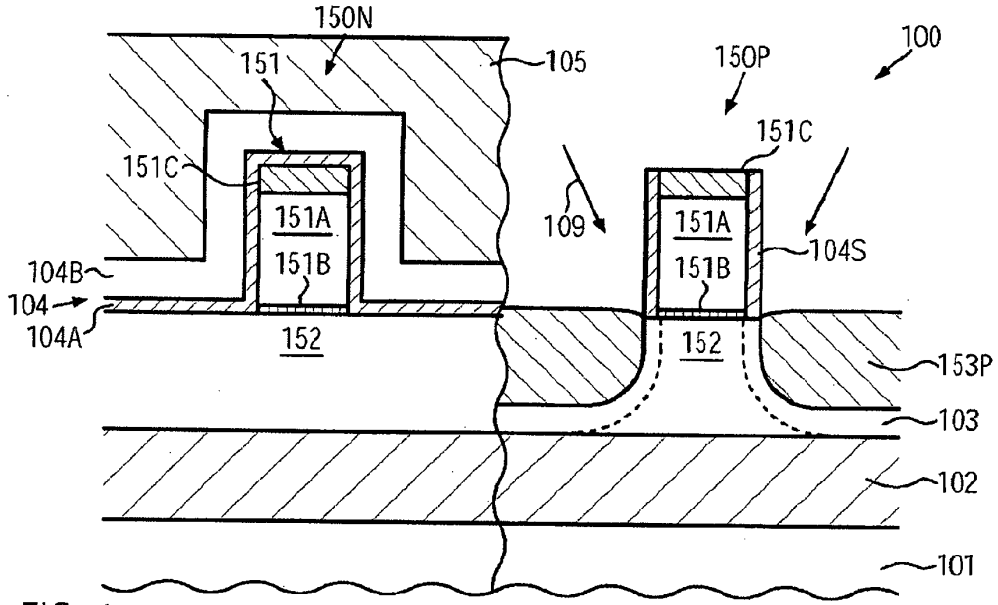


FIG. 1e

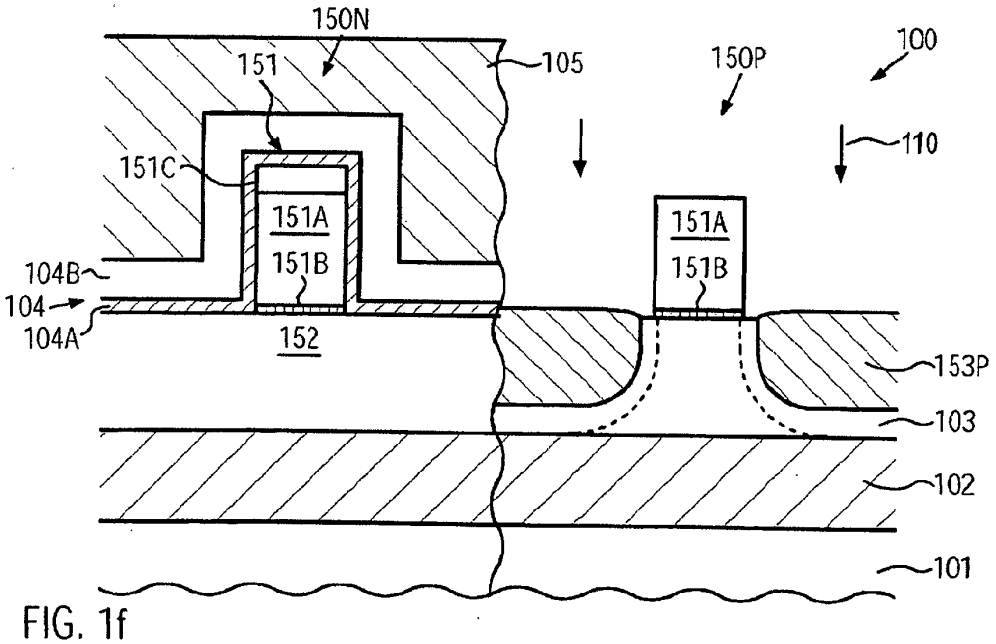


FIG. 1f

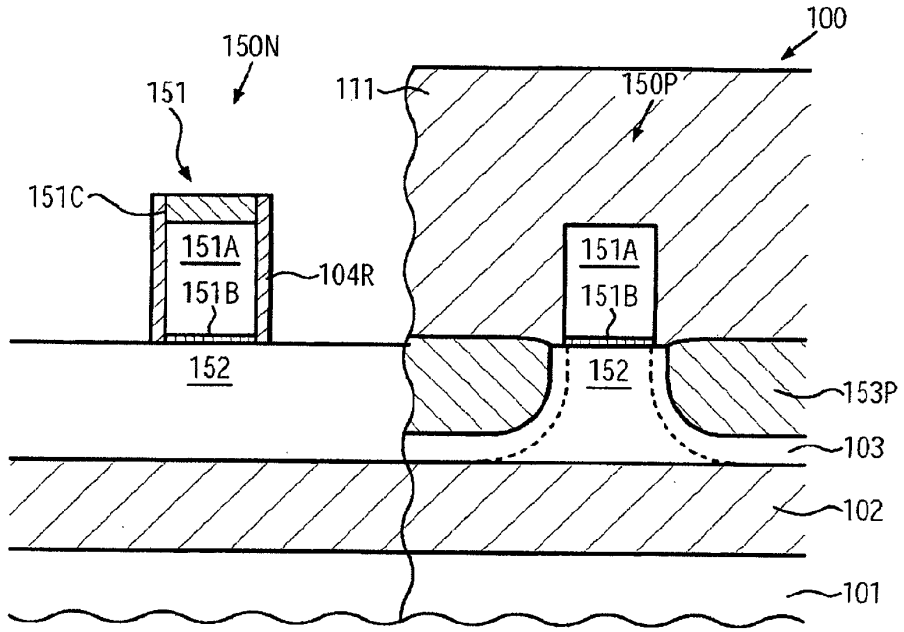

100
150N
151
111
150P
151C
151A
151B
104R
152
153P
103
102
101

FIG. 1g

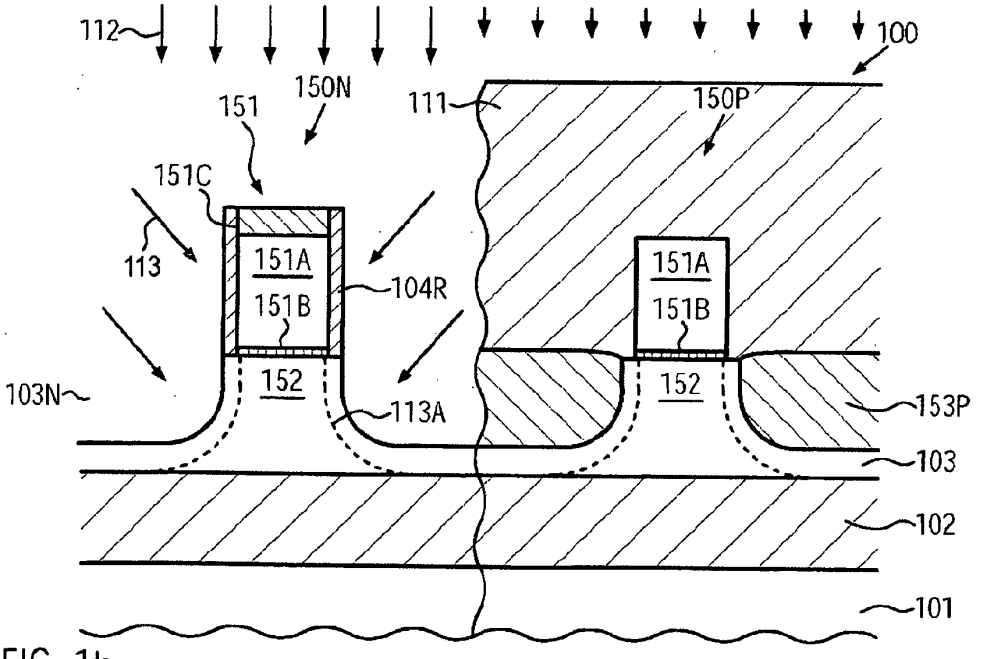

112
100
150N
151
111
150P
151C
113
151A
151B
104R
152
103N
113A
153P
103
102
101

FIG. 1h

5/10

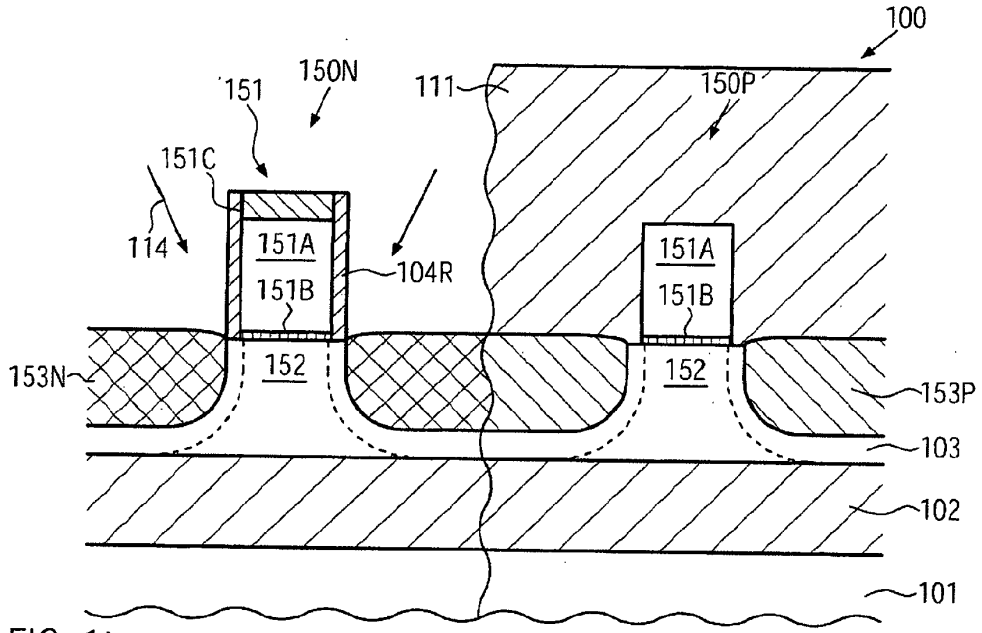


FIG. 1i

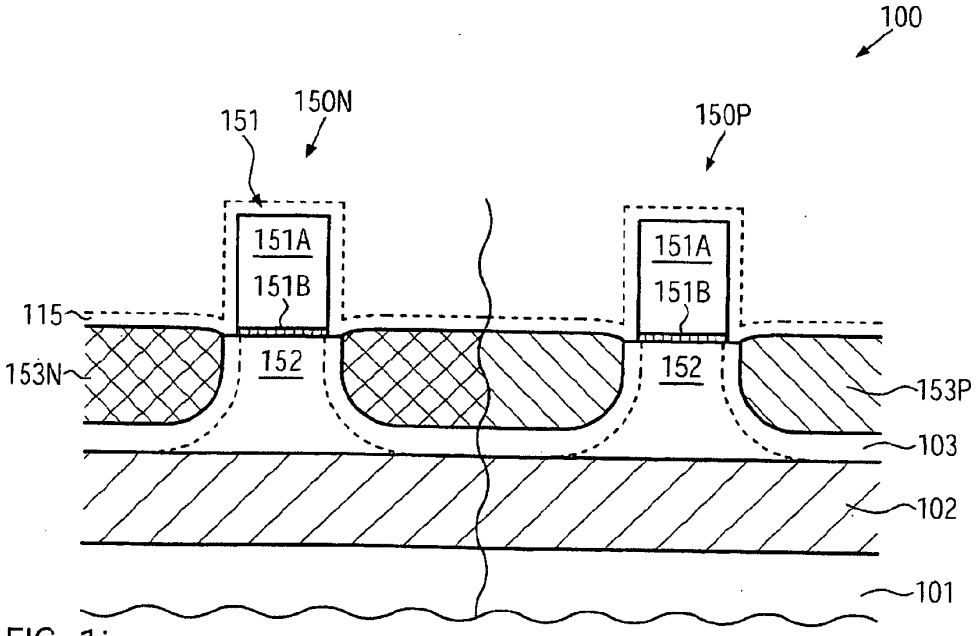


FIG. 1j

6/10

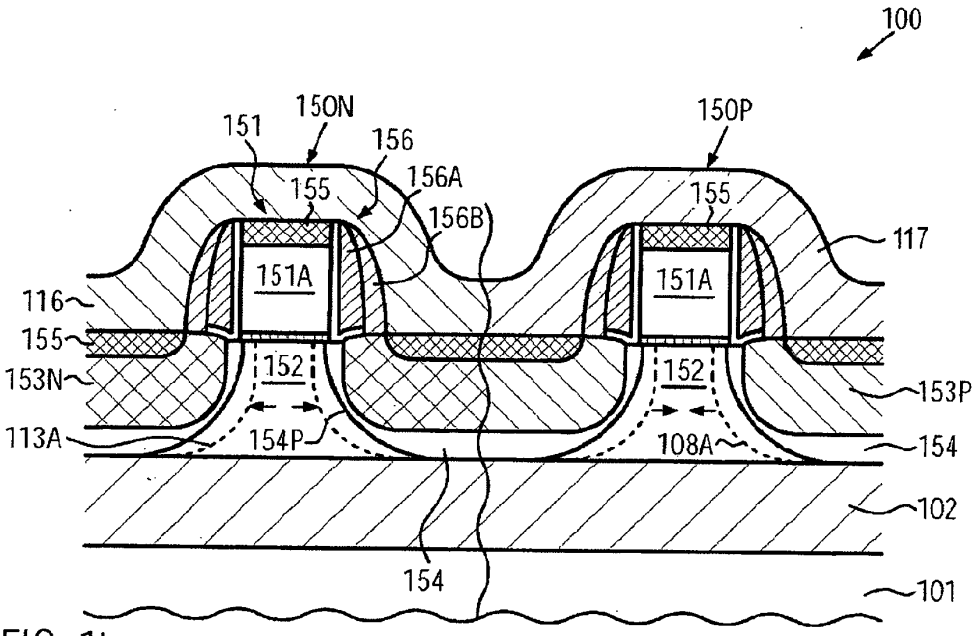

100
150N
151
156
155
156A
156B
150P
155
117
151A
151A
116
155
153N
152
152
153P
113A
154P
108A
154
102
154
101

FIG. 1k

7/10

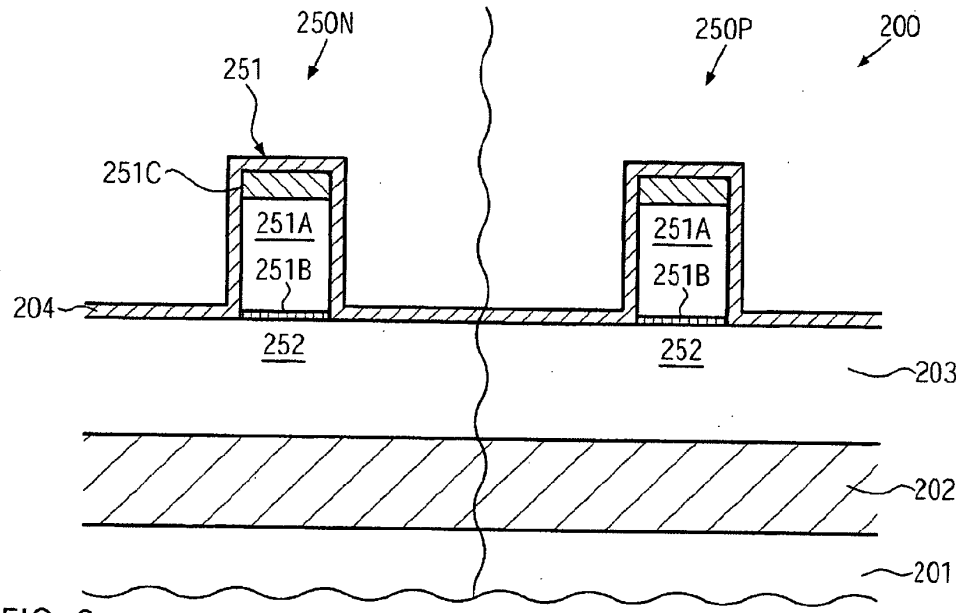


FIG. 2a

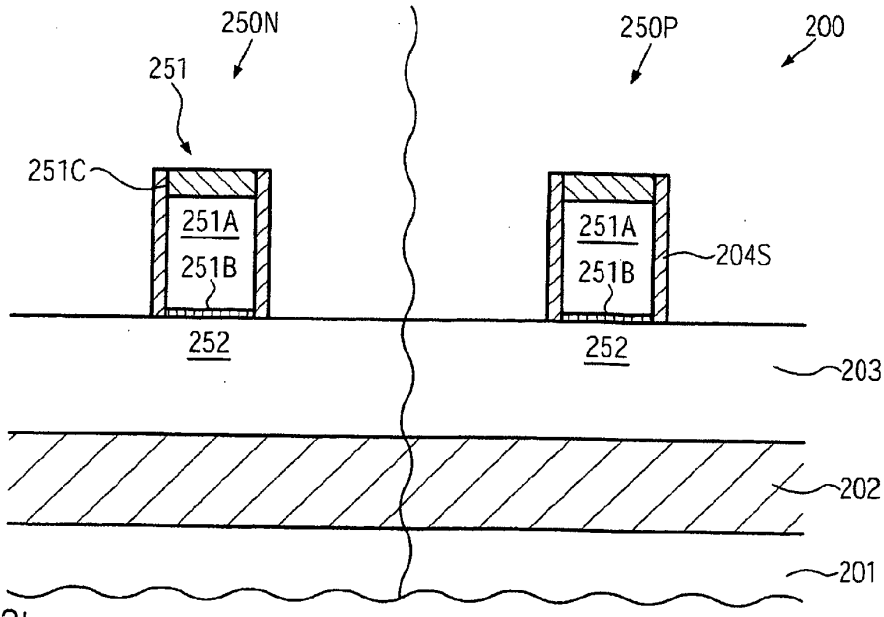


FIG. 2b

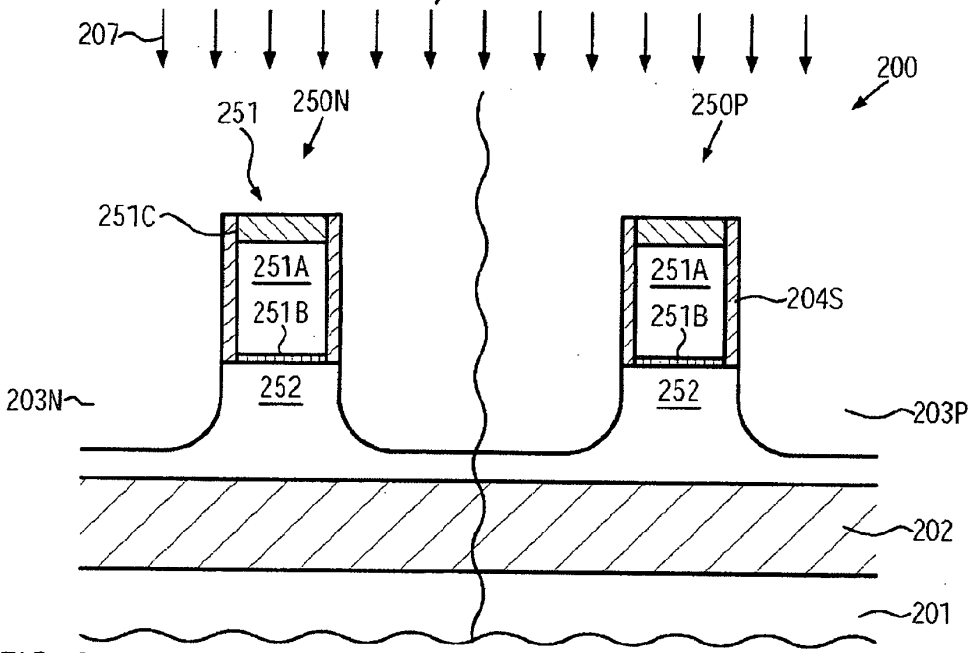

207
200
251
250N
250P
251C
251A
251B
252
204S
203N
203P
202
201

FIG. 2c

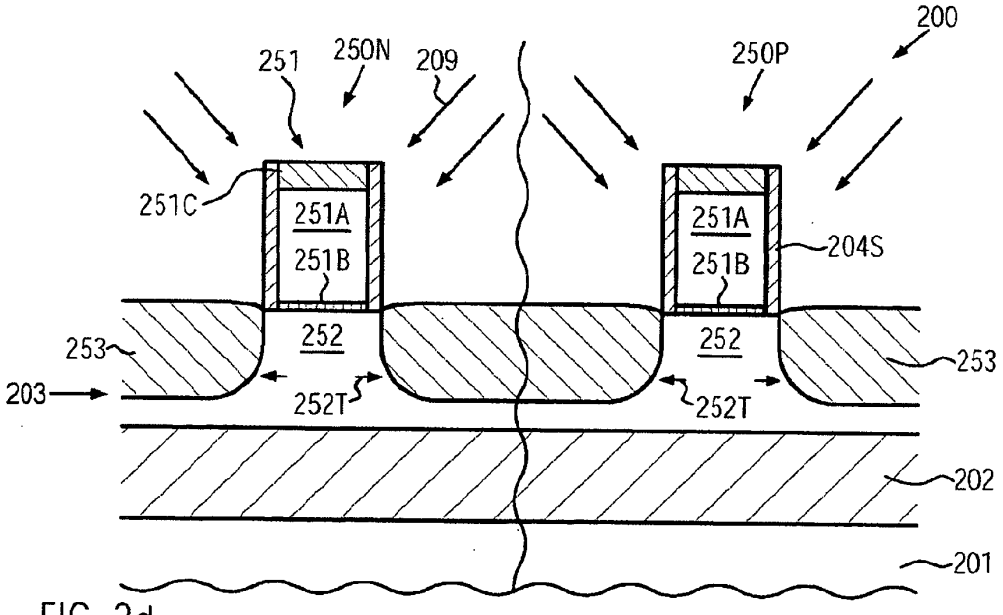

200
251
250N
209
250P
251C
251A
251B
252
204S
253
203
252T
202
201

FIG. 2d

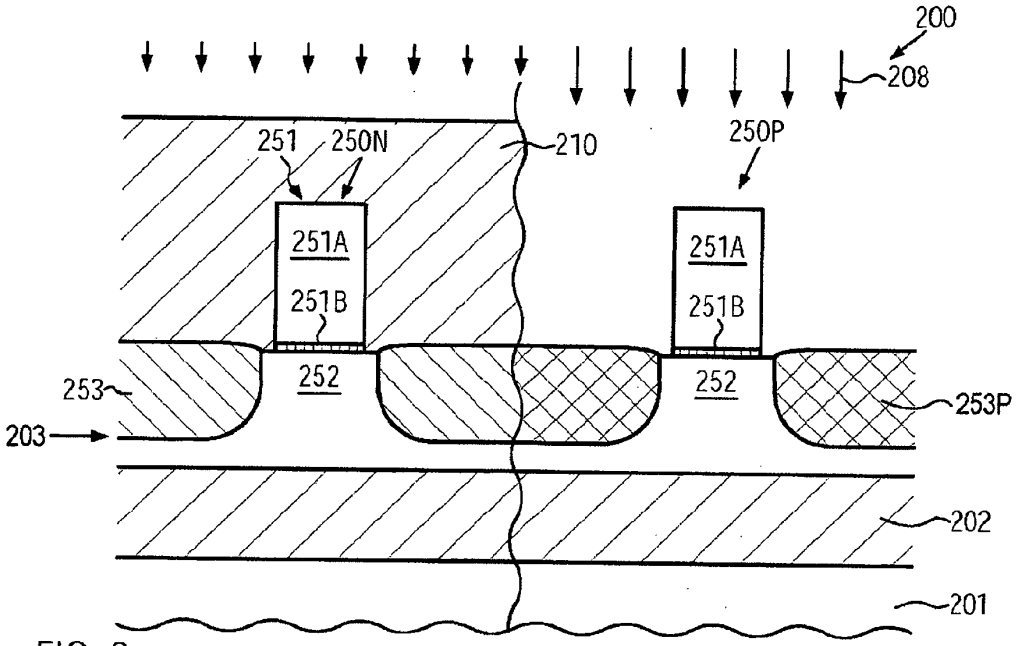

200
208
251
250N
210
250P
251A
251B
252
253
253P
203
202
201

FIG. 2e

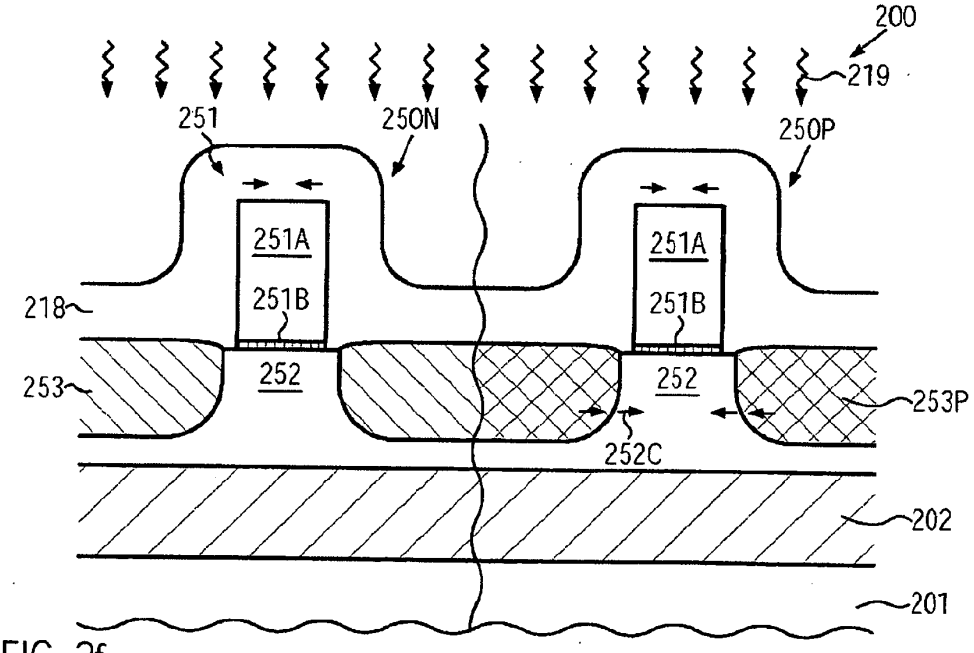

200
219
251
250N
250P
251A
251B
218
252
253
253P
252C
202
201

FIG. 2f

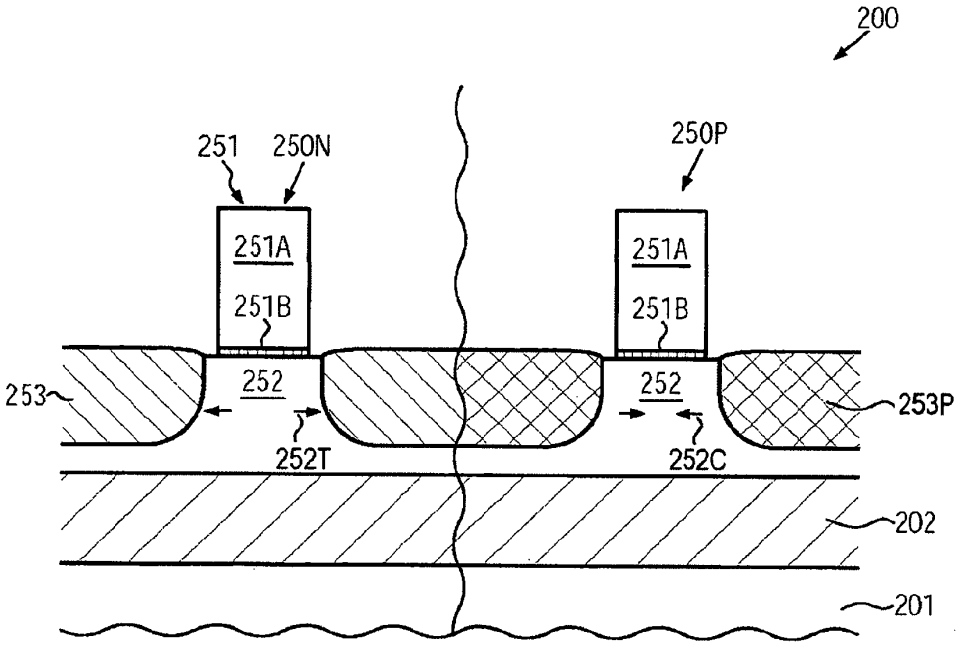

200
251
250N
250P
251A
251B
252
253
253P
252T
252C
202
201

FIG. 2g

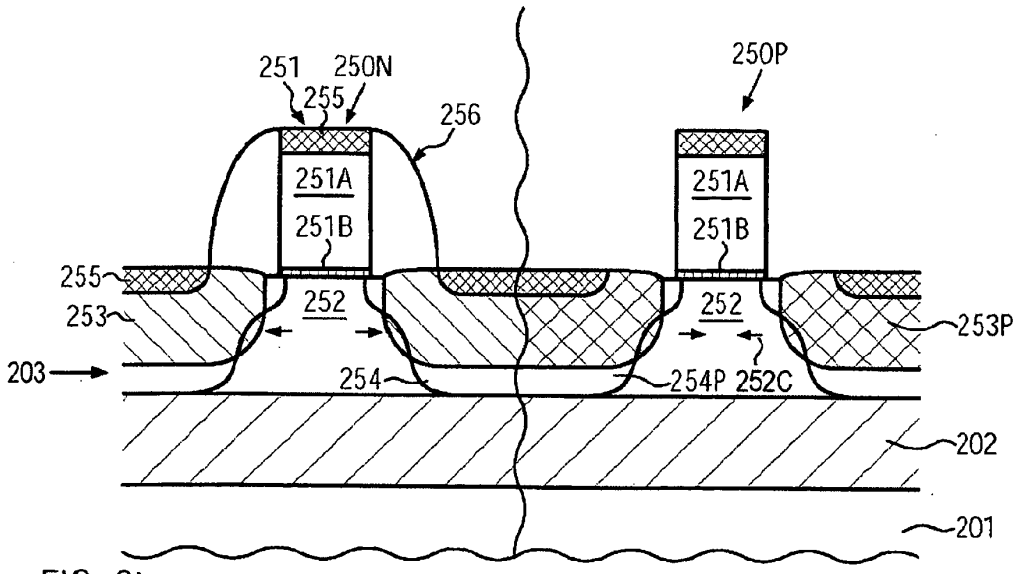

251
250N
255
256
250P
251A
251B
252
253
253P
255
203
254
254P
252C
202
201

FIG. 2h

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/004417

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/8238 H01L21/336 H01L21/265 H01L29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2008/166841 A1 (HSIEH CHAO-CHING [TW]) 10 July 2008 (2008-07-10) paragraphs [0017] - [0025]; figures 5-12	1,10 2-9
Y	US 2002/072176 A1 (PARK HEEMYONG [US] ET AL) 13 June 2002 (2002-06-13) paragraphs [0027] - [0032]; figures 2-4	2-7
Y	US 2007/196991 A1 (NANDAKUMAR MAHALINGAM [US] ET AL) 23 August 2007 (2007-08-23) claim 1	8
Y	US 2007/228482 A1 (WEI ANDY [DE] ET AL) 4 October 2007 (2007-10-04) paragraph [0064]; figure 2h	9

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 September 2009	16/11/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ott, André

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2009/004417

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers allsearchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search reportcovers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-10

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Form PCT/ISA/210 (continuation of first sheet (2)) (April 2005)

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-10

A method of forming a strained semiconductor material in a first transistor of a first conductivity type and a second transistor of a second conductivity type, the method comprising: forming first cavities in drain and source areas of said first transistor; forming a first strained semiconductor material in said first cavities; forming second cavities in drain and source areas of said second transistor; and forming a second strained semiconductor material in said second cavities, said first and second strained semiconductor materials having a different material composition.

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2. claims: 11-15

A method of forming a strained semiconductor material in a first transistor of a first conductivity type and a second transistor of a second conductivity type, the method comprising: forming first cavities in drain and source areas of said first transistor; forming second cavities in drain and source areas of said second transistor; and forming a semiconductor material having a first type of strain in said first and second cavities; creating lattice damage in said semiconductor material selectively in said fist transistor to form a relaxed semiconductor material; and re-crystallizing said relaxed semiconductor material in a strained state, said strained state corresponding to a second type of strain that is opposite to said first tape of strain.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/004417

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008166841 A1	10-07-2008	NONE	
US 2002072176 A1	13-06-2002	NONE	
US 2007196991 A1	23-08-2007	NONE	
US 2007228482 A1	04-10-2007	CN 101416287 A	22-04-2009
		DE 102006015077 A1	11-10-2007
		JP 2009532861 T	10-09-2009
		KR 20090007388 A	16-01-2009

Form PCT/ISA/210 (patent family annex) (April 2005)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
14 July 2011 (14.07.2011)

PCT

(10) International Publication Number
WO 2011/084262 A2

(51) International Patent Classification:
H01L 21/336 (2006.01) *H01L 29/78* (2006.01)

(21) International Application Number:
PCT/US2010/058199

(22) International Filing Date:
29 November 2010 (29.11.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/643,912 21 December 2009 (21.12.2009) US

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, MS: RNB-4-150, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **MURTHY, Anand S.** [US/US]; 10934 NW Lucerne CT, Portland, Oregon 97229 (US). **AUBERTINE, Daniel Bourne** [US/US]; 11145 NW Timeric St, North Plains, Oregon 97133 (US). **GHANI, Tahir** [US/US]; 15523 NW Andalusian Way, Portland, Oregon 97229 (US). **PETHE, Abhijit Jayant** [IN/US]; 2848 NW Moda Way, Hillsboro, Oregon 97124 (US).

(74) Agents: **VINCENT, Lester J.** et al.; BLAKELY SOKOLOFF TAYLOR & ZAFMAN, 1279 Oakmead Parkway, Sunnyvale, California 94085 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) Title: SEMICONDUCTOR DEVICE HAVING DOPED EPITAXIAL REGION AND ITS METHODS OF FABRICATION

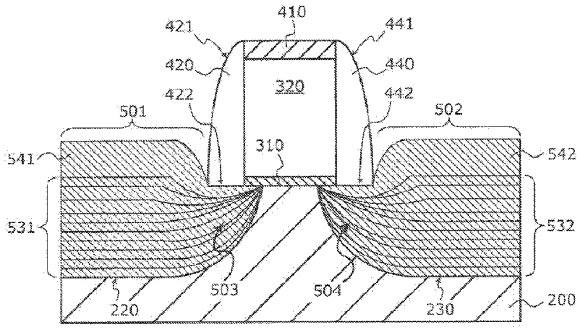


FIGURE 1

(57) Abstract: Embodiments of the present invention describe a epitaxial region on a semiconductor device. In one embodiment, the epitaxial region is deposited onto a substrate via cyclical deposition-etch process. Cavities created underneath the spacer during the cyclical deposition-etch process are backfilled by an epitaxial cap layer. The epitaxial region and epitaxial cap layer improves electron mobility at the channel region, reduces short channel effects and decreases parasitic resistance.

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SEMICONDUCTOR DEVICE HAVING DOPED EPITAXIAL REGION AND ITS METHODS OF FABRICATION

BACKGROUND

1. FIELD

The present invention relates to the field of semiconductor processing and more particularly to a semiconductor device having doped epitaxial regions and its methods of fabrication.

2. DISCUSSION OF RELATED ART

Increasing the performance of semiconductor devices, in particular transistors, has always been a major consideration in the semiconductor industry. For example, during the design and fabrication of metal oxide semiconductor field effect transistors (MOSFETs), it has always been a common goal to increase the electron mobility of the channel region and to reduce the parasitic resistance to improve device performance.

Other methods of improving device performance include, for example, reducing the overall resistance of the MOSFET by doping the region between the source/drain regions and the channel region, which is referred to as the 'tip' or source/drain extension regions of the MOSFET. For example, a dopant is implanted in the source/drain regions and an annealing step diffuses the dopant towards the channel region. However, there are limits to controlling the dopant concentration and location. Furthermore, the implant and diffusion method does not address the issues of lateral undercut or parasitic resistance at the tip regions.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view that illustrates a semiconductor device in accordance with one embodiment of the present invention.

Figure 2 is a cross-sectional view that illustrates a semiconductor device in accordance with another embodiment of the present invention.

Figure 3 is a cross-sectional view that illustrates a semiconductor device in accordance with another embodiment of the present invention.

Figure 4 is a perspective view that illustrates a semiconductor device in accordance with another embodiment of the present invention.

Figures 5A – 5F are cross-sectional views that illustrate the method of fabricating

the semiconductor device shown in Figure 1.

Figures 6A – 6F are cross-sectional views that illustrate the method of fabricating the semiconductor device shown in Figure 2.

Figures 7A – 7C are cross-sectional views that illustrate the method of fabricating the semiconductor device shown in Figure 3.

Figures 8A – 8I are perspective views that illustrate the method of fabricating the semiconductor device shown in Figure 4.

Figures 9 – 15 are cross-sectional views of the semiconductor device shown in Figures 8E – 8I.

Figure 8E' is a perspective view that illustrates an alternative embodiment of the semiconductor device shown in Figure 8E.

Figure 9' is a perspective view that illustrates an alternative embodiment of the semiconductor device shown in Figure 9.

DETAILED DESCRIPTION

A semiconductor device having doped epitaxial regions and its method of fabrication are described. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. In other instances, well known semiconductor processing techniques and features have not been described in particular detail in order not to unnecessarily obscure the present invention.

Embodiments of the present invention describe a method of forming epitaxial regions on a semiconductor device. In one embodiment, the epitaxial region is an in-situ carbon and phosphorus doped silicon ($Si_y(C,P)_{1-y}$) region deposited via cyclical deposition-etch process. Cavities created underneath the spacer during the cyclical deposition-etch process are backfilled by a very highly phosphorus doped silicon (Si_yP_{1-y}) epitaxial cap layer. The fabrication of the epitaxial region and cap layer stack in a Self-aligned Epi Tip (SET) architecture provides a dramatic transistor performance gain due to combined effects of increased electron mobility gain at channel region, reduced short channel effects (due to carbon suppressing phosphorus diffusion), and reduced parasitic resistance provided by very high phosphorus doping in the (Si_yP_{1-y}) epitaxial cap layer.

Figure 1 illustrates a cross-sectional view of a semiconductor device in accordance with one embodiment of the present invention. The semiconductor device comprises a substrate 200 made of a semiconductor material such as, but not limited to,

monocrystalline silicon. In one embodiment, the substrate 200 is the silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate comprising silicon, silicon germanium, germanium, III-V compound semiconductors.

A gate dielectric 310 is formed over a channel region of the substrate 200. In one embodiment, the dielectric layer 310 is made from any well known insulative material, such as but not limited to silicon oxide (e.g., SiO_2). In another embodiment, the dielectric layer 310 is made of a high-k dielectric material having a substantially higher dielectric constant than silicon dioxide (i.e. $k > 3.9$). Examples of high-k dielectric materials include but are not limited to tantalum oxide (Ta_2O_5), titanium oxide (TiO_2) and hafnium oxide (HfO_2).

A gate electrode 320 is formed over the gate dielectric 310. In one embodiment, the gate electrode 320 is made of any well known materials, such as but not limited to polysilicon. In other embodiments, the gate electrode 320 is made of a metal or metal alloy material such as, but not limited to, platinum, tungsten or titanium.

In one embodiment, a hard mask 410 is formed on top of the gate electrode 320. In one embodiment, hard mask 410 is made of a material such as but not limited to silicon nitride or silicon oxynitride. Spacers 420, 440 are formed on opposite sidewalls of the gate electrode 320. In one embodiment, spacers 420, 440 are formed along the entire sidewall width of the gate electrode 320. Spacers 420, 440 comprise sidewalls 421, 441, and bottom surfaces 422, 442. In one embodiment, the spacers 420, 440 are made of a material such as but not limited to a silicon nitride, silicon dioxide or silicon oxynitride.

In an embodiment of the present invention, a recessed source interface 220 and a recessed drain interface 230 are formed on the substrate 200 at opposite sides of the gate electrode 320. In one embodiment, a portion of the recessed source interface 220 extends laterally beneath the bottom surface 422 of the spacer 420 and beneath a portion of the gate electrode 320. Similarly, a portion of the recessed drain interface 230 extends laterally beneath the bottom surface 442 of the spacer 440 and beneath a portion of the gate electrode 320.

A source region 501 is formed over the recessed source interface 220. In an embodiment of the present invention, the source region 501 comprises an epitaxial region 531 formed over the recessed source interface 220. A cap layer 541 is formed over the epitaxial region 531. The source region 501 comprises a source epi-tip region 503 that includes portions of the epitaxial region 531 and cap layer 541 formed directly beneath the spacer 420 and gate dielectric 310.

A drain region 502 is formed over the recessed drain interface 230. In one embodiment, the drain region 502 comprises an epitaxial region 532 formed over the recessed drain interface 230. A cap layer 542 is formed over the epitaxial region 532. The drain region 502 comprises a drain epi-tip region 504 that includes portions of the epitaxial region 532 and cap layer 542 formed directly beneath the spacer 440 and gate dielectric 310. By forming the source and drain epi-tip regions 503, 504 in relatively close proximity to the channel region, a larger hydrostatic stress is induced on the channel region, resulting in higher electron mobility and increasing drive current.

In an embodiment of the present invention, the epitaxial regions 531, 532 comprise silicon and carbon doped with phosphorus. In this case, the semiconductor device shown in Figure 1 is a NMOS planar or trigate transistor with a Self-aligned Epi Tip (SET) architecture. In one embodiment, the epitaxial regions 531, 532 comprise silicon having a carbon concentration of about 0.5 atomic % to 4 atomic % and a phosphorus concentration of about 9E19 cm^{-3} to 3E21 cm^{-3}. In a specific embodiment, the epitaxial regions 531, 532 comprise silicon having a carbon concentration of 2.2 atomic % and a phosphorus concentration of 2E20 cm^{-3}. The substitutional carbon (over 2 atomic %) in the epitaxial regions 531, 532 of the source and drain regions 501, 502 impart hydrostatic stress on the channel region, which enhances electron mobility. Furthermore, the substitutional carbon suppresses any phosphorus diffusion during any subsequent thermal anneals, thus reducing short channel effects.

In an embodiment of the present invention, the cap layers 541, 542 are epitaxial layers comprising silicon doped with phosphorus. In one embodiment, the cap layers 541, 542 comprise silicon having a phosphorus concentration of about 8E19 cm^{-3} to 3E21 cm^{-3}. In a specific embodiment, the cap layers 541, 542 comprise silicon having a phosphorus concentration of 2E21 cm^{-3}. The high phosphorus concentration level in the cap layers 541, 542 reduces parasitic resistance, particularly in contact resistance between salicide and source/drain regions 501, 502.

Figure 2 illustrates a cross-sectional view of a semiconductor device similar to Figure 1. The substrate 200 is made of {001} silicon, and comprises a recessed source interface 240 having a {111} facet 241 in the {111} crystallographic plane of the {001} silicon substrate 200, and a recessed drain interface 250 having a {111} facet 251 in the {111} crystallographic plane of the {001} silicon substrate 200. The {111} facets 241, 251 provide reduced volume in depletion and corresponding improved control of short channel effects. In one embodiment, the recessed source and drain interfaces 240, 250

each further comprises a {010} facet 242, 252 in the {010} crystallographic plane of the {001} silicon substrate 200, where the {010} facets 242, 252 extend directly beneath the gate electrode 320. The {010} facets 242, 252 contribute to more precisely defining the metallurgical channel length of the semiconductor device and reduce short channel effects.

Similar to Figure 1, the semiconductor device shown in Figure 2 comprises a source region 501 and a drain region 502, each having an epitaxial region 531, 532 and a cap layer 541, 542. Epitaxial regions 531, 532 and cap layers 541, 542 are formed over the recessed source and drain interfaces 240, 250 including their {111} facets 241, 251 and {010} facets 242, 252. The source region 501 comprises a source epi-tip region 505 that includes portions of the epitaxial region 531 and cap layer 541 surrounded by the spacer 420, the gate dielectric 310 and the {111}, {010} facets 241, 242. The drain region 502 comprises a drain epi-tip region 506 that includes portions of the epitaxial region 532 and cap layer 541 surrounded by the spacer 440, the gate dielectric 310 and the {111}, {010} facets 251, 252. Forming the source and drain epi-tip regions 505, 506 in relatively close proximity to the channel region induces a larger hydrostatic stress on the channel region, thus increasing electron mobility which results in higher drive current.

Figure 3 illustrates a cross-sectional view of a semiconductor device similar to Figure 2. In one embodiment, the source and drain regions 501, 502 each comprises an epitaxial layer 610, 620 formed over the recessed source and drain interfaces 240, 250 including their {111} facets 241, 251 and {010} facets 242, 252.

The source region 501 comprises a source epi-tip region 611 that includes portions of the epitaxial layer 610 surrounded by the spacer 420, the gate dielectric 310 and the {111}, {010} facets 241, 242. The drain region comprises a drain epi-tip region 621 that includes portions of the epitaxial layer 610 surrounded by the spacer 440, the gate dielectric 310 and the {111}, {010} facets 251, 252. Forming the source and drain epi-tip regions 611, 621 in relatively close proximity to the channel region induces a larger hydrostatic stress on the channel region, thus increasing electron mobility which results in higher drive current.

In an embodiment of the present invention, the epitaxial layer 610, 620 comprises silicon doped with phosphorus. In one embodiment, the epitaxial layers 610, 620 comprise silicon having a phosphorus concentration of about 8E19 cm^{-3} to 3E21 cm^{-3}. In a specific embodiment, the epitaxial layers 610, 620 comprise silicon having a phosphorus concentration of 2E21 cm^{-3}. The high phosphorus concentration level in the epitaxial layers 610, 620 reduces parasitic resistance, particularly in contact resistance between

salicide and source/drain regions 501, 502.

Figures 1, 2 and 3 illustrate the application of epitaxial regions in planar transistors to enhance electron mobility at the channel region or to reduce contact resistance at the source/drain regions. It can be appreciated that the epitaxial regions are not limited to planar transistors but can be fabricated on other devices, such as but not limited to a tri-gate transistor. Figure 4 illustrates a perspective view of a tri-gate device comprising a substrate 200 having a semiconductor body or fin 260 (represented by dashed lines). A gate electrode 340 is formed over 3 surfaces of the fin 260 to form 3 gates. A hard mask 410 is formed on top of the gate electrode 340. Gate spacers 460, 470 are formed at opposite sidewalls of the gate electrode 340. The source region comprises the epitaxial region 531 formed on a recessed source interface 266 and on a fin 260 sidewall. The cap layer 541 is deposited over the epitaxial region 531.

Figures 5A – 5F illustrate a method of forming the semiconductor device as discussed in relation to Figure 1. The fabrication of the semiconductor device begins by providing the substrate 200 as shown in Figure 5A. The gate dielectric 310 is formed over a desired channel region of the substrate 200. In one embodiment, the gate dielectric 310 is formed by any well known methods, such as but not limited to physical vapor deposition (PVD), chemical vapor deposition (CVD) or atomic layer deposition (ALD).

The gate electrode 320 is formed over the gate dielectric 310. In an embodiment of the present invention, the gate electrode 320 is a sacrificial gate electrode that is subsequently replaced by an actual gate electrode in a replacement gate process. The hard mask 410 is formed on top of the gate electrode 320. In an embodiment of the present invention, gate electrode 320 and hard mask 410 are deposited using PVD or CVD, and then patterned using well known photolithography and etching techniques.

Spacers 420, 440 are then formed on opposite sidewalls of the gate electrode 320. Spacers 420, 440 comprises sidewalls 421, 441, and bottom surfaces 422, 442 that are formed on the top surface of the substrate 200. In one embodiment, the spacers 420, 440 are formed by using well known techniques, such as depositing a layer of spacer material over the entire substrate 200 including the gate electrode 320, and then anisotropically etching the layer of spacer material to form the spacers 420, 440 on the sidewalls of gate electrode 320.

Next, a source region and a drain region are formed on the substrate 200. In an embodiment of the present invention, fabrication of the source and drain regions begins by recessing portions of the substrate 200 using well known etching techniques, such as but

not limited to dry etching or wet etching. In an embodiment of the present invention, a wet etching comprising an etchant chemistry that is substantially selective to the substrate 200 is utilized to recess the substrate 200 so as to form a recessed source interface 220 and a recessed drain interface 230 as shown in Figure 5B.

In one embodiment, the wet etching undercuts the spacers 420, 440 and forms a source epi-tip cavity 271 between the bottom surface 422 of spacer 420 and the recessed source interface 220, and forms a drain epi-tip cavity 272 between the bottom surface of spacer 440 and the recessed drain interface 230. As a result, the source epi-tip cavity 271 and drain epi-tip cavity 272 expose the bottom surfaces 422, 442 of the spacers 420, 440. In one embodiment, the source epi-tip cavity 271 and drain epi-tip cavity 272 also expose portions of the gate dielectric 310. As a result, a portion of the recessed source interface 220 extends laterally beneath the spacer 420 and beneath a portion of the gate electrode 320. Similarly, a portion of the recessed drain interface 230 extends laterally beneath the spacer 440 and beneath a portion of the gate electrode 320.

It can be appreciated that the wet etching can be controlled (e.g. by adjusting the etching duration) so that the source and drain epi-tip cavities 271, 272 do not expose the gate dielectric 310. For instance, the recessed source interface 220 only extends laterally beneath the spacer 420, and the recessed drain interface 230 only extends laterally beneath the spacer 440.

In an embodiment of the present invention, the recessed source and drain interfaces 220, 230 define the channel region of the semiconductor device. The channel region refers to the portion of the substrate 200 located directly beneath the gate dielectric 310 and between the recessed source and drain interfaces 220, 230.

Next, an epitaxial region is deposited over each of the recessed source and drain interfaces 220, 230 by alternatingly exposing the substrate 200 to a first precursor and a second precursor. Fabrication of the epitaxial region begins, in Figure 5C, by exposing the entire substrate 200 to the first precursor so as to deposit epitaxial films 511, 512 on the recessed source and drain interfaces 220, 230. In the case where the substrate 200 is made of monocrystalline silicon, the recessed source and drain interfaces 220, 230 are monocrystalline surfaces that allow epitaxial growth of the epitaxial films 511, 512 thereon. On the other hand, the hard mask 410, the spacers 420, 440, and the gate dielectric 310 are non-crystalline surfaces. As a result, an amorphous layer 513 is deposited on the top surface of the hard mask 410, on the sidewalls 421, 441 and bottom surfaces 422, 442 of the spacers 420, 440, and on portions of the bottom surface of the

gate dielectric 310.

In an embodiment of the present invention, the first precursor comprises a silicon-containing compound, a carbon-containing compound, and a dopant. In one embodiment, the silicon-containing compound includes, but not limited to, silanes and halogenated silanes. Such silicon-containing compound includes silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), and penta-chloro silane.

In one embodiment, the carbon-containing compound includes, but not limited to, organosilanes. For example, the carbon-containing compound comprises mono-methyl silane (CH_3-SiH_3). In one embodiment, the carbon-containing compound is mixed with hydrogen (H_2) or argon. For example, mono-methyl silane (CH_3-SiH_3) is mixed with hydrogen (H_2) or argon with the CH_3-SiH_3 concentration in the range of 0.5% to 20%.

In an embodiment of the present invention, the dopant is a n-type dopant such as, but not limited to, phosphorus or arsenic. In one embodiment, the Phosphorus dopant is incorporated in the epitaxial film using phosphine (PH_3) without any dilution in Hydrogen or an inert gas, such as N_2 or Ar. In another embodiment, the phosphine gas is mixed with hydrogen, for example as a mixture of 3% phosphine (PH_3) in hydrogen (H_2).

In one embodiment, the first precursor is delivered or released onto the substrate 200 with a carrier gas. In one embodiment, the carrier gas includes, but is not limited, to hydrogen (H_2), or any inert gas such as nitrogen (N_2) argon and helium and any combinations thereof.

In an embodiment of the present invention, the substrate 200 is exposed to the first precursor at a temperature of about 500 to 700 degrees Celsius, at a pressure of about 5 to 300 torr, and for a time duration of about 3 to 60 seconds. In a specific embodiment, the substrate 200 is exposed to the first precursor at a temperature of 600 degrees Celsius, at a pressure of 30 torr, and for a time duration of 15 seconds.

In one embodiment, the epitaxial films 511, 512 are grown to have a thickness of about 6 to 100 Angstroms. In a specific embodiment, the epitaxial films 511, 512 are grown to have a thickness of 50 Angstroms. In the case where the first precursor uses a phosphorus dopant, the deposited epitaxial films 511, 512 are crystalline films containing silicon and carbon doped with phosphorus (i.e. in-situ carbon and phosphorus doped silicon layer). The amorphous layer 513 contains silicon and carbon doped with phosphorus.

An optional surface pre-treatment can be performed on the substrate 200 before exposing it to the first precursor to facilitate epitaxial growth and reduce surface defects.

In an embodiment of the present invention, the surface pre-treatment includes a hydrogen bake treatment performed on the substrate 200 (in Figure 5B) to clean the recessed source and drain interfaces 220, 230. The hydrogen bake treatment desorbs oxygen and renders surface reconstruction so that the epitaxial films 511, 512 can readily nucleate without formation of defects. In one embodiment, the hydrogen bake treatment is performed at around 700 to 1050 degrees Celsius for a duration of about 10 to 120 seconds. In an embodiment of the present invention, hydrogen chloride (HCl) is added to the hydrogen bake treatment. The hydrogen chloride (HCl) enables removal of about 1 to 3 monolayers of the recessed source and drain interfaces 220, 230 so that they are free of oxygen, hydrocarbons and any other contaminants. In one embodiment, the hydrogen bake treatment with hydrogen chloride (HCl) is performed at a lower temperature of around 700 to 900 degrees Celsius for a duration of about 10 to 120 seconds. Alternatively, chlorine (Cl_2), germane (GeH_4) or phosphine (PH_3) can be used as an additional or alternative chemical compound for hydrogen chloride (HCl).

In an alternative embodiment, the surface pre-treatment utilizes an etch step to clean the recessed source and drain interfaces 220, 230. In one embodiment, the etch step uses an etchant gas, such as but not limited to hydrogen (H_2), anhydrous hydrochloric acid (HCl), or a mixture of germane (GeH_4) and hydrogen (H_2). In another embodiment, the surface pre-treatment uses a combination of the etch step and the hydrogen bake treatment.

Before exposing the substrate 200 to the second precursor, a purging process can be performed to remove the first precursor and other by-products from the substrate 200. In one embodiment, the purging process injects an inert gas, such as but not limited to nitrogen (N_2), helium or argon to remove any unreacted first precursor or by-products.

Next, in Figure 5D, the entire substrate 200 is exposed to the second precursor to remove the amorphous layer 513 from the sidewalls 421, 441 and bottom surfaces 422, 442 of the spacers 420 , 440. Furthermore, the second precursor also removes any amorphous layer 513 formed on the hard mask 410 and beneath the gate dielectric 310. In one embodiment, the second precursor 900 uses an etchant chemistry that etches the amorphous layer 513 faster than the epitaxial films 511, 512. In one embodiment, the second precursor 900 is an etchant gas, such as but not limited to hydrogen (H_2), anhydrous hydrochloric acid (HCl), and a mixture of germane (GeH_4) and hydrogen (H_2). Germane (GeH_4) enables etch through catalysis, thus providing high etch rate at low temperatures.

In one embodiment, the substrate 200 is exposed to the second precursor at a

pressure of about 30 to 300 torr, and for a time duration of about 5 to 60 seconds. In a specific embodiment, the substrate 200 is exposed to the second precursor at a pressure of 80 torr, and for a time duration of 20 seconds. In one embodiment, the temperature is maintained at substantially the same level when exposing the substrate 200 to both the first precursor and the second precursor.

Due to the weak chemical bonding between the amorphous layer 513 and the hard mask 410, spacers 420, 440 and gate dielectric 310, the second precursor easily removes the amorphous layer 513 deposited thereon. The second precursor reacts with the amorphous layer 513 to convert it into by-products, thus removing the amorphous layer 513 from the hard mask 410, spacers 420, 440 and gate dielectric 310.

On the other hand, the epitaxial films 511, 512 have strong chemical bonds with the recessed source and drain interfaces 220, 230. Due to the strong chemical bonds, only small portions of the epitaxial films 511, 512 are removed by the second precursor. In one embodiment, the thickness of the epitaxial films 511, 512 deposited during Figure 5C or the duration of exposing the second precursor to the substrate 200 in Figure 5D can be adjusted so as to effectively remove the amorphous layer 513 while maintaining sufficient thickness for the epitaxial films 511, 512.

Figures 5C and 5D illustrate one deposition-etch cycle of forming the epitaxial films 511, 512 over the recessed source and drain interfaces 220, 230. In one embodiment, the deposition-etch cycle is repeated using the same type of first and second precursors until a desired number of epitaxial films are deposited. For example, Figure 5E shows epitaxial regions 531, 532 containing ten epitaxial films each.

It can be appreciated that the epitaxial regions 531, 532 are not limited to only ten layers of epitaxial films each. In one embodiment, about 3 to 100 deposition-etch cycles are performed to form the epitaxial regions 531, 532. In a specific embodiment, 30 deposition-etch cycles are performed to form the epitaxial regions 531, 532 having a thickness of around 30 nanometers.

In an embodiment of the present invention, the epitaxial regions 531, 532 are deposited with a graded concentration of carbon or phosphorus. The carbon and phosphorus concentration of each epitaxial film deposition can be optimized to provide optimal selectivity and defect-free epitaxy. Furthermore, the graded carbon or phosphorus concentration promotes the removal of the amorphous material during the deposition-etch cycles. In one embodiment, the graded carbon concentration of the epitaxial regions 531, 532 (shown in Figure 5E) begins at around 0.5 atomic % for the lowest epitaxial film and

is gradually increased to a desired level of about 2 atomic % in the uppermost epitaxial film. In another embodiment, the graded phosphorus concentration level of the epitaxial regions 531, 532 begins at around 8E19 cm^{-3} for the lowest epitaxial film and is gradually increased to a desired level of around 2E21 cm^{-3} in the uppermost epitaxial film. In one embodiment, the epitaxial regions 531, 532 are deposited with a combination of graded carbon concentration (0.5 - 2 atomic %) and graded phosphorus concentration (8E19 - 2E21 cm^{-3}).

The epitaxial regions 531, 532 are selectively formed over the recessed source and drain interfaces 220, 230 as shown in Figure 5E. However, the removal of the amorphous layer 513 during each deposition-etch cycle results in voids or cavities 281,282 formed between the bottom surfaces 422, 442 of spacers 420, 440 and the top surfaces of the epitaxial regions 531, 532. In one embodiment, the cavities 281, 282 also extend between portions of the gate dielectric 310 and the epitaxial regions 531, 532. The cavities 281, 282 may cause detrimental effects on the transistor performance, and thus need to be eliminated. In an embodiment of the present invention, the cavities 281, 282 are substantially backfilled by cap layers 541, 542 selectively deposited over the epitaxial regions 531, 532 as shown in Figure 5F.

In an embodiment of the present invention, the cap layers 541, 542 are selectively deposited over the epitaxial regions 531, 532 in a single deposition process by exposing the substrate 200 to a third precursor. In one embodiment, the third precursor comprises the same silicon-containing compound and dopant of the first precursor, and the same etchant gas of the second precursor.

In the case where the epitaxial regions 531, 532 are crystalline films having silicon and carbon doped with phosphorus, the third precursor uses the same phosphorus dopant to form cap layers 541, 542. The crystalline surfaces of the epitaxial layers 531, 532 allow epitaxial growth of cap layers 541, 542 thereon, and as a result, the cap layers 541, 542 are epitaxial layers containing silicon doped with phosphorus. Apart from backfilling the cavities, the phosphorus doped silicon cap layers 541, 542 provides an advantage of inducing tensile stress on the channel region, thereby increasing electron mobility and improving the device performance.

In one embodiment, a co-flown deposition technique is used to expose the substrate 200 to the silicon-containing compound, the dopant, and the etchant gas at the same time. In one embodiment, the etchant gas does not include germane (GeH_4). During deposition, the etchant gas easily removes any silicon and phosphorus-containing

compound that are weakly bonded on the hard mask 410 and spacers 420, 440 so that the cap layers 541, 542 are deposited over the epitaxial regions 531, 532 and not deposited on the hard mask 410 or the spacers 420, 440.

In an embodiment of the present invention, the substrate 200 is exposed to the third precursor at a temperature of about 550 to 800 degrees Celsius, at a pressure of about 10 torr to atmospheric pressure, and for a time duration of about 30 to 900 seconds. In a specific embodiment, the substrate 200 is exposed to the first precursor at a temperature of 635 degrees Celsius, at a pressure of 600 torr, and for a time duration of 180 seconds.

In one embodiment, the cap layers 541, 542 are grown to have a thickness of about 50 to 500 Angstroms. In a specific embodiment, the cap layers 541, 542 are grown to have a thickness of 300 Angstroms.

Portions of the epitaxial region 531 and cap layer 541 directly beneath the spacer 420 and gate dielectric 310 forms the source epi-tip region 503. Similarly, portions of the epitaxial region 532 and cap layer 542 directly beneath the spacer 440 and gate dielectric 310 forms the drain epi-tip region 504. By forming the source and drain epi-tip regions 503, 504 in relatively close proximity to the channel region, a larger hydrostatic stress is induced on the channel region, resulting in higher electron mobility and increasing drive current. The stress can be further amplified by increasing the carbon concentrations of the source and drain epi-tip regions 503, 504 during fabrication of the epitaxial regions 531, 532. Furthermore, the carbon concentrations of the source and drain epi-tip regions 503,504 also help to suppress any phosphorus diffusion during subsequent thermal anneals.

In an embodiment of the present invention, the gate electrode 320 is a sacrificial gate electrode that is subsequently replaced by an actual gate electrode in a replacement gate process. In one embodiment, the replacement gate process begins by depositing a mask on the cap layers 541, 542 and then planarizing the mask to be coplanar with the hard mask 410 (not shown). Next, the hard mask 410 and gate electrode 320 are removed using well known etching techniques. After removing the hard mask 410 and gate electrode 320, the actual gate electrode is then deposited on the gate dielectric 310. In one embodiment, the actual gate electrode is a metal gate electrode comprising materials such as, but not limited to, platinum, tungsten or titanium. This completes the fabrication of the semiconductor device shown in Figure 1.

Figures 6A – 6F illustrate a method of forming the semiconductor device as discussed in relation to Figure 2. The fabrication of the semiconductor device begins by

providing the substrate 200 as shown in Figure 6A. The semiconductor device shown in Figure 6A is the same as Figure 5A, and thus will not be discussed in detail. Briefly, the semiconductor device comprises the gate dielectric 310 formed over a desired channel region of the substrate 200. The gate electrode 320 is formed over the gate dielectric 310. In an embodiment of the present invention, the gate electrode 320 is a sacrificial gate electrode that is subsequently replaced by an actual gate electrode in a replacement gate process. Hard mask 410 is formed on top of the gate electrode and spacers 420, 440 are formed at the sidewalls of the gate electrode 320.

Next, a source region and a drain region are formed on the substrate 200. In an embodiment of the present invention, fabrication of the source and drain regions begins by recessing portions of the substrate 200 using well known etching techniques, such as but not limited to dry etching or wet etching. In an embodiment of the present invention, a wet etching that is substantially selective to the substrate 200 is utilized to recess the substrate 200 so as to form a recessed source interface 240 and a recessed drain interface 250 as shown in Figure 6B.

In an embodiment of the present invention, the substrate 200 is made of {001} silicon. The wet etch uses an etchant chemistry that etches the {001} silicon substrate 200 based on crystallographic direction, and in particular etches the {001} silicon substrate 200 much more slowly along its {111} crystallographic plane to form the {111} facets 241, 251 as the etch proceeds much more rapidly in other crystallographic directions. As a result, a source epi-tip cavity 271 is formed between the bottom surface 422 of spacer 420 and the {111} facet 241. A drain epi-tip cavity 272 is formed between the bottom surface of spacer 440 and the {111} facet 251.

The wet etch chemistry includes, but not limited to, an ammonia-based or amine-based etchant. Examples of ammonia-based etchants are ammonium hydroxide (NH4OH), tetramethylammonium hydroxide (TMAH) and benzyltrimethylammonium hydroxide (BTMH). The wet etch chemistry includes other types of etchants, such as potassium hydroxide (KOH) and sodium hydroxide (NaOH).

In one embodiment, the wet etch further creates {010} facets 242, 252 in the channel region of the {001} silicon substrate 200. The {010} facets 242, 252 extends directly beneath the gate dielectric 310. In a specific embodiment, {010} facets 242, 252 are formed up to a length of around 3 nanometers from the gate dielectric 310.

Next, an epitaxial region is deposited over each of the recessed source and drain interfaces 240, 250 by alternatingly exposing the substrate 200 to a first precursor and a

second precursor. The method of fabricating the epitaxial region, as illustrated in Figures 6C, 6D and 6E, is similar to the methods of fabrication discussed in Figures 5C, 5D and 5E. Before exposing the substrate 200 to the first precursor, an optional surface pre-treatment can be performed on the substrate 200 to facilitate epitaxial growth and reduce surface defects. In one embodiment, the surface pre-treatment comprises a hydrogen bake treatment and/or etching step as previously discussed in Figure 5C to clean the recessed source and drain interfaces 240, 250.

Beginning from Figure 6C, the entire substrate 200 is exposed to the first precursor so at to deposit epitaxial films 511, 512 on the recessed source and drain interfaces 240, 250. The recessed source and drain interfaces 240, 250, including their {111} facets 241, 251 and {010} facets 242, 252, are monocrystalline surfaces that allow epitaxial growth of the epitaxial films 511, 512 thereon. On the other hand, the hard mask 410, the spacers 420, 440, and the gate dielectric 310 are non-crystalline surfaces, and thus the amorphous layer 513 is deposited thereon. The same first precursor and process conditions, as discussed in relation to Figure 5C, are applicable here and will not be discussed.

Next, in Figure 6D, the entire substrate 200 is similarly exposed to the second precursor to remove the amorphous layer 513 from the sidewalls 421, 441 and bottom surfaces 422, 442 of the spacers 420 , 440. Furthermore, the second precursor also removes any amorphous layer 513 formed on the hard mask 410 and beneath the gate dielectric 310. The same second precursor and process conditions, as discussed in relation to Figure 5D, are applicable here and will not be discussed.

Figures 6C and 6D illustrate one deposition-etch cycle of forming the epitaxial films 511, 512 over the recessed source and drain interfaces 240, 250 including their {111} facets 241, 251 and {010} facets 242, 252. The deposition-etch cycle is repeated until a desired number of epitaxial films are deposited. For illustration purposes, Figure 6E shows epitaxial regions 531, 532 containing ten epitaxial films each. In an embodiment of the present invention, the epitaxial regions 531, 532 are deposited with a graded concentration of carbon or phosphorus as previously described in Figure 5E. For example, the epitaxial regions 531, 532 (shown in Figure 6E) are deposited with a graded carbon concentration of around 0.5 atomic % for the lowest epitaxial film and are gradually increased to a desired level of about 2 atomic % for the uppermost epitaxial film. Alternatively, the epitaxial regions 531, 532 are deposited with a graded phosphorus concentration level of around 8E19 cm^{-3} for the lowest epitaxial film and are gradually increased to a desired level of around 2E21 cm^{-3} for the uppermost epitaxial film. In one

embodiment, the epitaxial regions 531, 532 are deposited with a combination of graded carbon concentration (0.5 - 2 atomic %) and graded phosphorus concentration (8E19 - 2E21 cm^{-3}).

The removal of the amorphous layer 513 during each deposition-etch cycle similarly results in cavities 281,282 formed between the bottom surfaces 422, 442 of spacers 420, 440 and the top surfaces of the epitaxial regions 531, 532. The cavities 281, 282 are substantially backfilled by the cap layers 541, 542 selectively deposited over the epitaxial regions 531, 532 as shown in Figure 6F.

In one embodiment, the cap layers 541, 542 are selectively deposited over the epitaxial regions 531, 532 in a single deposition process by exposing the substrate 200 to a third precursor. The same third precursor and process conditions, as discussed in relation to Figure 5F, are applicable here. In the case where the epitaxial regions 531, 532 are crystalline films having silicon and carbon doped with phosphorus, the third precursor uses the same phosphorus dopant to form cap layers 541, 542. The crystalline surfaces of the epitaxial regions 531, 532 allow epitaxial growth of cap layers 541, 542 thereon, and as a result, the cap layers 541, 542 are epitaxial layers containing silicon doped with phosphorus. This completes the fabrication of the semiconductor device shown in Figure 2.

Figures 7A – 7C illustrate a method of forming the semiconductor device as discussed in relation to Figure 3. Beginning from Figure 7A, the fabrication of the semiconductor device begins by providing the substrate 200. The semiconductor device shown in Figure 7A is the same as Figure 5A, and thus will not be discussed here.

Next, a source region and a drain region are formed on the substrate 200. In an embodiment of the present invention, fabrication of the source and drain regions begins by recessing portions of the substrate 200 using well known etching techniques, such as but not limited to dry etching or wet etching. In one embodiment, the wet etching used in Figure 6B is similarly applied here to recess the substrate 200 so as to form a recessed source interface 240 and a recessed drain interface 250, as shown in Figure 7B. The wet etch uses the same etchant chemistry as described in relation to Figure 6B to form {111} facets 241, 251 in the {111} crystallographic plane of the {001} silicon substrate 200. In one embodiment, the wet etch further creates {010} facets 242, 252 in the channel region of the {001} silicon substrate 200.

Next, epitaxial layers 610, 620 are selectively deposited over the recessed source and drain interfaces 240, 250 as shown in Figure 7C. In an embodiment of the present

invention, the epitaxial layers 610, 620 are selectively deposited in a single deposition process by exposing the substrate 200 to a precursor comprising an etchant gas.

In one embodiment, the precursor comprises the silicon-containing compound and dopant similarly described in Figure 5C. In one embodiment, the silicon-containing compound includes, but not limited to, silanes and halogenated silanes. Such silicon-containing compound includes silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), and penta-chloro silane. In an embodiment of the present invention, the dopant is a n-type dopant such as, but not limited to, phosphorus or arsenic. In one embodiment, the phosphorus dopant is introduced into the epitaxial layers using phosphine (PH_3) without any dilution in Hydrogen or an inert gas, such as N_2 or Ar. In another embodiment, the phosphine gas is mixed with hydrogen, for example as a mixture of 3% phosphine (PH_3) in hydrogen (H_2). In one embodiment, the etchant gas of the precursor includes, but is not limited to hydrogen (H_2) and anhydrous hydrochloric acid (HCl).

In one embodiment, a co-flown deposition technique is used to deliver the precursor, including the etchant gas to the substrate 200 at the same time. In one embodiment, the substrate 200 is exposed to the precursor at a temperature of about 550 to 800 degrees Celsius, at a pressure of about 10 torr to atmospheric pressure, and for a time duration of about 30 to 2000 seconds. In a specific embodiment, the substrate 200 is exposed to the first precursor at a temperature of 635 degrees Celsius, at a pressure of 600 torr, and for a time duration of 800 seconds.

In one embodiment, the epitaxial layers 610, 620 are grown to have a thickness of about 30 to 2000 Angstroms. In a specific embodiment, the epitaxial layers 610, 620 are grown to have a thickness of 750 Angstroms. In the case where a phosphorus dopant is used, the epitaxial layers 610, 620 comprise silicon doped with phosphorus.

In the case where the substrate 200 is made of monocrystalline silicon, the recessed source and drain interfaces 240, 250 including their {111} facets 241, 251 and {010} facets 242, 252 are monocrystalline surfaces that allow epitaxial growth of the epitaxial layers 610, 620 thereon. Since the hard mask 410 and spacers 420, 440 have non-crystalline surfaces, the etchant gas easily removes any silicon and phosphorus-containing compound that are weakly bonded on the hard mask 410 and spacers 420, 440 during deposition so that the epitaxial layers 610, 620 are deposited over the recessed source and drain interfaces 240, 250 and not deposited on the hard mask 410 or spacers 420, 440.

Portions of the epitaxial layer 610 deposited between the spacer 420 and {111}, {010} facets 241, 242 form the source epi-tip region 611. Similarly, portions of the epitaxial layer 620 deposited between the spacer 440 and {111}, {010} facets 251, 252 form the drain epi-tip region 621. By forming the source and drain epi-tip regions 611, 621 in relatively close proximity to the channel region, a larger hydrostatic stress is induced on the channel region, resulting in higher electron mobility. Furthermore, the phosphorus doped silicon epitaxial layers 610, 620 induces tensile stress on the channel region, thereby increasing electron mobility and improving the device performance. This completes the fabrication of the semiconductor device shown in Figure 3.

In addition, an optional surface pre-treatment can be performed on the substrate 200 before exposing it to the precursor to facilitate epitaxial growth and reduce surface defects. For example, a similar hydrogen bake treatment described in relation to Figure 5C is performed on the substrate 200 (in Figure 7B) to clean the recessed source and drain interfaces 240, 250 including theirs {111} facets 241, 251 and {010} facets 242, 252.

Figures 8A – 8I illustrate a method of forming the tri-gate device as discussed in relation to Figure 4. The fabrication of the tri-gate device begins by providing the substrate 200 as shown in Figure 8A. The substrate 200 comprises a semiconductor body or fin 260 extending from the substrate 200 through the isolation regions 710, 720. In one embodiment, the isolation regions 710, 720 are shallow trench isolation (STI) regions formed by common techniques, such as etching the substrate 200 to form trenches, and then depositing oxide material onto the trenches to form the STI regions. The isolation regions 710, 720 are made from any well known insulative material, such as but not limited to silicon oxide (e.g., SiO_2).

In one embodiment, the fin 260 comprises a top surface 261 above the isolation regions 700. The fin 260 further includes a front surface 262 exposed above the isolation region 710, and a back surface 263 exposed above the isolation region 720. In one embodiment, the fin 260 is made from the same semiconductor materials as the substrate 200.

Next, in Figure 8B, a gate dielectric 330 is formed over a portion of the top surface 261, the front surface 262 and the back surface 263. In one embodiment, the gate dielectric 330 is formed by any well known methods, such as but not limited to physical vapor deposition (PVD), chemical vapor deposition (CVD) or atomic layer deposition (ALD).

Then, a gate electrode 340 is formed over the gate dielectric 330, and exposing portions 264, 265 of the fin 260 at either sides of the gate electrode 340. In one

embodiment, the gate electrode 340 is made of any well known materials, such as but not limited to polysilicon. The gate electrode 340 formed over the top surface 261, the front surface 262 and the back surface 263 creates three gates for the tri-gate device. The hard mask 410 is then formed on top of the gate electrode 320.

Next, gate spacers 460, 470 are deposited on opposite sidewalls of the gate electrode 340 as shown in Figure 8C. In one embodiment, the spacers 460, 470 are formed by using well known techniques, such as depositing a layer of spacer material over the entire substrate 200 including the gate electrode 320, and then anisotropically etching the layer of spacer material to form the spacers 460, 470 on the sidewalls of gate electrode 340. At the same time, fin spacers 480, 490 are formed on the sidewalls of the exposed portions 264, 265 of the fin 260. In one embodiment, the gate spacers 460, 470 and fin spacers 480, 490 are made of a material such as but not limited to a silicon nitride, silicon dioxide or silicon oxynitride.

Next, a source region and a drain region are formed on the substrate 200. In an embodiment of the present invention, fabrication of the source and drain regions begins in Figure 8D by removing the fin spacers 480, 490 from the sidewalls of the exposed portions 264, 265 of the fin 260. The fin spacers 480, 490 are removed by well known etching techniques, such as but not limited to dry etching or wet etching.

In one embodiment, an anisotropic wet-etch is used to completely remove the fin spacers 480, 490 from the exposed portions 264, 265 of the fin 260. At the same time, the anisotropic wet-etch also removes portions of the gate spacers 460, 470, thus exposing portions of the hard mask 410 sidewalls. Since the gate spacers 460, 470 have a larger height and thickness than the fin spacers 480, 490, the anisotropic wet-etch removes the fin spacers 480, 490 faster than the gate spacers 460, 470. The anisotropic wet-etch can be controlled to completely remove the fin spacers 480, 490 but leaving sufficient thickness of the gate spacers 460, 470 on the gate electrode 340 so that the gate electrode 340 sidewalls are not exposed.

Next, an etching is performed on the substrate 200 to recess the exposed portions 264, 265 of the fin 260. In an embodiment of the present invention, the etching uses an etchant chemistry that is substantially selective to the fin 260 to recess the exposed portion 264 so as to form a recessed source interface 266 below the top surface of the isolation regions 710, 720, and to form a fin sidewall 267 as shown in Figure 8E. On the other side of the gate electrode 340, the exposed portion 264 is recessed to form a recessed drain interface 268 and a fin sidewall 269. In one embodiment, the recessed source and drain

interfaces 266, 268 are about 100 to 400 Angstroms below the top surface of the isolation regions 710, 720.

Figure 9 illustrates a cross-sectional view of the tri-gate device showing the fin sidewall 267 extending from the top surface 261to the recessed source interface 266, and the fin sidewall 269 extending from the top surface 261 to the recessed drain interface 268. In an embodiment of the present invention, the fin sidewalls 267, 269 are substantially coplanar or flushed with the gate spacers 460, 470 sidewalls 461, 471. In one embodiment, the fin sidewalls 267, 269 are {110} facets in the {110} crystallographic plane of the substrate 200, and the recessed source and drain interfaces 266, 268 are {100} facets in the {100} crystallographic plane of the substrate 200.

In an alternative embodiment, an isotropic etch is used to form fin sidewalls 267, 269 recessed within the gate spacers 460, 470. Figure 8E' is a perspective view of the tri-gate device showing the fin sidewall 267 recessed within the gate spacer 470. Figure 9' is a cross-sectional view showing both the fin sidewalls 267, 269 recessed beneath the gate spacer 460, 470. In one embodiment, the fin sidewalls 267, 269 are recessed until about 25 to 200 Angstroms from the gate spacer sidewalls 461, 471.

Continuing from Figure 8E, an epitaxial region is then deposited over each of the recessed source and drain interfaces 266, 268 by alternatingly exposing the substrate 200 to a first precursor and a second precursor. The method of fabricating the epitaxial region, as illustrated in Figures 8F, 8G and 8H, is similar to the methods of fabrication discussed in Figures 5C, 5D and 5E.

Beginning from Figure 8F, the entire substrate 200 is exposed to the first precursor so at to deposit an epitaxial film 511 on the recessed source interface 266 and fin sidewall 267. At the same time, an epitaxial film 512 is deposited on the recessed drain interface 268 and fin sidewall 269 as shown in cross-sectional view of Figure 10. The recessed source and drain interfaces 266, 268, and the fin sidewalls 267, 269, are monocrystalline surfaces that allow epitaxial growth of the epitaxial films 511, 512 thereon. On the other hand, the hard mask 410, the gate spacers 460, 470, and isolation regions 710, 720 are non-crystalline surfaces, and thus the amorphous layer 513 is formed thereon. The same first precursor and process conditions, as discussed in relation to Figure 5C, are applicable here and will not be discussed.

Next, in Figure 8G, the entire substrate 200 is similarly exposed to the second precursor to remove the amorphous layer 513 from the gate spacers 460, 470, and isolation regions 710, 720. Furthermore, the second precursor also removes any amorphous layer

513 formed on the hard mask 410. Figure 11 shows a cross-sectional view of the tri-gate device after the amorphous layer 513 has been removed. The same second precursor and process conditions, as discussed in relation to Figure 5D, are applicable here and will not be discussed.

Figures 8F-8G and Figures 10-11 illustrate one deposition-etch cycle of forming the epitaxial films 511, 512 over the recessed source and drain interfaces 266, 268 and the fin sidewalls 267, 269. The deposition-etch cycle is repeated until a desired number of epitaxial films are deposited. In one embodiment, the final epitaxial regions 531, 532 comprise five epitaxial films as shown in Figure 12. In an embodiment of the present invention, the epitaxial regions 531, 532 are deposited with a graded concentration of carbon or phosphorus as previously described in Figure 5E. For example, the epitaxial regions 531, 532 (shown in Figure 12) are deposited with a graded carbon concentration of around 0.5 atomic % for the lowest epitaxial film and are gradually increased to a desired level of about 2 atomic % for the uppermost epitaxial film. Alternatively, the epitaxial regions 531, 532 are deposited with a graded phosphorus concentration level of around 8E19 cm^{-3} for the lowest epitaxial film and are gradually increased to a desired level of around 2E21 cm^{-3} for the uppermost epitaxial film. In one embodiment, the epitaxial regions 531, 532 are deposited with a combination of graded carbon concentration (0.5 - 2 atomic %) and graded phosphorus concentration (8E19 - 2E21 cm^{-3})

In the alternative embodiment where the fin sidewalls 267, 269 are recessed within the gate spacers 460, 470, the epitaxial regions 531, 531 are formed in closer proximity to the channel region of the tri-gate device, thus inducing a higher amount of stress on the channel region.

The removal of the amorphous layer 513 during each deposition-etch cycle similarly results in voids or cavities 281,282 formed between the epitaxial regions 531, 532 and the isolation regions 710, 720 as shown in Figures 8H and 13. The cavities 281, 282 are substantially backfilled by the cap layers 541, 542 selectively deposited over the epitaxial regions 531, 532 as shown in Figures 8I, 14 and 15.

In one embodiment, the cap layers 541, 542 are selectively deposited over the epitaxial regions 531, 532 in a single deposition process by exposing the substrate 200 to a third precursor. The same third precursor and process conditions, as discussed in relation to Figure 5F, are applicable here. In the case where the epitaxial regions 531, 532 are crystalline films having silicon and carbon doped with phosphorus, the third precursor uses the same phosphorus dopant to form cap layers 541, 542. The crystalline surfaces of

the epitaxial regions 531, 532 allow epitaxial growth of cap layers 541, 542 thereon, and as a result, the cap layers 541, 542 are epitaxial layers containing silicon doped with phosphorus. The phosphorus doped silicon cap layers 541, 542 provide an advantage of inducing tensile stress on the channel region of the semiconductor fin 260, which increases the electron mobility and improves the device performance. This completes the fabrication of the semiconductor device shown in Figure 4.

Several embodiments of the invention have thus been described. However, those ordinarily skilled in the art will recognize that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims that follow.

IN THE CLAIMS

We claim:

1. A method of forming a semiconductor device comprising:

providing a substrate having a gate electrode, and a spacer formed on the sidewall of the gate electrode;

etching the substrate to form a recessed interface;

forming an epitaxial region over the recessed interface by alternatingly exposing the substrate to a first precursor and a second precursor; and

selectively depositing a cap layer over the epitaxial region.

2. The method of claim 1, wherein alternatingly exposing the substrate to the first precursor and the second precursor comprises:

exposing the substrate to the first precursor to

deposit an epitaxial film over the recessed interface, and

deposit an amorphous layer on the sidewall and bottom surface of the spacer; and

exposing the substrate to the second precursor to remove the amorphous layer from the sidewall and bottom surface of the spacer.

3. The method of claim 1, wherein the first precursor comprises

a silicon-containing compound comprising silane;

a carbon-containing compound comprising organsilane; and

a dopant comprising phosphorus.

4. The method of claim 3, wherein the epitaxial region comprises silicon and carbon doped with phosphorus.

5. The method of claim 1, wherein the second precursor is an etchant gas.

6. The method of claim 1,

wherein forming the epitaxial region over the recessed interface results in a void between the epitaxial region and the bottom surface of the spacer; and

wherein the cap layer backfills the void.

7. The method of claim 1, wherein the cap layer is selectively deposited over the epitaxial region by exposing the substrate to a third precursor, the third precursor comprising

a silicon-containing compound comprising silane;

a dopant comprising phosphorus; and

an etchant gas.

8. The method of claim 7, wherein the cap layer comprises silicon doped with phosphorus.

9. The method of claim 1, further comprising:

performing a hydrogen bake treatment on the substrate before alternatingly exposing the substrate to a first precursor and a second precursor.

10. The method of claim 1, wherein etching the substrate to form a recessed interface comprises:

performing a wet etch to form a {111} facet in the {111} crystallographic plane of the substrate.

11. The method of claim 10, wherein the wet etch forms a {010} facet in the {010} crystallographic plane of the substrate.

12. The method of claim 10, wherein the wet etch uses an etchant chemistry selected from the group consisting of potassium hydroxide (KOH), sodium hydroxide (NaOH), an ammonia-based etchant or an amine-based etchant.

13. A method of forming a semiconductor device comprising:

providing a substrate having a gate electrode, and a first spacer and a second spacer formed on opposite sidewalls of the gate electrode;

etching the substrate to form a recessed source interface and a recessed drain interface;

selectively depositing a first epitaxial layer over the recessed source interface and a

second epitaxial layer over the recessed drain interface by exposing the substrate to a precursor comprising an etchant gas.

14. The method of claim 13, wherein the precursor comprises
a silicon-containing compound comprising silane; and
a dopant comprising phosphorus.

15. The method of claim 14, wherein both the first and second epitaxial layers comprises silicon doped with phosphorus.

16. The method of claim 13, wherein etching the substrate to form a recessed source interface and a recessed drain interface comprises:
performing a wet etch to form a {111} facet in the {111} crystallographic plane of the substrate at the recessed source interface and the recessed drain interface.

17. The method of claim 16, wherein the wet etch forms a {010} facet in the {010} crystallographic plane of the substrate at the recessed source interface and the recessed drain interface.

18. The method of claim 16, wherein the wet etch uses an etchant chemistry selected from the group consisting of potassium hydroxide (KOH), sodium hydroxide (NaOH), an ammonia-based etchant or an amine-based etchant.

19. A method of forming a semiconductor device comprising:
providing a substrate having an insulation layer thereon, and a semiconductor body that extends from the substrate through the insulation layer;
forming a gate electrode over a portion of the semiconductor body, thereby defining an exposed portion of the semiconductor body;
depositing a gate spacer on a sidewall of the gate electrode;
etching the exposed portion of the semiconductor body to form
a first surface recessed below the top surface of the insulation layer, and
a second surface coplanar with the gate spacer;
forming an epitaxial region on the first surface and second surface by alternatingly exposing the substrate to a first precursor and a second precursor; and

selectively depositing a cap layer over the epitaxial region.

20. The method of claim 19, wherein depositing the gate spacer on the sidewall of the gate electrode comprises:

depositing body spacers on the sidewalls of the exposed portion of the semiconductor body.

21. The method of claim 20, further comprising:

removing the body spacers from the sidewalls of the exposed portion of the semiconductor body prior to etching the exposed portion of the semiconductor body.

22. The method of claim 19, further comprising:

etching the second surface so that the second surface is recessed within the gate spacer.

23. The method of claim 19,

wherein forming an epitaxial region on the first surface and second surface results in a void between the epitaxial region and the insulation layer; and

wherein the cap layer backfills the void.

24. The method of claim 19, wherein alternatingly exposing the substrate to the first precursor and the second precursor comprises:

exposing the substrate to the first precursor to

deposit an epitaxial film over the first surface and second surface, and

deposit an amorphous layer on the insulation layer and the gate spacer; and

exposing the substrate to the second precursor to remove the amorphous layer from the insulation layer and the gate spacer.

25. The method of claim 19, wherein the first precursor comprises

a silicon-containing compound comprising silane;

a carbon-containing compound comprising organsilane; and

a dopant comprising phosphorus.

26. The method of claim 25, wherein the epitaxial region comprises silicon and carbon

doped with phosphorus.

27. The method of claim 19, wherein the second precursor is an etchant gas.

28. The method of claim 19, wherein the cap layer is selectively deposited over the epitaxial region by exposing the substrate to a third precursor, the third precursor comprising

a silicon-containing compound comprising silane;

a dopant comprising phosphorus; and

an etchant gas.

29. The method of claim 28, wherein the cap layer comprises silicon doped with phosphorus.

30. A semiconductor device comprising:

a substrate comprising

a gate electrode formed over a channel region of the substrate, and

a recessed source interface and a recessed drain interface formed on the substrate at opposite sides of the gate electrode;

a first spacer and a second spacer formed on opposite sidewalls of the gate electrode, wherein a portion of the recessed source interface extends laterally beneath the bottom surface of the first spacer, and a portion of the recessed drain interface extends laterally beneath the bottom surface of the second spacer;

a source region comprising

a first epitaxial region formed over the recessed source interface, and

a first cap layer formed over the first epitaxial region, wherein a portion of the first cap layer is formed between the first epitaxial region and the bottom surface of the first spacer; and

a drain region comprising

a second epitaxial region formed over the recessed drain interface, and

a second cap layer formed over the second epitaxial region, wherein a portion of the second cap layer is formed between the second epitaxial region and the bottom surface of the second spacer.

31. The semiconductor device of claim 30, wherein the first and second epitaxial regions each comprises silicon and carbon doped with phosphorus.

32. The semiconductor device of claim 31, wherein the wherein the first and second epitaxial regions each comprises silicon having

a carbon concentration in the range of 0.5 atomic % to 4 atomic %, and

a phosphorus concentration in the range of 9E19 cm^{-3} to 3E21 cm^{-3} .

33. The semiconductor device of claim 31, wherein the first and second cap layers each comprises silicon doped with phosphorus.

34. The semiconductor device of claim 33, wherein the first and second cap layers each comprises silicon having a phosphorus concentration in the range of 8E19 cm^{-3} to 3E21 cm^{-3}.

35. A semiconductor device comprising:

a substrate having an insulation layer formed thereon;

a semiconductor body extending from the substrate through the insulation layer, wherein the semiconductor body comprises

a top surface, a front surface and a back surface exposed above the insulation layer,

a first sidewall extending from the top surface to a source interface, and

a second sidewall opposite the first sidewall, the second sidewall extending from the top surface to a drain interface;

a gate electrode formed over the top surface, the front surface and the back surface of the semiconductor body;

a first spacer and a second spacer formed on opposite sidewalls of the gate electrode;

a source region comprising

a first epitaxial region formed on the first sidewall and the source interface, and

a first cap layer formed over the first epitaxial region, wherein a portion of the first cap layer is formed between the first epitaxial region and the insulation layer; and

a drain region comprising

a second epitaxial region formed over the second sidewall and the drain interface, and

a second cap layer formed over the second epitaxial region, wherein a portion of the second cap layer is formed between the second epitaxial region and the insulation layer.

36. The semiconductor device of claim 35, wherein the first sidewall is substantially coplanar to the first spacer, and the second sidewall is coplanar to the second spacer.

37. The semiconductor device of claim 35, wherein the first sidewall is recessed within the first spacer, and the second sidewall is recessed within the second spacer.

38. The semiconductor device of claim 35, wherein the source interface and the drain interface are recessed below the top surface of the insulation layer.

39. The semiconductor device of claim 35, wherein the first and second epitaxial regions each comprises silicon and carbon doped with phosphorus.

40. The semiconductor device of claim 39, wherein the wherein the first and second epitaxial regions each comprises silicon having

a carbon concentration in the range of 0.5 atomic % to 4 atomic %, and

a phosphorus concentration in the range of 9E19 cm^{-3} to 3E21 cm^{-3} .

41. The semiconductor device of claim 35, wherein the first and second cap layers each comprises silicon doped with phosphorus.

42. The semiconductor device of claim 41, wherein the first and second cap layers each comprises silicon having a phosphorus concentration in the range of 8E19 cm^{-3} to 3E21 cm^{-3}.

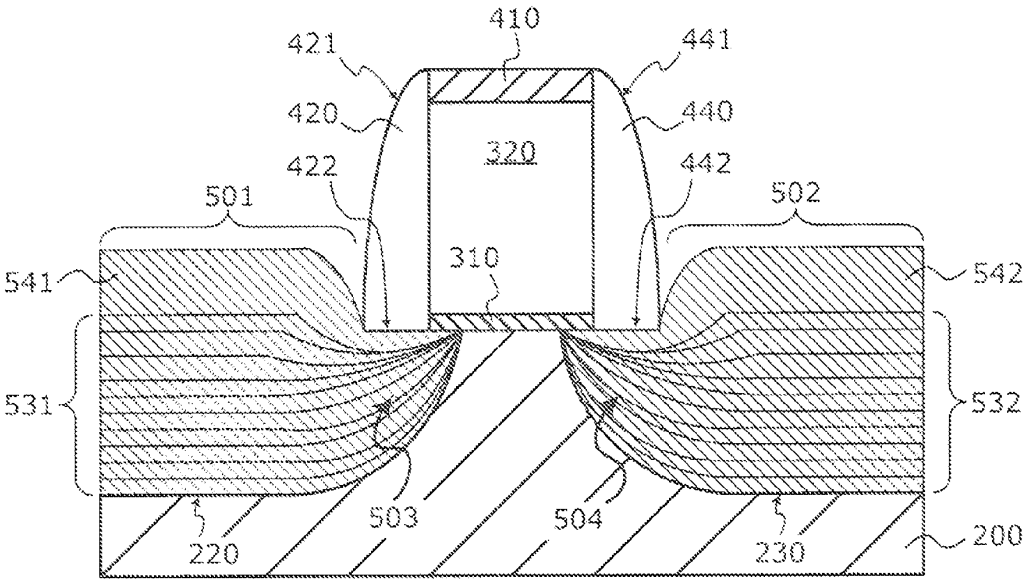

410
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200

FIGURE 1

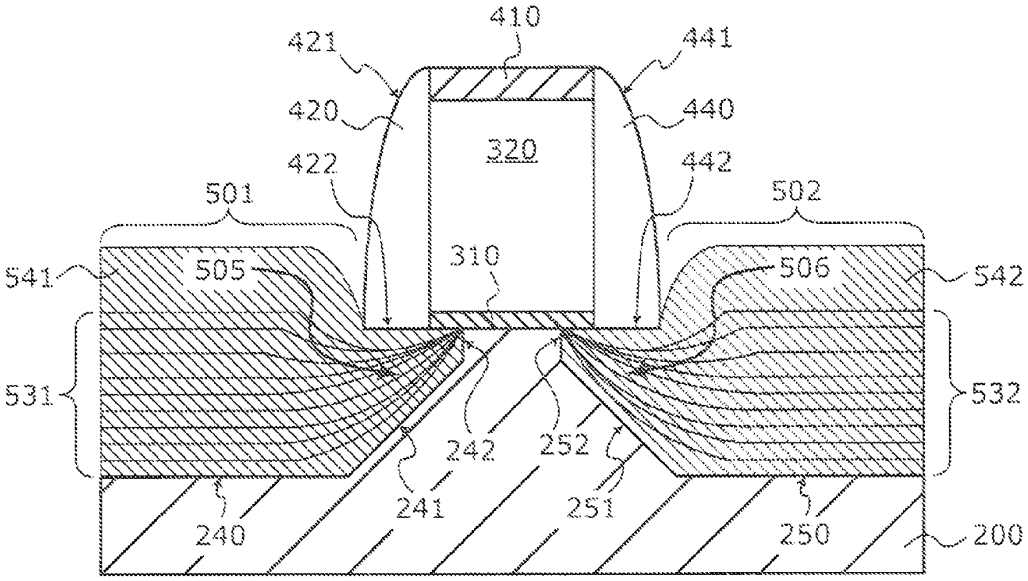


FIGURE 2

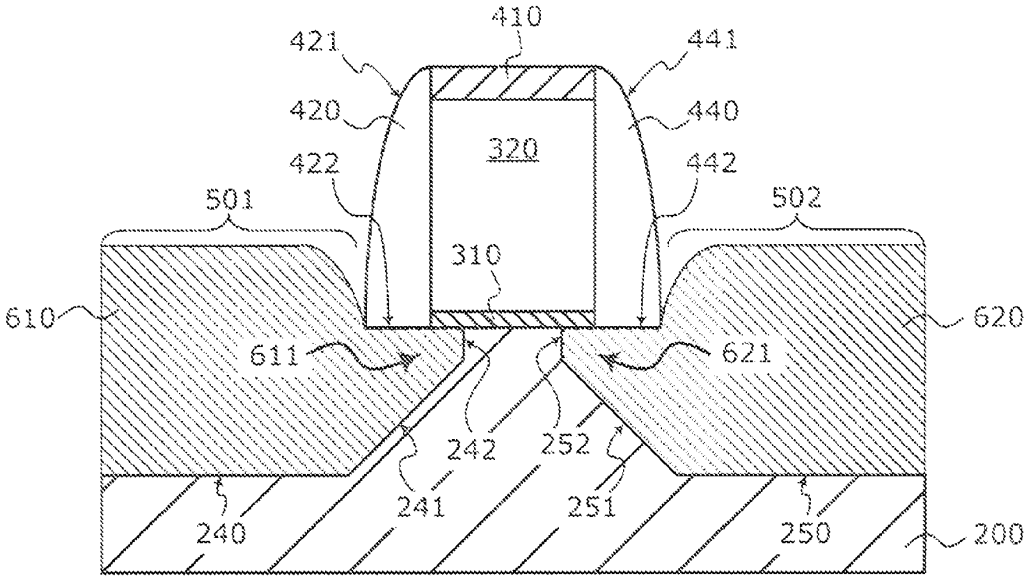


FIGURE 3

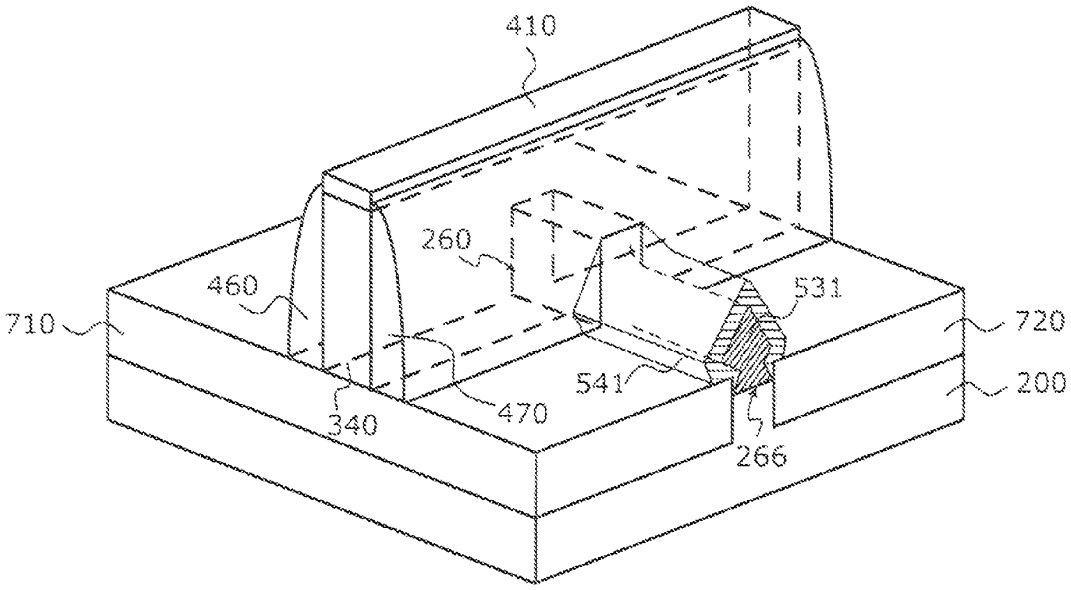


FIGURE 4

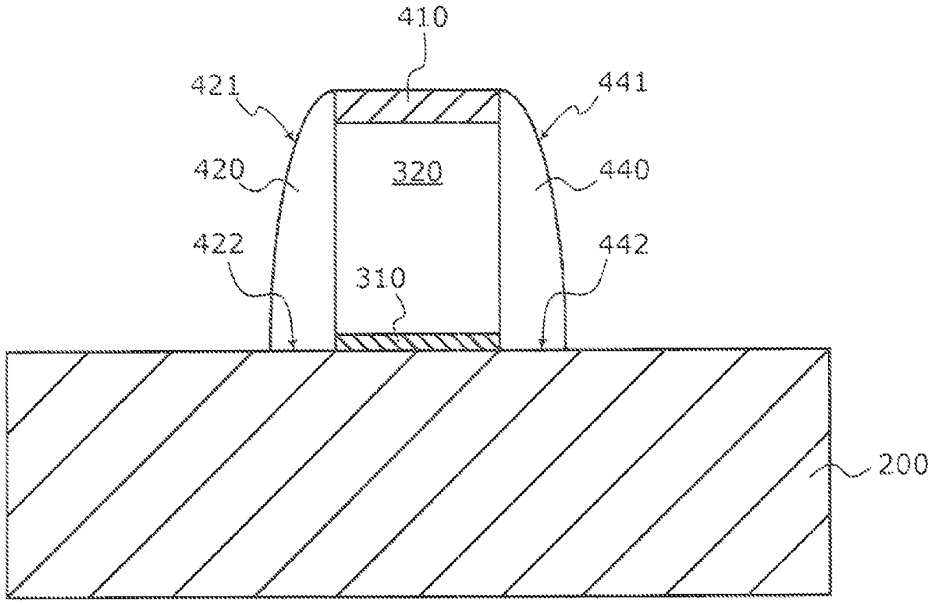


FIGURE 5A

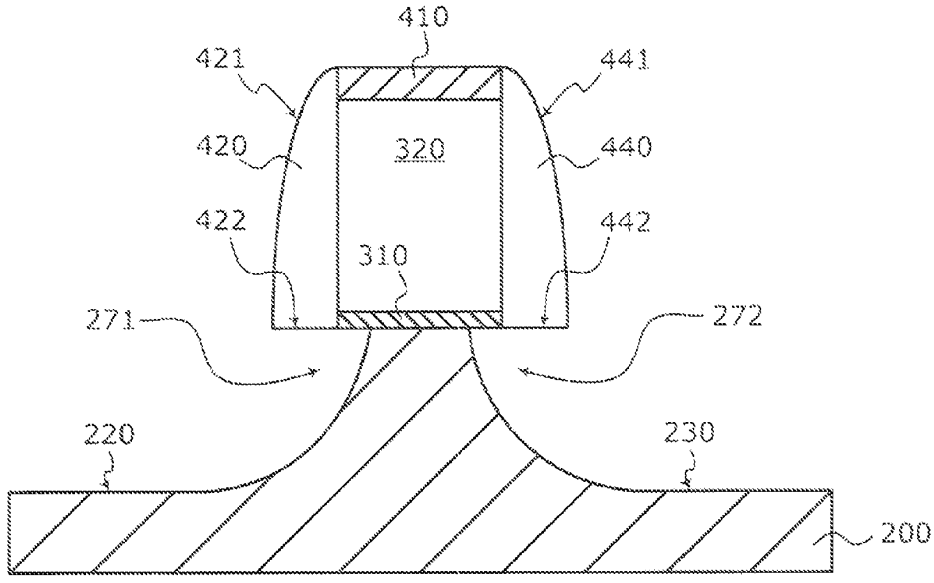


FIGURE 5B

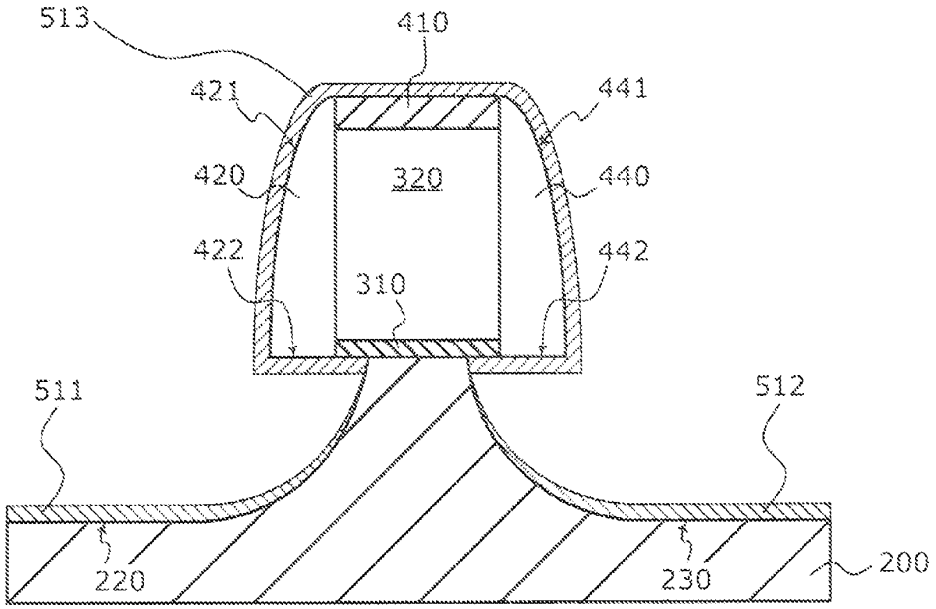


FIGURE 5C

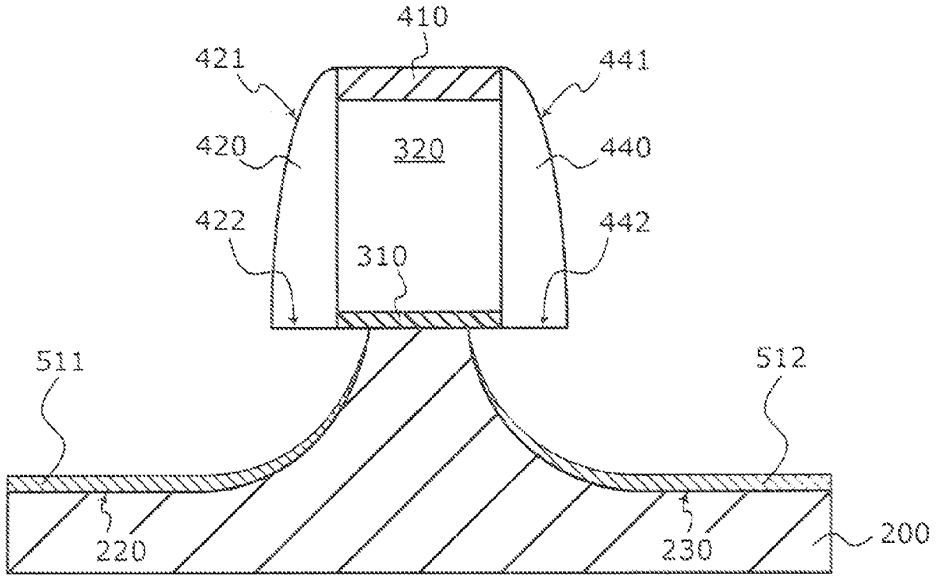


FIGURE 5D

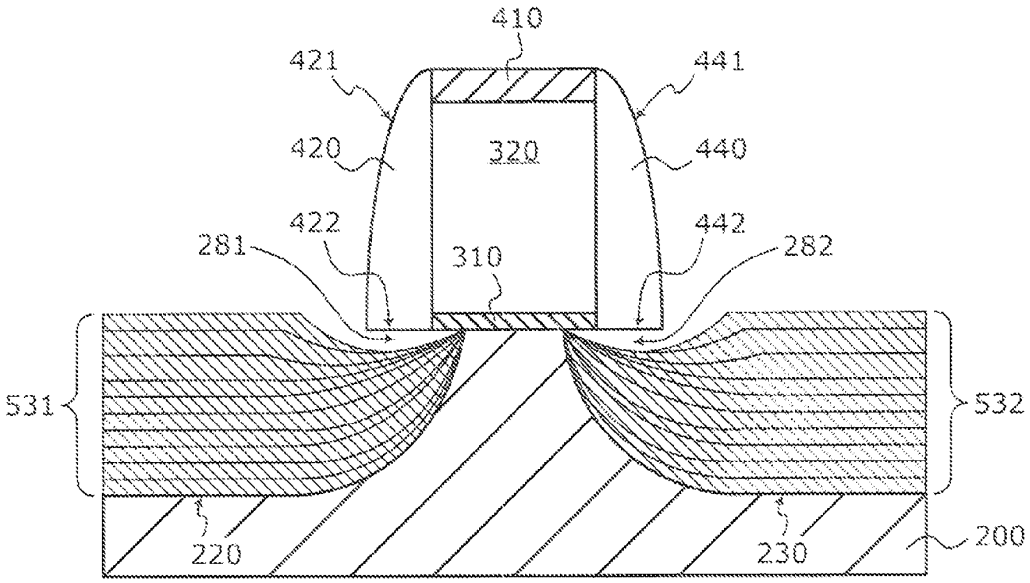


FIGURE 5E

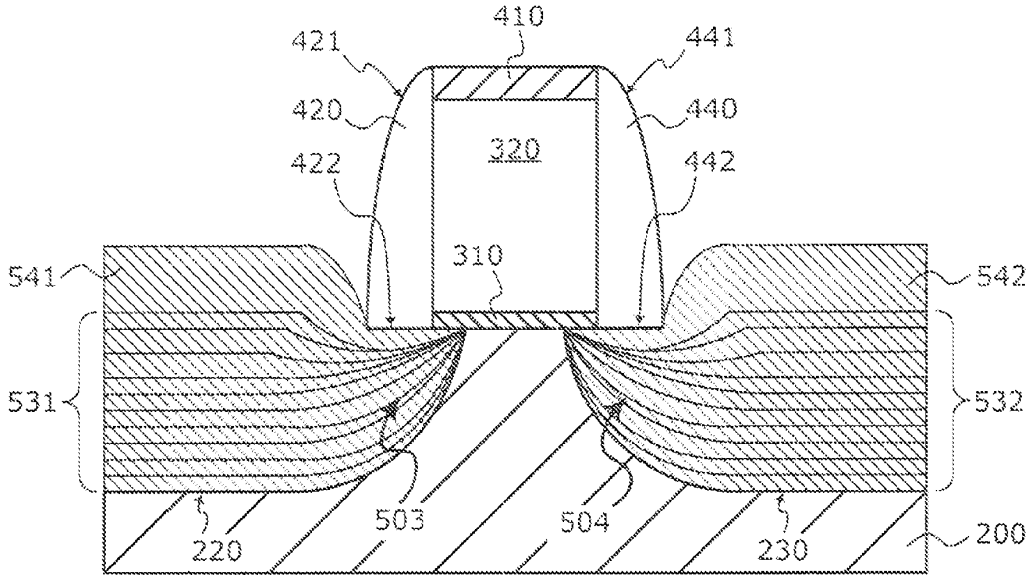


FIGURE 5F

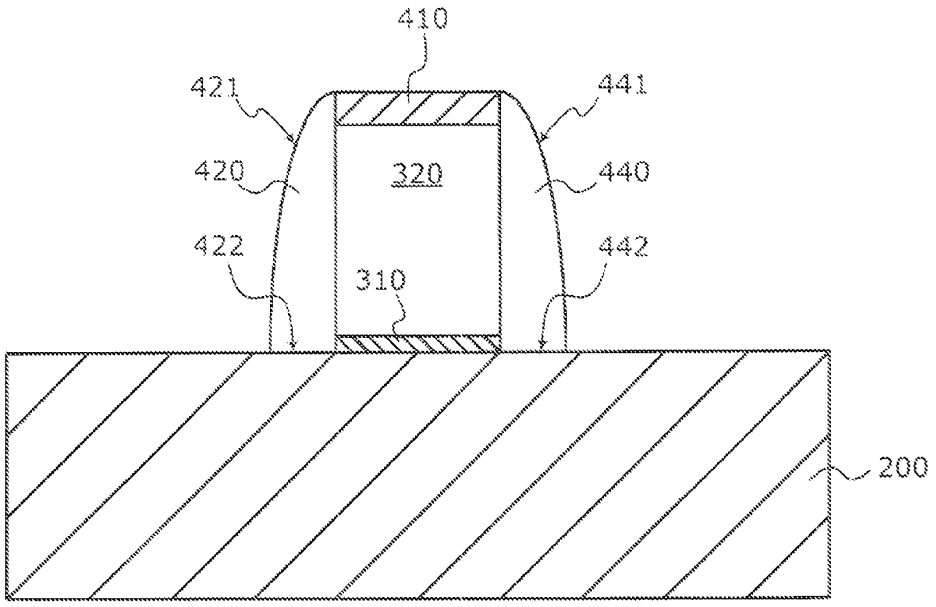


FIGURE 6A

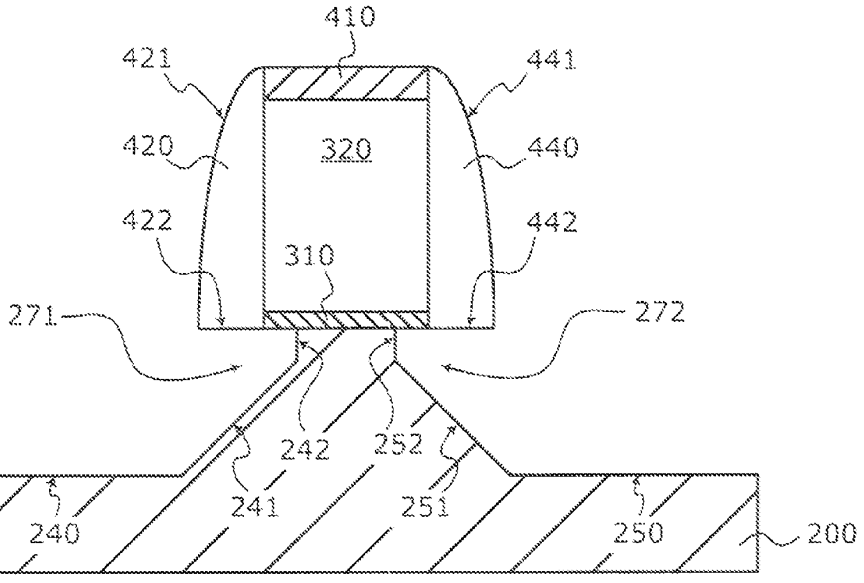


FIGURE 6B

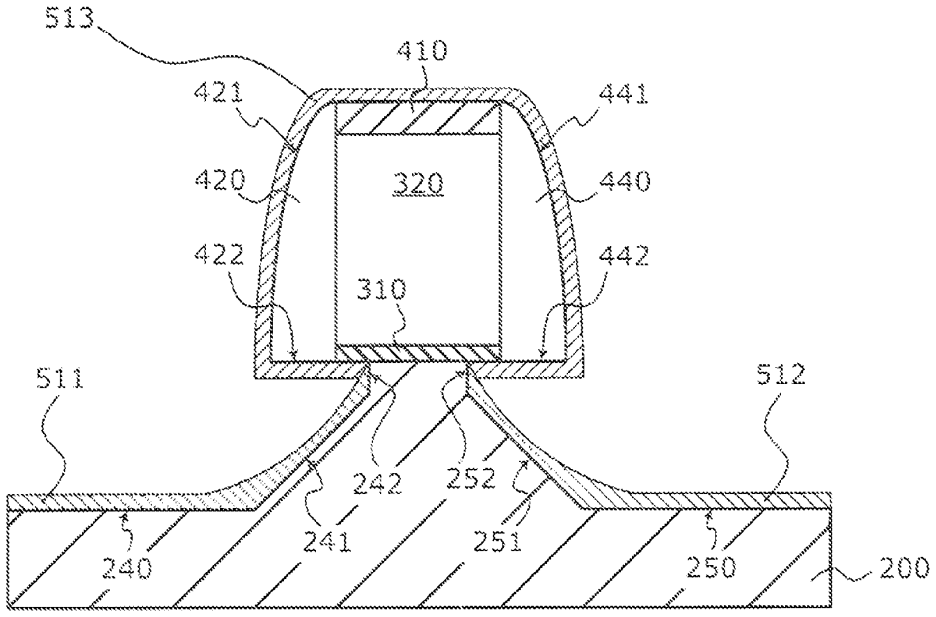


FIGURE 6C

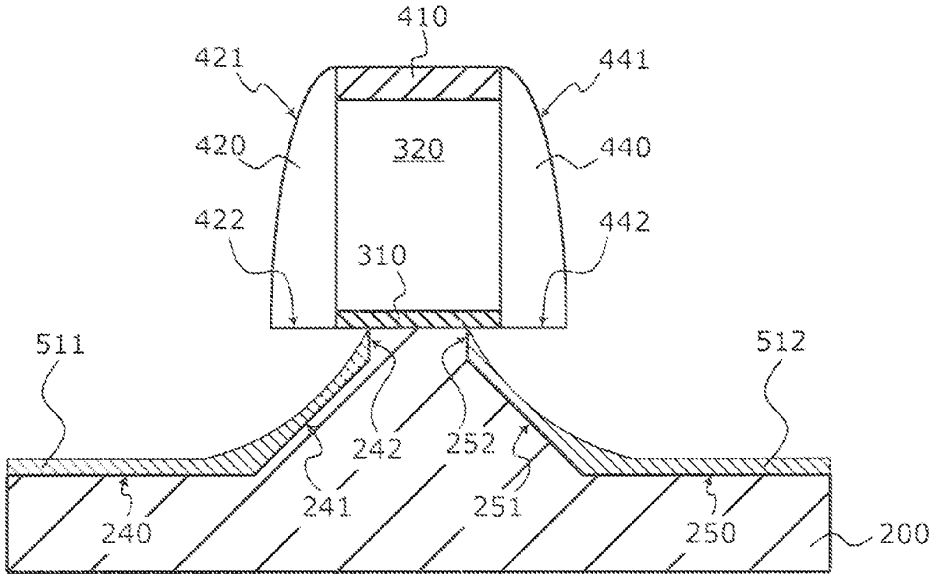


FIGURE 6D

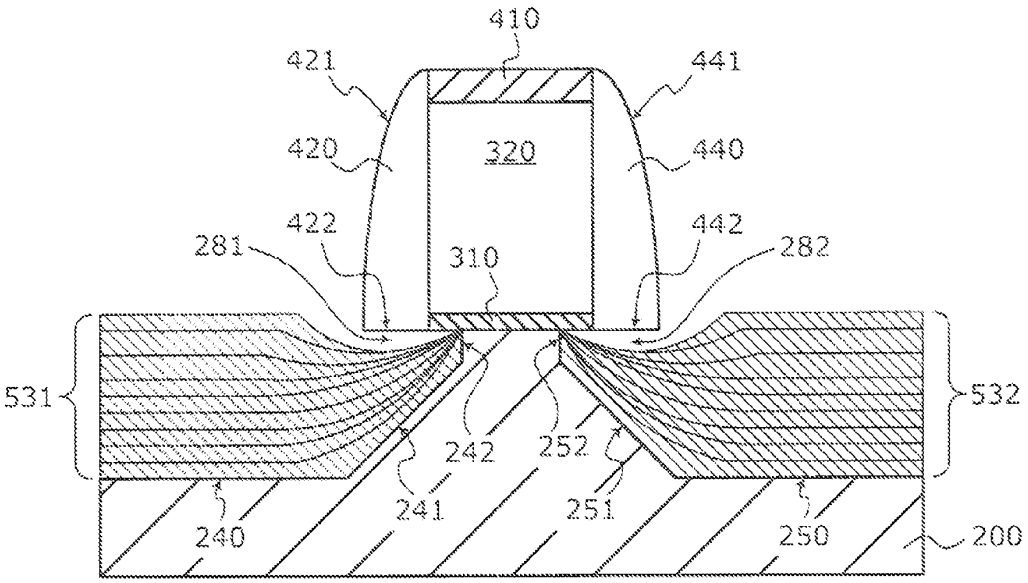


FIGURE 6E

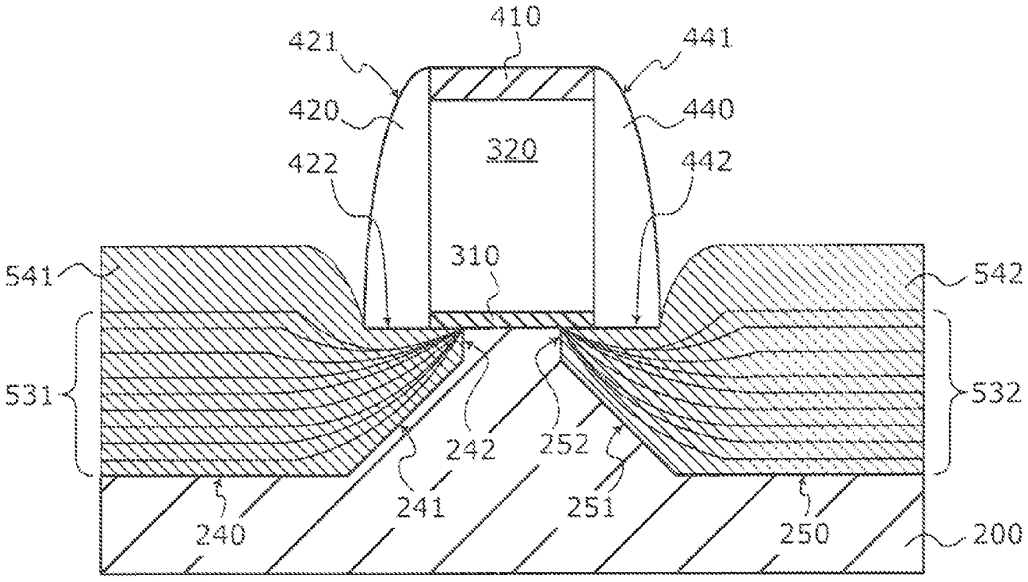


FIGURE 6F

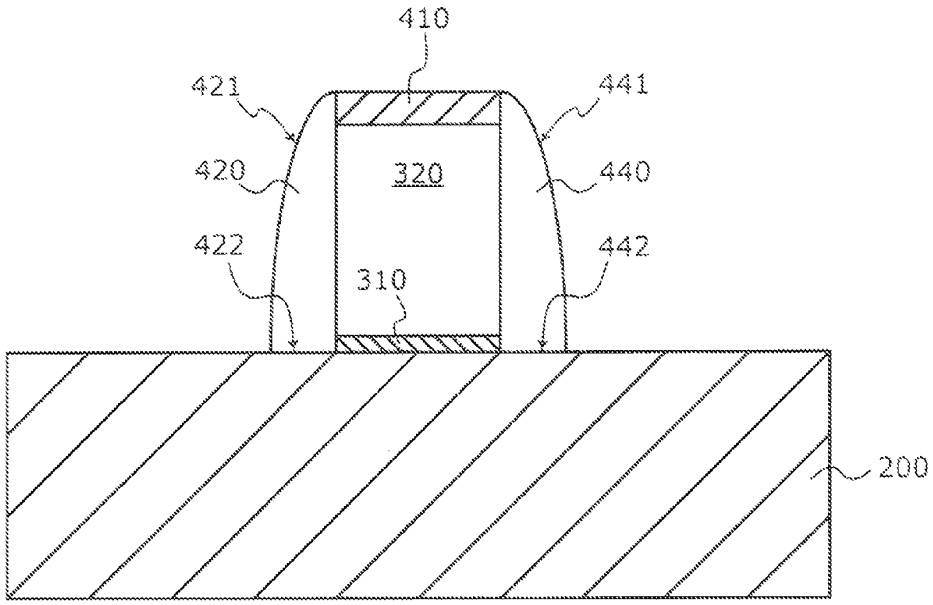


FIGURE 7A

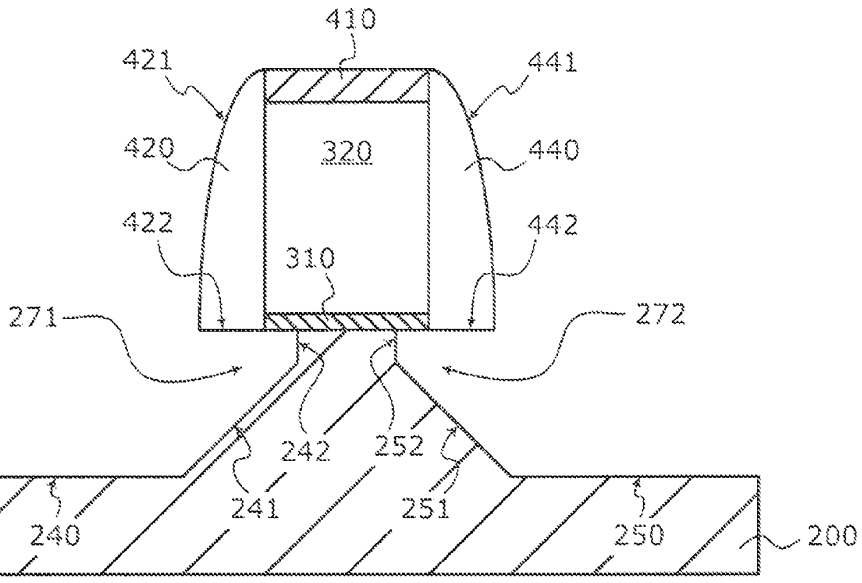


FIGURE 7B

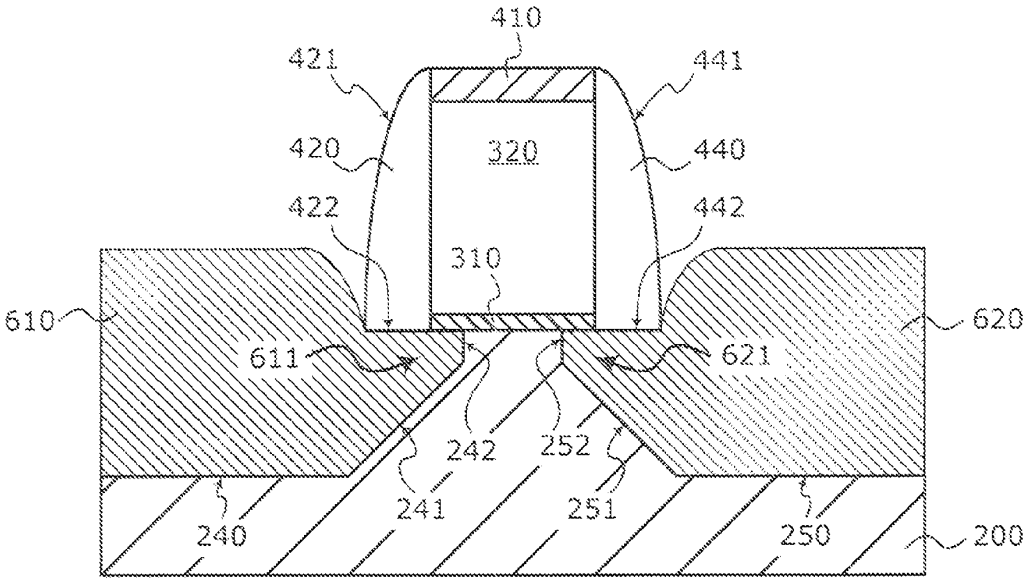

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FIGURE 7C

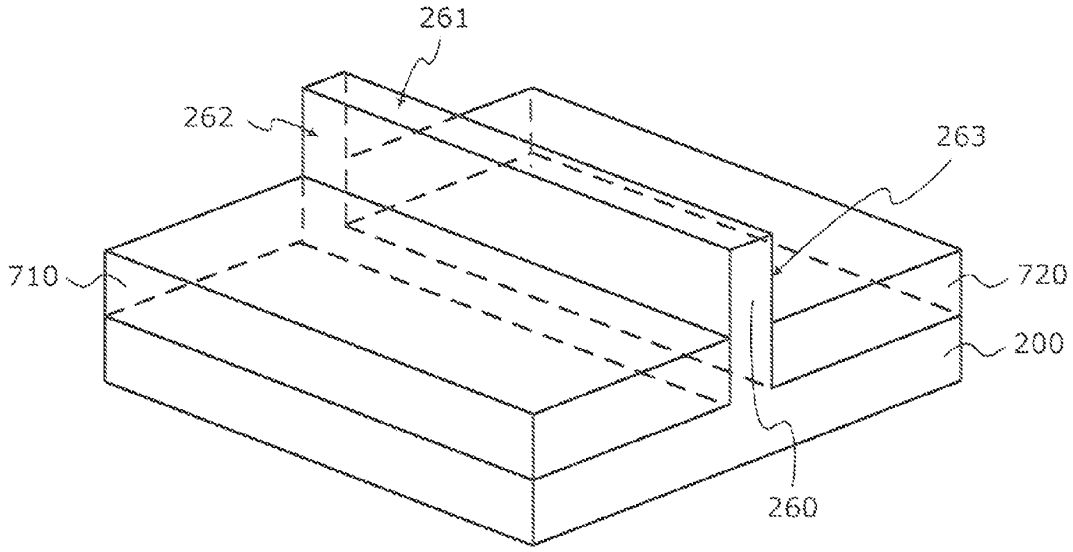


FIGURE 8A

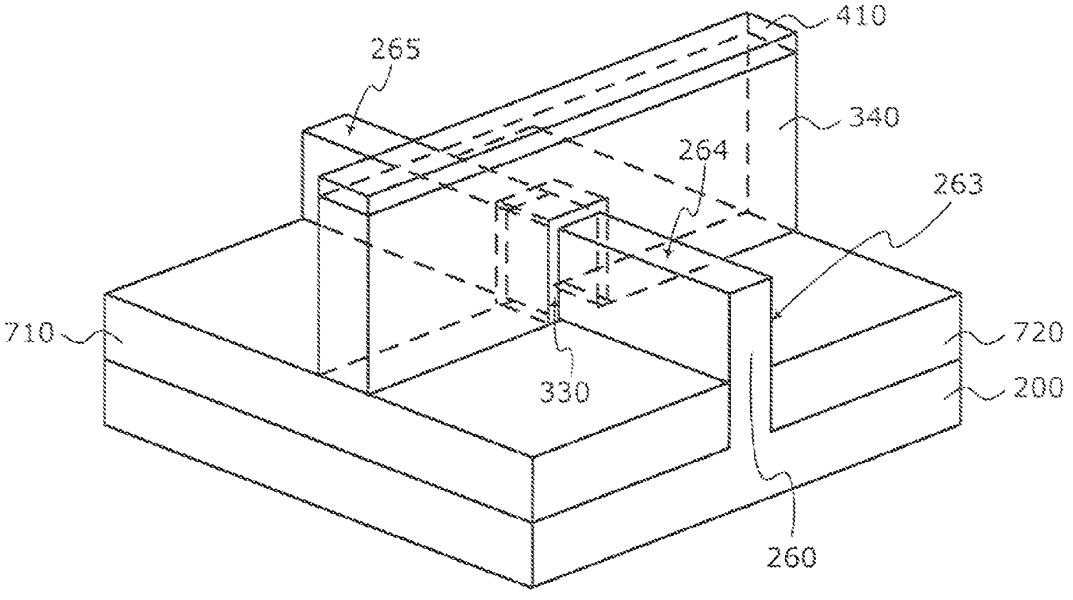


FIGURE 8B

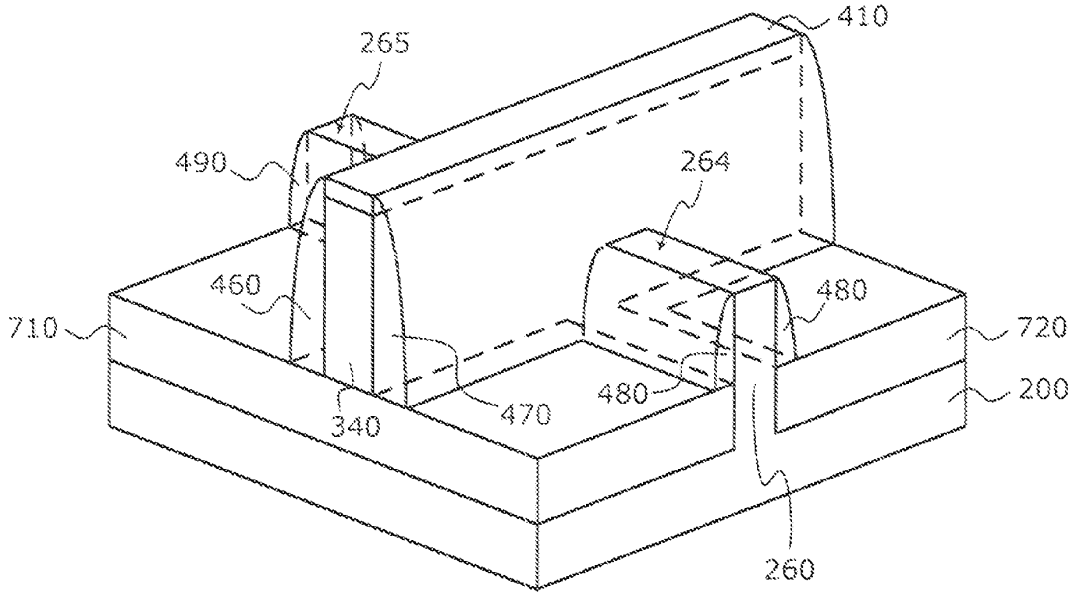


FIGURE 8C

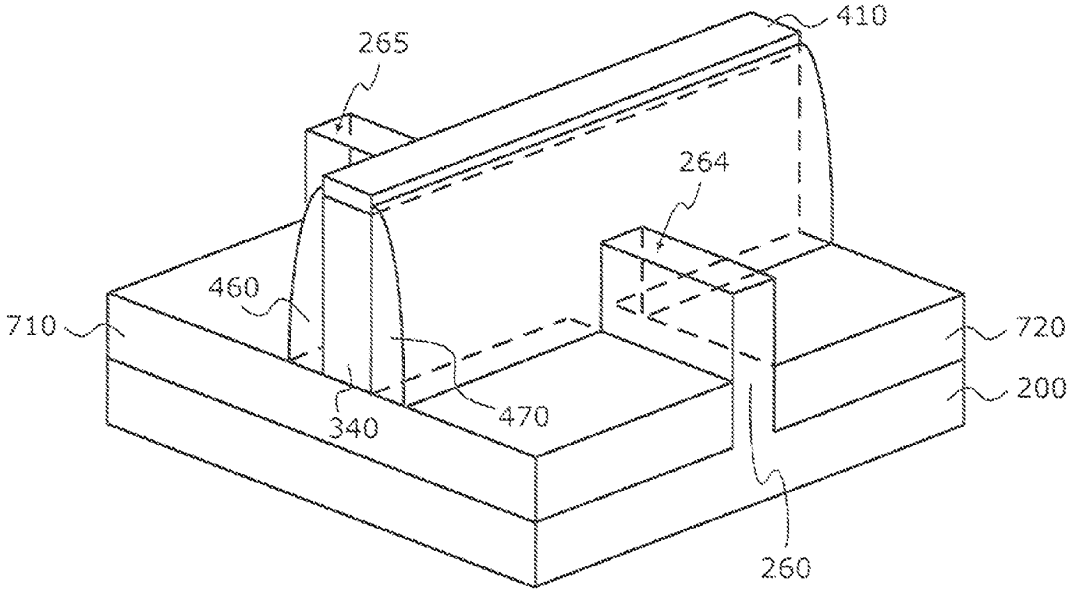


FIGURE 8D

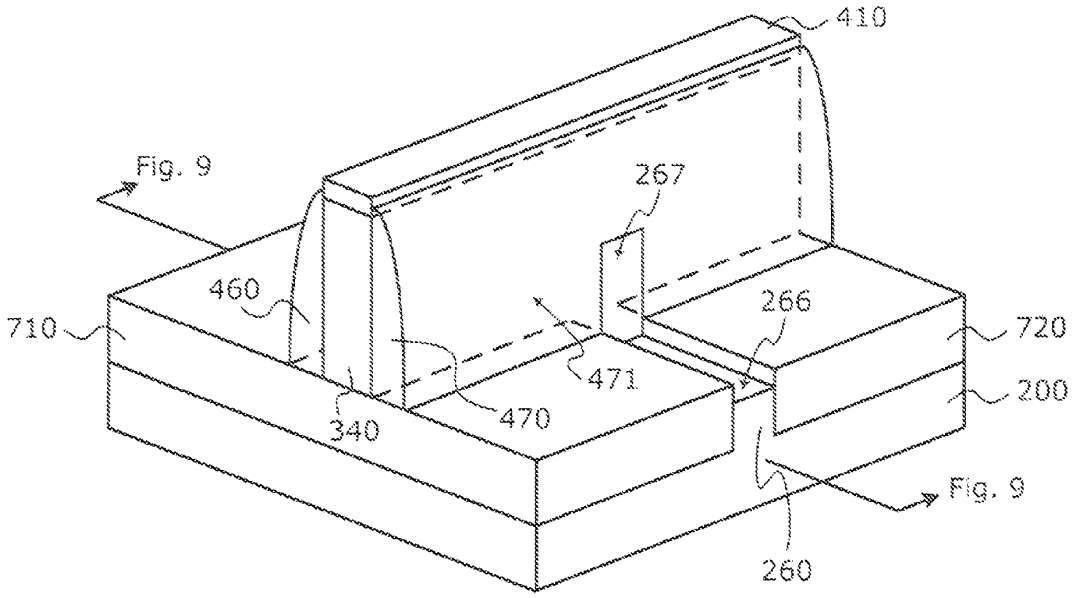


FIGURE 8E

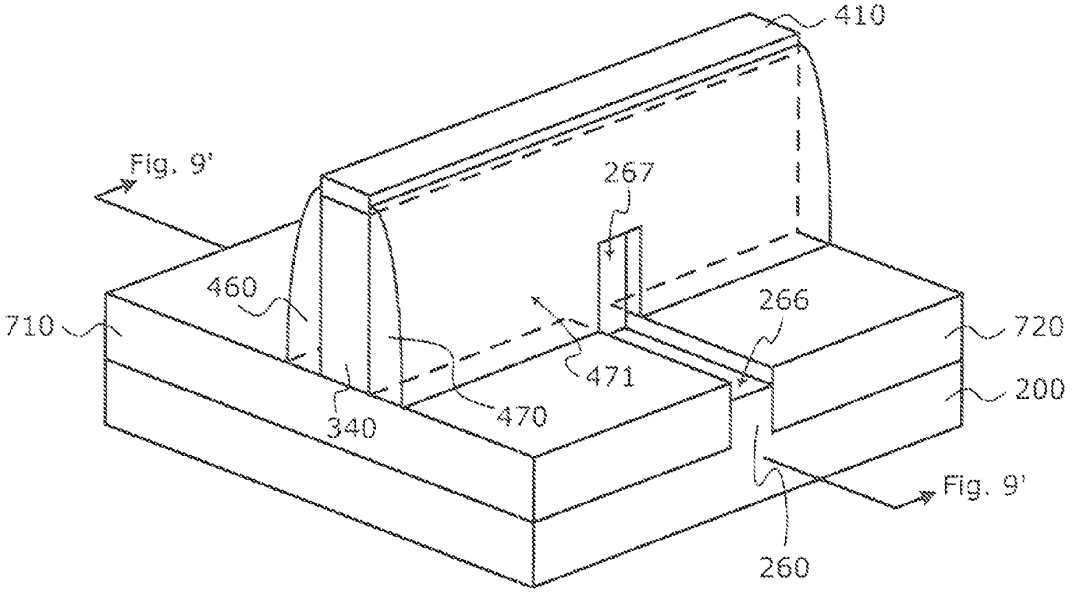


FIGURE 8E'

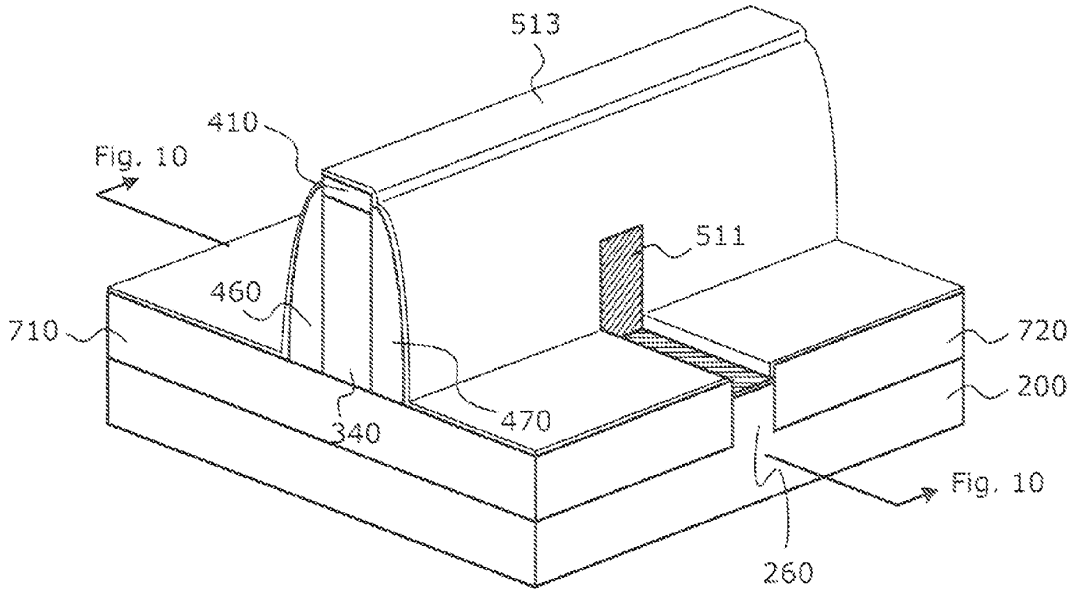


FIGURE 8F

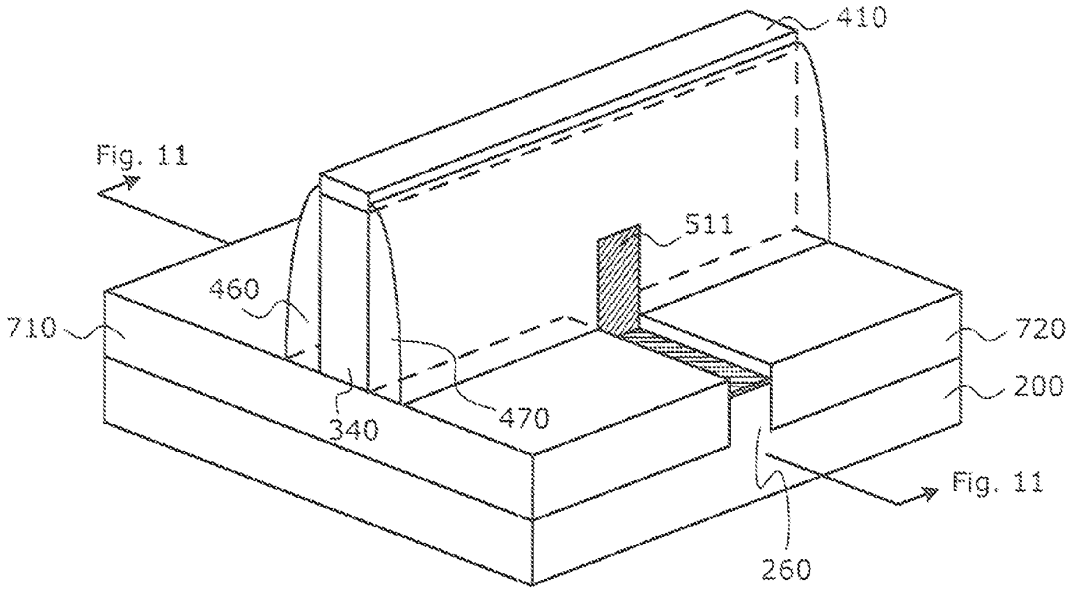


FIGURE 8G

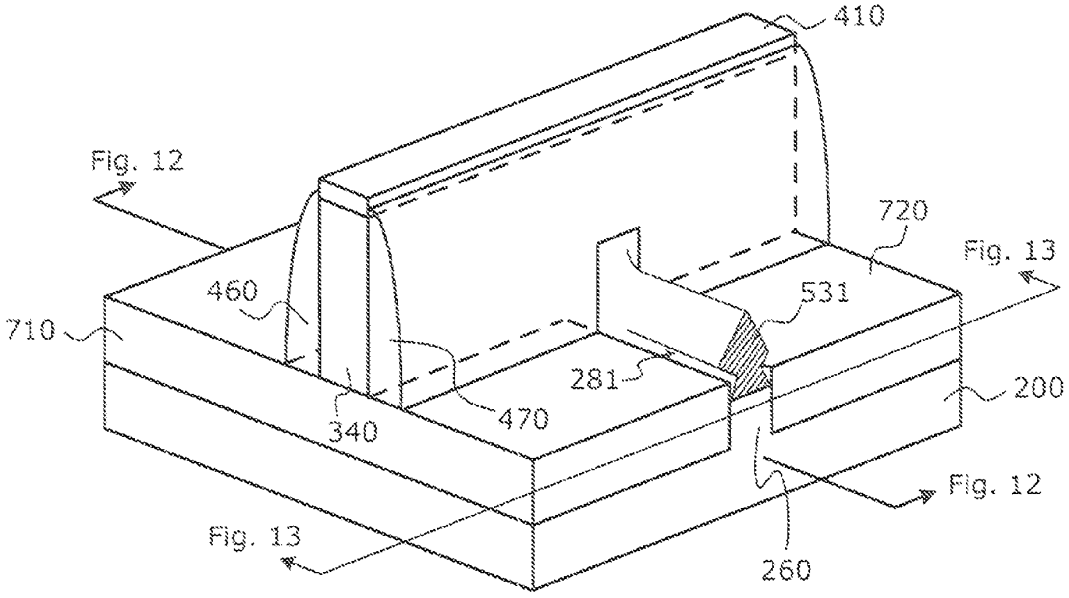


FIGURE 8H

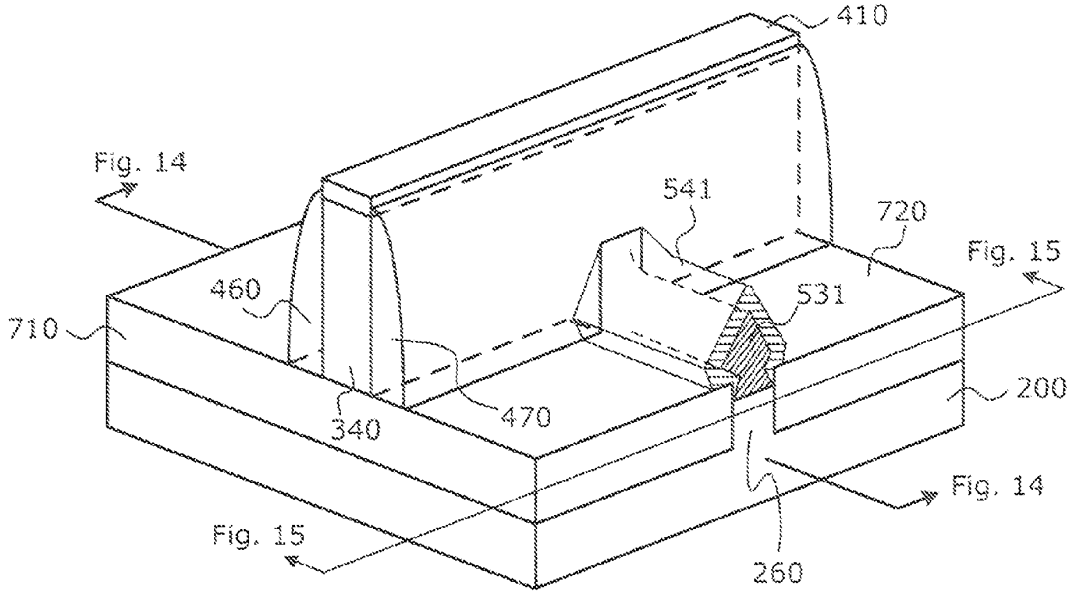


FIGURE 8I

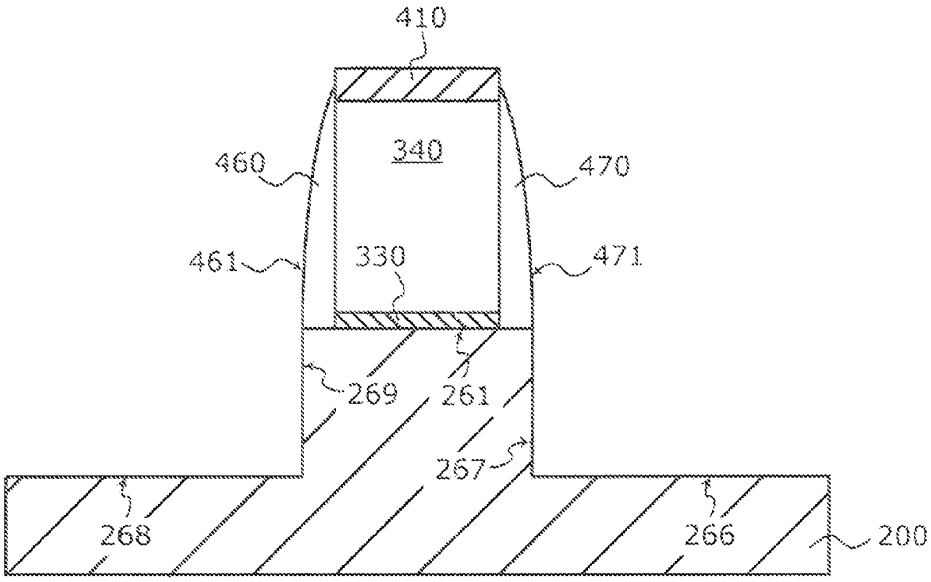


FIGURE 9

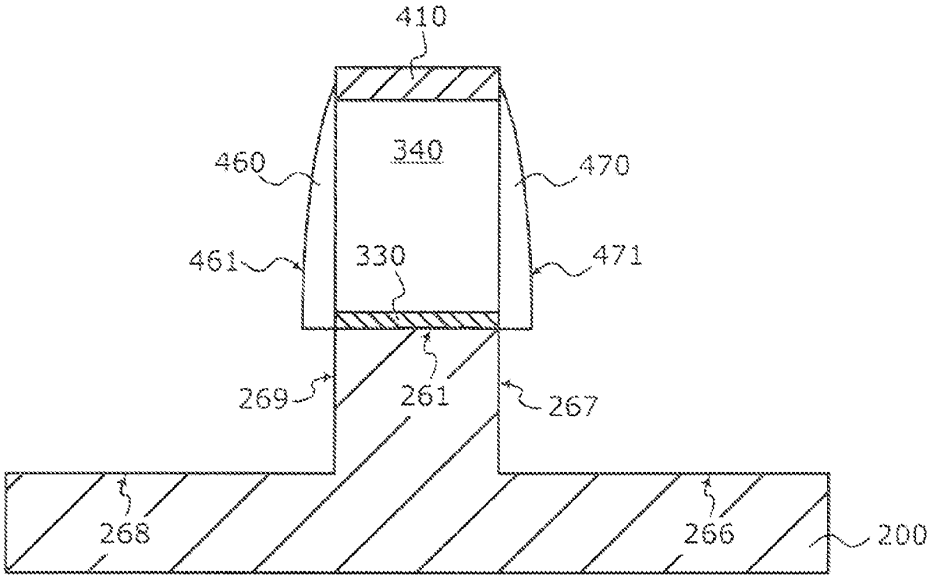


FIGURE 9'

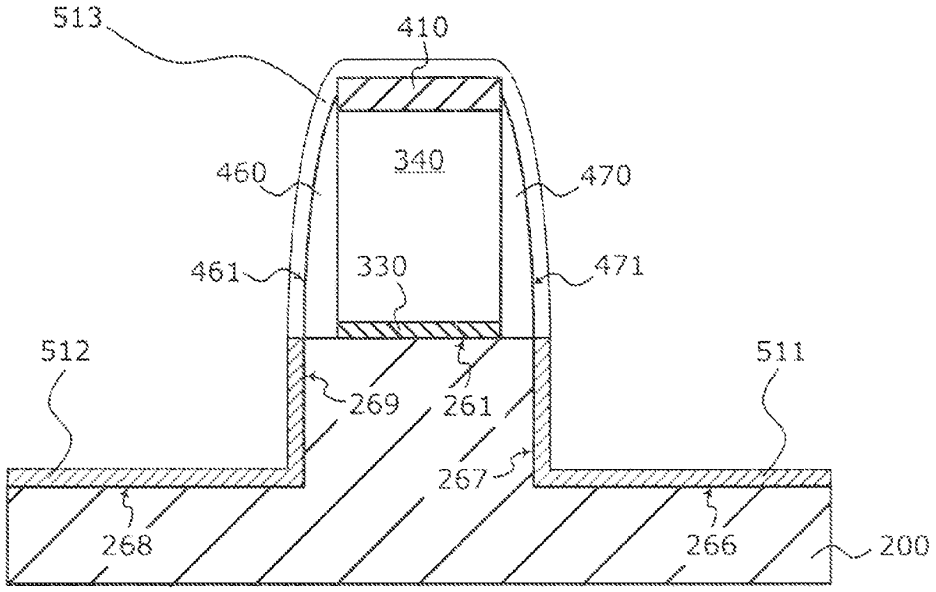


FIGURE 10

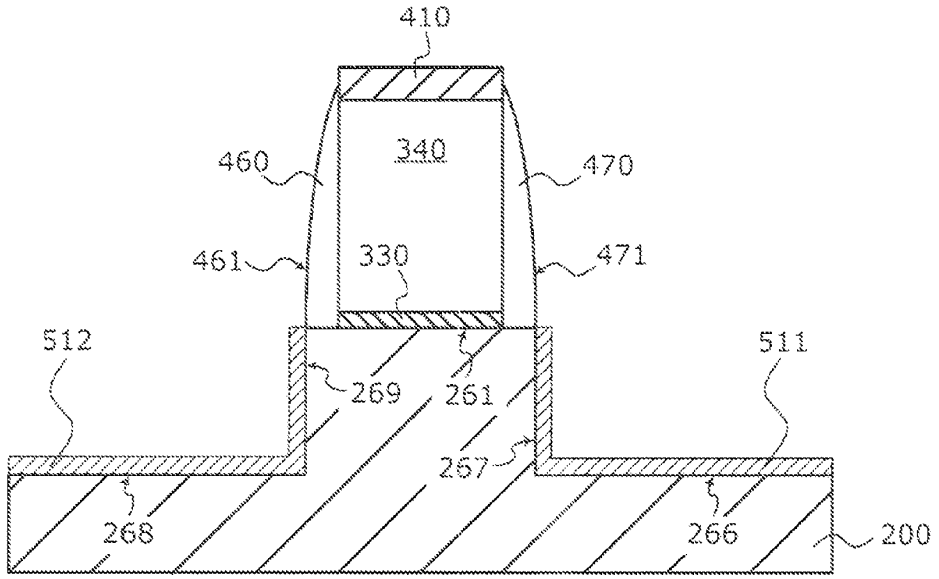


FIGURE 11

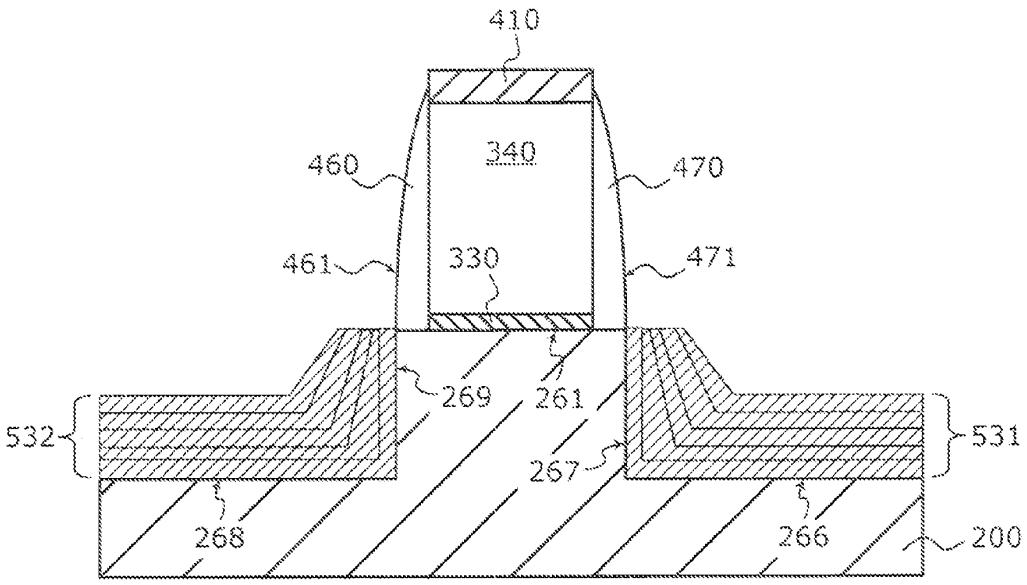


FIGURE 12

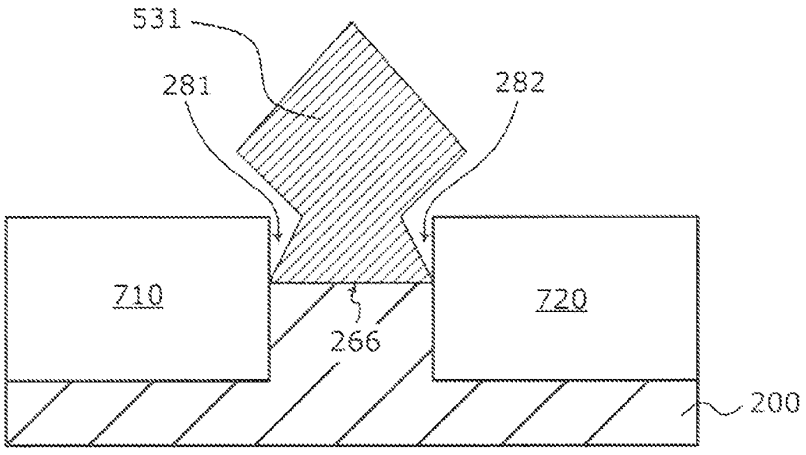


FIGURE 13

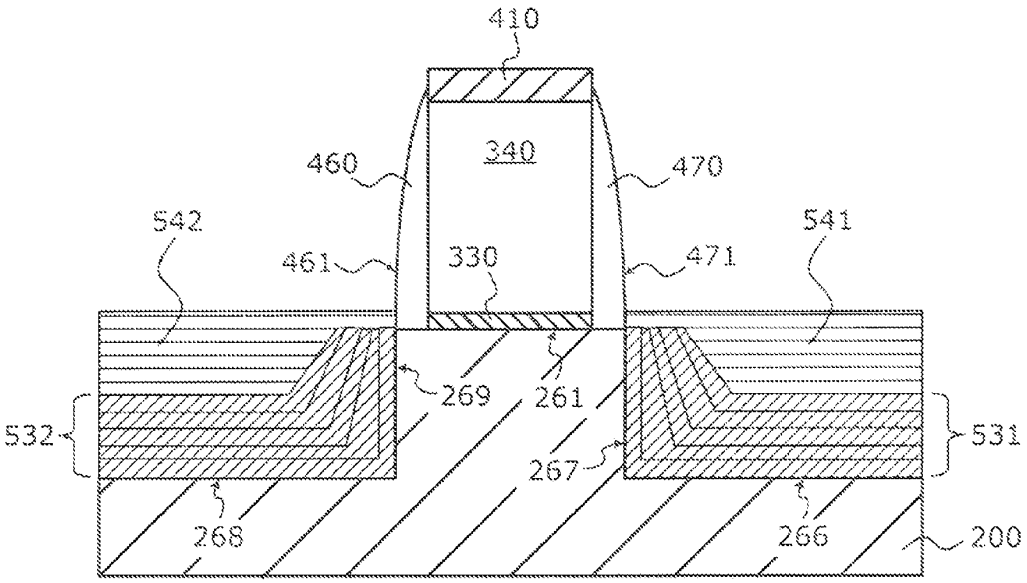


FIGURE 14

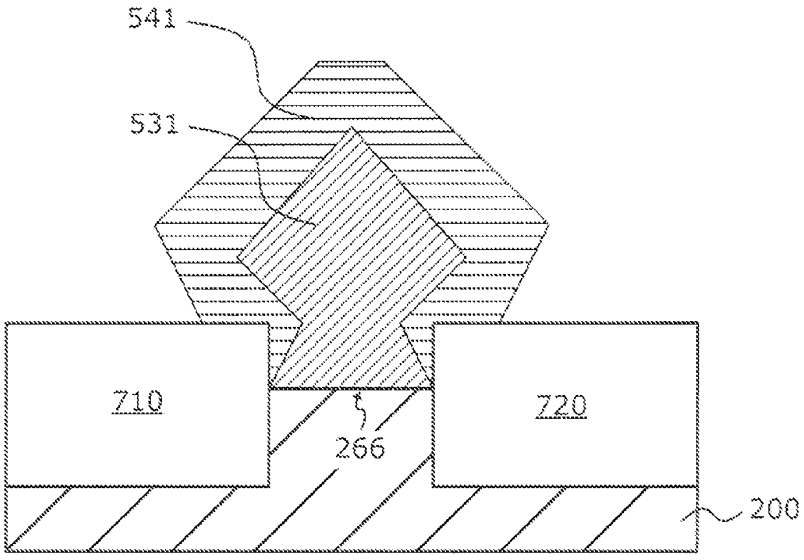


FIGURE 15

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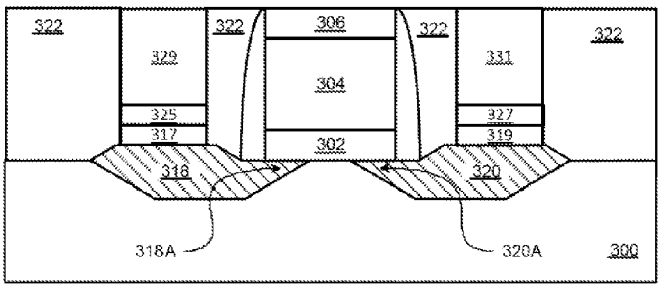


FIG. 5F

(57) Abstract: Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on, for example, silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures. Graded buffering can be used to reduce misfit dislocation. The techniques are particularly well-suited for implementing p-type devices, but can be used for n-type devices if so desired.

WO 2012/087403 A1

CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Inventors:
Glenn A. Glass
Anand S. Murthy
Tahir Ghani

RELATED APPLICATION

[0001] This application is a continuation-in-part of U.S. Application No. 12/975,278 filed December 21, 2010.

BACKGROUND

[0002] Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to minimize the parasitic resistance associated with contacts otherwise known as external resistance R_{ext}. Decreased R_{ext} enables higher current from an equal transistor design.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1A illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention.

[0004] Figure 1B illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0005] Figure 1C illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0006] Figure 2 is a method for forming a transistor structure with low contact resistance in accordance with an embodiment of the present invention.

[0007] Figures 3A to 3I illustrate structures that are formed when carrying out the method of Figure 2, in accordance with various embodiment of the present invention.

[0008] Figure 4 is a method for forming a transistor structure with low contact resistance in accordance with another embodiment of the present invention.

[0009] Figures 5A to 5F illustrate structures that are formed when carrying out the method of Figure 4, in accordance with various embodiment of the present invention.

[0010] Figure 6 shows a perspective view of a FinFET transistor architecture, configured in accordance with one embodiment of the present invention.

[0011] Figure 7 shows a plot of a split lot showing contact resistance for transistor structures configured with in accordance with embodiments of the present invention and standard transistor structures configured with no cap.

[0012] Figure 8 illustrates a computing system implemented with one or more transistor structures in accordance with an example embodiment of the present invention.

[0013] As will be appreciated, the figures are not necessarily drawn to scale or intended to limit the claimed invention to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of a transistor structure may have less than perfect straight lines, right angles, and some features may have surface topology or otherwise be non-smooth, given real world limitations of the processing equipment and techniques used. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

[0014] Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and

suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures. The techniques are particularly well-suited for implementing p-type devices, but can be used for n-type devices if so desired.

General Overview

[0015] As previously explained, increased drive current in the transistors can be achieved by reducing device resistance. Contact resistance is one component of a device's overall resistance. A standard transistor contact stack typically includes, for example, a silicon or SiGe source/drain layer, a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad. In such configurations, the contact resistance is effectively limited by the silicon or SiGe valence band alignment to the pinning level in the metal. Typically, using industry standard silicides such as nickel (or other suitable silicides, such as titanium, cobalt, or platinum), this results in a band misalignment of about 0.5 eV. Thus, and in accordance with an example embodiment of the present invention, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce the band misalignment value and contact resistance.

[0016] In one specific example embodiment, contacts configured with the intermediate boron doped germanium layer exhibit a reduction in the band misalignment value to less than 0.2 eV and a corresponding reduction in contact resistance of about 3X (relative to a conventional contact stack similarly configured, but without the intermediate boron doped germanium layer between the source/drain regions and contact metal). A transmission electron microscopy (TEM) cross section or secondary ion mass spectrometry (SIMS) profile can be used to show the germanium concentration throughout the vertical stack of the film structure, as profiles of epitaxial alloys of silicon and SiGe can readily be distinguished from germanium concentration profiles.

[0017] Thus, transistor structures configured in accordance with embodiments of the present invention provide an improvement over conventional structures with respect to lower contact resistance. Some such embodiments effectively marry superior contact properties of germanium with superior semiconductor transistor properties of Si and SiGe to provide next generation low resistance contacts.

[0018] Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., such as double-gate and trigate transistor structures), as well as strained and unstrained channel structures. Any number of such structural features and material systems can be used in conjunction with a germanium overlayer as described herein. The transistor structure may include p-type source/drain regions, n-type source/drain regions, or both n-type and p-type source/drain regions. In some example embodiments, the transistor structure includes dopant-implanted source/drain regions or epitaxial (or poly) replacement source/drain regions of silicon, SiGe alloys, or nominally pure germanium films (e.g., such as those with less than 10% silicon) in a MOS structure. In any such implementations, an overlayer or cap of boron doped germanium can be formed directly over the source/drain regions, in accordance with an embodiment of the present invention. A contact metal (or series of metals) can then be deposited and a subsequent reaction (annealing) can be carried out to form metal germanide source and drain contacts. As will be appreciated, the contact may be implemented as a stack including one or more of a silicide layer, an adhesion layer, and/or a metal pad layer. The boron doped germanium overlayer can be formed directly over other parts of the transistor structure as well, such as the poly gate and/or grounding tap regions, if so desired.

[0019] As is known, a MOS transistor may include source and drain tip regions that are designed to decrease the overall resistance of the transistor while improving short channel effects (SCE). Conventionally, these tip regions are portions of the substrate where a dopant such as boron or carbon is implanted using an implant and diffusion technique. The source tip region is formed in the area between the source region and the channel region. Likewise, the drain tip region is formed in the area between the drain region and the channel region. Some embodiments of the present invention are configured with such conventionally formed tip regions. In other example embodiments, fabrication techniques are employed to extend self-aligned epitaxial tip (SET) transistors to achieve very near to the theoretical limit of uniaxial strain. This can be accomplished, for instance, by selective epitaxial deposition in the source and drain regions as well as their corresponding tip regions to form a bilayer construction of boron doped silicon or SiGe (for the source/drain regions) capped with an overlayer of a boron doped germanium layer in the source/drain and respective tip regions. The germanium and boron concentrations can vary, but in some example embodiments, the germanium concentration is in

the range of 20 atomic % to 100 atomic %, and the boron concentration is in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., germanium concentration in excess of 50 atomic % and boron concentration in excess of 2E20 cm^{-3}). Note that the boron doped germanium layer may be provided in the tip regions, but in other embodiments is just provided over the source/drain regions (and not in the tip regions).

[0020] In still other example embodiments, an optional thin buffer with graded germanium concentration and/or boron concentration can be used as an interfacial layer between the underlying substrate with the source/drain layer (e.g., silicon or SiGe). Likewise, a thin buffer with graded germanium concentration and/or boron concentration can be used as an interfacial layer between the source/drain layer and the boron doped germanium cap. In still other embodiments, the boron doped germanium overlayer or source/drain layer themselves can have a graded germanium and/or boron concentration in a similar fashion as to the optional buffers. In any such case, since boron diffusion is suppressed in germanium (the higher the concentration, the greater the relative suppression), a high concentration of boron can be doped in the germanium, which in turn results in lower parasitic resistance and without degrading tip abruptness. In addition, the contact resistance is reduced from lowering of Schottky-barrier height.

Architecture and Methodology

[0021] Figure 1A illustrates a MOS device 100A formed on a substrate 102 and configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention. In particular, boron doped germanium layer 117 is provided between the source layer 110 and contact metals 125, and boron doped germanium layer 119 is provided between the drain layer 112 and contact metals 127. The source region 110 and the drain region 112 can be formed using any number of conventional techniques. In this example embodiment, for instance, the source region 110 and the drain region 112 are formed by etching the substrate and then epitaxially depositing a silicon or silicon germanium material (e.g., with a germanium concentration in the range of, for instance, 10 to 70 atomic %).

[0022] A gate stack 122 is formed over a channel region 120 of the transistor 100A. As can further be seen, the gate stack 122 includes a gate dielectric layer 106 and a gate electrode 104,

and spacers 108 are formed adjacent to the gate stack 122. In some example cases, and depending on the technology node, the spacers 108 create a distance of about 10 to 20 nanometers (nm) between the edges of the gate dielectric layer 106 and the edges of each of the source and drain regions 110/112. It is within this space that a source tip region 110A and a drain tip region 112A can be formed. In this example embodiment, the tip regions 110A/112A are formed via a typical implantation-diffusion based process, and overlap the spacers 108 and may also overlap or underdiffuse the gate dielectric layer 106 by a distance of, for instance, less than 10 nm. In forming the implantation-diffusion based tip regions 110A/112A, a dopant such as boron or carbon is implanted into the source region 110 and the drain region 112. The transistor 100A is then annealed to cause the dopant to diffuse towards the channel region 120. Angled ion implantation techniques may also be used to further implant dopants into those areas between the gate dielectric layer 106 and the source/drain regions 110/112. Such implantation-diffusion-based tip formation processes generally do not induce a strain on the channel region.

[0023] In any case, and as will be appreciated in light of this disclosure, whether a transistor structure has a strained or unstrained channel, or source-drain tip regions or no source-drain tip regions, is not particularly relevant to various embodiments of the present invention, and such embodiments are not intended to be limited to any particular such structural features. Rather, any number of transistor structures and types can benefit from employing a boron doped germanium overlayer as described herein. The techniques provided herein are compatible, for instance, with conventional dopant implanted silicon, raised source/drain, strained SiGe (or other suitable materials), and any deposited epitaxial tip (sometimes referred to as source-drain extensions) that extend below the gate electrode dielectric or are spaced away from the vertical line defined by the gate electrode dielectric.

[0024] The germanium overlayer 117/119 is generally provided after formation of the source/drain regions 110/112 and prior to formation of the contacts 125/127. The thickness of this overlayer 117/119 can vary from one embodiment to the next, but in one example embodiment is in the range of 50 to 250 Angstroms (Å). The boron concentration of overlayer 117/119 can also vary, but in one example embodiment is in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., in excess of 2E20 cm^{-3}). The overlayer 117/119 can be selectively deposited over the source/drain 110/112 regions (and/or other regions as desired, such as the poly gate or grounding tap regions). Any number of suitable deposition techniques can be used to provide the overlayer

117/119 (e.g., chemical vapor deposition, molecular beam epitaxy, etc). In accordance with one example embodiment, the contact metals 125 and 127 each comprise a stack a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad, and although any number of contact metal configurations can be used as will be appreciated in light of this disclosure. Standard deposition techniques can be used in providing the contact metals 125/127.

[0025] Figure 1B illustrates an example MOS device 100B formed on a substrate 102 and configured with a boron doped germanium layer 117/119 between the source/drain layer 110/112 and contact metals 125/127, in accordance with another embodiment of the present invention. This example configuration includes source and drain epitaxial tips (generally referred to herein as epi-tips). In more detail, the MOS transistor 100B uses an undercut etch to allow the source region 110 and the drain region 112 to extend below the spacers 108, and in some cases, below the gate dielectric layer 106. The portions of the source/drain regions 110/112 that extend below the spacers 108 (and possibly the gate dielectric layer 106) are generally referred to as the source epi-tip 110B and the drain epi-tip 112B, respectively. The source and drain epi-tips 110B/112B replace the implantation/diffusion based tip regions 110A/112A described with regard to Figure 1A. In accordance with one embodiment, the source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be formed, for example, by etching the substrate 102, which includes undercutting the spacers 108 (and possibly the gate dielectric layer 106), and then using selective epitaxial deposition to provide, for instance, an in situ doped silicon, germanium, or SiGe to fill the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, as shown in Figure 1B. Note the epitaxial fill may be raised relative to the surface of substrate 102, as further shown in Figure 1B, although non-raised configurations can be used as well. The germanium overlayer 117/119 and the contact metals 125/127 can be implemented, for instance, as previously described with respect to Figure 1A.

[0026] Figure 1C illustrates a MOS device 100C formed on a substrate 102 and configured with boron doped germanium layers 117/119 between the respective source/drain layers 110/112 and contact metals 125/127, in accordance with another embodiment of the present invention. The source region 110 and the drain region 112 in this example embodiment are formed by implanting dopants such as boron into the substrate. The gate stack 122 is formed over a channel region 120 of the transistor 100C and is this example case does not include sidewalls 108. Nor does this example transistor structure include an undercut or tip regions like the embodiments

shown in Figures 1A and 1B. The germanium overlayer 117/119 and the contact metals 125/127 can be implemented, for instance, as previously described with respect to Figure 1A.

[0027] Numerous other variations and features can be implemented for transistor structures configured in accordance with an embodiment of the present invention. For example, a graded buffer may be used in one or more locations of the structure. For instance, the substrate 102 can be a silicon substrate, or a silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate comprising silicon, silicon germanium, germanium, and/or III-V compound semiconductors. Thus, and by way of example, in an embodiment having a silicon or silicon germanium substrate 102 and an in situ boron doped SiGe fill in the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, a buffer can be provided between the underlying substrate 102 and the source/drain material. In one such embodiment, the buffer can be a graded boron doped (or intrinsic) silicon germanium layer with the germanium concentration graded from a base level compatible with the underlying substrate up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). The boron concentration within this buffer can be either fixed (e.g., at a high level) or graded, for instance, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 2E20 cm^{-3}). Note that 'compatibility' as used herein does not necessitate an overlap in concentration levels (for instance, the germanium concentration of underlying substrate can be 0 to 20 atomic % and initial germanium concentration of the buffer can be 30 to 40 atomic %). In addition, as used herein, the term 'fixed' with respect to a concentration level is intended to indicate a relatively constant concentration level (e.g., the lowest concentration level in the layer is within 10% of the highest concentration level within that layer). In a more general sense, a fixed concentration level is intended to indicate the lack of an intentionally graded concentration level. The thickness of the buffer can vary depending on factors such as the range of concentrations being buffered, but in some embodiments is in the range of 30 to 120 Å, such as 50 to 100 Å (e.g., 60 Å or 65 Å). As will be further appreciated in light of this disclosure, such a graded buffer beneficially lowers the Schottky-barrier height.

[0028] Alternatively, rather than using a thin buffer between the substrate 102 and the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, the source/drain material itself can be graded in a similar fashion. For example, and in accordance with one example

embodiment, boron doped SiGe source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to 70 atomic %) up to 100 atomic %. In some such embodiments, the boron concentration within this boron doped germanium layer can range, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 2E20 cm^{-3}).

[0029] In other embodiments, a buffer can be provided between the source/drain material and the boron doped germanium overlayer 117/119. In one such embodiment, the source/drain material is a boron doped SiGe layer having a fixed concentration of germanium (e.g., in the range of 30 to 70 atomic %) and the buffer can be a thin SiGe layer (e.g., 30 to 120 Å, such as 50 to 100 Å) having a germanium concentration graded from a base level concentration compatible with the underlying boron doped SiGe layer up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). In some such cases, the boron concentration within this buffer can be fixed at a desired high level or can range, for example, from a base concentration at or otherwise compatible with the underlying SiGe layer up to the desired high concentration (e.g., in excess of 1E20 cm^{-3}, 2E20 cm^{-3}, or 3E20 cm^{-3}). Alternatively, rather than using a buffer between the source/drain material and the boron doped germanium overlayer 117/119, the overlayer 117/119 itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, the boron doped overlayer 117/119 can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate and/or source/drain regions (e.g., in the range of 30 to 70 atomic %) up to 100 atomic % (or near 100 atomic %). The boron concentration within this overlayer 117/119 layer can be fixed at a desired high level or can range, for example, from a base concentration at or otherwise compatible with the underlying substrate and/or source/drain regions up to the desired high level (e.g., in excess of 2E20 cm^{-3}).

[0030] Thus, a low contact resistance architecture for numerous transistor devices is provided. The devices may be formed in part using any number of conventional processes such as, for example, by gate oxide, poly gate electrode, thin spacer, and an isotropic undercut etch in the source/drain regions (or an ammonia etch to form faceted fin recess in monocrystalline substrate, or other suitable etch to form fin recess). In accordance with some embodiments, selective

epitaxial deposition can be used to provide in situ doped silicon or alternatively, a fully strained silicon germanium layer to form source/drain regions with or without tips. Optional buffers may be used as previously explained. Any suitable high-k replacement metal gate (RMG) process flow can also be used, where a high-k dielectric replaces the conventional gate oxide. Silicidation with, for example, nickel, nickel-platinum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. The techniques provided herein can be applied, for example, to benefit any technology nodes (e.g., 90nm, 65nm, 45nm, 32nm, 22nm, 14nm, and 10nm transistors, and lower), and the claimed invention is not intended to be limited to any particular such nodes or range of device geometries. Other advantages will be apparent in light of this disclosure.

[0031] Figure 2 is a method for forming a transistor structure with low contact resistance in accordance with an embodiment of the present invention. Figures 3A through 3I illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments.

[0032] As can be seen, the method begins with forming 202 a gate stack on a semiconductor substrate upon which a MOS device, such as a PMOS transistor, may be formed. The semiconductor substrate may be implemented, for example, with a bulk silicon or a silicon-on-insulator configuration. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, such as germanium, silicon germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. In a more general sense, any material that may serve as a foundation upon which a semiconductor device may be built can be used in accordance with embodiments of the present invention. The gate stack can be formed as conventionally done or using any suitable custom techniques. In some embodiments of the present invention, the gate stack may be formed by depositing and then patterning a gate dielectric layer and a gate electrode layer. For instance, in one example case, a gate dielectric layer may be blanket deposited onto the semiconductor substrate using conventional deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Alternate deposition techniques may be used as well, for instance, the gate dielectric layer may be thermally grown. The gate dielectric material may be formed, for example, from materials such as silicon dioxide or high-k dielectric materials.

Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some specific example embodiments, the high-k gate dielectric layer may be between around 5 Å to around 200 Å thick (e.g., 20 Å to 50 Å). In general, the thickness of the gate dielectric layer should be sufficient to electrically isolate the gate electrode from the neighboring source and drain contacts. In further embodiments, additional processing may be performed on the high-k gate dielectric layer, such as an annealing process to improve the quality of the high-k material. Next, a gate electrode material may be deposited on the gate dielectric layer using similar deposition techniques such as ALD, CVD, or PVD. In some such specific embodiments, the gate electrode material is polysilicon or a metal layer, although other suitable gate electrode materials can be used as well. The gate electrode material, which is may be a sacrificial material that is later removed for a replacement metal gate (RMG) process, has a thickness in the range of 50Å to 500Å (e.g., 100Å), in some example embodiments. A conventional patterning process may then be carried out to etch away portions of the gate electrode layer and the gate dielectric layer to form the gate stack, as shown in Figure 3A. As can be seen, Figure 3A illustrates a substrate 300 upon which a gate stack is formed. In this example embodiment, the gate stack includes a gate dielectric layer 302 (which may be high-k gate dielectric material) and a sacrificial gate electrode 304. In one specific example case, the gate stack includes a silicon dioxide gate dielectric layer 302 and a polysilicon gate electrode 304. The gate stack may also include a gate hard mask layer 306 that provides certain benefits or uses during processing, such as protecting the gate electrode 304 from subsequent ion implantation processes. The hard mask layer 306 may be formed using typical hard mask materials, such as such as silicon dioxide, silicon nitride, and/or other conventional dielectric materials. Figure 3A further illustrates spacers 310 formed on either side of the stack. The spacers 310 may be formed, for example, using conventional materials such as silicon oxide, silicon nitride, or other suitable spacer materials. The width of the spacers 310 may generally be chosen based on design requirements for the transistor being formed. In accordance with some embodiments, however, the width of the spacers 310 is not subject to design constraints imposed

by the formation of the source and drain epi-tips, given sufficiently high boron doped germanium content in the source/drain tip regions, as described herein (boron won't diffuse into channel).

[0033] With further reference to Figure 2, after the gate stack is formed, the method continues with defining 204 the source/drain regions of the transistor structure. As previously explained, the source/drain regions can be implemented with any number of suitable processes and configurations. For example, the source/drain regions may be implanted, etched and epi filled, raised, silicon or SiGe alloy, p-type and/or n-type, and have a planar or fin shaped diffusion region. In the example embodiment shown in Figure 3A, substrate 300 has been etched to provide cavities 312/314 as well as respective tip areas 312A/314A which undercuts the gate dielectric 302. Figure 3B illustrates the substrate 300 after cavities 312/314 and tip areas 312A/314A have been filled to provide the source/drain regions 318/320 and tip regions 318A/320A. In accordance with some example embodiments, the source and drain region cavities 312/314 along with their respective tip areas 312A/314A are filled with in situ doped silicon or SiGe, thereby forming source region 318 (along with epi-tip 318A) and drain region 320 (along with drain epi-tip 320A). Any number of source/drain layer configurations can be used here, with respect to materials (e.g., silicon, SiGe, III-V materials), dopant (e.g., boron in excess of 2E21 cm^{-3}, or other suitable dopant/concentration), and dimension (e.g., thickness of source/drain layer may range, for instance, from 50 to 500 nm so as to provide a flush or raised source/drain region).

[0034] As previously explained, some such embodiments may include with a thin buffer between the source/drain layer and the substrate or the source/drain and boron doped germanium overlayer. For instance, and as can further be seen in the example embodiment shown in Figure 3B, a source buffer 313 and a drain buffer 315 are deposited prior to depositing the source/drain materials. In some embodiments, the buffers 313 and 315 can be a graded boron doped silicon germanium layer with the germanium composition graded from a base level concentration compatible with the underlying substrate 300 material up to 100 atomic % (or near to 100 atomic % as previously described). The boron concentration can be appropriately graded as well. Numerous buffer schemes will be apparent in light of this disclosure.

[0035] With further reference to Figure 2, after the source/drain regions are defined, the method continues with depositing 206 boron doped germanium on the source/drain regions of the transistor structure. Figure 3C shows the boron doped germanium layer 317/319. In some

example embodiments, the boron doped germanium layer 317/319, which may be epitaxially deposited in one or more layers, has a germanium concentration in excess of 90 atomic %, although other suitable concentration levels can be used as will be appreciated in light of this disclosure (e.g., in excess of 91 atomic %, or 92 atomic %, ..., or 98 atomic %, or 99 atomic %, or truly pure germanium). As previously explained, this germanium concentration may be fixed or graded so as to increase from a base level (near substrate 300) to a high level (e.g., in excess of 90 atomic %). The boron concentration in some such embodiments can be in excess of 1E20 cm^{-3}, such as higher than 2E20 cm^{-3} or 2E21 cm^{-3}, and may also be graded so as to increase from a base level near substrate 300 to a high level (e.g., in excess of 1E20 cm^{-3} or 2E20 cm^{-3} or 3E20 cm^{-3}, ..., 2E21 cm^{-3}). In embodiments where the germanium concentration of the underlying source/drain regions 318/320 is fixed or otherwise relatively low, a graded buffer may be used to better interface source/drain regions 318/320 with the boron doped germanium layer 317/319, as previously explained. The thickness of the boron doped germanium cap 317/319 may have a thickness in the range, for example, of 50 to 250 Å, in accordance with some specific example embodiments, although alternative embodiments may have other layer thicknesses, as will be apparent in light of this disclosure.

[0036] In some embodiments, a CVD process or other suitable deposition technique may be used for the depositing 206 or otherwise forming the boron doped germanium layer 317/319. For example, the depositing 206 may be carried out in a CVD, or rapid thermal CVD (RT-CVD), or low pressure CVD (LP-CVD), or ultra-high vacuum CVD (UHV-CVD), or gas source molecular beam epitaxy (GS-MBE) tool using germanium and boron containing precursors such as germane (GeH_4) or digermane (Ge_2H_6) and diborane (B_2H_6) or boron difluoride (BF_2). In some such embodiments, there may be a carrier gas such as, for instance, hydrogen, nitrogen, or a noble gas (e.g., precursor is diluted at 1-5% concentration of carrier gas). There may also be an etchant gas such as, for example, halogen-based gas such as hydrogen chloride (HCl), chlorine (Cl), or, hydrogen bromide (HBr). The basic deposition of germanium and also boron doped germanium is possible over a wide range of conditions using deposition temperature in the range, for example, of 300°C to 800°C (e.g., 300-500°C) and reactor pressure, for instance, in the range 1 Torr to 760 Torr. Germanium is naturally selective in that it deposits on silicon or silicon-germanium alloy, and does not deposit on other materials such as silicon dioxide and silicon nitride. Since this natural selectivity is not entirely perfect, a small flow of etchant can be used

to increase the selectivity of the deposition, as previously noted. Each of the carrier and etchants can have a flow in the range of 10 and 300 SCCM (typically, no more than 100 SCCM of flow is required, but some embodiments may require higher flow rates). In one specific example embodiment, the deposition 206 is carried out using GeH_4 that is diluted in hydrogen at a 1% concentration and at a flow rate that ranges between 100 and 1000 SCCM. For an in situ doping of boron, diluted B_2H_6 may be used (e.g., the B_2H_6 may be diluted in H_2 at 3% concentration and at a flow rate that ranges between 100 and 600 SCCM. In some such specific example cases, an etching agent of HCl or Cl_2 is added at a flow rate that ranges, for example, between 10 and 100 SCCM, to increase the selectivity of the deposition.

[0037] As will be appreciated in light of this disclosure, the selectivity at which the boron doped germanium layer 317/319 is deposited can vary as desired. In some cases, for instance, the boron doped germanium layer 317/319 is deposited only on the source/drain regions 318/320 or a portion of the source/drain regions 318/320 (rather than across the entire structure). Any number of masking/patterning techniques can be used to selectively deposit layer 317/319. Moreover, other embodiments may benefit from layer 317/319 covering, for example, poly gate regions or grounding tap regions. As will further be appreciated in light of this disclosure, the combination of high germanium concentration (e.g., in excess of 90 atomic % and up to pure germanium) and high boron concentration (e.g., in excess of 2E20 cm^{-3}) can be used to realize significantly lower contact resistance in the source and drain regions (and other areas where low contact resistance is desirable, such as ground tap regions), in accordance with some example embodiments. Further, and as previously explained, since boron diffusion is sufficiently suppressed by pure germanium, no adverse SCE degradation is realized with subsequent thermal anneals despite any high boron concentration proximate the channel (if applicable). Barrier height lowering is also enabled from the higher concentration of germanium at the contact surface. In some example embodiments, a germanium concentration in excess of 95 atomic % and up to pure germanium (100 atomic %) can be used to achieve such benefits.

[0038] With further reference to Figure 2, after the boron doped germanium layer 317/319 is provided, the method continues with depositing 208 a dielectric over layer 317/319. Figure 3D shows dielectric 322 as being flush with the hard mask 306 of the gate stack, but it need not be. The dielectric can be configured in a number of ways. In some embodiments, dielectric 322 is implemented with silicon dioxide (SiO_2) or other low-k dielectric materials. In other

embodiments, dielectric 322 is implemented with a silicon nitride (SiN) liner followed by one or more layers of SiO_2, or any combination of nitride, oxide, oxynitride, carbide, oxycarbide, or other suitable dielectric materials). The dielectric 322, which may be referred to as an interlayer dielectric (ILD), may be planarized as commonly done. Other example dielectric materials include, for instance, carbon doped oxide (CDO), organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. In some example configurations, the ILD layer may include pores or other voids to further reduce its dielectric constant.

|0039| Next, in some embodiments of the present invention where a replacement metal gate (RMG) process is used and as best shown in Figure 3E, the method may further include removing the gate stack (including the high-k gate dielectric layer 302, the sacrificial gate electrode 304, and the hard mask layer 306) using an etching process as conventionally done. In alternate implementations, only the sacrificial gate 304 and hard mask layer 306 are removed. Figure 3E illustrates the trench opening that is formed when the gate stack is etched away, in accordance with one such embodiment. If the gate dielectric layer is removed, the method may continue with depositing a new gate dielectric layer into the trench opening (designated as 324 in Figure 3F). Any suitable high-k dielectric materials such as those previously described may be used here, such as hafnium oxide. The same deposition processes may also be used. Replacement of the gate dielectric layer may be used, for example, to address any damage that may have occurred to the original gate dielectric layer during application of the dry and wet etch processes, and/or to replace a low-k or sacrificial dielectric material with a high-k or otherwise desired gate dielectric material. As further shown in Figure 3F, the method may further continue with depositing the metal gate electrode layer 326 into the trench and over the gate dielectric layer 324. Conventional metal deposition processes may be used to form the metal gate electrode layer, such as CVD, ALD, PVD, electroless plating, or electroplating. The metal gate electrode layer may include, for example, a P-type workfunction metal, such as ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. In some example configurations, two or more metal gate electrode layers may be deposited. For instance, a workfunction metal may be deposited in the gate trench followed by a suitable metal gate electrode fill metal such as aluminum or silver.

[0040] With further reference to Figure 2, after dielectric layer 322 is provided over layer 317/319 (and any desired RMG process), the method continues with etching 210 to form the source/drain contact trenches. Any suitable dry and/or wet etch processes can be used. Figure 3G shows the source/drain contact trenches after etching is complete, in accordance with one example embodiment. The method then continues with depositing 212 contact resistance reducing metal and annealing to form silicide/germanide, and then depositing 214 the source/drain contact plugs. Figure 3H shows the contact metals 325/327, which in some embodiments includes the silicide/germanide, although other embodiments may include additional layers (e.g., adhesion layer). Figure 3I shows the contact plug metal 329/331, which in some embodiments includes aluminum, although any suitably conductive contact metal or alloy can be used for the contact plug 329/331, such as silver, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium, using conventional deposition processes. The germanide/metalization 212 of the source and drain contacts can be carried out, for instance, by silicidation with nickel, aluminum, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants to form a low resistance germanide. The boron doped germanium layer 317/319 allows for metal-germanide formation (e.g., nickel-germanium). The germanide allows for significantly lower Schottky-barrier height and improved contact resistance (including R_{ext}) over that in conventional metal-silicide systems. For instance, conventional transistors typically use a source/drain SiGe epi process, with germanium concentration in the range of 30-40 atomic %. Such conventional systems exhibit R_{ext} values of about 140 Ohm*um, limited by epi/silicide interfacial resistance, which is high and may impede future gate pitch scaling. Some embodiments of the present invention allow for a significant improvement in R_{ext} in PMOS devices (e.g., about a 2x improvement or better, such as a R_{ext} of about 70 Ohm*um), which can better support PMOS device scaling. Thus, transistors having a source/drain configured with boron doped germanium cap 317/319 in accordance with an embodiment of the present, with a boron concentration in excess of 1E20 cm^{-3} and a germanium concentration in excess of 90 atomic % and up to or otherwise near pure germanium (100 atomic %) at the interface between the source/drain regions 318/320 and the contact metals 325/327, can exhibit R_{ext} values of less than 100 Ohm*um, and in some cases less than 90 Ohm*um, and in some cases less than 80 Ohm*um, and in some cases less than 75 Ohm*um, or lower.

[0041] Figure 4 is a method for forming a transistor structure with low contact resistance in accordance with another embodiment of the present invention. Figures 5A through 5F illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments. In general, this method is similar to the method described with reference to Figures 2 and 3A-H, except that the deposition of the boron doped germanium layer 317/319 on the source/drain regions is carried out after the dielectric 322 is deposited and etched to form the contact trench. Thus, the method includes depositing 406 the dielectric 322 directly over the source/drain regions 318/320, and then continues with etching 408 to form the source/drain contact trench and then selectively deposting 410 the boron doped germanium layer 317/319 into the trench (and directly onto the source/drain regions 318/320), as best shown in Figures 5C through 5E. Deposting 410 can be carried out using any suitable deposition process, such as selective epitaxy. Once layer 317/319 is provided, the contact metals 325/327 can be provided on top of the layer 317/319, as shown in Figure 5F. This alternate methodology provides the same benefit of improved contact resistance, but is more selective in where the boron doped germanium is deposited. Other such selective deposition processes will be apparent in light of this disclosure, using any suitable combination of masking/patterning and selective deposition techniques.

[0042] As will be further appreciated, the previous relevant discussion with respect to similar parts of the method is equally applicable here. In particular, forming 402 a gate stack and defining 404 the source/drain regions of the transistor structure can be carried as previously discussed with reference to the forming 202 and defining 204 previously discussed with reference to Figure 2. Likewise, depositing 412 contact resistance reducing metal and annealing to form silicide/germanide, and then depositing 414 the source/drain contact plugs can be carried as previously discussed with reference to the forming 212 and defining 214 previously discussed with reference to Figure 2.

FinFET Configuration

[0043] As is known, FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin). The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, a source region, and a drain region. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both sidewalls of the fin (sides perpendicular to the substrate

surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate FinFET. Other types of FinFET configurations are also available, such as so-called double-gate FinFETs, in which the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin).

[0044] Figure 6 shows a perspective view of an example tri-gate architecture, configured in accordance with one embodiment of the present invention. As can be seen, the tri-gate device includes a substrate 600 having a semiconductor body or fin 660 (represented by dashed lines) extending from the substrate 600 through isolation regions 610, 620. A gate electrode 640 is formed over 3 surfaces of the fin 660 to form 3 gates. A hard mask 690 is formed on top of the gate electrode 640. Gate spacers 670, 680 are formed at opposite sidewalls of the gate electrode 640.

[0045] A source region comprises the epitaxial region 631 formed on a recessed source interface 650 and on one fin 660 sidewall, and a drain region comprises the epitaxial region 631 formed on a recessed source interface 650 and on the opposing fin 660 sidewall (not shown). A cap layer 641 is deposited over the epitaxial regions 631. Note that the boron cap layer 641 may be provided in the recessed (tip) regions, but in other embodiments is just provided over the source/drain regions (and not in the recessed regions). In one embodiment, the isolation regions 610, 620 are shallow trench isolation (STI) regions formed using conventional techniques, such as etching the substrate 600 to form trenches, and then depositing oxide material onto the trenches to form the STI regions. The isolation regions 610, 620 can be made from any suitable dielectric/insulative material, such as SiO_2. The previous discussion with respect to the substrate 102 is equally applicable here (e.g., substrate 600 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).

[0046] As will be appreciated in light of this disclosure, conventional processes and forming techniques can be used to fabricate the FinFET transistor structure. However, and in accordance with one example embodiment of the present invention, the bilayer structure of the epitaxial region 631 and cap layer 641 can be implemented, for instance, using an in situ doped silicon or SiGe (for 631) capped with a boron doped germanium (for 641), with an optional germanium and/or boron graded buffer between the two bilayers. As previously explained, such a buffer

may be used to transition from a base level germanium/boron concentration compatible with the epitaxial region 631 to the boron doped germanium cap 641. Alternatively, germanium and/or boron concentration grading can be implemented directly in the epitaxial region 631 and/or the cap 641, rather than in an intervening graded buffer arrangement. As will further be appreciated, note that an alternative to the tri-gate configuration is a double-gate architecture, which includes a dielectric/isolation layer on top of the fin 660.

[0047] Figure 7 shows a plot of a split lot showing contact resistance for transistor structures configured with in accordance with embodiments of the present invention and standard transistor structures configured with no cap. The transistor structures associated with the high resistance numbers in excess of 0.18 are all implemented with standard SiGe alloy raised PMOS source/drain regions with contact metal deposited directly thereon. The transistor structures associated with the resistance numbers of 0.107 and lower are all similarly implemented but with the addition a boron doped germanium cap between the source/drain regions and contact metal, in accordance with various embodiments of the present invention. Table 1 shows the raw data quantiles resulting from testing of the example structures with and without a boron doped germanium cap as described herein.

Ge Cap	Min	10%	25%	Median	75%	90%	Max
Yes	0.032	0.032	0.033	0.040	0.078	0.105	0.107
No	0.183	0.183	0.192	0.239	0.250	0.265	0.265

Table 1

As can be seen, this example lot actually shows an improvement (reduction) in contact resistance of about a three to six times (3X to 6X) over conventional transistor structures. The units are Ohms per arbitrary area.

[0048] Other improvements enabled by using a boron doped germanium cap in accordance with an embodiment of the present invention will be apparent in light of this disclosure. In particular, the resulting germanide materials and Schottky barrier height improvement enables more than a 2x R_{ext} improvement over that in conventional SiGe source/drain PMOS devices, in accordance with some example embodiments of the present invention. As is known, the Schottky barrier height is the barrier for electrical conduction across a semiconductor-metal junction. The magnitude of the Schottky barrier height reflects a mismatch in the energy position

of the metal's Fermi level and the majority carrier band edge of the semiconductor across the semiconductor-metal interface. For a p-type semiconductor-metal interface, the Schottky barrier height is the difference between the metal Fermi level and the valence band maximum of the semiconductor.

Example System

[0049] Figure 8 illustrates a computing device 1000 configured in accordance with one embodiment of the invention. As can be seen, the computing device 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board or a daughterboard mounted on a main board or the only board of device 1000, etc. Depending on its applications, computing device 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing device 1000 may include one or more transistor structures as described herein. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

[0050] The communication chip 1006 enables wireless communications for the transfer of data to and from the computing device 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE

802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0051] The processor 1004 of the computing device 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments of the present invention, the integrated circuit die of the processor includes an onboard non-volatile memory or cache, and/or is otherwise communicatively coupled to off-chip memory that is implemented with one or more transistor structures as described herein. The term "processor" may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0052] The communication chip 1006 may also include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more devices implemented with one or more transistor structures as described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

[0053] In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder.

In further implementations, the device 1000 may be any other electronic device that processes data or employs transistors.

[0054] Numerous embodiments will be apparent in light of this disclosure, and features described herein can be combined in any number of configurations. One example embodiment of the present invention provides a transistor device. The device includes a substrate having a channel region, and a gate electrode above the channel region. A gate dielectric layer is provided between the gate electrode and the channel region, and source and drain regions are provided in the substrate and adjacent to the channel region. The device further includes a boron doped germanium layer on at least a portion of the source and drain regions. This boron doped germanium layer comprises a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}. The device further includes metal-germanide source and drain contacts on the boron doped germanium layer. In one such example, the device is one of a planar or FinFET transistor. In another example case, the device comprises a PMOS transistor. In another example case, the device further includes an interlayer dielectric. In another example case, the device further includes a graded buffer between the substrate and the source and drain regions and/or a graded buffer between the source and drain regions and the boron doped germanium layer. In one such case, the graded buffer between the source and drain regions and the boron doped germanium layer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %. In one such specific example case, the high concentration reflects pure germanium. In another example case, the graded buffer between the source and drain regions and the boron doped germanium layer has a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron. In another example case, the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %. In another example case, the source and drain regions comprise boron doped silicon germanium having a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}. In another

example case, the source and drain regions comprise silicon or silicon germanium, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}. In another example case, the boron doped germanium layer comprises a germanium concentration in excess of 98 atomic %, and a boron concentration in excess of 2E20 cm^{-3}. Another embodiment provides an electronic device that includes a printed circuit board having one or more integrated circuits, wherein at least one of the one or more integrated circuits comprises one or more transistor devices as variously defined in in this paragraph. In one such case, the one or more integrated circuits includes at least one of a communication chip and/or a processor, and at least one of the communication chip and/or processor comprises the one or more transistor devices. In another such case, the device is a computing device (e.g., mobile telephone or smartphone, laptop, tablet computer, etc).

[0055] Another embodiment of the present invention provides a transistor device. In this example case, the device includes a substrate having a channel region, and a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The device further includes source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers. The device further includes a boron doped germanium layer on at least a portion of the source and drain regions, and comprising a germanium concentration in excess of 95 atomic % and a boron concentration in excess of 2E20 cm^{-3}. The device further includes metal-germanide source and drain contacts on the boron doped germanium layer. The device is one of a planar or FinFET transistor. In one such example case, the device further includes a buffer between the source and drain regions and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}. In another example

case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron. In another example case, the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 98 atomic %. In another example case, the source and drain regions have a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}. In another example case, the source and drain regions comprise silicon germanium having a fixed germanium concentration, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms. Another embodiment provides a computing device (e.g., desktop or portable computer, etc) that includes a printed circuit board having a communication chip and/or a processor, wherein at least one of the communication chip and/or processor comprises one or more transistor devices as variously defined in this paragraph.

[0056] Another embodiment of the present invention provides a method for forming a transistor device. The method includes providing a substrate having a channel region, and providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region. The method continues with providing source and drain regions in the substrate and adjacent to the channel region, and providing a boron doped germanium layer on at least a portion of the source and drain regions. The boron doped germanium layer comprises a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}. The method continues with providing metal-germanide source and drain contacts on the boron doped germanium layer. In some example such cases, the method further includes providing a graded buffer between the substrate and the source and drain regions, and/or providing a graded buffer between the source and drain regions and the boron doped germanium layer. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron (which may be used with or

without graded buffers). This method may be employed, for example, in the fabrication of any electronic devices such as a computing device.

[0057] The foregoing description of example embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

CLAIMS

What is claimed is:

1. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region;

source and drain regions in the substrate and adjacent to the channel region;

a boron doped germanium layer on at least a portion of the source and drain regions, and comprising a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}; and

metal-germanide source and drain contacts on the boron doped germanium layer.

2. The device of claim 1 wherein the device is one of a planar or FinFET transistor.

3. The device of claims 1 or 2 wherein the device comprises a PMOS transistor.

4. The device of any of the preceding claims further comprising an interlayer dielectric.

5. The device of the preceding claims, further comprising at least one of:

a graded buffer between the substrate and the source and drain regions; and

a graded buffer between the source and drain regions and the boron doped germanium layer.

6. The device of claim 5 wherein the graded buffer between the source and drain regions and the boron doped germanium layer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %.

7. The device of claim 6 wherein the high concentration reflects pure germanium.

8. The device of claims 5, 6, or 7 wherein the graded buffer between the source and drain regions and the boron doped germanium layer has a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}.

9. The device of any of the preceding claims wherein the boron doped germanium layer has a graded concentration of at least one of germanium and boron.

10. The device of any of the preceding claims wherein the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %.

11. The device of any of the preceding claims wherein the source and drain regions comprise boron doped silicon germanium having a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

12. The device of any of claims 1 through 4 wherein the source and drain regions comprise silicon or silicon germanium, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}.

13. The device of any of the preceding claims wherein the boron doped germanium layer comprises a germanium concentration in excess of 98 atomic %, and a boron concentration in excess of 2E20 cm^{-3}.

14. An electronic device comprising:

a printed circuit board having one or more integrated circuits, wherein at least one of the one or more integrated circuits comprises one or more transistor devices as defined in any of the preceding claims.

15. The electronic device of claim 14 wherein the one or more integrated circuits includes at least one of a communication chip and/or a processor, and at least one of the communication chip and/or processor comprises the one or more transistor devices.

16. The electronic device of claims 14 or 15 wherein the device is a computing device.

17. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers;

a boron doped germanium layer on at least a portion of the source and drain regions, and comprising a germanium concentration in excess of 95 atomic % and a boron concentration in excess of 2E20 cm^{-3}; and

metal-germanide source and drain contacts on the boron doped germanium layer;

wherein the device is one of a planar or FinFET transistor.

18. The device of claim 17, the device further comprising:

a buffer between the source and drain regions and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}.

19. The device of claim 17 wherein the boron doped germanium layer has a graded concentration of at least one of germanium and boron.

20. The device of claim 17 wherein the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 98 atomic %.

21. The device of claim 20 wherein the source and drain regions have a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

22. The device of claim 17 wherein the source and drain regions comprise silicon germanium having a fixed germanium concentration, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms.

23. A method for forming a transistor device, comprising:

providing a substrate having a channel region;

providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region; and

providing source and drain regions in the substrate and adjacent to the channel region;

providing a boron doped germanium layer on at least a portion of the source and drain regions, the boron doped germanium layer comprising a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}; and

providing metal-germanide source and drain contacts on the boron doped germanium layer.

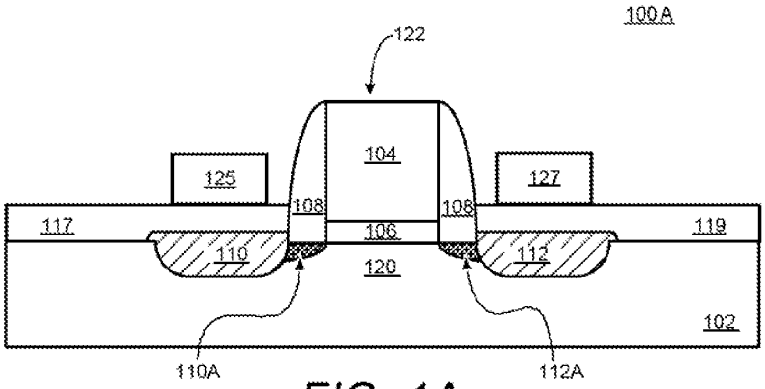


FIG. 1A

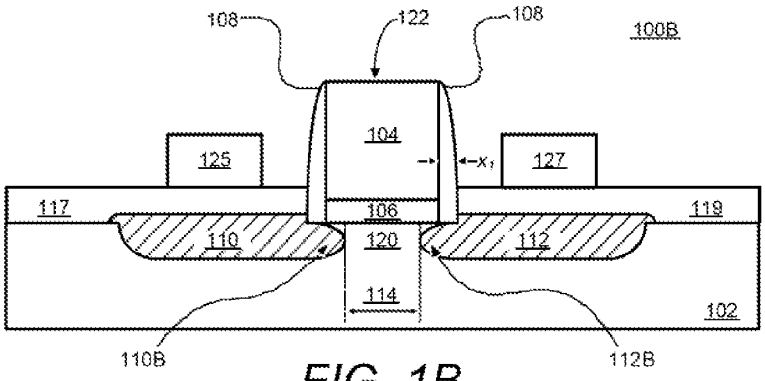


FIG. 1B

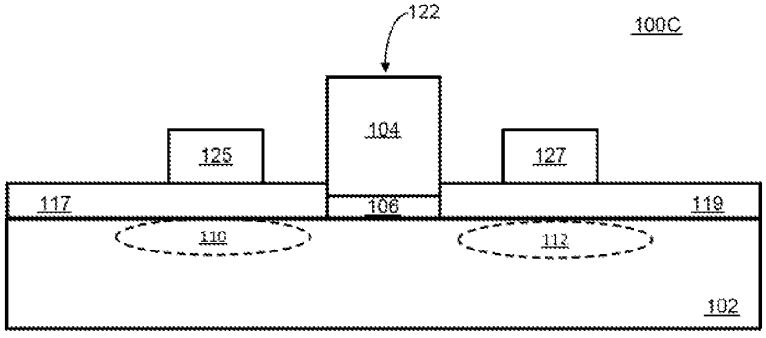


FIG. 1C

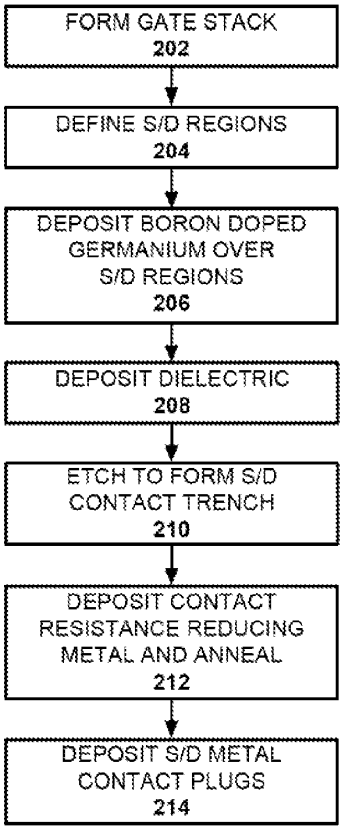

FORM GATE STACK
202
DEFINE S/D REGIONS
204
DEPOSIT BORON DOPED GERMANIUM OVER S/D REGIONS
206
DEPOSIT DIELECTRIC
208
ETCH TO FORM S/D CONTACT TRENCH
210
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
212
DEPOSIT S/D METAL CONTACT PLUGS
214

FIG. 2

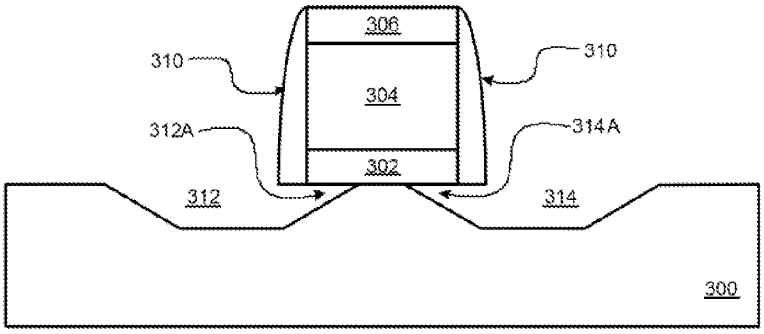


FIG. 3A

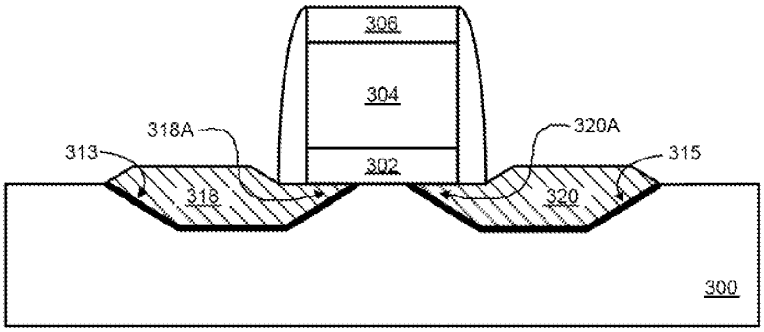


FIG. 3B

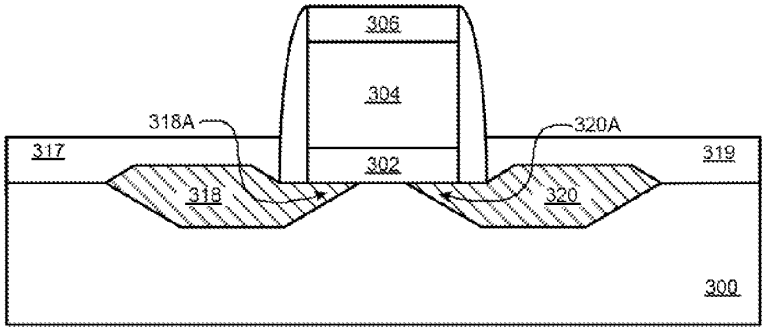


FIG. 3C

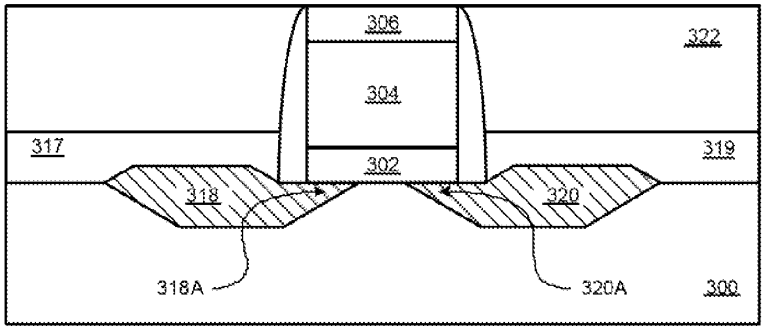


FIG. 3D

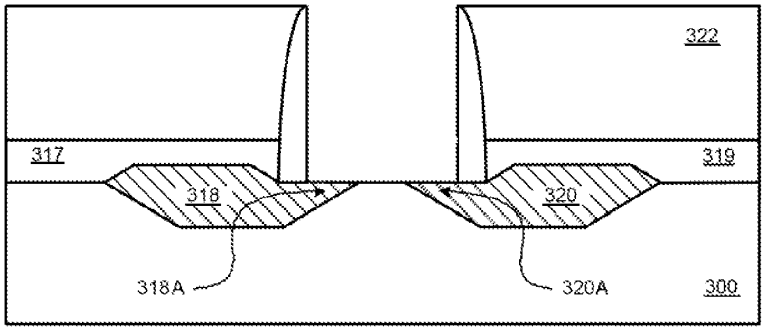


FIG. 3E

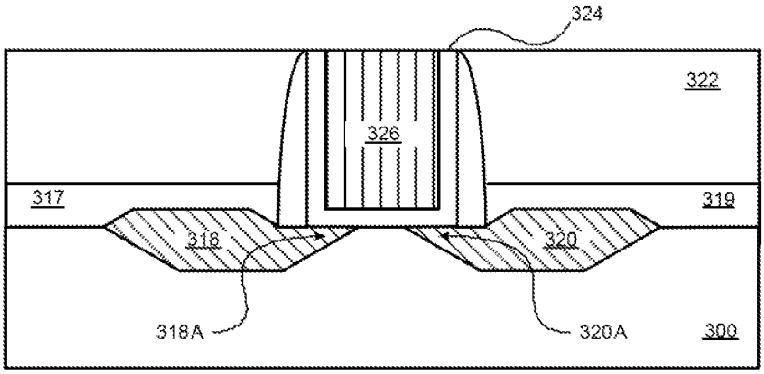


FIG. 3F

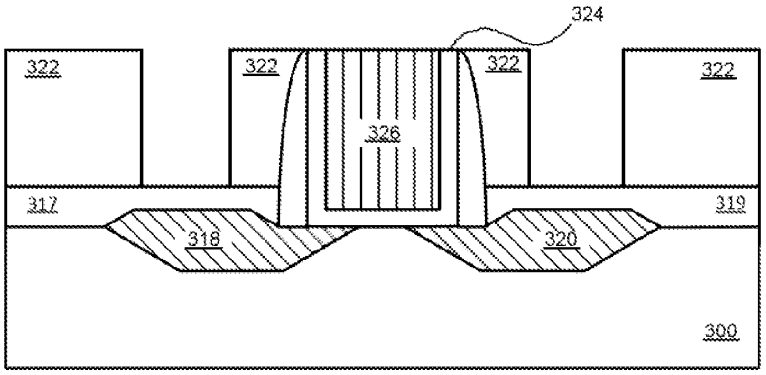


FIG. 3G

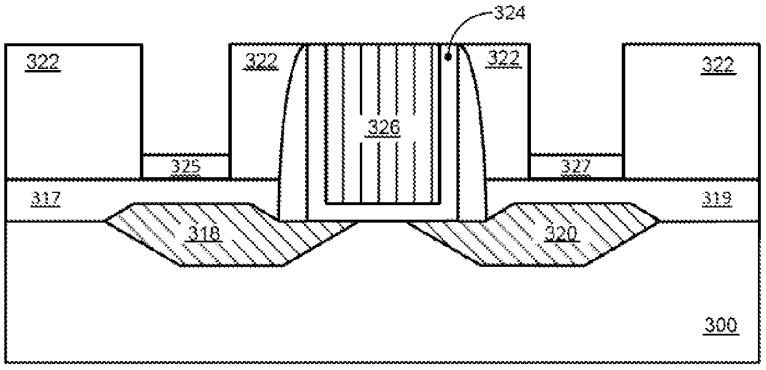


FIG. 3H

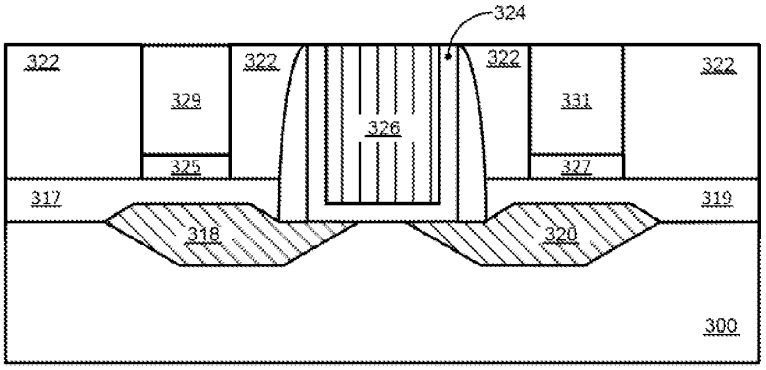


FIG. 3I

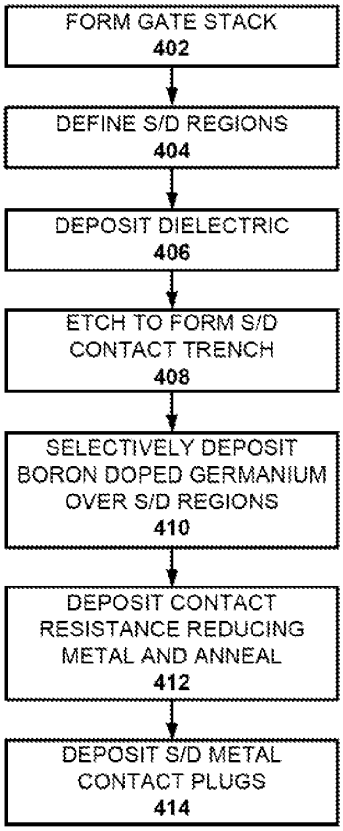

FORM GATE STACK
402
DEFINE S/D REGIONS
404
DEPOSIT DIELECTRIC
406
ETCH TO FORM S/D CONTACT TRENCH
408
SELECTIVELY DEPOSIT BORON DOPED GERMANIUM OVER S/D REGIONS
410
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
412
DEPOSIT S/D METAL CONTACT PLUGS
414

FIG. 4

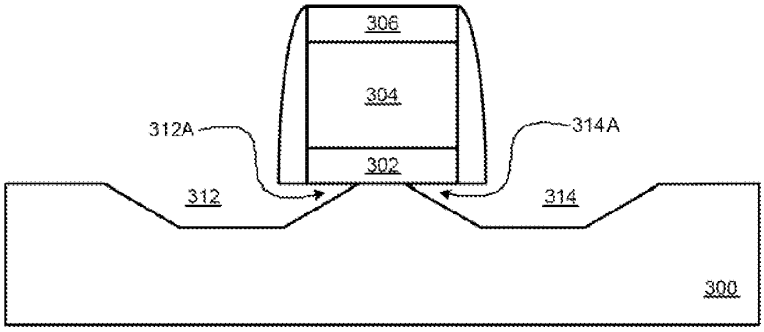


FIG. 5A

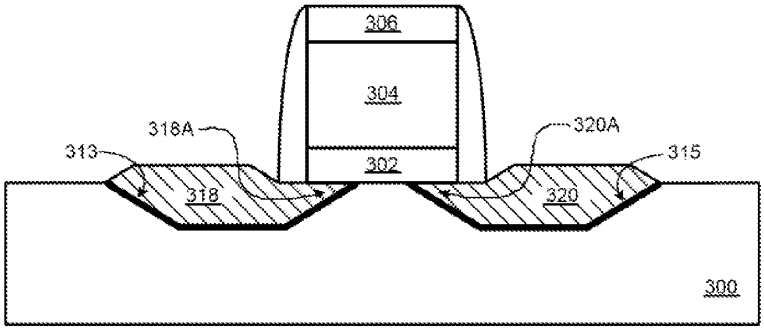


FIG. 5B

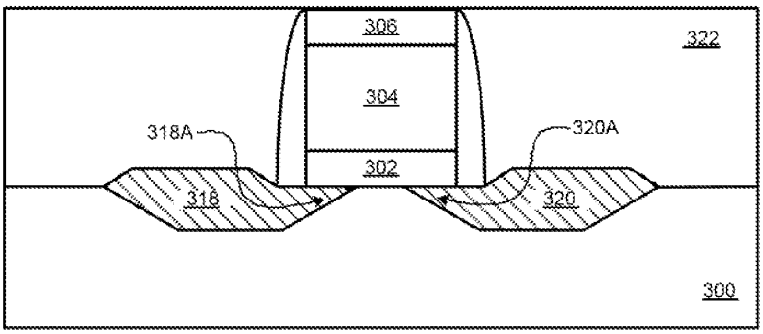


FIG. 5C

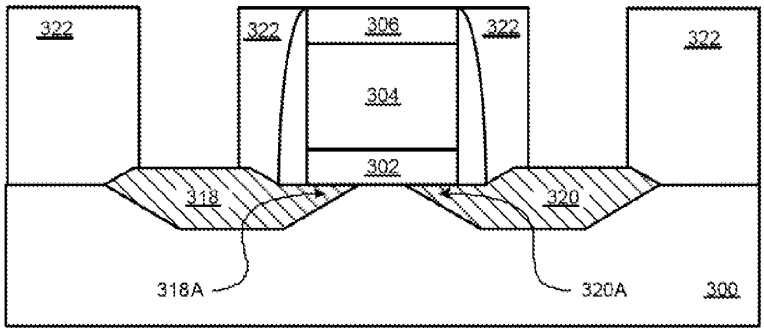


FIG. 5D

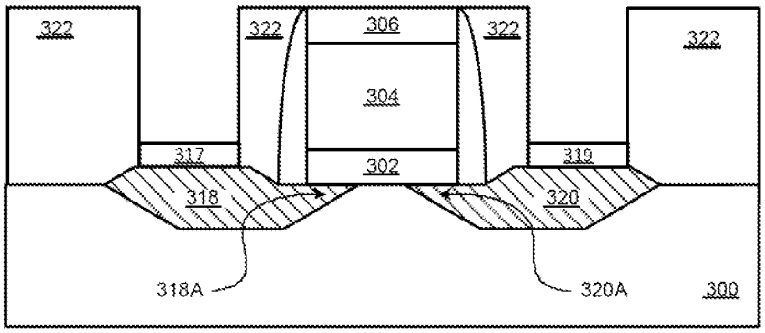


FIG. 5E

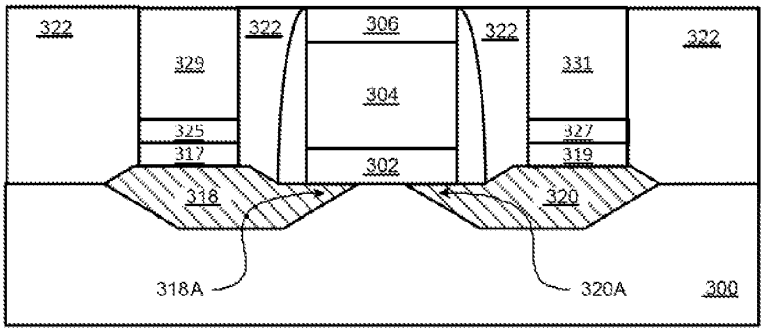


FIG. 5F

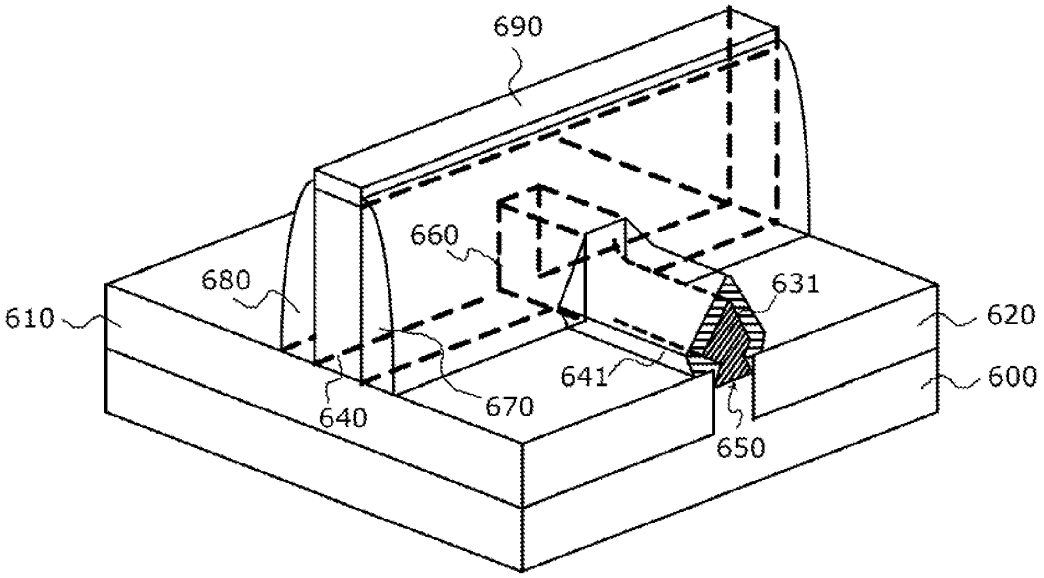


FIG. 6

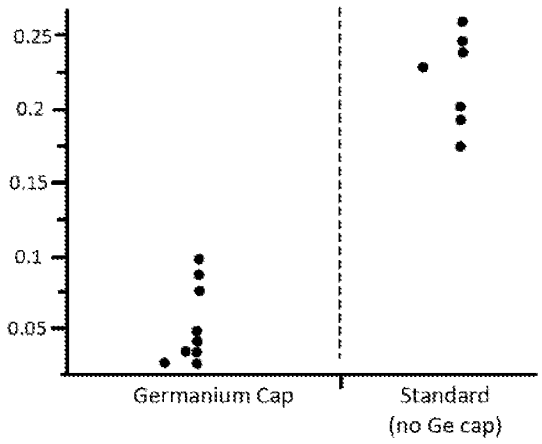


FIG. 7

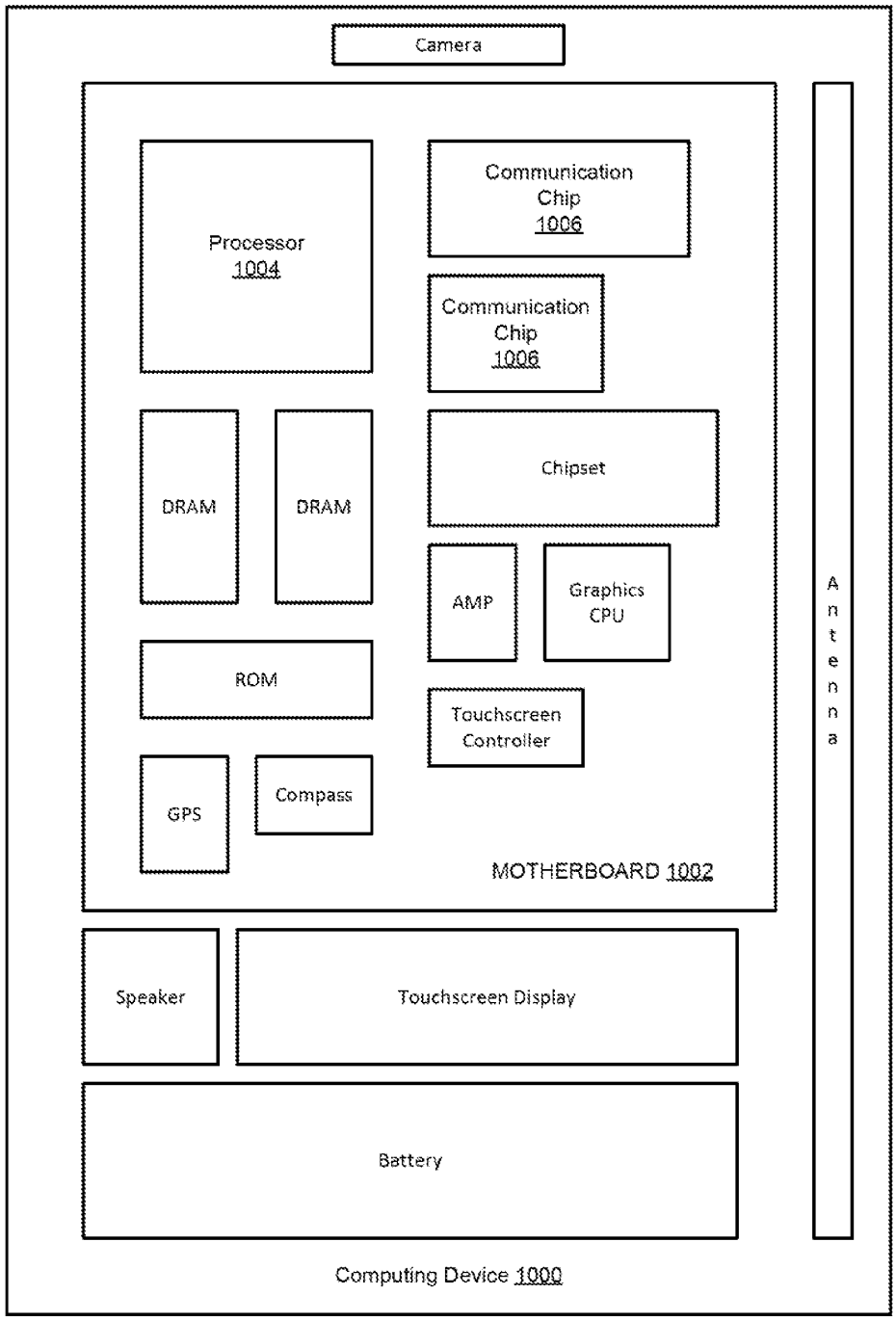

Camera
Processor
1004
Communication
Chip
1006
Communication
Chip
1006
DRAM
DRAM
Chipset
AMP
Graphics
CPU
ROM
Touchscreen
Controller
GPS
Compass
MOTHERBOARD 1002
Antenna
Speaker
Touchscreen Display
Battery
Computing Device 1000

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/054198

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; G11B 5/00; G11B 20/20; H01L 21/20; H01L 21/336; H01L 29/94

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: germanium, boron, transistor, printed circuit board, contact resistance, doping

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2007-0187767 A1 (YASUTAKE, NOBUAKI) 16 August 2007 See abstract; paragraphs[0020]-[0090]; figs.1,9,16	1-13,23 14-16,17-22
Y	US 2006-0156080 A1 (TELLKAMP, JOHN P. et al.) 13 July 2006 See abstract; paragraphs[0014]-[0031]; figs.1,2	14-16
Y	US 2010-0148217 A1 (SIMONELLI, DANIELLE et al.) 17 June 2010 See abstract; paragraphs[0037]-[0043]; figs.4,5	17-22
A	US 2008-0135878 A1 (KIM, SANG HUN et al.) 12 June 2008 See abstract; paragraphs[0024]-[0038]; figs.2A-2H,3	1-23

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 APRIL 2012 (18.04.2012)	**19 APRIL 2012 (19.04.2012)**

Name and mailing address of the ISA/KR	Authorized officer
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Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-8708

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/054198

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0187767 A1	16.08.2007	JP 2007-214481 A	23.08.2007
		US 2010-0244154 A1	30.09.2010
		US 7880228 B2	01.02.2011
US 2006-0156080 A1	13.07.2006	None	
US 2010-0148217 A1	17.06.2010	CN 102171794 A	31.08.2011
		EP 2356670 A2	17.08.2011
		KR 10-2011-0050713 A	16.05.2011
		TW 201036044 A	01.10.2010
		US 7902009 B2	08.03.2011
		WO 2010-068530 A2	17.06.2010
		WO 2010-068530 A3	17.06.2010
US 2008-0135878 A1	12.06.2008	KR 10-0817217 B1	27.03.2008
		US 7550796 B2	23.06.2009

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(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

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(54) Title: SELECTIVE GERMANIUM P-CONTACT METALIZATION THROUGH TRENCH

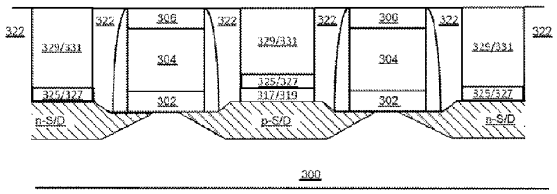


FIG. 5F

(57) Abstract: Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on, for example, silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and suitable fabrication processes will be apparent in Sight of this disclosure, including both planar and non-planar transistor structures {e.g., FinFETs), as well as strained and unstrained channel structures. Graded buffering can be used to reduce misfit dislocation. The techniques are particularly well-suited for implementing p-type de vices, but can be used for n-type de vices if so desired.

WO 2012/087404 A1

SELECTIVE GERMANIUM P-CONTACT METALIZATION THROUGH TRENCH

RELATED APPLICATION

[0001] This application is a continuation-in-part of U.S. Application No. 12/975,278 filed December 21, 2010.

BACKGROUND

[0002] Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to minimize the parasitic resistance associated with contacts otherwise known as external resistance R_{ext}. Decreased R_{ext} enables higher current from an equal transistor design.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1A illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention.

[0004] Figure 1B illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0005] Figure 1C illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0006] Figure 2 is a method for forming a transistor structure with low contact resistance in accordance with an embodiment of the present invention.

[0007] Figures 3A to 3I illustrate structures that are formed when carrying out the method of Figure 2, in accordance with various embodiment of the present invention.

[0008] Figure 4 is a method for forming a transistor structure with low contact resistance in accordance with another embodiment of the present invention.

[0009] Figures 5A to 5F illustrate structures that are formed when carrying out the method of Figure 4, in accordance with various embodiment of the present invention.

[0010] Figure 6 shows a perspective view of a FinFET transistor architecture, configured in accordance with one embodiment of the present invention.

[0011] Figure 7 shows a plot of a split lot showing contact resistance for transistor structures configured with in accordance with embodiments of the present invention and standard transistor structures configured with no cap.

[0012] Figure 8 illustrates a computing system implemented with one or more transistor structures in accordance with an example embodiment of the present invention.

[0013] As will be appreciated, the figures are not necessarily drawn to scale or intended to limit the claimed invention to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of a transistor structure may have less than perfect straight lines, right angles, and some features may have surface topology or otherwise be non-smooth, given real world limitations of the processing equipment and techniques used. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

[0014] Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and

suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures. The techniques are particularly well-suited for implementing p-type devices, but can be used for n-type devices if so desired.

General Overview

[0015] As previously explained, increased drive current in the transistors can be achieved by reducing device resistance. Contact resistance is one component of a device's overall resistance. A standard transistor contact stack typically includes, for example, a silicon or SiGe source/drain layer, a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad. In such configurations, the contact resistance is effectively limited by the silicon or SiGe valence band alignment to the pinning level in the metal. Typically, using industry standard silicides such as nickel (or other suitable silicides, such as titanium, cobalt, or platinum), this results in a band misalignment of about 0.5 eV. Thus, and in accordance with an example embodiment of the present invention, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce the band misalignment value and contact resistance.

[0016] In one specific example embodiment, contacts configured with the intermediate boron doped germanium layer exhibit a reduction in the band misalignment value to less than 0.2 eV and a corresponding reduction in contact resistance of about 3X (relative to a conventional contact stack similarly configured, but without the intermediate boron doped germanium layer between the source/drain regions and contact metal). A transmission electron microscopy (TEM) cross section or secondary ion mass spectrometry (SIMS) profile can be used to show the germanium concentration throughout the vertical stack of the film structure, as profiles of epitaxial alloys of silicon and SiGe can readily be distinguished from germanium concentration profiles.

[0017] Thus, transistor structures configured in accordance with embodiments of the present invention provide an improvement over conventional structures with respect to lower contact resistance. Some such embodiments effectively marry superior contact properties of germanium with superior semiconductor transistor properties of Si and SiGe to provide next generation low resistance contacts. Selectivity can be achieved in various ways. In one embodiment, for instance, selectivity to n-type MOS (NMOS) source/drain locations can be provided by having

NMOS regions masked off during p-type MOS device (PMOS) deposition. In another embodiment, both NMOS and PMOS regions can be open simultaneously, but deposition only occurs in the PMOS regions by way of a trench. An advantage here is that the low melting point germanium is absent during the relatively high thermal budget steps typical in the front end of a MOS flow. After trench processing and germanium deposition, and in accordance with one specific such example embodiment, the structure sees no temperatures above 500°C, and therefore the germanium overlayer is not in jeopardy of melting and or otherwise degrading performance. As will be further appreciated in light of this disclosure, selectively may include natural selectivity. For instance, while boron doped germanium grows on p-type SiGe (or silicon) source drain regions, it does not grow on dielectric surfaces such as silicon dioxide (SiO_2) or silicon nitride (SiN); nor does it grow on, for instance, exposed heavily phosphorous doped silicon in n-type regions.

[0018] Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., such as double-gate and trigate transistor structures), as well as strained and unstrained channel structures. Any number of such structural features and material systems can be used in conjunction with a germanium overlayer as described herein. The transistor structure may include p-type source/drain regions, n-type source/drain regions, or both n-type and p-type source/drain regions. In some example embodiments, the transistor structure includes dopant-implanted source/drain regions or epitaxial (or poly) replacement source/drain regions of silicon, SiGe alloys, or nominally pure germanium films (e.g., such as those with less than 10% silicon) in a MOS structure. In any such implementations, an overlayer or cap of boron doped germanium can be formed directly over the source/drain regions, in accordance with an embodiment of the present invention. A contact metal (or series of metals) can then be deposited and a subsequent reaction (annealing) can be carried out to form metal germanide source and drain contacts. As will be appreciated, the contact may be implemented as a stack including one or more of a silicide layer, an adhesion layer, and/or a metal pad layer. The boron doped germanium overlayer can be formed directly over other parts of the transistor structure as well, such as the poly gate and/or grounding tap regions, if so desired.

[0019] As is known, a MOS transistor may include source and drain tip regions that are designed to decrease the overall resistance of the transistor while improving short channel effects

(SCE). Conventionally, these tip regions are portions of the substrate where a dopant such as boron or carbon is implanted using an implant and diffusion technique. The source tip region is formed in the area between the source region and the channel region. Likewise, the drain tip region is formed in the area between the drain region and the channel region. Some embodiments of the present invention are configured with such conventionally formed tip regions. In other example embodiments, fabrication techniques are employed to extend self-aligned epitaxial tip (SET) transistors to achieve very near to the theoretical limit of uniaxial strain. This can be accomplished, for instance, by selective epitaxial deposition in the source and drain regions as well as their corresponding tip regions to form a bilayer construction of boron doped silicon or SiGe (for the source/drain regions) capped with an overlayer of a boron doped germanium layer in the source/drain and respective tip regions. The germanium and boron concentrations can vary, but in some example embodiments, the germanium concentration is in the range of 20 atomic % to 100 atomic %, and the boron concentration is in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., germanium concentration in excess of 50 atomic % and boron concentration in excess of 2E20 cm^{-3}). Note that the boron doped germanium layer may be provided in the tip regions, but in other embodiments is just provided over the source/drain regions (and not in the tip regions).

[0020] In still other example embodiments, an optional thin buffer with graded germanium concentration and/or boron concentration can be used as an interfacial layer between the underlying substrate with the source/drain layer (e.g., silicon or SiGe). Likewise, a thin buffer with graded germanium concentration and/or boron concentration can be used as an interfacial layer between the source/drain layer and the boron doped germanium cap. In still other embodiments, the boron doped germanium overlayer or source/drain layer themselves can have a graded germanium and/or boron concentration in a similar fashion as to the optional buffers. In any such case, since boron diffusion is suppressed in germanium (the higher the concentration, the greater the relative suppression), a high concentration of boron can be doped in the germanium, which in turn results in lower parasitic resistance and without degrading tip abruptness. In addition, the contact resistance is reduced from lowering of Schottky-barrier height.

Architecture and Methodology

[0021] Figure 1A illustrates a MOS device 100A formed on a substrate 102 and configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention. In particular, boron doped germanium layer 117 is provided between the source layer 110 and contact metals 125, and boron doped germanium layer 119 is provided between the drain layer 112 and contact metals 127. The source region 110 and the drain region 112 can be formed using any number of conventional techniques. In this example embodiment, for instance, the source region 110 and the drain region 112 are formed by etching the substrate and then epitaxially depositing a silicon or silicon germanium material (e.g., with a germanium concentration in the range of, for instance, 10 to 70 atomic %).

[0022] A gate stack 122 is formed over a channel region 120 of the transistor 100A. As can further be seen, the gate stack 122 includes a gate dielectric layer 106 and a gate electrode 104, and spacers 108 are formed adjacent to the gate stack 122. In some example cases, and depending on the technology node, the spacers 108 create a distance of about 10 to 20 nanometers (nm) between the edges of the gate dielectric layer 106 and the edges of each of the source and drain regions 110/112. It is within this space that a source tip region 110A and a drain tip region 112A can be formed. In this example embodiment, the tip regions 110A/112A are formed via a typical implantation-diffusion based process, and overlap the spacers 108 and may also overlap or underdiffuse the gate dielectric layer 106 by a distance of, for instance, less than 10 nm. In forming the implantation-diffusion based tip regions 110A/112A, a dopant such as boron or carbon is implanted into the source region 110 and the drain region 112. The transistor 100A is then annealed to cause the dopant to diffuse towards the channel region 120. Angled ion implantation techniques may also be used to further implant dopants into those areas between the gate dielectric layer 106 and the source/drain regions 110/112. Such implantation-diffusion-based tip formation processes generally do not induce a strain on the channel region.

[0023] In any case, and as will be appreciated in light of this disclosure, whether a transistor structure has a strained or unstrained channel, or source-drain tip regions or no source-drain tip regions, is not particularly relevant to various embodiments of the present invention, and such embodiments are not intended to be limited to any particular such structural features. Rather, any number of transistor structures and types can benefit from employing a boron doped

germanium overlayer as described herein. The techniques provided herein are compatible, for instance, with conventional dopant implanted silicon, raised source/drain, strained SiGe (or other suitable materials), and any deposited epitaxial tip (sometimes referred to as source-drain extensions) that extend below the gate electrode dielectric or are spaced away from the vertical line defined by the gate electrode dielectric.

[0024] The germanium overlayer 117/119 is generally provided after formation of the source/drain regions 110/112 and prior to formation of the contacts 125/127. The thickness of this overlayer 117/119 can vary from one embodiment to the next, but in one example embodiment is in the range of 50 to 250 Angstroms (Å). The boron concentration of overlayer 117/119 can also vary, but in one example embodiment is in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., in excess of 2E20 cm^{-3}). The overlayer 117/119 can be selectively deposited over the source/drain 110/112 regions (and/or other regions as desired, such as the poly gate or grounding tap regions). Any number of suitable deposition techniques can be used to provide the overlayer 117/119 (e.g., chemical vapor deposition, molecular beam epitaxy, etc). In accordance with one example embodiment, the contact metals 125 and 127 each comprise a stack a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad, and although any number of contact metal configurations can be used as will be appreciated in light of this disclosure. Standard deposition techniques can be used in providing the contact metals 125/127.

[0025] Figure 1B illustrates an example MOS device 100B formed on a substrate 102 and configured with a boron doped germanium layer 117/119 between the source/drain layer 110/112 and contact metals 125/127, in accordance with another embodiment of the present invention. This example configuration includes source and drain epitaxial tips (generally referred to herein as epi-tips). In more detail, the MOS transistor 100B uses an undercut etch to allow the source region 110 and the drain region 112 to extend below the spacers 108, and in some cases, below the gate dielectric layer 106. The portions of the source/drain regions 110/112 that extend below the spacers 108 (and possibly the gate dielectric layer 106) are generally referred to as the source epi-tip 110B and the drain epi-tip 112B, respectively. The source and drain epi-tips 110B/112B replace the implantation/diffusion based tip regions 110A/112A described with regard to Figure 1A. In accordance with one embodiment, the source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be formed, for example, by etching the substrate 102, which includes undercutting the spacers 108 (and possibly the gate dielectric layer 106), and then using selective

epitaxial deposition to provide, for instance, an in situ doped silicon, germanium, or SiGe to fill the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, as shown in Figure 1B. Note the epitaxial fill may be raised relative to the surface of substrate 102, as further shown in Figure 1B, although non-raised configurations can be used as well. The germanium overlayer 117/119 and the contact metals 125/127 can be implemented, for instance, as previously described with respect to Figure 1A.

[0026] Figure 1C illustrates a MOS device 100C formed on a substrate 102 and configured with boron doped germanium layers 117/119 between the respective source/drain layers 110/112 and contact metals 125/127, in accordance with another embodiment of the present invention. The source region 110 and the drain region 112 in this example embodiment are formed by implanting dopants such as boron into the substrate. The gate stack 122 is formed over a channel region 120 of the transistor 100C and is this example case does not include sidewalls 108. Nor does this example transistor structure include an undercut or tip regions like the embodiments shown in Figures 1A and 1B. The germanium overlayer 117/119 and the contact metals 125/127 can be implemented, for instance, as previously described with respect to Figure 1A.

[0027] Numerous other variations and features can be implemented for transistor structures configured in accordance with an embodiment of the present invention. For example, a graded buffer may be used in one or more locations of the structure. For instance, the substrate 102 can be a silicon substrate, or a silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate comprising silicon, silicon germanium, germanium, and/or III-V compound semiconductors. Thus, and by way of example, in an embodiment having a silicon or silicon germanium substrate 102 and an in situ boron doped SiGe fill in the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, a buffer can be provided between the underlying substrate 102 and the source/drain material. In one such embodiment, the buffer can be a graded boron doped (or intrinsic) silicon germanium layer with the germanium concentration graded from a base level compatible with the underlying substrate up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). The boron concentration within this buffer can be either fixed (e.g., at a high level) or graded, for instance, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 2E20 cm^{-3}). Note that 'compatibility' as used herein does not necessitate an overlap in concentration levels (for

instance, the germanium concentration of underlying substrate can be 0 to 20 atomic % and initial germanium concentration of the buffer can be 30 to 40 atomic %). In addition, as used herein, the term 'fixed' with respect to a concentration level is intended to indicate a relatively constant concentration level (e.g., the lowest concentration level in the layer is within 10% of the highest concentration level within that layer). In a more general sense, a fixed concentration level is intended to indicate the lack of an intentionally graded concentration level. The thickness of the buffer can vary depending on factors such as the range of concentrations being buffered, but in some embodiments is in the range of 30 to 120 Å, such as 50 to 100 Å (e.g., 60 Å or 65 Å). As will be further appreciated in light of this disclosure, such a graded buffer beneficially lowers the Schottky-barrier height.

[0028] Alternatively, rather than using a thin buffer between the substrate 102 and the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, the source/drain material itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, boron doped SiGe source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to 70 atomic %) up to 100 atomic %. In some such embodiments, the boron concentration within this boron doped germanium layer can range, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 2E20 cm^{-3}).

[0029] In other embodiments, a buffer can be provided between the source/drain material and the boron doped germanium overlayer 117/119. In one such embodiment, the source/drain material is a boron doped SiGe layer having a fixed concentration of germanium (e.g., in the range of 30 to 70 atomic %) and the buffer can be a thin SiGe layer (e.g., 30 to 120 Å, such as 50 to 100 Å) having a germanium concentration graded from a base level concentration compatible with the underlying boron doped SiGe layer up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). In some such cases, the boron concentration within this buffer can be fixed at a desired high level or can range, for example, from a base concentration at or otherwise compatible with the underlying SiGe layer up to the desired high concentration (e.g., in excess of 1E20 cm^{-3}, 2E20 cm^{-3}, or 3E20 cm^{-3}). Alternatively, rather than using a buffer between the source/drain material and the boron doped

germanium overlayer 117/119, the overlayer 117/119 itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, the boron doped overlayer 117/119 can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate and/or source/drain regions (e.g., in the range of 30 to 70 atomic %) up to 100 atomic % (or near 100 atomic %). The boron concentration within this overlayer 117/119 layer can be fixed at a desired high level or can range, for example, from a base concentration at or otherwise compatible with the underlying substrate and/or source/drain regions up to the desired high level (e.g., in excess of 2E20 cm^{-3}).

[0030] Thus, a low contact resistance architecture for numerous transistor devices is provided. The devices may be formed in part using any number of conventional processes such as, for example, by gate oxide, poly gate electrode, thin spacer, and an isotropic undercut etch in the source/drain regions (or an ammonia etch to form faceted fin recess in monocrystalline substrate, or other suitable etch to form fin recess). In accordance with some embodiments, selective epitaxial deposition can be used to provide in situ doped silicon or alternatively, a fully strained silicon germanium layer to form source/drain regions with or without tips. Optional buffers may be used as previously explained. Any suitable high-k replacement metal gate (RMG) process flow can also be used, where a high-k dielectric replaces the conventional gate oxide. Silicidation with, for example, nickel, nickel-platinum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. The techniques provided herein can be applied, for example, to benefit any technology nodes (e.g., 90nm, 65nm, 45nm, 32nm, 22nm, 14nm, and 10nm transistors, and lower), and the claimed invention is not intended to be limited to any particular such nodes or range of device geometries. Other advantages will be apparent in light of this disclosure.

[0031] Figure 2 is a method for forming a transistor structure with low contact resistance in accordance with an embodiment of the present invention. Figures 3A through 3I illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments.

[0032] As can be seen, the method begins with forming 202 a gate stack on a semiconductor substrate upon which a MOS device, such as a PMOS transistor, may be formed. The semiconductor substrate may be implemented, for example, with a bulk silicon or a silicon-on-insulator configuration. In other implementations, the semiconductor substrate may be formed

using alternate materials, which may or may not be combined with silicon, such as germanium, silicon germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. In a more general sense, any material that may serve as a foundation upon which a semiconductor device may be built can be used in accordance with embodiments of the present invention. The gate stack can be formed as conventionally done or using any suitable custom techniques. In some embodiments of the present invention, the gate stack may be formed by depositing and then patterning a gate dielectric layer and a gate electrode layer. For instance, in one example case, a gate dielectric layer may be blanket deposited onto the semiconductor substrate using conventional deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Alternate deposition techniques may be used as well, for instance, the gate dielectric layer may be thermally grown. The gate dielectric material may be formed, for example, from materials such as silicon dioxide or high-k dielectric materials. Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some specific example embodiments, the high-k gate dielectric layer may be between around 5 Å to around 200 Å thick (e.g., 20 Å to 50 Å). In general, the thickness of the gate dielectric layer should be sufficient to electrically isolate the gate electrode from the neighboring source and drain contacts. In further embodiments, additional processing may be performed on the high-k gate dielectric layer, such as an annealing process to improve the quality of the high-k material. Next, a gate electrode material may be deposited on the gate dielectric layer using similar deposition techniques such as ALD, CVD, or PVD. In some such specific embodiments, the gate electrode material is polysilicon or a metal layer, although other suitable gate electrode materials can be used as well. The gate electrode material, which is may be a sacrificial material that is later removed for a replacement metal gate (RMG) process, has a thickness in the range of 50Å to 500Å (e.g., 100Å), in some example embodiments. A conventional patterning process may then be carried out to etch away portions of the gate electrode layer and the gate dielectric layer to form the gate stack, as shown in Figure 3A. As can be seen, Figure 3A illustrates a substrate 300 upon which a gate stack is formed. In this

example embodiment, the gate stack includes a gate dielectric layer 302 (which may be high-k gate dielectric material) and a sacrificial gate electrode 304. In one specific example case, the gate stack includes a silicon dioxide gate dielectric layer 302 and a polysilicon gate electrode 304. The gate stack may also include a gate hard mask layer 306 that provides certain benefits or uses during processing, such as protecting the gate electrode 304 from subsequent ion implantation processes. The hard mask layer 306 may be formed using typical hard mask materials, such as such as silicon dioxide, silicon nitride, and/or other conventional dielectric materials. Figure 3A further illustrates spacers 310 formed on either side of the stack. The spacers 310 may be formed, for example, using conventional materials such as silicon oxide, silicon nitride, or other suitable spacer materials. The width of the spacers 310 may generally be chosen based on design requirements for the transistor being formed. In accordance with some embodiments, however, the width of the spacers 310 is not subject to design constraints imposed by the formation of the source and drain epi-tips, given sufficiently high boron doped germanium content in the source/drain tip regions, as described herein (boron won't diffuse into channel).

[0033] With further reference to Figure 2, after the gate stack is formed, the method continues with defining 204 the source/drain regions of the transistor structure. As previously explained, the source/drain regions can be implemented with any number of suitable processes and configurations. For example, the source/drain regions may be implanted, etched and epi filled, raised, silicon or SiGe alloy, p-type and/or n-type, and have a planar or fin shaped diffusion region. In the example embodiment shown in Figure 3A, substrate 300 has been etched to provide cavities 312/314 as well as respective tip areas 312A/314A which undercuts the gate dielectric 302. Figure 3B illustrates the substrate 300 after cavities 312/314 and tip areas 312A/314A have been filled to provide the source/drain regions 318/320 and tip regions 318A/320A. In accordance with some example embodiments, the source and drain region cavities 312/314 along with their respective tip areas 312A/314A are filled with in situ doped silicon or SiGe, thereby forming source region 318 (along with epi-tip 318A) and drain region 320 (along with drain epi-tip 320A). Any number of source/drain layer configurations can be used here, with respect to materials (e.g., silicon, SiGe, III-V materials), dopant (e.g., boron in excess of 2E21 cm^{-3}, or other suitable dopant/concentration), and dimension (e.g., thickness of source/drain layer may range, for instance, from 50 to 500 nm so as to provide a flush or raised source/drain region).

[0034] As previously explained, some such embodiments may include with a thin buffer between the source/drain layer and the substrate or the source/drain and boron doped germanium overlayer. For instance, and as can further be seen in the example embodiment shown in Figure 3B, a source buffer 313 and a drain buffer 315 are deposited prior to depositing the source/drain materials. In some embodiments, the buffers 313 and 315 can be a graded boron doped silicon germanium layer with the germanium composition graded from a base level concentration compatible with the underlying substrate 300 material up to 100 atomic % (or near to 100 atomic % as previously described). The boron concentration can be appropriately graded as well. Numerous buffer schemes will be apparent in light of this disclosure.

[0035] With further reference to Figure 2, after the source/drain regions are defined, the method continues with depositing 206 boron doped germanium on the source/drain regions of the transistor structure. Figure 3C shows the boron doped germanium layer 317/319. In some example embodiments, the boron doped germanium layer 317/319, which may be epitaxially deposited in one or more layers, has a germanium concentration in excess of 90 atomic %, although other suitable concentration levels can be used as will be appreciated in light of this disclosure (e.g., in excess of 91 atomic %, or 92 atomic %, …, or 98 atomic %, or 99 atomic %, or truly pure germanium). As previously explained, this germanium concentration may be fixed or graded so as to increase from a base level (near substrate 300) to a high level (e.g., in excess of 90 atomic %). The boron concentration in some such embodiments can be in excess of 1E20 cm^{-3}, such as higher than 2E20 cm^{-3} or 2E21 cm^{-3}, and may also be graded so as to increase from a base level near substrate 300 to a high level (e.g., in excess of 1E20 cm^{-3} or 2E20 cm^{-3} or 3E20 cm^{-3}, …, 2E21 cm^{-3}). In embodiments where the germanium concentration of the underlying source/drain regions 318/320 is fixed or otherwise relatively low, a graded buffer may be used to better interface source/drain regions 318/320 with the boron doped germanium layer 317/319, as previously explained. The thickness of the boron doped germanium cap 317/319 may have a thickness in the range, for example, of 50 to 250 Å, in accordance with some specific example embodiments, although alternative embodiments may have other layer thicknesses, as will be apparent in light of this disclosure.

[0036] In some embodiments, a CVD process or other suitable deposition technique may be used for the depositing 206 or otherwise forming the boron doped germanium layer 317/319. For example, the depositing 206 may be carried out in a CVD, or rapid thermal CVD (RT-CVD),

or low pressure CVD (LP-CVD), or ultra-high vacuum CVD (UHV-CVD), or gas source molecular beam epitaxy (GS-MBE) tool using germanium and boron containing precursors such as germane (GeH_4) or digermane (Ge_2H_6) and diborane (B_2H_6) or boron difluoride (BF_2). In some such embodiments, there may be a carrier gas such as, for instance, hydrogen, nitrogen, or a noble gas (e.g., precursor is diluted at 1-5% concentration of carrier gas). There may also be an etchant gas such as, for example, halogen-based gas such as hydrogen chloride (HCl), chlorine (Cl), or, hydrogen bromide (HBr). The basic deposition of germanium and also boron doped germanium is possible over a wide range of conditions using deposition temperature in the range, for example, of 300°C to 800°C (e.g., 300-500°C) and reactor pressure, for instance, in the range 1 Torr to 760 Torr. Germanium is naturally selective in that it deposits on silicon or silicon-germanium alloy, and does not deposit on other materials such as silicon dioxide and silicon nitride. Since this natural selectivity is not entirely perfect, a small flow of etchant can be used to increase the selectivity of the deposition, as previously noted. Each of the carrier and etchants can have a flow in the range of 10 and 300 SCCM (typically, no more than 100 SCCM of flow is required, but some embodiments may require higher flow rates). In one specific example embodiment, the deposition 206 is carried out using GeH_4 that is diluted in hydrogen at a 1% concentration and at a flow rate that ranges between 100 and 1000 SCCM. For an in situ doping of boron, diluted B_2H_6 may be used (e.g., the B_2H_6 may be diluted in H_2 at 3% concentration and at a flow rate that ranges between 100 and 600 SCCM. In some such specific example cases, an etching agent of HCl or Cl_2 is added at a flow rate that ranges, for example, between 10 and 100 SCCM, to increase the selectivity of the deposition.

[0037] As will be appreciated in light of this disclosure, the selectivity at which the boron doped germanium layer 317/319 is deposited can vary as desired. In some cases, for instance, the boron doped germanium layer 317/319 is deposited only on the source/drain regions 318/320 or a portion of the source/drain regions 318/320 (rather than across the entire structure). Any number of masking/patterning techniques can be used to selectively deposit layer 317/319. Moreover, other embodiments may benefit from layer 317/319 covering, for example, poly gate regions or grounding tap regions. As will further be appreciated in light of this disclosure, the combination of high germanium concentration (e.g., in excess of 90 atomic % and up to pure germanium) and high boron concentration (e.g., in excess of 2E20 cm^{-3}) can be used to realize significantly lower contact resistance in the source and drain regions (and other areas where low

contact resistance is desirable, such as ground tap regions), in accordance with some example embodiments. Further, and as previously explained, since boron diffusion is sufficiently suppressed by pure germanium, no adverse SCE degradation is realized with subsequent thermal anneals despite any high boron concentration proximate the channel (if applicable). Barrier height lowering is also enabled from the higher concentration of germanium at the contact surface. In some example embodiments, a germanium concentration in excess of 95 atomic % and up to pure germanium (100 atomic %) can be used to achieve such benefits.

[0038] With further reference to Figure 2, after the boron doped germanium layer 317/319 is provided, the method continues with depositing 208 a dielectric over layer 317/319. Figure 3D shows dielectric 322 as being flush with the hard mask 306 of the gate stack, but it need not be. The dielectric can be configured in a number of ways. In some embodiments, dielectric 322 is implemented with SiO_2 or other low-k dielectric materials. In other embodiments, dielectric 322 is implemented with a SiN liner followed by one or more layers of SiO_2, or any combination of nitride, oxide, oxynitride, carbide, oxycarbide, or other suitable dielectric materials). The dielectric 322, which may be referred to as an interlayer dielectric (ILD), may be planarized as commonly done. Other example dielectric materials include, for instance, carbon doped oxide (CDO), organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. In some example configurations, the ILD layer may include pores or other voids to further reduce its dielectric constant.

[0039] Next, in some embodiments of the present invention where a replacement metal gate (RMG) process is used and as best shown in Figure 3E, the method may further include removing the gate stack (including the high-k gate dielectric layer 302, the sacrificial gate electrode 304, and the hard mask layer 306) using an etching process as conventionally done. In alternate implementations, only the sacrificial gate 304 and hard mask layer 306 are removed. Figure 3E illustrates the trench opening that is formed when the gate stack is etched away, in accordance with one such embodiment. If the gate dielectric layer is removed, the method may continue with depositing a new gate dielectric layer into the trench opening (designated as 324 in Figure 3F). Any suitable high-k dielectric materials such as those previously described may be used here, such as hafnium oxide. The same deposition processes may also be used. Replacement of the gate dielectric layer may be used, for example, to address any damage that

may have occurred to the original gate dielectric layer during application of the dry and wet etch processes, and/or to replace a low-k or sacrificial dielectric material with a high-k or otherwise desired gate dielectric material. As further shown in Figure 3F, the method may further continue with depositing the metal gate electrode layer 326 into the trench and over the gate dielectric layer 324. Conventional metal deposition processes may be used to form the metal gate electrode layer, such as CVD, ALD, PVD, electroless plating, or electroplating. The metal gate electrode layer may include, for example, a p-type workfunction metal, such as ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. In some example configurations, two or more metal gate electrode layers may be deposited. For instance, a workfunction metal may be deposited in the gate trench followed by a suitable metal gate electrode fill metal such as aluminum or silver.

[0040] With further reference to Figure 2, after dielectric layer 322 is provided over layer 317/319 (and any desired RMG process), the method continues with etching 210 to form the source/drain contact trenches. Any suitable dry and/or wet etch processes can be used. Figure 3G shows the source/drain contact trenches after etching is complete, in accordance with one example embodiment. The method then continues with depositing 212 contact resistance reducing metal and annealing to form silicide/germanide, and then depositing 214 the source/drain contact plugs. Figure 3H shows the contact metals 325/327, which in some embodiments includes the silicide/germanide, although other embodiments may include additional layers (e.g., adhesion layer). Figure 3I shows the contact plug metal 329/331, which in some embodiments includes aluminum, although any suitably conductive contact metal or alloy can be used for the contact plug 329/331, such as silver, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium, using conventional deposition processes. The germanide/metalization 212 of the source and drain contacts can be carried out, for instance, by silicidation with nickel, aluminum, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants to form a low resistance germanide. The boron doped germanium layer 317/319 allows for metal-germanide formation (e.g., nickel-germanium). The germanide allows for significantly lower Schottky-barrier height and improved contact resistance (including R_{ext}) over that in conventional metal-silicide systems. For instance, conventional transistors typically use a source/drain SiGe epi process, with germanium concentration in the range of 30-40 atomic %.

Such conventional systems exhibit R_{ext} values of about 140 Ohm*um, limited by epi/silicide interfacial resistance, which is high and may impede future gate pitch scaling. Some embodiments of the present invention allow for a significant improvement in R_{ext} in PMOS devices (e.g., about a 2x improvement or better, such as a R_{ext} of about 70 Ohm*um), which can better support PMOS device scaling. Thus, transistors having a source/drain configured with boron doped germanium cap 317/319 in accordance with an embodiment of the present, with a boron concentration in excess of 1E20 cm^{-3} and a germanium concentration in excess of 90 atomic % and up to or otherwise near pure germanium (100 atomic %) at the interface between the source/drain regions 318/320 and the contact metals 325/327, can exhibit R_{ext} values of less than 100 Ohm*um, and in some cases less than 90 Ohm*um, and in some cases less than 80 Ohm*um, and in some cases less than 75 Ohm*um, or lower.

[0041] Figure 4 is a method for forming a transistor structure with low contact resistance in accordance with another embodiment of the present invention. Figures 5A through 5F illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments. As can be seen, this example transistor structure includes both p-type and n-type source and drain regions (designated p-S/D and n-S/D, respectively), and the boron doped germanium is selectively deposited on the p-type regions only. In general, this method is similar to the method described with reference to Figures 2 and 3A-H, except that the deposition of the boron doped germanium layer 317/319 on the source/drain regions is selectively carried out after the dielectric 322 is deposited and etched to form the contact trench.

[0042] The method includes forming 402 the gate stacks and defining 404 the various p-S/D and n-S/D regions using standard processing and as best shown in Figure 5A. In some embodiments, the p-S/D and n-S/D regions can be doped to provide a desired degree of selectivity with respect to boron doped germanium. The method further includes depositing 406 the dielectric 322 directly over the p-S/D and n-S/D regions, as shown in Figure 5B. The method continues with etching 408 to form the p-S/D and n-S/D region contact trenches, and then selectively deposting 410 the boron doped germanium layer 317/319 into the trench and onto the p-S/D regions (of which there may be one or more depending on the desired function and application of the transistor structure), as best shown in Figures 5C and 5D. Deposting 410 can be carried out using any suitable deposition process, such as selective epitaxy. Once layer 317/319 is provided, the method continues with depositing 412 contact metals 325/327 on top of

the layer 317/319 as well as on top of any exposed n-S/D regions, and then depositing 414 the source/drain contact plugs 329/331, as shown in Figures 5E and 5F. This alternate methodology provides the same benefit of improved contact resistance, but is more selective in where the boron doped germanium is deposited. Other such selective deposition processes will be apparent in light of this disclosure, using any suitable combination of masking/patterning and selective deposition techniques. As will be further appreciated, the previous relevant discussion with respect to similar parts of the method is equally applicable here.

FinFET Configuration

[0043] As is known, FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin). The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, a source region, and a drain region. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both sidewalls of the fin (sides perpendicular to the substrate surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate FinFET. Other types of FinFET configurations are also available, such as so-called double-gate FinFETs, in which the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin).

[0044] Figure 6 shows a perspective view of an example tri-gate architecture, configured in accordance with one embodiment of the present invention. As can be seen, the tri-gate device includes a substrate 600 having a semiconductor body or fin 660 (represented by dashed lines) extending from the substrate 600 through isolation regions 610, 620. A gate electrode 640 is formed over 3 surfaces of the fin 660 to form 3 gates. A hard mask 690 is formed on top of the gate electrode 640. Gate spacers 670, 680 are formed at opposite sidewalls of the gate electrode 640.

[0045] A source region comprises the epitaxial region 631 formed on a recessed source interface 650 and on one fin 660 sidewall, and a drain region comprises the epitaxial region 631 formed on a recessed source interface 650 and on the opposing fin 660 sidewall (not shown). A cap layer 641 is deposited over the epitaxial regions 631. Note that the boron cap layer 641 may be provided in the recessed (tip) regions, but in other embodiments is just provided over the

source/drain regions (and not in the recessed regions). In one embodiment, the isolation regions 610, 620 are shallow trench isolation (STI) regions formed using conventional techniques, such as etching the substrate 600 to form trenches, and then depositing oxide material onto the trenches to form the STI regions. The isolation regions 610, 620 can be made from any suitable dielectric/insulative material, such as SiO_2. The previous discussion with respect to the substrate 102 is equally applicable here (e.g., substrate 600 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).

[0046] As will be appreciated in light of this disclosure, conventional processes and forming techniques can be used to fabricate the FinFET transistor structure. However, and in accordance with one example embodiment of the present invention, the bilayer structure of the epitaxial region 631 and cap layer 641 can be implemented, for instance, using an in situ doped silicon or SiGe (for 631) capped with a boron doped germanium (for 641), with an optional germanium and/or boron graded buffer between the two bilayers. As previously explained, such a buffer may be used to transition from a base level germanium/boron concentration compatible with the epitaxial region 631 to the boron doped germanium cap 641. Alternatively, germanium and/or boron concentration grading can be implemented directly in the epitaxial region 631 and/or the cap 641, rather than in an intervening graded buffer arrangement. As will further be appreciated, note that an alternative to the tri-gate configuration is a double-gate architecture, which includes a dielectric/isolation layer on top of the fin 660.

[0047] Figure 7 shows a plot of a split lot showing contact resistance for transistor structures configured with in accordance with embodiments of the present invention and standard transistor structures configured with no cap. The transistor structures associated with the high resistance numbers in excess of 0.18 are all implemented with standard SiGe alloy raised PMOS source/drain regions with contact metal deposited directly thereon. The transistor structures associated with the resistance numbers of 0.107 and lower are all similarly implemented but with the addition a boron doped germanium cap between the source/drain regions and contact metal, in accordance with various embodiments of the present invention. Table 1 shows the raw data quantiles resulting from testing of the example structures with and without a boron doped germanium cap as described herein.

Ge Cap	Min	10%	25%	Median	75%	90%	Max
Yes	0.032	0.032	0.033	0.040	0.078	0.105	0.107
No	0.183	0.183	0.192	0.239	0.250	0.265	0.265

Table 1

As can be seen, this example lot actually shows an improvement (reduction) in contact resistance of about a three to six times (3X to 6X) over conventional transistor structures. The units are Ohms per arbitrary area.

[0048] Other improvements enabled by using a boron doped germanium cap in accordance with an embodiment of the present invention will be apparent in light of this disclosure. In particular, the resulting germanide materials and Schottky barrier height improvement enables more than a 2x R_{ext} improvement over that in conventional SiGe source/drain PMOS devices, in accordance with some example embodiments of the present invention. As is known, the Schottky barrier height is the barrier for electrical conduction across a semiconductor-metal junction. The magnitude of the Schottky barrier height reflects a mismatch in the energy position of the metal's Fermi level and the majority carrier band edge of the semiconductor across the semiconductor-metal interface. For a p-type semiconductor-metal interface, the Schottky barrier height is the difference between the metal Fermi level and the valence band maximum of the semiconductor.

Example System

[0049] Figure 8 illustrates a computing device 1000 configured in accordance with one embodiment of the invention. As can be seen, the computing device 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board or a daughterboard mounted on a main board or the only board of device 1000, etc. Depending on its applications, computing device 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto

processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing device 1000 may include one or more transistor structures as described herein. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

[0050] The communication chip 1006 enables wireless communications for the transfer of data to and from the computing device 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0051] The processor 1004 of the computing device 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments of the present invention, the integrated circuit die of the processor includes an onboard non-volatile memory or cache, and/or is otherwise communicatively coupled to off-chip memory that is implemented with one or more transistor structures as described herein. The term "processor" may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0052] The communication chip 1006 may also include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more devices implemented with one or more transistor structures as described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

[0053] In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the device 1000 may be any other electronic device that processes data or employs transistors.

[0054] Numerous embodiments will be apparent in light of this disclosure, and features described herein can be combined in any number of configurations. One example embodiment of the present invention provides a transistor device. The device includes a substrate having a channel region, and a gate electrode above the channel region. A gate dielectric layer is provided between the gate electrode and the channel region, and p-type and n-type source/drain regions are provided in the substrate and adjacent to the channel region. The device further includes a boron doped germanium layer on at least a portion of the p-type source/drain region. This boron doped germanium layer comprises a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}. The device further includes a metal-germanide source/drain contact on the boron doped germanium layer. In one such example, the boron doped germanium layer is only on p-type source/drain regions of the device. In another example case, the device further includes an interlayer dielectric. In another example case, the device further includes a graded buffer between the substrate and at least one of the p-type and n-type source/drain regions, and/or a graded buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer. In one such case, the graded buffer

between the at least one p-type and n-type source and drain regions and the boron doped germanium layer has a germanium concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 95 atomic %. In one such specific example case, the high concentration reflects pure germanium. In another example case, the graded buffer between the at least one of the p-type and n-type source/drain regions and the boron doped germanium layer has a boron concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 1E20 cm^{-3}. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron. In another example case, the p-type and n-type source/drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %. In another example case, the p-type and n-type source/drain regions comprise boron doped silicon germanium having a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}. In another example case, the p-type and n-type source/drain regions comprise silicon or silicon germanium, and the device further comprises a buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 1E20 cm^{-3}. In another example case, the boron doped germanium layer comprises a germanium concentration in excess of 98 atomic %, and a boron concentration in excess of 2E20 cm^{-3}. Another embodiment provides an electronic device that includes a printed circuit board having one or more integrated circuits, wherein at least one of the one or more integrated circuits comprises one or more transistor devices as variously defined in this paragraph. In one such case, the one or more integrated circuits includes at least one of a communication chip and/or a processor, and at least one of the communication chip and/or processor comprises the one or

more transistor devices. In another such case, the device is a computing device (e.g., mobile telephone or smartphone, laptop, tablet computer, etc).

[0055] Another embodiment of the present invention provides a transistor device. In this example case, the device includes a substrate having a channel region, and a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The device further includes p-type and n-type source/drain regions in the substrate and adjacent to the channel region, each of the p-type and n-type source/drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers. The device further includes a boron doped germanium layer on at least a portion of the p-type source/drain region, and comprising a germanium concentration in excess of 95 atomic % and a boron concentration in excess of 2E20 cm^{-3}. The device further includes metal-germanide source/drain contacts on the boron doped germanium layer. The device is one of a planar or FinFET transistor. In one such example case, the device further includes a buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 2E20 cm^{-3}. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron. In another example case, the p-type and n-type source/drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 98 atomic %. In another example case, the p-type and n-type source/drain regions have a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}. In another example case, the p-type and n-type source/drain regions comprise silicon germanium having a fixed germanium concentration, and the device further comprises a buffer between the p-type and n-type source/drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the p-type and n-

type source/drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the p-type and n-type source/drain regions to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms. Another embodiment provides a computing device (e.g., desktop or portable computer, etc) that includes a printed circuit board having a communication chip and/or a processor, wherein at least one of the communication chip and/or processor comprises one or more transistor devices as variously defined in this paragraph.

[0056] Another embodiment of the present invention provides a method for forming a transistor device. The method includes providing a substrate having a channel region, and providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region. The method continues with providing p-type and n-type source/drain regions in the substrate and adjacent to the channel region, and providing a boron doped germanium layer on at least a portion of the p-type source/drain region. The boron doped germanium layer comprises a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}. The method continues with providing metal-germanide source/drain contacts on the boron doped germanium layer. In some example such cases, the method further includes providing a graded buffer between the substrate and at least one of the p-type and n-type source/drain regions, and/or providing a graded buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron (which may be used with or without graded buffers). This method may be employed, for example, in the fabrication of any electronic devices such as a computing device.

[0057] The foregoing description of example embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

CLAIMS

What is claimed is:

1. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region;

p-type and n-type source/drain regions in the substrate and adjacent to the channel region;

a boron doped germanium layer on at least a portion of the p-type source/drain region, and comprising a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}; and

a metal-germanide source/drain contact on the boron doped germanium layer.

2. The device of claim 1 wherein the device is one of a planar or FinFET transistor.

3. The device of claims 1 or 2 wherein the boron doped germanium layer is only on p-type source/drain regions of the device.

4. The device of any of the preceding claims further comprising an interlayer dielectric.

5. The device of the preceding claims, further comprising at least one of:

a graded buffer between the substrate and at least one of the p-type and n-type source/drain regions; and

a graded buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer.

6. The device of claim 5 wherein the graded buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer has a germanium concentration that is graded from a base level concentration compatible with

the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 95 atomic %.

7. The device of claim 6 wherein the high concentration reflects pure germanium.

8. The device of claims 5, 6, or 7 wherein the graded buffer between the at least one of the p-type and n-type source/drain regions and the boron doped germanium layer has a boron concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 1E20 cm^{-3}.

9. The device of any of the preceding claims wherein the boron doped germanium layer has a graded concentration of at least one of germanium and boron.

10. The device of any of the preceding claims wherein the p-type and n-type source/drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %.

11. The device of any of the preceding claims wherein the p-type and n-type source/drain regions comprise boron doped silicon germanium having a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

12. The device of any of claims 1 through 4 wherein the p-type and n-type source/drain regions comprise silicon or silicon germanium, and the device further comprises a buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the at least one p-type and n-type source/drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the at least

one of the p-type and n-type source/drain regions to a high concentration in excess of 1E20 cm^{-3}.

13. The device of any of the preceding claims wherein the boron doped germanium layer comprises a germanium concentration in excess of 98 atomic %, and a boron concentration in excess of 2E20 cm^{-3}.

14. An electronic device comprising:

a printed circuit board having one or more integrated circuits, wherein at least one of the one or more integrated circuits comprises one or more transistor devices as defined in any of the preceding claims.

15. The electronic device of claim 14 wherein the one or more integrated circuits includes at least one of a communication chip and/or a processor, and at least one of the communication chip and/or processor comprises the one or more transistor devices.

16. The electronic device of claims 14 or 15 wherein the device is a computing device.

17. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

p-type and n-type source/drain regions in the substrate and adjacent to the channel region, each of the p-type and n-type source/drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers;

a boron doped germanium layer on at least a portion of the p-type source/drain region, and comprising a germanium concentration in excess of 95 atomic % and a boron concentration in excess of 2E20 cm^{-3}; and

a metal-germanide source/drain contact on the boron doped germanium layer;

wherein the device is one of a planar or FinFET transistor.

18. The device of claim 17, the device further comprising:

a buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 2E20 cm^{-3}.

19. The device of claims 17 wherein the boron doped germanium layer has a graded concentration of at least one of germanium and boron.

20. The device of claim 17 wherein the p-type and n-type source/drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 98 atomic %.

21. The device of claim 20 wherein the p-type and n-type source/drain regions have a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

22. The device of claim 17 wherein the p-type and n-type source/drain regions comprise silicon germanium having a fixed germanium concentration, and the device further comprises a buffer between the p-type and n-type source/drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the p-type and n-type source/drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the p-type and n-type source/drain regions

to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms.

23. A method for forming a transistor device, comprising:

providing a substrate having a channel region;

providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region; and

providing p-type and n-type source/drain regions in the substrate and adjacent to the channel region;

providing a boron doped germanium layer on at least a portion of the p-type source/drain region, the boron doped germanium layer comprising a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}; and

providing metal-germanide source/drain contacts on the boron doped germanium layer.

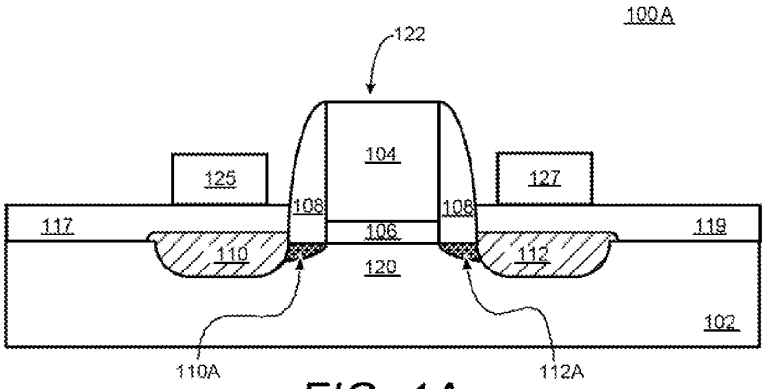


FIG. 1A

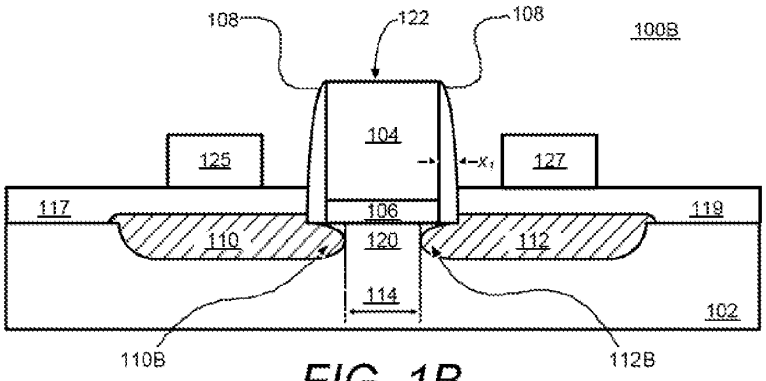


FIG. 1B

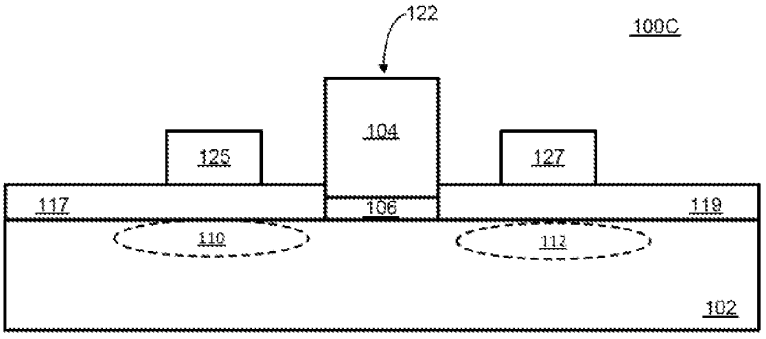


FIG. 1C

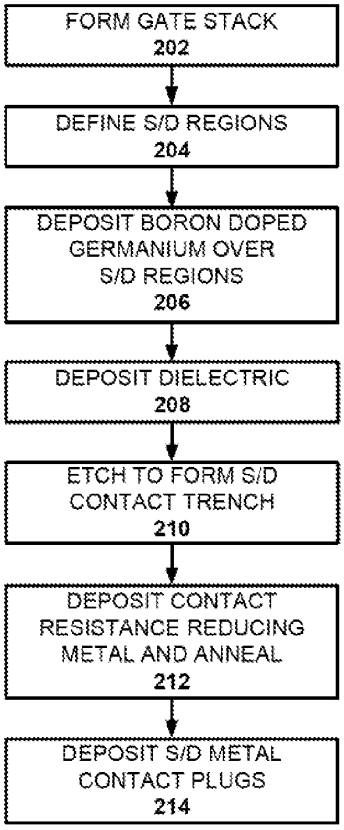

FORM GATE STACK
202
DEFINE S/D REGIONS
204
DEPOSIT BORON DOPED GERMANIUM OVER S/D REGIONS
206
DEPOSIT DIELECTRIC
208
ETCH TO FORM S/D CONTACT TRENCH
210
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
212
DEPOSIT S/D METAL CONTACT PLUGS
214

FIG. 2

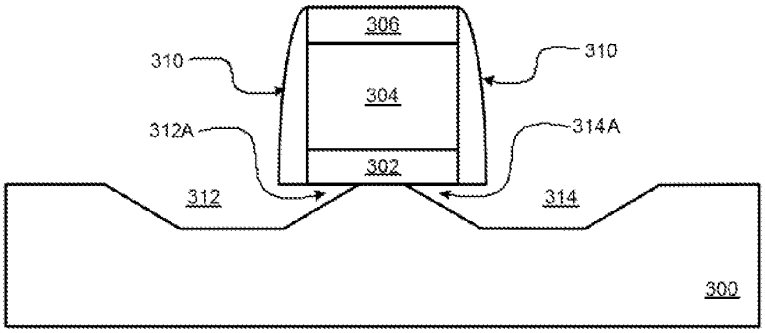


FIG. 3A

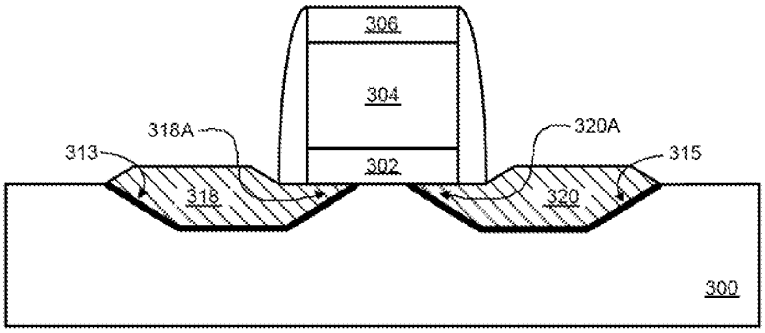


FIG. 3B

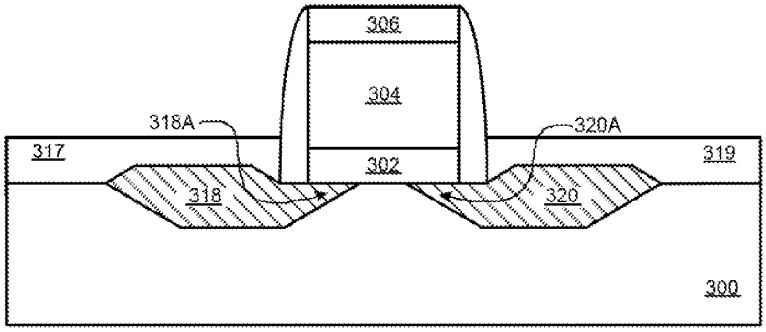


FIG. 3C

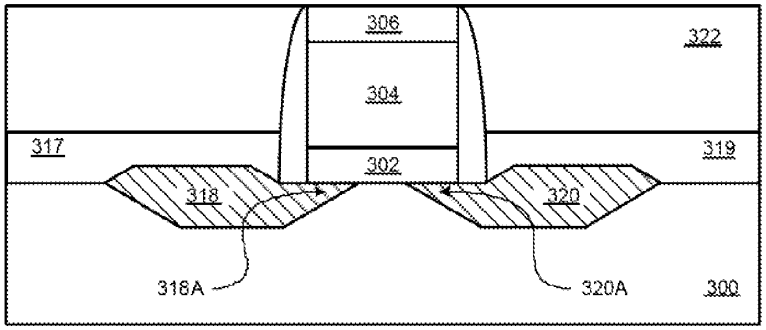


FIG. 3D

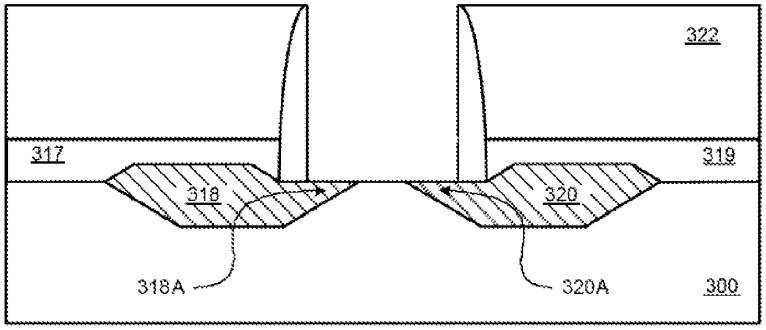


FIG. 3E

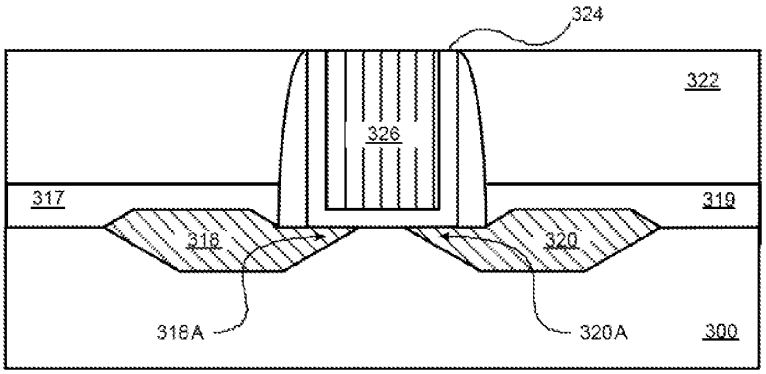


FIG. 3F

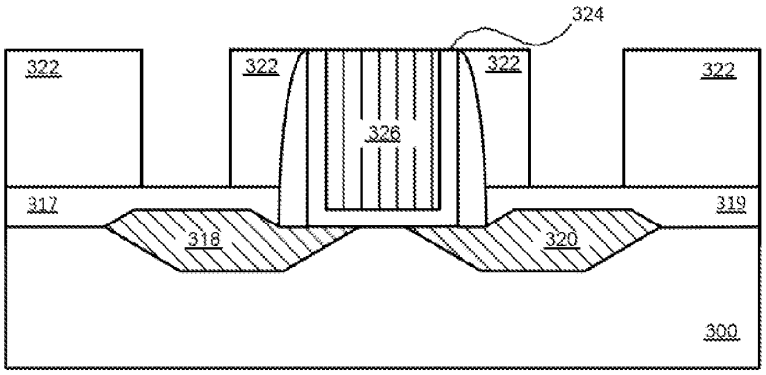


FIG. 3G

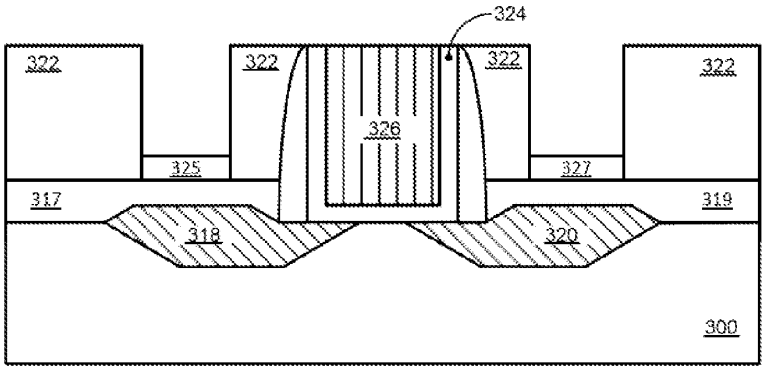


FIG. 3H

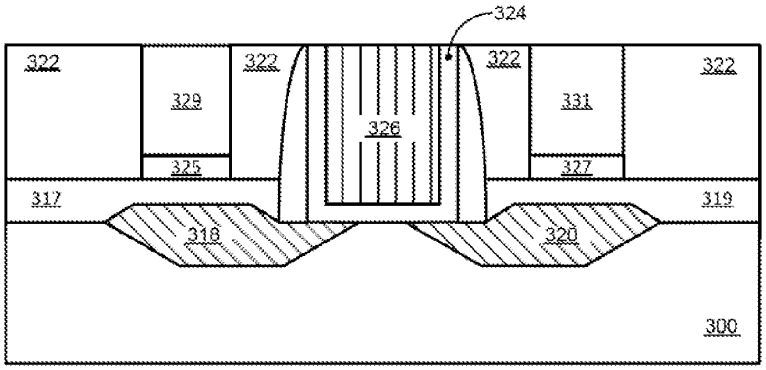


FIG. 3I

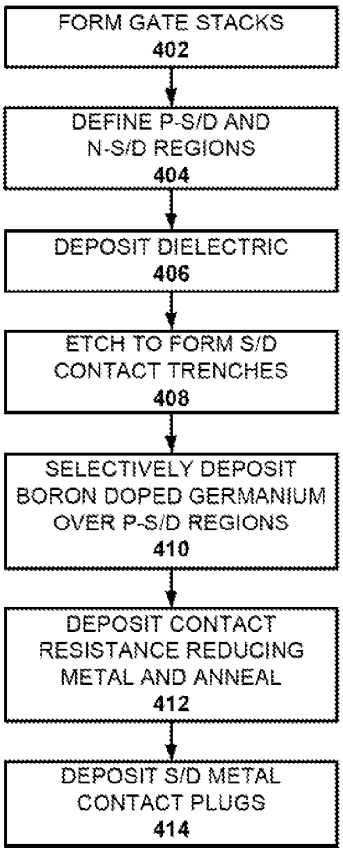

FORM GATE STACKS
402
DEFINE P-S/D AND N-S/D REGIONS
404
DEPOSIT DIELECTRIC
406
ETCH TO FORM S/D CONTACT TRENCHES
408
SELECTIVELY DEPOSIT BORON DOPED GERMANIUM OVER P-S/D REGIONS
410
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
412
DEPOSIT S/D METAL CONTACT PLUGS
414

FIG. 4

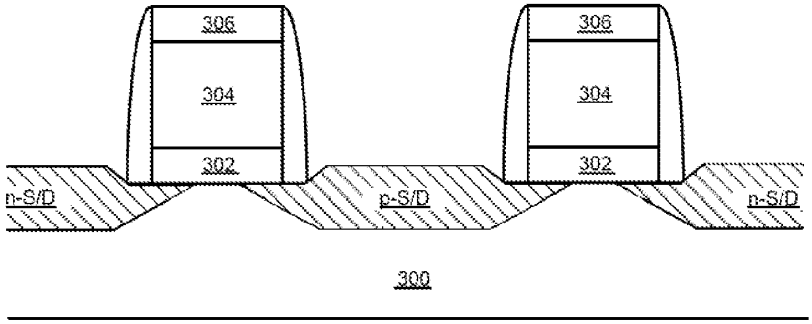


FIG. 5A

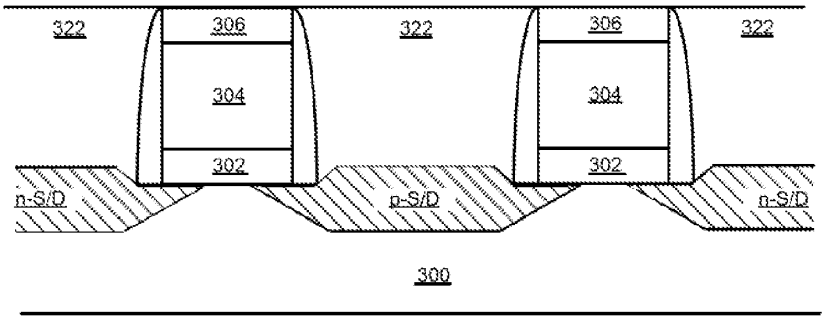


FIG. 5B

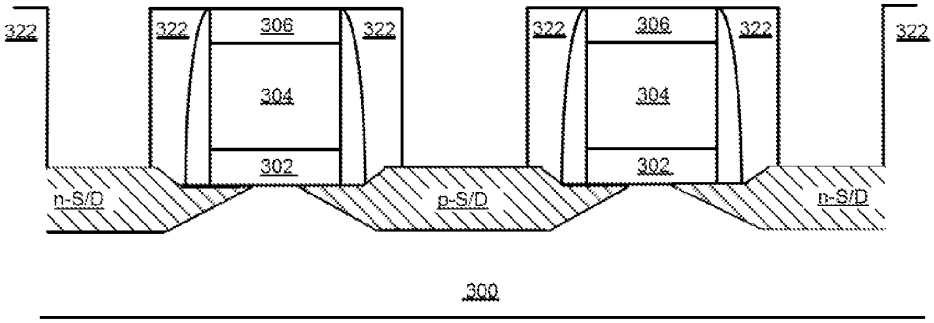


FIG. 5C

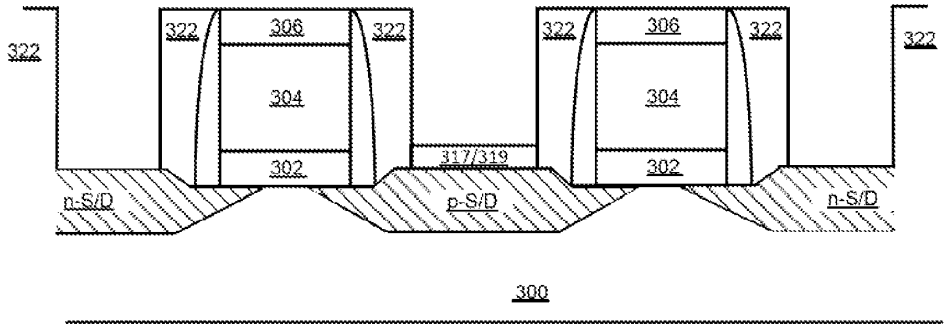


FIG. 5D

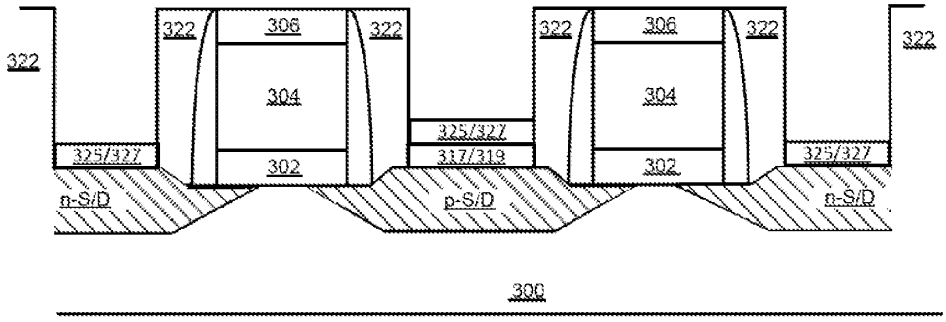


FIG. 5E

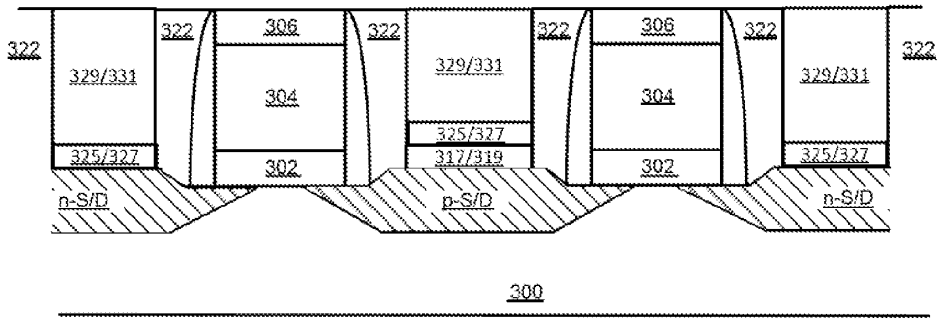


FIG. 5F

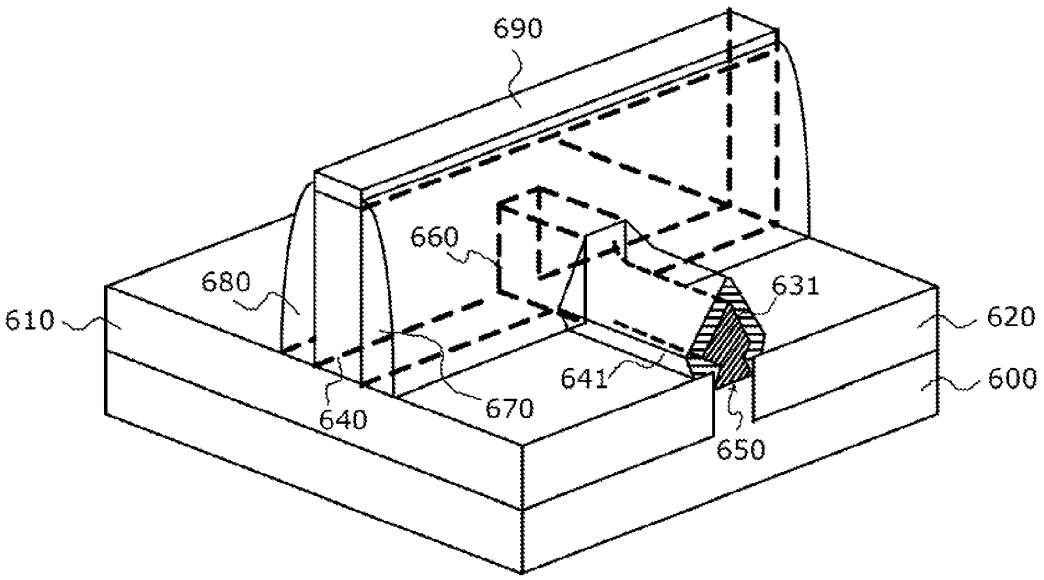


FIG. 6

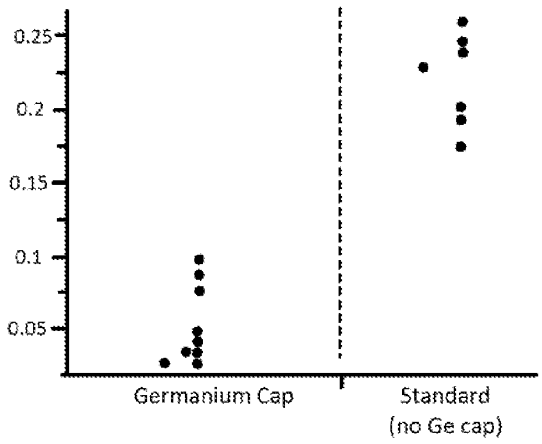


FIG. 7

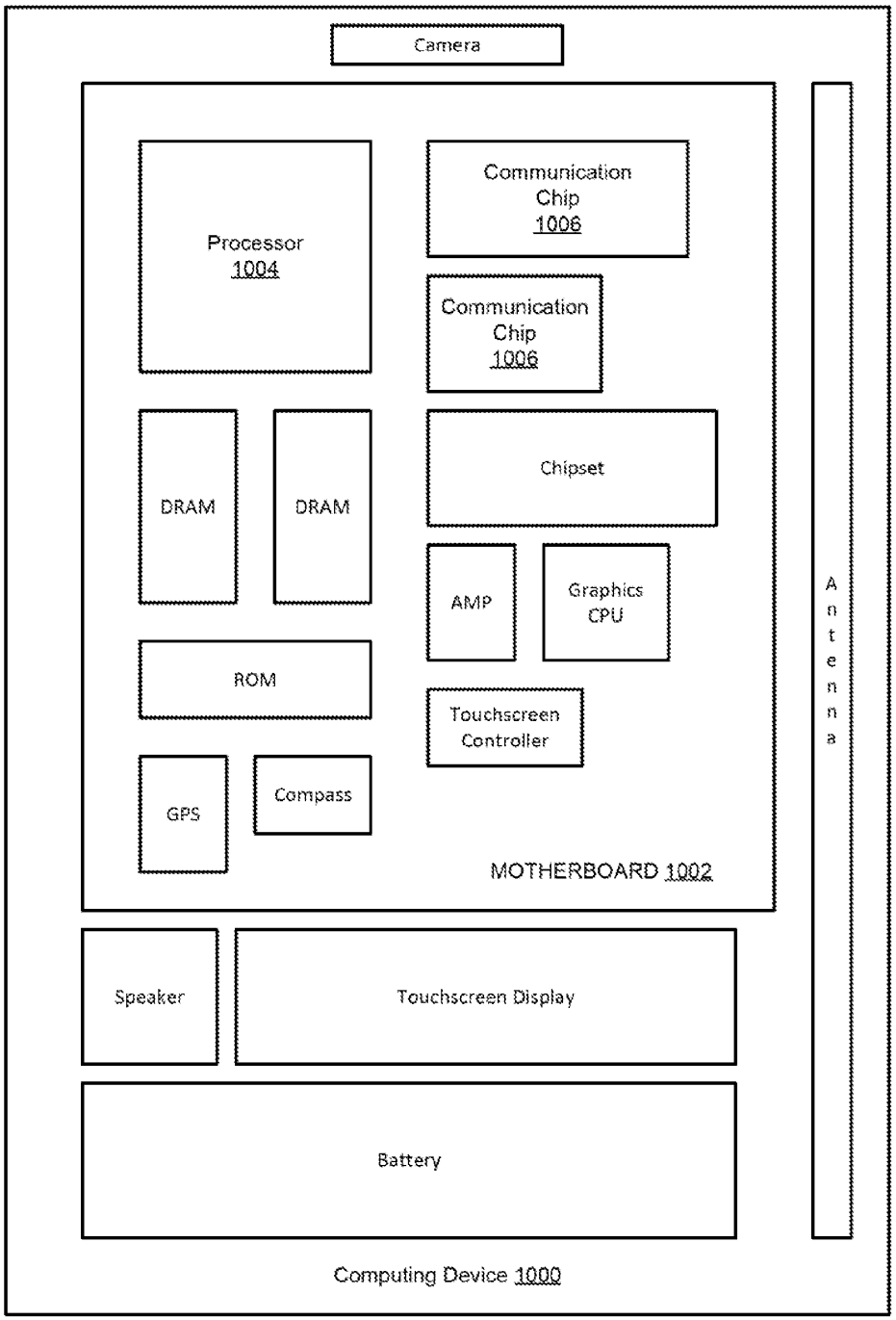

Camera
Processor
1004
Communication
Chip
1006
Communication
Chip
1006
DRAM
DRAM
Chipset
AMP
Graphics
CPU
ROM
Touchscreen
Controller
GPS
Compass
MOTHERBOARD 1002
Antenna
Speaker
Touchscreen Display
Battery
Computing Device 1000

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/054202

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; G11B 5/00; H01L 21/20; G11B 20/20; H01L 21/336; H01L 29/94

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: germanium, contact resistance, transistor, source, drain, boron, printed circuit board

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2007-0187767 A1 (YASUTAKE, NOBUAKI) 16 August 2007 See abstract; paragraphs[0020]-[0090]; figs.1,9,16	1-13,23 14-16,17-22
Y	US 2006-0156080 A1 (TELLKAMP, JOHN P. et al.) 13 July 2006 See abstract; paragraphs[0014]-[0031]; figs.1,2	14-16
Y	US 2010-0148217 A1 (SIMONELLI, DANIELLE et al.) 17 June 2010 See abstract; paragraphs[0037]-[0043]; figs.4,5	17-22
A	US 2008-0135878 A1 (KIM, SANG HUN et al.) 12 June 2008 See abstract; paragraphs[0024]-[0038]; figs.2A-2H,3	1-23

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0187767 A1	16.08.2007	JP 2007-214481 A	23.08.2007
		US 2010-0244154 A1	30.09.2010
		US 7880228 B2	01.02.2011
US 2006-0156080 A1	13.07.2006	None	
US 2010-0148217 A1	17.06.2010	CN 102171794 A	31.08.2011
		EP 2356670 A2	17.08.2011
		KR 10-2011-0050713 A	16.05.2011
		TW 201036044 A	01.10.2010
		US 7902009 B2	08.03.2011
		WO 2010-068530 A2	17.06.2010
		WO 2010-068530 A3	17.06.2010
US 2008-0135878 A1	12.06.2008	KR 10-0817217 B1	27.03.2008
		US 7550796 B2	23.06.2009

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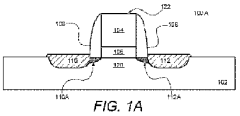


FIG. 1A

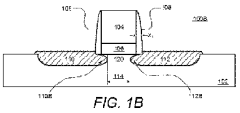


FIG. 1B

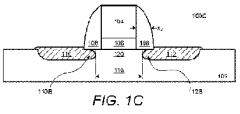


FIG. 1C

(57) Abstract: Techniques are disclosed for forming transistor devices having source and drain regions with high concentrations of boron doped germanium. In some embodiments, an in situ boron doped germanium, or alternatively, boron doped silicon germanium capped with a heavily boron doped germanium layer, are provided using selective epitaxial deposition in the source and drain regions and their corresponding tip regions. In some such cases, germanium concentration can be, for example, in excess of 50 atomic % and up to 100 atomic %, and the boron concentration can be, for instance, in excess of 1E20 cm^{-3}. A buffer providing graded germanium and/or boron concentrations can be used to better interface disparate layers. The concentration of boron doped in the germanium at the epi-metal interface effectively lowers parasitic resistance without degrading tip abruptness. The techniques can be embodied, for instance, in planar or non-planar transistor devices.

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TRANSISTORS WITH HIGH CONCENTRATION OF BORON DOPED GERMANIUM

BACKGROUND

Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to increase movement of electrons in N-type MOS device (NMOS) channel regions and to increase movement of positive charged holes in P-type MOS device (PMOS) channel regions. Such increased drive current in the transistors can be achieved by reducing device resistance.

One method of reducing the overall resistance of a MOS device is to dope the area between the source/drain regions and the channel region, known as the tip regions (or sometimes as source/drain extensions) of a MOS device. For instance, a dopant may be implanted in the source/drain regions and a subsequent anneal may be carried out to diffuse the dopant towards the channel region. Because an implant and diffusion method is used, the ability to control the dopant concentration and location is limited. Furthermore, the size of other parts of a MOS device, such as the thickness of its offset spacers, can also have a great impact on the location of the tip regions. All of this, in turn, affects the ability of the tip regions to maximize dopant concentration and come into close proximity of the channel region. Accordingly, improved methods or structures are needed to overcome the limitations of conventional tip regions.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A illustrates a conventional MOS device that includes source and drain tip regions formed using implantation and diffusion.

Figure 1B illustrates a MOS device that includes source and drain epitaxial tips configured in accordance with an embodiment of the present invention.

Figure 1C illustrates how spacer thickness can impact etching of epitaxial tips of a MOS device.

Figure 1D is a graph illustrating the dependence of UC-to-UC distance on spacer thickness.

Figure 2 is a method of forming source and drain epitaxial tips in accordance with an embodiment of the present invention.

Figures 3A to 3J illustrate structures that are formed when carrying out the method of Figure 2, in accordance with various embodiment of the present invention.

Figure 4 shows a perspective view of a FinFET transistor architecture, configured in accordance with one embodiment of the present invention.

Figure 5 is a graph illustrating how the UC-to-UC distance of a MOS device formed in accordance with an embodiment of the present invention is less dependent on spacer thickness.

Figure 6A illustrates Schottky barrier nickel germanide (NiGe) diode measurements, confirming that the NiGe workfunction is about 85 mV of the valance band edge, in accordance with some embodiments of the present invention.

Figure 6B plots simulation data that shows that such germanide materials provide a significant Rext improvement over that in conventional silicon germanium source/drain PMOS devices, in accordance with some embodiments of the present invention.

DETAILED DESCRIPTION

Techniques are disclosed for forming transistor devices having source and drain regions with high concentrations of boron doped germanium. The techniques can be used, for example, to extend self-aligned epitaxial tip (SET) transistors to achieve very near to the theoretical limit of uniaxial strain. In some embodiments, this is accomplished by use of an in situ boron doped germanium provided by selective epitaxial deposition in the source and drain regions as well as their corresponding tip regions. In other embodiments, selective epitaxial deposition is used to form a bilayer construction of boron doped silicon germanium capped with a heavily boron doped germanium layer in the source/drain and respective tip regions. In such cases, the germanium concentration can be, for example, in the range of 20 atomic % to 100 atomic %, and the boron concentration can be, for instance, in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., germanium concentration in excess of 50 atomic % and boron concentration in excess of 2E20 cm^{-3}). An optional thin buffer with graded germanium and/or boron concentration can be used as an interfacial layer to the underlying substrate material or materials with the layer of boron doped germanium. Likewise, in a bilayer configuration, a thin buffer with graded germanium and/or boron concentration can be used as an interfacial layer to the silicon germanium layer with the boron doped germanium cap. In still other embodiments, the boron doped

germanium or silicon germanium layers themselves can have a graded germanium and/or boron concentration in a similar fashion as to the optional buffers. In any such case, since boron diffusion is suppressed in germanium (the higher the concentration, the greater the suppression), a high concentration of boron can be doped in the germanium, which in turn results in lower parasitic resistance and without degrading tip abruptness. In addition, the contact resistance is reduced from lowering of Schottky-barrier height. The techniques can be embodied, for instance, in planar or non-planar FinFET transistor devices.

General Overview

As is known, a metal oxide semiconductor (MOS) transistor may include source and drain tip regions that are designed to decrease the overall resistance of the transistor while improving short channel effects (SCE). Conventionally, these tip regions are portions of the substrate where a dopant such as boron or carbon is implanted using an implant and diffusion technique. The source tip region is formed in the area between the source region and the channel region. Likewise, the drain tip region is formed in the area between the drain region and the channel region. The tip regions resulting from such conventional processing minimally underdiffuse the gate dielectric layer of the transistor.

In more detail, Figure 1A illustrates a conventional MOS transistor 100A formed on a substrate 102. The source region 110 and the drain region 112 are typically formed by either implanting dopants such as boron into the substrate or by etching the substrate and then epitaxially depositing a silicon or silicon germanium material (with a germanium concentration in the range of 10 to 40 atomic %). A gate stack 122 is formed over a channel region 120 of the transistor 100A. As can further be seen, the gate stack 122 includes a gate dielectric layer 106 and a gate electrode 104, and spacers 108 are formed adjacent to the gate stack 122. In some example cases, and depending on the technology node, the spacers 108 create a distance of about 10 to 20 nanometers (nm) between the edges of the gate dielectric layer 106 and the edges of each of the source and drain regions 110/112. It is within this space that a source tip region 110A and a drain tip region 112A are formed. As can be seen, the implantation-diffusion based tip regions 110A/112A overlap the spacers 108 and may also overlap or underdiffuse the gate dielectric layer 106 by a distance of less than 10 nm. In forming the implantation-diffusion based tip regions 110A/112A, a dopant such as boron or carbon is implanted into the source region 110 and the drain region 112. The transistor 100A is then annealed to cause the dopant to diffuse towards the channel region 120. Angled ion implantation techniques may also be used to further implant dopants into those areas between the gate dielectric layer 106 and the

source/drain regions 110/112. Unfortunately, factors such as the shape of the tip regions 110A/112A, the distance the dopants penetrate below the spacers 108, and the concentration gradient of the tip regions 110A/112A are dependent on the diffusion properties of the dopant in the substrate material. For instance, the concentration of the tip regions will be high proximate to the source/drain region 110/112 and low proximate to the channel region 120. Although highly desired, it is nearly impossible to make the dopant concentration proximate to the channel region 120 very high without driving the dopant into the channel region 120. Furthermore, the source and drain regions 110/112 cannot be moved closer to the channel region 120 because the dopant may again be driven into the channel region 120. This limits how close the source and drain regions 110/112 can be formed to the channel region 120, thereby constraining gate length scaling.

Figure 1B illustrates an example MOS device 100B that includes source and drain epitaxial tips (generally referred to herein as epi-tips) configured in accordance with an embodiment of the present invention. In more detail, the MOS transistor 100B uses an undercut etch to allow the source region 110 and the drain region 112 to extend below the spacers 108, and in some cases, below the gate dielectric layer 106. The portions of the source/drain regions 110/112 that extend below the spacers 108 (and possibly the gate dielectric layer 106) are referred to herein as the source epi-tip 110B and the drain epi-tip 112B, respectively. The source and drain epi-tips 110B/112B replace the implantation/diffusion based tip regions 110A/112A described with regard to Figure 1A.

In accordance with an embodiment of the present invention, the source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be formed, for example, by etching the substrate 102, which includes undercutting the spacers 108 (and possibly the gate dielectric layer 106), and then using selective epitaxial deposition to provide an in situ boron doped germanium, or boron doped silicon germanium (SiGe) capped with heavily boron doped germanium, to fill the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, as shown in Figure 1B. Note the epitaxial fill may be raised relative to the surface of substrate 102, as further shown in Figure 1B.

In accordance with some embodiments of the present invention, a graded buffer may be used in more or more locations of the structure, depending on factors such as the substrate composition and extent to which misfit dislocation is to be inhibited between disparate layers of the device structure. For instance, the substrate 102 can be a silicon substrate, or a silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate comprising silicon, silicon germanium, germanium, and/or III-V compound

semiconductors. Thus, and by way of example, in an embodiment having a silicon or silicon germanium substrate 102 and an in situ boron doped germanium is used to fill the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, a buffer can be provided between the underlying substrate 102 and the upper boron doped germanium. In such an embodiment, the buffer can be a graded boron doped (or intrinsic) silicon germanium layer with the germanium composition graded from a base level concentration compatible with the underlying silicon substrate or silicon germanium substrate up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). In one specific such embodiment, the germanium concentration ranges from 40 atomic % or less to in excess of 98 atomic %. The boron concentration within this buffer can be fixed, for example, at a high level or grade, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 1E20 cm^{-3}, or 5E20 cm^{-3}). Note that compatibility as used herein does not necessitate an overlap in concentration levels (for instance, the germanium concentration of underlying substrate can be 0 to 20 atomic % and initial germanium concentration of the buffer can be 30 to 40 atomic %). In addition, as used herein, the term 'fixed' with respect to a concentration level is intended to indicate a relatively constant concentration level (e.g., the lowest concentration level in the layer is within 10% of the highest concentration level within that layer). In a more general sense, a fixed concentration level is intended to indicate the lack of an intentionally graded concentration level. The thickness of the buffer can vary depending on factors such as the range of concentrations being buffered, but in some embodiments is in the range of 30 to 120 Angstroms (Å), such as 50 to 100 Å (e.g., 60 Å or 65 Å). As will be appreciated in light of this disclosure, such a graded buffer beneficially lowers the Schottky-barrier height.

Alternatively, rather than using a thin buffer between the underlying substrate 102 and the upper boron doped germanium, the boron doped boron doped germanium layer itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, the boron doped germanium layer can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to 70 atomic %) up to 100 atomic %. In some such embodiments, the boron concentration within this boron doped germanium layer can

range, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 1E20 cm^{-3}).

In other embodiments having a silicon or silicon germanium substrate 102 and a bi-layer structure of an in situ boron doped SiGe and boron doped germanium cap filling the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, a buffer can be provided between the boron doped SiGe layer and the upper boron doped germanium cap. In one such embodiment, the boron doped SiGe layer has a fixed concentration of germanium (e.g., in the range of 30 to 70 atomic %) and the buffer can be a thin SiGe layer (e.g., 30 to 120 Å, such as 50 to 100 Å) having a germanium concentration graded from a base level concentration compatible with the underlying boron doped SiGe layer up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). In some such cases, the boron concentration within this buffer can be fixed, for example, at a high level or can range, for example, from a base concentration at or otherwise compatible with the underlying SiGe layer up to a desired high concentration (e.g., in excess of 1E20 cm^{-3}, 2E20 cm^{-3}, 3E20 cm^{-3}, 4E20 cm^{-3}, or 5E20 cm^{-3}).

Alternatively, rather than using a thin buffer between the two layers of the bilayer structure, the boron doped SiGe layer itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, the boron doped SiGe layer can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to 70 atomic %) up to 100 atomic % (or near 100 atomic %, as previously explained). The boron concentration within this boron doped SiGe layer can be fixed, for example, at a high level or can range, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 1E20 cm^{-3}).

Thus, a SET architecture for planar and non-planar FinFET transistor devices is provided. The devices may be formed in part using conventional processes such as, for example, by dummy gate oxide, thin spacer, and an isotropic undercut etch (or an ammonia etch to form faceted fin recess in monocrystalline substrate, or other suitable etch to form fin recess). In accordance with some embodiments, selective epitaxial deposition can then be used to provide in situ boron doped germanium or alternatively, a fully strained boron doped silicon germanium layer capped with heavily boron doped pure germanium, to form both tips and source/drain regions. Optional buffers may be used as previously explained. With such embodiments, no P-type source and drain (PSD)

implants or high temp diffusion-based anneals are required, since boron is fully active as deposited. Any suitable high-k replacement metal gate (RMG) process flow can also be used, where a high-k dielectric replaces the dummy gate oxide. Silicidation with, for example, nickel, nickel-platinum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. As previously explained, such embodiments extend SET transistor device architecture to achieve (near) theoretical limit of uniaxial strain. The techniques provided herein can be applied, for example, to benefit any technology nodes (e.g., 90nm, 65nm, 45nm, 32nm, 22nm, 14nm, and 10nm transistors, and lower), and the claimed invention is not intended to be limited to any particular such nodes or range of device geometries. Other advantages will be apparent in light of this disclosure.

For instance, note that the source and drain epi-tips 110B/112B configured in accordance with an embodiment of the present invention can be formed in the same process as the source and drain regions 110/112, which reduces process time. In addition, unlike conventional implantation/diffusion based tip regions, the lattice parameter of the source/drain epi-tips 110B/112B configured in accordance with an embodiment of the present invention induces a strain in the channel region 120 that increases hole mobility and therefore decreases resistance in the channel. Another advantage of a SET architecture configured in accordance with some embodiments of the present invention is that the interface between the source/drain epi-tips 110B and 112B and the substrate material 102 that forms the channel region 120 is abrupt. For instance, on one side of the interface is the epitaxially deposited boron doped germanium (B:Ge) material (e.g., with B concentration in excess of 2E20 cm^{-3} or 5E20 cm^{-3}) and on the other side of the interface is the substrate material that makes up the channel region 120 (e.g., silicon germanium, or other suitable substrate material). This structure enables the epitaxial source/drain epi-tips 110B/112B to bring the heavily boron doped high concentration germanium material in very close proximity to the channel region 120. The boron in the epitaxial source/drain epi-tips 110B/112B remains substantially or completely within the epi-tips and does not tend to diffuse into the channel region 120.

Conventional methods that can be used in forming the source and drain epi-tips 110B/112B can have issues that should be considered. In particular, and with reference to Figures 1B and 1C, conventional undercut etching techniques may result in the formation of a bulleted profile for the undercut region. In such cases, more of the substrate material

is etched a slight distance below the gate dielectric layer 106 than is etched directly adjacent to the gate dielectric layer 106. As such, the source epi-tip 110B and the drain epi-tip 112B each conform to that bulleted profile, which may produce a less than optimal strain in the channel region 120. Furthermore, variance in conventional undercut etching techniques can translate into a variance in the resulting source and drain epi-tips 110B/112B that are formed. Another issue with conventional methods of forming source and drain epi-tips 110B/112B concerns the effect that spacer thickness has on the undercut etch, as shown in Figures 1B and 1C. With reference to Figure 1B, the MOS transistor 100B is shown having offset spacers 108 of a first thickness x_1. A substrate etch has been performed that undercuts the spacers 108 and a portion of the gate dielectric layer 106 to enable the formation of source and drain epi-tips 110B/112B. An undercut-to-undercut (UC-to-UC) distance 114 separates source epi-tip 110B from drain epi-tip 112B. With reference to Figure 1C, a MOS transistor 100C is shown with offset spacers 108 having a thickness x_2. Here, the thickness x_2 is much greater than the thickness x_1 of the spacers 108 in Figure 1B. As a result, when the substrate etch is performed, the thicker spacers 108 push out the undercut etch and cause the source/drain epi-tips 110B/112B to be formed further away from the channel region 120 of the transistor 100C. The substrate etch therefore undercuts less of the surface area beneath the MOS transistor 100C. Accordingly, a UC-to-UC distance 116 for the MOS transistor 100C is much larger than the UC-to-UC distance 114 for the MOS transistor 100B. Altering the UC-to-UC distance in this manner yields large drive current variations for MOS transistors. Figure 1D is a graph illustrating how spacer thickness affects the UC-to-UC distance in devices formed using known methods. The graph provides data, represented by line 118, showing that as spacer thickness increases, the UC-to-UC distance also increases, leading to large drive current variations. Typically, for every nanometer of spacer thickness increase, the UC-to-UC distance increases by around 2 nm. In this sense, forming source/drain epi-tips using conventional methods at least in some cases permits the thickness of the offset spacers to have a significant impact on the performance of the MOS device. As will be appreciated in light of this disclosure, some embodiments of the present invention provide methods of forming self-aligned and epitaxially deposited source and drain tips that address such issues.

Architecture and Methodology

Figure 2 is a method 200 of building a MOS transistor with self-aligned source and drain epi-tips, in accordance with an embodiment of the present invention. Figures 3A