

through 3J illustrate example structures that are formed as the method 200 is carried out, and in accordance with some embodiments.

As can be seen, the method 200 begins with providing 202 a semiconductor substrate upon which a MOS device, such as a PMOS transistor, may be formed. The semiconductor substrate may be implemented, for example, with a bulk silicon or a silicon-on-insulator configuration. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, such as germanium, silicon germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. In a more general sense, any material that may serve as a foundation upon which a semiconductor device may be built can be used in accordance with embodiments of the present invention.

The method 200 continues with forming 204 a gate stack on the semiconductor substrate. The gate stack can be formed as conventionally done or using any suitable custom techniques. In some embodiments of the present invention, the gate stack may be formed by depositing and then patterning a gate dielectric layer and a gate electrode layer. For instance, in one example case, a gate dielectric layer may be blanket deposited onto the semiconductor substrate using conventional deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Alternate deposition techniques may be used as well, for instance, the gate dielectric layer may be thermally grown. The gate dielectric material may be formed, for example, from materials such as silicon dioxide or high-k dielectric materials. Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some specific example embodiments, the high-k gate dielectric layer may be between around 5 Å to around 200 Å thick (e.g., 20 Å to 50 Å). In general, the thickness of the gate dielectric layer should be sufficient to electrically isolate the gate electrode from the neighboring source and drain contacts. In further embodiments, additional processing may be performed on the high-k gate dielectric layer, such as an annealing process to improve the quality of the high-k material. Next, a gate electrode material may be deposited on the gate dielectric layer using similar deposition techniques such as ALD, CVD, or PVD. In some such specific embodiments, the gate electrode material is polysilicon or a metal layer, although other

suitable gate electrode materials can be used as well. The gate electrode material, which is typically a sacrificial material that is later removed for a replacement metal gate (RMG) process, has a thickness in the range of 50Å to 500Å (e.g., 100Å), in some example embodiments. A conventional patterning process may then be carried out to etch away portions of the gate electrode layer and the gate dielectric layer to form the gate stack, as shown in Figure 3A.

Figure 3A illustrates a substrate 300 upon which a gate stack is formed. As can be seen with this example embodiment, the gate stack includes a gate dielectric layer 302 (which may be high-k gate dielectric material) and a sacrificial gate electrode 304. In one specific example case, the gate stack includes a silicon dioxide gate dielectric layer 302 and a polysilicon gate electrode 304. The gate stack may also include a gate hard mask layer 306 that provides certain benefits or uses during processing, such as protecting the gate electrode 304 from subsequent ion implantation processes. The hard mask layer 306 may be formed using typical hard mask materials, such as such as silicon dioxide, silicon nitride, and/or other conventional dielectric materials.

With further reference to Figure 2, after the gate stack is formed, the method 200 continues with an ion implantation process to highly dope portions of the substrate adjacent to the gate stack, by implanting 206 dopants into the substrate. The dopant used in the ion implantation process can be chosen, for example, based on its ability to increase the etch rate of the substrate material in which it is implanted, and the specific dopant selected for the ion implantation process may vary based on the substrate material(s) and the etchant used in a subsequent etching process. Specific dopants that may be selected to increase the etch rate of the substrate include, for example, carbon, phosphorous, and arsenic. For instance, carbon may be used at a dosage that ranges from 1×10^{14} to 1×10^{16} atoms/cm³ using an implantation energy that falls between 5 and 15 kilo-electron volts (keV). Phosphorous may be used at a dosage that ranges from 1×10^{14} to 5×10^{15} atoms/cm³ using an implantation energy that falls between 1 and 5 keV. Arsenic may be used at a dosage that ranges from 1×10^{14} to 5×10^{15} atoms/cm³ using an implantation energy that falls between 2 and 5 keV. Other suitable dopants and dosage schemes will be apparent in light of this disclosure. In some embodiments, the ion implantation substantially occurs in a vertical direction (i.e., a direction perpendicular to substrate); while in other embodiments at least a portion of the ion implantation process occurs in an angled direction to implant ions below the gate stack. Note that the hard mask 306 can be used to prevent doping of the gate electrode 304 material.

Next, the method 200 continues with annealing 207 the substrate to drive the dopants further into the substrate and to reduce any damage sustained by the substrate during the ion implantation process. In some embodiments, the implanting 206 and subsequent annealing 207 may drive the ions to a substrate depth that falls, for example, between 2 nm and 20 nm. The annealing 207 may be carried out at a temperature that falls, for example, between 700°C and 1100°C for a time duration of up sixty seconds or less (e.g., five seconds). As will be appreciated, the annealing temperature and duration can vary from one embodiment to the next, depending on factors such as the diffusion rate, substrate material, dopant used, and desired end dopant concentration.

Figure 3B illustrates the substrate 300 after the ion implantation and diffusion process. As shown in this example embodiment, the ion implantation process creates two doped regions 308 adjacent to the gate dielectric layer 302, for the MOS transistor being formed. When exposed to an appropriate etchant, the doped regions 308 will have an etch rate that is higher than the etch rate of the surrounding substrate material. One of the doped regions 308 will serve as a portion of a source region, including its self-aligned epi-tip. The other doped region 308 will serve as a portion of a drain region, including its self-aligned epi-tip. In the example embodiment shown, portions of the doped regions 308 are sited below the gate dielectric layer 302. Note that the size of the doped regions 308, including their depth, may vary based on the requirements of the MOS transistor being formed.

Next, the method 200 continues with forming 208 spacers on either side of the gate stack. The spacers may be formed, for example, using conventional materials such as silicon oxide, silicon nitride, or other suitable spacer materials. The width of the spacers may generally be chosen based on design requirements for the MOS transistor being formed. In accordance with some embodiments, however, the width of the spacers is not subject to design constraints imposed by the formation of the source and drain epi-tips. Figure 3C illustrates the substrate 300 with spacers 310 formed on either side of the gate electrode layer 304 and the gate dielectric layer 302, in accordance with an example embodiment.

With further reference to Figure 2, the method 200 continues with dry etching 210 the doped regions of the substrate to form cavities in which source/drain regions including their respective epi-tips may be formed. As best seen with reference to Figure 3D, the etched cavities are generally adjacent to the gate stack, and the epi-tip areas are effectively extensions of the source/drain cavity regions. In some example embodiments, the etched

cavities may be formed to a depth that falls between 50 nm and 1500 nm, which can be deeper than the doped regions. In a more general sense, the etch depth can be set as needed, based on desired MOS device performance. In some embodiments, the dry etch process can use an etchant recipe that complements the dopant used in the ion implantation process to increase the etch rate of the doped regions, thereby enabling the etching process to remove substrate material from the doped regions at a faster rate than the remainder of the substrate 300. In some embodiments, this includes portions of the doped regions that undercut the spacers 310 and the gate dielectric layer 302, thereby defining the self-aligned tip architecture of the transistor. Increasing the etch rate of the doped regions enables the etched source and drain tip cavities to undercut the spacers 310 and the gate dielectric layer 302 without the UC-to-UC distance being substantially impacted by factors such as the thickness of the spacers, variations in the dry etch process, and other process variations.

In accordance with some embodiments, the dry etch process may use a chlorinated chemistry that takes place in a plasma reactor. In some specific such embodiments, the etchant recipe may include a combination of NF_3 and Cl_2 with argon or helium used as a buffer or carrier gas. In accordance with some such embodiments, the flow rate for the active etchant species may vary, for example, between 50 and 200 standard cubic centimeters per minute (SCCM) while the flow rate of the carrier gas may vary, for example, between 150 and 400 SCCM. A high energy plasma may be employed at a power that ranges, for instance, from 700W to 1100W with a low RF bias of less than 100W, in accordance with some such embodiments. The reactor pressure may range from around 1 pascal (Pa) to around 2 Pa, in accordance with some such embodiments. In another specific example embodiment, the etchant chemistry may include a combination of HBr and Cl_2 . In some such embodiments, the flow rate for the etchant species may vary, for example, between 40 SCCM and 100 SCCM. A high energy plasma may be employed at a power that ranges from around 600W to around 1000W with a low RF bias of less than 100W, and the reactor pressure may range from around 0.3 Pa to around 0.8 Pa, in accordance with some such embodiments. In yet another example embodiment, the etchant chemistry may include a combination of Ar and Cl_2 . In some such embodiments, the flow rate for the etchant species may vary, for example, between 40 SCCM and 80 SCCM. A medium energy plasma may be employed at a power that ranges from around 400W to around 800W with a high RF bias of between around 100W and 200W, and the reactor pressure may range from around 1 Pa to around 2 Pa, in accordance with some

such embodiments. The dry etch process times for each of these example embodiments may be, for example, up to 60 seconds per substrate, but can vary depending factors such as desired etch depth and etchant. Such etch process parameters may vary, as will be appreciated.

Figure 3D illustrates the substrate 300 after the dry etch process has been carried out, in accordance with some embodiments of the present invention. As shown, a source region cavity 312 and a drain region cavity 314 are formed. In addition, a source tip cavity 312A and a drain tip cavity 314A have been formed as extensions of cavities 312 and 314, respectively, by the etching 210 of the doped regions as previously discussed. Note that the thickness of the spacers 310 has minimal impact on the etching of the source tip cavity 312A and the drain tip cavity 314A due to the use of dopants and etchant recipes that increase the etch rate of the doped regions during etching 210.

After the dry etch process has completed, and with further reference to Figure 2, the method of this example embodiment continues with wet etching 212 to clean and further etch the source region cavity 312 and its source epi-tip cavity 312A, as well as the drain region cavity 314 and its drain epi-tip cavity 314A. The wet etching 212, which can be carried out using conventional or custom wet etch chemistries, can be used to remove contaminants such as carbon, fluorine, chlorofluorocarbons, and oxides such as silicon oxide to provide a clean surface upon which subsequent processes may be carried out. In addition, and assuming a monocrystalline silicon substrate, the wet etching 212 may also be used to remove a thin portion of the substrate along the $\langle 111 \rangle$ and $\langle 001 \rangle$ crystallographic planes to provide a smooth surface upon which a high quality epitaxial deposition may occur. In some example cases, the thin portion of the substrate that is etched away may be, for example, up to 5 nm thick and may also remove residual contaminants. As best shown in Figure 3E, the wet etching 212 causes edges of the source region cavity 312 and its epi-tip region 312A, as well as the drain region cavity 314 its epi-tip region 314A to follow the $\langle 111 \rangle$ and $\langle 001 \rangle$ crystallographic planes. Further note that the source and drain epi-tip regions 312A and 314A do not have the bulleted profile that occurs in conventional processing.

After the wet etch process has completed, and with further reference to Figure 2, the method 200 continues with epitaxially depositing 214 in the source/drain and respective tip cavities either an in situ boron doped germanium (with an intervening thin buffer in some cases), or boron doped silicon germanium capped with a heavily boron doped germanium layer. This epitaxial deposition fills the source and drain cavities

including their respective epi-tip regions in one process, in accordance with some embodiments. A CVD process or other suitable deposition technique may be used for the depositing 214. For example, the depositing 214 may be carried out in a CVD reactor, an LPCVD reactor, or an ultra high vacuum CVD (UHVCVD). In some example cases, the reactor temperature may fall, for instance, between 600°C and 800°C and the reactor pressure may fall, for instance, between 1 and 760 Torr. The carrier gas may include, for example, hydrogen or helium at a suitable flow rate, such as between 10 and 50 SLM. In some specific embodiments, the deposition may be carried out using a germanium source precursor gas such as GeH_4 that is diluted in H_2 (e.g., the GeH_4 may be diluted at 1-5%). For instance, the diluted GeH_4 may be used at a 1% concentration and at a flow rate that ranges between 50 and 300 SCCM. For an in situ doping of boron, diluted B_2H_6 may be used (e.g., the B_2H_6 may be diluted in H_2 at 1-5%). For instance, the diluted B_2H_6 may be used at a 3% concentration and at a flow rate that ranges between 10 and 100 SCCM. In some example cases, an etching agent may be added to increase the selectivity of the deposition. For instance, HCl or Cl_2 may be added at a flow rate that ranges, for example, between 50 and 300 SCCM.

In accordance with some example embodiments of the present invention, and as best shown in Figure 3F, the source and drain region cavities 312/314 along with their respective tip regions 312A/314A are filled with in situ boron doped germanium, thereby forming source region 318 (along with epi-tip 318A) and drain region 320 (along with drain epi-tip 320A) of a MOS transistor 316 in substrate 300. In some such embodiments, the boron doped germanium has a boron concentration in excess of $5 \times 10^{20} \text{ cm}^{-3}$, such as $2 \times 10^{21} \text{ cm}^{-3}$ or higher. The thickness of the boron doped germanium deposited layer may range, for example, from 50 to 500 nm (e.g., 120 nm), in accordance with some specific embodiments, although other layer thicknesses will be apparent in light of this disclosure. As previously explained, some such embodiments may include with a thin buffer between the pure germanium layer and the substrate. For instance, and as can further be seen in the example embodiment shown in Figure 3F, a source buffer 313 and a drain buffer 315 are deposited prior to depositing the in situ boron doped germanium. In some such embodiments, the buffers 313 and 315 can be a graded boron doped silicon germanium layer with the germanium composition graded from a base level concentration compatible with the underlying substrate 300 material up to 100 atomic % (or near to 100 atomic % as previously described). The thickness of the buffers 313 and 315 will vary depending on

factors such as the concentration range over which the buffer transitions and the make-up of the underlying substrate 300. In one example embodiment having a silicon germanium substrate, the buffer thickness ranges from 2 nm to 10 nm, although other suitable thicknesses can be used also. In one specific such embodiment, the boron concentration within the buffers 313 and 315 can range, for example, from a base concentration compatible with the underlying silicon germanium substrate up to a desired concentration (e.g., in excess of $1\text{E}20\text{ cm}^{-3}$ and up to $2\text{E}21\text{ cm}^{-3}$), with two specific embodiments being in excess of $2\text{E}20\text{ cm}^{-3}$ or in excess of $5\text{E}20\text{ cm}^{-3}$. In a more general sense, the boron concentration can be adjusted as necessary to provide the desired degree of conductivity, as will be appreciated in light of this disclosure.

In accordance with other example embodiments of the present invention, and as best shown in Figure 3G, the source and drain region cavities 312/314 along with their respective tip regions 312A/314A are filled with in situ boron doped silicon germanium to form source region 318 (along with epi-tip 318A) and drain region 320 (along with drain epi-tip 320A) of MOS transistor 316 in substrate 300. The boron doped silicon germanium fill is then capped with a heavily boron doped germanium layer, to provide source cap 317 and drain cap 319. In some such bilayer construction embodiments, the boron doped silicon germanium fill, which may be epitaxially deposited in one or more layers, has a germanium concentration in the range of 30 to 70 atomic %, or higher. As previously explained, this germanium concentration of the SiGe fill may be fixed or graded so as to increase from a base level (near substrate 300) to a high level (e.g., in excess of 50 atomic %, near the pure germanium cap 317/319). The boron concentration in some such embodiments can be in excess of $1\text{E}20\text{ cm}^{-3}$, such as higher than $5\text{E}20\text{ cm}^{-3}$ or $2\text{E}21\text{ cm}^{-3}$, and may also be graded so as to increase from a base level near substrate 300 to a high level (e.g., in excess of $1\text{E}20\text{ cm}^{-3}$ or $2\text{E}20\text{ cm}^{-3}$ or $3\text{E}20\text{ cm}^{-3}$, etc, near cap 317/319). In embodiments where the germanium concentration of the boron doped SiGe layer is fixed, a thin graded buffer may be used to better interface the boron doped SiGe layer with the boron doped Ge cap, as previously explained. The thickness of the boron doped SiGe deposited layer (or collection of layers) 318/320 may range, for example, from 50 to 250 nm (e.g., 60 nm), and the pure germanium cap 317/319 may have a thickness in the range, for example, of 50 to 250 nm (e.g., 50 nm), in accordance with some specific embodiments, although alternative embodiments may have other layer and cap thicknesses, as will be apparent in light of this disclosure. In some embodiments, note that

cavities may be created underneath the spacers during cyclical deposition-etch processing, and those cavities can be backfilled by an epitaxial cap layer as well (which can have, for example, the same composition as the boron doped germanium cap 317/319).

As will further be appreciated in light of this disclosure, the combination of high germanium concentration (e.g., in excess of 50 atomic % and up to pure germanium) and high boron concentration (e.g., in excess of $1\text{E}20\text{ cm}^{-3}$), such as discussed with respect to embodiments shown in Figures 3F and 3G, can be used to realize significantly higher conductance in the source and drain regions as well as their respective tip regions in PMOS SET transistor devices. Further, and as previously explained, since boron diffusion is sufficiently suppressed by pure germanium, no adverse SCE degradation is realized with subsequent thermal anneals despite high boron in the deposited stressor film. Barrier height lowering is also enabled from the higher concentration of germanium at the contact surface. In some example embodiments, a germanium concentration in excess of 95 atomic % and up to pure germanium (100 atomic %) can be used to achieve such benefits.

As further shown in Figures 3F and 3G, unlike conventional source and drain tip regions that are formed through implant and diffusion techniques and therefore have no clear boundary between the tip regions and the channel region, the self-aligned source and drain epi-tips of the MOS transistor 316 have an abrupt boundary. In other words, the interface between the source/drain epi-tips and the channel region is clear and well-defined. On one side of the interface is the heavily boron doped germanium layer (layer 318/320 of Figure 3F or cap 317/319 of Figure 3G) and on the other side of the interface is the substrate 300 material that makes up the channel region. The boron in the source/drain epi-tips 318A/320A remains substantially or completely within the epi-tips and does not tend to diffuse into the channel region, thereby enabling the heavily boron doped germanium material in very close proximity to the channel region relative to conventional techniques. For instance, in some specific embodiments, the source/drain epi-tips 318A/320A may undercut the gate dielectric layer 302 by more than 10 nm. This in turn enables the gate length to be scaled down without having to shorten the channel region.

Forming the source and drain epi-tips in relatively close proximity to the channel region also imparts a larger hydrostatic stress on the channel. This stress increases the strain within the channel, thereby increasing mobility in the channel and increasing drive current. This stress can be further amplified by increasing the germanium concentration of

the source and drain epi-tips. This is an improvement over diffusion-based processes where the tip regions generally do not induce a strain on the channel region.

Once the source and drain regions are filled in accordance with an embodiment of the present invention, various conventional MOS processing can be carried out to complete fabrication of MOS transistor 316, such as replacement gate oxide processes, replacement metal gate processes, annealing, and salicidation processes, that may further modify the transistor 316 and/or provide the necessary electrical interconnections. For instance, after the epitaxial deposition of the source/drain regions along with their respective tips, and with further reference to Figure 2, the method 200 may continue with depositing 216 an interlayer dielectric (ILD) over the transistor 316, and then planarizing the ILD layer as commonly done. The ILD layer may be formed using materials known for the applicability in dielectric layers for integrated circuit structures, such as low-k dielectric materials. Such dielectric materials include, for example, oxides such as silicon dioxide (SiO_2) and carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. In some example configurations, the ILD layer may include pores or other voids to further reduce its dielectric constant. Figure 3H illustrates an example ILD layer 322 that has been deposited and then planarized down to the hard mask 306.

Next, in some embodiments of the present invention where a replacement metal gate process is used, the method 200 continues with removing 218 the gate stack (including the high-k gate dielectric layer 302, the sacrificial gate electrode 304, and the hard mask layer 306) using an etching process as conventionally done. In alternate implementations, only the sacrificial gate 304 is removed. Figure 3I illustrates the trench opening that is formed when the gate stack is etched away, in accordance with one such embodiment. If the gate dielectric layer is removed, the method may continue with depositing 220 a new gate dielectric layer into the trench opening. Any suitable high-k dielectric materials such as those previously described may be used here, such as hafnium oxide. The same deposition processes may also be used. Replacement of the gate dielectric layer may be used, for example, to address any damage that may have occurred to the original gate dielectric layer during application of the dry and wet etch processes, and/or to replace a low-k or sacrificial dielectric material with a high-k or otherwise desired gate dielectric material.

The method 200 may then continue with depositing 222 the metal gate electrode layer into the trench and over the gate dielectric layer. Conventional metal deposition processes may be used to form the metal gate electrode layer, such as CVD, ALD, PVD, electroless plating, or electroplating. The metal gate electrode layer may include, for example, a P-type workfunction metal, such as ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. In some example configurations, two or more metal gate electrode layers may be deposited. For instance, a workfunction metal may be deposited followed by a suitable metal gate electrode fill metal such as aluminum. Figure 3J illustrates an example high-k gate dielectric layer 324 and a metal gate electrode 326 that have been deposited into the trench opening, in accordance with one embodiment.

Metalization of the source and drain contacts can be carried out using a silicidation process (generally, deposition of contact metal and subsequent annealing). For instance, silicidation with nickel, aluminum, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. The boron doped germanium epi layer allows for metal-germanide formation (e.g., nickel-germanium). The germanide allows for significantly lower Schottky-barrier height and improved contact resistance (including R_{ext}) over that in conventional metal-silicide systems. For instance, conventional transistors typically use a source/drain SiGe epi process, with germanium concentration in the range of 30-40 atomic %. Such conventional systems exhibit R_{ext} values of about 140 $\text{Ohm}\cdot\mu\text{m}$, limited by epi/silicide interfacial resistance, which is high and may impede future gate pitch scaling. Some embodiments of the present invention allow for a significant improvement in R_{ext} in PMOS devices (e.g., about a 2x improvement, or a R_{ext} of about 70 $\text{Ohm}\cdot\mu\text{m}$), which can better support PMOS device scaling. Thus, transistors having a source/drain configured with heavily boron doped germanium in accordance with an embodiment of the present, with a boron concentration in excess of $1\text{E}20\text{ cm}^{-3}$ and a germanium concentration in excess of 50 atomic % and up to or otherwise near pure germanium (100 atomic %) at the interface between the source/drain epi-tips and the channel region, can exhibit R_{ext} values of less than 100 $\text{Ohm}\cdot\mu\text{m}$, and in some cases less than 90 $\text{Ohm}\cdot\mu\text{m}$, and in some cases less than 80 $\text{Ohm}\cdot\mu\text{m}$, and in some cases less than 75 $\text{Ohm}\cdot\mu\text{m}$, or lower.

Accordingly, self-aligned source and drain epi-tips have been disclosed that reduce the overall resistance of the MOS transistor and increase channel strain due to increased boron doped germanium volume (e.g., boron doped germanium or boron doped silicon germanium volume with a germanium cap). In some such embodiments, the source and drain epi-tips do not have a bulleted profile, form an abrupt boundary between the channel region and the source and drain regions, and/or have a doping concentration that is more readily controlled, yielding a more optimized source-drain profile. Furthermore, by selecting an appropriate combination of a dopant and an etchant recipe in accordance with some embodiments, the source and drain epi-tips can be etched without being substantially impacted by the spacer thickness. This self-aligned process can therefore be used to increase performance while minimizing process variation, where desirable to do so.

FinFET Configuration

As is known, FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin). The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, a source region, and a drain region. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both sidewalls of the fin (sides perpendicular to the substrate surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate FinFET. Other types of FinFET configurations are also available, such as so-called double-gate FinFETs, in which the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin).

Figure 4 shows a perspective view of an example tri-gate architecture, configured in accordance with one embodiment of the present invention. As can be seen, the tri-gate device includes a substrate 400 having a semiconductor body or fin 260 (represented by dashed lines) extending from the substrate 400 through isolation regions 710, 720. A gate electrode 340 is formed over 3 surfaces of the fin 260 to form 3 gates. A hard mask 410 is formed on top of the gate electrode 340. Gate spacers 460, 470 are formed at opposite sidewalls of the gate electrode 340. A source region comprises the epitaxial region 531 formed on a recessed source interface 266 and on one fin 260 sidewall, and a drain region comprises the epitaxial region 531 formed on a recessed source interface 266 and on the opposing fin 260 sidewall (not shown). A cap layer 541 is deposited over the epitaxial

regions 531. In one embodiment, the isolation regions 710, 720 are shallow trench isolation (STI) regions formed by common techniques, such as etching the substrate 200 to form trenches, and then depositing oxide material onto the trenches to form the STI regions. The isolation regions 710, 720 can be made from any well known insulative material, such as SiO₂. The previous discussion with respect to the substrate 102 is equally applicable here (e.g., substrate 400 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).

As will be appreciated in light of this disclosure, conventional processes and forming techniques can be used to fabricate the tri-gate transistor structure. However, and in accordance with one example embodiment of the present invention, the bilayer structure of the epitaxial region 531 and cap layer 541 can be implemented using an in situ boron doped silicon germanium capped with a heavily boron doped germanium, with an optional germanium and/or boron graded buffer between the two bilayers. As previously explained, such a buffer may be used to transition from a base level germanium/boron concentration compatible with the boron doped SiGe deposited for epitaxial region 531 in the recessed source interface 266 to the heavily boron doped germanium cap 541. Alternatively, germanium and/or boron concentration grading can be implemented directly in the epitaxial region 531, rather than in an intervening graded buffer arrangement. As will further be appreciated, note that an alternative to the tri-gate configuration is a double-gate architecture, which includes a dielectric/isolation layer on top of the fin 260.

Figure 5 is a graph illustrating an improvement made available by using self-aligned source and drain epi-tips configured in accordance with one example embodiment of the present invention. Line 500 represents data collected for MOS devices built using techniques provided herein. As shown, the UC-to-UC distance is much less impacted by spacer thickness than devices formed using conventional processes, the data for which is again represented by line 118. Figures 6A and 6B further demonstrate improvements enabled by using self-aligned source and drain epi-tips configured in accordance with one example embodiment of the present invention. In particular, Figure 6A illustrates Schottky barrier NiGe diode measurements (leakage v. voltage), confirming that the nickel-germanium workfunction is very p-type (roughly 85 mV above the Ge valance band). Figure 6B plots simulation data that shows that such germanide materials and Schottky barrier height improvement enables more than a 2x Rext improvement over that in conventional SiGe source/drain PMOS devices, in accordance with some example embodiments of the present invention. As is known, the Schottky barrier height is the

rectifying barrier for electrical conduction across a semiconductor-metal junction. The magnitude of the Schottky barrier height reflects a mismatch in the energy position of the metal's Fermi level and the majority carrier band edge of the semiconductor across the semiconductor-metal interface. For a p-type semiconductor-metal interface, the Schottky barrier height is the difference between the metal Fermi level and the valence band maximum of the semiconductor.

Thus, and as will be appreciated in light of this disclosure, various embodiments of the present invention provided herein can be used to address several transistor scaling issues, such as providing for higher channel mobility with pitch and power supply (V_{cc}) scaling, providing reduced source/drain and contact resistance, providing for improved channel abruptness, providing reduced barrier height between salicide and source/drain to minimize overall parasitic resistance, particularly in planar and non-planar architectures. Numerous embodiments will be apparent in light of this disclosure.

One example embodiment of the present invention provides a transistor device. The device includes a substrate having a channel region. The device further includes a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The device further includes source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $1E20\text{ cm}^{-3}$. In one such case, the device is one of a planar or FinFET PMOS transistor. In another such case, the device may include metal-germanide source and drain contacts. In another such case, the device may include an interlayer dielectric over the source and drain regions. In another such case, the device may include a buffer between the substrate and the boron doped germanium layer. In one such specific case, the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %. In another such specific case, the buffer has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $1E20\text{ cm}^{-3}$. In another particular embodiment, the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron

doped germanium cap thereon. In one such specific case, the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %. In another such specific case, the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $1\text{E}20\text{ cm}^{-3}$. In another such specific case, the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of $1\text{E}20\text{ cm}^{-3}$. In another particular case, the transistor has a R_{ext} value of less than $100\text{ Ohm}\cdot\mu\text{m}$ (such as $R_{\text{ext}} = 70\text{ Ohm}\cdot\mu\text{m}$, $\pm 10\%$). As will be appreciated, the boron concentration can be set higher based on factors such as desired conductivity, and in some such example cases is in excess of $2\text{E}20\text{ cm}^{-3}$ or $3\text{E}20\text{ cm}^{-3}$ or $4\text{E}20\text{ cm}^{-3}$ or $5\text{E}20\text{ cm}^{-3}$ or $2\text{E}21\text{ cm}^{-3}$.

Another embodiment of the present invention provides a transistor device. In this example case, the device includes a substrate having a channel region and a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The device further includes source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $2\text{E}20\text{ cm}^{-3}$. The device further includes metal-germanide source and drain contacts. In some such cases, the device may further include a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of

$2 \times 10^{20} \text{ cm}^{-3}$. In other example cases, the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon. In some such specific cases, the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %. In some such specific embodiments, the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $2 \times 10^{20} \text{ cm}^{-3}$. In other specific cases, the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a thin buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of $2 \times 10^{20} \text{ cm}^{-3}$, the buffer having a thickness of less than 100 Angstroms.

Another embodiment of the present invention provides a method for forming a transistor device. The method includes providing a substrate having a channel region, and providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The method continues with forming source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $1 \times 10^{20} \text{ cm}^{-3}$. In some such embodiments, the method further includes providing a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $1 \times 10^{20} \text{ cm}^{-3}$. In other embodiments, the boron doped germanium layer has a bilayer construction comprising a boron doped

silicon germanium portion and a boron doped germanium cap thereon. In one such case, the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %. In another such case, the boron doped silicon germanium portion has a fixed germanium concentration, and the method further includes providing a buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of $1E20\text{ cm}^{-3}$. In some such cases, the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $1E20\text{ cm}^{-3}$.

The foregoing description of example embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. For instance, while some embodiments of the present invention utilize in situ boron doping of germanium, other embodiments may use an intrinsic germanium that after its deposition is subsequently subjected to boron implantation and annealing processes to provide the desired boron doping concentration. Moreover, some embodiments may include source and drain regions fabricated as described herein (e.g., having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $1E20\text{ cm}^{-3}$), but still use conventional processing (e.g., implantation and annealing) to form the tips of the source and drain regions. In such embodiments, the tips may have a lower germanium and/or boron concentration than the main source/drain region, which may be acceptable in some applications. In still other embodiments, only tips of the source and drain regions may be configured with the high germanium and boron concentrations and the main portions of the source and drain regions may have conventional or otherwise lower germanium/boron concentrations. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

CLAIMS

What is claimed is:

1. A transistor device, comprising:
a substrate having a channel region;
a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode; and
source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $1\text{E}20\text{ cm}^{-3}$.
2. The device of claim 1 wherein the device is one of a planar or FinFET PMOS transistor.
3. The device of claim 1 further comprising metal-germanide source and drain contacts.
4. The device of claim 1 further comprising an interlayer dielectric over the source and drain regions.
5. The device of claim 1, the device further comprising:
a buffer between the substrate and the boron doped germanium layer.
6. The device of claim 5 wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %.
7. The device of claim 6 wherein the high concentration reflects pure germanium.
8. The device of claim 5 wherein the buffer has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $1\text{E}20\text{ cm}^{-3}$.
9. The device of claim 1 wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon.

10. The device of claim 9 wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %.

11. The device of claim 9 wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $1E20\text{ cm}^{-3}$.

12. The device of claim 9 wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of $1E20\text{ cm}^{-3}$.

13. The device of claim 9 wherein the transistor has a R_{ext} value of less than $100\text{ Ohm}\cdot\mu\text{m}$.

14. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $2E20\text{ cm}^{-3}$; and

metal-germanide source and drain contacts.

15. The device of claim 14, the device further comprising:

a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in

excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $2 \times 10^{20} \text{ cm}^{-3}$.

16. The device of claim 14 wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon.

17. The device of claim 16 wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %.

18. The device of claim 17 wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $2 \times 10^{20} \text{ cm}^{-3}$.

19. The device of claim 16 wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a thin buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of $2 \times 10^{20} \text{ cm}^{-3}$, the buffer having a thickness of less than 100 Angstroms.

20. A method for forming a transistor device, comprising:

providing a substrate having a channel region;

providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode; and

forming source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $1 \times 10^{20} \text{ cm}^{-3}$.

21. The method of claim 20, further comprising:
providing a buffer between the substrate and the boron doped germanium layer,
wherein the buffer has a germanium concentration that is graded from a
base level concentration compatible with the substrate to a high
concentration in excess of 95 atomic %, and a boron concentration that is
graded from a base level concentration compatible with the substrate to a
high concentration in excess of $1\text{E}20\text{ cm}^{-3}$.
22. The method of claim 20 wherein the boron doped germanium layer has a
bilayer construction comprising a boron doped silicon germanium portion and a boron
doped germanium cap thereon.
23. The method of claim 22 wherein the boron doped silicon germanium
portion has a germanium concentration that is graded from a base level concentration
compatible with the substrate to a high concentration in excess of 50 atomic %, and the
boron doped germanium cap has a germanium concentration in excess of 95 atomic %.
24. The method of claim 22 wherein the boron doped silicon germanium
portion has a fixed germanium concentration, and the method further comprises providing
a buffer between the boron doped silicon germanium portion and the boron doped
germanium cap, the buffer having a germanium concentration that is graded from a base
level concentration compatible with the boron doped silicon germanium portion to a high
concentration in excess of 50 atomic %, and a boron concentration that is graded from a
base level concentration compatible with the boron doped silicon germanium portion to a
high concentration in excess of $1\text{E}20\text{ cm}^{-3}$.
25. The method of claim 24 wherein the boron doped silicon germanium
portion has a boron concentration that is graded from a base level concentration
compatible with the substrate to a high concentration in excess of $1\text{E}20\text{ cm}^{-3}$.

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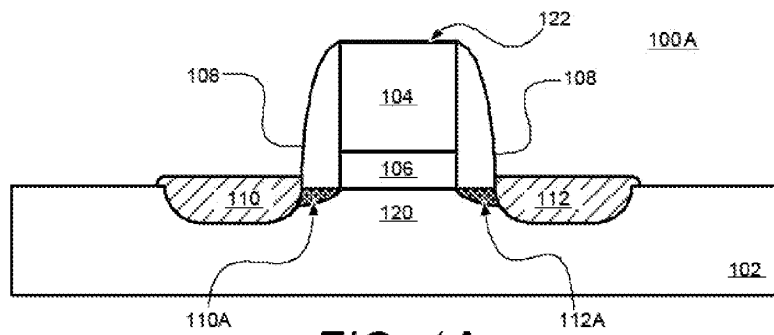


FIG. 1A

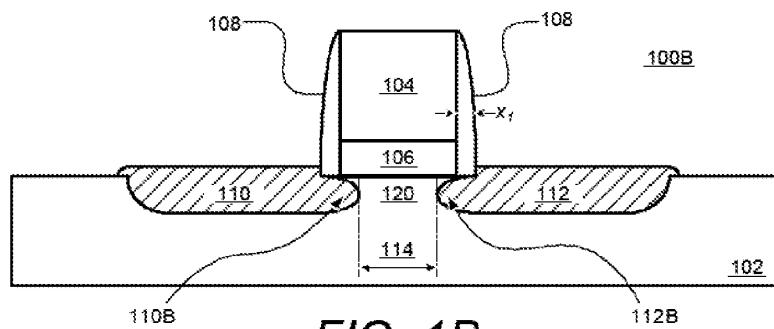


FIG. 1B

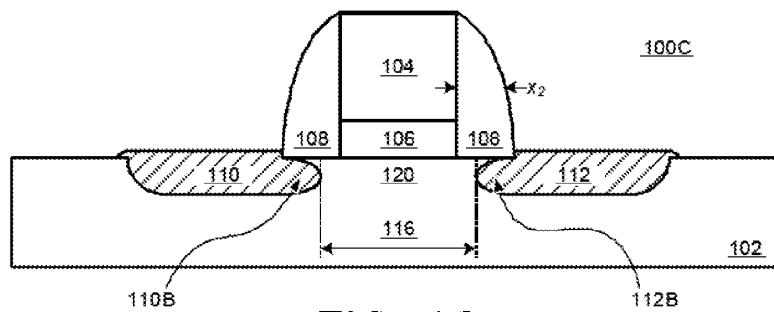
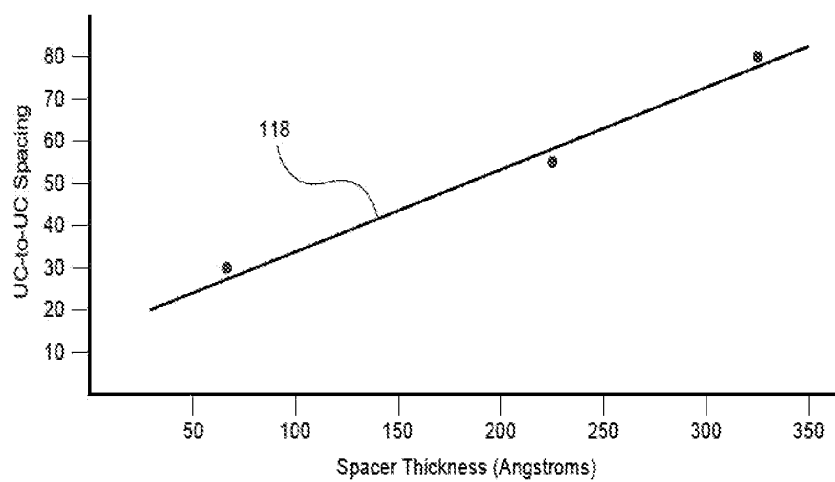
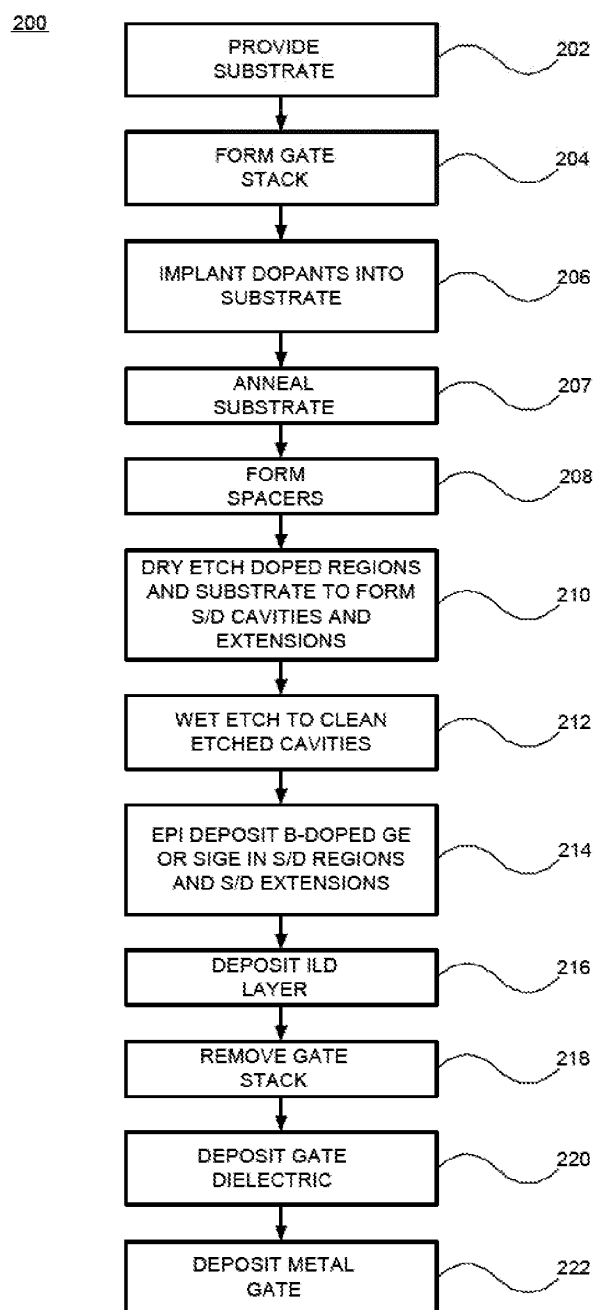


FIG. 1C

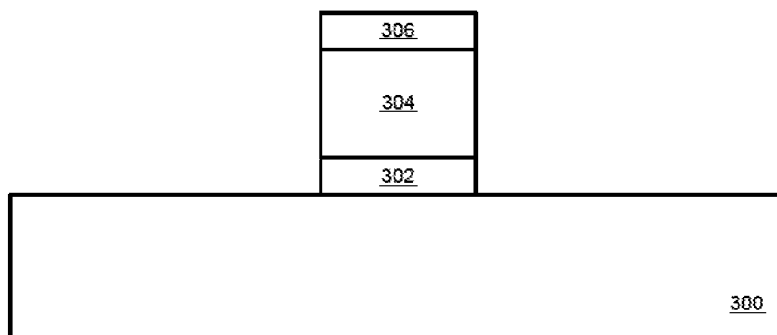
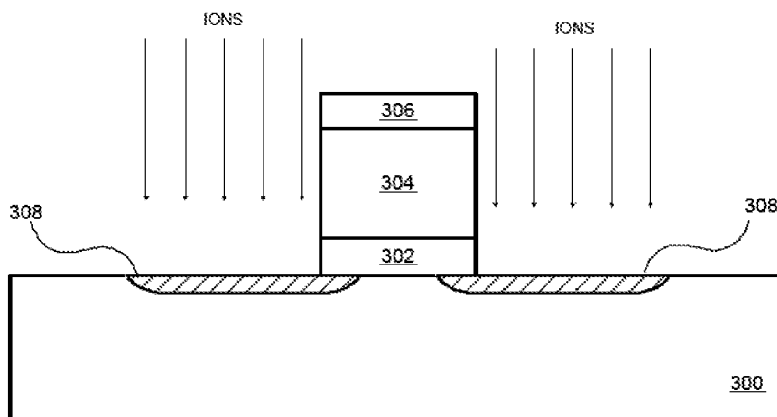
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*FIG. 1D*

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*FIG. 3A**FIG. 3B*

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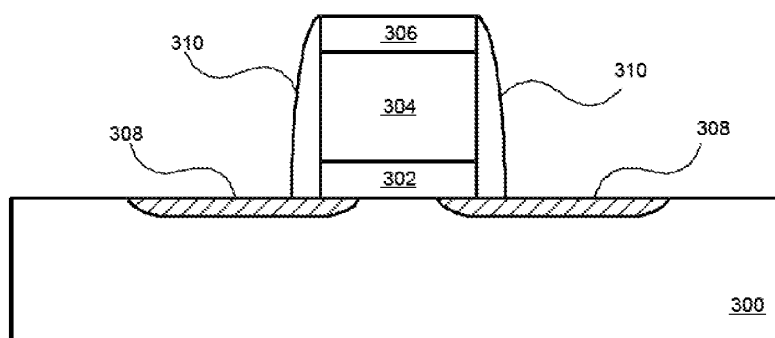


FIG. 3C

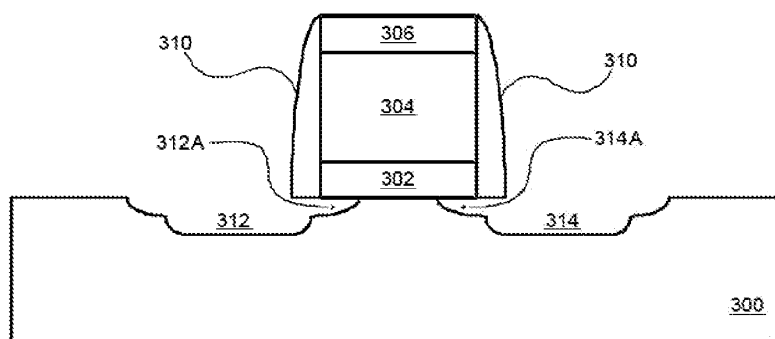


FIG. 3D

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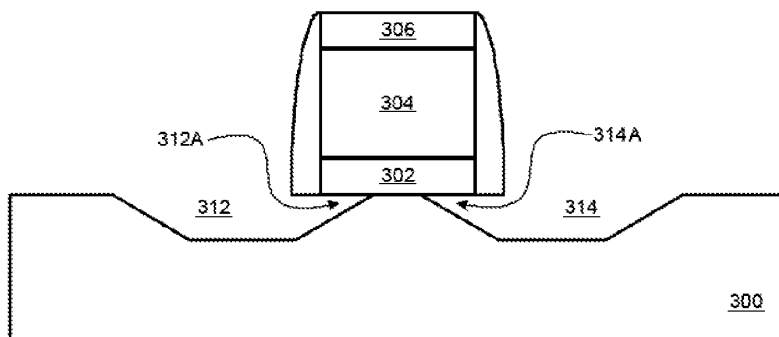


FIG. 3E

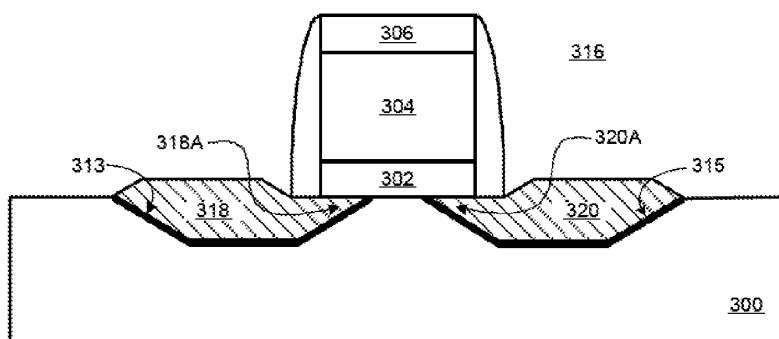


FIG. 3F

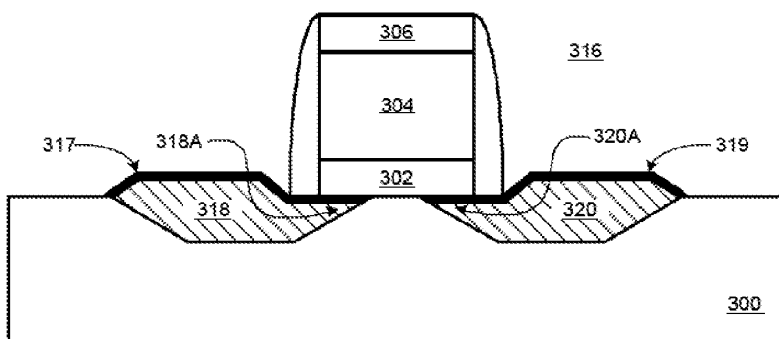


FIG. 3G

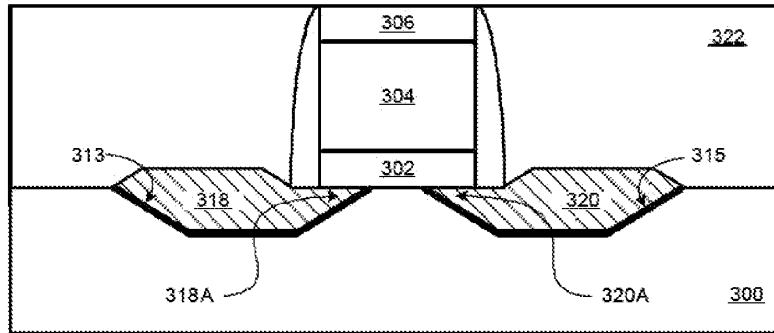


FIG. 3H

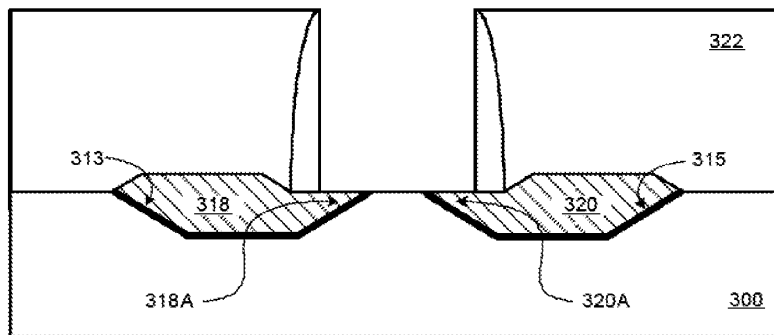


FIG. 3I

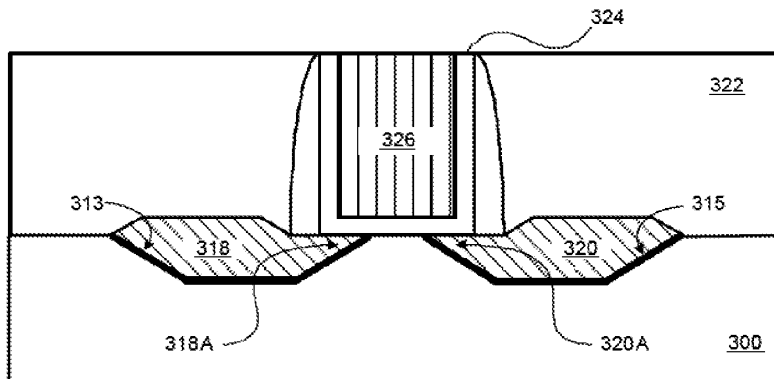


FIG. 3J

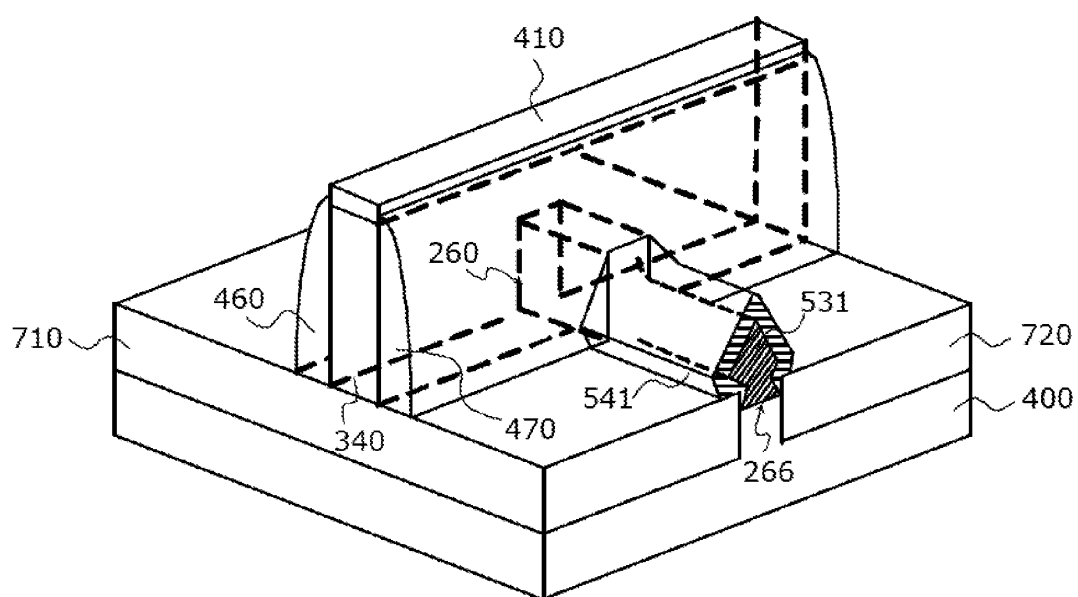
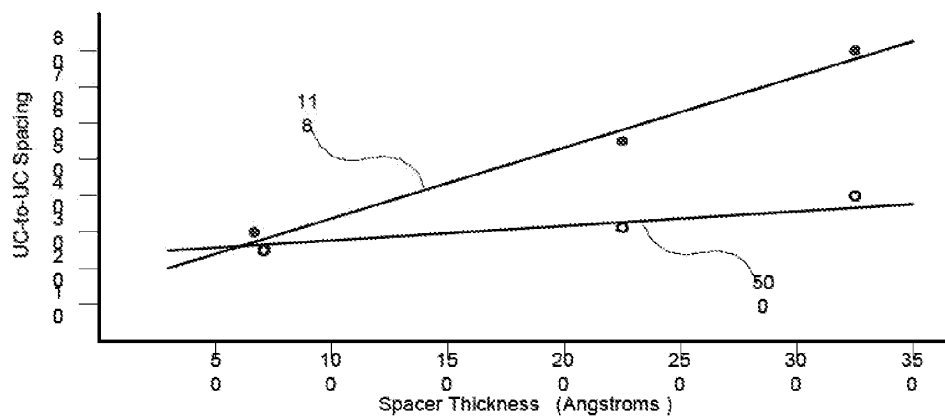


FIG. 4

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*FIG. 5*

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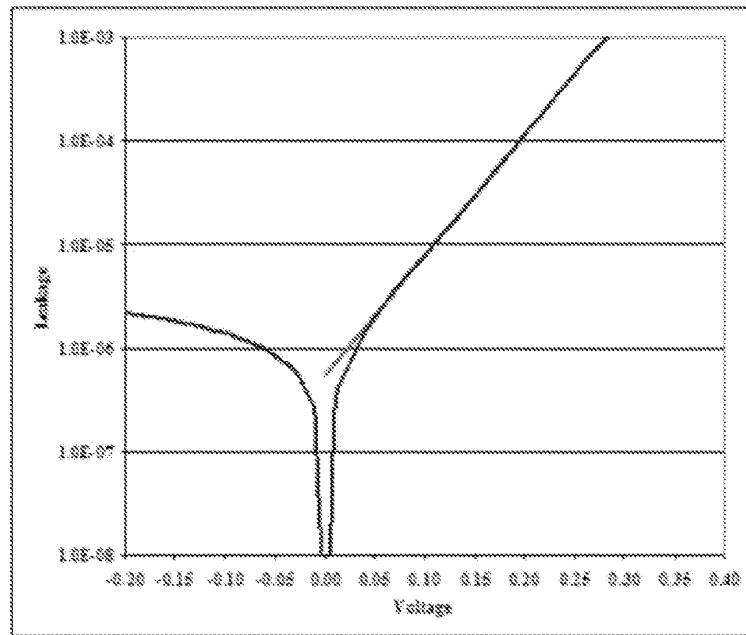


FIG. 6A

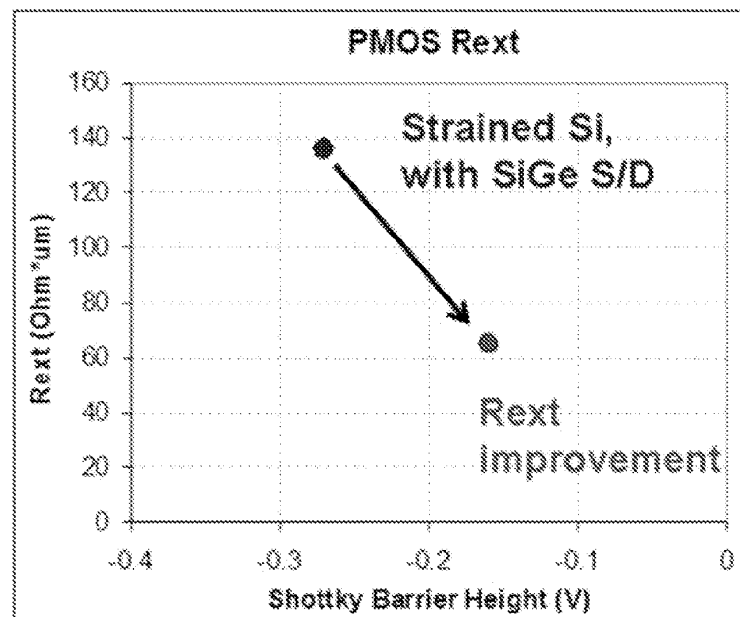


FIG. 6B

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(54) Title: COLUMN IV TRANSISTORS FOR PMOS INTEGRATION

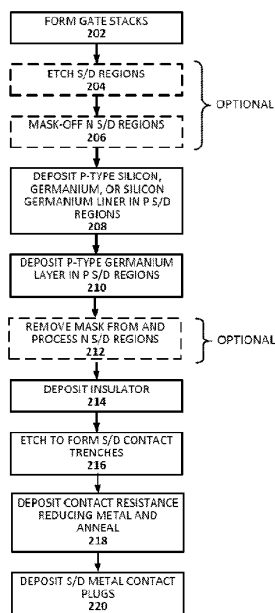


FIG. 2

(57) Abstract: Techniques are disclosed for forming column IV transistor devices having source/drain regions with high concentrations of germanium, and exhibit reduced parasitic resistance relative to conventional devices. In some example embodiments, the source/drain regions each includes a thin p-type silicon or germanium or SiGe deposition with the remainder of the source/drain material deposition being p-type germanium or a germanium alloy (e.g., germanium:tin or other suitable strain inducer, and having a germanium content of at least 80 atomic % and 20 atomic % or less other components). In some cases, evidence of strain relaxation may be observed in the germanium rich cap layer, including misfit dislocations and/or threading dislocations and/or twins. Numerous transistor configurations can be used, including both planar and non-planar transistor structures (e.g., FinFETs and nanowire transistors), as well as strained and unstrained channel structures.

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GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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COLUMN IV TRANSISTORS FOR PMOS INTEGRATION

5

RELATED APPLICATION

This application is a continuation-in-part of and claims priority to U.S. Application No. 12/975,278 filed December 21, 2010.

10

BACKGROUND

Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to minimize the parasitic resistance associated with contacts otherwise known as external resistance R_{ext} . Decreased R_{ext} enables higher current from an equal transistor design.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 schematically illustrates components of resistance of a typical MOS transistor that includes source and drain tip regions.

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Figure 2 is a method of forming a column IV transistor in accordance with an embodiment of the present invention.

Figures 3A to 3F illustrate structures that are formed when carrying out the method of Figure 2, in accordance with various embodiments of the present invention.

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Figures 4A to 4G each shows a perspective view of a FinFET transistor structures formed in accordance with one embodiment of the present invention.

Figures 5A and 5B each shows a perspective view of a nanowire transistor structure formed in accordance with an embodiment of the present invention.

30

Figure 6 illustrates a computing system implemented with one or more transistor structures in accordance with an example embodiment of the present invention.

As will be appreciated, the figures are not necessarily drawn to scale or intended to limit the claimed invention to the specific configurations shown. For instance, while some figures generally

indicate straight lines, right angles, and smooth surfaces, an actual implementation of a transistor structure may have less than perfect straight lines and/or right angles, and some features may have surface topology or otherwise be non-smooth, given real world limitations of the processing equipment and techniques used. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

Techniques are disclosed for forming column IV transistor devices having source and drain regions with high concentrations of germanium, and exhibit reduced parasitic resistance relative to conventional devices. In some example embodiments, the source/drain regions of the resulting transistor structure each includes a thin p-type silicon or germanium or silicon germanium (SiGe) liner layer with the remainder of the source/drain material being p-type germanium or a germanium alloy comprising, for instance, germanium and tin, and having a germanium content of at least 80 atomic % (and 20 atomic % or less other components, such as tin and/or other suitable strain inducers). In some example cases, evidence of strain relaxation may be observed in this germanium rich layer including misfit dislocations and/or threading dislocations. Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., FinFETs and nanowire transistors), as well as strained and unstrained channel structures. The techniques are particularly well-suited for implementing p-type MOS (PMOS) devices, although other transistor configurations may benefit as well.

General Overview

As previously explained, increased drive current in the transistors can generally be achieved by reducing device external resistance, R_{ext} . However, PMOS transistor performance is a function of various component resistances within the device, as can be seen with reference to Figure 1. Channel resistance R_1 can be modulated through carrier mobility, which is a function of compressive strain within the channel. External resistance R_{ext} of the device includes tip resistance R_2 (tip region is also referred to as source/drain extension), source/drain resistance R_3 , and contact resistance R_4 (metal to semiconductor). All of these segmented resistances have a material component (e.g., energy barrier across an interface, carrier concentration and mobility) a geometry component (e.g., length, width, etc) and a dynamic electrical load component (current crowding).

Thus, and in accordance with some embodiments of the present invention, replacing the typical silicon or SiGe alloy materials in the source/drain regions with a p-type thin liner and high

content of germanium (with very high p-type doping concentration) minimizes the external resistance components (R2, R3, and R4). In addition, by introducing a highly compressively strained material, the channel hole mobility is maximized or otherwise increased and hence reduces channel resistance (R1). The net impact of decreased channel, tip, source/drain and contact resistance is improved transistor current for a given voltage (relative to threshold voltage, V_t , i.e. $V - V_t$).

In some example cases, the thin liner is p-type doped silicon or or germanium or SiGe alloy, and is generally less than 50% of the total source/drain deposition layer thickness. The remaining source/drain deposition layer thickness is generally greater than 50% of the total source/drain deposition layer thickness and can be, for example, p-type doped germanium or a germanium alloy such as germanium:tin or germanium:tin:x (where x is, for example, silicon or other marginal component or process/diffusion-based artifact) having at least 80 atomic % germanium and 20 atomic % or less of other constituents (e.g., tin and/or any other suitable strain inducer and/or other marginal unintentional components). In some specific such example embodiments, the thickness ratio of the source/drain liner to the high concentration germanium cap is about 1:5 or less (where the liner makes up about 20% or less of the total source/drain deposition layer thickness). In some such example cases, the thickness liner is one to several monolayers.

The techniques can be used to form transistor devices in any number of devices and systems. In some embodiments, such as CMOS devices having both n-type MOS (NMOS) and PMOS transistors, selectivity can be achieved in various ways. In one embodiment, for instance, deposition on NMOS source/drain locations can be avoided by having NMOS regions masked off during PMOS deposition. In other embodiments, selectivity may include natural selectivity. For instance, while boron doped germanium grows on p-type SiGe (or silicon) source drain regions, it does not grow on insulator surfaces such as silicon dioxide (SiO_2) or silicon nitride (SiN); nor does it grow on, for instance, exposed heavily phosphorous doped silicon in n-type regions.

The techniques provided herein can be employed to improve device resistance in any number of transistor structures and configurations, including planar, flush or raised source/drain, non-planar (e.g., nanowire transistors and finned transistors such as double-gate and trigate transistor structures), as well as strained and unstrained channel structures. The source/drain areas can be recessed (e.g., using an etch process) or not recessed (e.g., formed on top surface of substrate). In addition, the transistor devices may optionally include source and drain tip regions that are designed, for instance, to decrease the overall resistance of the transistor while improving short channel effects

(SCE), but such tip regions are not required. The transistor devices may further include any number of gate configurations, such as poly gates, high-k dielectric metal gates, replacement metal gate (RMG) process gates, or any other gate structure. Any number of structural features can be used in conjunction with low resistance transistor techniques as described herein.

5 A transmission electron microscopy (TEM) cross-section perpendicular to gate lines or secondary ion mass spectrometry (SIMS) profile can be used to show the germanium concentration in the structure, as profiles of epitaxial alloys of silicon and SiGe can readily be distinguished from high germanium concentration profiles, in accordance with some embodiments. In some such silicon-containing substrate cases, by forgoing the typical requirement to maintain strained
10 (dislocation free) source/drain regions, the lattice dimension mismatch between the source/drain fill material and silicon channel can be increased by at least 2X for pure germanium and even more for germanium-tin alloys. While not 100% of the strain is able to transfer to the channel in cases where dislocations are present in the germanium rich cap layer, post deposition thermal treatments can be used to provide a clear transistor performance (current at a given $V_g - V_t$) gain even for relaxed films
15 (as described herein) relative to strained SiGe controls. As will be appreciated, relaxed generally means that the films can have misfit dislocations present, but may also refer to a plastic relaxation mechanism which involves dislocation formation and propagation. A process of elastic relaxation becomes possible in non-planar configurations such as FinFET (e.g., tri-gate) and nanowire structures where the strained material is not fully constrained by the substrate. Thus, the in-plane
20 lattice constant has more flexibility to expand or contract independent of the substrate and this process does not require formation and propagation of misfit dislocations. Going forward herein, the word relaxation is used in the sense of plastic relaxation and not in the sense of elastic relaxation. The use of tin or other suitable strain inducers to alloy the high concentration germanium cap as described herein can optionally be used to increase the strain in the channel
25 region, and thereby further reduce the overall device resistance via reduction in resistance R_1 in Figure 1. As will further be appreciated, while defect free pure germanium may be desirable, it is generally difficult to grow defect free for deposition on, for example, a silicon substrate or even SiGe substrate having say 50 atomic% germanium. Surprisingly, however, if performance of a typical fully strained SiGe layer and such a germanium-rich layer having some defects (e.g., has
30 misfit and/or threading dislocations) were compared, then the defective germanium-rich layer would perform better. As will be appreciated, this result is generally not intuitive, as it runs counter to the conventional understanding with respect to thin film. In any case, while some embodiments of the

present invention may include germanium-rich caps that are lacking in crystal features such as misfit dislocations, threading dislocations and twins (defects resulting from a change in lattice orientation across a twin plane), other embodiments may include germanium-rich caps that have one or more such features.

5

Architecture and Methodology

Figure 2 is a method of forming a column IV transistor in accordance with an embodiment of the present invention. Figures 3A to 3F illustrate example structures that are formed when carrying out the method of Figure 2, in accordance with various embodiments. One or more such transistors
10 may be formed in the fabrication of, for example, a processor or a communications chip or memory chip. Such integrated circuits can then be used in various electronic devices and systems.

The example method includes forming 202 one or more gate stacks on a semiconductor substrate upon which a MOS device may be formed. The MOS device may comprise, for example, PMOS transistors, or both NMOS and PMOS transistors (e.g., for CMOS devices). Figure 3A
15 shows an example resulting structure, which in this case includes a PMOS transistor formed on substrate 300. As can be seen, the gate stack is formed over a channel region, and includes a gate dielectric layer 302, a gate electrode 304, and an optional hardmask 306. Spacers 310 are formed adjacent to the gate stack.

The gate dielectric 302 can be, for example, any suitable oxide such as silicon dioxide (SiO_2)
20 or high-k gate dielectric materials. Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may
25 be carried out on the gate dielectric layer 302 to improve its quality when a high-k material is used. In some specific example embodiments, the high-k gate dielectric layer 302 may have a thickness in the range of 5 Å to around 100 Å thick (e.g., 10 Å). In other embodiments, the gate dielectric layer 302 may have a thickness of one monolayer of oxide material. In general, the thickness of the gate dielectric 302 should be sufficient to electrically isolate the gate electrode 304 from the source and
30 drain contacts. In some embodiments, additional processing may be performed on the high-k gate dielectric layer 302, such as an annealing process to improve the quality of the high-k material.

The gate electrode 304 material can be, for example, polysilicon, silicon nitride, silicon carbide, or a metal layer (e.g., tungsten, titanium nitride, tantalum, tantalum nitride) although other suitable gate electrode materials can be used as well. The gate electrode 304 material, which may be a sacrificial material that is later removed for a replacement metal gate (RMG) process, has a thickness in the range of about 10Å to 500Å (e.g., 100Å), in some example embodiments.

The optional gate hard mask layer 306 can be used to provide certain benefits or uses during processing, such as protecting the gate electrode 304 from subsequent etch and/or ion implantation processes. The hard mask layer 306 may be formed using typical hard mask materials, such as silicon dioxide, silicon nitride, and/or other conventional insulator materials.

The gate stack can be formed as conventionally done or using any suitable custom techniques (e.g., conventional patterning process to etch away portions of the gate electrode and the gate dielectric layers to form the gate stack, as shown in Figure 2A). Each of the gate dielectric 302 and gate electrode 304 materials may be formed, for example, using conventional deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Alternate deposition techniques may be used as well, for instance, the gate dielectric 302 and gate electrode 304 materials may be thermally grown. As will be appreciated in light of this disclosure, any number of other suitable materials, geometries, and formation processes can be used to implement an embodiment of the present invention, so as to provide a low resistance transistor device or structure as described herein.

The spacers 310 may be formed, for example, using conventional materials such as silicon oxide, silicon nitride, or other suitable spacer materials. The width of the spacers 310 may generally be chosen based on design requirements for the transistor being formed. In accordance with some embodiments, however, the width of the spacers 310 is not subject to design constraints imposed by the formation of the source and drain tip regions, given sufficiently high p-doped germanium content (e.g., boron doped germanium) or SiGe alloy liner in the source/drain tip regions.

Any number of suitable substrates can be used to implement substrate 300, including bulk substrates, semiconductors-on-insulator substrates (XOI, where X is a semiconductor material such as silicon, germanium, or germanium-enriched silicon), and multi-layered structures, including those substrates upon which fins or nanowires can be formed prior to a subsequent gate patterning process. In some specific example cases, the substrate 300 is a germanium or silicon or SiGe bulk substrate, or a germanium or silicon or SiGe on oxide substrate. Although a few examples of materials from which the substrate 300 may be formed are described here, other suitable materials

that may serve as a foundation upon which a low resistance transistor device may be built falls within the spirit and scope of the claimed invention.

With further reference to Figure 3A, after the one or more gate stacks are formed, the method continues with some optional processing which in this example embodiment includes etching 204 the source/drain regions of the transistor structure, and masking-off 206 any NMOS source/drain regions of the structure (if present). As will be appreciated, the source/drain regions need not be recessed or otherwise etched. In such cases, the source/drain materials can be formed on the substrate 300 without any etching. While such non-recessed source/drain regions will not impact channel resistance, a bi-layer source/drain structure having a thin liner and high germanium content cap can still be implemented to provide low contact resistance, in accordance with some embodiments. As will further be appreciated, not all embodiments will include n-type regions. In some example cases, for instance, the circuit being fabricated may include only PMOS devices. In such example cases, there would be no n-type source/drain regions to mask off. When n-type regions are present, any suitable masking technique can be used to protect the n-type regions during p-type processing.

In example embodiments where the source/drain regions are etched, source/drain cavities 312/314 result, as best shown in Figure 3A. The cavities effectively define the location of the source/drain regions. As can be further seen, substrate 300 has been etched not only to provide source/drain cavities 312/314, but also their respective tip areas 312A/314A which undercut the gate dielectric 302. The cavities 312/314 and their respective tip areas 312A/314A can be formed as conventionally done using any number of suitable processes. In some example cases, this includes ion implantation to highly dope portions of substrate 300 adjacent to gate stack followed by annealing to drive the dopants further into substrate 300 to improve the etch rate of the intended source/drain areas. A dry etch process can then be used to etch the doped regions of substrate 300 to form cavities 312/314 and their respective tip areas 312A/314A. After the dry etch process has completed, a wet etch may be used, for instance, to clean and further etch the cavities 312/314 and their respective tip areas 312A/314A. Such wet etching, which can be carried out using conventional or custom wet etch chemistries, can be used to remove contaminants such as carbon, fluorine, chlorofluorocarbons, and oxides such as silicon oxide to provide a clean surface upon which subsequent processes may be carried out. In addition, and assuming a monocrystalline silicon substrate, the wet etching may also be used to remove a thin portion of substrate 300 along the <111> and <001> crystallographic planes to provide a smooth surface upon which a high quality

epitaxial deposition may occur. In some example cases, the thin portion of substrate 300 that is etched away may be, for example, up to 5 nm thick and may also remove residual contaminants. The wet etching generally causes edges of the cavities 312/314 and their respective tip areas 312A/314A to follow the <111> and <001> crystallographic planes.

5 With further reference to Figure 2, the method continues with depositing 208 a p-type silicon or germanium or SiGe liner 313/315 in the p-type source/drain regions, and then depositing 210 a p-type germanium or germanium alloy in the p-type source/drain regions over the liner 313/315. Each of these depositions can be carried out, for instance, using selective epitaxial deposition, although any suitable deposition process can be used. As can be seen with reference to Figure 3B, the p-type
10 silicon or germanium or SiGe liners 313/315 are deposited into cavities 312/314 and their respective tip areas 312A/314A. In addition, and as best shown in Figure 3C, cavities 312/314 and tip areas 312A/314A have been further filled to provide a thick capping layer of p-type germanium or germanium alloy 318/320 over the p-type liners 313/315. Example p-type dopants include, for instance, boron, gallium, or any other suitable p-type dopant or dopants, as will be appreciated, and
15 the claimed invention is not intended to be limited to any particular one.

 In accordance with some specific example embodiments where the substrate 300 is a silicon or SiGe bulk substrate, or a semiconductor-on-insulator substrate (XOI, where X is silicon or SiGe), the source and drain cavities 312/314 along with their respective tip areas 312A/314A are filled with in-situ boron doped silicon or SiGe thereby forming the corresponding liners 313/315, and then
20 further filled with in-situ boron doped germanium or germanium rich alloy to provide caps 318/320. In other example embodiments where the substrate 300 is a germanium bulk substrate or a germanium-on-insulator substrate, the source and drain cavities 312/314 along with their respective tip areas 312A/314A can be filled with in-situ boron doped germanium thereby forming the corresponding liners 313/315, and then further filled with in-situ boron doped germanium rich alloy
25 (such as germanium:tin) to provide caps 318/320. As will be appreciated in light of this disclosure, the respective germanium and p-type dopant concentrations of the liners 313/315 and caps 318/320 can vary depending on factors such as the composition of the substrate 300, the use of grading for lattice matching/compatibility, and the overall desired thickness of the total source/drain deposition. Numerous material system and p-type doping configurations can be implemented, as will be
30 appreciated in light of this disclosure.

 For instance, in some example embodiments having a silicon or germanium or SiGe substrate, the germanium concentration of the liners 313/315 can be in the range of 20 atomic % to 100 atomic

%, and the boron concentration is in the range of $1\text{E}20\text{ cm}^{-3}$ to $2\text{E}21\text{ cm}^{-3}$. To avoid lattice mismatch with an underlying silicon-containing substrate, the germanium concentration of the liners 313/315 can be graded, in accordance with some embodiments. For example, in one such embodiment, the liners 313/315 can be a graded boron doped SiGe layer with the germanium composition graded from a base level concentration compatible with the underlying silicon or SiGe substrate 300 up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). In one specific such embodiment, the germanium concentration ranges from 40 atomic % or less to in excess of 98 atomic %. The boron concentration within liners 313/315 can be fixed, for example, at a high level, or alternatively can be graded. For instance, for example, the boron concentration within liners 313/315 can be graded from a base concentration at or otherwise compatible with the underlying substrate 300 up to a desired high concentration (e.g., in excess of $1\text{E}20\text{ cm}^{-3}$, in excess of $2\text{E}20\text{ cm}^{-3}$, or in excess of $5\text{E}20\text{ cm}^{-3}$). In some such embodiments, the boron doped germanium caps 318/320 have a boron concentration in excess of $1\text{E}20\text{ cm}^{-3}$, such as in excess of $2\text{E}20\text{ cm}^{-3}$ or in excess of $2\text{E}21\text{ cm}^{-3}$, or higher. This boron concentration in the caps 318/320 can be graded in a similar fashion as described with reference to the liners 313/315. In a more general sense, the boron concentrations can be adjusted as necessary to provide the desired degree of conductivity, as will be appreciated in light of this disclosure. The germanium concentration of the caps 318/320 can be, for instance, fixed at 100 atomic%. Alternatively, germanium concentration of the caps 318/320 can be graded from a low to high concentration (e.g., from 20 atomic % to 100 atomic %), as will be appreciated in light of this disclosure, to account for lattice mismatch between the liners 313/315 and the desired peak germanium concentration of the caps 318/320. In still other embodiments, the caps 318/320 are implemented with a germanium alloy, where the blend can be, for example, up to 80 atomic % germanium and up to 20 atomic % for the alloying material, which in some embodiments is tin. Note that the tin concentration (or other alloying material) can also be graded, as will be appreciated. In one such case, channel strain is increased with a tin concentration in the range of 3 to 8 atomic % in the caps 318/320 (with the balance atomic percentage of the caps 318/320 substantially being germanium and any gradient material). In spite of relaxation, lattice constants are still relatively large and capable of applying significant strain on the adjacent channel. Other suitable tin concentrations will be apparent, as will other suitable strain inducers.

Note that with a pure germanium substrate, the liners 313/315 can be implemented with germanium and need not be graded. In some such cases, the germanium concentration of the liners

313/315 can be fixed (e.g., 100 atomic %) and the caps 318/320 can be implemented with a germanium alloy (e.g., germanium:tin, as or other suitable germanium alloy as previously described). As previously explained, the germanium concentration (or the tin or other alloying material concentration) in the caps 318/320 can be graded to effect desired channel strain. In some
5 such cases, further note that the germanium liners 313/315 can effectively be integrated with the germanium alloy caps 318/320 or otherwise be an undetectable component of the source/drain region deposition.

With respect to gradings, note that compatibility as used herein does not necessitate an overlap in concentration levels (for instance, the germanium concentration of underlying substrate 300 can
10 be 0 to 20 atomic % and initial germanium concentration of the liners 313/315 can be 30 to 40 atomic %). In addition, as used herein, the term 'fixed' with respect to a concentration level is intended to indicate a relatively constant concentration level (e.g., the lowest concentration level in the layer is within 10% of the highest concentration level within that layer). In a more general sense, a fixed concentration level is intended to indicate the lack of an intentionally graded
15 concentration level.

The thickness of the liners 313/315 and caps 318/320 can also vary depending on factors such as the composition of the substrate 300, the use of grading for lattice matching/compatibility, and the overall desired thickness of the total source/drain deposition. In general, the liners 313/315 may be thicker in cases where they are configured with a graded germanium content to provide
20 compatibility with a substrate 300 that has no or an otherwise low germanium content. In other cases where the substrate 300 is a germanium substrate or otherwise contains a relatively high concentration of germanium, the liners 313/315 need not be graded, and may therefore be relatively thinner (e.g., one to several monolayers). In yet still other cases where the substrate has no or an otherwise low germanium content, the liners 313/315 can be implemented with a relatively thin
25 layer of silicon or otherwise low germanium content material, and the germanium content of the caps 318/320 can be graded as needed for compatibility. In any such cases, the liners 313/315 generally make up less than 50% of the total source/drain deposition layer thickness, and the remaining source/drain deposition layer thickness is generally greater than 50% of the total source/drain deposition layer thickness. In accordance with some such example embodiments where
30 the liners 313/315 are not graded, the thickness ratio of liners 313/315 to caps 318/320 is about 2:5 or less (i.e., where the liner makes up about 40% or less of the total source/drain deposition layer thickness). In some specific such embodiments, the thickness ratio of liners 313/315 to caps

318/320 is about 1:5 or less (i.e., where the liner makes up about 20% or less of the total source/drain deposition layer thickness). In one such specific example case, the thickness of liners 313/315 is in the range of one-to-several monolayers to about 10 nm, and the total source/drain deposition layer thickness is in the range of 50 to 500 nm. Numerous source/drain liner and cap geometries and material configurations will be apparent in light of this disclosure.

As will be appreciated in light of this disclosure, any number of other transistor features may be implemented with an embodiment of the present invention. For instance, the channel may be strained or unstrained, and the source/drain regions may or may not include tip regions formed in the area between the corresponding source/drain region and the channel region. In this sense, whether a transistor structure has strained or unstrained channels, or source/drain tip regions or no source/drain tip regions, is not particularly relevant to various embodiments of the present invention, and the claimed invention is not intended to be limited to any particular such structural features. Rather, any number of transistor structures and types, and particularly those structures having p-type or both n-type and p-type source/drain transistor regions, can benefit from employing a bi-layer source/drain configuration having a liner and high germanium concentration cap as described herein.

A CVD process or other suitable deposition technique may be used for depositing 208 and 210. For example, depositing 208 and 210 may be carried out in a CVD reactor, an LPCVD reactor, or an ultra high vacuum CVD (UHVCVD). In some example cases, the reactor temperature may fall, for instance, between 600°C and 800°C and the reactor pressure may fall, for instance, between 1 and 760 Torr. The carrier gas may include, for example, hydrogen or helium at a suitable flow rate, such as between 10 and 50 SLM. In some specific embodiments, the deposition may be carried out using a germanium source precursor gas such as GeH₄ that is diluted in H₂ (e.g., the GeH₄ may be diluted at 1-20%). For instance, the diluted GeH₄ may be used at a 1% concentration and at a flow rate that ranges between 50 and 300 SCCM. For an in situ doping of boron, diluted B₂H₆ may be used (e.g., the B₂H₆ may be diluted in H₂ at 1-20%). For instance, the diluted B₂H₆ may be used at a 3% concentration and at a flow rate that ranges between 10 and 100 SCCM. In some example cases, an etching agent may be added to increase the selectivity of the deposition. For instance, HCl or Cl₂ may be added at a flow rate that ranges, for example, between 50 and 300 SCCM.

Numerous variations on the source/drain bi-layer construction will be apparent in light of this disclosure. For instance, in some embodiments, the liners 313/315 are implemented with epitaxially deposited boron doped SiGe, which may be in one or more layers, and have a germanium concentration in the range of 30 to 70 atomic %, or higher. As previously explained, this

germanium concentration of the SiGe liner may be fixed or graded so as to increase from a base level (near substrate 300) to a high level (e.g., in excess of 50 atomic %, near a base concentration of the germanium concentration of caps 318/320, which continue with the germanium gradient to 100 atomic %). The boron concentration in some such embodiments can be in excess of $1\text{E}20\text{ cm}^{-3}$,
5 such as higher than $5\text{E}20\text{ cm}^{-3}$ or $2\text{E}21\text{ cm}^{-3}$, and may also be graded so as to increase from a base level near substrate 300 to a high level (e.g., in excess of $1\text{E}20\text{ cm}^{-3}$ or $2\text{E}20\text{ cm}^{-3}$ or $3\text{E}20\text{ cm}^{-3}$, etc, near caps 318/320). In embodiments where the germanium concentration of boron doped SiGe liners 313/315 is fixed, a thin graded buffer may be used to better interface the liners 313/315 with the boron doped caps 318/320. Note this buffer can be an intermediate layer or otherwise integrated
10 into the composition of the caps 318/320. For purposes of this disclosure, such a buffer can be treated as part of the caps 318/320. The thickness of the boron doped SiGe deposited layer (or collection of layers) 313/315 may range, for example, from monolayers to 50 nm, and the layer (or collection of layers) 318/320 may have a thickness in the range, for example, of 51 to 500 nm, in accordance with some specific embodiments, although alternative embodiments may have other
15 liner and cap thicknesses, as will be apparent in light of this disclosure. In some embodiments, note that cavities 312/314 may be created underneath the spacers during cyclical deposition-etch processing, and those cavities 312/314 can be backfilled by an epitaxial cap layer as well (which can have, for example, the same composition as the boron doped germanium caps 318/320).

As will further be appreciated in light of this disclosure, the combination of high germanium
20 concentration (e.g., in excess of 50 atomic % and up to pure germanium) and high boron concentration (e.g., in excess of $1\text{E}20\text{ cm}^{-3}$), as discussed herein, can be used to realize significantly higher conductance in the source and drain regions (R3 in Figure 1) as well as their respective tip regions (R2 in Figure 1) in PMOS transistor devices. Further, and as previously explained, since boron diffusion is sufficiently suppressed in high germanium composition layers relative to lower
25 germanium composition layers, less adverse SCE degradation is realized with subsequent thermal anneals when comparing to a lower germanium composition layer with equal p-type dopant species and doping levels despite high doping levels in the deposited stressor film. Barrier height lowering is also enabled from the higher concentration of germanium at the contact surface resulting in lower contact resistance R4 in Figure 1. In some example embodiments, a germanium concentration in
30 excess of 80 atomic % and up to pure germanium (100 atomic %) can be used to achieve such benefits. Note that pure germanium is not required, however. For instance, some embodiments may have a germanium concentration in excess of 90 or 95 atomic %, but not be pure.

As further seen with reference to Figure 3C, forming the source/drain tips 318A/320A in relatively close proximity to the channel region also imparts a larger hydrostatic stress on the channel. This stress increases the strain within the channel, thereby increasing mobility in the channel and increasing drive current. This stress can be further amplified by increasing the germanium concentration of the source/drain tips 318A/320A in the case of a silicon-containing substrate, and by increasing the tin concentration in the case of a germanium substrate. This is an improvement over diffusion-based processes where the tip regions generally do not induce a strain on the channel region.

Once the source and drain regions are filled in accordance with an embodiment of the present invention, various conventional MOS processing can be carried out to complete fabrication of MOS transistor, such as replacement gate oxide processes, replacement metal gate processes, annealing, and salicidation processes, that may further modify the transistor and/or provide the necessary electrical interconnections. For instance, after the epitaxial deposition of the source/drain regions along with their respective tips, and with further reference to Figure 2, the method may continue with removing 212 any masking from n-type regions and processing those regions as desired (if applicable, such as in a CMOS process), and depositing 214 an insulator over the transistor, and then planarizing that insulator layer as commonly done. The insulator layer may be formed using materials known for the applicability in insulator layers for integrated circuit structures, such as low-k dielectric (insulator) materials. Such insulator materials include, for example, oxides such as silicon dioxide (SiO₂) and carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. In some example configurations, the insulator layer may include pores or other voids to further reduce its dielectric constant. Figure 3D illustrates an example insulator layer 322 that has been deposited and then planarized down to the hard mask 306.

As can be further seen with reference to Figure 3D', some embodiments of the present invention use a replacement metal gate process, and the method may include removing the gate stack (including the high-k gate dielectric layer 302, the sacrificial gate electrode 304, and the hard mask layer 306) using an etching process as conventionally done. In alternate implementations, only the sacrificial gate 304 is removed. If the gate dielectric 302 is removed, the method may include depositing a new gate dielectric layer into the trench opening. Any suitable high-k dielectric materials such as those previously described may be used here, such as hafnium oxide. The same

deposition processes may also be used. Replacement of the gate dielectric 302 may be used, for example, to address any damage that may have occurred to the original gate dielectric layer during application of the dry and wet etch processes, and/or to replace a low-k or sacrificial dielectric material with a high-k or otherwise desired gate dielectric material. The method may then continue
5 with depositing the metal gate electrode layer into the trench and over the gate dielectric layer. Conventional metal deposition processes may be used to form the metal gate electrode layer, such as CVD, ALD, PVD, electroless plating, or electroplating. The metal gate electrode layer may include, for example, a p-type workfunction metal, such as ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. In some example configurations, two or more
10 metal gate electrode layers may be deposited. For instance, a workfunction metal may be deposited followed by a suitable metal gate electrode fill metal such as aluminum. Figure 3D' illustrates an example high-k gate dielectric layer 324 and a metal gate electrode 326 that have been deposited into the trench opening, in accordance with one embodiment. Note that such a RMG process may be carried out at a different time in the process, if so desired.

15 With further reference to Figure 2, after insulator layer 322 is provided (and any desired pre-contact formation RMG process), the method continues with etching 216 to form the source/drain contact trenches. Any suitable dry and/or wet etch processes can be used. Figure 3E shows the source/drain contact trenches after etching is complete, in accordance with one example embodiment.

20 The method then continues with depositing 218 contact resistance reducing metal and annealing, and then depositing 220 the source/drain contact plugs. Figure 3F shows the contact resistance reducing metals 325, which in some embodiments include silver, nickel, aluminum, titanium, gold, gold-germanium, nickel-platinum or nickel-aluminum, and/or other such resistance reducing metals or alloys. Figure 3F further shows the contact plug metal 329, which in some
25 embodiments includes aluminum or tungsten, although any suitably conductive contact metal or alloy can be used, such as silver, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium, using conventional deposition processes. Metalization of the source/drain contacts can be carried out, for example, using a germanidation process (generally, deposition of contact metal and subsequent annealing). For instance, germanidation with nickel, aluminum,
30 nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. The boron doped germanium caps 318/320 allow for metal-germanide formation (e.g., nickel-

germanium). The germanide allows for significantly lower Schottky-barrier height and improved contact resistance over that in conventional metal-silicide systems. For instance, conventional transistors typically use a source/drain SiGe epi process, with germanium concentration in the range of 30-40 atomic %. Such conventional systems exhibit R_{ext} values of about 140 Ohm-um, limited by epi/silicide interfacial resistance, which is high and may impede future gate pitch scaling. Some embodiments of the present invention allow for a significant improvement in R_{ext} in PMOS devices (e.g., a 2x or better improvement, such as an R_{ext} of about 70 Ohm-um, or less), which can better support PMOS device scaling. Thus, transistors having a source/drain configured with a bi-layer source/drain structure as described herein, can exhibit relatively lower R_{ext} values compared to conventional transistors.

Non-Planar Configuration

A non-planar architecture can be implemented, for instance, using FinFETs or nanowire configurations. A FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin). The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, a source region, and a drain region. The conductive channel of the device resides on/within the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both sidewalls of the fin (sides perpendicular to the substrate surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate FinFET. Other types of FinFET configurations are also available, such as so-called double-gate FinFETs, in which the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin).

Figures 4A to 4G each shows a perspective view of a FinFET transistor structure formed in accordance with one embodiment of the present invention. The previous discussion with respect to Figures 2 through 3F is equally applicable here, as will be appreciated. As can be seen, the example non-planar configuration shown in Figure 4A is implemented with a fin structure which includes a substrate 400 having a semiconductor body or fin 410 extending from the substrate 400 through shallow trench isolation (STI) layer 420. The substrate may be, for example, silicon, germanium, or SiGe.

Figure 4B shows a gate electrode 440 formed over three surfaces of the fin 410 to form three gates (hence, a tri-gate device). A gate dielectric material 430 is provided between the fin 410 and

gate electrode 440, and hard mask 450 is formed on top of the gate electrode 440. Figure 4C illustrates the resulting structure after deposition of insulating material and subsequent etch that leaves a coating of the insulator material on all vertical surfaces, so as to provide spacers 460.

Figure 4D illustrates the resulting structure after an additional etch treatment to eliminate excess insulating/spacer material from sidewalls of fin 410, thereby leaving only spacers 460 opposite sidewalls of the gate electrode 440. Figure 4E illustrates the resulting structure after a recess etch to remove fin 410 in the source/drain region of substrate 400, thereby forming recess 470. Note that other embodiments may not be recessed (e.g., source/drain region is flush with STI layer 420).

Figure 4F illustrates the resulting structure after growth of epitaxial liner 480, which may be thin, p-type and contain significant fraction of silicon (e.g., silicon or SiGe having 70 atomic % silicon), or be pure germanium (e.g., a separate layer of germanium, or a non-detectable layer that is integrated or otherwise included in the composition of the caps 318/320). Figure 4G illustrates the resulting structure after growth of epitaxial source/drain cap 490, which can be p-type, and comprise primarily germanium but may contain less than 20 atomic % tin or other suitable alloying material, as previously explained. As will be appreciated in light of this disclosure, conventional processes and forming techniques can be used to fabricate the FinFET transistor structure having the bi-layer source/drain structure as described herein.

As will further be appreciated, note that an alternative to the tri-gate configuration as shown is a double-gate architecture, which would include a dielectric/isolation layer on top of the fin 410. Further note that the example shapes of the liner 480 and cap 490 making up the source/drain regions shown in Figure 4G are not intended to limit the claimed invention to any particular source/drain types or formation processes, and other source/drain shapes will be apparent in light of this disclosure (e.g., round, square or rectangular source/drain regions may be implemented).

Figure 5A shows a perspective view of a nanowire transistor structure formed in accordance with one embodiment of the present invention. A nanowire transistor (sometimes referred to as gate-all-around FET) is configured similarly to a fin-based transistor, but instead of a fin, a nanowire is used and the gate material generally surrounds the channel region on all sides. Depending on the particular design, some nanowire transistors have, for instance, four effective gates. Figure 5A illustrates a nanowire channel architecture having two nanowires 510, although other embodiments can have any number of wires. The nanowires 510 can be implemented, for example, with p-type silicon or germanium or SiGe nanowire. As can be seen, one nanowire 510 is formed or otherwise

provided in a recess of substrate 400 and the other nanowire 510 effectively floats in the source/drain material bi-layer construction comprising liner 580 and cap 590. Just as with the fin configuration, note that the nanowire 510 can be replaced in the source/drain regions with a bi-layer construction of source/drain material as described herein (e.g., relatively thin silicon or germanium or SiGe liner and relatively thick high concentration germanium cap). Alternatively, the bi-layer construction can be provided around the originally formed nanowire 510 as shown (where liner 580 is provided around nanowire 510, and cap 590 is then provided around liner 580). Figure 5B also illustrates a nanowire configuration having multiple nanowires 510, but in this example case, non-active material 511 is not removed from between the individual nanowires during the nanowire forming process, which can be carried out using various conventional techniques, as will be appreciated in light of this disclosure. Thus, one nanowire 510 is provided in a recess of substrate 400 and the other nanowire 510 effectively sits on top of the material 511. Note the nanowires 510 are active through the channel, but the 511 material is not. As can be seen, the bi-layer source/drain construction of liner 580 and cap 590 is provided around all other exposed surfaces of the nanowires 510.

Example System

Figure 6 illustrates a computing system 1000 implemented with one or more transistor structures configured in accordance with an example embodiment of the present invention. As can be seen, the computing system 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board or a daughterboard mounted on a main board or the only board of system 1000, etc. Depending on its applications, computing system 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing system 1000 may include one or more

transistor structures as described herein (e.g., having a bi-layer source/drain structure comprising a relatively thin p-type silicon or germanium or SiGe liner and a relatively thicker p-type high germanium content cap). These transistor structures can be used, for instance, to implement an on-board processor cache or memory array. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing system 1000. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing system 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing system 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments of the present invention, the integrated circuit die of the processor includes onboard memory circuitry that is implemented with one or more transistor structures (e.g., PMOS or CMOS) as described herein. The term “processor” may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 may also include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more circuits implemented with one or more transistor structures as described herein (e.g., on-chip processor or memory). As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into

the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated
5 therein.

In various implementations, the computing system 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further
10 implementations, the system 1000 may be any other electronic device that processes data or employs low resistance transistor devices as described herein (e.g., PMOS and CMOS circuitry).

Numerous embodiments will be apparent, and features described herein can be combined in any number of configurations. One example embodiment of the present invention provides a transistor device. The device includes a substrate having a channel region, a gate electrode above
15 the channel region, and source and drain regions formed on or in the substrate and adjacent to the channel region. Each of the source and drain regions has a total thickness comprising a p-type liner of silicon or germanium or silicon germanium, and a p-type cap having a germanium concentration in excess of 80 atomic %, wherein the liner is less than 50% of the total thickness. In some cases, the device is one of a planar, FinFET, or nanowire PMOS transistor. In some cases, the device
20 further includes metal-germanide source and drain contacts. In some cases, the thickness ratio of liner thickness to cap thickness is 2:5, or less (liner is 40% or less of the total thickness). In some cases, the thickness ratio of liner thickness to cap thickness is 1:5, or less (liner is 20% or less of the total thickness). In some cases, each of the liners has a thickness in the range of about one monolayer to 10 nm, and each of the caps has a thickness in the range of about 50 nm to 500 nm. In
25 some cases, at least one of the liners and/or caps has at least one of a graded concentration of germanium and/or p-type dopant. For instance, in some cases, at least one of the liners has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %. In one such case, the high concentration is in excess of 90 atomic %. In some cases, at least one of the liners has a p-type dopant
30 concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $1\text{E}20\text{ cm}^{-3}$. In one such case, the p-dopant of the one or more liners is boron. In some cases, at least one of the caps has a germanium concentration in excess of 95 atomic

%. In some cases, at least one of the caps has a germanium concentration that is graded from a base level concentration compatible with the corresponding liner to a high concentration in excess of 80 atomic %. In some cases, at least one of the caps has a p-type dopant concentration that is graded from a base level concentration compatible with the corresponding liner to a high concentration in excess of $1\text{E}20\text{ cm}^{-3}$. In one such case, the p-dopant of the one or more caps is boron. In some cases, at least one of the caps further comprises tin. Numerous variations will be apparent. For instance, in some example cases the substrate is a silicon-containing substrate. In some such cases, the p-type liner comprises silicon or silicon germanium. In other example cases, the substrate is a germanium substrate. In some such cases, the p-type liner is p-type germanium. In some example such cases, each liner is included in the composition of the corresponding cap (such that a distinct and separate liner layer may not be discernible from a distinct and separate cap layer). In some cases, at least one of the caps further comprises misfit dislocations and/or threading dislocations and/or twins, while in other cases, the caps are free of misfit dislocations, threading dislocations, and twins. Another embodiment of the present invention includes an electronic device that includes a printed circuit board having an integrated circuit including one or more transistor devices as variously defined in this paragraph. In one such case, the integrated circuit comprises at least one of a communication chip and/or a processor. In some cases, the electronic device is a computing device.

Another embodiment of the present invention provides an integrated circuit. The circuit includes a substrate (e.g., silicon, SiGe, or germanium) having a channel region, a gate electrode above the channel region, source and drain regions formed on or in the substrate and adjacent to the channel region, and metal-germanide source and drain contacts. Each of the source and drain regions has a total thickness comprising a p-type liner of silicon or germanium or silicon germanium and a p-type cap having a germanium concentration in excess of 80 atomic %, wherein the liner is 40% or less of the total thickness. In some cases, the thickness ratio of liner thickness to cap thickness is 1:5, or less. In some case, at least one of the caps further comprises tin.

Another embodiment of the present invention provides a method for forming a transistor device. The method includes providing a substrate having a channel region, providing a gate electrode above the channel region, and providing source and drain regions formed on or in the substrate and adjacent to the channel region. Each of the source and drain regions has a total thickness comprising a p-type liner of silicon or germanium or silicon germanium and a p-type cap having a germanium concentration in excess of 80 atomic %, wherein the liner is less than 50% of

the total thickness. In some cases, the method includes providing metal-germanide source and drain contacts. In some cases, the thickness ratio of liner thickness to cap thickness is 2:5, or less. In some cases, at least one of the liners and/or caps has at least one of a graded concentration of germanium and/or p-type dopant. In some cases, at least one of the caps further comprises tin (or
5 other suitable strain inducer).

The foregoing description of example embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. For instance, while some embodiments of the present invention utilize in situ boron
10 doping of germanium, other embodiments may use an intrinsic germanium that after its deposition is subsequently subjected to p-type dopant implantation and annealing processes to provide the desired p-type doping concentration. Moreover, some embodiments may include source and drain regions fabricated as described herein, but still use conventional processing (e.g., implantation and annealing) to form the tips of the source and drain regions. In such embodiments, the tips may have
15 a lower germanium and/or p-type dopant concentration than the main source/drain region, which may be acceptable in some applications. In still other embodiments, only tips of the source and drain regions may be configured with the high germanium and p-type dopant concentrations and the main portions of the source and drain regions may have conventional or otherwise lower germanium/dopant concentrations. It is intended that the scope of the invention be limited not by
20 this detailed description, but rather by the claims appended hereto.

CLAIMS

What is claimed is:

1. A transistor device, comprising:
a substrate having a channel region;
5 a gate electrode above the channel region; and
source and drain regions formed on or in the substrate and adjacent to the channel region, each of
the source and drain regions having a total thickness comprising a p-type liner of silicon or
germanium or silicon germanium and a p-type cap having a germanium concentration in
excess of 80 atomic %, wherein the liner is less than 50% of the total thickness.
10
2. The device of claim 1 wherein the device is one of a planar, FinFET, or nanowire PMOS
transistor.
3. The device of claims 1 or 2 further comprising metal-germanide source and drain contacts.
15
4. The device of any of the preceding claims wherein the thickness ratio of liner thickness to cap
thickness is 2:5, or less.
5. The device of any of the preceding claims wherein the thickness ratio of liner thickness to cap
20 thickness is 1:5, or less.
6. The device of any of the preceding claims wherein each of the liners has a thickness in the
range of about one monolayer to 10 nm, and each of the caps has a thickness in the range of
about 50 nm to 500 nm.
25
7. The device of any of the preceding claims wherein at least one of the liners and/or caps has at
least one of a graded concentration of germanium and/or p-type dopant.
8. The device of claim 7 wherein at least one of the liners has a germanium concentration that is
30 graded from a base level concentration compatible with the substrate to a high concentration in
excess of 50 atomic %.

9. The device of claim 8 wherein the high concentration is in excess of 90 atomic %.
10. The device of any of claims 7 through 9 wherein at least one of the liners has a p-type dopant concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of $1 \times 10^{20} \text{ cm}^{-3}$.
11. The device of claim 10 wherein the p-dopant of the one or more liners is boron.
12. The device of any of claims 7 through 11 wherein at least one of the caps has a germanium concentration in excess of 95 atomic %.
13. The device of any of claims 7 through 12 wherein at least one of the caps has a germanium concentration that is graded from a base level concentration compatible with the corresponding liner to a high concentration in excess of 80 atomic %.
14. The device of any of claims 7 through 13 wherein at least one of the caps has a p-type dopant concentration that is graded from a base level concentration compatible with the corresponding liner to a high concentration in excess of $1 \times 10^{20} \text{ cm}^{-3}$.
15. The device of claim 14 wherein the p-dopant of the one or more caps is boron.
16. The device of any of the preceding claims wherein at least one of the caps further comprises tin.
17. The device of any of the preceding claims wherein at least one of the caps further comprises misfit dislocations and/or threading dislocations and/or twins.
18. The device of any of the preceding claims wherein the caps are free of misfit dislocations, threading dislocations, and twins.
19. An electronic device comprising:
a printed circuit board having an integrated circuit including one or more transistor devices as

defined in any of the preceding claims.

20. The electronic device of claim 19 wherein the integrated circuit comprises at least one of a communication chip and/or a processor.
- 5
21. The electronic device of claims 19 or 20 wherein the electronic device is a computing device.
22. An integrated circuit, comprising:
a substrate having a channel region;
10 a gate electrode above the channel region;
source and drain regions formed on or in the substrate and adjacent to the channel region, each of the source and drain regions having a total thickness comprising a p-type liner of silicon or germanium or silicon germanium and a p-type cap having a germanium concentration in excess of 80 atomic %, wherein the liner is less than 40% of the total thickness; and
15 metal-germanide source and drain contacts.
23. The circuit of claim 20 wherein the thickness ratio of liner thickness to cap thickness is 1:5, or less.
- 20 24. The circuit of claims 20 or 21 wherein at least one of the caps further comprises tin.
25. A method for forming a transistor device, comprising:
providing a substrate having a channel region;
providing a gate electrode above the channel region; and
25 providing source and drain regions formed on or in the substrate and adjacent to the channel region, each of the source and drain regions having a total thickness comprising a p-type liner of silicon or germanium or silicon germanium and a p-type cap having a germanium concentration in excess of 80 atomic %, wherein the liner is less than 50% of the total thickness.
30
26. The method of claim 25 further comprising providing metal-germanide source and drain contacts.

27. The method of claims 25 or 26 wherein the thickness ratio of liner thickness to cap thickness is 2:5, or less.
- 5 28. The method of any of claims 25 through 27 wherein at least one of the liners and/or caps has at least one of a graded concentration of germanium and/or p-type dopant.
29. The method of any of claims 25 through 28 wherein at least one of the caps further comprises tin.
- 10 30. A transistor device, comprising:
a silicon-containing substrate having a channel region;
a gate electrode above the channel region; and
source and drain regions formed on or in the substrate and adjacent to the channel region, each of
15 the source and drain regions having a total thickness comprising a p-type liner of silicon or silicon germanium and a p-type cap having a germanium concentration in excess of 80 atomic %, wherein the liner is less than 50% of the total thickness.
31. A transistor device, comprising:
20 a germanium substrate having a channel region;
a gate electrode above the channel region; and
source and drain regions formed on or in the substrate and adjacent to the channel region, each of
the source and drain regions having a total thickness comprising a p-type liner of germanium
and a p-type cap having a germanium concentration in excess of 80 atomic %, wherein the
25 liner is less than 50% of the total thickness.
32. The device of claim 31 wherein each liner is included in the composition of the corresponding cap.

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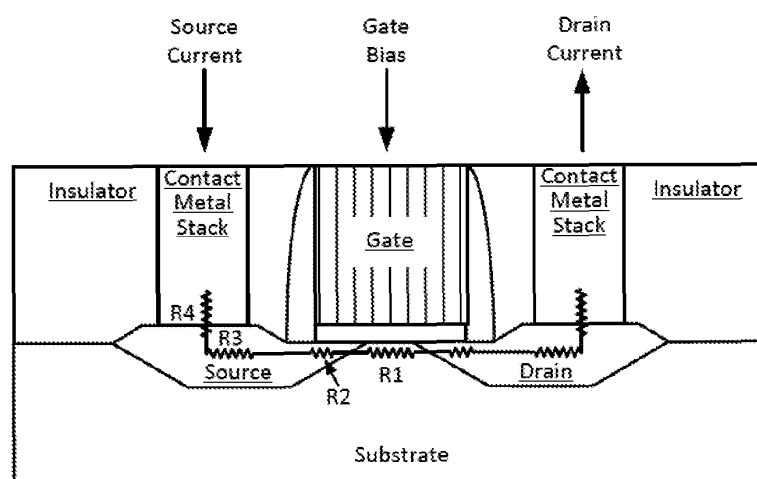


FIG. 1

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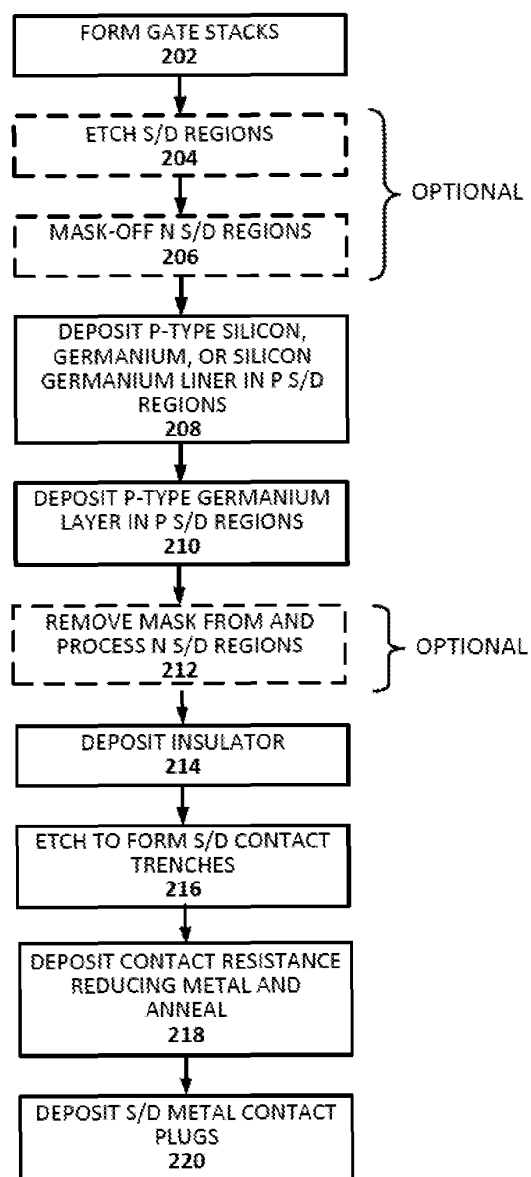


FIG. 2

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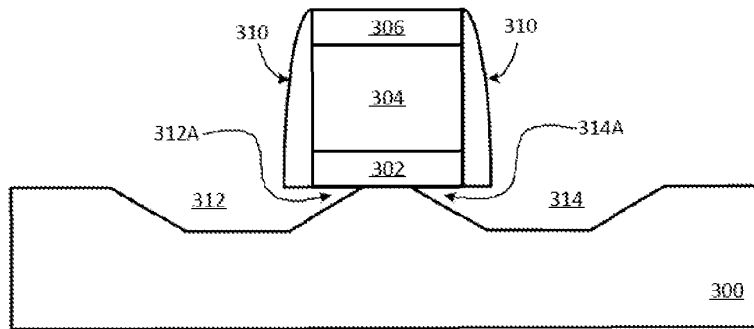


FIG. 3A

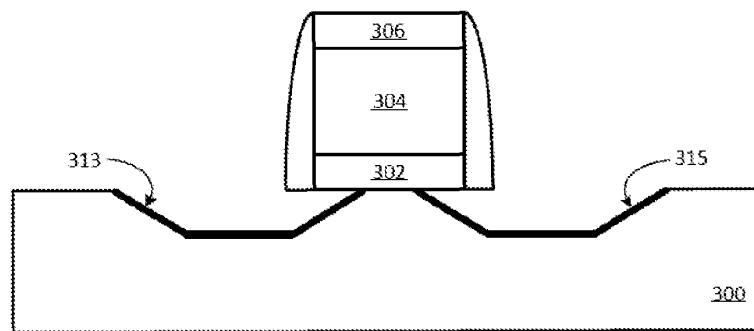


FIG. 3B

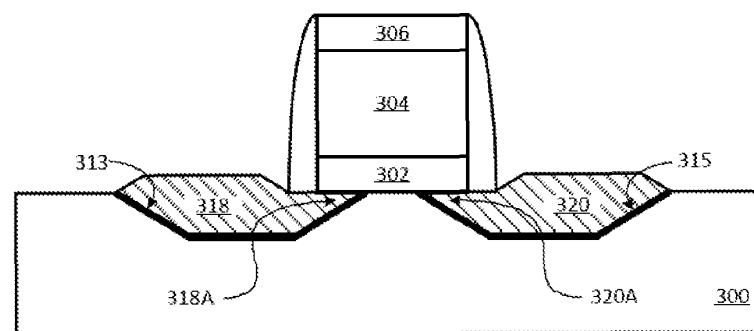


FIG. 3C

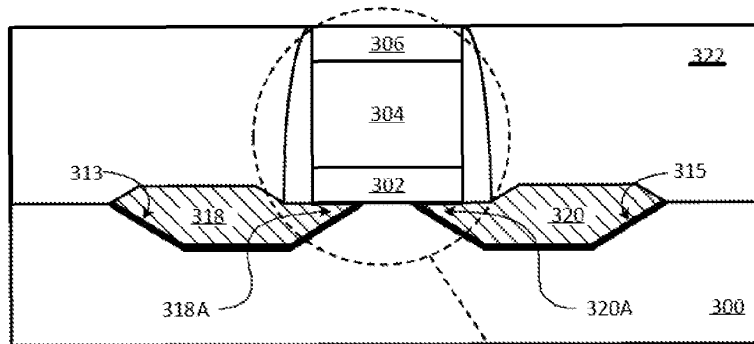


FIG. 3D

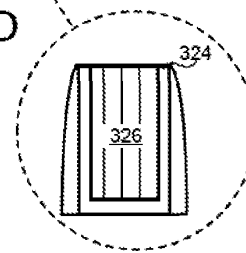


FIG. 3D'

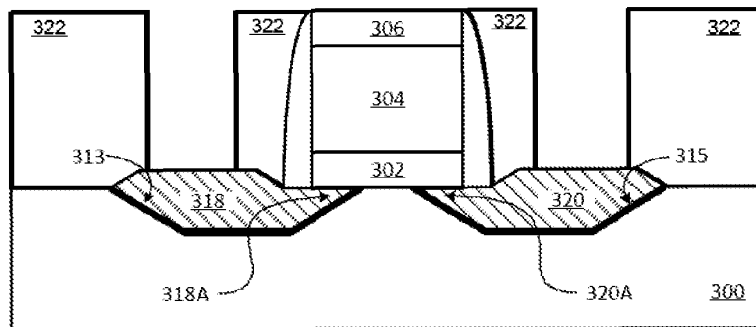


FIG. 3E

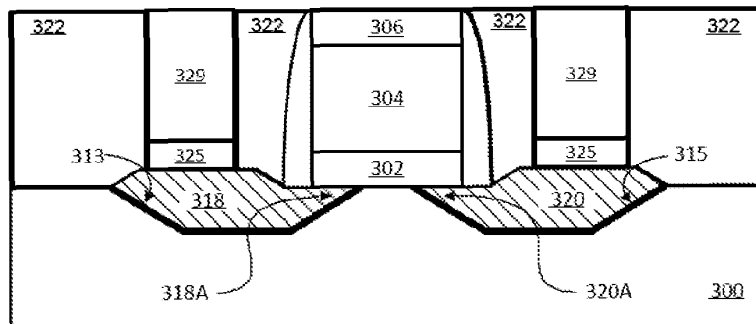


FIG. 3F

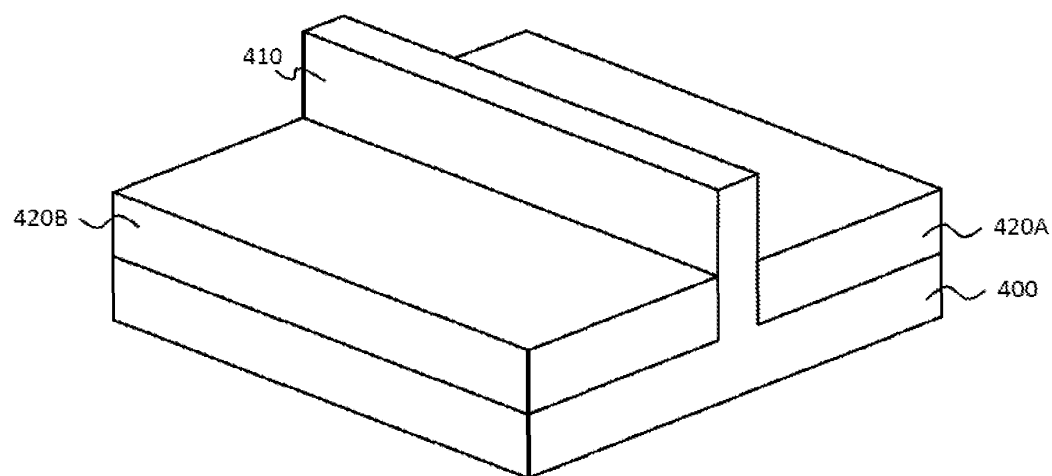


FIG. 4A

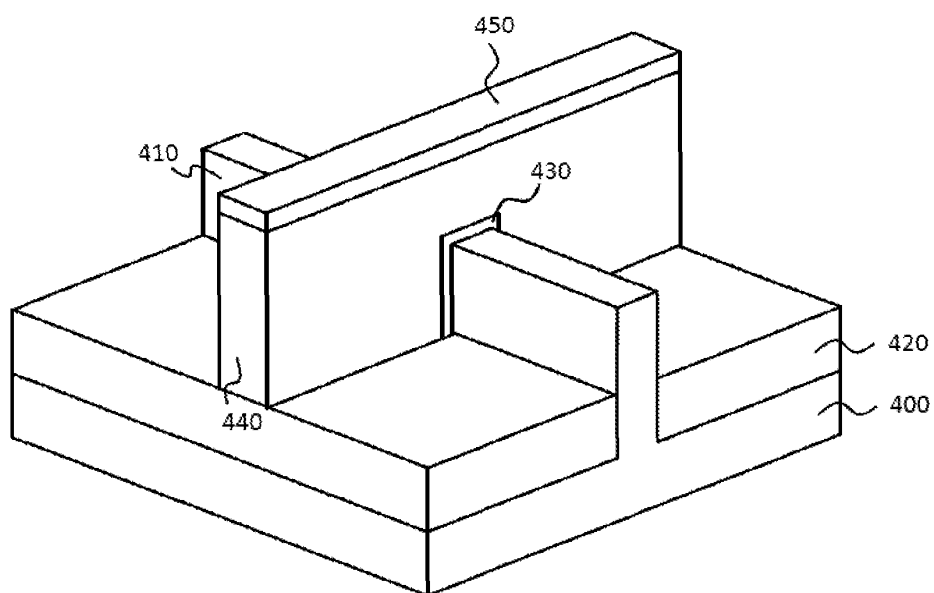


FIG. 4B

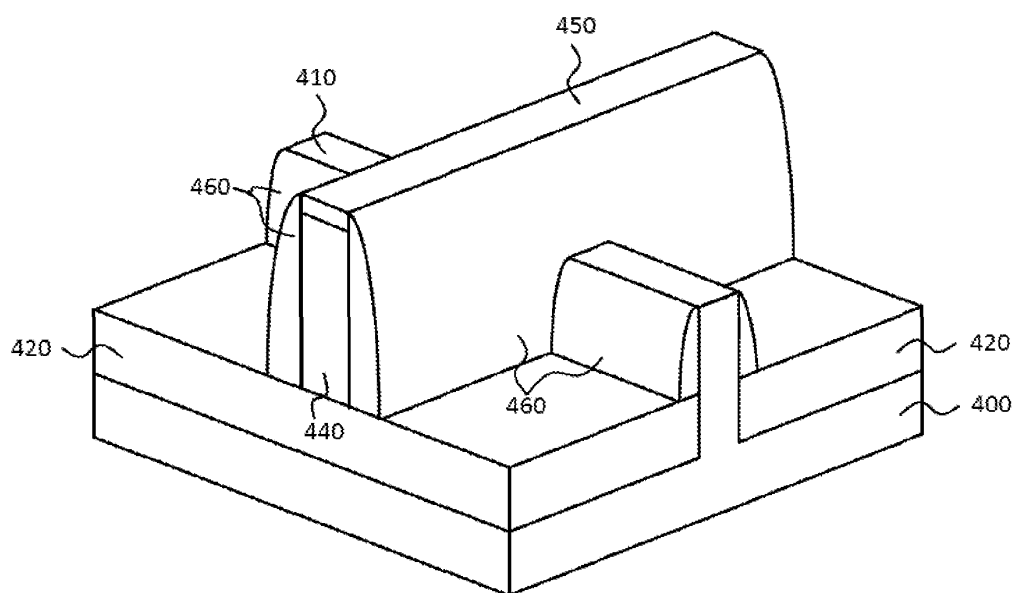


FIG. 4C

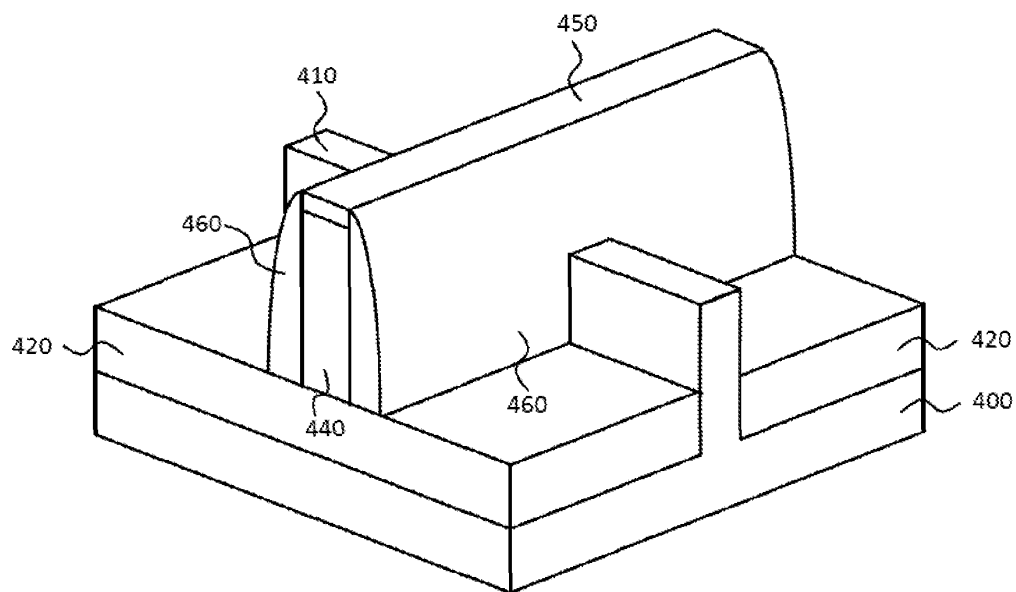


FIG. 4D

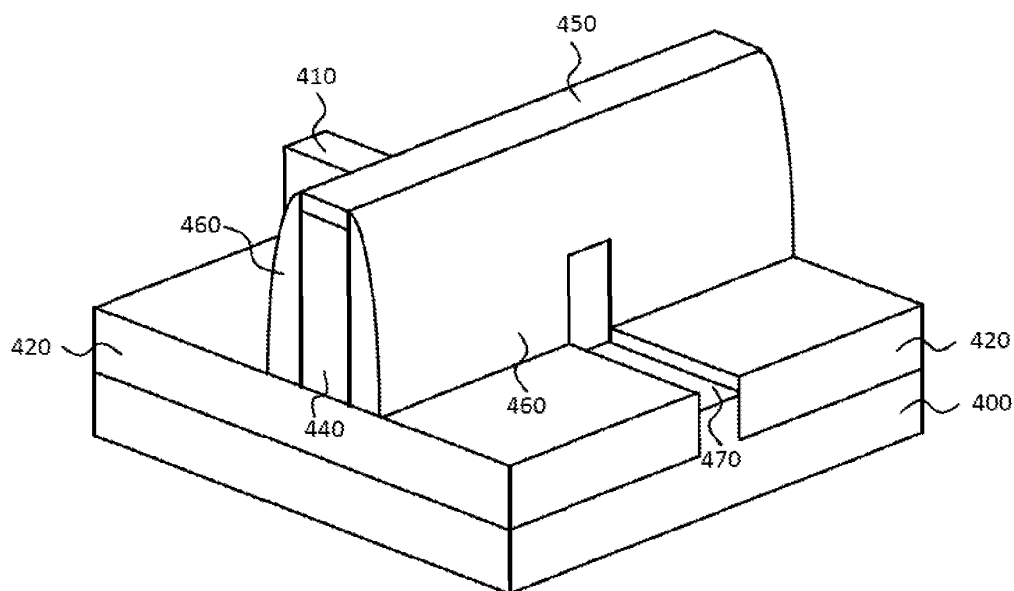


FIG. 4E

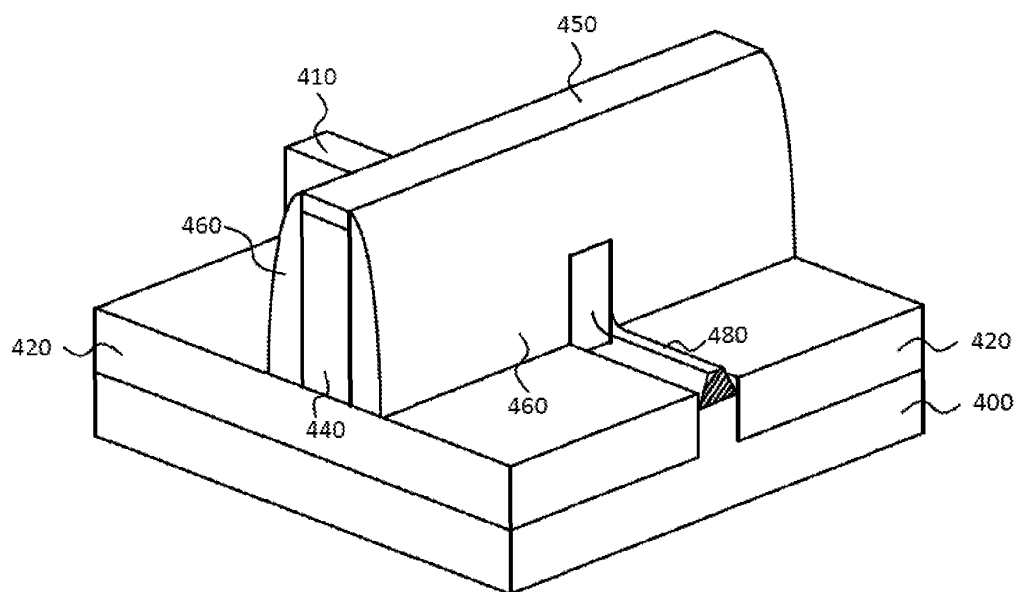


FIG. 4F

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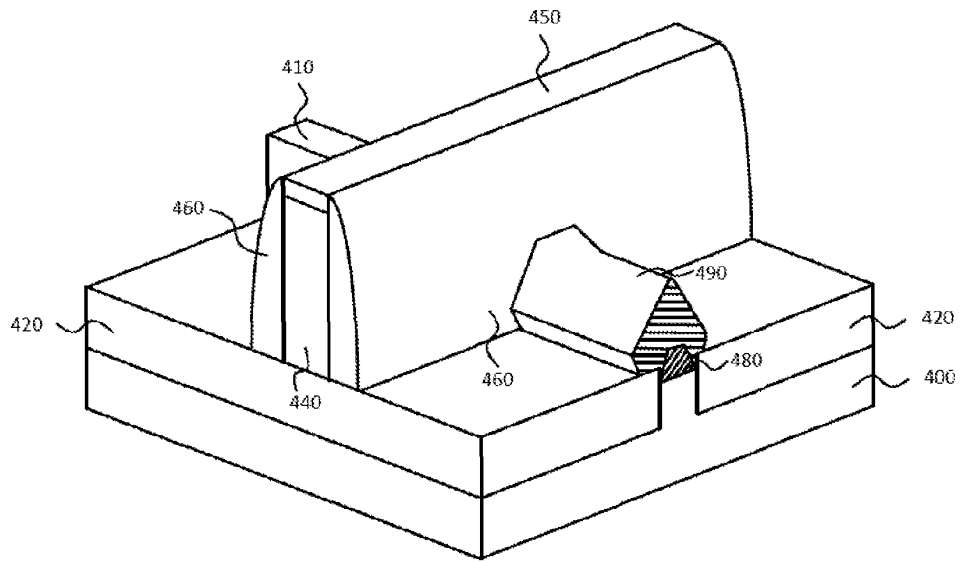


FIG. 4G

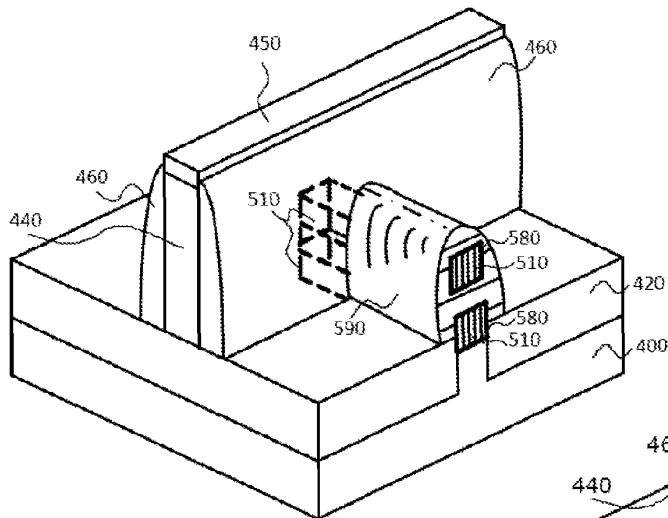


FIG. 5A

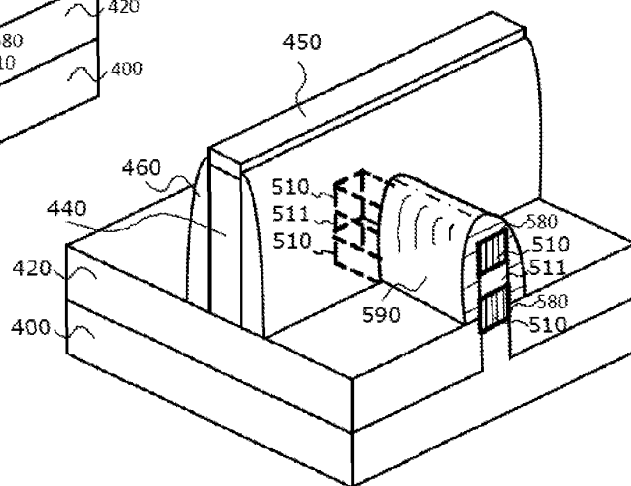
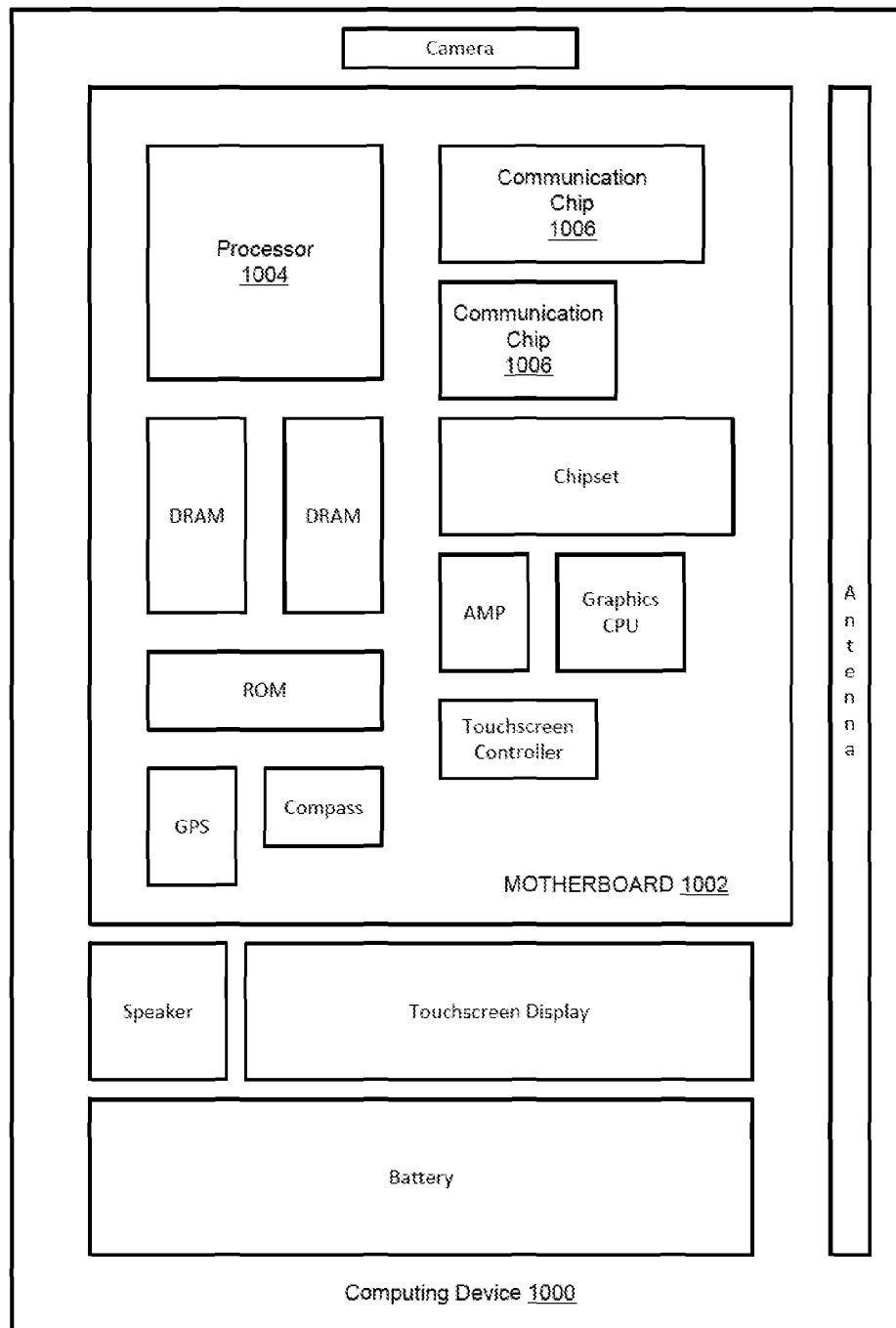


FIG. 5B

**Fig. 6**

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16881541
	Filing Date	2020-05-22
	First Named Inventor	Glenn A. Glass
	Art Unit	2826
	Examiner Name	Fazli Erdem
	Attorney Docket Number	D480-012044

U.S. PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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	2	5216271	A	1993-06-01	TAKAGI, et al.	
	3	5281552	A	1994-01-25	KING, et al.	
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	8	6605498	B1	2003-08-12	MURTHY, et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		16881541
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	Art Unit	2826	
	Examiner Name	Fazli Erdem	
	Attorney Docket Number	D480-012044	

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	First Named Inventor	Glenn A. Glass	
	Art Unit	2826	
	Examiner Name	Fazli Erdem	
	Attorney Docket Number	D480-012044	

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	Art Unit		2826	
	Examiner Name		Fazli Erdem	
	Attorney Docket Number		D480-012044	

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	1	20020168868	A1	2002-11-14	TODD	
	2	20020197806	A1	2002-12-26	FURUKAWA, et al.	
	3	20030124761	A1	2003-07-03	BAERT, et al.	
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	1	S6313379	JP	A	1988-01-20	NIPPON TELEGR & TELEPH CORP <NTT>		×

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	Art Unit		2826	
	Examiner Name		Fazli Erdem	
	Attorney Docket Number		D480-012044	

	2	H10261792	JP	A	1998-09-29	HITACHI LTD		☒
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	Art Unit	2826		
	Examiner Name	Fazli Erdem		
	Attorney Docket Number	D480-012044		

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	Attorney Docket Number	D480-012044		

	24	101677110	CN	A	2010-03-24	INTEL CORP.		☒
	25	2010510720	JP	A	2010-04-02			☒
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	Art Unit	2826		
	Examiner Name	Fazli Erdem		
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	35	690084	TW	B	2020-04-01	INTEL CORPORATION	☒
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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Communication Pursuant to Article 94(3) EPC for EP Application No. 17193291.6, Dated February 26, 2020, Pages 3	
	2	Communication Pursuant to Article 94(3) EPC for EP Application No. 17193291.6, Dated June 16, 2021, Pages 5	
	3	Extended European Search Report for EP Application No. 17193291.6, Dated March 23, 2018, Pages 9	
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	First Named Inventor	Glenn A. Glass	
	Art Unit	2826	
	Examiner Name	Fazli Erdem	
	Attorney Docket Number	D480-012044	

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

✓ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ian D. MacKinnon/	Date (YYYY-MM-DD)	2021-10-08
Name/Print	Ian D. MacKinnon	Registration Number	34,660

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Application Number:		16881541		
Filing Date:		22-May-2020		
Title of Invention:		CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION		
First Named Inventor/Applicant Name:		Glenn A. GLASS		
Filer:		Ian David MacKinnon/Nicole Chambers		
Attorney Docket Number:		D480-012044		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1360	1360
Total in USD (\$)				1360

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EFS ID:	43986207
Application Number:	16881541
International Application Number:	
Confirmation Number:	8383
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Customer Number:	164
Filer:	Ian David MacKinnon
Filer Authorized By:	
Attorney Docket Number:	D480-012044
Receipt Date:	08-OCT-2021
Filing Date:	22-MAY-2020
Time Stamp:	15:39:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$1360
RAM confirmation Number	E202108F41294797
Deposit Account	110982
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2	Foreign Reference	ForRef_CN101087002A_WithAbstract.pdf	2924939	no	34
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	Filing Date	2020-05-22
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	2	20080075009	KR	A	2008-08-13	INTEL CORP.		☒

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	1	Communication Pursuant to Article 94(3) EPC for EP Application No. 19188924.5, Dated October 14, 2021, Pages 9	
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	Art Unit	2826
	Examiner Name	Fazli Erdem
	Attorney Docket Number	D480-012044

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Bibliographic data: CN1518771 (A) — 2004-08-04

Tri-gate devices and method of fabrication

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Applicant(s): INTEL CORP [US] ± (英特尔公司, ; INTEL CORP)

Classification: - **international:** H01L21/336; H01L29/423; H01L29/786; (IPC1-7): H01L21/336; H01L29/423; H01L29/786
 - **cooperative:** B82Y10/00 (EP); H01L29/0665 (EP, KR); H01L29/0673 (EP); H01L29/1033 (EP, KR); H01L29/41791 (EP, KR); H01L29/42384 (EP, KR); H01L29/42392 (EP, KR); H01L29/4908 (EP, KR); H01L29/66795 (EP, KR); H01L29/772 (EP, KR); H01L29/785 (EP, KR); H01L29/7854 (KR); H01L29/78696 (EP); H01L51/0048 (EP); H01L51/0554 (EP); H01L29/7854 (EP); H01L29/78645 (EP); Y10S977/742 (EP); Y10S977/842 (EP); Y10S977/938 (EP)

Application number: CN20038000511 20030822

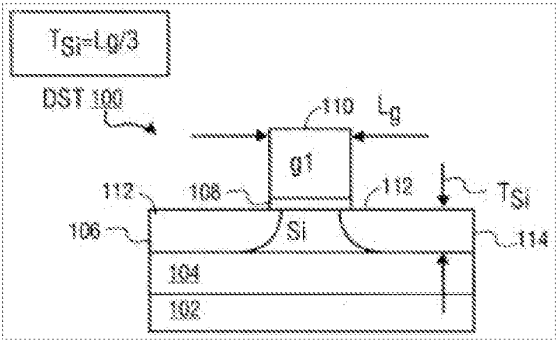
Priority number(s): US20020227068 20020823

Also published as: AU2003262770 (A1) CN1287433 (C) CN1822338 (A) CN1897232 (A) EP1425801 (A1) more

Abstract not available for CN1518771 (A)

Abstract of corresponding document: US2004036126 (A1)

The present invention is a semiconductor device comprising a semiconductor body having a top surface and laterally opposite sidewalls formed on a substrate. A gate dielectric layer is formed on the top surface of the semiconductor body and on the laterally opposite sidewalls of the semiconductor body. A gate electrode is formed on the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the laterally opposite sidewalls of the semiconductor body.





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DESCRIPTION CN1518771A

Tri-gate device and its processing method

[0001]

Technical field

[0002]

The present invention relates to the field of semiconductor integrated circuit manufacturing. More specifically, the present invention relates to a tri-gate fully depleted substrate transistor and a processing method thereof.

[0003]

Background technique

[0004]

In order to improve device performance, silicon on insulator (SOI) transistors have been suggested for processing modern integrated circuits.

FIG. 1 shows a standard fully depleted silicon-on-insulator (SOI) transistor 100.

The SOI transistor 100 includes a single crystal silicon substrate 102 having an insulating layer 104, such as a buried oxide layer formed thereon.

A single crystal silicon body 106 is formed on the insulating layer 104. A gate dielectric layer 108 is formed on the single crystal silicon body 106, and a gate electrode 110 is formed on the gate dielectric layer 108. The source 112 and drain 114 regions are formed in the silicon body 106 along the laterally opposite sides of the gate electrode 110.

[0005]

It has been proposed to use a fully depleted SOI as a transistor structure to take advantage of the ideal subthreshold gradient of the optimized on-current/off-current ratio.

In order to obtain the ideal sub-threshold gradient of the transistor 100, the thickness of the silicon body 106 must be approximately 1/3 of the size of the transistor gate length (L_g), that is, $T_{Si} = L_g/3$. However, as gate lengths change, especially when they approach 30 nm, the need to minimize the silicon film thickness (T_{Si}) makes this approach increasingly impractical. For a gate length of 30 nanometers, it is believed that the required thickness of the silicon body needs to be less than 10 nanometers, and for a gate length of 20 nanometers, the thickness needs to be about 6 nanometers. The processing of thin silicon films with a thickness of less than 10 nanometers is extremely difficult. On the one hand, achieving wafer uniformity on

the order of a nanometer is an arduous challenge. On the other hand, being able to contact these thin silicon films to form raised source/drain regions to reduce junction resistance becomes almost impossible, because the gate etching and the gate etching and isolation layer etching after each. During this cleaning process, the thin silicon layer in the source/drain regions is consumed, leaving insufficient silicon for silicon growth.

[0006]

Dual-gate (DG) devices such as those shown in FIGS. 2A and 2B have been proposed to alleviate the problem with silicon thickness.

The dual gate (DG) device 200 includes a silicon body 202 formed on an insulating substrate 204. A gate dielectric 206 is formed on both sides of the silicon body 202, and a gate electrode 208 is formed adjacent to the gate dielectric 206 formed on both sides of the silicon body 202. A sufficiently thick insulating layer 209 such as silicon nitride electrically insulates the gate electrode 208 from the top of the silicon body 202.

[0007]

The dual gate (DG) device 200 basically has two gates, which are located on both sides of the device channel.

Because the dual gate device 200 has gates on both sides of the channel, the thickness (T_{si}) of the silicon body can be twice that of a single gate, and the operation of a fully depleted transistor can still be obtained. That is to say, by using the double gate device 200, a fully depleted transistor can be formed, where $T_{si} = (2 \times L_g) / 3$. However, the most manufacturable form of the dual-gate (DG) device 200 requires the use of a certain lithography technique to complete the patterning of the silicon body 202, which is less expensive than the gate length (L_g) used to pattern the device. The photolithography technology is 0.7 times smaller. In order to obtain a high-density integrated circuit, it is generally desired to apply the most aggressive photolithography method to the gate length (L_g) of the gate electrode 208. Although the double-gate structure doubles the thickness of the silicon film (because there are now gates on both sides of the channel), these structures are extremely difficult to process. For example, the silicon body 202 requires a silicon body etching that can produce a silicon body 202 with an aspect ratio (height-to-width ratio) of about 5:1.

[0008]

Description of the drawings

[0009]

FIG. 1 is an example of a cross-sectional view of a depletion type substrate transistor.

[0010]

Figures 2A and 2B illustrate dual-gate depletion-type substrate transistors.

[0011]

Fig. 3 is an example of a tri-gate transistor according to an embodiment of the present invention.

[0012]

FIG. 4A is an example of a tri-gate transistor according to an embodiment of the present invention.

[0013]

FIG. 4B is an example of a tri-gate transistor according to an embodiment of the present invention.

[0014]

5A-5J illustrate a method of processing a tri-gate transistor according to an embodiment of the present invention.

[0015]

FIG. 6 is a graph illustrating the body height and body width that can be used to obtain partially depleted and fully depleted transistors with gate lengths (L_g) of 30 nm and 20 nm.

[0016]

Detailed ways

[0017]

The invention is a novel tri-gate transistor structure and its processing method.

In the following description, a lot of specific details are given to provide a thorough understanding of the present invention.

In other cases, the well-known semiconductor process and manufacturing technology are not described in specific details so as not to unnecessarily obscure the present invention.

[0018]

The invention is a novel tri-gate transistor structure and its processing method.

In an embodiment of the present invention, the tri-gate transistor is a silicon-on-insulator (SOI) transistor.

It is ideal to use tri-gate transistors in fully depleted transistor applications.

The tri-gate transistor includes a thin semiconductor body formed on a substrate, which may be an insulating substrate or a semiconductor substrate.

A gate dielectric is formed on the top surface and sidewalls of the semiconductor body.

A gate electrode is formed on the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric formed on the sidewall of the semiconductor body.

Source and drain regions are formed on opposite sides of the gate electrode in the semiconductor body.

Because the gate electrode and the gate dielectric surround the three sides of the semiconductor body, the transistor essentially has three separate channels and gates.

The gate "width" of the transistor is equal to the sum of each of the three sides of the semiconductor body.

A larger "width" transistor can be formed by connecting several tri-gate transistors together.

[0019]

Because three separate channels are formed in the semiconductor body, the semiconductor body can be completely depleted when the transistor is "turned on", so that a gate length of less than 30 nanometers can be used to form a fully depleted transistor. There is no need to use an ultra-thin semiconductor body or the size of the photolithographic pattern of the semiconductor body is smaller than the gate length (L_g) of the device.

In other words, when the thickness of the semiconductor body and the width of the semiconductor body are equal to the gate length of the device, the structure of the tri-gate transistor of the present invention makes it possible to process a fully depleted transistor. Because the novel tri-gate transistor of the present invention can be operated in a fully depleted manner, the device has the following characteristics: ideal (ie very steep) sub-threshold slope; reduced Drain Field Induced Barrier Reduction (DIBL) short channel The channel effect, which is less than 100mV/V, and the ideal value is about 60mV/V, obtains a smaller leakage current when the device is "off", and thus lower power consumption.

[0020]

An example of a tri-gate transistor 300 according to an embodiment of the present invention is illustrated in FIG. 3.

The tri-gate transistor 300 is formed on the substrate 302. In the embodiment of the present invention, the substrate 302 is an insulating substrate, which includes a lower single crystal silicon substrate 304, and an insulating layer 306, such as a silicon dioxide film, is formed on the single crystal silicon substrate. However, the tri-gate transistor 300 may be formed on any well-known insulating substrate, such as a substrate formed of silicon dioxide, nitride, oxide, and sapphires. In the embodiment of the present invention, the substrate 302 may be a semiconductor substrate, such as but not limited to a single crystal silicon substrate and a gallium arsenide substrate.

[0021]

The tri-gate transistor 300 includes a semiconductor body 308 formed on an insulator 306 of an insulating substrate 302.

The semiconductor body 308 may be formed of any well-known semiconductor material, such as but not limited to silicon (Si), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), InSb, GaP, GaSb, and carbon nanotubes. The semiconductor body 308 may be formed of any such known material that can be reversibly changed from an insulating state to a conductive state by applying external electrical control. When the best electrical performance of the transistor 300 is desired, the semiconductor body 308 is desirably a single crystal film. For example, when the transistor 300 is used in a high-performance application such as a high-density circuit like a microprocessor, the semiconductor body 308 is a single crystal film. However, when the transistor 300 is used in an application requiring lower performance such as a liquid crystal display, the semiconductor body 308 may be a polycrystalline film. The insulator 306 insulates the semiconductor body 308 from the single crystal silicon substrate 302. In the embodiment of the present invention, the semiconductor body 308 is a single crystal silicon film. The semiconductor body 308 has a pair of laterally opposed sidewalls 310 and 312 separated by a distance defining a width 314 of the semiconductor body. In addition, the semiconductor body 308 has a top surface 316 opposite to the bottom surface 318 formed on the substrate 302. The distance between the top surface 316 and the bottom surface 318 defines the body height 320. In the embodiment of the present invention, the main body height 320 and the main body width 314 are substantially equal. In an embodiment of the present invention, the main body 308 has a width 314 and a height 320 less than 30 nanometers, and ideally less than 20 nanometers. In the embodiment of the present invention, the main body height 320 is between 1/2 of the main body width 314 and 2 times the main body width 314.

[0022]

The tri-gate transistor 300 has a gate dielectric layer 322.

The gate dielectric layer 322 is formed on three sides of the semiconductor body 308 and surrounds the three sides, as shown in FIG. 3. The gate dielectric layer 322 is formed on or adjacent to the sidewall 312 of the body 308, on the top surface 316, and on or adjacent to the sidewall 310, as shown in FIG. 3. The gate dielectric layer 322 may be any well-known gate dielectric layer. In an embodiment of the present invention, the gate dielectric layer is a silicon dioxide (SiO₂), silicon oxynitride (SiO_xN_y) or silicon nitride (Si₃N₄) dielectric layer. In the embodiment of the present invention, the gate dielectric layer 322 is a silicon oxynitride film formed with a thickness between 5-20 angstroms. In an embodiment of the present invention, the gate dielectric layer 322 is a high-K gate dielectric layer, such as a metal oxide dielectric, such as but not limited to tantalum pentoxide (Ta₂O₅) and titanium dioxide (TiO₂). The gate dielectric layer 322 may be other types of high-K dielectrics, such as but not limited to PZT.

[0023]

The tri-gate device 300 has a gate electrode 324.

The gate electrode 324 is formed on the gate dielectric layer 322 and surrounds the gate dielectric layer 322, as shown in FIG. 3. The gate electrode 324 is formed on or adjacent to the gate dielectric 322 formed on the sidewall 312 of the semiconductor body 308, on the gate dielectric 322 formed on the top surface 316 of the semiconductor body 308, and formed on the semiconductor body 308. On or adjacent to the gate dielectric layer 322 on the sidewall 310 of the main body 308. The gate electrode 324 has a pair of laterally opposed sidewalls 326 and 328 separated by a distance that defines the gate length (L_g) 330 of the transistor 300. In the embodiment of the present invention, the laterally opposite sidewalls 326 and 328 of the gate electrode 324 are perpendicular to the laterally opposite sidewalls 310 and 312 of the semiconductor body 308.

[0024]

The gate electrode 324 may be formed of any suitable gate electrode material.

In the embodiment of the present invention, the gate electrode 324 is made of polysilicon doped to a concentration of 1×10^{19} atoms/cm³– 1×10^{20} atoms/cm³. In the embodiment of the present invention, the gate electrode may be a metal gate electrode, such as but not limited to tungsten, tantalum, titanium and their nitrides. In the embodiment of the present invention, the gate electrode is formed of a material having a mid-gap work function between 4.6 and 4.8 eV. It should be realized that the gate electrode 324 does not necessarily need to be a single material, but may be a composite laminate of multiple thin films, such as but not limited to a polysilicon/metal electrode or a metal/polysilicon electrode.

[0025]

The tri-gate transistor 300 has a source region 330 and a drain region 332.

The source region 330 and the drain region 332 are formed on opposite sides of the gate electrode 324 in the semiconductor body 308, as shown in FIG. 3. The source region 330 and the drain region 332 are formed of the same conductivity type, for example, N-type or P-type conductivity. In the embodiment of the present invention, the source region 330 and the drain region 332 have a doping concentration between 1×10^{19} and 1×10^{20} atoms/cm³. The source region 330 and the drain region 332 may be formed to have a uniform concentration, or may include sub-regions with different concentrations or doping characteristics, such as tip regions (such as source/drain extensions). In the embodiment of the present invention, when the transistor 300 is a symmetrical transistor, the source region 330 and the drain region 332 will have the same doping concentration and characteristics. In the embodiment of the present invention, when the tri-gate transistor 300 is formed as an asymmetric transistor, the doping concentration and characteristics of the source region 330 and the drain region 332 may be different to obtain specific electrical characteristics.

[0026]

The portion of the semiconductor body 308 between the source region 330 and the drain region 332 defines the channel region 350 of the transistor 300.

The channel region 350 can also be defined as the region of the semiconductor body 308 surrounded by the gate electrode 324. However, the source/drain regions can sometimes be extended slightly below the gate electrode by, for example, diffusion to define a channel region slightly smaller than the length (L_g) of the gate electrode. In one embodiment of the present invention, the channel region 350 is intrinsic or undoped single crystal silicon. In one embodiment of the present invention, the channel region 350 is doped single crystal silicon. When the channel region 350 is doped, it is generally doped to a conductivity level between 1×10^{16} and 1×10^{19} atoms/cm³. In the embodiment of the present invention, when the channel region is doped, it is generally doped to a conductivity type opposite to that of the source region 330 and the drain region 332. For example, when the source and drain regions are of N-type conductivity, the channel region is doped with P-type conductivity. Similarly, when the source and drain regions are of P-type conductivity, the channel region is of N-type conductivity. In this way, the tri-gate transistor 300 may be formed as an NMOS transistor or a PMOS transistor, respectively. The channel region 350 may be doped uniformly, or may be doped non-uniformly or at different concentrations to provide specific electrical and performance characteristics. For example, if desired, the channel region 350 may include the well-known "halo" region.

[0027]

By providing the gate dielectric and gate electrode surrounding the semiconductor body on three sides, the tri-gate transistor has the characteristics of including three channels and three gates, one of which (g_1) extends on the silicon body 308 between the source and drain regions on the side surface 312, the second (g_2) extends between the source and drain regions on the top surface 316 of the silicon body 308, and the third (g_3) extends across the silicon body between the source and drain regions on the sidewall 310 of 308.

The gate "width" (G_w) of the transistor 300 is the sum of the widths of these three channel regions. That is, the gate width of the transistor 300 is equal to the height of the silicon body 308 at the sidewall 310, plus the width of the silicon body 308 at the top surface 316, plus the height of the silicon body 308 at the sidewall 312. By using multiple devices coupled together (e.g., multiple silicon bodies 308 surrounded by a single gate electrode 324), a larger "width" transistor can be obtained.

[0028]

Because the channel region 350 is surrounded by the gate electrode 324 and the gate dielectric 322 on three sides, the transistor 300 can be operated in a fully depleted manner, wherein when the transistor 300 is "on", the channel region 350 is fully depleted, thereby providing the favorable electrical characteristics and performance of a fully depleted transistor.

That is, when the transistor 300 is "turned on", a depletion region is formed at the channel region 350, and an inversion layer is formed at the surface of the region 350 (that is, an inversion layer is formed on the side surface and the top surface of the semiconductor body). Transfer layer). The inversion layer has the same conductivity type as the source and drain regions, and a conductive channel is formed between the source and drain regions so that current can flow between the two. The tri-gate transistor of the present invention can be said to be a non-planar transistor, because a channel region is formed in both the horizontal and vertical directions of the semiconductor body 308. The depletion zone will deplete the free carrier from below the inversion layer. The depletion region extends to the bottom of the channel region 350, so the transistor can be said to be a "fully depleted" transistor. Compared with non-fully depleted or partially depleted transistors, fully depleted transistors have improved electrical performance characteristics. For example, by operating the transistor 300 in a fully depleted manner, the transistor 300 can be made to have an ideal or very steep sub-threshold slope. Tri-gate transistors can be processed to have a very steep sub-threshold slope of less than 80mV/decade, ideally about 60mV/decade, even if the transistor is processed with a semiconductor body with a thickness of less than 30nm. In addition, when the transistor 300 is operated in a fully depleted mode, the transistor 300 has an improved leakage field induced barrier reduction (DIBL) effect, which provides better "off" state leakage current, resulting in a smaller leakage current, thereby reducing power consumption. In the embodiment of the present invention, the tri-gate transistor 300 has a DIBL effect of less than 100 mV/V, and ideally, less than 40 mV/V.

[0029]

Figure 6 shows two graphs showing the body height of fully depleted (FD) or partially depleted (PD) tri-gate transistors with gate lengths of 30nm (602) and 20nm (604). And the body width.

In the embodiment of the present invention, the body height, body width, and gate length are selected to have such dimensions that a fully depleted transistor can be formed in these dimensions. In other embodiments, the tri-gate transistor has a body height, body width, and gate length such that a partially depleted transistor can be formed.

[0030]

In an embodiment of the present invention, the source and drain regions of the tri-gate transistor 300 may include silicon or other semiconductor films formed on and around the semiconductor body 308, as shown in FIG. 4A.

For example, the semiconductor film 410 may be a silicon film or a silicon alloy such as silicon germanium (SixGe_y). In the embodiment of the present invention, the semiconductor film 410 is a single crystal silicon film formed with the same conductivity type as the source region 330 and the drain region 332. In an embodiment of the present invention, the semiconductor film may be a silicon alloy such as silicon germanium, where silicon constitutes about 1 to 99 atomic percent of the alloy. The semiconductor film 410 does not necessarily need to be a single crystal semiconductor film, and in one embodiment, may be a polycrystalline film. In an embodiment of the present invention, the semiconductor film 410 is formed on the source region 330 and the drain region 332 of the semiconductor body 308 to form "bumped" source and drain regions. The semiconductor film 410 may be electrically insulated from the gate electrode 324 by a pair of dielectric sidewall spacers 420 such as silicon nitride or silicon dioxide or a combination thereof. The sidewall isolation layer 420 extends along the laterally opposite sidewalls 326 and 328 of the gate electrode 324, as shown in FIG. 4A, thereby electrically insulating the semiconductor film 410 from the gate electrode 324, as shown in FIG. 4A. In the embodiment of the present invention, the sidewall isolation layer 420 has a thickness between 20-200 Å. By adding silicon or semiconductor films to the source and drain regions 330 and 332 of the semiconductor body and forming "bumped" source and drain regions, the thickness of the source and drain regions is increased, thereby reducing the source/drain region. The contact resistance of the drain to the transistor 300 is improved, and its electrical characteristics and performance are improved.

[0031]

In the embodiment of the present invention, a silicide film 430 is formed on the source region 330 and the drain region 332, such as but not limited to titanium silicide, nickel silicide, and cobalt silicide.

In the embodiment of the present invention, a silicide film 430 is formed on the silicon film 410 of the silicon body 308, as shown in FIG. 4A. However, the silicide film 430 may also be formed directly on the top surface 316 of the silicon body 308. For example, by first forming a silicon film such as an undoped silicon film and a silicon body, and then completely consuming the

silicon film in the silicidation process, the silicide film 430 can be formed on the silicon body 308. The dielectric isolation layer 420 makes it possible to form the silicide film 430 on the semiconductor body 308 or the silicon film 410 in a self-aligning process (ie, a silicidation process).

[0032]

In addition, in the described embodiment of the present invention, a semiconductor or silicon film 440 may also be formed on the top of the gate electrode 324, just as the silicide film 450 is formed on the top surface of the gate electrode 325.

The silicide film 450 and the silicon film 440 are generally formed at the same time as the silicide film 430 and the silicon film 410 are formed on the silicon body 308. Forming the silicon film 440 on the silicide film 450 on the gate electrode reduces the contact resistance to the gate, thereby improving the electrical performance of the transistor 300.

[0033]

As described above, the gate "width" of the transistor 300 is equal to the sum of the three gate widths created from the semiconductor body 308 of the transistor 300.

In order to process a transistor with a larger gate width, the transistor 300 may include additional or more semiconductor bodies or fingers 308, as shown in FIG. 4B. Each semiconductor body 308 has a gate dielectric layer 322 formed on its top surface and sidewalls, as shown in FIG. 4B. The gate electrode 324 is formed on or adjacent to each gate dielectric 322 of each of the plurality of semiconductor bodies 308. Each semiconductor body 308 further includes a source region 330 and a drain region 332, both of which are formed on the side of the semiconductor body 308 opposite to the gate electrode 324, as shown in FIG. 4B. In the embodiment of the present invention, each semiconductor body 308 is formed to have the same width and height (thickness) as the other semiconductor bodies 308. In the embodiment of the present invention, each source region 330 and drain region 332 of the plurality of semiconductor bodies 308 are electrically coupled with the semiconductor material used to form the semiconductor body 308 to form a source attachment block 460 and The drain attachment block 480 is shown in FIG. 4B. Alternatively, multiple sources 330 and multiple drains may be connected by a high-level metalization process (such as metal 1, metal 2, metal 3...) for electrically interconnecting various transistors 300 into functional circuits. The poles 332 are coupled together. The gate width of the transistor 300 shown in FIG. 4B is equal to the sum of the gate widths created by each of the plurality of semiconductor bodies 308. In this way, a tri-gate transistor 300 having any desired gate width can be formed.

[0034]

5A-5J illustrate a method for processing a tri-gate transistor according to an embodiment of the present invention.

The processing of the tri-gate transistor starts at the substrate 502. A silicon or semiconductor film 508 is formed on the substrate 502, as shown in FIG. 5A. In an embodiment of the present invention, the substrate 502 is an insulating substrate, as shown in FIG. 5A. In the embodiment of the present invention, the insulating substrate 502 includes a lower monocrystalline silicon substrate 504 and a top insulating layer 506, such as a silicon dioxide film or a silicon nitride film. The insulating layer 506 insulates the semiconductor film 508 from the substrate 504, and is formed to have a thickness of 200-2000 Å in the embodiment. The insulating layer 506 is sometimes referred to as a "buried oxide" layer. When the silicon or semiconductor film 508 is formed on the insulating substrate 502, a silicon-on-insulator or semiconductor (SOI) substrate 500 is also created. In other embodiments of the present invention, the substrate 502 may be a semiconductor substrate, such as but not limited to a silicon single crystal substrate and a gallium arsenide substrate.

[0035]

Although the semiconductor film 508 is ideally a silicon film, in other embodiments, it may be other types of semiconductor films, such as but not limited to germanium (Ge), silicon germanium alloy (SixGe_y), gallium arsenide (GaAs), InSb, GaP, GaSb and carbon nanotubes.

In the embodiment of the present invention, the semiconductor film 508 is an intrinsic (ie undoped) silicon film. In other embodiments, the semiconductor film 508 is doped with P-type or N-type conductivity, and has a concentration level between 1×10^{16} - 1×10^{19} atoms/cm³. By, for example, ion implantation, the semiconductor film 508 can be insitu doped (ie, doped during deposition), or doped after it is formed on the substrate 502. Doping after formation makes it possible to simultaneously process PMOS and NMOS tri-gate devices on the same insulating substrate. At this time, the doping level of the semiconductor body determines the doping level of the channel region of the device.

[0036]

The semiconductor film 508 is formed to have a thickness approximately equal to the desired height of the semiconductor body or bodies of the tri-gate transistor to be subsequently formed.

In an embodiment of the present invention, the semiconductor film 508 has a thickness or height 509 less than 30 nanometers, and ideally less than 20 nanometers. In the embodiment of the present invention, the semiconductor film 508 is formed to have a thickness approximately equal to the desired gate "length" of the processed tri-gate transistor. In the embodiment of the present invention, the semiconductor film 508 is formed to be thicker than the desired gate length of the device. In the embodiment of the present invention, the semiconductor film 508 is formed to have a thickness that allows the processed tri-gate transistor to operate in a fully depleted manner for its designed gate length (Lg).

[0037]

The semiconductor film 508 can be formed on the insulating substrate 502 in any well-known method.

In a method of forming a silicon-on-insulator substrate called SIMOX technology, a high dose of oxygen atoms is implanted into a single crystal silicon substrate and then annealed to form a buried oxide layer 506 in the substrate. The portion of the single crystal silicon substrate on the buried oxide layer becomes the silicon film 508. Another technology currently used to form SOI substrates is the epitaxial silicon film transfer technology, which is generally referred to as bonded SOI (bonded SOI). In this technique, the first silicon wafer has a thin layer of oxide grown on its surface, which will be used as the buried oxide layer 506 in the SOI structure later. Then, a high dose of hydrogen is injected into the first silicon wafer to form a high-pressure region under the silicon surface of the first wafer. Then the first wafer is turned over and bonded to the surface of the second silicon wafer. The first wafer is then cleaved along the high-pressure plane generated by the hydrogen injection. This results in an SOI structure with a thin silicon layer on top and a buried oxide layer on top of the single crystal silicon substrate underneath. Various well-known smoothing techniques such as HC smoothing or chemical mechanical polishing (CMP) can be used to smooth the top surface of the semiconductor film 508 until the desired thickness is obtained.

[0038]

At this time, if desired, an insulating region (not shown) may be formed in the SOI substrate 500 to insulate the transistors to be formed therein from each other.

By using, for example, well-known photolithography and etching techniques to etch away the portion of the substrate 508 surrounding the tri-gate transistor, and then backfill the etched area with an insulating film such as SiO₂, an insulating region can be formed.

[0039]

In order to form a tri-gate transistor on the substrate 500, a photoresist mask 510 is formed on the semiconductor film 508, as shown in FIG. 5B.

The photoresist mask 510 includes a pattern or a plurality of patterns 512 that define a position where a semiconductor body or fin-shaped portion is subsequently formed in the semiconductor film 508. The photoresist pattern 512 defines a desired width 518 of the semiconductor body or fin portion of the tri-gate transistor to be formed later. In an embodiment of the present invention, the pattern 512 defines a fin-shaped portion or body having a width 518, wherein the width 518 is equal to or greater than a desired width of the gate length (Lg) of the processed transistor. In this way, the most stringent photolithographic constraints for processing transistors are associated with gate electrode patterns instead of semiconductor body or fin definitions. In an embodiment of the present invention, the semiconductor body or fin-shaped portion will have a width 518 less than or equal to 30 nanometers, and ideally less than or equal to 20 nanometers. In an embodiment of the present invention, the pattern 512 for the semiconductor body or fin has a width 518 approximately equal to the height 509 of the silicon body. In an embodiment of the present invention, the photoresist pattern 512 has a width 518 between 1/2 of the height of the semiconductor body 509 and twice the height of the semiconductor body 509.

[0040]

In addition, as shown in FIG. 5B, the photoresist mask 510 may further include patterns 514 and 516 for defining positions for forming the source attachment block and the drain attachment block, respectively.

The attachment block can be used to connect the source regions of the processed transistors together, and connect the drain regions together. The photoresist mask 510 can be formed by a well-known photolithography technique including mask setting, exposure, and development of the deposited photoresist film.

[0041]

After the photoresist mask 510 is formed, the semiconductor film 508 is etched in alignment with the photoresist mask 510 to form one or more silicon bodies or fin-shaped portions, and source and drain attachment blocks (if desired). As shown in Figure 5C.

The semiconductor film 508 is etched until the underlying buried oxide layer 506 is exposed. A well-known semiconductor etching technique such as anisotropic plasma etching or reactive ion etching may be used to etch the semiconductor film 508 in alignment with the mask 510, as shown in FIG. 5C.

[0042]

After the semiconductor film 508 is etched to form the semiconductor body or fin portion 520 (and the source/drain attachment blocks 522 and 524, if desired), the photoresist mask is removed by well-known techniques such as chemical lift-off and O₂ ash removal. Film to yield the substrate shown in Figure 5D.

[0043]

Then, a gate dielectric layer 526 is formed on and around each semiconductor body 520.

That is, the gate dielectric layer 526 is formed on the top surface 527 of each semiconductor body 520 and on the laterally opposite sidewalls 528 and 529 of each semiconductor body 520.

The gate dielectric can be a deposited dielectric or a grown dielectric. In the embodiment of the present invention, the gate dielectric layer 526 is a silicon dioxide dielectric film grown by a dry/wet oxidation process. In the embodiment of the present invention, the silicon dioxide film is grown to a thickness between 5-15 angstroms. In the embodiment of the present invention, the gate dielectric film 526 is a deposited dielectric, such as but not limited to a film with a higher dielectric constant, such as a metal oxide dielectric, such as tantalum pentoxide (Ta₂O₅) and titanium oxide (TiO₂). And other high-K dielectrics, such as PZT and BST. A film with a relatively high dielectric constant can be formed by any well-known technique such as chemical vapor deposition (CVD).

[0044]

Then, as shown in FIG. 5E, a gate electrode 530 is formed.

The gate electrode 530 is formed on the gate dielectric layer 526 formed on the top surface 527 of each semiconductor body 520, and formed on or adjacent to the sidewalls 528 and 529 of each semiconductor body. On or adjacent to the gate dielectric 526, as shown in Figure 5E. The gate electrode 530 has a top surface 532 opposite to the bottom surface formed on the insulating substrate 502, and has a pair of laterally opposite sidewalls 534 and 536. The distance between laterally opposed sidewalls 534 and 536 defines the gate length (L_g) 538 of the tri-gate transistor. The gate electrode 530 may be formed by covering and depositing a suitable gate electrode material on the substrate shown in FIG. 5D. The gate electrode may be formed to have a thickness between 200-3000 Å. In an embodiment, the gate electrode has a thickness or height 533 that is at least 3 times the height 509 of the semiconductor body 520. The gate electrode material can then be patterned by a well-known photolithography or etching technique to form the gate electrode 530 from the gate electrode material. In an embodiment of the present invention, the gate electrode material includes polysilicon. In another embodiment of the present invention, the gate electrode material includes polycrystalline silicon germanium alloy. In another embodiment of the present invention, the gate electrode material may include a metal film, such as tungsten, tantalum and their nitrides. The gate electrode 530 may be formed by a known technique, for example, a gate electrode material is deposited on the substrate of FIG. 5D, and then the gate electrode material is patterned by a known photolithography or etching technique. In another embodiment of the present invention, the photolithography process for defining the gate electrode 530 utilizes the minimum or minimum size photolithography process for processing the tri-gate transistor. (That is, in the embodiment of the present invention, the gate

length (L_g) 538 of the gate electrode 530 has the minimum feature size of the transistor defined by photolithography.) In the embodiment of the present invention, the gate length 538 is less than or equal to 30 nanometers, and ideally less than or equal to 20 nanometers.

[0045]

Then, the source and drain regions of the transistor are formed on the side of the semiconductor body 520 opposite to the gate electrode 530.

In an embodiment of the present invention, the source and drain regions include tips or source/drain extension regions. The source and drain extension regions 540 and 542 can be respectively formed by placing the dopant 544 in the two side faces 532 and 534 of the gate electrode 530 in the semiconductor body 520 to form the tip regions 540 and 542. As shown in Figure 5F. The source and drain attachment blocks 522 and 524 are not shown in FIGS. 5F-5J to better illustrate aspects of the present invention. If the source and drain attachment blocks 522 and 524 are used, they can also be doped at this time. For a PMOS tri-gate transistor, the semiconductor fin or body 520 is doped with P-type conductivity and has a concentration of 1×10^{20} - 1×10^{21} atoms/cm³. For an NMOS tri-gate transistor, the semiconductor fin-shaped portion or body 520 is doped with n-type conductivity ions to have a concentration of 1×10^{20} - 1×10^{21} atoms/cm³. In the embodiment of the present invention, ion implantation is used to dope the silicon film. In the embodiment of the present invention, ion implantation is performed in a vertical direction (ie, a direction perpendicular to the substrate 500), as shown in FIG. 5F. When the gate electrode 530 is a polysilicon gate electrode, it may be doped during the ion implantation process. The gate electrode 530 serves as a mask to prevent the channel region(s) 548 of the tri-gate transistor from being doped by the ion implantation step. The channel region 548 is a part of the silicon body 520 located under or surrounded by the gate electrode 530. If the gate electrode 530 is a metal electrode, a dielectric hard mask can be used to block the doping during the ion implantation process. In other embodiments, other methods such as solid-state source diffusion may be used to dope the semiconductor body to form source and drain extensions.

[0046]

In various embodiments of the present invention, before forming the source/drain regions or source/drain extension regions, a "halo" region may be formed in the silicon body.

The Halo region is a doped region formed in the channel region 548 of the device, which has the same conductivity as the channel region of the device, but has a slightly higher doping concentration than the channel region of the device. Using the ion implantation technique at a larger angle, the halo region can be formed by ion implantation of dopants under the gate electrode.

[0047]

Then, if desired, the substrate in Figure 5F can be further processed to form additional features, such as heavily doped source/drain contact regions, source and drain regions, and deposited silicon on the gate electrode, and a silicide is formed on the source/drain contact area and the gate electrode.

[0048]

In various embodiments of the present invention, the dielectric sidewall isolation layer 550 may be formed on the sidewall of the gate electrode.

The sidewall isolation layer can be used to compensate for heavy source/drain contact implantation, insulate the source/drain region from the gate electrode in the selective silicon deposition process, and in the source and drain in the silicidation process. Silicide is formed on the region and the gate electrode.

The isolation layer may be formed by covering and depositing a conformal dielectric film 550 on the substrate 500 of FIG. 5F, the dielectric film being, for example, but not limited to, silicon nitride, silicon oxide, silicon oxynitride, or a combination thereof. The dielectric film is deposited in a conformal manner so that it is formed to have approximately equal heights on the vertical surface and the horizontal surface. The vertical surface shown is, for example, the sidewalls 534 and 536 of the gate electrode 530, and the horizontal surface is, for example, These are the top 526 of the silicon film 520 and the top of the gate electrode 530. In an embodiment of the present invention, the dielectric film is a silicon nitride film formed by a hot wall low pressure chemical vapor deposition (LPCVD) process. The deposition thickness of the dielectric film determines the width or thickness of the isolation layer formed. In the embodiment of the present invention, the illustrated dielectric film is formed to have a thickness between 20-200 Å.

[0049]

Then, as shown in FIG. 5G, the dielectric film is anisotropically etched by, for example, plasma etching or reactive ion etching to form a sidewall isolation layer 550.

The anisotropic etching of the dielectric film removes the dielectric film from a horizontal surface such as the top of the gate electrode 530 (and the top of the attachment blocks 522 and 524, if used), and leaves the vertical surface such as the gate electrode 530. The sidewalls 534 and 536 are adjacent to the dielectric sidewall isolation layer. The etching lasts for a sufficiently long time to remove the dielectric film from all horizontal surfaces. In the embodiment of the present invention, over-etching is used, so that the isolation layer material on the sidewall of the semiconductor body 520 can be removed, as shown in FIG. 5G. As a result, a sidewall spacer 550 is formed, which extends along and adjacent to the sidewalls 532 and 534 of the gate electrode 530, as shown in FIG. 5H.

[0050]

Then, if desired, a semiconductor film 560 may be formed on the exposed surface of the semiconductor body 520 (and on the attachment blocks 522 and 524), as shown in FIG. 5H.

In addition, if desired, a semiconductor film 562 may be formed on top of the gate electrode 530. The semiconductor film may be a single crystal film or a polycrystalline film. In the embodiment of the present invention, the semiconductor film 560 is an epitaxial (single crystal) silicon film. In the embodiment of the present invention, the silicon film 560 is formed by a selective deposition process, so that silicon is formed only on exposed areas containing silicon, such as the top surface 527 and the sidewalls 528 and 529 of the silicon body 520. In the selective deposition process, no silicon film is formed on the dielectric region such as the sidewall spacer 555. When the gate electrode 530 includes a polysilicon film, a silicon film may also be selectively formed on the top surface of the gate electrode 530 to form the silicon film 562. In the embodiment of the present invention, the silicon film 560 is formed to have a thickness between 50-500 Å. In the embodiment of the present invention, the silicon film is formed to have a thickness sufficient to provide enough silicon to be used or consumed during the formation of the silicon film on the source and drain regions. The silicon film may be doped instantaneously (ie, doped during deposition) or subsequently doped, by, for example, ion implantation or solid-state source diffusion. The silicon film is doped to the desired conductivity type for the source and drain regions of the device. In the embodiment of the present invention, the deposited silicon films 560 and 562 are intrinsic silicon films (ie, undoped silicon films). The deposition of the semiconductor film 560 forms raised source and drain regions, which improves the parasitic effect of the device.

[0051]

In the embodiment of the present invention, as shown in FIG. 5I, the deposited silicon films 560 and 562 are doped by ion implantation using a vertical ion implantation angle.

The ion implantation process doped the deposited silicon film 560 and the underlying silicon body 520 to have a concentration of 1×10^{20} to 1×10^{21} atoms/cm³ to form a source contact region 570 and a drain contact region 572. The sidewall isolation layer 550 compensates for the source/drain contact implantation step, and defines the region of the doped silicon body under the sidewall isolation layer 550 as the tip region. The above process forms the source region 570 and the drain region 572, both of which include the tip region and the contact region. The tip area is the area where the silicon body 520 is located under the sidewall isolation layer 550. The contact area is the area where the silicon body and the deposited silicon film are adjacent to the outer edge of the sidewall isolation layer 550. In addition, if the source and drain attachment blocks 522 and 524 are used, the source/drain contact area includes the source and drain attachment blocks 522 and 524.

[0052]

Then, if desired, a refractory metal silicide 580 may be formed on the top surface (or silicon film 562) of the source and drain contact regions and the gate electrode 530, as shown in FIG. 5J.

The refractory metal silicide film 580 may be formed by a self-aligning process such as a silicidation process. In the silicidation process, a refractory metal film, such as titanium, tungsten, nickel, cobalt, etc., is deposited on the substrate of FIG. 5J. The substrate is then heated to a suitable temperature so that the refractory metal film reacts with the silicon part of the substrate 500 to form a refractory metal silicide. The silicon part is, for example, a silicon film 560 formed on the silicon body and a gate electrode 530. The positions where there is no silicon that can react, such as the exposed parts of the

dielectric isolation layer 555 and the buried oxide layer 506, do not react, and are still refractory metals. Then, selective etching, such as wet etching, can be used to remove the unreacted refractory metal, while retaining the refractory metal silicide on the contact area. In this way, the metal silicide film can be self-aligned with the contact area of the tri-gate transistor. This completes the processing of the tri-gate transistor according to the present invention.

{0053}

So far, the tri-gate transistor and its processing method have been described.



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CLAIMS CN1518771A

1.

A semiconductor device including:

The semiconductor body is formed on the substrate film and has a top surface and laterally opposite sidewalls;

A gate dielectric formed on the top surface of the silicon body and on the laterally opposite sidewalls of the silicon body; and

A gate electrode is formed on the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the laterally opposite sidewalls of the silicon body.

2.

The device of claim 1, wherein the semiconductor body is silicon.

3.

The device of claim 1, wherein the semiconductor body single crystal film.

4.

The device of claim 2, wherein the semiconductor body is intrinsic single crystal silicon.

5.

The device of claim 1, wherein the semiconductor body is made of silicon (Si), germanium (Ge), silicon germanium (SixGe_y), gallium arsenide (GaAs), InSb, GaP, GaSb, and carbon nanotubes The semiconductor selected from the group consisting of.

6.

The semiconductor device according to claim 1, wherein the substrate is an insulating substrate.

7.

The semiconductor device according to claim 1, wherein the substrate is a semiconductor substrate.

8.

A tri-gate transistor including:

A monocrystalline silicon body formed on an insulating substrate, the silicon body having a top surface and first and second laterally opposite sidewalls;

A gate dielectric formed on the top surface of the silicon body and on the first and second laterally opposite sidewalls of the silicon body;

A gate electrode formed on the gate dielectric on the top surface of the silicon body, and on the sidewalls opposite to the first and second lateral sides of the silicon body Adjacent to the gate dielectric; and

A pair of source/drain regions are formed on opposite sides of the gate electrode in the silicon body.

9.

8. The tri-gate transistor of claim 8, wherein the transistor has a gate length (L_g) approximately equal to the distance between the first and second laterally opposed sidewalls of the silicon body.

10.

8. The tri-gate transistor according to claim 8, wherein the transistor has a gate length (L_g) approximately equal to the distance of the insulating film to the top surface of the silicon body.

11.

8. The tri-gate transistor of claim 8, wherein the distance between the laterally opposed sidewalls of the silicon body is approximately equal to the distance from the insulating substrate to the top surface of the silicon body distance.

12.

8. The tri-gate transistor of claim 8, wherein the distance between the laterally opposed sidewalls of the semiconductor is 1/2 to 2 times the thickness of the silicon body on the insulating surface between.

13.

8. The tri-gate transistor of claim 8, wherein the monocrystalline silicon body is intrinsic silicon.

14.

8. The tri-gate transistor according to claim 8, wherein the monocrystalline silicon body is doped to have the first conductivity type, and its doping concentration is between 1×10^{16} - 1×10^{20} atoms/cm³.

15.

The tri-gate transistor according to claim 14, wherein the single crystal silicon body is doped to have the first conductivity type, and the doping concentration is between 1×10^{16} - 1×10^{18} atoms/cm³.

16.

8. The tri-gate transistor according to claim 8, further comprising a pair of sidewall spacers formed along laterally opposite sidewalls of the gate electrode.

17.

8. The tri-gate transistor of claim 8, wherein the source/drain region pair further includes silicon formed on and around the silicon body.

18.

The tri-gate transistor of claim 15, wherein the silicon on the source/drain regions is epitaxial silicon.

19.

A type of transistor including:

A plurality of semiconductor bodies formed on the substrate film, each of the bodies having a top surface and a pair of laterally opposite sidewalls;

A gate dielectric formed on the top surface and sidewalls of each of the plurality of semiconductor bodies;

A gate electrode formed on the gate dielectric on the top surface of each of the plurality of semiconductor bodies, and the first and second portions of each of the plurality of silicon bodies Adjacent to the gate dielectric on laterally opposite sidewalls; and

A pair of source/drain regions are formed on opposite sides of the gate electrode in each of the plurality of semiconductor bodies.

20.

The transistor of claim 19, wherein the gate width of the transistor is approximately the sum of the gate widths of each of the plurality of semiconductor bodies, wherein the gate width of the semiconductor body is the same as that of the semiconductor body 2 times the height plus the distance between the laterally opposed side walls.

21.

The transistor of claim 19, wherein the distance between the laterally opposed sidewalls of each of the plurality of semiconductor bodies is substantially the same.

22.

The transistor of claim 19, wherein each of the source regions are coupled together and each of the drain regions are coupled together.

23.

The transistor of claim 19, wherein the substrate is an insulating substrate.

24.

The transistor according to claim 19, wherein the substrate is a semiconductor substrate.

25.

A fully depleted semiconductor-on-insulator transistor, including:

Silicon body, formed on the insulating film;

A gate dielectric formed on and around the silicon body;

A gate electrode formed on the gate dielectric on and around the silicon body;

A pair of source/drain regions formed on opposite sides of the gate electrode in the silicon body;

Wherein the gate length of the transistor is less than or equal to the width of the silicon body; and

When the transistor is "on", the silicon body between the source/drain regions is fully depleted.

26.

The transistor of claim 25, wherein the gate length is less than 60 nanometers.

27.

The transistor of claim 25, wherein the gate length is less than 30 nanometers.

28.

The transistor of claim 25, wherein the gate length is less than 20 nanometers.

29.

The transistor according to claim 25, wherein the gate length is less than or equal to the height of the semiconductor body on the insulating film.

30.

The transistor according to claim 25, wherein the semiconductor body is a single crystal silicon film.

31.

The transistor according to claim 30, wherein said single crystal silicon film is intrinsic silicon.

32.

A fully depleted silicon-on-insulator transistor including:

Silicon body, formed on an insulating substrate;

A gate dielectric formed on and around the silicon body;

A gate electrode formed on and adjacent to the gate dielectric on and around the silicon body;

A pair of source/drain regions formed on opposite sides of the gate electrode in the silicon body; and

The transistor has a very steep sub-threshold slope of less than 80 mV/decade and a leakage field induced barrier reduction effect of less than 100 mV/V.

33.

The transistor of claim 32, wherein the drain field induced barrier reduction effect is less than 80 mV/V.

34.

The transistor of claim 32, wherein said sub-threshold slope is approximately 60 mV/decade.

35.

A method of forming a semiconductor device includes:

Forming a semiconductor body on the substrate film, which has a top surface and laterally opposite sidewalls;

Forming a gate dielectric on the top surface of the semiconductor body and on the laterally opposed sidewalls of the semiconductor body; and

A gate electrode is formed on the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the laterally opposite sidewalls of the silicon body.

36.

The method of claim 35, wherein the semiconductor body comprises single crystal silicon.

37.

The method of claim 36, wherein the monocrystalline silicon body is intrinsic silicon.

38.

The method of claim 35, wherein the semiconductor body is made of silicon (Si), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), InSb, GaP, GaSb, and carbon nanotubes. The semiconductor selected from the group consisting of:

39.

The method of forming the device according to claim 35, wherein the thickness of the silicon body from the insulating film to the top surface of the silicon body is approximately equal to the thickness between the laterally opposed sidewalls of the silicon body.

40.

The method of claim 35, wherein the thickness of the silicon body from the insulating layer to the top surface is between 2 times and 1/2 of the distance between the laterally opposed sidewalls.

41.

The method of claim 35, wherein the substrate is an insulating substrate.

42.

The method of claim 35, wherein the substrate is a semiconductor substrate.

43.

A method of forming a silicon-on-insulator transistor includes:

Pattern the silicon film formed on the insulating substrate into a silicon body having a top surface opposite to the bottom surface formed on the insulating film, and first and second laterally opposite sidewalls;

Form a gate dielectric layer on the top surface of the silicon body and on the sidewalls of the silicon body;

Deposit gate material on the silicon body and on the insulating substrate;

The gate material is patterned to be on the gate dielectric layer on the top surface of the silicon body and adjacent to the gate dielectric on the sidewalls of the silicon body. Form a gate electrode, the gate electrode having laterally opposed sidewalls extending perpendicular to the laterally opposed sidewalls of the silicon body; and

In the silicon body, a pair of source/drain regions are formed on opposite sides of the laterally opposite sidewalls of the gate electrode.

44.

The method of claim 43, wherein the distance between the laterally opposed sidewalls of the silicon body is approximately equal to the thickness of the silicon body on the insulating substrate.

45.

The method of claim 43, wherein the distance (gate length) between the laterally opposed sidewalls of the gate electrode is less than or equal to the distance between the laterally opposed sidewalls of the silicon body.

46.

The method according to claim 43, wherein the distance (gate length) between the laterally opposed sidewalls of the gate electrode is less than or equal to the thickness of the silicon body on the insulating film.

47.

The method according to claim 43, wherein said silicon film is single crystal silicon.

48.

The method of claim 47, wherein the single crystal silicon film is intrinsic silicon.

49.

The method of claim 43, further comprising forming a pair of sidewall spacers on opposite sides of the laterally opposite sidewalls of the gate electrode; and

A silicon film is formed on and around the silicon body and adjacent to the sidewall isolation layer.

50.

The method of claim 43, further comprising forming a silicide on the silicon film formed on the silicon body.

51.

The method of claim 43, wherein the silicon film is formed by a selective deposition process.

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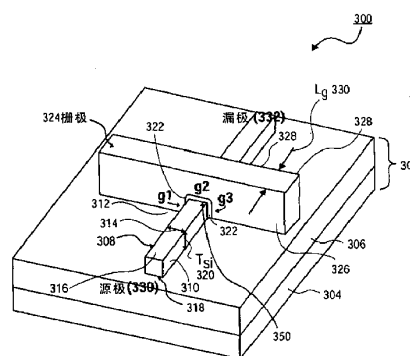
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权利要求书 6 页 说明书 15 页 附图 10 页

[54] 发明名称 三栅极器件及其加工方法

[57] 摘要

本发明公开了一种半导体器件，包括形成在衬底上的半导体主体，其具有顶表面和横向相对的侧壁。在半导体主体的顶表面上以及半导体主体的横向相对的侧壁上形成栅极电介质层。在半导体主体的顶表面上的栅极电介质上以及与半导体主体的横向相对的侧壁上的栅极电介质的相邻处形成栅极电极。



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1. 一种半导体器件，包括：
半导体主体，形成在衬底膜上，具有顶表面和横向相对的侧壁；
5 栅极电介质，形成在所述硅主体的所述顶表面上，以及所述硅主体的所述横向相对的侧壁上；以及
栅极电极，形成在所述半导体主体的所述顶表面上的所述栅极电介质上，以及与所述硅主体的所述横向相对的侧壁上的所述栅极电介质相邻处。
- 10 2. 如权利要求 1 所述的器件，其中所述半导体主体是硅。
3. 如权利要求 1 所述的器件，其中所述半导体主体单晶体膜。
4. 如权利要求 2 所述的器件，其中所述半导体主体是本征单晶硅。
5. 如权利要求 1 所述的器件，其中所述半导体主体是从由硅（Si）、
锗（Ge）、锗化硅（ Si_xGe_y ）、砷化镓（GaAs）、InSb、GaP、GaSb 以及
15 碳纳米管构成的组中选择的半导体。
6. 如权利要求 1 所述的半导体器件，其中所述衬底是绝缘衬底。
7. 如权利要求 1 所述的半导体器件，其中所述衬底是半导体衬底。
8. 一种三栅极晶体管，包括：
单晶硅主体，形成在绝缘衬底上，所述硅主体具有顶表面和第一与
20 第二横向相对的侧壁；
栅极电介质，形成在所述硅主体的所述顶表面上，以及所述硅主体的所述第一与第二横向相对的侧壁上；
栅极电极，形成在所述硅主体的所述顶表面上的所述栅极电介质之上，以及与所述硅主体的所述第一与第二横向相对的侧壁上的所述栅
25 极电介质相邻处；以及
一对源极/漏极区，形成在所述硅主体中所述栅极电极的相对侧面上。
9. 如权利要求 8 所述的三栅极晶体管，其中所述晶体管具有约等于所述硅主体的所述第一和第二横向相对的侧壁之间的距离的栅极长度（ L_g ）。

10. 如权利要求 8 所述的三栅极晶体管，其中所述晶体管具有约等于所述绝缘膜到所述硅主体的顶表面的距离的栅极长度（Lg）。

11. 如权利要求 8 所述的三栅极晶体管，其中所述硅主体的所述横向相对的侧壁之间的所述距离约等于从所述绝缘衬底到所述硅主体的顶表面
5 之间的距离。

12. 如权利要求 8 所述的三栅极晶体管，其中所述半导体的所述横向相对的侧壁之间的所述距离在所述绝缘表面上的所述硅主体的厚度的 1/2 到 2 倍之间。

13. 如权利要求 8 所述的三栅极晶体管，其中所述单晶硅主体是本
10 征硅。

14. 如权利要求 8 所述的三栅极晶体管，其中所述单晶硅主体掺杂成具有第一导电性类型，其掺杂浓度在 $1 \times 10^{16} - 1 \times 10^{20}$ 原子数/cm³ 之间。

15. 如权利要求 14 所述的三栅极晶体管，其中所述单晶硅主体掺杂
15 成具有第一导电性类型，其掺杂浓度在 $1 \times 10^{16} - 1 \times 10^{18}$ 原子数/cm³ 之间。

16. 如权利要求 8 所述的三栅极晶体管，还包括一对沿着所述栅极电极的横向相对的侧壁而形成的侧壁隔离层。

17. 如权利要求 8 所述的三栅极晶体管，其中所述源极/漏极区对还包
20 括形成在所述硅主体之上及其周围的硅。

18. 如权利要求 15 所述的三栅极晶体管，其中所述源极/漏极区上的硅是外延硅。

19. 一种晶体管，包括：

多个半导体主体，形成在衬底膜上，每个所述主体都具有顶表面和一
25 对横向相对的侧壁；

栅极电介质，形成在所述多个半导体主体中的每一个的顶表面和侧壁上；

栅极电极，形成在所述多个半导体主体中的每一个的所述顶表面上的所述栅极电介质之上，以及所述多个硅主体中的每一个的所述第一与第二

横向相对的侧壁上的所述栅极电介质相邻处；以及

一对源极/漏极区，形成在所述多个半导体主体中的每一个中所述栅极电极的相对侧面上。

20. 如权利要求 19 所述的晶体管，其中所述晶体管的所述栅极宽度大约
5 是所述多个半导体主体中的每一个的栅极宽度的总和，其中半导体主体的栅极宽度是所述半导体主体的高度的 2 倍加上所述横向相对的侧壁之间的距离。

21. 如权利要求 19 所述的晶体管，其中所述多个半导体主体中的每一个的所述横向相对的侧壁之间的距离基本相同。

10 22. 如权利要求 19 所述的晶体管，其中所述源极区中的每一个都耦合在一起，并且所述漏极区中的每一个都耦合在一起。

23. 如权利要求 19 所述的晶体管，其中所述衬底是绝缘衬底。

24. 如权利要求 19 所述的晶体管，其中所述衬底是半导体衬底。

25. 一种全耗尽型绝缘体上半导体晶体管，包括：
15 硅主体，形成在绝缘膜上；
栅极电介质，形成在所述硅主体之上及其周围；
栅极电极，形成在所述硅主体之上及其周围的所述栅极电介质上；
一对源极/漏极区，形成在所述硅主体中所述栅极电极的相对侧面上；
其中所述晶体管的所述栅极长度小于或等于所述硅主体的宽度；并且
20 当所述晶体管“导通”时，所述源极/漏极区之间的硅主体是全耗尽的。

26. 如权利要求 25 所述的晶体管，其中所述栅极长度小于 60 纳米。

27. 如权利要求 25 所述的晶体管，其中所述栅极长度小于 30 纳米。

28. 如权利要求 25 所述的晶体管，其中所述栅极长度小于 20 纳米。

25 29. 如权利要求 25 所述的晶体管，其中所述栅极长度小于或等于所述绝缘膜上的所述半导体主体的高度。

30. 如权利要求 25 所述的晶体管，其中所述半导体主体是单晶硅膜。

31. 如权利要求 30 所述的晶体管，其中所述单晶硅膜是本征硅。

32. 一种全耗尽型绝缘体上硅晶体管，包括：

硅主体，形成在绝缘衬底上；

栅极电介质，形成在所述硅主体之上及其周围；

栅极电极，形成在所述硅主体之上及其周围的所述栅极电介质之上及与之相邻处；

- 5 一对源极/漏极区，形成在所述硅主体中所述栅极电极的相对侧面上；
并且

其中所述晶体管具有非常陡峭的小于 80mV/decade 的亚阈值斜率和小于 100mV/V 的漏场感应势垒降低效应。

33. 如权利要求 32 所述的晶体管，其中所述漏场感应势垒降低效应小
10 于 80mV/V。

34. 如权利要求 32 所述的晶体管，其中所述亚阈值斜率约是 60mV/decade。

35. 一种形成半导体器件的方法，包括：

在衬底膜上形成半导体主体，其具有顶表面和横向相对的侧壁；

- 15 在所述半导体主体的所述顶表面上以及所述半导体主体的所述横向相对的侧壁上形成栅极电介质；以及

在所述半导体主体的所述顶表面上的所述栅极电介质上、以及与所述硅主体的所述横向相对的侧壁上的所述栅极电介质相邻处形成栅极电极。

36. 如权利要求 35 所述的方法，其中所述半导体主体包含单晶硅。

- 20 37. 如权利要求 36 所述的方法，其中所述单晶硅主体是本征硅。

38. 如权利要求 35 所述的方法，其中所述半导体主体是从由硅（Si）、锗（Ge）、锗化硅（Si_xGe_y）、砷化镓（GaAs）、InSb、GaP、GaSb 以及碳纳米管构成的组中选择的半导体。

39. 如权利要求 35 所述的形成所述器件的方法，其中所述硅主体从所述绝缘膜到所述硅主体顶表面的厚度约等于所述硅主体的所述横向相对的侧壁之间的距离。
25

40. 如权利要求 35 所述的方法，所述硅主体从所述绝缘层到所述顶表面的厚度在所述横向相对的侧壁之间的距离的 2 倍到 1/2 之间。

41. 如权利要求 35 所述的方法，其中所述衬底是绝缘衬底。

42. 如权利要求 35 所述的方法，其中所述衬底是半导体衬底。

43. 一种形成绝缘体上硅晶体管的方法，包括：

将形成在绝缘衬底上的硅膜图案化成一种硅主体，其具有与形成在所述绝缘膜上的底表面相对的顶表面，以及第一和第二横向相对的侧壁；

5 在所述硅主体的所述顶表面上和所述硅主体的所述侧壁上形成栅极电介质层；

在所述硅主体上和所述绝缘衬底上沉积栅极材料；

图案化所述栅极材料，以在所述硅主体的所述顶表面上的所述栅极电介质层之上以及与所述硅主体的所述侧壁上的所述栅极电介质相邻处形成
10 栅极电极，所述栅极电极具有垂直于所述硅主体的所述横向相对的侧壁而延伸的横向相对的侧壁；以及

在所述硅主体中，在所述栅极电极的所述横向相对的侧壁的相对侧面上形成一对源极/漏极区。

44. 如权利要求 43 所述的方法，其中所述硅主体的所述横向相对的侧
15 壁之间的距离约等于所述绝缘衬底上的所述硅主体的厚度。

45. 如权利要求 43 所述的方法，其中所述栅极电极的所述横向相对的侧壁之间的距离（栅极长度）小于或等于所述硅主体的横向相对的侧壁之间的距离。

46. 如权利要求 43 所述的方法，其中所述栅极电极的所述横向相对的
20 侧壁之间的距离（栅极长度）小于或等于所述绝缘膜上的所述硅主体的厚度。

47. 如权利要求 43 所述的方法，其中所述硅膜是单晶硅。

48. 如权利要求 47 所述的方法，其中所述单晶硅膜是本征硅。

49. 如权利要求 43 所述的方法，还包括在所述栅极电极的横向相对的
25 侧壁的相对侧面上形成一对侧壁隔离层；以及

在所述硅主体之上及其周围，以及与所述侧壁隔离层相邻处形成硅膜。

50. 如权利要求 43 所述的方法，还包括在形成于所述硅主体上的所述硅膜上形成硅化物。

51. 如权利要求 43 所述的方法，其中所述硅膜是由选择性沉积工艺而形成的。

三栅极器件及其加工方法

5 技术领域

本发明涉及半导体集成电路制造领域，更具体地说，本发明涉及三栅极全耗尽型衬底晶体管及其加工方法。

背景技术

10 为了提高器件性能，绝缘体上硅（silicon on insulator, SOI）晶体管已被建议用来加工现代集成电路。图 1 示出了标准全耗尽型绝缘体上硅（SOI）晶体管 100。SOI 晶体管 100 包括单晶硅衬底 102，其具有绝缘层 104，例如其上形成的氧化埋层。在绝缘层 104 上形成单晶硅主体 106。在单晶硅主体 106 上形成栅极电介质层 108，并在栅极电介质层 108 上形成
15 栅极电极 110。在硅主体 106 中沿着栅极电极 110 的侧向相对的侧面形成源极 112 和漏极 114 区。

已建议将全耗尽型 SOI 作为晶体管结构，以利用优化的导通电流/截止电流比的理想亚阈值梯度。为了获得晶体管 100 的理想亚阈值梯度，硅主体 106 的厚度必须约是晶体管栅极长度（ L_g ）的尺寸的 $1/3$ ，即 $T_{si} =$
20 $L_g/3$ 。然而，随着栅极长度的变化，尤其是当它们接近 30nm 时，尽量降低硅膜厚度（ T_{si} ）的需求使得这一接近越来越不实际。对于 30 纳米的栅极长度，人们认为硅主体的所需厚度需要小于 10 纳米，而对于 20 纳米的栅极长度，该厚度需要是 6 纳米左右。厚度小于 10 纳米的薄硅膜的加工是极其困难的。一方面，在一个纳米的量级上获得晶片一致性是一项艰苦
25 的挑战。另一方面，能够接触这些薄硅膜以形成凸起的源极/漏极区从而降低结电阻变得几乎不可能，因为在栅极刻蚀以及栅极刻蚀和隔离层刻蚀之后的各种清洁工艺期间，源极/漏极区中的薄硅层被消耗掉了，从而剩下不足的硅 106 用于硅的生长。

诸如图 2A 和图 2B 中示出的双栅极（DG）器件已被建议用来缓和关

于硅厚度的问题。双栅极 (DG) 器件 200 包括形成在绝缘衬底 204 上的硅主体 202。在硅主体 202 的两侧上形成栅极电介质 206, 并在硅主体 202 的两侧上形成的栅极电介质 206 的相邻处形成栅极电极 208。足够厚的绝缘层 209 例如氮化硅使得栅极电极 208 与硅主体 202 的顶部之间电绝缘。

- 5 双栅极 (DG) 器件 200 基本上有 2 个栅极, 分别位于器件沟道的两侧。因为双栅极器件 200 在沟道两侧都有栅极, 所以硅主体的厚度 (Tsi) 可以是单栅极的两倍, 并且仍可以获得全耗尽型晶体管的操作。也就是说, 利用双栅极器件 200, 可以形成全耗尽型晶体管, 其中 $T_{si} = (2 \times L_g) / 3$ 。然而, 双栅极 (DG) 器件 200 最可制造的形式需要使用某种光刻
- 10 技术来完成硅主体 202 的图案化, 该光刻技术比用来图案化该器件的栅极长度 (L_g) 的光刻技术要小 0.7 倍。为了获得高密度集成电路, 一般希望将最激进的光刻法应用在栅极电极 208 的栅极长度 (L_g) 上。尽管双栅极结构使得硅膜的厚度加倍 (由于现在沟道的两侧都有栅极), 但是这些结构极难加工。例如, 硅主体 202 需要这样一种硅主体刻蚀, 其可产出纵横
- 15 比 (高宽比) 约为 5:1 的硅主体 202。

附图说明

- 图 1 是耗尽型衬底晶体管的截面图的示例。
- 图 2A 和图 2B 图示了双栅极耗尽型衬底晶体管。
- 20 图 3 是根据本发明实施例的三栅极晶体管的示例。
- 图 4A 是根据本发明实施例的三栅极晶体管的示例。
- 图 4B 是根据本发明实施例的三栅极晶体管的示例。
- 图 5A—5J 图示了加工根据本发明实施例的三栅极晶体管的方法。
- 图 6 是一张曲线图表, 图示了可用于获得具有 30nm 和 20nm 的栅极
- 25 长度 (L_g) 的部分耗尽型和全耗尽型晶体管的主体高度和主体宽度。

具体实施方式

本发明是一种新型三栅极晶体管结构及其加工方法。在下面的描述中, 给出了大量具体细节, 以提供对本发明的透彻的了解。在其他情况

下，没有以具体的细节来描述公知的半导体工艺和制造技术，以免不必要地混淆本发明。

本发明是一种新型三栅极晶体管结构及其加工方法。在本发明的实施例中，三栅极晶体管是绝缘体上硅（SOI）晶体管。将三栅极晶体管用于全耗尽型晶体管应用中是很理想的。三栅极晶体管包括在衬底上形成的薄半导体主体，该衬底可以是绝缘衬底或半导体衬底。在半导体主体的顶表面和侧壁上形成栅极电介质。在半导体主体顶表面上的栅极电介质上、以及在半导体主体侧壁上形成的栅极电介质相邻处形成栅极电极。在半导体主体中栅极电极的相对侧上形成源极和漏极区。因为栅极电极和栅极电介质包围在半导体主体的三个侧面上，因此晶体管本质上具有三个分离的沟道和栅极。晶体管的栅极“宽度”等于半导体主体三个侧面中的每一个侧面的总和。可以通过将几个三栅极晶体管连接在一起来形成更大“宽度”的晶体管。

因为在半导体主体中形成了三个分离的沟道，所以当晶体管被“导通”时半导体主体可以是完全耗尽的，从而使得可用小于 30 纳米的栅极长度来形成全耗尽型晶体管，而不需要使用超薄半导体主体或需要半导体主体的光刻图案的尺寸小于器件的栅极长度（ L_g ）。也就是说，在半导体主体的厚度以及半导体主体的宽度等于器件的栅极长度的情况下，本发明的三栅极晶体管的结构使得可加工出全耗尽型晶体管。因为本发明的新型三栅极晶体管可以按全耗尽的方式操作，所以器件具有下述特征：理想的（即非常陡峭的）亚阈值斜率；降低的漏场感应势垒降低（DIBL）短沟道效应，其小于 100mV/V，理想值约为 60mV/V，获得了器件“截止”时较小的漏电流，从而获得了较低的功耗。

图 3 中图示了根据本发明实施例的三栅极晶体管 300 的例子。三栅极晶体管 300 形成在衬底 302 上。在本发明的实施例中，衬底 302 是绝缘衬底，其包括较下面的单晶硅衬底 304，在此单晶硅衬底上形成绝缘层 306，例如二氧化硅膜。然而，三栅极晶体管 300 可在任意公知的绝缘衬底上形成，例如由二氧化硅、氮化物、氧化物和蓝宝石（sapphires）形成的衬底。在本发明的实施例中，衬底 302 可以是半导体衬底，例如但不局

限于单晶硅衬底和砷化镓衬底。

三栅极晶体管 300 包括形成在绝缘衬底 302 的绝缘体 306 上的半导体主体 308。半导体主体 308 可由任意公知的半导体材料形成，例如但不局限于硅 (Si)、锗 (Ge)、锗化硅 (Si_xGe_y)、砷化镓 (GaAs)、InSb、GaP、GaSb 和碳纳米管。半导体主体 308 可由任意这样的公知材料形成，该材料可以通过施加外部电控制而从绝缘状态可逆地改变成导电状态。当希望得到晶体管 300 的最佳电学性能时，半导体主体 308 理想地是单晶体膜。例如，当晶体管 300 用于高性能应用例如像微处理器之类的高密度电路中时，半导体主体 308 是单晶体膜。然而，当晶体管 300 用于需要较低性能的应用例如液晶显示器中时，半导体主体 308 可以是多晶体膜。绝缘体 306 将半导体主体 308 从单晶硅衬底 302 绝缘开来。在本发明的实施例中，半导体主体 308 是单晶硅膜。半导体主体 308 具有一对横向相对的侧壁 310 和 312，二者被一段界定了半导体主体宽度 314 的距离所分开。另外，半导体主体 308 具有与形成在衬底 302 上的底表面 318 相对的顶表面 316。顶表面 316 和底表面 318 之间的距离界定了主体高度 320。在本发明的实施例中，主体高度 320 与主体宽度 314 基本相等。在本发明的实施例中，主体 308 具有小于 30 纳米的宽度 314 和高度 320，理想情况下小于 20 纳米。在本发明的实施例中，主体高度 320 介于主体宽度 314 的 1/2 和主体宽度 314 的 2 倍之间。

三栅极晶体管 300 具有栅极电介质层 322。栅极电介质层 322 形成在半导体主体 308 的三个侧面上并包围这三个侧面，如图 3 所示。栅极电介质层 322 形成在主体 308 的侧壁 312 上或与之相邻、顶表面 316 上以及侧壁 310 上或与之相邻，如图 3 所示。栅极电介质层 322 可以是任意公知的栅极电介质层。在本发明的实施例中，栅极电介质层是二氧化硅 (SiO_2)、氮氧化硅 (SiO_xN_y) 或氮化硅 (Si_3N_4) 电介质层。在本发明的实施例中，栅极电介质层 322 是厚度形成在 5—20Å 之间的氮氧化硅膜。在本发明的实施例中，栅极电介质层 322 是高 K 栅极电介质层，例如金属氧化物电介质，例如但不局限于五氧化钽 (Ta_2O_5) 和二氧化钛 (TiO_2)。栅极电介质层 322 可以是其他类型的高 K 电介质，例如但不局限于 PZT。

三栅极器件 300 具有栅极电极 324。栅极电极 324 形成在栅极电介质层 322 上并包围栅极电介质层 322，如图 3 所示。栅极电极 324 形成在形成于半导体主体 308 的侧壁 312 上的栅极电介质 322 之上或与之相邻、形成于半导体主体 308 的顶表面 316 上的栅极电介质 322 之上以及形成于半导体主体 308 的侧壁 310 上的栅极电介质层 322 之上或与之相邻。栅极电极 324 具有一对横向相对的侧壁 326 和 328，二者被一段界定了晶体管 300 的栅极长度 (L_g) 330 的距离所分开。在本发明的实施例中，栅极电极 324 的横向相对的侧壁 326 和 328 与半导体主体 308 的横向相对的侧壁 310 和 312 垂直。

栅极电极 324 可以由任意合适的栅极电极材料形成。在本发明的实施例中，栅极电极 324 由掺杂到浓度为 1×10^{19} 原子数/ cm^3 — 1×10^{20} 原子数/ cm^3 之间的多晶硅构成。在本发明的实施例中，栅极电极可以是金属栅极电极，例如但不限于钨、钼、钛及其氮化物。在本发明的实施例中，栅极电极由具有在 4.6—4.8eV 之间的中间带隙 (mid-gap) 功函数的材料而形成。应该认识到，栅极电极 324 不一定需要是单种材料，而可以是多个薄膜的复合叠层，例如但不限于多晶硅/金属电极或金属/多晶硅电极。

三栅极晶体管 300 具有源极区 330 和漏极区 332。源极区 330 和漏极区 332 形成在半导体主体 308 中栅极电极 324 的相对两侧，如图 3 所示。源极区 330 和漏极区 332 由相同的导电性类型形成，例如 N 型或 P 型导电性。在本发明的实施例中，源极区 330 和漏极区 332 具有 1×10^{19} 和 1×10^{20} 原子数/ cm^3 之间的掺杂浓度。源极区 330 和漏极区 332 可以形成为具有均匀的浓度，或者可以包括具有不同浓度或掺杂特性的子区域，例如尖端区域 (tip region) (例如源极/漏极延伸)。在本发明的实施例中，当晶体管 300 是对称晶体管时，源极区 330 和漏极区 332 将具有相同的掺杂浓度和特性。在本发明的实施例中，当三栅极晶体管 300 形成为非对称晶体管时，源极区 330 和漏极区 332 的掺杂浓度和特性可以不同，以获得特定的电学特性。

半导体主体 308 位于源极区 330 和漏极区 332 之间的部分界定了晶体管 300 的沟道区 350。沟道区 350 也可以定义为半导体主体 308 被栅极电

极 324 所包围的区域。然而，源极/漏极区有时候可以通过例如扩散而稍微延伸到栅极电极的下面，以定义稍小于栅极电极长度 (L_g) 的沟道区。在本发明的一个实施例中，沟道区 350 是本征的或未掺杂的单晶硅。在本发明的一个实施例中，沟道区 350 是掺杂的单晶硅。当沟道区 350 掺杂时，
5 它一般掺杂到 1×10^{16} 和 1×10^{19} 原子数/ cm^3 之间的导电性水平。在本发明的实施例中，当沟道区掺杂时，它一般掺杂成与源极区 330 和漏极区 332 相反的导电性类型。例如，当源极和漏极区是 N 型导电性时，沟道区就被掺杂成 P 型导电性。类似地，当源极和漏极区是 P 型导电性时，沟道区就是 N 型导电性。以这种方式，三栅极晶体管 300 可以分别被形成为 NMOS
10 晶体管或 PMOS 晶体管。沟道区 350 可以被均匀地掺杂，或者可以非均匀地或以不同浓度掺杂，以提供特定的电学和性能特性。例如，如果希望的话，沟道区 350 可以包括公知的 “halo” 区。

通过提供在三个侧面上包围半导体主体的栅极电介质和栅极电极，三栅极晶体管就具有了包括三个沟道和三个栅极的特性，其中一个 (g_1) 延伸在硅主体 308 的侧面 312 上的源极和漏极区之间，第二个 (g_2) 延伸在
15 硅主体 308 的顶表面 316 上的源极和漏极区之间，而第三个 (g_3) 延伸在硅主体 308 的侧壁 310 上的源极和漏极区之间。晶体管 300 的栅极 “宽度” (G_w) 是这三个沟道区的宽度的总和。也就是说，晶体管 300 的栅极宽度等于硅主体 308 在侧壁 310 处的高度，加上硅主体 308 在顶表面 316
20 处的宽度，再加上硅主体 308 在侧壁 312 处的高度。通过使用耦合在一起的多个器件 (例如，单个栅极电极 324 所包围的多个硅主体 308)，可以获得更大 “宽度” 的晶体管。

因为沟道区 350 在三个侧面上被栅极电极 324 和栅极电介质 322 所包围，所以晶体管 300 可以按全耗尽方式而操作，其中，当晶体管 300 “导
25 通” 时，沟道区 350 是全耗尽的，从而提供了全耗尽型晶体管的有利的电学特性和性能。也就是说，当晶体管 300 “导通” 时，在沟道区 350 处形成了耗尽区，并在区 350 的表面处形成反转层 (即，在半导体主体的侧表面和顶表面形成反转层)。所述反转层具有和源极与漏极区相同的导电性类型，并在源极和漏极区之间形成导电沟道，以使得电流可在二者之间流

动。本发明的三栅极晶体管可以说是一种非平面的晶体管，因为在半导体主体 308 的水平和垂直方向上都形成了沟道区。耗尽区将来自反转层下面的自由载波耗尽。耗尽区延伸到沟道区 350 的底部，因此该晶体管可以说是“全耗尽型”晶体管。全耗尽型晶体管与非全耗尽型或部分耗尽型晶体管相比具有改进的电学性能特性。例如，通过按全耗尽方式来操作晶体管 300，可以使得晶体管 300 具有理想的或非常陡峭的亚阈值斜率。三栅极晶体管可以被加工成具有非常陡峭的小于 80mV/decade 的亚阈值斜率，理想情况下约是 60mV/decade，即使该晶体管是用厚度小于 30nm 的半导体主体加工而成的。另外，以全耗尽方式操作晶体管 300 时，晶体管 300 具有改进的漏场感应势垒降低（DIBL）效应，其提供了更好的“截止”状态漏电流，导致了更小漏电流，从而降低了功耗。在本发明的实施例中，三栅极晶体管 300 具有小于 100mV/V 的 DIBL 效应，理想状况下小于 40mV/V。

图 6 图示了两张曲线图表，给出可产出栅极长度分别为 30nm（602）和 20nm（604）的全耗尽（F.D）或部分耗尽（P.D）三栅极晶体管的主体高度和主体宽度。在本发明的实施例中，选择具有这样尺寸的主体高度、主体宽度和栅极长度，即在这些尺寸中可以形成全耗尽型晶体管。在其他实施例中，三栅极晶体管具有使得可形成部分耗尽型晶体管的主体高度、主体宽度和栅极长度。

在本发明的实施例中，三栅极晶体管 300 的源极和漏极区可包括形成在半导体主体 308 之上及其周围的硅或其他半导体膜，如图 4A 所示。例如，半导体膜 410 可以是硅膜或诸如锗化硅（ Si_xGe_y ）的硅合金。在本发明的实施例中，半导体膜 410 是形成有与源极区 330 和漏极区 332 相同的导电性类型的单晶硅膜。在本发明的实施例中，该半导体膜可以是硅合金例如锗化硅，其中硅构成该合金约 1 到 99 的原子百分比。半导体膜 410 不一定需要是单晶体半导体膜，并且在一个实施例中，可以是多晶体膜。在本发明的实施例中，半导体膜 410 形成在半导体主体 308 的源极区 330 和漏极区 332 上，以形成“凸起”的源极和漏极区。半导体膜 410 可以通过一对电介质侧壁隔离层 420 例如氮化硅或二氧化硅或其组合物而与栅极电

极 324 电绝缘。侧壁隔离层 420 沿着栅极电极 324 的横向相对的侧壁 326 和 328 延伸,如图 4A 所示,从而将半导体膜 410 与栅极电极 324 电绝缘,如图 4A 所示。在本发明的实施例中,侧壁隔离层 420 具有 20—200Å 之间的厚度。通过向半导体主体的源极和漏极区 330 和 332 添加硅或半导
5 体膜并形成“凸起”的源极和漏极区,提高了源极和漏极区的厚度,从而减少了源极/漏极到晶体管 300 的接触电阻,并改进了其电学特性和性能。

在本发明的实施例中,在源极区 330 和漏极区 332 上形成硅化物膜 430,例如但不局限于硅化钛、硅化镍和硅化钴。在本发明的实施例中,在硅主体 308 的硅膜 410 上形成硅化物膜 430,如图 4A 所示。然而,也可
10 将硅化物膜 430 直接形成到硅主体 308 的顶表面 316 上。例如,通过先形成诸如未掺杂硅膜的硅膜和硅主体,然后在硅化工艺中完全消耗该硅膜,可以在硅主体 308 上形成硅化物膜 430。电介质隔离层 420 使得可在一个自对齐工艺(即硅化工艺)中在半导体主体 308 或硅膜 410 上形成硅化物膜 430。

15 另外,在本发明的所述实施例中,也可在栅极电极 324 的顶部上形成半导体或硅膜 440,如在栅极电极 325 的顶表面上形成硅化物膜 450 一样。硅化物膜 450 和硅膜 440 一般与在硅主体 308 上形成硅化物膜 430 和硅膜 410 的相同时间形成。在栅极电极上的硅化物膜 450 上形成硅膜 440 减小了到栅极的接触电阻,从而改进了晶体管 300 的电学性能。

20 如上所述,晶体管 300 的栅极“宽度”等于从晶体管 300 的半导体主体 308 创建的三个栅极宽度的总和。为了加工出具有更大栅极宽度的晶体管,晶体管 300 可以包括额外的或多个半导体主体或者指形(finger) 308,如图 4B 所示。每个半导体主体 308 具有形成在其顶表面和侧壁上的栅极电介质层 322,如图 4B 所示。栅极电极 324 形成在所述多个半导体主
25 体 308 中的每一个的每个栅极电介质 322 上或与其相邻。每个半导体主体 308 还包括源极区 330 和漏极区 332,二者形成在半导体主体 308 中与栅极电极 324 相对的侧面上,如图 4B 所示。在本发明的实施例中,每个半导体主体 308 形成为具有与其他半导体主体 308 相同的宽度和高度(厚度)。在本发明的实施例中,所述多个半导体主体 308 的每个源极区 330

和漏极区 332 被用来形成半导体主体 308 的半导体材料电耦合在一起，以形成源极附着块 460 和漏极附着块 480，如图 4B 所示。或者，可以通过用于将各种晶体管 300 电互连成功能电路的高级别敷金属（metalization）处理（例如金属 1、金属 2、金属 3……）而将多个源极 330 和多个漏极 332 耦合在一起。图 4B 所示的晶体管 300 的栅极宽度等于所述多个半导体主体 308 中的每一个所创建的栅极宽度的总和。按这种方式，可形成具有任意所需栅极宽度的三栅极晶体管 300。

图 5A—5J 中图示了根据本发明实施例的三栅极晶体管的加工方法。三栅极晶体管的加工开始于衬底 502。在衬底 502 上形成硅或半导体膜 508，如图 5A 所示。在本发明的实施例中，衬底 502 是绝缘衬底，如在图 5A 中所示。在本发明的实施例中，绝缘衬底 502 包括较下层的单晶硅衬底 504 和顶部绝缘层 506，例如二氧化硅膜或氮化硅膜。绝缘层 506 将半导体膜 508 与衬底 504 绝缘开来，在实施例中形成为厚度在 200—2000Å 之间。有时将绝缘层 506 称为“氧化埋”层。当在绝缘衬底 502 上形成硅或半导体膜 508 时，也就创建了绝缘体上硅或半导体（SOI）衬底 500。在本发明的其他实施例中，衬底 502 可以是半导体衬底，例如但不限于硅单晶体衬底和砷化镓衬底。

尽管理想情况下半导体膜 508 是硅膜，单在其他实施例中，它可以是其他类型的半导体膜，例如但不限于锗（Ge）、硅锗合金（ Si_xGe_y ）、砷化镓（GaAs）、InSb、GaP、GaSb 以及碳纳米管。在本发明的实施例中，半导体膜 508 是本征（即未掺杂）硅膜。在其他实施例中，半导体膜 508 掺杂成 P 型或 N 型导电性，具有在 $1 \times 10^{16} - 1 \times 10^{19}$ 原子数/ cm^3 之间的浓度水平。通过例如离子注入，半导体膜 508 可以被即时（insitu）掺杂（即在沉积时掺杂），或当其在衬底 502 上形成后来掺杂。形成后掺杂使得可在相同绝缘衬底上同时加工出 PMOS 和 NMOS 三栅极器件。此时半导体主体的掺杂水平确定了器件的沟道区的掺杂水平。

半导体膜 508 被形成为具有这样一个厚度，其约等于随后形成的所加工三栅极晶体管的半导体主体或多个主体的所期望的高度。在本发明的实施例中，半导体膜 508 具有小于 30 纳米的厚度或者高度 509，理想情况下

小于 20 纳米。在本发明的实施例中，半导体膜 508 被形成为具有约等于所加工出的三栅极晶体管所期望的栅极“长度”的厚度。在本发明的实施例中，半导体膜 508 被形成为比器件所期望的栅极长度要厚。在本发明的实施例中，半导体膜 508 被形成为具有这样一个厚度，其使得所加工出的
5 三栅极晶体管对于其设计栅极长度 (L_g) 可以按全耗尽方式操作。

可以按任何公知方法来在绝缘衬底 502 上形成半导体膜 508。在一种称为 SIMOX 技术的形成绝缘体上硅衬底的方法中，将高剂量的氧原子注入到单晶硅衬底中，然后退火，以在衬底内形成氧化埋层 506。单晶硅衬底在氧化埋层上的部分成为硅膜 508。另一种当前用来形成 SOI 衬底的技术是外延硅膜转移 (epitaxial silicon film transfer) 技术，一般称为粘结
10 SOI (bonded SOI)。在此技术中，第一硅晶片具有在其表面上生长的薄层氧化物，该氧化物后面将用作 SOI 结构中的氧化埋层 506。然后，向第一硅晶片注入高剂量的氢，以在第一晶片的硅表面下形成高压区。然后将此第一晶片翻转并粘结到第二硅晶片的表面。然后沿着由氢注入而产生的
15 的高压平面将第一晶片劈开。这样就得到了一种 SOI 结构，在顶部具有薄硅层，其下是在单晶硅衬底的顶部上的氧化埋层。可以使用多种公知平滑技术例如 HC 平滑或化学机械抛光 (CMP) 来平滑半导体膜 508 的顶表面，直至得到所希望的厚度。

此时，如果希望的话，可以在 SOI 衬底 500 中形成绝缘区（未示出），以将其中要形成的各晶体管彼此绝缘。通过使用例如公知的光刻和刻蚀技术来将衬底 508 包围三栅极晶体管的部分刻蚀掉，然后用绝缘膜例如 SiO_2 来回填所刻蚀的区域，可形成绝缘区。
20

为了在衬底 500 上形成三栅极晶体管，在半导体膜 508 上形成光阻掩膜 510，如图 5B 所示。光阻掩膜 510 包含一个图案或多个图案 512，所述
25 图案界定了随后在半导体膜 508 中形成半导体主体或者鳍状部分的位置。光阻图案 512 界定了随后形成的三栅极晶体管的半导体主体或者鳍状部分的所希望的宽度 518。在本发明的实施例中，图案 512 界定了具有宽度 518 的鳍状部分或者主体，其中宽度 518 等于或大于所加工出的晶体管的栅极长度 (L_g) 的所希望的宽度。以这种方式，将用于加工晶体管的最严

格的光刻约束与栅极电极图案相关联，而不是半导体主体或者鳍状部分定义。在本发明的实施例中，半导体主体或者鳍状部分将具有小于或等于 30 纳米的宽度 518，理想情况下小于或等于 20 纳米。在本发明的实施例中，用于半导体主体或者鳍状部分的图案 512 具有约等于硅主体高度 509 的宽度 518。在本发明的实施例中，光阻图案 512 具有在半导体主体高度 509 的 1/2 和半导体主体高度 509 的两倍之间的宽度 518。

另外，如图 5B 所示，光阻掩膜 510 还可包括图案 514 和 516，用于定义分别形成源极附着块和漏极附着块的位置。所述附着块可以用来将加工出的晶体管的各源极区连接到一起，并将各漏极区连接到一起。通过包括对覆盖沉积光阻膜进行掩膜设置、曝光及显影在内的公知光刻技术，可形成光阻掩膜 510。

在形成光阻掩膜 510 之后，与光阻掩膜 510 对齐地刻蚀半导体膜 508，以形成一个或多个硅主体或者鳍状部分，以及源极和漏极附着块（如果希望的话），如图 5C 所示。刻蚀半导体膜 508，直到暴露出下面的氧化埋层 506。可以使用公知的半导体刻蚀技术例如各向异性等离子刻蚀或活性离子刻蚀来与掩膜 510 对齐地刻蚀半导体膜 508，如图 5C 所示。

在刻蚀半导体膜 508 以形成半导体主体或者鳍状部分 520（以及源极/漏极附着块 522 和 524，如果希望的话）之后，通过公知技术例如通过化学剥离和 O_2 除灰来去除光阻掩膜以产出图 5D 所示的衬底。

然后，在每个半导体主体 520 上及其周围形成栅极电介质层 526。也就是说，在每个半导体主体 520 的顶表面 527 上，以及在每个半导体主体 520 的横向相对的侧壁 528 和 529 上形成栅极电介质层 526。该栅极电介质可以是沉积的电介质或生长的电介质。在本发明的实施例中，栅极电介质层 526 是用干/湿氧化工艺生长的二氧化硅电介质膜。在本发明的实施例中，该二氧化硅膜生长到厚度在 5—15Å 之间。在本发明的实施例中，栅极电介质膜 526 是沉积的电介质，例如但不局限于介电常数较高的膜，例如金属氧化物电介质，例如五氧化钽（ Ta_2O_5 ）和氧化钛（ TiO_2 ）以及其他高 K 电介质，例如 PZT 和 BST。可以通过任意公知的技术例如化学气相沉积（CVD）来形成介电常数较高的膜。

然后,如图 5E 所示,形成栅极电极 530。栅极电极 530 形成在形成于每个半导体主体 520 的顶表面 527 上的栅极电介质层 526 之上,以及形成在形成于每个半导体主体的侧壁 528 和 529 之上或与之相邻的栅极电介质 526 之上或与之相邻,如图 5E 所示。栅极电极 530 具有与其形成在绝缘衬底 502 之上的底表面相对的顶表面 532,并具有一对横向相对的侧壁 534 和 536。横向相对的侧壁 534 和 536 之间的距离界定了三栅极晶体管的栅极长度 (L_g) 538。栅极电极 530 可以通过在图 5D 所示的衬底上覆盖沉积合适的栅极电极材料而形成。栅极电极可以形成为具有在 200—3000Å 之间的厚度。在实施例中,栅极电极具有至少 3 倍于半导体主体 520 的高度 509 的厚度或者高度 533。然后可用公知的光刻或刻蚀技术对栅极电极材料进行图案化,以从栅极电极材料形成栅极电极 530。在本发明的实施例中,栅极电极材料包括多晶硅。在本发明的另一个实施例中,栅极电极材料包括多晶体锗化硅合金。在本发明的另一个实施例中,栅极电极材料可以包括金属膜,例如钨、钽及其氮化物。栅极电极 530 可以通过公知的技术而形成,例如在图 5D 的衬底上覆盖沉积栅极电极材料,然后用公知的光刻或刻蚀技术对栅极电极材料进行图案化。在本发明的另一实施例中,用于定义栅极电极 530 的光刻工艺利用了用于加工三栅极晶体管的最低限度或者最小尺寸的光刻工艺。(也就是说,在本发明的实施例中,栅极电极 530 的栅极长度 (L_g) 538 具有由光刻定义的晶体管最小特征尺寸。)在本发明的实施例中,栅极长度 538 小于或等于 30 纳米,理想情况下小于或等于 20 纳米。

然后,在半导体主体 520 中相对于栅极电极 530 的侧面上形成晶体管的源极和漏极区。在本发明的实施例中,源极和漏极区包括尖端或者源/漏区延伸区。可以通过下述方式分别形成源极和漏极延伸区 540 和 542,即将掺杂剂 544 放置于半导体主体 520 中栅极电极 530 的两个侧面 532 和 534 中,以形成尖端区 540 和 542,如图 5F 所示。在图 5F—5J 中没有示出源极和漏极附着块 522 和 524,以更好地图示本发明的各方面。如果利用了源极和漏极附着块 522 和 524,它们也可以在此时进行掺杂。对 PMOS 三栅极晶体管来说,半导体鳍状部分或者主体 520 被掺杂成 P 型导电性,

并具有 $1 \times 10^{20} - 1 \times 10^{21}$ 原子数/cm³ 的浓度。对 NMOS 三栅极晶体管来说，半导体鳍状部分或者主体 520 以 n 型导电性离子而被掺杂成具有 $1 \times 10^{20} - 1 \times 10^{21}$ 原子数/cm³ 的浓度。在本发明的实施例中，用离子注入来对硅膜进行掺杂。在本发明的实施例中，在垂直方向（即与衬底 500 垂直的方向）上进行离子注入，如图 5F 所示。当栅极电极 530 是多晶硅栅极电极时，可以在离子注入工艺期间对它进行掺杂。栅极电极 530 用作掩膜，以防止离子注入步骤对三栅极晶体管的（多个）沟道区 548 产生掺杂。沟道区 548 是硅主体 520 位于栅极电极 530 下面或被其所包围的部分。如果栅极电极 530 是金属电极，则可以使用电介质硬掩膜来阻塞离子注入工艺期间的掺杂。在其他实施例中，可以使用其他方法例如固态源扩散来对半导体主体进行掺杂以形成源极和漏极延伸。

在本发明的多个实施例中，在形成源/漏区或源极/漏极延伸区之前，可在硅主体中形成“halo”区。Halo 区是在器件的沟道区 548 中形成的掺杂区，具有与器件道沟区相同的导电性，但具有稍高于器件沟道区的掺杂浓度。利用成较大角度的离子注入技术，通过在栅极电极下离子注入掺杂剂，可形成 halo 区。

然后，如果希望的话，可以进一步处理图 5F 中的衬底，以形成额外特征，例如重掺杂的源极/漏极接触区、源极和漏极区以及栅极电极上的沉积硅，以及在源极/漏极接触区和栅极电极上形成硅化物。

在本发明的多个实施例中，电介质侧壁隔离层 550 可以形成在栅极电极的侧壁上。可以利用侧壁隔离层来补偿重源极/漏极接触注入，在选择性硅沉积工艺中将源极/漏极区与栅极电极绝缘开来，以及在硅化工艺中在源极和漏极区以及栅极电极上形成硅化物。可以通过在图 5F 的衬底 500 上覆盖沉积适形的（conformal）电介质膜 550 来形成隔离层，所述电介质膜例如是但不局限于氮化硅、氧化硅、氮氧化硅或其组合物。以适形的方式沉积电介质膜，以使得它在垂直表面以及水平表面上形成为具有大致相等的高度，所示垂直表面例如是栅极电极 530 的侧壁 534 和 536，而所述水平表面例如是硅膜 520 的顶部 526 和栅极电极 530 的顶部。在本发明的实施例中，所述电介质膜是由热壁低压化学气相沉积（LPCVD）工艺形成的

氮化硅膜。电介质膜的沉积厚度确定了所形成的隔离层的宽度或者厚度。在本发明的实施例中，所示电介质膜形成为具有 20—200Å 之间的厚度。

然后，如图 5G 所示，通过例如等离子刻蚀或活性离子刻蚀来对电介质膜进行各向异性刻蚀，以形成侧壁隔离层 550。电介质膜的各向异性刻蚀从水平表面例如栅极电极 530 的顶部（以及附着块 522 和 524 的顶部，如果使用了的话）上去除电介质膜，而留下了与垂直表面例如栅极电极 530 的侧壁 534 和 536 相邻的电介质侧壁隔离层。所述刻蚀持续了一段充分长的时间，以从所有水平表面上去除电介质膜。在本发明的实施例中，利用了过度刻蚀，以使得可去除半导体主体 520 的侧壁上的隔离层材料，
5 如图 5G 所示。结果就形成了侧壁隔离层 550，其沿着栅极电极 530 的侧壁 532 和 534 而延伸并与之相邻，如图 5H 所示。

然后，如果希望的话，可以在半导体主体 520 的暴露表面上（以及在附着块 522 和 524 上）形成半导体膜 560，如图 5H 所示。另外，如果希望的话，可以在栅极电极 530 的顶部上形成半导体膜 562。所述半导体膜可以
15 是单晶体膜或多晶体膜。在本发明的实施例中，半导体膜 560 是外延（单晶体）硅膜。在本发明的实施例中，硅膜 560 是由选择性沉积工艺形成的，从而使得只在含有硅的暴露区域上形成硅，例如硅主体 520 的顶表面 527 以及侧壁 528 和 529。在选择性沉积工艺中，不在电介质区域例如侧壁隔离层 555 上形成硅膜。当栅极电极 530 包括多晶硅膜时，也可在栅极电极 530 的顶表面上选择性地形成硅膜，以形成硅膜 562。在本发明的
20 实施例中，硅膜 560 形成为具有在 50—500Å 之间的厚度。在本发明的实施例中，硅膜形成为具有这样的厚度，即该厚度足以提供足够的硅，以在源极和漏极区上形成硅膜期间被使用或消耗。所述硅膜可以是即时掺杂（即在沉积期间掺杂）或随后掺杂的，通过例如离子注入或固态源扩散。
25 硅膜被掺杂成器件的源极和漏极区所希望的导电性类型。在本发明的实施例中，沉积硅膜 560 和 562 是本征硅膜（即未掺杂硅膜）。半导体膜 560 的沉积形成了凸起的源极和漏极区，提高了器件的寄生效应。

在本发明的实施例中，如图 5I 所示，通过利用垂直离子注入角度的离子注入来对沉积硅膜 560 和 562 进行掺杂。离子注入工艺将沉积硅膜 560

和位于下面的硅主体 520 掺杂成具有在 $1 \times 10^{20} - 1 \times 10^{21}$ 原子数/cm³ 的浓度，以形成源极接触区 570 和漏极接触区 572。侧壁隔离层 550 补偿源极/漏极接触注入步骤，并将已掺杂的硅主体在侧壁隔离层 550 下的区域定义为所述尖端区域。上述工艺形成了源极区 570 和漏极区 572，二者都包括尖端区和接触区。尖端区是硅主体 520 位于侧壁隔离层 550 下面的区域。接触区是硅主体和沉积硅膜与侧壁隔离层 550 的外部边缘相邻的区域。另外，如果利用了源极和漏极附着块 522 和 524 的话，源极/漏极接触区包括源极和漏极附着块 522 和 524。

然后，如果希望的话，可以在源极和漏极接触区以及栅极电极 530 的顶表面（或硅膜 562）上形成耐火金属硅化物 580，如图 5J 所示。可用自对齐工艺例如硅化工艺来形成耐火金属硅化物膜 580。在硅化工艺中，在图 5J 的衬底上覆盖沉积耐火金属膜，例如钛、钨、镍、钴等等。然后将衬底加热到合适的温度，以使得耐火金属膜与衬底 500 的硅部分反应，以形成耐火金属硅化物，所述硅部分例如是形成在硅主体上的硅膜 560 和形成在栅极电极上的硅膜 562。没有硅可发生反应的位置例如电介质隔离层 555 和氧化埋层 506 的暴露部分不发生反应，仍然是耐火金属。然后可用选择性刻蚀例如湿刻蚀来去除未反应的耐火金属，而保留接触区上的耐火金属硅化物。按这种方式，金属硅化物膜可与三栅极晶体管的接触区自对齐。这就根据本发明完成了三栅极晶体管的加工。

至此，已描述了三栅极晶体管及加工方法。

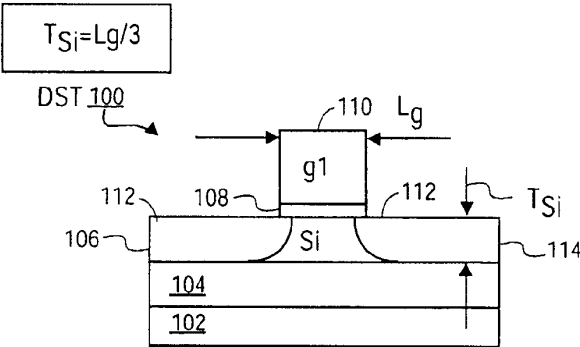


图1

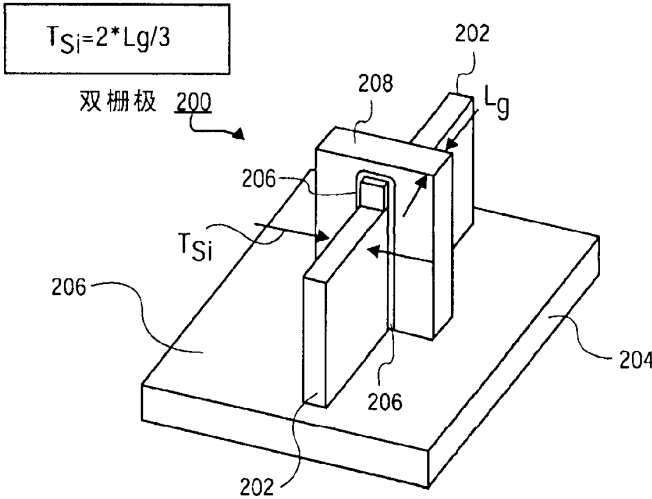


图2A

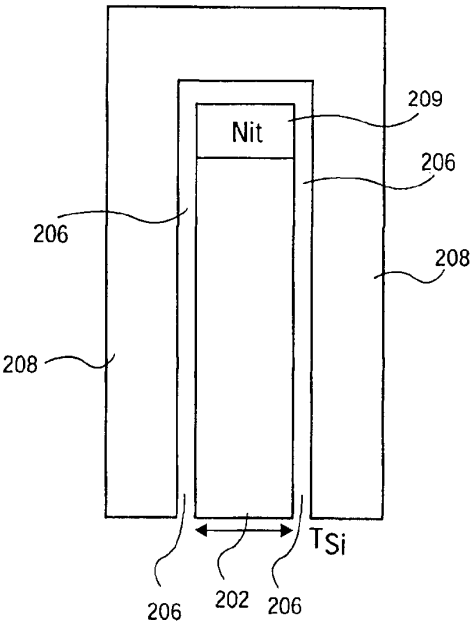


图2B

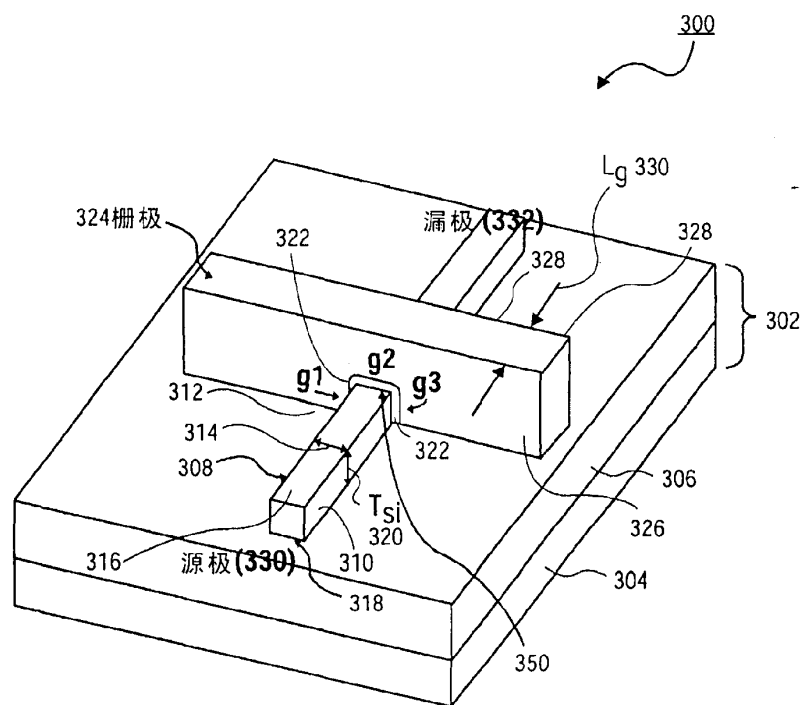


图3

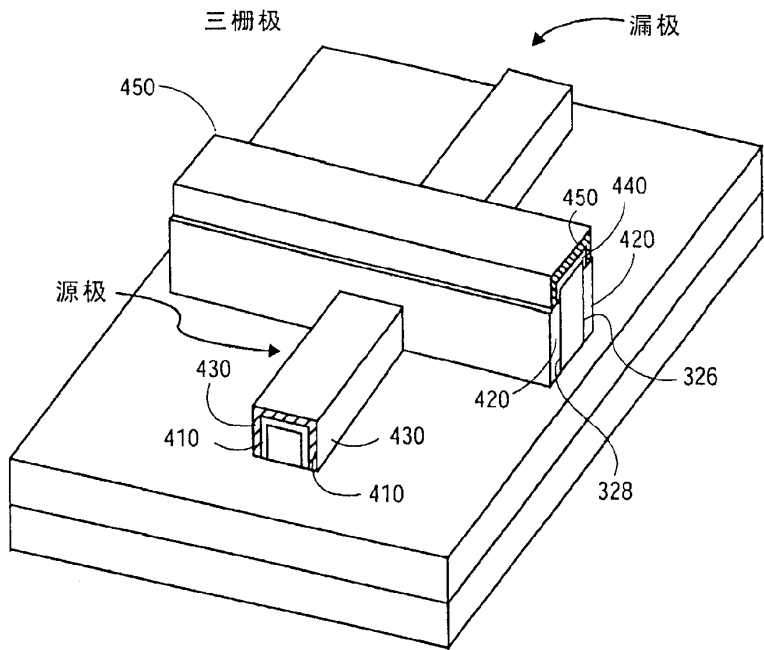


图4A

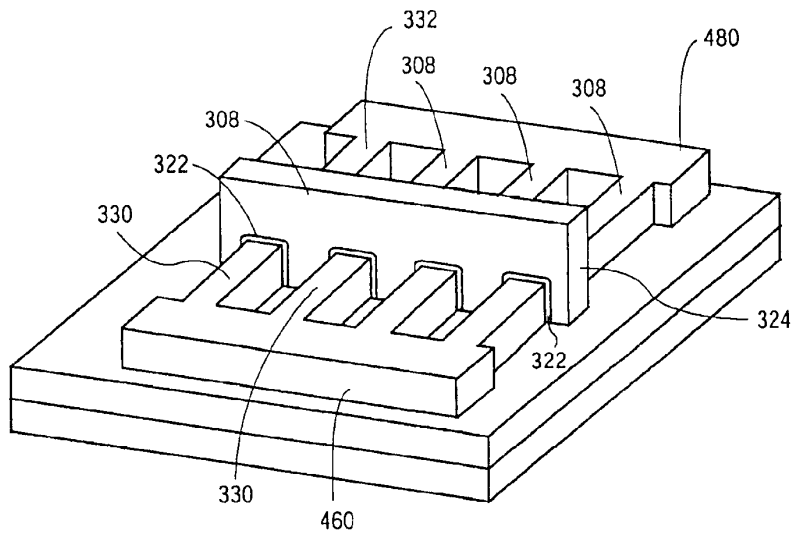


图4B

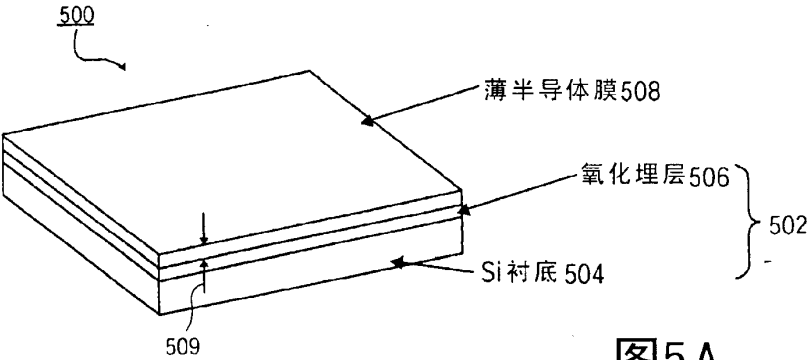


图5A

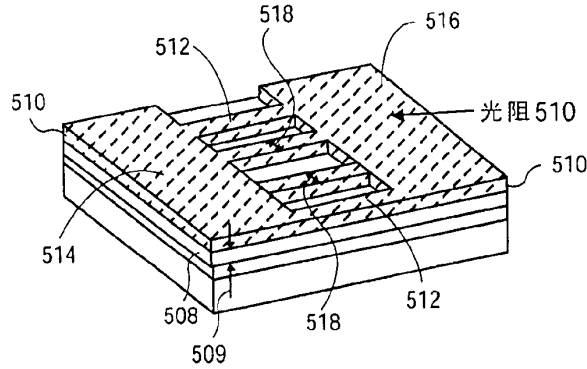


图5B

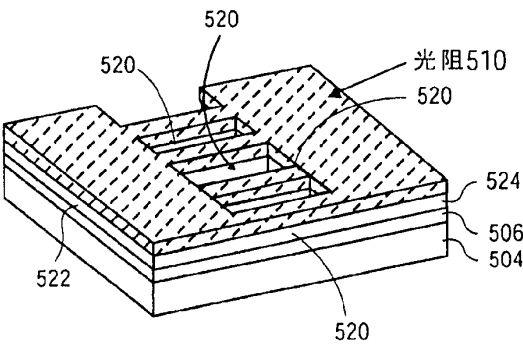


图5C

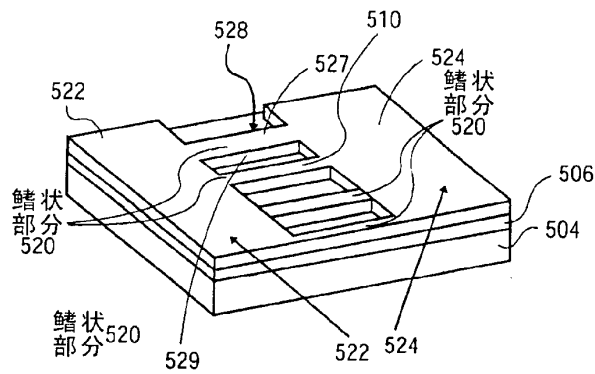


图5D

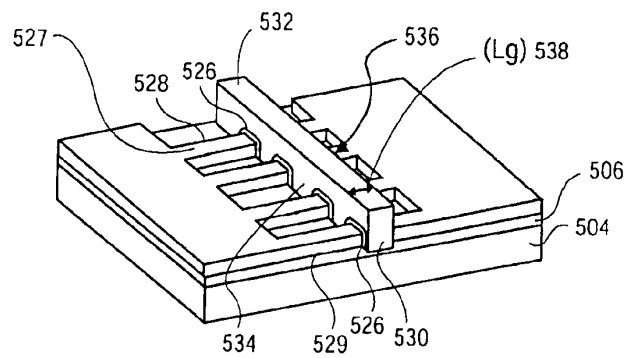


图5E

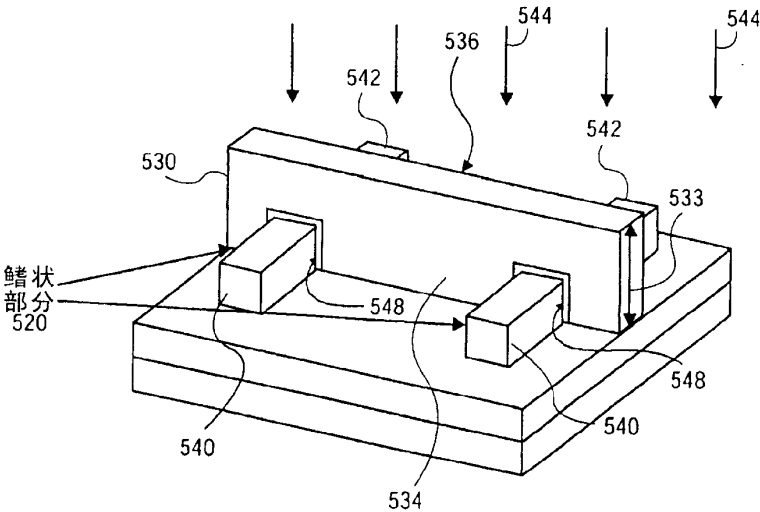


图5F

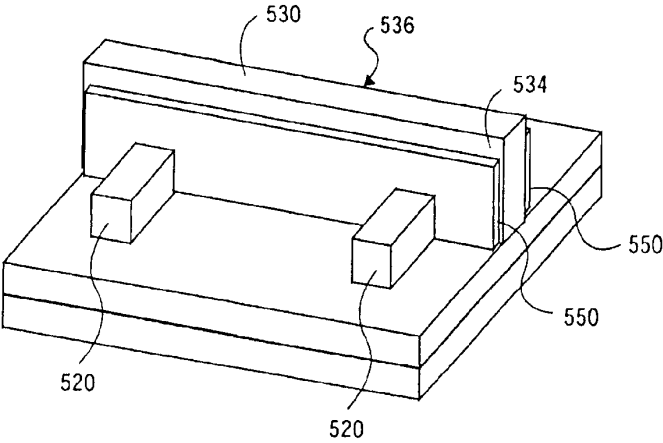


图5G

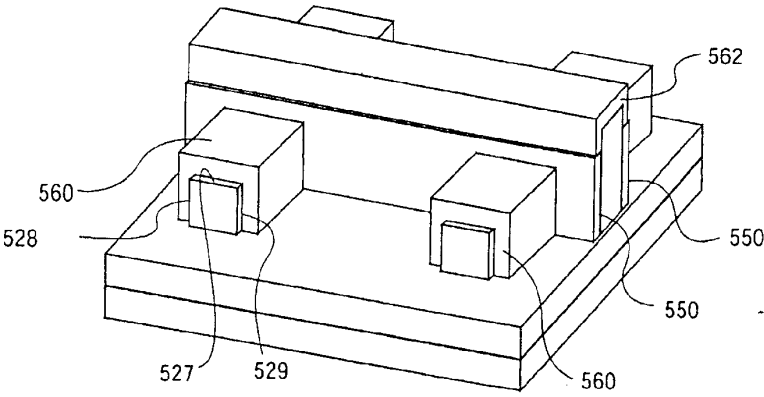


图5H

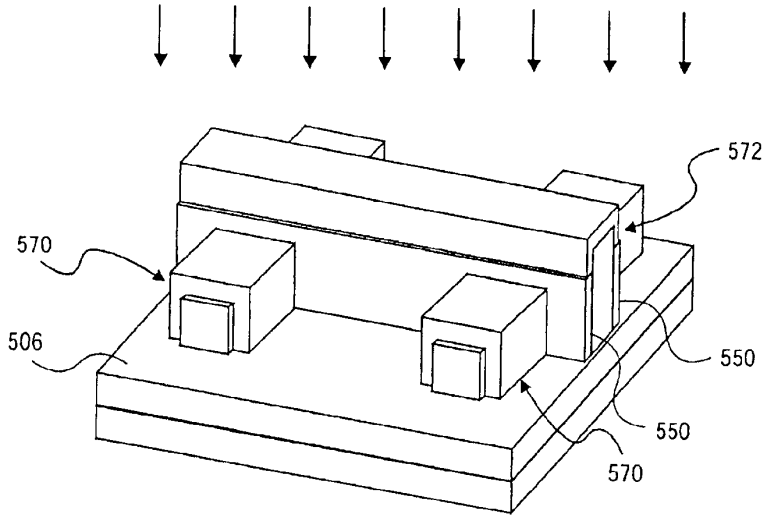


图5I

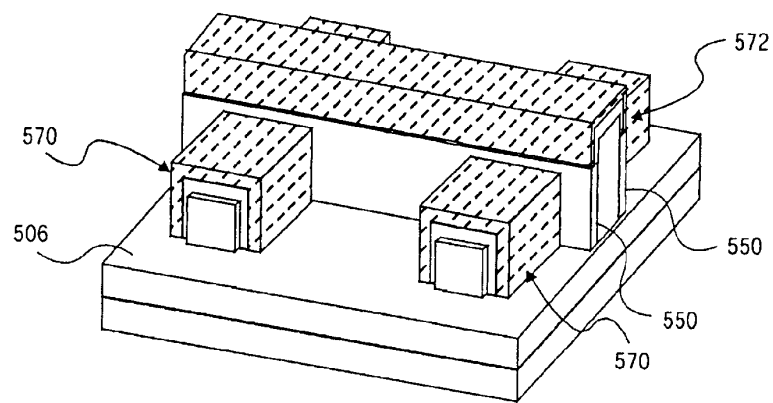


图5J

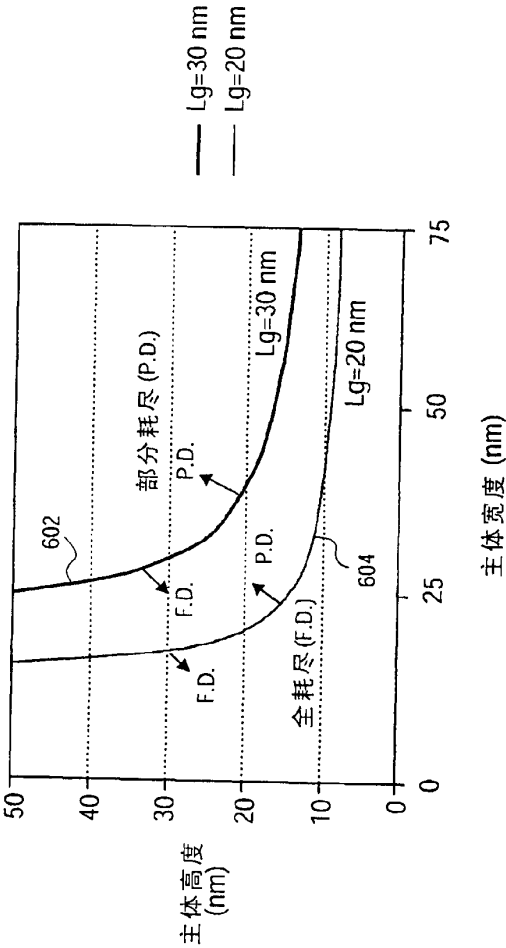


图6



Espacenet

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MULTIGATE DEVICE WITH RECESSED STRAIN REGIONS

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H01L29/66795 (EP, KR); H01L29/7848 (EP, KR);
H01L29/785 (EP, KR); H01L29/78696 (GB);
H01L29/165 (EP)

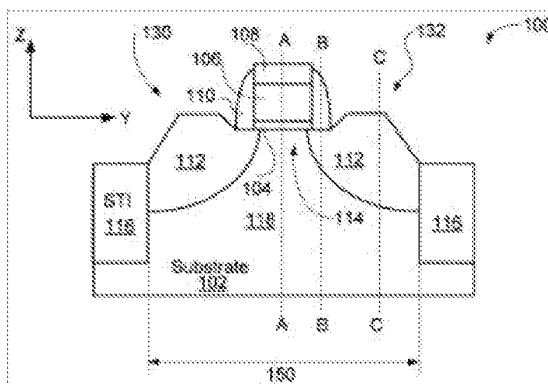
Application KR20087015867 20080627 Global Dossier
number:

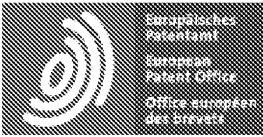
Priority number(s): US20050320309 20051227

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[DE112006003550 \(T5\)](#) [GB2444681 \(A\)](#) [more](#)

Abstract of KR20080075009 (A)

Embodiments of the invention provide a device with a multiple gates. Stress material within recesses of a device body metal gate may cause a stress in channel regions of the device, thereby improving performance of the device.





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DESCRIPTION KR20080075009A

MULTIGATE DEVICE WITH RECESSED STRAIN REGIONS

[1]

Performance enhancement of on-board circuit devices (eg, integrated circuit (IC) transistors, resistors, capacitors, etc. on semiconductor substrates) is generally considered a major factor during the design, manufacture, and operation of such devices. For example, during the design and manufacture or formation of a metal oxide semiconductor (MOS) transistor semiconductor device, such as used in complementary metal oxide semiconductor (CMOS), an N-type MOS device (NMOS) it is sometimes desirable to increase the mobility of negatively charged electrons in the channel, and also to increase the mobility of positively charged holes in a P-type MOS device (PMOS) channel.

[2]

1A to 1E are cross-sectional views illustrating a semiconductor device according to an embodiment of the present invention.

[3]

2 is a cross-sectional side view showing a substrate on which this device may be formed.

[4]

3 is a side cross-sectional view showing the substrate after STI regions are formed therein.

[5]

4 is a cross-sectional side view of the device after portions of the STI regions have been removed to form a fin.

[6]

5 is a perspective view showing a fin after fin formation.

[7]

6 is a cross-sectional side view illustrating a layer of gate dielectric material formed on surfaces of the body and STI regions.

[8]

7 is a cross-sectional side view illustrating a material layer forming a gate electrode deposited on the gate dielectric material.

[9]

8 is a cross-sectional side view illustrating a hard mask layer formed on the gate electrode material.

[10]

9 is a perspective view of the device after patterning of the hard mask and removal of regions of gate electrode material and gate dielectric material.

[11]

10 is a cross-sectional view showing the device after formation of spacers.

[12]

11 is a side cross-sectional view showing the device after recesses have been formed in the body;

[13]

12 is a cross-sectional side view of the device after source and drain material has been formed in the recesses.

[14]

13 is a block diagram illustrating a system according to an embodiment of the present invention.

[15]

In various embodiments, an apparatus and method for the formation of a strained multi-gate device are described. In the description that follows, several embodiments are set forth. However, those skilled in the art will recognize that the various embodiments may be practiced without one or more specific configurations or with other alternatives and/or other method materials or components. In other instances, well-known structures, materials, or operations are not shown or specifically described so as not to obscure features of various embodiments of the present invention. Similarly, for purposes of explanation, specific numbers, materials, and configurations are disclosed in order to provide a thorough understanding of the invention. Nevertheless, the present invention may be practiced without the specific configuration. Also, it is to be understood that the various embodiments shown in the drawings are illustrative and not unnecessarily to scale.

[16]

Reference throughout this specification to "one embodiment" or "one embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention, although these are all embodiments. It means not referring to what is in the example.

Thus, the phrases "in one embodiment" or "in one embodiment" in various places in this specification are not necessarily referring to the same embodiment of the invention. Moreover, the particular features, structures, materials, or properties may be combined in any suitable manner in one or more embodiments. Several additional layers and/or structures may be included, and/or features described may be omitted in other embodiments.

[17]

Several operations are described as a number of different operations in sequence in a manner that is optimally conducive to understanding the present invention.

However, the order of description is not necessarily to be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be executed in the order of presentation. The described operations may be performed in an order different from the described embodiment. Several additional operations may be performed and/or operations described may be omitted in other embodiments.

[18]

A non-planar multi-gate (tri-gate, etc.) transistor having a stressed channel and a method of manufacturing the same are described herein.

The transistor may include a stress material in a recess in the semiconductor body that provides stress to the channel region to improve carrier mobility. As the carrier mobility increases, the transistor driving current may increase. In one embodiment of the present invention, a stress material may be formed in recesses of all sides of the semiconductor body adjacent the channel region. Thus, stress is created on all sides of the channel, providing stress over a large area to improve device performance. The semiconductor body may be formed of a semiconductor substrate other than a semiconductor-on-insulator substrate (SOI).

[19]

1A is a side cross-sectional view illustrating a semiconductor device 100 according to an embodiment of the present invention.

The cross-sectional side view of FIG. 1A is taken through a plane defined as the Z-Y plane. Other figures may be side cross-sectional views through the Z-X plane defined perpendicular to the Z-Y plane. Still other figures may be perspective views showing three-dimensional X, Y, and Z. As described herein, the length of the device 100 is measured in the Y direction, the width is measured in the X direction, and the height is measured in the Z direction.

[20]

Device 100 may be a multi-gate transistor formed on substrate 102 in some embodiments.

In the embodiment shown herein, device 100 is shown as a tri-gate transistor, although device 100 may be other types of transistors or devices in other embodiments. The substrate 102 may comprise any material capable of serving as a basis upon which a semiconductor device may be built. The substrate 102 may be a substrate 102 containing silicon. In one embodiment, the substrate 102 may include a semiconductor material, such as single crystal silicon, gallium arsenide, or other suitable material. In some embodiments, the substrate 102 is a bulk semiconductor substrate 102 and may not be an SOI substrate. In other words, the substrate 102 may not include a buried oxide layer within the SOI substrate. In one embodiment, the substrate 102 may include a semiconductor material having a lattice structure and a crystal lattice having a lattice spacing.

[21]

Device 100 may include a body (also referred to as a "fin" in some embodiments) 118.

Body 118 may be a region of substrate 102, as shown in the embodiment of FIG. 1. In other embodiments, body 118 may be a different layer than substrate 102. In one embodiment, body 118 has a top surface and sidewalls and has a pin shape that protrudes over some other portions of device 100. In one embodiment, body 118 may include a semiconductor material having a lattice structure and a crystal lattice having a lattice spacing. Since the body 118 may simply be a region of the substrate 102, the body 118 may have the same lattice structure and the same crystalline structure with the lattice spacing as the body 102. The body 118 is pin-shaped and may have a length 150.

[22]

A gate dielectric layer 104 may be over the body 108.

The gate dielectric layer 104 may include any suitable type of dielectric material. In one embodiment of the present invention, the gate dielectric layer 104 may be a silicon dioxide (SiO₂), silicon oxynitride (SiO_xN_y) or silicon nitride (Si₃N₄) dielectric layer 104. In another embodiment of the present invention, the gate dielectric layer 104 may be a high-K gate dielectric layer, such as a metal oxide dielectric, tantalum pentoxide (Ta₂O₅), HfO₂, ZrO₂, and titanium. materials such as, but not limited to, titanium oxide (TiO₂).

[23]

A gate electrode 106 may be over the gate dielectric layer 104.

Gate electrode 106 may be formed of any suitable gate electrode material. In one embodiment, the gate electrode 106 may include polysilicon that may be doped. Gate electrode 106 may, in other embodiments, be a metal gate electrode and include tungsten, tantalum, titanium or their nitrides, metal alloys or other materials. Below the gate electrode 106 may be a channel region 114 of the body 118.

[24]

Over the gate electrode 106 may be a hard mask layer 108, which may include any material suitable for use in patterning the gate electrode 108.

[25]

Adjacent to the gate dielectric layer 104, the gate electrode 106 and the hard mask layer 108 may be spacers 110.

Spacer 110 may comprise any suitable material, such as silicon nitride, aluminum nitride, or other materials.

In some embodiments, the top of the spacer 110 may not be as high as the top of the hard mask layer 108.

[26]

Source and drain material 112 may be in recesses in body 118 on either side of gate electrode 106.

The source and drain materials 112 have a lattice structure substantially the same as the lattice structure of the body 118 and may have a lattice spacing different from the lattice spacing of the body. The source and drain material 112 can thus induce strain in the channel region 114 to improve the performance of the device 100. For example, the source and drain material 112 may have a greater lattice spacing than the material of the body 118, thereby providing a compressive stress within the channel region 114. This compressive stress can improve performance by increasing the migration of positively charged holes in P-type MOS device (PMOS) channels. In another embodiment, the source and drain material 112 has a smaller lattice spacing than the material of the body 118, resulting in a tensile stress in the channel region 114. This tensile stress can improve performance by improving the movement of negatively charged electrons in N-type MOS device (NMOS) channels. The source and drain materials 112 include silicon germanium (SiGe), silicon carbide (SiC), nickel silicide (NiSi), titanium silicide (TiSi₂), cobalt silicide (CoSi₂), or other suitable material capable of stressing the channel region 114. In embodiments where device 100 includes a source 130 and a drain 132, the source and drain material 112 may include both or a portion of the source 130 and drain 132.

[27]

There may also be front and back shallow trench isolation (STI) regions 116 that isolate the device 100 from other devices on the same substrate 102.

These STI regions 116 may include any suitable material.

[28]

FIG. 1B is a side cross-sectional view taken along line A-A of FIG. 1A showing the semiconductor device 100 according to an embodiment of the present invention.

The side cross-sectional view of Fig. 1B is a view obtained through a plane defined as the Z-X plane perpendicular to the Z-Y plane shown in Fig. 1A. 1B illustrates the multigate feature of device 100 in more detail.

[29]

The device 100 may include a lateral STI region 117 that separates the device 100 from other devices on the same substrate 102.

STI region 117 may comprise any suitable material.

[30]

The three-dimensional multi-gate feature of device 100 can be seen more clearly in FIG. 1B .

The dielectric layer 104 may be adjacent the top surface 122 and the sidewalls 120 of the body 118 . Similarly, the gate electrode 106 may be all three adjacent sides of the body 118 in the embodiment shown in FIG. 1B . Accordingly, three channel regions 114 instead of just one channel region 114 may be formed on the top and side surfaces. The channel region 114 including the channel region 114 at the sidewall 120 of the body 118 is referred to herein as "under" the gate electrode 106 . The gate electrode 106 is horizontally adjacent to the channel region 114 at the sidewall 120 of the body 118 , but nevertheless they are considered "below" the gate electrode 106, as described and claimed. Such a device 100 having a gate electrode 106 on three sides of the body 118 can be referred to as a tri-gate device 100 by creating three channel regions 114 . have. The gate electrode 106 may also be conformal to some extent with the body 118 and adjacent STI region 117 , the hard mask layer 108 being the gate electrode 106 , as shown in FIG. 1B .) and can be conformal.

[31]

The body 118 may have a height 152 measured from the top of the STI region 117 to the top of the body 118 below the central portion of the gate electrode 106 .

The body 118 may also have a width 156 measured at the non-recessed portion of the body 118 (ie, measured at the portion of the body 118 through which the AA line passes, and , not measured at the top of portions of body 118 through which BB or CC lines pass, where body 118 is recessed in these portions). The gate electrode 106 may have a height 154 measured from the top of the body 118 to the top of the gate electrode 106 . The STI region 117 has a depth 158 measured from the top of the STI region 117 to its bottom boundary. The depth of the STI region 116 may be substantially equal to the depth 158 of the STI region 117 .

[32]

In one embodiment, the depth 158 of the STI regions may be approximately twice the height 152 of the body 118 .

In another embodiment, the depth 158 of the STI regions may be greater than or approximately equal to twice the height 152 of the body 118 . In another embodiment, the depth 158 of the STI regions may be between about 1.8 times the height 152 of the body 118 and about 2.2 times the height 152 of the body 118 .

[33]

The height 154 of the gate electrode 106 may be about twice the height 152 of the body 118 in one embodiment.

The height 154 of the gate electrode 106 may be at least about twice the height 152 of the body 118 in one embodiment. The height 154 of the gate electrode 106 may be greater than about two-thirds the height 152 of the body 118 in one embodiment. In another embodiment, the height 154 of the gate electrode 106 may be between about 1.8 times the height 152 of the body 118 and about 2.2 times the height 152 of the body 118 . In another embodiment, the height 154 of the gate electrode 106 may be between about 1.5 times the height 152 of the body 118 and about twice the height 152 of the body 118 . In another embodiment, the height 154 of the gate electrode 106 may be between about 1.5 times the height 152 of the body 118 and approximately equal to the height 152 of the body 118 . In other embodiments, the height 154 of the gate electrode 106 may be smaller or larger.

[34]

The height 152 of the body 118 may be about twice the width 156 of the body 118 in one embodiment.

In other embodiments, the height 152 of the body 118 may be greater than twice the width 156 of the body 118 . In other embodiments, the height 152 of the body 118 may be between about 1.8 times the width 156 of the body 118 and about 2.2 times the width 156 of the body 118 . Other sizes of height 152 of body 118 and width 156 of body 118 may be used in other embodiments. In some embodiments, the width 156 of the body 118 may be selected such that the channel regions 114 are substantially completely depleted during operation. Thus, in some embodiments, when the substrate 102 is highly doped, the width 156 may become smaller and substantially completely depleted.

[35]

In one embodiment, the body 118 may have a width 156 of about 20 nanometers and a height 152 of about 40 nanometers, wherein the height 154 of the gate electrode 106 is at least 40 nanometers. , the depth 158 of the STI regions 116 and 117 may be at least 40 nanometers.

In one embodiment, the depth 158 of the STI regions 116 , 117 may be between about twice the height 152 of the body 118 and about three times the height 152 of the body 118 , but , in other embodiments, the STI regions 116 and 117 may have different depths. In another embodiment, the height 154 of the gate electrode 106 may be about 30 nanometers, and the width 156 of the body 118 may be between about 20 nanometers and about 40 nanometers. In some embodiments, the height 152 of the body 118 may be between about 20 nanometers and about 100 nanometers. In some embodiments, the width 156 of the body 118 may be between about 10 nanometers and about 50 nanometers. In still other embodiments, the structure of device 100 may have a different size.

[36]

FIG. 1C is a cross-sectional side view taken along line B-B of FIG. 1A showing a semiconductor device 100 according to an embodiment of the present invention.

As shown in FIG. 1C , the fins 118 are recess etched on all three sides (top and two sidewalls), and the etch undercuts under the spacers 110 . Since the source and drain material 112 is on all three sides of the fin 118 , it can apply stress to all three sides of the fin 118 . (As shown in FIG. 1C , the hard mask 108 is visible behind the spacer 110 , a cross-section through line B-B indicates that it does not cut the hard mask 108 .)

[37]

FIG. 1D is a cross-sectional side view taken along line C-C of FIG. 1A showing a semiconductor device 100 according to an embodiment of the present invention.

As can be seen in FIG. 1D , a larger portion of the fin 118 is etched away from the spacer 110 as opposed to FIG. 1C , where a smaller portion of the fin 118 below the spacer 110 is etched away. Dashed line 124 indicates the initial boundary of fin 118 before being etched away to form recesses in body 118 . In the embodiment shown in FIG. 1D , the source and drain material 112 is formed in the recesses of the fin 118 and also extends beyond the previous boundary 124 of the fin 118 . Also, in one embodiment, there may be recesses on all three sides of the fin 118 , and there may be a source and drain material 112 on all three sides 118 , the three sides being A stress may be applied to all three channel regions 114 . (In FIG. 1D , hard mask 108 and spacer 110 are visible behind source and drain material 112 , a cross-section through line CC indicates that it does not cut hard mask 108 or spacer 110 . do.) in some embodiments where the height 154 of the gate electrode 106 is less than the height 152 of the body 118 , a spacer separating the gate electrode 106 from the source/drain regions 130/132 The formation of 110 may limit recesses in the sides of the fin 118 . In such embodiments, most of the source/drain material 112 may be on top of the body 118 .

[38]

FIG. 1E is a side cross-sectional view taken along line C-C of FIG. 1A showing a semiconductor device 100 according to another embodiment of the present invention.

In the embodiment of FIG. 1E , the fin 118 is more etched away than in the embodiment of FIG. 1D to form deeper recesses. The source and drain material 112 is grown in the recess, but in this embodiment does not extend beyond the original boundary of the fin 118 . (It is pointed out that in other embodiments, the source and drain material 112 may extend beyond the limits shown in FIG. 1E .) the source and drain materials 112 of all three sides 118 may apply stress to all three channel regions 114 . (In FIG. 1E , the hard mask 108 and spacers 110 behind the source and drain materials 112 have been omitted.)

[39]

2-12 illustrate the steps in the formation of the apparatus 100 of FIG. 1 according to an embodiment.

[40]

2 is a cross-sectional side view illustrating a substrate 102 on which an apparatus 100 may be formed in accordance with one embodiment.

Substrate 102 may comprise any suitable material from which device 100 may be formed.

In one embodiment, the substrate 102 may be a bulk monocrystalline silicon material (ie, it is not an SOI substrate, and thus does not have a buried oxide layer). In this embodiment, the recesses in the source and drain material 112 may be formed as deep as desired rather than being limited to the depth at which the buried oxide layer is located. This allows deeper recesses and greater stresses to be applied to the channel region 114 to improve performance. In other embodiments, other semiconductor materials or other materials such as gallium arsenide may be used.

[41]

3 is a cross-sectional side view showing the substrate 102 after the STI regions 116 and 117 have been formed.

In one embodiment, portions of substrate 102 may be protected, unprotected portions may be removed to form trenches, and a material suitable for STI use may be deposited in the trenches. Both anterior and posterior STI regions 116 and lateral STI regions 117 may be formed simultaneously in some embodiments. The spacing between the trenches in which the front and rear STI regions 116 are formed defines the length 150 of the fin 118, and the spacing between the trenches in which the lateral STI regions 117 are formed is the length of the fin 118. A width 156 may be defined. The depth of the STI regions 116, 117 may be selected based on the predetermined height 152 of the body 118 and the predetermined STI depth 158.

[42]

4 is a cross-sectional side view of device 100 after STI regions 116 and 117 have been removed to form fins 118 in accordance with one embodiment.

In one embodiment, portions of STI regions 116 and 117 may be removed with hydrofluoric acid. In other embodiments, other methods may be used, such as RIE dry etching. The amount of original STI regions 116, 117 removed may determine the height 152 of the body in some embodiments. Accordingly, the amount of initially present STI regions 116, 117 removed may be determined based on the predetermined height 152 of the body 118. The remaining amount of the STI regions 116, 117 determines the depth 158 of the STI regions 116, 117. Thus, after partial removal of the STI regions 116 and 117, a body or fin 118 is defined that extends beyond the substrate 102 and the remainder of the STI regions 116, 117.

[43]

As described above with reference to FIG. 3, the initial depth of the STI regions 116, 117 shown in FIG. 3 is the predetermined height 152 of the body 118 and the predetermined depth of the STI regions 116, 117 (158).

Since the initial depth of the STI regions 116 and 117 includes both the height 152 of the body and the depth 158 of the STI regions 116 and 117 after the formation of the fin 118, the STI regions 116 and 117. The initial depth of is selected to be at least equal to the combined height 152 of the body 118 and the depth of the STI regions 116, 117. In one embodiment, the STI regions 116, 117 may have a depth 158 of at least about twice the height 152 of the body 118. In one embodiment, as shown in FIG. 3, the initial depth of the STI regions 116 and 117 may be about 1500 angstroms (Å). 4, after formation of the fin 118, the fin 118 may have a height 152 of about 500 angstroms, and the STI regions 116 and 117 have a depth 158 of about 1000 angstroms. In another embodiment, as shown in FIG. 3, the initial depth of the STI regions 116, 117 may be between about 1000 angstroms and about 3000 angstroms. In another embodiment, the initial depth of the STI regions 116 and 117 may be different. 4, after formation of the fin 118, the fin 118 may have a height 152 of about one-third or less of its original depth, and the STI regions 116, 117 are initially it may have a depth 158 of about two-thirds of its depth or greater. In other embodiments, the size of the height 152 of the fin 118 relative to the depth 158 of the STI regions 116, 117 may be different.

[44]

5 is a perspective view illustrating the fin 118 after formation by removal of portions of the STI regions 116 and 117 according to one embodiment.

Anterior and posterior STI regions 116 and lateral regions 117 may surround fins 118 projecting over STI regions 116, 117. Body 118 may extend down through STI regions 116, 117 to the remainder of substrate 102. Dashed line 125 depicts the boundary of body 118 below the top surface of STI regions 116, 117 as it extends to meet other regions of substrate 102. Also shown in FIG. 5 are the length 150 of the fin 118, the width 156 of the fin, the height 152 of the fin 118 and the depth 158 of the STI regions 116, 117. Note that the fin 118 is somewhat less long and less wide at the top than at the point where it meets the

STI regions 116 and 117 ; The drawings show an ideal representation. In some embodiments, such tapering is avoided as far as practicable to keep the sidewalls straight.

[45]

6 is a cross-sectional side view illustrating the gate dielectric 104 material layer formed on the surfaces of the body 118 and the STI regions 116 and 117, according to one embodiment.

The gate dielectric layer 104 material may include any suitable type of dielectric material.

[46]

7 is a cross-sectional side view illustrating the material layer forming the gate electrode 106 deposited over the gate dielectric layer 104 material.

In some embodiments, the layer of material forming the gate electrode 106 may comprise a single layer of a single material. In other embodiments, a number of different materials may be used, and there may be multiple layers of material. Thus, although shown only as a single layer in some embodiments, the gate electrode 106 may include multiple layers of different materials, although only referred to herein as a single layer of material, may actually include multiple layers. Gate electrode 106 may be formed of any suitable gate electrode material. In one embodiment, the gate electrode 106 may include polysilicon that may be doped. In another embodiment, the gate electrode 106 may include a polysilicon layer over a metal layer. In another embodiment, the gate electrode 106 may include different material layers, and may include two or more layers. The material layer forming the gate electrode 106 may have a thickness as large as at least about twice the height 152 of the body 118 in one embodiment, although other thicknesses may exist in other embodiments. . The material layer forming the gate electrode 106 may be conformally deposited.

[47]

8 is a cross-sectional side view illustrating a hard mask layer 108 formed on the gate electrode 106 material in accordance with one embodiment of the present invention.

The hard mask 108 may be patterned to expose regions where removal is desired, while protecting regions of the gate electrode 106 material and gate dielectric 104 material that are desired to be left in place. The exposed regions of the gate electrode 106 material and the gate dielectric 104 material may be removed in any suitable manner.

[48]

9 is a perspective view of the device 100 after the hard mask 108 has been patterned and the gate electrode 106 material and gate dielectric 104 material regions desired to be removed are removed, in accordance with one embodiment.

The gate dielectric layer 104 , the gate electrode 106 and the hard mask layer 108 can be seen adjacent all three sides (top and sidewalls) of the body 118 . It is pointed out that, for simplicity, the gate dielectric layer 104, the gate electrode 106, and the hard mask layer 108 are each not shown. By having a gate electrode adjacent to all three sides, the effective gate width of the device 100 is the width 156 of the body 118 plus twice the height 152 of the body 118 . Spacing 160 is the gate length of device 100 . In one embodiment, the spacing 160 may be between about 10 nanometers and about 50 nanometers. In other embodiments, the spacing may be larger or smaller, for example up to 2 μm .

[49]

10 is a cross-sectional side view illustrating the device 100 after formation of the spacer 110 according to an embodiment of the present invention.

Additional processes, such as tip junction formation, may be performed prior to formation of spacers 110 in some embodiments. Formation of spacers 110 may be performed in any suitable manner. In one embodiment, a layer of spacer 110 material may be deposited on device 100 . This material may include any suitable material, such as silicon nitride, silicon dioxide or other materials. Portions of the spacer 110 material layer are then removed leaving the spacer 110 adjacent the gate dielectric layer 104 , the gate electrode 106 and the hard mask 108 , but in effect the body 118 is the STI region 116 . , 117) as well as portions

of the spacer 110 material layer adjacent to where it meets other regions. As a result, the top of the spacer 110 may be below the top of the hard mask 108 .

[50]

11 is a cross-sectional side view of device 100 after recess 126 has been formed in body 118 in accordance with one embodiment of the present invention.

The recesses 126 may be referred to as source and drain recesses. Recess 126 may be formed by any suitable method, such as wet etching. Recess 126 may have a depth 162 below the top surface of body 118 adjacent gate dielectric 104 of between about 50 angstroms and about 1000 angstroms in some embodiments; other depths 162 are possible. In one embodiment, the recess 126 may extend horizontally below the sidewalls 110 and possibly under the gate dielectric 104 in the case of a spacing 164 of between 5 nanometers and about 50 nanometers. However, in other embodiments, this spacing 164 may be different. In some embodiments where the substrate 102 is a non-SOI substrate, the recess 126 may be made deeper than is possible in an SOI substrate, where in an SOI substrate, the depth of the buried oxide layer is in the recess 126 . This is because it provides the maximum possible depth for As the recess 126 is deepened, the stress applied to the channel region 114 may be increased, providing improved performance over the performance that may be obtained at low stress of an SOI-based device.

[51]

The process used to remove portions of the top surface of the fin 118 also removes portions of the sidewalls of the fin 118 when the process used is partially or fully isotropic in some embodiments. .

The results of this removal process can be shown in FIGS. 1C-1E , as described above, showing portions of the sidewalls of the fin 118 removed at various spacings from the gate electrode 106 .

[52]

12 is a cross-sectional side view illustrating device 100 after source and drain material 112 is formed in recess 126 according to one embodiment.

Source and drain material 112 may operate as a source and drain for device 100 or as part of a source and drain of device 100 . In one embodiment, the source and drain material 112 may include silicon germanium (SiGe), silicon carbide (SiC), nickel silicide (NiSi), titanium silicide (TiSi₂), cobalt silicide (CoSi₂), or other materials. .

[53]

In one embodiment, the substrate 102 includes a material having a lattice structure (eg, a base centered cube or other lattice structure) and lattice spacing.

The source and drain material 112 may have the same lattice structure as the material of the substrate 102 , but may have a different lattice spacing. A stress may be created in the channel region 114 of the device 100 as a result of these different grating spacings. If the source and drain material 112 has a greater lattice spacing than the substrate 112 material, a compressive stress 170 may be induced in the channel region 114 . If the source and drain material 112 has a smaller lattice spacing than the substrate 112 material, a tensile stress (not shown) may be induced in the channel region 114 . Accordingly, since stress is induced in the regions of the channel 114 of the device 100 by the source and drain material 112 , the material may also be referred to as the stress material 112 .

[54]

In one embodiment, the substrate 102 may include single crystal silicon, and the source and drain materials 112 in the recesses 126 may include silicon germanium having a greater lattice spacing than silicon.

In this embodiment, the SiGe stressed material may induce compressive stress 170 in the channel region 114 to improve the performance of the PMOS device 100 . In other embodiments, tensile stress may be induced in the channel region 114 by the stress material 112 to improve the performance of the NMOS device 100 . Recesses 126 may be formed in the sides of the fin 118 as well as the top surface of the fin 118 , where a stress material may be formed in the recesses 126 on both the sides and top of the fin 118 . Therefore, stress may be applied to all three channel regions 114 .

[55]

In one embodiment, the stress material 112 may be formed epitaxially, although other processes may be used.

The epitaxially formed source and drain material 112 may extend beyond the amount used to contain the fins 118, as shown in FIG. 12. In other embodiments, the stress material 112 may be substantially coplanar with the top surface of the fin 118.

[56]

In some embodiments, the source drain material 112 may be doped when it is formed.

For example, in one embodiment where the stress material 112 includes an epitaxially formed SiGe, a dopant may be incorporated into the SiGe as it is grown. In such embodiments, an ion implantation or annealing step may not be necessary. In other embodiments, ions may be implanted into the source and drain material 112 to transform the source and drain material into the source and drain of the device 100 after the source and drain material 112 is formed.

[57]

Additional process steps may be performed to complete the apparatus 100 as would be appreciated by one of ordinary skill in the art.

[58]

FIG. 13 is a block diagram illustrating a system 1300 according to an embodiment of the present invention.

Stress is induced in the channel region 114 as described above, which may be included in the system 1300 of FIG. 13 by one or more multigate devices 100 having a stress material 112.

As shown, in the case of this embodiment, system 1300 includes a computing device 1302 for processing data. The computing device 1302 may include a motherboard 1304, and in particular, a networking interface 1306 coupled to the bus 1310 and the processor 1308 coupled to or from a motherboard 1304. The chipset may form some or all of the bus 1310. Processor 1308, chipset and/or other portions of system 1300 may include one or more devices 100 as described above.

[59]

Depending on the application, system 1300 may include, but is not limited to, volatile and non-volatile memory 1312, a graphics processor (motherboard as integral with motherboard 1304 or each removable component such as an AGP or PCI-E graphics processor, etc.), connected to), a digital signal processor, a crypto processor, a mass storage device 1314 (hard disk, compact disk (CD), digital versatile disk (DVD), and others etc.), input and/or output devices 1316, and the like.

[60]

In various embodiments, system 1300 is a personal digital assistant (PDA), mobile phone, tablet computing device, laptop computing device, desktop computing device, set-top box, entertainment control unit, a digital camera, a digital video recorder, a CD player, a DVD player, or other digital device of the like.

[61]

Any of one or more components 1306, 1314, etc. of FIG. 13 may include one or more devices 100 described herein.

For example, trigate transistor 100 with SiGe stress material 112 may be part of CPU 1308, motherboard 1304, graphics processor, digital signal processor, or other device.

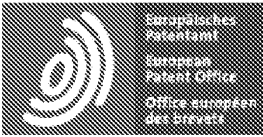
[62]

The foregoing description of embodiments of the present invention has been provided for purposes of illustration and description, and is not intended to be exhaustive or to limit the present invention to the form disclosed.

This description and the claims below include terms left, right, top, bottom, above, below, above, below, first, second, etc., which are used for descriptive purposes only and are not to be construed as limiting. shouldn't

For example, terms referring to relative vertical position refer to situations where the device side (or active surface) of a substrate or integrated circuit is the "top" side of the substrate, where the substrate is actually in any orientation. As may be the case, the "upper" side of the substrate is lower than the "lower" side in the standard terrestrial frame of reference and is included within the meaning of the term "upper".

The term "above" as used herein (including in the claims) does not indicate that a first layer "above" a second layer is directly "on" or in direct contact with a second layer, unless it is specifically stated otherwise. and there may be a third layer or other structure between the first layer and the second layer over the first layer. Embodiments of devices or articles described herein may be manufactured, used, and shipped in many locations and orientations. Those of ordinary skill in the relevant art will recognize that many modifications and variations are possible in light of the above teachings. Those skilled in the art will recognize many equivalent combinations and substitutions of the various parts shown in the drawings. It is, therefore, pointed out that the scope of the invention is intended to be limited not by this detailed description but by the appended claims.



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CLAIMS KR20080075009A

1.

a substrate comprising a semiconductor material, the semiconductor material having a first lattice structure and a first crystal lattice of a first lattice spacing;

a body region of the substrate, the body region having a top surface and sidewalls, the sidewalls being isolated by a width and extending a length;

a gate electrode on a top surface of the body region and a portion of sidewalls;

a source recess and a drain recess in the body region on either side of the gate electrode; and

stress material in the source and drain recesses

including,

wherein the stress material has a second lattice structure substantially the same as the first lattice structure and a second material having a second crystal lattice having a second lattice spacing different from the first lattice spacing.

2.

According to claim 1,

and channel regions between the source and the drain in the substrate below the gate electrode and adjacent to the top surface and sidewalls of the body region.

3.

According to claim 1,

The substrate is a semiconductor device that is not a semiconductor-on-insulator substrate (SOI).

4.

According to claim 1,

front and rear shallow trench isolation (STI) regions, wherein the length of the body region is between the front and rear STI regions; and

Lateral STI regions in the substrate on either side of the sidewalls of the body region

further comprising,

The STI regions have a predetermined depth.

5.

The method of claim 4,

The top surface of the body region, below the gate electrode, is at a height above the lateral STI regions.

6.

The method of claim 5,

The height of the body region is at least about twice the width of the body region.

7.

6. The method of claim 5,

The depth of the STI regions is at least about twice the height of the body region.

8.

The method of claim 7,

A height of the body region is at least about twice a width of the body region.

9.

According to claim 1,

The source and drain recesses are recessed into the sidewalls of the body region as well as recessed into the top surface of the body region.

10.

The method of claim 9,

the source and the drain comprise the second material, the second material extending vertically beyond the top surface of the body region at the source and the drain and horizontally extending beyond the sidewalls of the body region; semiconductor device.

11.

The method of claim 10,

The second lattice spacing is greater than the first lattice spacing.

12.

a substrate comprising a semiconductor material having a first lattice structure and a first grating at a first lattice spacing, wherein the substrate is not an SOI;

STI regions at the front, back and side of the substrate, the STI regions having a depth;

a body region of the substrate, at least a portion of the body region extending to a height above the STI regions, the body region extending a length between the front and rear STI regions and between the lateral STI regions has a certain width - ;

a gate electrode on the top surface and sidewalls of the body region;

channel regions in the body region below the gate electrode;

source/drain recesses on either side of the gate electrode, the source/drain recesses including recesses in the top surface and sidewalls of the body region; and

A second material in the source/drain regions having a second grating structure substantially the same as the first grating structure and a second grating at a second grating spacing different from the first grating spacing

A semiconductor device comprising a.

13.

The method of claim 12,

wherein the width is between about 20 nanometers and about 40 nanometers, and the height is between about 1.8 times and about 2.2 times the width.

14.

The method of claim 13,

wherein the height is between about 400 Angstroms and about 600 Angstroms, and the depth is between about 900 Angstroms and about 1100 Angstroms.

15.

The method of claim 14,

and the second material extends beyond the top surface and the sidewalls of the body region at the source and the drain.

16.

removing portions of the substrate comprising a semiconductor material having a first grating structure and a first grating at a first lattice spacing to form a fin having a top surface and sidewalls, the fin being constant between the sidewalls has width - ;

forming a gate electrode on top and sidewalls of the fin, adjacent to the top and sidewalls, channel regions under the gate electrode;

removing portions of the fin on either side of the gate electrode to form source/drain recesses extending into the top and sidewalls; and

forming a second material in the source/drain recesses having a second lattice of a second lattice spacing different from the first lattice spacing;

How to include.

17.

The method of claim 16,

wherein the substrate is not SOI.

18.

The method of claim 17,

forming lateral STI regions in the substrate on either side of the sidewalls of the body region;

further comprising,

wherein the body region has a height greater than the STI regions, and the STI regions have a depth.

19.

The method of claim 18,

wherein the depth of the STI regions is at least about twice the height of the body region.

20.

The method of claim 19.

The height of the body region is at least about twice the width of the body region.



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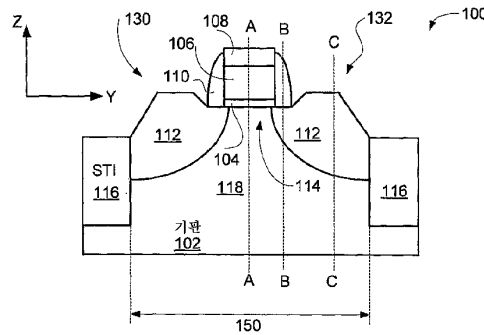
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(54) 리세스 스트레인 영역을 갖는 멀티게이트 장치

(57) 요약

본 발명의 실시예들은 다수의 게이트들을 갖는 장치를 제공한다. 장치 보디 금속 게이트의 리세스들 내의 스트
레스 재료에 의해 장치의 채널 영역들 내에 스트레스가 유도되어 장치의 성능을 개선한다.

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특허청구의 범위

청구항 1

반도체 재료(semiconductor material)를 포함하는 기판 - 상기 반도체 재료는 제1 격자 구조(lattice structure) 및 제1 격자 간격(lattice spacing)의 제1 결정 격자(crystal lattice)를 가짐 - ;

상기 기판의 보디 영역 - 상기 보디 영역은 상부면과 측벽들을 가지며, 상기 측벽들은 일정 폭(a width)으로 격리되고, 일정 길이(a length)로 연장함 - ;

상기 보디 영역의 상부면과 측벽들의 일부분 상의 게이트 전극;

상기 게이트 전극의 어느 한 측면 상의 상기 보디 영역 내의 소스 리세스(recess) 및 드레인 리세스; 및

상기 소스 및 드레인 리세스들 내의 스트레스 재료(stress material)

를 포함하고,

상기 스트레스 재료는 상기 제1 격자 구조와 실질적으로 동일한 제2 격자 구조를 갖고, 상기 제1 격자 간격과는 상이한 제2 격자 간격을 갖는 제2 결정 격자를 갖는 제2 재료를 포함하는 반도체 장치.

청구항 2

제1항에 있어서,

상기 게이트 전극 아래이고 상기 보디 영역의 상기 상부면과 측벽들과 인접하는, 상기 소스와 상기 드레인 사이의 채널 영역들을 상기 기판에 더 포함하는 반도체 장치.

청구항 3

제1항에 있어서,

상기 기판은 SOI(semiconductor-on-insulator substrate)가 아닌 반도체 장치.

청구항 4

제1항에 있어서,

전방 및 후방의 STI(shallow trench isolation) 영역들 - 상기 보디 영역의 상기 길이는 상기 전방 및 후방의 STI 영역들 사이임 - ; 및

상기 보디 영역의 측벽들의 어느 한 측면 상의 기판에 있는, 측방의 STI 영역들

을 더 포함하고,

상기 STI 영역들은 일정 깊이를 갖는 반도체 장치.

청구항 5

제4항에 있어서,

상기 게이트 전극 아래의, 상기 보디 영역의 상기 상부면은 상기 측방의 STI 영역들 위의 높이인 반도체 장치.

청구항 6

제5항에 있어서,

상기 보디 영역의 높이는 적어도 상기 보디 영역의 폭의 약 2배인 반도체 장치.

청구항 7

제5항에 있어서,

상기 STI 영역들의 깊이는 적어도 상기 보디 영역의 높이의 약 2배인 반도체 장치.

청구항 8

제7항에 있어서,

상기 보디 영역의 높이는 상기 보디 영역의 폭의 적어도 약 2배인 반도체 장치.

청구항 9

제1항에 있어서,

상기 소스 및 드레인 리세스들은 상기 보디 영역의 상기 측벽들 내로 리세스될 뿐만 아니라 상기 보디 영역의 상부면 내로도 리세스되는 반도체 장치.

청구항 10

제9항에 있어서,

상기 소스 및 상기 드레인은 상기 제2 재료를 포함하고, 상기 제2 재료는 상기 소스와 상기 드레인에서 상기 보디 영역의 상기 상부면을 넘어 수직으로 연장하고, 상기 보디 영역의 상기 측벽들을 넘어 수평으로 연장하는 반도체 장치.

청구항 11

제10항에 있어서,

상기 제2 격자 간격은 상기 제1 격자 간격보다 큰 반도체 장치.

청구항 12

제1 격자 구조와 제1 격자 간격의 제1 격자를 갖는 반도체 재료를 포함하는 기판 - 상기 기판은 SOI가 아님 - ;

상기 기판의 전방, 후방 및 측방의 STI 영역들 - 상기 STI 영역들은 일정 깊이를 가짐 - ;

상기 기판의 보디 영역 - 상기 보디 영역의 적어도 일 부분은 상기 STI 영역들 위의 높이로 연장하고, 상기 보디 영역은 상기 전방 및 후방의 STI 영역들 사이의 일정 길이와 상기 측방의 STI 영역들 사이의 일정 폭을 가짐 - ;

상기 보디 영역의 상부면과 측벽들 상의 게이트 전극;

상기 게이트 전극 아래의 상기 보디 영역 내의 채널 영역들;

상기 게이트 전극의 어느 한 측면 상의 소스/드레인 리세스들 - 상기 소스/드레인 리세스들은 상기 보디 영역의 상기 상부면과 상기 측벽들 내에 리세스들을 포함함 - ; 및

상기 소스/드레인 영역들에, 상기 제1 격자 구조와 실질적으로 동일한 제2 격자 구조 및 상기 제1 격자 간격과는 상이한 제2 격자 간격의 제2 격자를 갖는 제2 재료

를 포함하는 반도체 장치.

청구항 13

제12항에 있어서,

상기 폭은 약 20나노미터와 약 40나노미터 사이이며, 상기 높이는 약 상기 폭의 약 1.8배와 약 2.2배 사이인 반도체 장치.

청구항 14

제13항에 있어서,

상기 높이는 약 400Å과 약 600Å 사이이며, 상기 깊이는 약 900Å과 약 1100Å 사이인 반도체 장치.

청구항 15

제14항에 있어서,

상기 제2 재료는 상기 소스와 상기 드레인에서 상기 보디 영역의 상기 상부면과 상기 측벽들을 넘어 연장하는 반도체 장치.

청구항 16

제1 격자 구조와 제1 격자 간격의 제1 격자를 갖는 반도체 재료를 포함하는 기판의 부분들을 제거하여 상부면과 측벽들을 갖는 핀(fin)을 형성하는 단계 - 상기 핀은 상기 측벽들 사이에 일정 폭을 가짐 - ;

상기 핀의 상부와 측벽들 상의 게이트 전극을 형성하는 단계 - 상기 상부와 상기 측벽들에 인접하여 채널 영역들이 상기 게이트 전극 밑에 위치함 - ;

상기 게이트 전극의 어느 한 측면 상의 상기 핀의 부분들을 제거하여 상기 상부 및 측벽들 내로 연장하는 소스/드레인 리세스들을 형성하는 단계; 및

상기 소스/드레인 리세스들에서 상기 제1 격자 간격과는 상이한 제2 격자 간격의 제2 격자를 갖는 제2 재료를 형성하는 단계

를 포함하는 방법.

청구항 17

제16항에 있어서,

상기 기판은 SOI가 아닌 방법.

청구항 18

제17항에 있어서,

상기 보디 영역의 상기 측벽들의 어느 한 측면 상의 상기 기판에 측방의 STI 영역들을 형성하는 단계

를 더 포함하고,

상기 보디 영역은 상기 STI 영역들보다 위인 높이를 갖고, 상기 STI 영역들은 일정 깊이를 가지는 방법.

청구항 19

제18항에 있어서,

상기 STI 영역들의 상기 깊이는 상기 보디 영역의 높이의 적어도 약 2배인 방법.

청구항 20

제19항에 있어서,

상기 보디 영역의 높이는 상기 보디 영역의 폭의 적어도 약 2배인 방법.

명세서

배경 기술

- <1> 기판상의 회로 장치(예를 들어, 반도체 기판상의 집적회로(IC) 트랜지스터, 저항, 커패시터 등)의 성능 향상은 일반적으로 이러한 장치의 설계, 제조 및 동작동안 주요한 요인으로 고려된다. 예를 들어, 상보형 금속 산화 반도체(complementary metal oxide semiconductor; CMOS)에 사용된 것과 같은 금속 산화 반도체(metal oxide semiconductor; MOS) 트랜지스터 반도체 장치의 설계 및 제조 또는 형성 동안, N형 MOS 장치(NMOS) 채널에서 음으로 대전된 전자들의 이동성을 증가시키고, 또한, P형 MOS 장치(PMOS) 채널 내의 양으로 대전된 정공의 이동을 증가시키는 것이 때로 소망된다.

발명의 상세한 설명

- <15> 여러 실시예들에 있어서, 스트레인드 멀티게이트 장치(strained multi-gate device)의 형성에 관한 장치 및 방

법을 기술한다. 다음의 설명에 있어서, 여러 실시예들을 기술한다. 그러나 이 분야의 통상의 기술자라면, 여러 실시예들은 하나 이상의 특정 구성이 없이도 또는 다른 대체물 및/또는 다른 방법 재료 또는 부품으로도 실시될 수 있음을 인식할 것이다. 다른 예들에 있어서, 공지의 구조, 재료 또는 동작을 본 발명의 여러 실시예들의 특징들을 방해하지 않도록 도시하지 않거나 구체적으로 설명하지 않는다. 유사하게, 설명의 목적으로, 특정 숫자, 재료 및 구성을 본 발명의 충분한 이해를 제공하도록 개시한다. 그럼에도, 본 발명은 특정 구성없이 실시될 수 있다. 또한, 도면에 도시된 여러 실시예들은 대표적인 것을 예시하고, 불필요하게 스케일로 되지 않은 것은 물론이다.

- <16> 이 명세서를 통한 "일 실시예" 또는 "한 실시예"에 대한 참조는 이 실시예와 관련하여 기술한 특정 특징, 구조, 재료 또는 특성이 본 발명의 적어도 일 실시예에 포함되지만, 이들이 모든 실시예에 있는 것을 가리키는 것은 아님을 의미한다. 따라서, 이 명세서 여러 곳에서의 어구 "일 실시예에서" 또는 "한 실시예에서"는 반드시 본 발명의 같은 실시예를 참조하지는 않는다. 또한, 특정 특징, 구조, 재료 또는 특성은 일 이상의 실시예에서 임의의 적합한 방식으로 조합될 수 있다. 여러 추가의 층들 및/또는 구조들이 포함될 수 있으며, 및/또는 기술된 특징은 다른 실시예에서 생략될 수 있다.
- <17> 여러 동작들은 본 발명의 이해에 최적의 도움이 되는 방식으로 순서적으로 다수의 다른 동작들로서 기술한다. 그러나 기술의 순서는 이들 동작들이 반드시 순서 종속적(order dependent)이라는 것을 암시한다고 해석될 필요는 없다. 특히, 이들 동작은 표현 순서로 실행될 필요는 없다. 기술한 동작들은 기술한 실시예와는 다른 순서로 실행될 수 있다. 여러 추가적인 동작들이 실행될 수 있으며 및/또는 기술한 동작들이 다른 실시예들에서 생략될 수 있다.
- <18> 스트레스트 채널(stressed channel)을 갖는 비 평면 멀티게이트(트리게이트(tri-gate) 등) 트랜지스터 및 그 제조 방법을 여기에서 기술한다. 이 트랜지스터는 캐리어 이동도를 개선하기 위해 채널 영역에 스트레스를 제공하는 반도체 보디(body)의 리세스 내의 스트레스 재료(stress material)를 포함할 수 있다. 캐리어 이동도가 커지면, 트랜지스터 구동 전류가 증가할 수 있다. 본 발명의 일 실시예에서, 스트레스 재료는 채널 영역에 인접한 반도체 보디의 모든 측면(side)의 리세스내에 형성될 수 있다. 따라서, 채널의 모든 측면에 스트레스가 생겨서, 큰 면적에 걸쳐서 스트레스를 제공하여 장치 성능을 개선한다. 반도체 보디는 SOI(semiconductor-on-insulator substrate)가 아닌 반도체 기판으로 형성될 수 있다.
- <19> 도 1a는 본 발명의 일 실시예의 반도체 장치(100)를 도시하는 측 단면도이다. 도 1a의 측 단면도는 Z-Y 평면으로서 규정된 평면을 통해 얻어진다. 다른 도면들은 Z-Y 평면에 수직으로 규정된 Z-X 평면을 통한 측 단면도일 수 있다. 또 다른 도면들은 3차원 X, Y, 및 Z를 도시하는 사시도일 수 있다. 여기에서 설명한 바와 같이, 장치(100)의 길이는 Y 방향에서 측정되고, 폭은 X 방향에서 측정되고, 높이는 Z 방향에서 측정된다.
- <20> 장치(100)는 일부 실시예들에서 기판(102) 상에 형성된 멀티게이트 트랜지스터일 수 있다. 여기에서 도시된 실시예에서, 장치(100)는 트리게이트 트랜지스터로서 도시되지만, 장치(100)는 다른 실시예들에서 다른 타입의 트랜지스터 또는 장치일 수 있다. 기판(102)은 반도체 장치가 조립(built)될 수 있는 기초로서 작용할 수 있는 임의의 재료를 포함할 수 있다. 기판(102)은 실리콘을 함유하는 기판(102)일 수 있다. 일 실시예에서, 기판(102)은 단결정 실리콘, 갈륨 아세나이드(gallium arsenide) 또는 다른 적합한 재료 등의 반도체 재료를 포함할 수 있다. 몇몇 실시예들에서, 기판(102)은 벌크 반도체 기판(102)이고, SOI 기판이 아닐 수 있다. 반면, 기판(102)은 SOI 기판 내에 있는 매몰 산화물 층(buried oxide layer)을 포함하지 않을 수 있다. 일 실시예에서, 기판(102)은 격자 구조(lattice structure) 및 격자 간격(lattice spacing)을 갖는 결정 격자를 갖는 반도체 재료를 포함할 수 있다.
- <21> 장치(100)는 보디(일부 실시예들에서 "핀(fin)"이라고도 함)(118)를 포함할 수 있다. 보디(118)는 도 1의 실시예에서 도시한 바와 같이, 기판(102)의 영역일 수 있다. 다른 실시예들에서, 보디(118)는 기판(102)과는 다른 층일 수 있다. 일 실시예에서, 보디(118)는 상부면과 측면들을 가지며, 장치(100)의 일부 다른 부분들 위로 돌출하여 핀 형상을 갖는다. 일 실시예에서, 보디(118)는 격자 구조와 격자 간격을 갖는 결정 격자를 갖는 반도체 재료를 포함할 수 있다. 보디(118)는 간단히 기판(102)의 영역일 수 있으므로, 보디(118)는 보디(102)와 같은 격자 구조 및 격자 간격을 갖는 같은 결정 구조를 가질 수 있다. 보디(118)는 핀 형상이고, 길이(150)를 가질 수 있다.
- <22> 보디(108) 위에 게이트 유전층(104)이 있을 수 있다. 게이트 유전층(104)은 임의의 적합한 타입의 유전 재료를 포함할 수 있다. 본 발명의 일 실시예에서, 게이트 유전층(104)은 실리콘 이산화물(silicon dioxide; SiO₂),

실리콘 산질화물(silicon oxynitride; SiO_xN_y) 또는 실리콘 질화물(silicon nitride; Si_3N_4) 유전층(104)일 수 있다. 본 발명의 다른 실시예에서, 게이트 유전층(104)은 금속 산화 유전체 등의 하이 k 게이트 유전층(high-K gate dielectric layer)일 수 있으며, 탄탈륨 펜톡사이드(tantalum pentaoxide; Ta_2O_5), HfO_2 , ZrO_2 및 티타늄 산화물(titanium oxide; TiO_2) 등의 재료를 포함하지만 이로 한정되지 않는다.

- <23> 게이트 유전층(104) 위에는 게이트 전극(106)이 있을 수 있다. 게이트 전극(106)은 임의의 적합한 게이트 전극 재료로 형성될 수 있다. 일 실시예에서, 게이트 전극(106)은 도핑될 수 있는 폴리실리콘을 포함할 수 있다. 게이트 전극(106)은 다른 실시예에서, 금속 게이트 전극일 수 있으며, 텅스텐, 탄탈, 티타늄 또는 그들의 질화물, 금속 합금 또는 다른 재료를 포함한다. 게이트 전극(106) 아래에 보디(118)의 채널 영역(114)이 있을 수 있다.
- <24> 게이트 전극(106) 위에는 하드 마스크 층(108)이 있을 수 있으며, 하드 마스크 층(108)은 게이트 전극(106) 패터닝 시 사용에 적합한 임의의 재료를 포함할 수 있다.
- <25> 게이트 유전층(104), 게이트 전극(106) 및 하드 마스크층(108)에 인접하여 스페이서(110)가 있을 수 있다. 스페이서(110)는 실리콘 질화물, 알루미늄 질화물 또는 다른 재료 등의 임의의 적합한 재료를 포함할 수 있다. 일부 실시예들에서, 스페이서(110)의 상부는 하드 마스크 층(108)의 상부만큼 높지 않을 수 있다.
- <26> 게이트 전극(106)의 어느 한쪽의 보디(118) 내의 리세스들 내에 소스 및 드레인 재료(112)가 있을 수 있다. 소스 및 드레인 재료(112)는 실질적으로 보디(118)의 격자 구조와 같은 격자 구조를 갖고 보디의 격자 간격과는 다른 격자 간격을 가질 수 있다. 따라서 소스 및 드레인 재료(112)는 채널 영역(114) 내에 스트레인을 유도하여 장치(100)의 성능을 개선할 수 있다. 예를 들어, 소스 및 드레인 재료(112)는 보디(118)의 재료보다 큰 격자 간격을 가질 수 있어서, 채널 영역(114) 내에 압축 스트레스(compressive stress)를 제공한다. 이 압축 스트레스는 P 형 MOS 장치(PMOS) 채널들 내의 양으로 대전된 정공들의 이동을 증가시켜 성능을 개선할 수 있다. 다른 실시예에서, 소스 및 드레인 재료(112)는 보디(118)의 재료보다 작은 격자 간격을 가져서 채널 영역(114) 내에 인장 스트레스(tensile stress)를 초래한다. 이러한 인장 스트레스는 N 형 MOS 장치(NMOS) 채널들 내의 음으로 대전된 전자들의 이동을 개선하여 성능을 개선할 수 있다. 소스 및 드레인 재료(112)는 실리콘 게르마늄(silicon germanium; SiGe), 실리콘 카바이드(silicon carbide; SiC), 니켈 실리사이드(nickel silicide; NiSi), 티타늄 실리사이드(titanium silicide; TiSi_2), 코발트 실리사이드(cobalt silicide; CoSi_2), 또는 채널 영역(114)에 스트레스를 가할 수 있는 다른 적합한 재료를 포함할 수 있다. 장치(100)가 소스(130) 및 드레인(132)을 포함하는 실시예들에서, 소스 및 드레인 재료(112)는 소스(130) 및 드레인(132) 모두 또는 그 일부를 포함할 수 있다.
- <27> 같은 기판(102) 상에서 다른 장치들로부터 장치(100)를 분리하는 전방 및 후방의 STI(shallow trench isolation) 영역들(116)이 또한 있을 수 있다. 이 STI 영역들(116)은 임의의 적합한 재료를 포함할 수 있다.
- <28> 도 1b는 본 발명의 일 실시예의 반도체 장치(100)를 나타내는 도면 1a의 A-A 선을 따라 절취한 측 단면도이다. 도 1b의 측 단면도는 도 1a에 도시한 Z-Y 평면에 수직인 Z-X 평면으로서 규정된 평면을 통해 얻어진 도면이다. 도 1b는 장치(100)의 멀티게이트 특징을 보다 상세하게 나타낸다.
- <29> 장치(100)는 장치(100)를 같은 기판(102)에서 다른 장치들과 분리하는 측방의 STI 영역(117)을 포함할 수 있다. STI 영역(117)은 임의의 적합한 재료를 포함할 수 있다.
- <30> 장치(100)의 3차원 멀티게이트 특징은 도 1b에서 보다 명확하게 볼 수 있다. 유전층(104)은 보디(118)의 상부면(122) 및 측벽들(120)에 인접할 수 있다. 유사하게, 게이트 전극(106)은 도 1b에 도시된 실시예에서, 보디(118)의 인접한 모든 3개의 측면들일 수 있다. 따라서, 단 하나의 채널 영역(114)이 아닌 3개의 채널 영역들(114)이 상부와 측면들에 형성될 수 있다. 보디(118)의 측벽(120)에서의 채널 영역(114)을 포함하는 채널 영역(114)은 여기에서는 게이트 전극(106) "아래(under)"라고 한다. 게이트 전극(106)은 보디(118)의 측벽(120)에서 채널 영역(114)에 수평으로 인접하지만, 그럼에도 이들은 게이트 전극(106) "아래"라고 간주되며, 그렇게 기술하고 청구한다. 보디(118)의 3개의 측면들 상에 게이트 전극(106)을 갖는 이러한 장치(100)는 3개의 채널 영역들(114)을 생성하여 트리게이트 장치(tri-gate device)(100)라고 할 수 있다. 게이트 전극(106)은 또한, 보디(118) 및 인접 STI 영역(117)과 어느 정도 컨포멀할(conformal) 수 있으며, 하드 마스크 층(108)은 도 1b에 도시한 바와 같이, 게이트 전극(106)과 컨포멀할 수 있다.
- <31> 보디(118)는 STI 영역(117)의 상부로부터 게이트 전극(106)의 중앙 부분 아래, 보디(118)의 상부까지 측정된 높

이(152)를 가질 수 있다. 보디(118)는 또한, 보디(118)의 비 리세스 부분(non-recessed portion)에서 측정된 폭(156)을 가질 수 있다(즉, A-A 라인이 통과하는 보디(118)의 부분에서 측정되고, B-B 또는 C-C 라인이 통과하는 보디(118)의 부분들의 상부에서 측정되지 않음, 여기서 보디(118)는 이들 부분들에서 리세스됨). 게이트 전극(106)은 보디(118)의 상부로부터 게이트 전극(106)의 상부까지 측정된 높이(154)를 가질 수 있다. STI 영역(117)은 STI 영역(117)의 상부로부터 그 하부 경계까지 측정된 깊이(158)를 갖는다. STI 영역(116)의 깊이는 STI 영역(117)의 깊이(158)와 사실상 같을 수 있다.

- <32> 일 실시예에서, STI 영역들의 깊이(158)는 약 보디(118)의 높이(152)의 2배일 수 있다. 다른 실시예에서, STI 영역들의 깊이(158)는 보디(118)의 높이(152)의 2배보다 크거나 대략 동등할 수 있다. 다른 실시예에서, STI 영역들의 깊이(158)는 보디(118)의 높이(152)의 약 1.8배와 보디(118)의 높이(152)의 약 2.2배 사이에 있을 수 있다.
- <33> 게이트 전극(106)의 높이(154)는 일 실시예에서, 보디(118)의 높이(152)의 약 2배일 수 있다. 게이트 전극(106)의 높이(154)는 일 실시예에서, 보디(118)의 높이(152)의 약 2배 이상일 수 있다. 게이트 전극(106)의 높이(154)는 일 실시예에서, 보디(118)의 높이(152)의 약 3분의 2 이상 클 수 있다. 또 다른 실시예에서, 게이트 전극(106)의 높이(154)는 보디(118)의 높이(152)의 약 1.8배와 보디(118)의 높이(152)의 약 2.2배 사이에 있을 수 있다. 또 다른 실시예에서, 게이트 전극(106)의 높이(154)는 보디(118)의 높이(152)의 약 1.5배와 보디(118)의 높이(152)의 약 2배 사이에 있을 수 있다. 또 다른 실시예에서, 게이트 전극(106)의 높이(154)는 보디(118)의 높이(152)의 약 1.5배와 보디(118)의 높이(152)와 대략 동등한 사이에 있을 수 있다. 다른 실시예에서, 게이트 전극(106)의 높이(154)는 더 작거나 클 수 있다.
- <34> 보디(118)의 높이(152)는 일 실시예에서, 보디(118)의 폭(156)의 약 2배일 수 있다. 다른 실시예에서, 보디(118)의 높이(152)는 보디(118)의 폭(156)의 2배보다 클 수 있다. 다른 실시예에서, 보디(118)의 높이(152)는 보디(118)의 폭(156)의 약 1.8배와 보디(118)의 폭(156)의 약 2.2배 사이에 있을 수 있다. 보디(118)의 높이(152)와 보디(118)의 폭(156)의 다른 크기들이 다른 실시예들에서 사용될 수 있다. 일부 실시예들에서, 보디(118)의 폭(156)은 채널 영역들(114)이 동작중 사실상 완전하게 공핍되도록 선택될 수 있다. 따라서 일부 실시예들에서, 기판(102)이 고농도로(highly) 도핑되는 경우, 폭(156)은 더 작게 되어 사실상 완전 공핍될 수 있다.
- <35> 일 실시예에서, 보디(118)는 약 20나노미터의 폭(156)과 약 40나노미터의 높이(152)를 가질 수 있으며, 게이트 전극(106)의 높이(154)는 적어도 40나노미터이고, STI 영역(116, 117)의 깊이(158)는 적어도 40나노미터일 수 있다. 일 실시예에서, STI 영역(116, 117)의 깊이(158)는 보디(118)의 높이(152)의 약 2배와 보디(118)의 높이(152)의 약 3배 사이에 있을 수 있지만, 다른 실시예들에서, STI 영역(116, 117)은 다른 깊이를 가질 수 있다. 다른 실시예에서, 게이트 전극(106)의 높이(154)는 약 30나노미터일 수 있고, 보디(118)의 폭(156)은 약 20나노미터와 약 40나노미터 사이에 있을 수 있다. 일부 실시예들에서, 보디(118)의 높이(152)는 약 20나노미터와 약 100나노미터 사이에 있을 수 있다. 일부 실시예들에서, 보디(118)의 폭(156)은 약 10나노미터와 약 50나노미터 사이에 있을 수 있다. 또 다른 실시예들에서, 장치(100)의 구조는 다른 크기를 가질 수 있다.
- <36> 도 1c는 본 발명의 일 실시예의 반도체 장치(100)를 나타내는 도 1a의 B-B 라인을 따라 취한 측 단면도이다. 도 1c에 도시한 바와 같이, 핀(118)은 모든 3개의 측면들(상부면 및 2개의 측면)에서 리세스 예정되고, 예정은 스페이서(110) 아래에서 아랫부분을 잘라낸다(undercut). 소스 및 드레인 재료(112)는 핀(118)의 모든 3개의 측면들 상에 있으므로, 핀(118)의 모든 3개의 측면들에 스트레스를 인가할 수 있다. (도 1c에 도시한 바와 같이, 하드 마스크(108)는 스페이서(110) 뒤에서 볼 수 있는데, B-B 선을 통한 단면은 하드 마스크(108)를 절단하지 않음을 지적한다.)
- <37> 도 1d는 본 발명의 일 실시예의 반도체 장치(100)를 나타내는 도 1a의 C-C 라인을 따라 취한 측 단면도이다. 도 1d에서 볼 수 있는 바와 같이, 스페이서(110) 아래로 핀(118)의 더 적은 부분이 에칭 제거되는 도 1c와는 반대로 핀(118)의 더 많은 부분이 스페이서(110)로부터 에칭 제거된다. 파선(124)은 보디(118)에 리세스들을 형성하도록 에칭 제거되기 이전의 핀(118)의 최초 경계를 나타낸다. 도 1d에 도시한 실시예에서, 소스 및 드레인 재료(112)는 핀(118)의 리세스들에 형성되고, 또한, 핀(118)의 이전 경계(124)를 넘어 또한 연장한다. 또한, 일 실시예에서, 핀(118)의 모든 3개의 측면들 상에 리세스들이 있고, 모든 3개의 측면들(118) 위에 소스 및 드레인 재료(112)가 있을 수 있고, 이 3개의 측면들은 모든 3개의 채널 영역들(114)에 스트레스를 인가할 수 있다. (도 1d에서, 하드 마스크(108) 및 스페이서(110)를 소스 및 드레인 재료(112) 뒤에서 볼 수 있는데, C-C 라인을 통한 단면은 하드 마스크(108) 또는 스페이서(110)를 절단하지 않음을 지적한다.) 게이트 전극(106)의 높이(154)가 보디(118)의 높이(152)보다 적은 일부 실시예들에서, 소스/드레인 영역들(130/132)로부터 게이트 전

극(106)을 분리하는 스페이서(110)의 형성으로 핀(118)의 측면들 내에 리세스들이 제한될 수 있다. 이러한 실시예들에서, 소스/드레인 재료(112)의 대부분은 보디(118)의 상부에 있을 수 있다.

- <38> 도 1e는 본 발명의 다른 실시예의 반도체 장치(100)를 나타내는 도 1a의 C-C 라인을 통해 취한 측 단면도이다. 도 1e의 실시예에 있어서, 핀(118)이 도 1d의 실시예에서보다 더 많이 에칭 제거되어 더 깊은 리세스들을 형성한다. 소스 및 드레인 재료(112)는 리세스내에서 성장되지만, 이 실시예에서 핀(118)의 최초 경계를 넘어 연장하지 않는다. (다른 실시예들에서, 소스 및 드레인 재료(112)는 도 1e에 도시된 한계를 넘어 연장할 수 있음을 지적한다.) 모든 3개의 측면(118)의 소스 및 드레인 재료(112)는 스트레스를 모든 3개의 채널 영역(114)에 인가할 수 있다. (도 1e에서, 소스 및 드레인 재료(112) 뒤의 하드 마스크(108) 및 스페이서(110)는 생략되었다.)
- <39> 도 2 내지 도 12는 일 실시예에 따른 도 1의 장치(100)의 형성에 있어서, 단계들을 나타낸다.
- <40> 도 2는 장치(100)가 일 실시예에 따라 형성될 수 있는 기판(102)을 나타내는 측 단면도이다. 기판(102)은 장치(100)가 형성될 수 있는 임의의 적합한 재료를 포함할 수 있다. 일 실시예에서, 기판(102)은 벌크 단결정 실리콘 재료일 수 있다(즉, SOI 기판이 아니므로, 매몰 산화물 층을 갖지 않음). 이러한 실시예에서, 소스 및 드레인 재료(112)의 리세스들은 매몰 산화물 층이 위치한 깊이로 제한되기 보다는 소망되는 만큼 깊게 형성될 수 있다. 이로써 채널 영역(114)에 더 깊은 리세스들 및 더 큰 스트레스들이 적용되어 성능을 개선할 수 있다. 다른 실시예들에서, 갈륨 아세나이드(gallium arsenide) 같은 다른 반도체 재료들 또는 다른 재료 가 사용될 수 있다.
- <41> 도 3은 STI 영역(116, 117)이 형성된 후의 기판(102)을 나타내는 측 단면도이다. 일 실시예에서, 기판(102)의 부분들은 보호될 수 있으며, 보호되지 않은 부분들은 트렌치들을 형성하도록 제거될 수 있으며, STI 사용을 위해 적합한 재료가 트렌치들내에 증착될 수 있다. 전방 및 후방의 STI 영역(116) 및 측방의 STI 영역(117) 모두는 일부 실시예들에서 동시에 형성될 수 있다. 전방 및 후방의 STI 영역(116)이 형성된 트렌치들 사이의 간격은 핀(118)의 길이(150)를 규정하고, 측방의 STI 영역(117)이 형성된 트렌치들 사이의 간격은 핀(118)의 폭(156)을 규정할 수 있다. STI 영역(116, 117)의 깊이는 보디(118)의 소정의 높이(152) 및 소정의 STI 깊이(158)를 기반으로 선택될 수 있다.
- <42> 도 4는 일 실시예에 따른 STI 영역(116, 117)이 제거되어 핀(118)을 형성한 후의 장치(100)를 나타내는 측 단면도이다. 일 실시예에서, STI 영역(116, 117)의 부분들은 플루오르화 수소산(hydrofluoric acid)으로 제거될 수 있다. 다른 실시예들에서, RIE 건식 에칭(RIE dry etching) 등의 다른 방법들이 사용될 수 있다. 제거된 최초 STI 영역(116, 117)의 양은 몇몇 실시예들에서 보디의 높이(152)를 결정할 수 있다. 따라서, 제거된 처음에 존재한 STI 영역(116, 117)의 양은 보디(118)의 소정의 높이(152)를 기반으로 결정될 수 있다. STI 영역(116, 117)의 나머지 양은 STI 영역(116, 117)의 깊이(158)를 결정한다. 따라서, STI 영역(116, 117)의 부분 제거 후, 기판(102) 및 STI 영역(116, 117) 나머지 이상을 연장하는 보디 또는 핀(118)이 규정된다.
- <43> 도 3을 참조하여 전술한 바와 같이, 도 3에 도시된 STI 영역(116, 117)의 최초 깊이는 보디(118)의 소정의 높이(152) 및 소정의 STI 영역(116, 117)의 깊이(158)를 기초로 선택될 수 있다. STI 영역(116, 117)의 최초 깊이는 핀(118)의 형성후, 보디의 높이(152) 및 STI 영역(116, 117)의 깊이(158) 모두를 포함하므로, STI 영역(116, 117)의 최초 깊이는 보디(118)의 결합 높이(combined height)(152) 및 STI 영역(116, 117)의 깊이와 적어도 동일하게 되도록 선택된다. 일 실시예에서, STI 영역(116, 117)은 보디(118)의 적어도 약 2배의 높이(152)의 깊이(158)를 가질 수 있다. 일 실시예에서, 도 3에 도시한 바와 같이, STI 영역(116, 117)의 최초 깊이는 약 1500옹스트롬(Å)일 수 있다. 도 4에 도시한 바와 같이, 핀(118)의 형성후, 핀(118)은 약 500옹스트롬의 높이(152)를 가질 수 있으며, STI 영역(116, 117)은 약 1000옹스트롬의 깊이(158)를 가질 수 있다. 다른 실시예에서, 도 3에 도시한 바와 같이, STI 영역(116, 117)의 최초 깊이는 약 1000옹스트롬과 약 3000옹스트롬 사이에 있을 수 있다. 또 다른 실시예에서, STI 영역(116, 117)의 최초 깊이는 다를 수 있다. 도 4에 도시한 바와 같이, 핀(118)의 형성후, 핀(118)은 최초 깊이의 약 1/3 또는 그 이하의 높이(152)를 가질 수 있으며, STI 영역(116, 117)은 최초 깊이의 약 2/3 또는 그 이상의 깊이(158)를 가질 수 있다. 다른 실시예에서, STI 영역(116, 117)의 깊이(158)에 관해 표현된 핀(118)의 높이(152)의 크기는 다를 수 있다.
- <44> 도 5는 일 실시예에 따른 STI 영역(116, 117)의 부분의 제거에 의해 형성 후의 핀(118)을 나타내는 사시도이다. 전방 및 후방의 STI 영역(116) 및 측방의 영역(117)은 STI 영역(116, 117) 위로 돌출하는 핀(118)을 둘러쌀 수 있다. 보디(118)는 STI 영역(116, 117)을 통해 기판(102)의 나머지까지 하향 연장(extend down)할 수 있다. 파선(125)은 기판(102)의 다른 영역들과 만나게 연장할 때, STI 영역(116, 117)의 상부면 아래의 보디(118)의 경계를 도시한다. 또한, 도 5에 핀(118)의 길이(150), 핀의 폭(156), 핀(118)의 높이(152) 및 STI 영역(116,

117)의 깊이(158)가 도시되어 있다. 핀(118)이 STI 영역(116, 117)과 만나는 점에서보다 상부에서 다소 덜 길고 덜 넓은 것을 지적한다; 도면들은 이상적인 표현을 도시한다. 몇몇 실시예에서, 이러한 테이퍼링(tapering)은 측벽을 곧게 유지하도록, 실행가능한 한 방지된다.

- <45> 도 6은 일 실시예에 따르면, 보디(118) 및 STI 영역(116, 117)의 표면들 상에 형성된 게이트 유전(104) 재료 층을 도시하는 측 단면도이다. 게이트 유전층(104) 재료는 임의의 적합한 형태의 유전 재료를 포함할 수 있다.
- <46> 도 7은 게이트 유전층(104) 재료 상에 증착된 게이트 전극(106)을 형성하는 재료 층을 나타내는 측 단면도이다. 일부 실시예들에서, 게이트 전극(106)을 형성하는 재료 층은 단일 재료의 단일 층을 포함할 수 있다. 다른 실시예에서, 다수의 다른 재료들이 사용될 수 있고, 다수의 재료 층들이 있을 수 있다. 따라서, 몇몇 실시예들에서, 단일 층으로서만 도시하지만, 게이트 전극(106)은 다수의 다른 재료 층들을 포함할 수 있으며, 여기서는 단일 재료 층으로서만 언급되지만, 실제로 다수의 층들을 포함할 수 있다. 게이트 전극(106)은 임의의 적합한 게이트 전극 재료로 형성될 수 있다. 일 실시예에서, 게이트 전극(106)은 도핑될 수 있는 폴리실리콘을 포함할 수 있다. 다른 실시예에서, 게이트 전극(106)은 금속 층상의 폴리실리콘 층을 포함할 수 있다. 또 다른 실시예에서, 게이트 전극(106)은 다른 재료 층들을 포함할 수 있으며, 2 이상의 층들을 포함할 수 있다. 게이트 전극(106)을 형성하는 재료 층은 일 실시예에서, 보디(118)의 높이(152)의 적어도 약 2배 정도만큼 큰 두께를 가질 수 있는데, 다른 실시예들에서는 다른 두께를 가질 수 있다. 게이트 전극(106)을 형성하는 재료 층은 컨포멀하게 증착될 수 있다.
- <47> 도 8은 본 발명의 일 실시예에 따라 게이트 전극(106) 재료상에 형성된 하드 마스크 층(108)을 나타내는 측 단면도이다. 하드 마스크(108)는 제자리에 남기는 것이 소망되는 게이트 전극(106) 재료 및 게이트 유전(104) 재료의 영역들을 보호하면서, 제거가 소망되는 영역들을 노출하도록 패턴화될(patterned) 수 있다. 게이트 전극(106) 재료 및 게이트 유전(104) 재료의 노출 영역들은 임의의 적합한 방법으로 제거될 수 있다.
- <48> 도 9는 일 실시예에 따라 하드 마스크(108)가 패턴화되고, 제거가 소망되는 게이트 전극(106) 재료 및 게이트 유전(104) 재료 영역의 제거후의 장치(100)를 나타내는 사시도이다. 게이트 유전층(104), 게이트 전극(106) 및 하드 마스크 층(108)은 보디(118)의 모든 3개의 측면들(상부 및 측벽들)에 인접하게 보일 수 있다. 간략화를 위해, 게이트 유전층(104), 게이트 전극(106) 및 하드 마스크 층(108)은 각각 도시하지 않음을 지적한다. 모든 3개의 측면들에 인접한 게이트 전극을 가짐으로써 장치(100)의 유효 게이트 폭은 보디(118)의 폭(156)에 보디(118)의 높이(152)의 2배를 더한 것이 된다. 간격(160)은 장치(100)의 게이트 길이이다. 일 실시예에서, 간격(160)은 약 10나노미터와 약 50나노미터 사이에 있을 수 있다. 다른 실시예들에서, 간격은 예를 들어, 최대 2 μm 까지 더 클 수 있거나 또는 더 작을 수 있다.
- <49> 도 10은 본 발명의 일 실시예에 따른 스페이서(110)의 형성후의 장치(100)를 나타내는 측 단면도이다. 텅 접합부 형성 등의 추가 프로세스들이 일부 실시예들에서 스페이서들(110)의 형성 이전에 수행될 수 있다. 스페이서(110)의 형성은 임의의 적합한 방법으로 수행될 수 있다. 일 실시예에서, 스페이서(110) 재료 층은 장치(100) 상에 증착될 수 있다. 이 재료는 실리콘 질화물, 실리콘 이산화물 또는 다른 재료 등의 임의의 적합한 재료를 포함할 수 있다. 이어서 스페이서(110) 재료 층의 부분들이 제거되어 게이트 유전층(104), 게이트 전극(106) 및 하드 마스크(108)에 인접한 스페이서(110)를 남겨두지만, 사실상 보디(118)가 STI 영역(116, 117)뿐만 아니라 다른 영역들과 만나는 위치에 인접한 스페이서(110) 재료 층의 부분들을 제거한다. 이 결과, 스페이서(110)의 상부는 하드 마스크(108)의 상부 아래에 있을 수 있다.
- <50> 도 11은 본 발명의 일 실시예에 따라 리세스(126)가 보디(118) 내에 형성된 후의 장치(100)를 나타내는 측 단면도이다. 리세스(126)는 소스 및 드레인 리세스라할 수 있다. 리세스(126)은 습식 에칭과 같은 임의의 적합한 방법에 의해 형성될 수 있다. 리세스(126)은 일부 실시예들에서 약 50옹스트롬과 약 1000옹스트롬 사이의 게이트 유전층(104)에 인접한 보디(118)의 상부면 이하의 깊이(162)를 가질 수 있는데, 다른 실시예들에서, 다른 깊이(162)가 가능하다. 일 실시예에서, 리세스(126)는 측벽들(110) 아래에서 또한 가능하게는 5나노미터와 약 50나노미터 사이의 간격(164)의 경우에 게이트 유전층(104) 아래에서 수평으로 연장할 수 있는데, 다른 실시예들에서, 이 간격(164)은 다를 수 있다. 기판(102)이 비 SOI 기판인 일부 실시예들에서, 리세스(126)는 SOI 기판에서 가능한 것보다 깊게 만들어질 수 있는데, 이는 SOI 기판에서, 매물 산화물 층의 깊이가 리세스(126)에 대한 최대의 가능한 깊이를 제공하기 때문이다. 리세스(126)가 깊어지면, 채널 영역(114)에 가해지는 스트레스가 커질 수 있으므로, SOI 기반 장치의 낮은 스트레스에서 가질 수 있는 성능보다 개선된 성능이 제공된다.
- <51> 핀(118)의 상부면의 부분들을 제거하는데 사용된 프로세스는 또한, 사용된 프로세스가 일부 실시예들에서 부분적으로 또는 완전하게 등방성(isotropic)일 때, 핀(118)의 측벽들의 부분들을 제거한다. 이러한 제거 프로세스

의 결과는 전술한 바와 같이, 도 1c 내지 1e에 도시될 수 있는데, 핀(118)의 측면들의 부분들이 제거된 것을 게이트 전극(106)으로부터 여러 간격에서 도시한다.

- <52> 도 12는 일 실시예에 따른 소스 및 드레인 재료(112)가 리세스(126) 내에 형성된 후의 장치(100)를 나타내는 측면도이다. 소스 및 드레인 재료(112)는 장치(100)에 대한 소스 및 드레인으로서 또는 장치(100)의 소스 및 드레인의 일부로서 동작할 수 있다. 일 실시예에서, 소스 및 드레인 재료(112)는 실리콘 게르마늄(SiGe), 실리콘 카바이드(SiC), 니켈 실리사이드(NiSi), 티타늄 실리사이드(TiSi₂), 코발트 실리사이드(CoSi₂) 또는 다른 재료를 포함할 수 있다.
- <53> 일 실시예에서, 기판(102)은 격자 구조(예를 들어, 저심(base centered) 입방체 또는 다른 격자 구조) 및 격자 간격을 갖는 재료를 포함한다. 소스 및 드레인 재료(112)는 기판(102)의 재료와 같은 격자 구조를 가질 수 있지만, 다른 격자 간격을 가질 수 있다. 이 다른 격자 간격의 결과 장치(100)의 채널 영역(114) 내에 스트레스가 생성될 수 있다. 소스 및 드레인 재료(112)가 기판(112) 재료보다 큰 격자 간격을 가지면, 채널 영역(114) 내에 압축 스트레스(170)가 유도될 수 있다. 소스 및 드레인 재료(112)가 기판(112) 재료보다 작은 격자 간격을 가지면, 채널 영역(114) 내에 인장 스트레스(도시 않음)가 유도될 수 있다. 따라서, 소스 및 드레인 재료(112)에 의해 장치(100)의 채널(114) 영역들 내에 스트레스가 유도되므로, 이 재료를 또한 스트레스 재료(112)라 할 수 있다.
- <54> 일 실시예에서, 기판(102)은 단결정 실리콘을 포함할 수 있고, 리세스(126) 내의 소스 및 드레인 재료(112)는 실리콘보다 큰 격자 간격을 갖는 실리콘 게르마늄을 포함할 수 있다. 이 실시예에서, SiGe 스트레스 재료는 채널 영역(114) 내에 압축 스트레스(170)를 유도하여 PMOS 장치(100)의 성능을 개선할 수 있다. 다른 실시예들에서, 스트레스 재료(112)에 의해 채널 영역(114) 내에 인장 스트레스가 유도될 수 있어서 NMOS 장치(100)의 성능을 개선할 수 있다. 핀(118)의 상부면뿐만 아니라 핀(118)의 측면들에 리세스(126)가 형성될 수 있고, 스트레스 재료가 핀(118)의 측면들과 상부 양쪽 상의 리세스(126)에 형성될 수 있으므로, 모든 3개의 채널 영역(114)에 스트레스가 가해질 수 있다.
- <55> 일 실시예에서, 스트레스 재료(112)는 에피택시 방식으로(epitaxially) 형성될 수 있지만, 다른 프로세스들이 사용될 수도 있다. 에피택시 방식으로 형성된 소스 및 드레인 재료(112)는 도 12에 도시한 바와 같이, 핀(118)을 포함하도록 사용된 양 이상으로 확장할 수 있다. 다른 실시예들에서, 스트레스 재료(112)는 사실상 핀(118)의 상부면과 동일 평면상에 있을 수 있다.
- <56> 일부 실시예들에서, 소스 드레인 재료(112)는 그것이 형성될 때 도핑될 수 있다. 예를 들어, 스트레스 재료(112)가 에피택시 방식으로 형성된 SiGe를 포함하는 일 실시예에서, 도펀트는 그것이 성장될 때 SiGe 내에 포함될 수 있다. 이러한 실시예에서, 이온 주입 또는 애닐링(annealing) 단계는 필요치 않을 수 있다. 다른 실시예들에서, 소스 및 드레인 재료(112)가 형성된 후 소스 및 드레인 재료를 장치(100)의 소스 및 드레인으로 변형(transform)하기 위해 이온들이 소스 및 드레인 재료(112)에 주입될 수 있다.
- <57> 추가의 프로세스 단계가 수행되어 이 기술의 통상의 기술자라면 인식하게 되는 바와 같이 장치(100)를 완성할 수 있다.
- <58> 도 13은 본 발명의 일 실시예에 따른 시스템(1300)을 나타내는 블록도이다. 스트레스 재료(112)를 갖는 하나 이상의 멀티게이트 장치(100)에 의해 도 13의 시스템(1300) 내에 포함될 수 있는 전술한 바와 같은 채널 영역(114)에 스트레스가 유도된다. 도시한 바와 같이, 이 실시예의 경우에, 시스템(1300)은 데이터를 처리하기 위한 연산 장치(computing device)(1302)를 포함한다. 연산 장치(1302)는 마더보드(1304)를 포함할 수 있고, 특히, 버스(1310)에 결합된 네트워크 인터페이스(1308) 및 프로세서(1306)는 마더보드(1304)에 결합되거나 또는 마더보드의 일 부분일 수 있다. 칩셋은 버스(1310)의 일부 또는 모두를 형성할 수 있다. 프로세서(1306), 칩셋 및/또는 시스템(1300)의 다른 부분들은 전술한 바와 같이 하나 이상의 장치(100)를 포함할 수 있다.
- <59> 응용에 따라, 시스템(1300)은 환경은 아니지만, 휘발성 및 비휘발성 메모리(1312), 그래픽 프로세서(마더보드(1304)와 일체로 되거나 AGP 또는 PCI-E 그래픽 프로세서 등과 같은 각각 제거가능한 부품으로서 마더보드에 접속됨), 디지털 신호 처리기(digital signal processor), 크립토 프로세서(crypto processor), 대용량 저장 장치(1314)(하드 디스크, 콤팩트 디스크(CD), 디지털 다기능 디스크(digital versatile disk: DVD) 및 그 밖의 것 등), 입력 및/또는 출력 장치(1316) 등등을 포함한 다른 부품들을 포함할 수 있다.
- <60> 여러 실시예들에서, 시스템(1300)은 개인 휴대정보 단말기(personal digital assistant; PDA), 이동 전화(mobile phone), 태블릿(tablet) 연산 장치, 랩탑 연산 장치, 데스크탑 연산 장치, 셋톱 박스, 엔터테인먼트 제

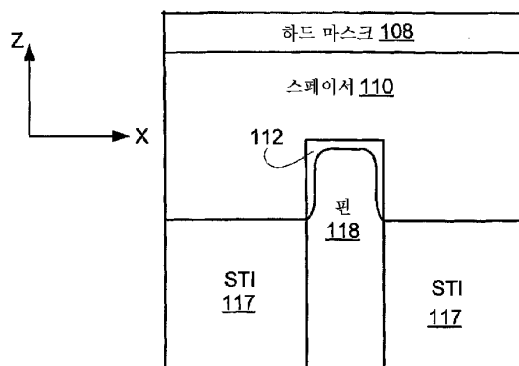
어 장치(entertainment control unit), 디지털 카메라, 디지털 비디오 레코더, CD 플레이어, DVD 플레이어 또는 동류의 다른 디지털 장치일 수 있다.

- <61> 도 13의 하나 이상의 부품(1306, 1314 등) 중 임의의 것은 여기에 기술한 하나 이상의 장치(100)를 포함할 수 있다. 예를 들어, SiGe 스트레스 재료(112)를 갖는 트리게이트 트랜지스터(100)는 CPU(1306), 마더보드(1304), 그래픽 프로세서, 디지털 신호 처리기 또는 다른 장치의 일부일 수 있다.
- <62> 본 발명의 실시예들의 기술한 설명은 예시 및 설명의 목적으로 제공되었으며, 본 발명이 기술한 것과 같은 형태만이라거나 이 형태로 한정하고자 하는 것은 아니다. 이 설명 및 이하의 청구범위는 좌측, 우측, 상부, 하부, 위에, 아래에, 위쪽, 아래쪽, 제1, 제2 등의 용어를 포함하는데, 그것들은 설명의 목적으로만 사용되고, 한정으로 해석되지 않아야 한다. 예를 들어, 상대적 수직 위치를 가리키는 용어들은 기관 또는 집적회로의 장치 쪽 (또는 활성 표면(active surface))이 그 기관의 "상부" 면인 상황을 참조하고, 기관은 실제로 임의의 방향(orientation)에 있을 수 있어서, 기관의 "상부" 쪽이 표준 지구 좌표계(standard terrestrial frame of reference)에서 "하부" 쪽보다 낮으면서 용어 "상부"의 의미 내에 포함될 수 있다. 여기에서(청구범위 포함) 사용된 "위에"라는 용어는 그것이 특히 명시되지 않는 한 제2 층 "위의" 제1층이 제2층의 바로 "위에" 또한 제2 층과 바로 접촉하는 것을 나타내지 않으며, 제1 층과 제1 층 위의 제2 층 사이에 제3 층 또는 다른 구조가 있을 수 있다. 여기에서 기술한 장치 또는 물품의 실시예들은 여러 위치 및 방향으로 제조, 사용 및 출하될 수 있다. 관련 기술의 통상의 기술자라면, 위의 교시를 기반으로 여러 많은 변형 및 변경들이 가능함을 인식할 것이다. 이 기술의 통상의 기술자라면, 도면에 도시한 여러 부품들에 대한 여러 등가의 조합 및 대체를 인식할 것이다. 따라서 본 발명의 영역은 이 상세한 설명이 아니라 첨부된 청구범위로 한정되도록 의도됨을 지적한다.

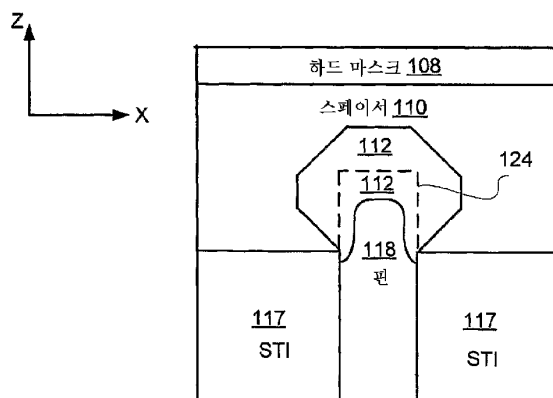
도면의 간단한 설명

- <2> 도 1a 내지 1e는 본 발명의 일 실시예의 반도체 장치를 나타내는 단면도이다.
- <3> 도 2는 이 장치가 형성될 수 있는 기관을 나타내는 측 단면도이다.
- <4> 도 3은 STI 영역들이 내부에 형성된 후의 기관을 나타내는 측 단면도이다.
- <5> 도 4는 STI 영역들의 부분들이 핀(fin)을 형성하도록 제거된 후의 장치를 나타내는 측 단면도이다.
- <6> 도 5는 핀 형성 후의 핀을 나타내는 사시도이다.
- <7> 도 6은 보디 및 STI 영역들의 표면들상에 형성된 게이트 유전 재료 층을 나타내는 측 단면도이다.
- <8> 도 7은 게이트 유전 재료상에 증착된 게이트 전극을 형성하는 재료 층을 나타내는 측 단면도이다.
- <9> 도 8은 게이트 전극 재료 상에 형성된 하드 마스크 층을 나타내는 측 단면도이다.
- <10> 도 9는 하드 마스크의 패터닝 및 게이트 전극 재료 및 게이트 유전 재료의 영역들의 제거 후 장치를 나타내는 사시도이다.
- <11> 도 10은 스페이서들의 형성 후 장치를 도시하는 단면도이다.
- <12> 도 11은 리세스들이 보디에 형성된 후의 장치를 나타내는 측 단면도이다.
- <13> 도 12는 소스 및 드레인 재료가 리세스들 내에 형성된 후의 장치를 나타내는 측 단면도이다.
- <14> 도 13은 본 발명의 일 실시예에 따른 시스템을 나타내는 블록도이다.

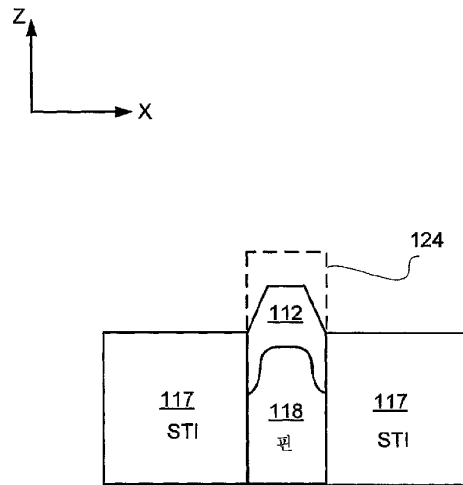
도면1c



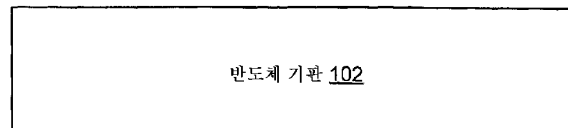
도면1d



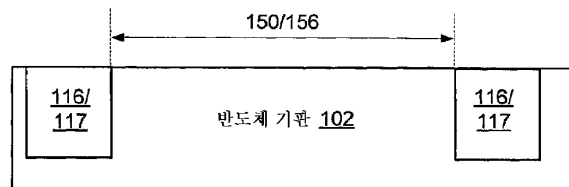
도면1e



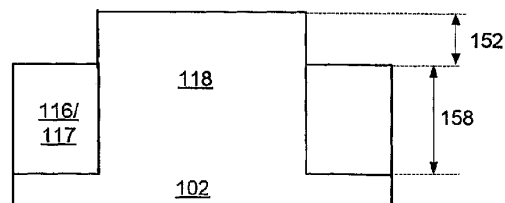
도면2



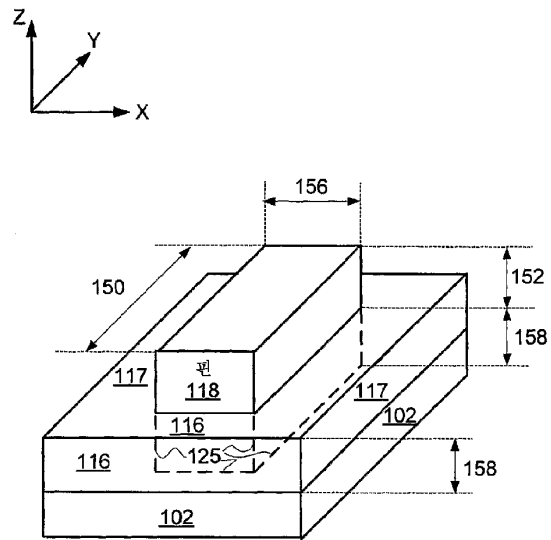
도면3



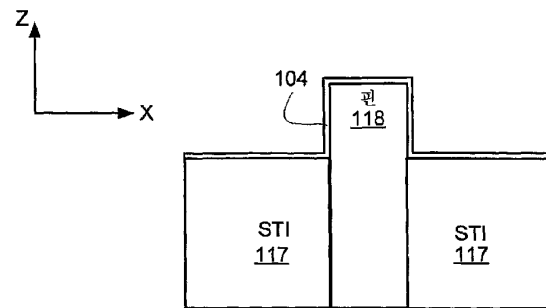
도면4



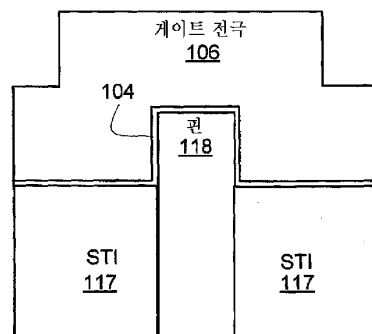
도면5



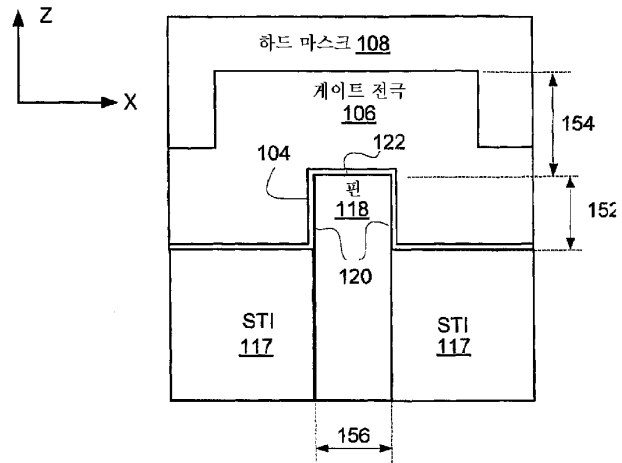
도면6



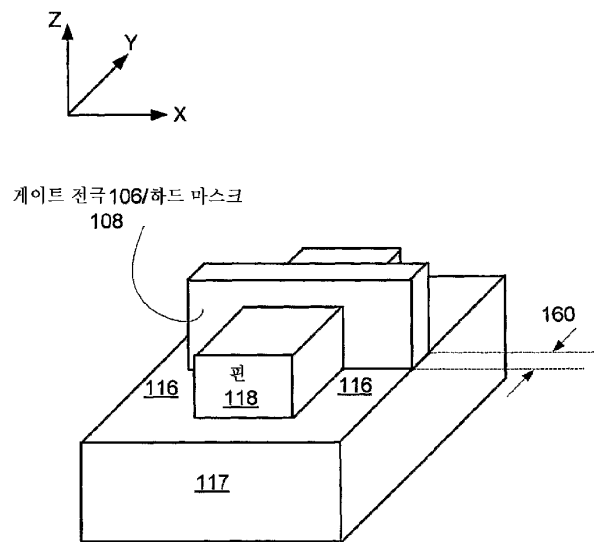
도면7



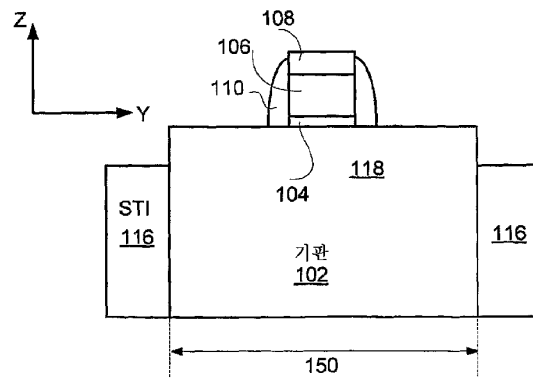
도 158



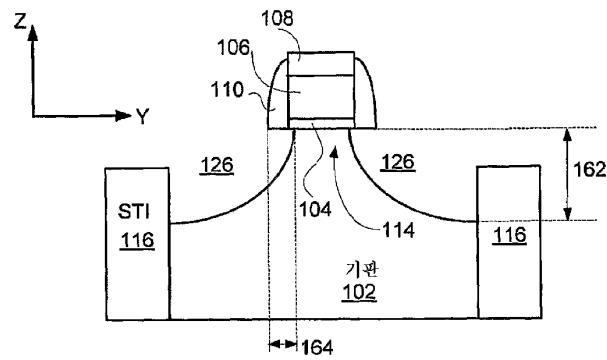
도 159



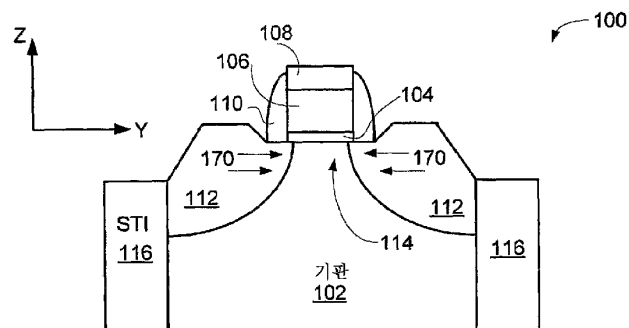
도면10



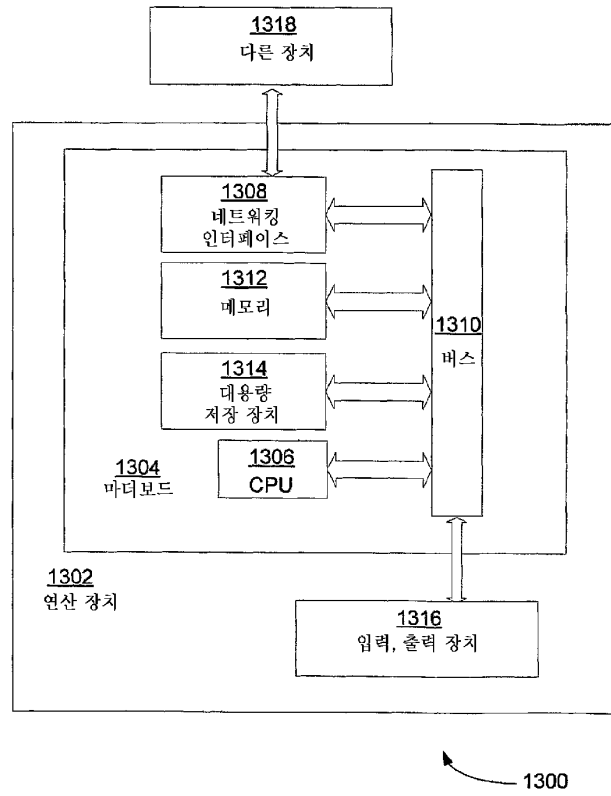
도면11



도면12



도면13



Electronic Acknowledgement Receipt	
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Application Number:	16881541
International Application Number:	
Confirmation Number:	8383
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Customer Number:	164
Filer:	Ian David MacKinnon
Filer Authorized By:	
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2021-10-15_SIDS_D480-012044.pdf	1035047 75b11174e8d9c012946167b295dd462c720ffddb	no	4

Warnings:

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Information:					
Total Files Size (in bytes):			8175692		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

164 7590 11/02/2021
KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

EXAMINER

ERDEM, FAZLI

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 11/02/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/881,541	05/22/2020	Glenn A. GLASS	D480-012044	8383

TITLE OF INVENTION: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	02/02/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

164 7590 11/02/2021
KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/881,541	05/22/2020	Glenn A. GLASS	D480-012044	8383

TITLE OF INVENTION: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	02/02/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
ERDEM, FAZLI	2826	257-190000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/881,541	05/22/2020	Glenn A. GLASS	D480-012044	8383
164	7590	11/02/2021	EXAMINER	
KINNEY & LANGE, P.A. 312 SOUTH THIRD STREET MINNEAPOLIS, MN 55415-1002			ERDEM, FAZLI	
			ART UNIT	PAPER NUMBER
			2826	
DATE MAILED: 11/02/2021				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/881,541	Applicant(s) GLASS et al.	
	Examiner FAZLI ERDEM	Art Unit 2826	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to RCE filed on 10/8/2021.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 2-21. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>10/8/2021, 10/15/2021</u> .	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	

/FAZLI ERDEM/ Primary Examiner, Art Unit 2826	
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DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 10/8/21 has been entered.

Allowable Subject Matter

1. Claims 2-21 are allowed.
2. The following is an examiner's statement of reasons for allowance:
3. Regarding Claim 2, prior art failed to disclose or fairly suggest an integrated circuit structure comprising, along with other recited claim limitations,
4. a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium; a first contact plug in the first opening and on the first germanide layer; and a

second contact plug in the second opening and on the second germanide layer. Claims 3-8 depend from claim 2 and hence are allowed for the same reason therein.

5. Regarding Claim 9, prior art failed to disclose or fairly suggest an integrated circuit structure comprising, along with other recited claim limitations,

6. a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium; a first contact plug in the first opening and on the first germanide layer; and a second contact plug in the second opening and on the second germanide layer. Claims 10-12 depend from claim 9 and hence are allowed for the same reason therein.

7. Regarding Claim 13 prior art failed to disclose or fairly suggest an integrated circuit structure comprising, along with other recited claim limitations, a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium; a first contact plug in the first opening and on the first germanide layer; and a second contact plug in the second opening and on the second germanide layer. Claims 14-21 depend from claim 13 and hence are allowed for the same reason therein.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to FAZLI ERDEM whose telephone number is (571)272-1914. The examiner can normally be reached on M-F, 8am-5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access

Application/Control Number: 16/881,541
Art Unit: 2826

Page 5

to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826
10/23/2021

Issue Classification 	Application/Control No. 16/881,541	Applicant(s)/Patent Under Reexamination GLASS et al.
	Examiner FAZLI ERDEM	Art Unit 2826

CPC						
Symbol				Type	Version	
H01L	/	29	/	45	F	2013-01-01
H01L	/	29	/	66795	I	2013-01-01
H01L	/	29	/	7848	I	2013-01-01
H01L	/	29	/	785	I	2013-01-01
H01L	/	29	/	66636	I	2013-01-01
H01L	/	29	/	7833	I	2013-01-01
H01L	/	29	/	0847	I	2013-01-01
H01L	/	29	/	165	I	2013-01-01
H01L	/	21	/	28525	I	2013-01-01
H01L	/	21	/	28518	I	2013-01-01
H01L	/	29	/	66545	I	2013-01-01
H01L	/	21	/	76805	I	2013-01-01
H01L	/	21	/	76843	I	2013-01-01
H01L	/	21	/	76864	I	2013-01-01
H01L	/	21	/	76895	I	2013-01-01
H01L	/	29	/	7851	I	2013-01-01

CPC Combination Sets						
Symbol			Type	Set	Ranking	Version
	/		/			

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/FAZLI ERDEM/ Primary Examiner, Art Unit 2826	23 October 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	2	5F

Issue Classification 	Application/Control No. 16/881,541	Applicant(s)/Patent Under Reexamination GLASS et al.
	Examiner FAZLI ERDEM	Art Unit 2826

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L	/	21	/ 28
H01L	/	29	/ 45
H01L	/	29	/ 66
H01L	/	29	/ 78
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
257	190

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE (Assistant Examiner) (Date)		Total Claims Allowed: 20	
/FAZLI ERDEM/ Primary Examiner, Art Unit 2826 (Primary Examiner)		23 October 2021 (Date)	O.G. Print Claim(s) 2
			O.G. Print Figure 5F

Issue Classification 	Application/Control No. 16/881,541	Applicant(s)/Patent Under Reexamination GLASS et al.
	Examiner FAZLI ERDEM	Art Unit 2826

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	2	10	11	19	20										
2	3	11	12	20	21										
3	4	12	13												
4	5	13	14												
5	6	14	15												
6	7	15	16												
7	8	16	17												
8	9	17	18												
9	10	18	19												

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 20	
/FAZLI ERDEM/ Primary Examiner, Art Unit 2826 (Primary Examiner) _____ (Date) 23 October 2021		O.G. Print Claim(s) 2	O.G. Print Figure 5F

<i>Search Notes</i> 	Application/Control No. 16/881,541	Applicant(s)/Patent Under Reexamination GLASS et al.
	Examiner FAZLI ERDEM	Art Unit 2826

CPC - Searched*		
Symbol	Date	Examiner
H01L21/28, 28518, 28525, 76, 76805, 76843, 76864, 76895	7/3/2021	FE
H01L29/45, 0847, 165, 66, 66545, 66636, 66795, 78, 7833, 7848, 785, 7851	7/3/2021	FE
H01L21/28, 28518, 28525, 76, 76805, 76843, 76864, 76895	10/23/2021	FE
H01L29/45, 0847, 165, 66, 66545, 66636, 66795, 78, 7833, 7848, 785, 7851	10/23/2021	FE

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	190	7/3/2021	FE
257	190	7/3/2021	FE

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

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<i>Search Notes</i> 	Application/Control No. 16/881,541	Applicant(s)/Patent Under Reexamination GLASS et al.
	Examiner FAZLI ERDEM	Art Unit 2826

Search Notes		
Search Notes	Date	Examiner
Inventors are searched	7/3/2021	FE
Assignee is searched	7/3/2021	FE
Searched 257/190 limited with text	7/3/2021	FE
Searched H01L21/28, 28518, 28525, 76, 76805, 76843, 76864, 76895 limited with text	7/3/2021	FE
Searched H01L29/0847, 45, 165, 66, 66545, 66636, 66795, 78,7833, 7848, 785, 7851 limited with text	7/3/2021	FE
Interference search is conducted	7/3/2021	FE
EAST Search History is attached	7/3/2021	FE
Inventors are searched	10/23/2021	FE
Assignee is searched	10/23/2021	FE
Searched 257/190 limited with text	10/23/2021	FE
Searched H01L21/28, 28518, 28525, 76, 76805, 76843, 76864, 76895 limited with text	10/23/2021	FE
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Interference search is conducted	10/23/2021	FE
Updated EAST Search History is attached	10/23/2021	FE

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<i>Search Notes</i> 	Application/Control No. 16/881,541	Applicant(s)/Patent Under Reexamination GLASS et al.
	Examiner FAZLI ERDEM	Art Unit 2826

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
257	190	7/3/2021	FE
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H01L29	0847, 45, 165, 66, 66545, 66636, 66795, 78, 7833, 7848, 785, 7851	7/3/2021	FE
257	190	10/23/2021	FE
H01L21	28, 28518, 28525, 76, 76805, 76843, 76864, 76895	10/23/2021	FE
H01L29	0847, 45, 165, 66, 66545, 66636, 66795, 78, 7833, 7848, 785, 7851	10/23/2021	FE

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EAST Search History

EAST Search History (Interference)

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L18	8,051	glass.in. or murthy.in. or ghani.in.	US-PGPUB; USPAT	OR	ON	2021/10/23 12:02
L19	1,603	257/190.ccls.	US-PGPUB; USPAT	OR	ON	2021/10/23 12:03
L20	82,594	H01L21/28.cpc. or H01L21/528.cpc. or H01L21/525.cpc. or H01L21/76.cpc. or H01L21/76805.cpc. or H01L21/76843.cpc. or H01L21/76864.cpc. or H01L21/76895.cpc. or H01L29/0847.cpc. or H01L29/45.cpc. or H01L29/66.cpc. or H01L29/66545.cpc. or H01L29/66636.cpc. or H01L29/66795.cpc. or H01L29/78.cpc. or H01L29/7833.cpc. or H01L29/7848.cpc. or H01L29/785.cpc. or H01L29/7851.cpc. or H01L29/165.cpc.	US-PGPUB; USPAT	OR	ON	2021/10/23 12:03
L21	160,018	l17 or l18 or l19 or l20	US-PGPUB; USPAT	OR	ON	2021/10/23 12:03
L22	283	l21 and (germanide same (source or drain or source/drain or s/d) same titanium)	US-PGPUB; USPAT	OR	ON	2021/10/23 12:03
L23	19,866	H01L21/28.cpc. or H01L21/528.cpc. or H01L21/525.cpc. or H01L21/76.cpc. or H01L21/76805.cpc. or H01L21/76843.cpc. or H01L21/76864.cpc. or H01L21/76895.cpc.	US-PGPUB; USPAT	OR	ON	2021/10/23 12:04
L24	1,225	l23 and contact same (source or drain or source/drain or s/d) same trench same etch\$3	US-PGPUB; USPAT	OR	ON	2021/10/23 12:04
L25	19,866	H01L21/28.cpc. or H01L21/528.cpc. or H01L21/525.cpc. or H01L21/76.cpc. or H01L21/76805.cpc. or H01L21/76843.cpc. or H01L21/76864.cpc. or H01L21/76895.cpc.	US-PGPUB; USPAT	OR	ON	2021/10/23 12:04
L27	19	l25 and germanide near10 (source or drain or s/d or source/drain) near10 titanium	US-PGPUB; USPAT	OR	ON	2021/10/23 12:05

L28	433	I24 and contact adj resistance	US- PGPUB; USPAT	OR	ON	2021/10/23 12:05
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10/23/2021 12:05:43 PM

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EAST Search History

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L2	3	("20070145487" "20090242989")	US-PGPUB; USPAT	OR	ON	2021/10/23 16:32

L3	1,704	I1 or I2	US-PGPUB; USPAT	OR	ON	2021/10/23 16:33
L4	421	I3 and (plug or contact) same (s/d or source or drain or source/drain) same (etch\$3)	US-PGPUB; USPAT	OR	ON	2021/10/23 16:33
L5	183	I4 and contact near resistance	US-PGPUB; USPAT	OR	ON	2021/10/23 16:33
L6	49	I5 and germanide	US-PGPUB; USPAT	OR	ON	2021/10/23 16:33
L7	28	I6 and (ge or germanide) near10 (ti or titanium)	US-PGPUB; USPAT	OR	ON	2021/10/23 16:34
L8	21	I6 and (ge or germanide) near10 (ti or titanium) same (trench or cavity or recess or hole or opening)	US-PGPUB; USPAT	OR	ON	2021/10/23 16:34

10/23/2021 4:35:12 PM

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EAST Search History

EAST Search History (Prior Art)

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L2	24,889	glass.in. or murthy.in. or ghani.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 11:24
L3	2,739	257/190.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 11:25
L4	197,628	H01L21/28.cpc. or H01L21/528.cpc. or H01L21/525.cpc. or H01L21/76.cpc. or H01L21/76805.cpc. or H01L21/76843.cpc. or H01L21/76864.cpc. or H01L21/76895.cpc. or H01L29/0847.cpc. or H01L29/45.cpc. or H01L29/66.cpc. or H01L29/66545.cpc. or H01L29/66636.cpc. or H01L29/66795.cpc. or H01L29/78.cpc. or H01L29/7833.cpc. or H01L29/7848.cpc. or H01L29/785.cpc. or H01L29/7851.cpc. or H01L29/165.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 11:28
L5	442,351	l1 or l2 or l3 or l4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 11:28

L6	8	I5 and finfet same (source or drain or source/drain or s/d) same germanide same titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 11:29
L7	219	I5 and finfet and (source or drain or source/drain or s/d) same germanide same titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 11:29
L8	64	I5 and finfet and (source or drain or source/drain or s/d) same germanide near5 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 11:29
L9	50,001	H01L21/28.cpc. or H01L21/528.cpc. or H01L21/525.cpc. or H01L21/76.cpc. or H01L21/76805.cpc. or H01L21/76843.cpc. or H01L21/76864.cpc. or H01L21/76895.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 11:59
L10	25,313	I9 and (etch\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 11:59
L11	2,577	I10 and finfet	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 11:59
L12	655	I11 and (source or drain or source/drain or s/d) same trench same etch\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:00

L13	498	l11 and contact same (source or drain or source/drain or s/d) same trench same etch\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:00
L14	216	l13 and contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:00
L15	155,184	H01L29/0847.cpc. or H01L29/45.cpc. or H01L29/66.cpc. or H01L29/66545.cpc. or H01L29/66636.cpc. or H01L29/66795.cpc. or H01L29/78.cpc. or H01L29/7833.cpc. or H01L29/7848.cpc. or H01L29/785.cpc. or H01L29/7851.cpc. or H01L29/165.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:01
L16	26	l15 and germanide near10 (source or drain or s/d or source/drain) near10 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:02

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EAST Search History

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L3	104	I1 or I2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:41
L4	26	I3 and (contact or source or drain or source/drain) near5 (resistivity or resistance) same (trench or cavity or recess or hole or opening)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:42
L5	25	I4 and (germanium or ge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:42
L6	15	I5 and germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:42
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L10	239	I9 and (contact or source or drain or source/drain) near5 (resistivity or resistance) same (trench or cavity or recess or hole or opening)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:43
L11	47	I10 and (germanium or ge or germanide) near10 (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:43
L12	27	I10 and (hole or opening or trench or cavity or recess) same (germanium or ge or germanide) near10 (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:44
L13	24	I10 and (hole or opening or trench or cavity or recess) same (germanium or ge or germanide) near10 (ti or titanium) same (source or drain or source/drain or s/d)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:44
L14	21	I13 and germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/10/23 12:45

10/23/2021 12:46:15 PM

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BIB DATA SHEET

CONFIRMATION NO. 8383

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
16/881,541	05/22/2020 RULE	257	2826	D480-012044		
APPLICANTS INTEL CORPORATION, Santa Clara, CA; INVENTORS Glenn A. GLASS, Portland, OR; Anand S. MURTHY, Portland, OR; Tahir GHANI, Portland, OR; ** CONTINUING DATA ***** This application is a CON of 16/416,445 05/20/2019 PAT 10700178 which is a CON of 15/339,308 10/31/2016 PAT 10297670 which is a CON of 14/673,143 03/30/2015 PAT 9484432 which is a CON of 13/990,224 05/29/2013 PAT 8994104 which is a 371 of PCT/US2011/054198 09/30/2011 which is a CIP of 12/975,278 12/21/2010 PAT 8901537 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 06/02/2020						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/FAZLI ERDEM/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY OR	SHEETS DRAWINGS 11	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS KINNEY & LANGE, P.A. 312 SOUTH THIRD STREET MINNEAPOLIS, MN 55415-1002 UNITED STATES						
TITLE CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION						
FILING FEE RECEIVED 1720	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees		
				☐ 1.16 Fees (Filing)		
				☐ 1.17 Fees (Processing Ext. of time)		
				☐ 1.18 Fees (Issue)		
				☐ Other _____		
				☐ Credit		

EAST Search History

EAST Search History (Prior Art)

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L34	286	I33 and (source or drain or s/d) same contact near resistance	US- PGPUB; USPAT	OR	ON	2021/10/23 12:10

L35	24	I34 and germanide near10 titanium	US- PGPUB; USPAT	OR	ON	2021/10/23 12:10
L36	7	I34 and germanide near5 titanium	US- PGPUB; USPAT	OR	ON	2021/10/23 12:11
L37	1	I34 and germanide near5 titanium same (opening or trench or hole or cavity or recess)	US- PGPUB; USPAT	OR	ON	2021/10/23 12:12

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Doc code: IDS

PTO/SB/08a (02-18)

Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16881541
	Filing Date	2020-05-22
	First Named Inventor	Glenn A. Glass
	Art Unit	2826
	Examiner Name	Fazli Erdem
	Attorney Docket Number	D480-012044

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	1	Communication Pursuant to Article 94(3) EPC for EP Application No. 19188924.5, Dated October 14, 2021, Pages 9	
	2	First Japanese Search Report for JP Application No. 2019-189786, Dated September 10, 2020, Pages 13	
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Filing Date	2020-05-22
First Named Inventor	Glenn A. Glass
Art Unit	2826
Examiner Name	Fazli Erdem
Attorney Docket Number	D480-012044

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

✓ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ian D. MacKinnon/	Date (YYYY-MM-DD)	2021-10-15
Name/Print	Ian D. MacKinnon	Registration Number	34,660

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L8	54	I7 and germanide same titanium	US-PGPUB; USPAT	OR	ON	2021/10/22 12:12
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L12	30	I6 and titanium same plug same source same drain same germanide	US-PGPUB; USPAT	OR	ON	2021/10/22 12:18
L13	1	I6 and opening same titanium same plug same source same drain same germanide	US-PGPUB; USPAT	OR	ON	2021/10/22 12:18
L14	20	I6 and (trench or opening) same titanium same plug same source same drain same germanide	US-PGPUB; USPAT	OR	ON	2021/10/22 12:19

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	Examiner Name	Fazli Erdem
	Attorney Docket Number	D480-012044

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20020168868	A1	2002-11-14	TODD	
	2	20020197806	A1	2002-12-26	FURUKAWA, et al.	
	3	20030124761	A1	2003-07-03	BAERT, et al.	
	4	20030157787	A1	2003-08-21	MURTHY, et al.	
	5	20040014276	A1	2004-01-22	MURTHY, et al.	
	6	20050145944	A1	2005-07-07	MURTHY, et al.	
	7	20060060859	A1	2006-03-23	JOSHI, et al.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16881541
Filing Date	2020-05-22
First Named Inventor	Glenn A. Glass
Art Unit	2826
Examiner Name	Fazli Erdem
Attorney Docket Number	D480-012044

8	20060065914	A1	2006-03-30	CHEN, et al.
9	20060125025	A1	2006-06-15	KAWASHIMA, et al.
10	20060138398	A1	2006-06-29	SHIMAMUNE, et al.
11	20060148151	A1	2006-07-06	MURTHY, et al.
12	20060172511	A1	2006-08-03	KAMMLER, et al.
13	20060199622	A1	2006-09-07	BHANJI, et al.
14	20060289856	A1	2006-12-28	SHIMAMUNE, et al.
15	20070004123	A1	2007-01-04	BOHR, et al.
16	20070053381	A1	2007-03-08	CHACKO, et al.
17	20070075378	A1	2007-04-05	LIN, et al.
18	20070122954	A1	2007-05-31	LIU, et al.

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19	20070235802	A1	2007-10-11	CHONG, et al.
20	20070254414	A1	2007-11-01	MIYANAMI
21	20070264801	A1	2007-11-15	CODY, et al.
22	20070294757	A1	2007-12-20	STEPHENS, et al.
23	20080054347	A1	2008-03-06	WANG
24	20080135949	A1	2008-06-12	LO, et al.
25	20080230805	A1	2008-09-25	HOKAZONO, et al.
26	20090075029	A1	2009-03-19	THOMAS, et al.
27	20100109044	A1	2010-05-06	TEKLEAB, et al.
28	20100123198	A1	2010-05-20	KIM, et al.
29	20100197092	A1	2010-08-05	KIM, et al.

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30	20100244154	A1	2010-09-30	YASUTAKE
31	20100272859	A1	2010-10-28	GIVEN
32	20100295021	A1	2010-11-25	CHANG, et al.
33	20110147811	A1	2011-06-23	KAVALIEROS, et al.
34	20110147828	A1	2011-06-23	MURTHY, et al.
35	20110183486	A1	2011-07-28	CHAN, et al.
36	20120153387	A1	2012-06-21	MURTHY, et al.
37	20120161249	A1	2012-06-28	KRONHOLZ, et al.
38	20130248999	A1	2013-09-26	GLASS, et al.
39	20130264639	A1	2013-10-10	GLASS, et al.
40	20140231914	A1	2014-08-21	CHANG, et al.

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41	20150060945	A1	2015-03-05	MURTHY, et al.
42	20150206942	A1	2015-07-23	GLASS, et al.
43	20150333180	A1	2015-11-19	GLASS, et al.
44	20160322359	A1	2016-11-03	GLASS, et al.
45	20160372547	A1	2016-12-22	GLASS, et al.
46	20170047419	A1	2017-02-16	GLASS, et al.
47	20170221724	A1	2017-08-03	MURTHY, et al.
48	20170373147	A1	2017-12-28	GLASS, et al.

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FOREIGN PATENT DOCUMENTS

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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²ⁱ	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1	S6313379	JP	A	1988-01-20	NIPPON TELEGR & TELEPH CORP <NTT>		×

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Examiner Name	Fazli Erdem
Attorney Docket Number	D480-012044

2	H10261792	JP	A	1998-09-29	HITACHI LTD	☒
3	200304703	TW	A	2003-10-01	INTERNATIONAL BUSINESS MACHINES CORPORATION	☒
4	2006013428	JP	A	2006-01-12	FUJITSU LTD	☒
5	2007053381	WO	A1	2007-05-10	ADVANCED MICRO DEVICES, INC.	☐
6	2007258485	JP	A	2007-10-04	TOSHIBA CORP	☒
7	2007294757	JP	A	2007-11-08	TOSHIBA CORP	☒
8	2007294780	JP	A	2007-11-08	SONY CORP	☒
9	101087002	CN	A	2007-12-12	IBM	☒
10	2008034650	JP	A	2008-02-14	FUJITSU LTD	☒
11	101140948	CN	A	2008-03-12	TAIWAN SEMICONDUCTOR MFG	☒
12	2008100687	WO	A1	2008-08-21	FREESCALE SEMICONDUCTOR INC.	☐

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13	2008192989	JP	A	2008-08-21	FUJITSU LTD	☒
14	2008533695	JP	A	2008-08-21		☒
15	2008218725	JP	A	2008-09-18	RENESAS TECHNOLOGY CORP	☒
16	101300664	CN	A	2008-11-05	ADVANCED MICRO DEVICES INC.	☒
17	2009514248	JP	A	2009-04-02		☒
18	2009517867	JP	A	2009-04-30		☒
19	2009164281	JP	A	2009-07-23	FUJITSU MICROELECTRONICS LTD	☒
20	2009182360	JP	A	2009-08-13	INTEL CORP	☒
21	2009200090	JP	A	2009-09-03	PANASONIC CORP	☒
22	20090118935	KR	A	2009-11-18	FREESCALE SEMICONDUCTOR, INC.	☒
23	2010014246	WO	A1	2010-02-04	GLOBALFOUNDRIES INC.	☐

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Attorney Docket Number	D480-012044

24	101677110	CN	A	2010-03-24	INTEL CORP.	☒
25	2010510720	JP	A	2010-04-02		☒
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27	2010171337	JP	A	2010-08-05	TOSHIBA CORP	☒
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29	2011084262	WO	A2	2011-07-14	INTEL CORPORATION	☐
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33	2012087581	WO	A2	2012-06-28	INTEL CORPORATION	☐
34	2012088097	WO	A2	2012-06-28	INTEL CORPORATION	☐

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35	690084	TW	B	2020-04-01	INTEL CORPORATION	☒
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NON-PATENT LITERATURE DOCUMENTS

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Communication Pursuant to Article 94(3) EPC for EP Application No. 17193291.6, Dated February 26, 2020, Pages 3	
	2	Communication Pursuant to Article 94(3) EPC for EP Application No. 17193291.6, Dated June 16, 2021, Pages 5	
	3	Extended European Search Report for EP Application No. 17193291.6, Dated March 23, 2018, Pages 9	
	4	First Japanese Office Action for JP Application No. 2019-189786, Dated June 22, 2021, Pages 10	
	5	First Taiwanese Office Action for TW Application No. 108107651, Dated August 15, 2021, Pages 10	

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Examiner Signature	/FAZLI ERDEM/	Date Considered	10/23/2021
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

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Filing Date	2020-05-22
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Art Unit	2826
Examiner Name	Fazli Erdem
Attorney Docket Number	D480-012044

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

✓ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ian D. MacKinnon/	Date (YYYY-MM-DD)	2021-10-08
Name/Print	Ian D. MacKinnon	Registration Number	34,660

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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164 7590 11/02/2021
KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

FILED VIA EFS-WEB

Ian D. MacKinnon	(Typed or printed name)
/Ian D. MacKinnon/	(Signature)
January 6, 2022	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/881,541	05/22/2020	Glenn A. GLASS	D480-012044	8383

TITLE OF INVENTION: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	02/02/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
ERDEM, FAZLI	2826	257-190000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

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1 Kinney & Lange, P. A.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Intel Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Santa Clara, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

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☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

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Authorized Signature /Ian D. MacKinnon/

Date January 6, 2022

Typed or printed name Ian D. MacKinnon

Registration No. 34,660

Electronic Patent Application Fee Transmittal				
Application Number:		16881541		
Filing Date:		22-May-2020		
Title of Invention:		CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION		
First Named Inventor/Applicant Name:		Glenn A. GLASS		
Filer:		Ian David MacKinnon/Nicole Chambers		
Attorney Docket Number:		D480-012044		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	44683802
Application Number:	16881541
International Application Number:	
Confirmation Number:	8383
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	Glenn A. GLASS
Customer Number:	164
Filer:	Ian David MacKinnon
Filer Authorized By:	
Attorney Docket Number:	D480-012044
Receipt Date:	06-JAN-2022
Filing Date:	22-MAY-2020
Time Stamp:	14:03:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$1200
RAM confirmation Number	E202216E04171646
Deposit Account	110982
Authorized User	Ian MacKinnon
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.21 (Miscellaneous fees and charges) 37 CFR 1.20 (Post Issuance fees)	

37 CFR 1.19 (Document supply fees)
 37 CFR 1.17 (Patent application and reexamination processing fees)
 37 CFR 1.16 (National application filing, search, and examination fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2022-01-06_PART-B_D480-012044.pdf	157260	no	1
			650eba577436ab0b536953891b541801a21e7191		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	37860	no	2
			ab403bd070e96fd83ba16feff8f158c5bd32de4d		

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	16/881,541
	Filing Date	May 22, 2020
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2811
	Examiner Name	N/A
Sheet 1 of 3	Attorney Docket No: P38507USC2-C1-C1 111548	

US PATENT DOCUMENTS

Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-5,312,766	05-17-1994	Sheldon Aronowitz et al.	
		US-5,296,387	03-22-1994	Sheldon Aronowitz et al.	
		US-5,296,386	03-22-1994	Sheldon Aronowitz et al.	
		US-7,821,044	10-26-2010	Mark T. Bohr et al.	
		US-8,575,652	11-05-2013	Yoshiki Kamata	
		US-7,221,006	05-22-2007	Marius Orlowski et al.	
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Change(s) applied
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EXAMINER /FAZLI ERDEM/

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 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.E./



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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

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