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(54) METHOD TO CONTROL SOURCE/DRAIN STRESSOR PROFILES FOR STRESS ENGINEERING

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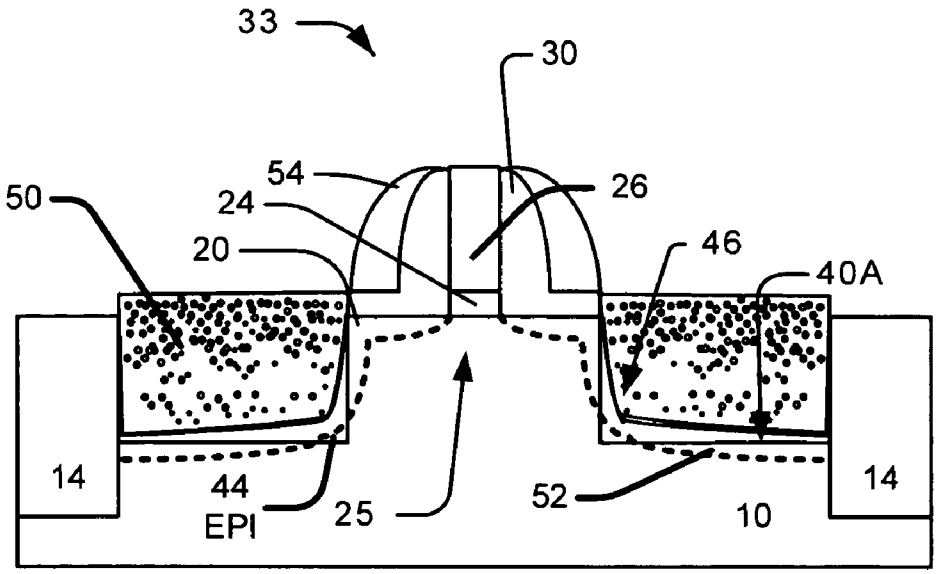
(57) **ABSTRACT**

An example embodiment of a strained channel transistor structure comprises the following: a strained channel region comprising a first semiconductor material with a first natural lattice constant; a gate dielectric layer overlying the strained channel region; a gate electrode overlying the gate dielectric layer; and a source region and drain region oppositely adjacent to the strained channel region, one or both of the source region and drain region are comprised of a stressor region comprised of a second semiconductor material with a second natural lattice constant different from the first natural lattice constant; the stressor region has a graded concentration of a dopant impurity and/or of a stress inducing molecule. Another example embodiment is a process to form the graded impurity or stress inducing molecule stressor embedded S/D region, whereby the location/profile of the S/D stressor is not defined by the recess depth/profile.



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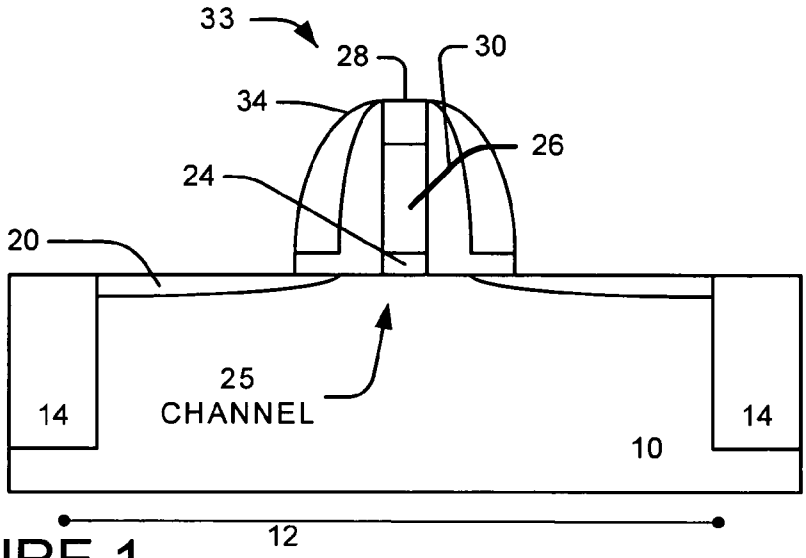

FIGURE 1

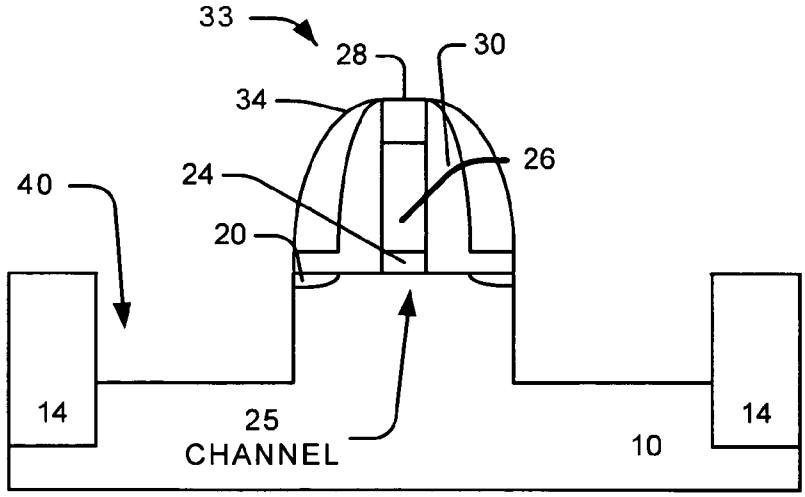

FIGURE 2

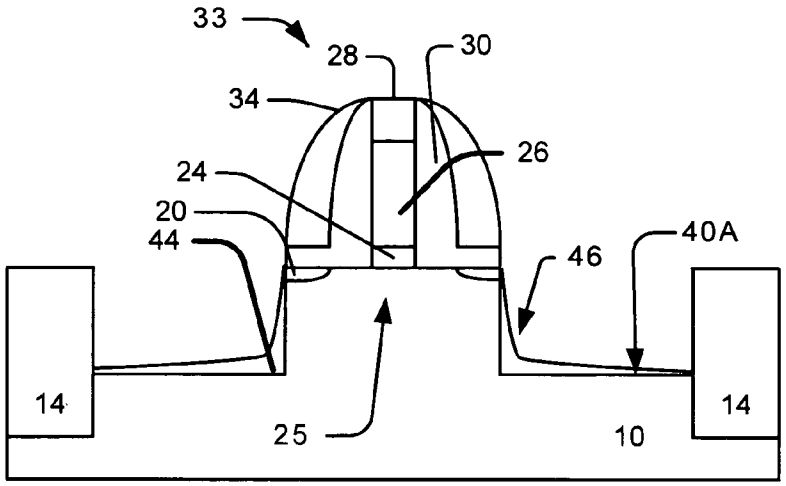

FIGURE 3

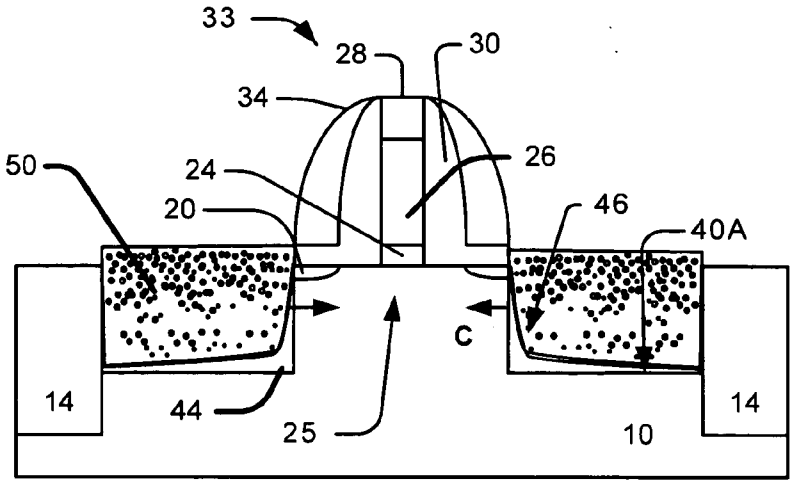

FIGURE 4A

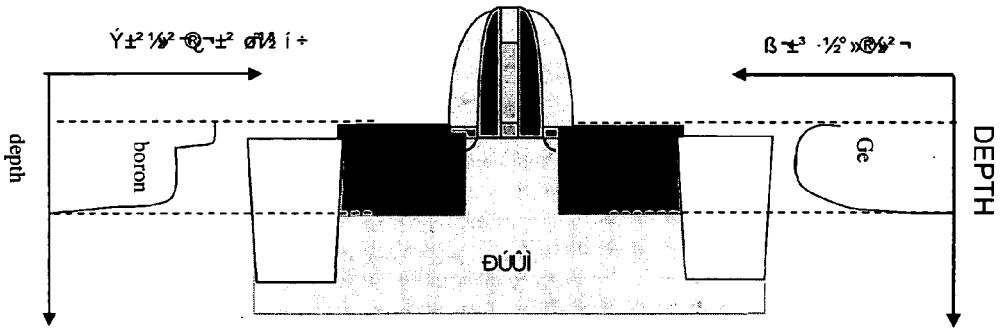

FIGURE 4B

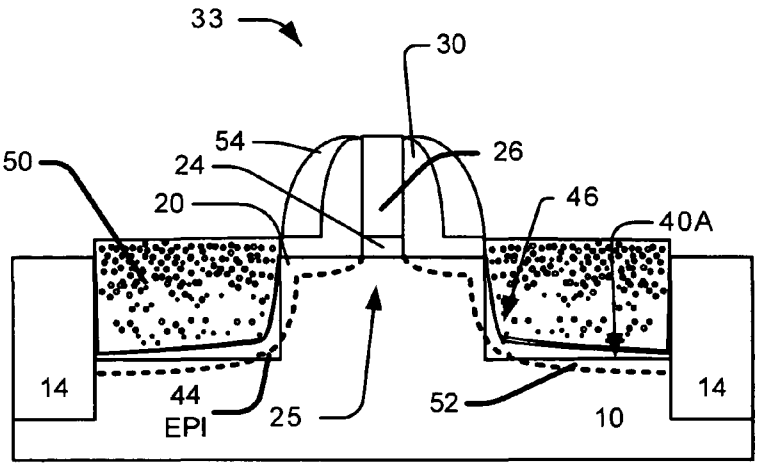

FIGURE 5

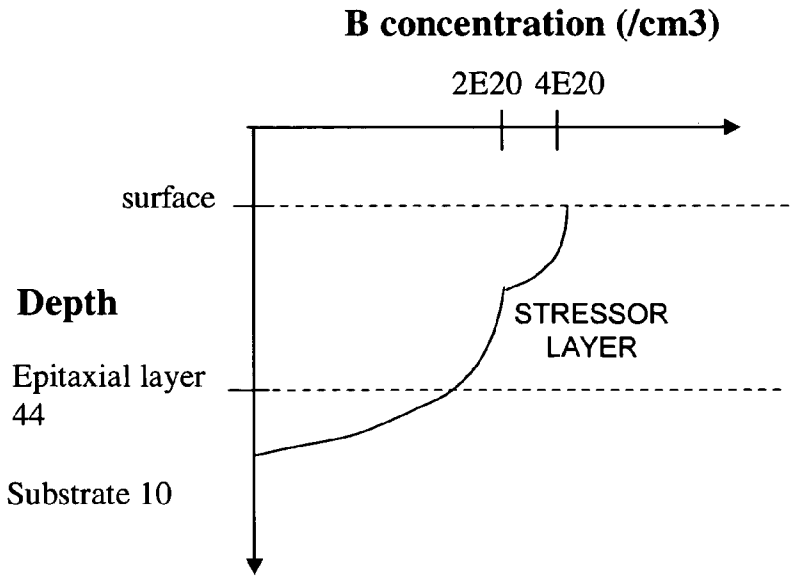

FIGURE 6A

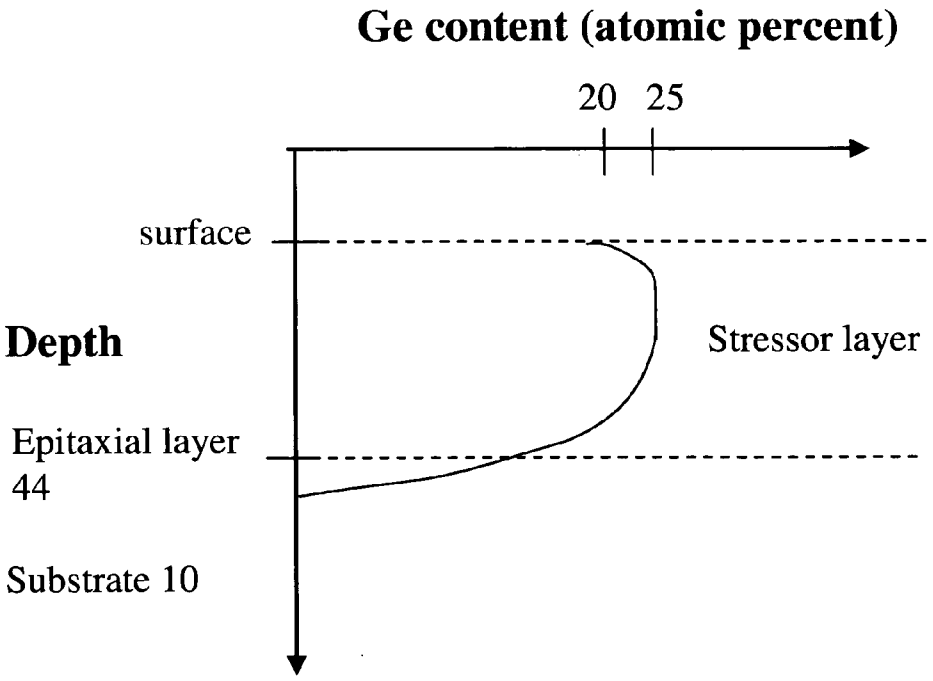

FIGURE 6B

METHOD TO CONTROL SOURCE/DRAIN STRESSOR PROFILES FOR STRESS ENGINEERING

BACKGROUND OF INVENTION

[0001] 1) Field of the Invention

[0002] This invention generally relates to the devices and methods for the fabrication of semiconductor devices, and more particularly to the fabrication of Field Effect Transistors (FETs) having embedded Source/Drain regions with controlled impurity profiles.

[0003] 2) Description of the Prior Art

[0004] It is now well-known that SiGe can be embedded into the source/drain (S/D) regions of PFETs to generate uniaxial stress in the silicon channel. This in turn increases the carrier mobility in the PFET channel and thus enhances the PFET device performance significantly. However, the integration of embedded SiGe (eSiGe) into the normal CMOS process flow is extremely challenging. The extent of performance enhancement also depends strongly on the stress generated by the SiGe itself, the active dopant concentration in the eSiGe and the proximity of the stressor to the channel region.

[0005] The importance of overcoming the various deficiencies noted above is evidenced by the extensive technological development directed to the subject, as documented by the relevant patent and technical literature. The closest and apparently more relevant technical developments in the patent literature can be gleaned by considering the following.

[0006] U.S. Pat. No. 6,921,913: Strained-channel transistor structure with lattice-mismatched zone—Strained-channel transistor structure includes portions of source and drain regions adjacent to strained channel region and lattice mismatched with respect to channel region. Inventor: Yeo, Yee-Chia; Singapore, Singapore

[0007] U.S. Pat. No. 5,442,205: Semiconductor heterostructure devices with strained semiconductor layers—Semiconductor heterostructure devices with strained semiconductor layers—have monocrystalline silicon substrate, spatially graded epitaxial layer of germanium-silicon, spatially ungraded layers of germanium-silicon and epitaxial layer of germanium or silicon. Inventor: Brasen, Daniel.

[0008] U.S. Pat. No. 6,831,292 and US20050054168A1: Semiconductor structures employing strained material layers with defined impurity gradients and methods for fabricating same—Semiconductor structure has strained layer(s) with specified impurity gradient. Inventor: Currie, Matthew; et al.

[0009] U.S. Pat. No. 6,844,227: Semiconductor devices and method for manufacturing the same—Field effect transistor includes a channel layer whose thickness is a critical film thickness or less so that dislocation due to strain may not be caused depending on the carbon content. Inventor: Kubo, Minoru; Mie, Japan

[0010] US20040262694A1: Transistor device containing carbon doped silicon in a recess next to MDD to create strain in channel—Metal oxide semiconductor transistor e.g. NMOS transistor has stress inducing regions on opposite of channel, such that distance between source and drain extension regions is greater than distance between stress inducing regions. Inventor: Chidambaram, P R

[0011] U.S. Pat. No. 6,323,525: MISFET semiconductor device having relative impurity concentration levels between layers—MISFET element for semiconductor IC—has source and drain areas formed from n+ type semiconductor layer and n− type semiconductor layer—Inventor: Noguchi, Mitsuhiro

[0012] US20050082522A1: Strained channel transistor formation—Transistor comprises strained channel region formed of first material and being intermediate source region and drain region Inventor: Huang, Yi-Chun;

SUMMARY OF THE INVENTION

[0013] The example embodiments of the present invention provide a structure and a method of manufacturing a transistor having a strained channel region which is characterized as follows.

[0014] An example embodiment method for forming semiconductor device comprising the steps of:

[0015] providing a FET gate structure over a substrate;

[0016] performing an etch to form a recess adjacent to the FET gate structure;

[0017] forming an epitaxial layer over the sidewalls and bottom of the recess so to form rounded corners and to form a rounded corner recess;

[0018] forming a stressor layer filling the rounded corner recess; the stressor is doped with an impurity.

[0019] Another example embodiment method for forming semiconductor device comprises the steps of:

[0020] providing a PFET gate structure over a substrate;

[0021] providing PFET SDE regions adjacent to the PFET gate structure;

[0022] providing isolation regions in the substrate;

[0023] performing an anisotropic etch to form a recess adjacent to the PFET gate structure;

[0024] the recess has substantially straight sidewalls and a substantially flat bottom;

[0025] performing a epitaxy preclean of the substrate;

[0026] forming an epitaxial layer over the sidewalls and bottom of the recess to form rounded corners in the recess and to form a rounded corner recess;

[0027] forming a stressor layer filling the rounded corner recess;

[0028] the epitaxial layer and the stressor layer are formed in-situ;

[0029] annealing the substrate to form source/drain regions that diffuse from the stressor region into the substrate.

[0030] Another example embodiment is the semiconductor device comprised of:

[0031] a FET gate structure over a FET region in a substrate;

[0032] FET SDE regions in the substrate adjacent to the FET gate structure;

[0033] isolation regions in the substrate around the FET region;

[0034] a recess in the substrate adjacent to the PFET gate structure;

[0035] the recess has substantially straight sidewalls and a substantially flat bottom;

[0036] an epitaxial layer over the sidewalls and bottom of the recess so to form rounded corners in the recess and to form a rounded corner recess;

[0037] a stressor layer filling the rounded corner recess; the stressor is doped with an impurity.

[0038] The above and below advantages and features are of representative embodiments only, and are not exhaustive and/or exclusive. They are presented only to assist in understanding the invention. It should be understood that they are not representative of all the inventions defined by the claims, to be considered limitations on the invention as defined by the claims, or limitations on equivalents to the claims. For instance, some of these advantages may be mutually contradictory, in that they cannot be simultaneously present in a single embodiment. Similarly, some advantages are applicable to one aspect of the invention, and inapplicable to others. Furthermore, certain aspects of the claimed invention have not been discussed herein. However, no inference should be drawn regarding those discussed herein relative to those not discussed herein other than for purposes of space and reducing repetition. Thus, this summary of features and advantages should not be considered dispositive in determining equivalence. Additional features and advantages of the invention will become apparent in the following description, from the drawings, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] The features and advantages of a semiconductor device according to the present invention and further details of a process of fabricating such a semiconductor device in accordance with the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

[0040] FIGS. **1**, **2**, **3**, **4**A and **5** are cross sectional views for illustrating a method for manufacturing FETs having strained channels according to an example embodiment of the present invention.

[0041] FIG. **4**B is a cross sectional view of an FET with graphs overlaid that show the concentration profiles of B and Ge according to an example embodiment of the present invention.

[0042] FIGS. **6**A and **6**B are graphs showing B and Ge concentration profiles according to an example embodiment of the present invention.

DETAILED DESCRIPTION OF THE EXAMPLE EMBODIMENTS

[0043] A. Overview

[0044] An example embodiment is a method to form a strained channel transistor using a stressor region. The recess for the stressor region is preferably formed using an anisotropic etch. An epitaxial layer is preferably formed in the recess. Then a graded stressor region is formed has a gradual change in dopant impurity concentration and/or in stress inducing atom concentration. The graded stressor region overlaps at least a portion of the source/drain region.

[0045] An example method embodiment comprises the following.

[0046] form gate structure and Source/drain extension (SDE) regions

[0047] form recess preferably using anisotropic etch

[0048] form epitaxially grown layer in recess (lightly doped Si or SiGe buffer layer)

[0049] form graded stressor layer in recess with graded dopant concentration and/or stressor atom concentration.

[0050] reform spacers on gate structure

[0051] the profile of the S/D stressor is not defined by the recess depth/profile

[0052] anneal structure to diffuse dopant from graded stressor region into substrate to form S/D region

[0053] The example embodiment allows the flexibility of using the epitaxy process to tailor the S/D stressor profile, rather than relying on the isotropic recess etch process alone. This is done by using a multi-step epitaxy process after an anisotropic dry S/D recess etch. In general, anisotropic RIE is more stable than isotropic dry etch and is less susceptible to microloading effects from a neighboring protective layer.

[0054] In an example embodiment for PFETs with embedded SiGe, we first provide a gate structure with a nitride hard mask and offset spacers, and with SDE implants in place. Then we form nitride spacers adjacent to the offset spacers.

[0055] Subsequently, we perform an anisotropic RIE to etch the substrate to form the recessed S/D regions. Next, we perform a multi-step epitaxy process with varying growth conditions (such as gas chemistries and flow rates) to tailor the S/D stressor profile. For e.g., we can first form a lightly doped Si or SiGe buffer layer that rounds the corner of the Si recess, followed by epitaxial growth of in-situ boron doped SiGe with graded concentrations. The last SiGe layer towards the surface should preferably be highly doped with impurities (1E20 to 2E21/cm^3) such that the boron atoms can diffuse toward the SDE regions upon subsequent spike annealing. In this way, the series resistance can also be significantly reduced.

[0056] The example embodiments of the present invention can produce two kinds of stress modes (tensile or compression) exerted on the stressed-channel region.

MORE DETAILED DESCRIPTION OF AN EXAMPLE EMBODIMENT

[0057] The example embodiments of the present invention will be described in detail with reference to the accompa-

nying drawings. The example embodiments provide a method of forming a FET with a S/D stressor region with graded concentrations. The example below describes a PFET device, but the embodiment can also be used to form NFET devices.

[0058] A. Provide a PFET Gate Structure Over a Substrate

[0059] Referring to FIG. **1**, we provide a PFET gate structure **33** over a PFET region **12** in a substrate **10**.

[0060] The substrate **10** is preferably comprised of a first semiconductor material. The substrate **10** is preferably substantially comprised of silicon, with a natural lattice constant. The substrate can be a silicon wafer or any other appropriate semiconductor substrate.

[0061] PFET devices are preferably formed in the PFET region **12**. The PFET region **12** can be comprised of a N-well (not shown).

[0062] The PFET gate structure can be comprised of a gate electrode and a gate dielectric and is not limited to the example shown in the figs.

[0063] FIG. **1** shows a preferred PFET gate structure **33** that is comprised of a PFET gate dielectric **24**, a PFET gate **26**, a PFET channel **25**, PFET gate capping layer **28**, PFET first (L-shaped) spacers **30**, and PFET second spacers **34**.

[0064] An example of the scale and a composition of the PFET gate structure **33** is given below.

[0065] The PFET gate dielectric **24** can be comprised of SiO_xN_Y, nitrided SiO_2 (either by plasma or thermal means, or a combination thereof), HfO_2, $HfSi_XO_Y$, $HfAl_XO_Y$ and can have a thickness between 8 and 50 angstroms.

[0066] The PFET gate **26** can comprise of poly-Si or poly-SiGe or metals such as Ta, TaN, TaSiN, TiN, Mo, Ru, Ni, NiSi or a combination thereof and can have a thickness between 500 and 1200 angstroms.

[0067] The PFET gate capping layer **28** is preferably comprised of nitride or SiO_xN_Y or SiO_2 and can have thickness between 200 and 600 angstroms.

[0068] The PFET first L shaped spacers **30** can comprise of thermal oxide or TEOS and have thickness between 20 and 200 angstroms.

[0069] Next we provide PFET SDE (source drain extension) regions **20** adjacent to the PFET gate structure **33**.

[0070] Then, we provide the PFET second spacers **34** which can be comprised of nitride or oxide can have a thickness between 200 and 700 angstroms.

[0071] We preferably provide isolation regions **14** in the substrate that can separate the PFET regions from NFET regions and other regions.

[0072] B. Perform an Etch to Form a Recess

[0073] Referring to FIG. **2**, we perform an etch to form a recess **40** in the substrate adjacent to the PFET gate structure. Preferably the etch is an anisotropic etch. If NFET devices are present, they can be covered by a protective layer to prevent the etch.

[0074] Preferably the recess **40** has substantially straight sidewalls and a substantially straight bottom. In general, anisotropic RIE is more stable than isotropic dry etch. The embodiment's anisotropic etch provide advantages over an isotropic etch.

[0075] C. Form an Epitaxial Layer of a Undoped or Lightly Doped Si or SiGe Buffer Layer that has Rounded Corners in the Recess to Form a Rounded Corner Recess

[0076] Referring to FIG. **3**, we preferably perform an epitaxy preclean. The preclean preferably contains HF, either in the gaseous or liquid state, or a combination of other chemicals and steps that include the gaseous HF or liquid HF.

[0077] We can form an epitaxial layer **44** in the recess **40** to form a rounded corner recess **40**A that has a rounded corner **46**.

[0078] Prior to the epitaxy process, an optional moderate to high temperature prebake may be used to form the rounded corners **46** and to improve the interface quality by removing C or O at the surface of the recess **40**. The temperature of the prebake is preferably between 750 and 1000 C, and the duration is preferably between 2 sec and 5 min. H2, N2 or a combination of both can be used as the ambient gases during prebake. The pressure is preferably between 2 and 760 Torr. Besides improving the interface quality and hence the resultant epitaxy quality, the high temperature prebake can also be used to cause rounding of the corners of recess **40**. This is achieved because the surface Si atoms become mobile during the prebake and starts to move around to reduce the surface energy of the recess.

[0079] Preferably the epi layer **44** is comprised of an undoped or lightly doped Si or SiGe buffer layer that has rounded corners **46**.

[0080] The epitaxial layer **44** preferably has a B doping range for the lightly doped Si or SiGe between about 0 and 1E17 atom/cm^3.

[0081] In the case where the epitaxial layer **44** is SiGe, epitaxial layer **44** preferably has a Ge doping range between 0 and 10 atomic percent.

[0082] A purpose of epitaxial layer **44** is form the rounded corners **46** (in addition to the prebake) and thereby define the final profile of the S/D stressor. The profile of the S/D stressor and the proximity of the S/D stressor to the channel determines the amount of stress induced in the device channel.

[0083] In addition to forming the rounded corners, epitaxial layer **44** also helps to define the final profile of the S/D stressor.

[0084] D. Forming a Graded Stressor Layer Filling the Rounded Corner Recess

[0085] Referring to FIG. **4**A, we form a graded stressor layer **50** filling the rounded corner recess **40**A. The stress layer puts stress on the channel **25**. The prebake, epitaxial layer **44**, and the stressor **50** are preferably formed in-situ. The graded stressor layer (lattice-mismatched zone) **50** preferably comprises an alloy semiconductor material with a natural lattice constant larger than that of the substrate.

[0086] The graded stressor layer **50** is formed preferably in-situ with the epitaxial layer **44** and preferably formed using a boron doped SiGe epitaxy process with graded

concentrations of B and/or Ge. It is possible that the concentration of B and/or Ge remains constant at a desired value, which means that concentration gradient of stressor layer **50** is zero.

[**0087**] FIG. **4**B shows an example of the graded impurity and graded Ge strained graded stressor layer **50**.

[**0088**] The graded stressor layer is preferably formed using a selective epitaxy process.

Graded Ge Profile (as Deposited)

[**0089**] The graded stressor layer preferably has a high concentration of the stressor material near the top substrate surface. We want a graded Ge profile because we do not really need a uniform Ge concentration throughout the stressor layer. For e.g., the Ge concentration near the original surface (before the Si recess etch) should be the highest since it is nearest to the channel to exert more stress. However, there may be silicidation problems if it is too high, hence the top most layer of the stressor should have a relatively lower Ge concentration. Similarly, the Ge concentration at the bottom should not be too high else there may be defects formed, causing strain relaxation. Also, if the Si/SiGe interface is not good, leakage current through this interface may be high.

[**0090**] For example, the Ge concentration at the top most surface is preferably between 5 and 15 atomic percent; the Ge concentration at the region next to the top most surface is preferably between 10 and 40 atomic percent, and the Ge concentration at the bottom of layer **50** is preferably between 0 and 20 atomic percent. Preferably the concentration changes are smooth, not abrupt or stepped. We can steadily change the Ge flow into the reactor. The temperature and pressure of the epitaxy process can also be controlled to give the graded B and/or Ge. The thickness of the top most surface layer is between 2 and 35 nm; the thickness of the (e.g., middle region) region next to the top most surface is preferably between 5 and 120 nm; and the thickness of the (bottom region) bottom of layer **50** is preferably between 2 and 15 nm.

[**0091**] In the stressed-channel transistor structure, the substrate **10** preferably comprises silicon, with a natural lattice constant of approximately 5.431 angstroms.

[**0092**] The graded stressor layer (lattice-mismatched zone) **50** preferably comprises an alloy semiconductor material such as a silicon-germanium alloy, SiAr, SiKr, or SiXe alloy. The alloy semiconductor material with a natural lattice constant between about 5.431 to 5.657 angstroms depending on concentration of germanium in the silicon-germanium alloy.

[**0093**] The germanium concentration in the silicon-germanium alloy of graded stressor layer (lattice-mismatched zone) **50** is preferably between about 1 and 40 atomic percent.

[**0094**] Therefore, graded stressor region **50** acts as a stressor and preferably exerts a compressive stress C in a source-to-drain direction on the strained channel region **25**, resulting in strained channel region **25** under a compressive strain in the source-to-drain direction. Hole mobility in the strained channel region **25** is significantly enhanced, enhancing drive current when stressed-channel transistor structure in accordance with the example embodiment is a P-channel transistor structure.

Graded B Stressor Layer (Before Anneal)

[**0095**] The graded stressor layer preferably has a graded impurity (e.g., B) profile. We want a graded B profile because we do not really need a uniform B concentration throughout the stressor layer. For e.g., the B concentration near the top most surface should be the highest since it can reduce the series and external resistance. However, there may be severe short channel effects if the thickness of this highly B doped region exceeds a certain depth (for e.g. 20 nm). Hence the adjacent layer ("middle" layer) of the B doped stressor should have a relatively lower B concentration, yet it cannot be too low to maintain desirable low S/D sheet resistance. The B concentration at the bottom should be even lower to form a graded junction and reduce the leakage current or reduce the junction capacitance.

[**0096**] The B impurity concentration (before anneal) in the stressor layer near the top surface is preferably between 1E20 and 2E21 atoms/cm^3. The B impurity concentration at the "middle" layer is preferably between 8E19 and 1E20 atoms/cm^3 and the B impurity concentration near the bottom of the stressor layer **50** is preferably between 6E17 and 8E19 atoms/cm^3.

Both Graded Ge and B Stressor Layer

[**0097**] Preferably the graded stressor layer **50** has both a graded Ge and graded B concentration profile. The temperature and pressure of the chamber can be controlled during the epitaxy process to give the graded B and/or Ge. Furthermore, graded Ge can also controlled by the flow of GeH_4. Graded B can also controlled by the flow of B_2H_6. Both gases are flowing into the chamber independently.

"Graded" concentration means a sloped or even or gradual increase or decrease. In contrast, an abrupt concentration gradient occurs.

[**0098**] E. Remove the PFET Cap and the PFET Second Spacers; and Form Third Spacers on the Sidewalls of the First Spacer

[**0099**] Referring to FIG. **5**, in an optional but preferred step, we remove the PFET cap **28** and the PFET second spacers **34**. Next, we form third spacers **54** on the sidewalls of the first spacer **30**.

[**0100**] Preferably the third spacers **54** have a larger thickness than the second spacers **34**. This is in order to prevent subsequent silicide to encroach into the SiGe regions or into the channel.

[**0101**] F. Anneal the Substrate to Form Source/Drain Regions that Diffuse from the Stressor Region into the Substrate

[**0102**] Still referring to FIG. **5** we anneal the substrate to form source/drain regions **52** that diffuse from the stressor region **50** into the substrate **10**. The source drain regions are comprised of the Stressor regions **50** and the S/D doped regions that diffuse from the stressor regions.

[**0103**] The anneal is preferably a spike anneal preferably performed at a temperature between 950 and 1300 C for a time between 100 microsec and 5 sec.

[0104] The stressor should be as close as possible to the channel without subjecting the transistor to short channel effects. Hence, there is an optimum position for the in-situ B doped SiGe stressor with respect to the channel.

Graded Ge Profile (after Anneal)

[0105] The Ge concentration at the top most surface is preferably between 5 and 15 atomic percent; the Ge concentration at the region next to the top most surface is preferably between 10 and 40 atomic percent, and the Ge concentration at the bottom of layer **50** is preferably between 1 and 20 atomic percent.

[0106] The thickness (depth) of the (e.g., top region) top most surface layer is between 2 and 35 nm; the thickness of the (e.g., middle region) region next to the top most surface is preferably between 5 and 120 nm; and the thickness of the (bottom region) bottom of layer **50** is preferably between 2 and 15 nm.

Graded B Stressor Layer (after Anneal)

[0107] The B impurity concentration (before anneal) in the stressor layer near the top surface is preferably between 1E20 and 2E21 atoms/cm^3. The B impurity concentration at the "middle" layer is preferably between 8E19 and 1E20 atoms/cm^3 and the B impurity concentration near the bottom of the stressor layer **50** is preferably between 6E17 and 8E19 atoms/cm^3.

[0108] The B impurity concentration (after anneal) in the Stressor layer near the top surface is preferably between 2E20 and 2E21 atoms/cm^3. The B impurity concentration at the "middle" layer is preferably between 8E19 and 2E20 atoms/cm^3 and the B impurity concentration near the bottom of the stressor layer **50** is preferably between 6E17 and 8E19 atoms/cm^3.

[0109] G. Concentration Profiles

[0110] FIGS. **6**A and **6**B show example concentration profiles after anneal.

[0111] H. Alternate Embodiments—e.g., NFET Graded Stressor

[0112] The example embodiments can be implemented on both PFET and NFET devices. For example, the embodiments can be used on NFET with SiC stressor region (graded stressor and/or graded N-type impurity). For SiC, the C content is between 0.5 to 2.5 atomic percent. The SiC can be in-situ doped with As or P, or undoped, which is subsequently implanted with As or P.

I. Device Example Embodiments

[0113] Referring to FIG. **5**. an example embodiment of a semiconductor device comprised of:

[0114] a FET gate structure over a FET region in a substrate;

[0115] FET SDE regions in said substrate adjacent to said FET gate structure;

[0116] isolation regions in said substrate around said FET region;

[0117] a recess in said substrate adjacent to said PFET gate structure;

[0118] the recess has substantially straight sidewalls and a substantially flat bottom;

[0119] an epitaxial layer over the sidewalls and bottom of the recess so to form rounded corners in the recess and to form a rounded corner recess;

[0120] a stressor layer filling the rounded corner recess; said stressor is doped with an impurity.

[0121] J. Some Non-Limiting Benefits of Some Example Embodiments

[0122] Strained silicon channels are known to be effective to increase electron or hole mobilities. One method to increase the stress/strain in the device channel is to first etch the S/D regions to a certain depth and then fill the recessed S/D with appropriate materials (such as SiGe for PFETs and SiC for NFETs), which become the S/D "stressors". The location/profile of the S/D stressors is thus defined by the recess depth/profile. In order to have the stressors to be closer to the channel, one has to ensure some degree of undercutting beneath the spacers, i.e. to etch the S/D regions isotropically. However, it is difficult to control the recess profile because the isotropic dry etch process is easily affected by the presence of residual film on the surface, as well as by the microloading effects from the neighboring protective layer (either resist, nit, or oxide) that is covering regions that should not have recess. The example embodiments allow the flexibility of using a multi-step epitaxy process to tailor the S/D stressor profile, rather than relying on the isotropic RIE process alone. Hence, the profile of the S/D stressor is NOT defined by the recess depth/profile. Furthermore, no deep S/D implants are needed since the epitaxy process can tailor the S/D junction profile.

Benefits of Graded Ge Stressor

[0123] The example embodiment's graded Ge stressor region provides the following advantages: Typically, we need a relatively high Ge concentration (~20 to 40 atomic percent) in the stressor to induce sufficiently high stress in the channel. However, this may cause a lot of defects (such as stacking fault, dislocations, misfits etc.) in the stressor film, especially at the SiGe/Si interface. Another problem is that when the Ge concentration increases, it becomes increasingly difficult to form a low resistivity silicide film with the typical metallic materials (e.g. Co, Ti, Ni or NiPt), and usually the silicide formed has poor surface and interface roughness. Hence, by having a graded Ge stressor region, e.g. low Ge concentration at the SiGe/Si interface, and low Ge concentration near the top of the stressor, the epitaxy quality will improve and it is easer to form low resistivity silicide.

Benefits of Graded B Stressor

[0124] The example embodiment's graded (e.g., B) impurity stressor region gives the following advantages: In general, the B concentration in the stressor region should be as high as possible to reduce the series resistance. However, if it is too high, the transistor may suffer from severe short channel effects. Hence, the graded (e.g, B) impurity stressor gives the flexibility to tune the active carrier profile in the S/D region such that the boron concentration at the near surface regions is extremely high (1E20 to 2E21/cm^3) and boron concentration at the middle and lower portion of the

S/D region is relatively low (1E18 to 1E20/cm^3). The lowest portion of the S/D region should ideally be graded to reduce the junction capacitance.

[0125] K. Non-Limiting Example Embodiments

[0126] In the above description numerous specific details are set forth such as flow rates, pressure settings, thicknesses, etc., in order to provide a more thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these details. In other instances, well known process have not been described in detail in order to not unnecessarily obscure the present invention.

[0127] Given the variety of embodiments of the present invention just described, the above description and illustrations show not be taken as limiting the scope of the present invention defined by the claims.

[0128] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention. It is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

What is claimed is:

1. A method for forming semiconductor device comprising the steps of:

a) providing a FET gate structure over a substrate;

b) performing an etch to form a recess adjacent to said FET gate structure;

c) forming an epitaxial layer over the sidewalls and bottom of the recess so to form rounded corners and to form a rounded corner recess;

d) forming a stressor layer filling the rounded corner recess; said stressor is doped with an impurity.

2. The method of claim 1 which further includes:

providing FET SDE regions adjacent to said FET gate structure;

providing isolation regions in said substrate; and

after the stressor layer is formed, annealing the substrate to form source/drain regions that comprise the stressor regions and doped regions that diffuse from the stressor region into the substrate.

3. The method of claim 1 wherein the etch to form the recesses comprises an anisotropic etch and the recess has substantially straight sidewalls and a substantially flat bottom.

4. The method of claim 1 wherein the formation of the epitaxial grown layer and the stress layer are performed in-situ.

5. The method of claim 1 which further includes after the etch to form the recess and before the formation of the epitaxial layer:

performing a epi preclean.

6. The method of claim 1 wherein the epitaxial layer is comprised of a material selected from the group consisting of undoped Si, a lightly doped silicon, SiC and SiGe.

7. The method of claim 1 wherein the stressor layer is comprised of a layer selected from the group consisting of a SiGe layer with a graded Ge concentration; a SiGe layer with a graded SiGe dopant concentration.

8. The method of claim 1 wherein the stressor layer has a higher concentration of Ge near the top surface than near the substrate.

9. A method form forming semiconductor device comprising the steps of:

a) providing a PFET gate structure over a substrate;

b) providing PFET SDE regions adjacent to said PFET gate structure;

c) providing isolation regions in said substrate;

d) performing an anisotropic etch to form a recess adjacent to said PFET gate structure;

(1) the recess has substantially straight sidewalls and a substantially flat bottom;

e) performing a epi preclean of the substrate;

f) forming an epitaxial layer over the sidewalls and bottom of said recess to form rounded corners in the recess and to form a rounded corner recess;

g) forming a stressor layer filling the rounded corner recess;

(1) the epitaxial layer and the stressor layer are formed in-situ.

10. The method of claim 9 which further includes annealing the substrate to form source/drain regions that diffuse from the stressor region into the substrate.

11. The method of claim 9 wherein said PFET gate structure is comprised of a PFET gate dielectric, a PFET gate, a PFET channel, PFET gate cap comprised of nitride, PFET first spacers, and PFET second spacers.

12. The method of claim 9 wherein the epitaxial grown layer is comprised of a material selected from the group consisting of undoped Si, lightly P doped silicon, SiGe, SiAr, SiKr, and SiXe alloy.

13. The method of claim 9 wherein the stressor layer has a higher concentration of Ge near the top surface than near the substrate.

14. The method of claim 9 wherein the stressor layer is comprised of a layer selected from the group consisting of a SiGe layer with a graded Ge concentration; a SiGe layer with a graded SiGe dopant concentration.

15. The method of claim 9 wherein the stressor layer is formed using a boron doped SiGe epi growth process with graded concentrations of B and/or Ge with the B or Ge concentrations greatest near the top surface.

16. The method of claim 9 wherein the stressor layer is formed using a boron doped SiGe epi growth process with graded concentrations of B and/or Ge with the B or Ge concentrations greatest near the top surface;

said stressor layer is comprised of: a top region with a thickness is between 2 and 35 nm; a middle region with the thickness of between 5 and 120 nm; and a bottom region with a thickness between 2 and 15 nm;

the Ge concentration in the top region is between 5 and 15 atomic percent; the Ge concentration in the middle region is between 10 and 40 atomic percent, and the Ge concentration in the bottom region is between 1 and 20 atomic percent.

17. A semiconductor device comprised of:

a) a FET gate structure over a FET region in a substrate;

b) FET SDE regions in said substrate adjacent to said FET gate structure;

c) isolation regions in said substrate around said FET region;

d) a recess in said substrate adjacent to said PFET gate structure;

the recess has substantially straight sidewalls and a substantially flat bottom;

e) an epitaxial layer over the sidewalls and bottom of the recess so to form rounded corners in the recess and to form a rounded corner recess;

f) a stressor layer filling the rounded corner recess; said stressor is doped with an impurity.

18. The semiconductor device of claim 17 wherein the epitaxial layer is comprised of a material selected from the group consisting of undoped Si, a lightly doped silicon, SiC and a SiGe.

19. The semiconductor device of claim 17 wherein the stressor layer is comprised of a layer selected from the group consisting of a SiGe layer with a graded Ge concentration; a SiGe layer with a graded dopant concentration.

20. The semiconductor device of claim 17 wherein the stressor layer has a higher concentration of Ge near the top surface than near the substrate.

21. The semiconductor device of claim 17 wherein the stressor layer has graded concentrations of B and/or Ge with the B or Ge concentrations greatest near the top surface;

said stressor layer is comprised of: a top region with a thickness is between 2 and 35 nm; a middle region with the thickness of between 5 and 120 nm; and a bottom region with a thickness between 2 and 15 nm;

the Ge concentration in the top region is between 5 and 15 atomic percent; the Ge concentration in the middle region is between 10 and 40 atomic percent, and the Ge concentration in the bottom region is between 1 and 20 atomic percent.

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