A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging

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ABSTRACT

A 45nm logic technology is described that for the first time incorporates high-k + metal gate transistors in a high volume manufacturing process. The transistors feature 1.0nm EOT high-k gate dielectric, dual band edge workfunction metal gates and third generation strained silicon, resulting in the highest drive currents yet reported for NMOS and PMOS. The technology also features trench contact based local routing, 9 layers of copper interconnect with low-k ILD, low cost 193nm dry patterning, and 100% Pb-free packaging. Process yield, performance and reliability are demonstrated on 153Mb SRAM arrays with SRAM cell size of 0.346μm^2, and on multiple microprocessors.

INTRODUCTION

Since the advent of MOS devices over 40 years ago, SiO_2 has served as the transistor gate insulator of choice. Electrical oxide thickness ($T_{OX(e)}$) was scaled at ~0.7x per generation up to the 130nm node, but scaling slowed at the 90nm and 65nm nodes as SiO_2 ran out of atoms and gate leakage power limited further scaling (Fig. 1). High-k gate dielectric materials have held the promise of continued scaling at low gate leakage. Many challenges with high-k integration have included V_T pinning, mobility degradation due to soft optical phonons, and poor reliability [1-3]. Metal gate electrodes not only eliminate the poly depletion effect, but enable high-k dielectrics by screening the SO phonons that cause mobility degradation [4]. High performance high-k + metal gate transistors have been demonstrated using band edge workfunction metal gate electrodes [5]. However, challenges have remained in finding a compatible integration scheme that addresses thermal budget concerns. In this work high-k + metal gate integration challenges are overcome (Fig. 2), enabling a return to 0.7X $T_{OX(e)}$ scaling while simultaneously reducing gate leakage >25X.

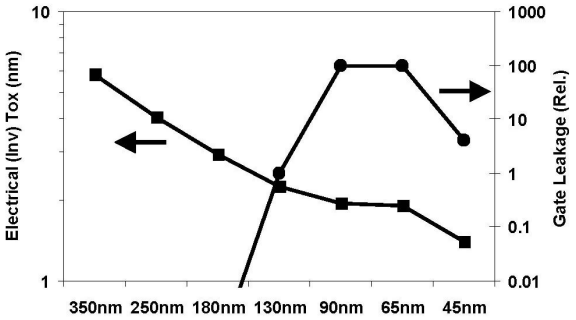

Fig. 1 Intel scaling trend for inversion electrical T_{OX}

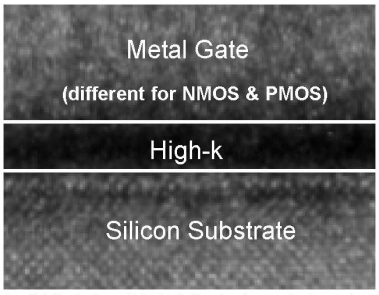

Fig. 2 TEM of High-k + Metal Gate transistor stack

KEY DESIGN RULES & TECHNOLOGY FEATURES

TABLE I summarizes key design rules & layer thicknesses. Contacted gate pitch - a key measure of front end density - is scaled to 160nm, maintaining 0.7x scaling trend (Fig. 3). This is the most aggressive CGP reported for 45nm high performance logic technologies. Conventional contacts have been replaced with trench contacts for lower series resistance. Trench contact based local routing improves layout density, especially for cross-coupled inverter pairs that are very common in microprocessor SRAM and register file arrays. Tight pitches and trench contacts allow SRAM cell size to be scaled to 0.346μm^2 (Fig. 4).

Innovative processes for 0.92NA 193nm dry patterning allow for low cost & robust patterning, as demonstrated by the fidelity of the poly lines in Fig. 4. Metal gate materials are chosen with optimal workfunctions for NMOS and PMOS performance. The transistor process flow, described next, is chosen so as to maintain the workfunction of the metal gates.

TABLE I: Layer Pitch, thickness and aspect ratio

Layer	Pitch (nm)	Thick (nm)	Aspect Ratio
Isolation	200	200	-
Contacted Gate Pitch	160	60	-
Metal 1	160	144	1.8
Metal 2	160	144	1.8
Metal 3	160	144	1.8
Metal 4	240	216	1.8
Metal 5	280	252	1.8
Metal 6	360	324	1.8
Metal 7	560	504	1.8
Metal 8	810	720	1.8
Metal 9	30.5μm	7μm	0.4

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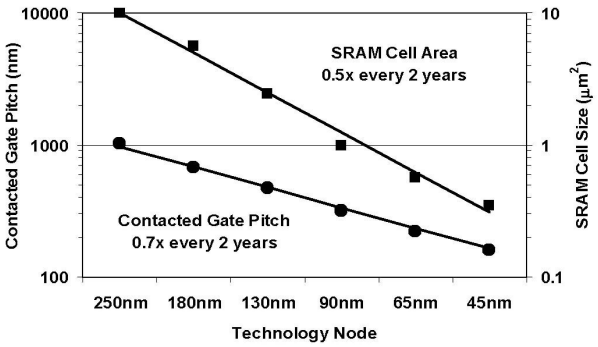

Fig. 3 Intel contacted gate pitch and SRAM cell scaling trend

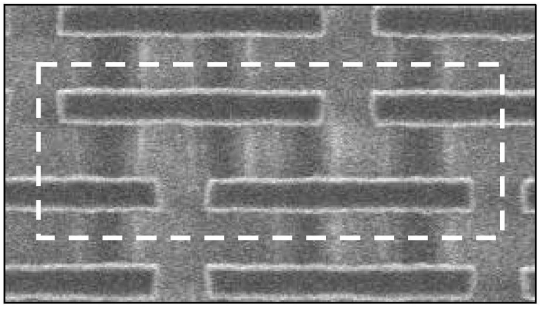

Fig. 4 Diffusion and poly layers of 0.346 μm^2 6-T SRAM cell

TRANSISTOR PROCESS FLOW

Strained silicon mobility enhancement techniques have dramatically improved transistor performance recently [6-8]. In this work, we further enhance the strained silicon techniques we first introduced at the 90nm and 65nm nodes. A key challenge was to simultaneously integrate high-k gate dielectrics, optimal workfunction metal gate electrodes and highly strained silicon channels. Transistors feature 160nm gate pitch, 35nm physical gate length, hafnium-based 1.0nm EOT high-k gate dielectric, dual workfunction metal gate electrodes, enhanced channel strain, ultra shallow junctions & nickel silicide.

Fig. 5 describes the transistor formation process, which features high-k first and metal gate last. The process flow up to and including salicidation is similar to 90nm and 65nm [6,7], except that SiO_2 growth is replaced by hafnium-based high-k gate dielectric formation using atomic layer deposition. After ILD0 deposition, a polish step exposes poly gates and the dummy poly is removed. The PMOS workfunction metal is deposited. A patterning step removes the PMOS metal from NMOS areas and the NMOS workfunction metal is deposited. Gate trenches are filled with Al for low gate resistance; innovative techniques allow robust gapfill down to 30nm gate length. Finally, the gate trenches are planarized via a metal polish step, followed by contact etch stop layer deposition. Fig.6 shows a TEM of the high-k/metal gate PMOS transistors with SiGe strain layer and Ni salicide.

TRANSISTOR CHARACTERISTICS

High-k + metal gate provides dramatic gate leakage reduction: relative to 65nm transistors [7], gate leakage is reduced by >25X for NMOS & by 1000X for PMOS (Fig. 7).

Fig.5 Transistor process flow highlighting differences from [6,7]

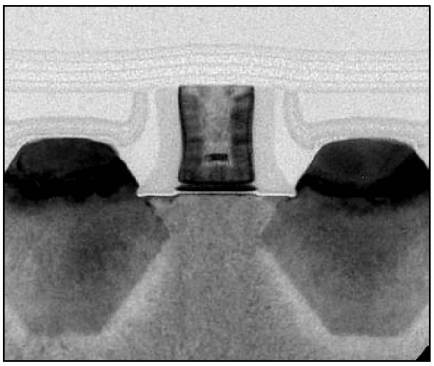

Fig.6 TEM micrograph of high-k + metal gate PMOS transistor.

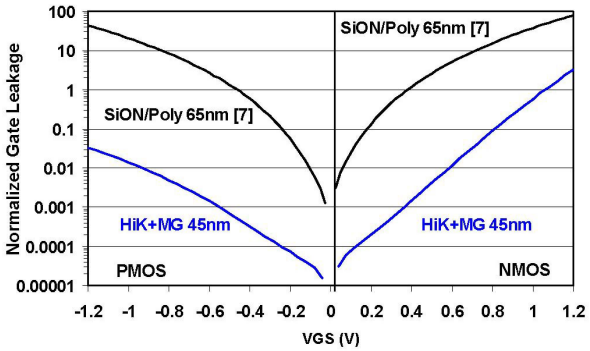

Fig.7 HiK+MG enables 25-1000X gate leakage reduction.

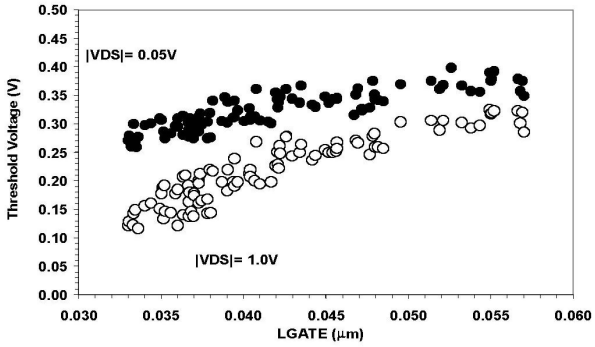

Fig.8 NMOS VT vs. LGATE showing good VT rolloff & DIBL

Excellent short channel characteristics are observed due to T_{OX} scaling and optimal workfunction metal gates (Fig. 8,9).

PMOS performance is improved by using high-k+MG as well as by increasing the Ge content of the embedded SiGe to 30% from 23% (65nm [8]) and 17% (90nm [6]) and by reducing SiGe proximity to the channel. Drive currents are benchmarked at 1.0V, a low 100nA/µm I_{OFF} and at 160nm contacted gate pitch. PMOS drive current (Fig. 10) of 1.07 mA/µm demonstrates 51% improvement over 65nm [8].

NMOS drive current (Fig. 11) is 1.36mA/µm, 12% better than our 65nm transistors [8]. The average drive current improvement over 65nm is 32% at the same voltage and I_{OFF} despite scaled transistor pitch. These represent the best drive currents reported to date for 45nm technology at low I_{OFF}.

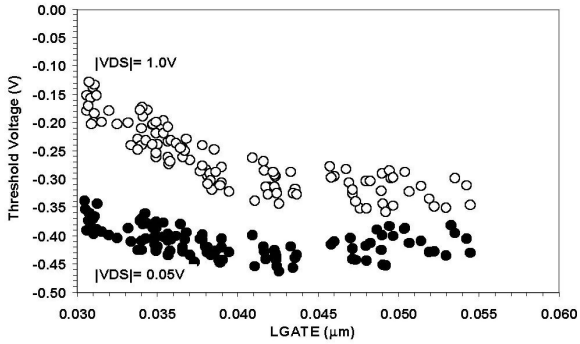

Fig. 9 PMOS VT vs. LGATE showing good VT rolloff & DIBL

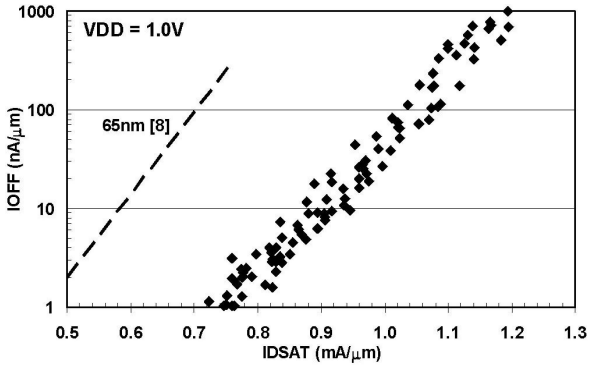

Fig.10 PMOS I_{DSAT} vs. I_{OFF} shows 1.07mA/µm at 1.0V & 100nA

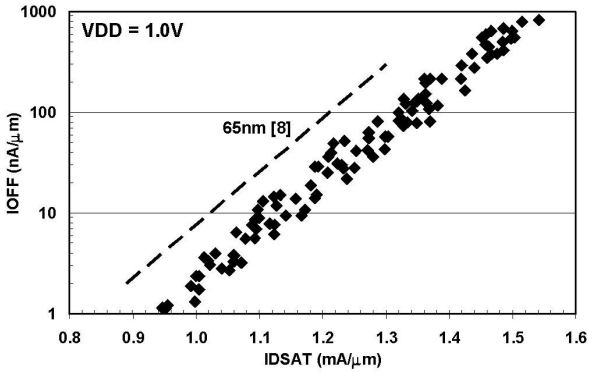

Fig.11 NMOS I_{DSAT} vs. I_{OFF} shows 1.36mA/µm at 1.0V & 100nA

The transistor performance gains are reflected in ring oscillator performance. Fanout=2 gate delay is benchmarked at a low 100nA/µm I_{OFF} each for NMOS and PMOS, at 1.2V for 65nm [8] and a lower 1.1V for 45nm. The ring oscillators use the minimum contacted gate pitch (220nm and 160nm) for each technology. Despite the scaling of both voltage and contacted gate pitch, FO=2 gate delay is reduced from 6.65pS (65nm) to 5.1pS (45nm), a gain of 23% (Fig. 12).

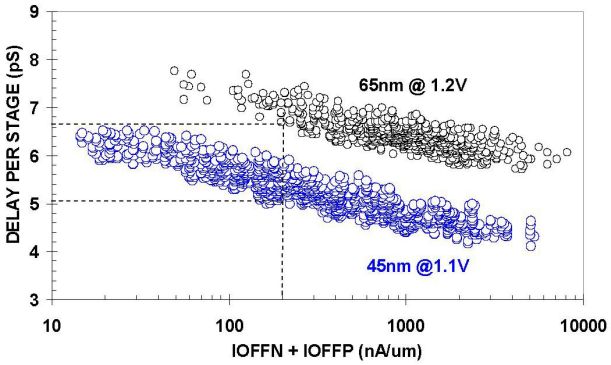

Fig.12 FO=2 ring oscillator delay vs leakage for 45nm vs 65nm

TRANSISTOR RELIABILITY

TDDB and bias-temperature reliability of high-k + metal transistors have been a concern [3], driven in part by the propensity for oxygen vacancy formation [9]. By careful engineering and optimization of the gate stack, the reliability

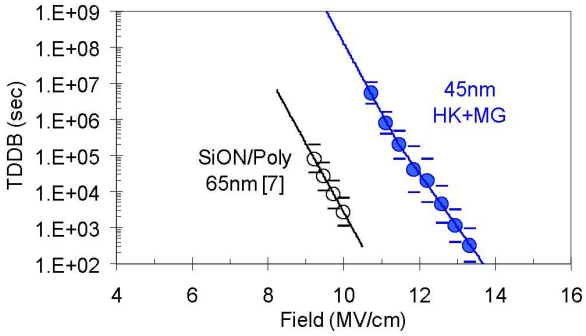

Fig. 13 NMOS TDDB time to fail vs. electric field

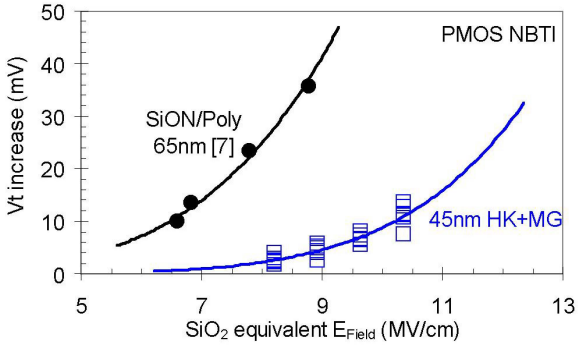

Fig. 14 PMOS NBTI V_T shift vs. electric field

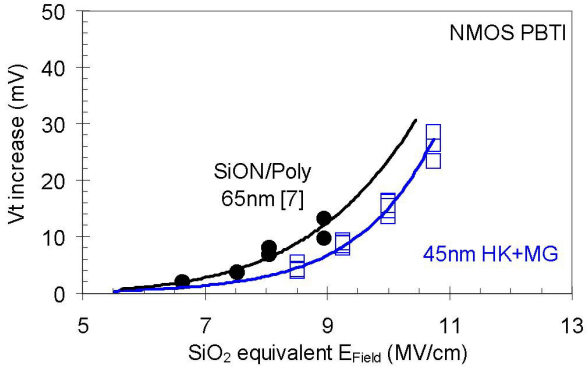

Fig. 15 NMOS PBTI V_T shift vs. electric field

concerns have been overcome. Oxide breakdown (Fig. 13) is improved relative to 65nm SiON transistors, supporting 30% higher E-field. PMOS NBTI (Fig. 14) is improved compared to 65nm SiON transistors at the same E-field and is matched at 50% higher E-field. NMOS PBTI (Fig. 15) is better than 65nm and supports 15% higher E-field; the net BT shift for NMOS and PMOS is matched to 65nm at 30% higher field. Note that while NMOS transistors are considered stable for SiON/Poly, they actually show PBTI at very high E-fields.

INTERCONNECTS

Nine layers of copper interconnect are employed along with low-k CDO dielectrics (Fig. 16). Lower layer metal pitches are matched to the contacted gate pitch, while upper layer metal pitches increase progressively to optimize density and performance. Compared to 65nm [7] interconnect capacitance is reduced by aggressive scaling of the SiCN etch stop layer, and by extending the use of CDO to more layers, including Metal-1. The Metal-9 layer is very thick and is used for improved on-die power distribution. Packaging is 100% Pb-free with Cu bumps and SnAgCu solder. Interconnects are optimized to reliably withstand the added stress of Pb-free packaging on CDO films.

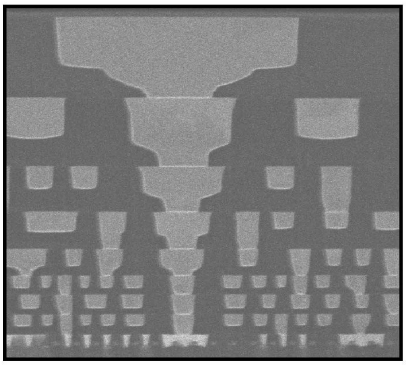

Fig.16 Cross-section of 8 of the 9 Cu interconnect layers

SRAM AND PRODUCTS

The 45nm yield learning vehicle was a 153Mbit SRAM featuring a 0.346μm^2 SRAM cell and over a billion transistors. The first fully functional 45nm 153Mb SRAM was reported in Jan 2006; yields are now at mature levels. The SRAM has demonstrated 3.8 Ghz operating frequency at 1.1V power supply and stable low voltage operation (Fig. 17). High yield has also been demonstrated on microprocessors for server, desktop, mobile & handheld applications (Fig. 18).

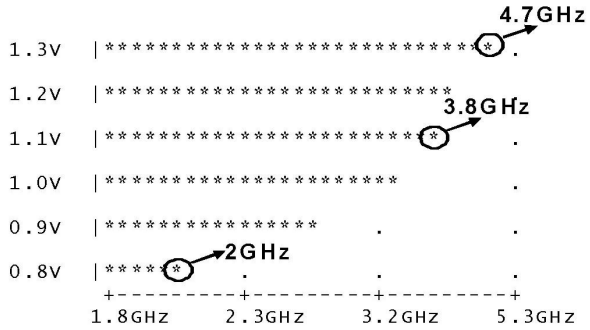

Fig. 17 Voltage-Frequency shmoo for 153Mb SRAM

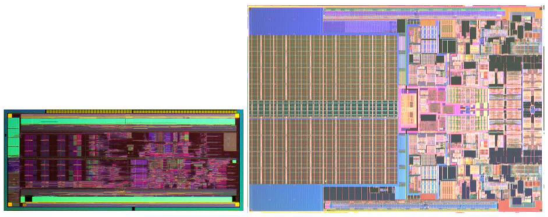

Fig. 18 Die photos of single core & dual core microprocessors

CONCLUSIONS

For the first time, high-k + metal gate transistors have been integrated into a manufacturable 45nm process. Combined with third generation strained silicon these transistors provide record drive current at low leakage and at tight contacted gate pitch. Ring oscillators demonstrate 23% gate delay reduction compared to 65nm [8] at the same I_{OFF} and 10% lower V_{DD}.

Low-k CDO is employed for low interconnect RC delay and is integrated with 100% Pb-free packaging. Aggressive pitch scaling and trench contact based local routing achieve good layout density, while low cost is maintained using novel 193nm dry patterning techniques for critical layers. The technology maintains historical scaling trends for performance and density. Mature yield has been demonstrated and the technology is now in high volume manufacturing.

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