# A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-node high-performance pMOSFET Technology

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***Abstract*—We have presented the high performance pMOSFET with embedded SiGe (eSiGe) technique which is applicable to 32 nm node ground rule (dense gate space) [1]. In general, close eSiGe S/D structure to the channel improves pMOSFET performance because of higher strain in the channel. However, we found the relation between boron diffusion modulation in SiGe region and short channel effect (SCE) in the context of eSiGe proximity change. Therefore, additional source drain extension (SDE) optimization is required to improve device performance with close eSiGe structure focusing on parasitic resistance reduction. As a results, we have demonstrated high drive current of 755 µA/µm at $V_{dd}$ = 1.0 V, $I_{OFF}$ = 100 nA/µm, 30 nm gate length pMOSFET.**

## I. INTRODUCTION

From 90 to 45 nm node, device scaling strategy has modulated mainly because of two reasons: gate oxide thickness and shallow junction depth limitations. For the continual performance improvement of 32 nm node MOSFET, stress techniques such as eSiGe [2-4] and stress liner [5] are indispensable. Various channel stress techniques have been proposed so far, however, eSiGe technique is the most effective stress booster for pMOSFET; accordingly, optimization of eSiGe process becomes significant for the further performance improvement. In eSiGe technique, eSiGe proximity to channel is dominant parameter for increasing channel strain as shown Fig. 1. From the viewpoint of parasitic resistance, in-situ boron-doped eSiGe structure exhibits higher performance than non-doped eSiGe structure with S/D implantation [6]. However, in-situ boron-doped eSiGe device tends to degrade short channel behavior at close eSiGe proximity structure. Therefore, boron-implanted eSiGe device has an advantage to suppress SCE with close eSiGe structure. In this work, eSiGe proximity impact on device performance enhancement is discussed considering two key parameters; 1) mobility enhancement 2) SDE resistance reduction in SiGe region owing to boron diffusion modulation. As a results, high drive current of 755 µA/µm $V_{dd}$= 1.0 V, $I_{OFF}$= 100 nA/µm, 30 nm gate length, is demonstrated.

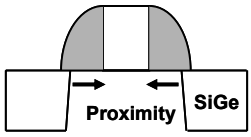



Figure 1. eSiGe proximity is key for mobility enhancement and SDE resistance reduction.

## II. DEVICE FABRICATION

The process sequence of eSiGe pMOSFET is illustrated in Fig. 2. Following the gate electrode formation, dummy SiN spacer was formed, where the thickness of dummy spacer defines the distance between channel and eSiGe. In this work, dummy spacer thickness was changed from 25 nm to 5 nm. While dummy spacer was used as a mask, anisotropic RIE process was applied to make recessed Si shape. Next, non-doped eSiGe was deposited by utilizing selective epitaxial growth on recessed Si regions. Ge concentration in eSiGe is 20at%. After dummy spacer strip, offset spacer was formed and SDE implantation was performed. Next, final spacer formation, SD implantation and spike activation annealing were performed. Finally, silicide films were formed on gate, source and drain, followed by metallization process.

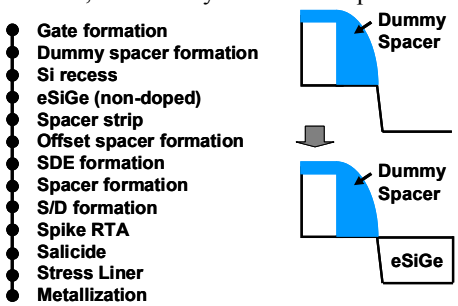



Figure 2. Process sequence of pMOSFET

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## III. Experimental Results

The eSiGe proximity to channel is key parameter to increase the channel strain. To reduce distance from eSiGe to channel, SiN dummy spacer was scaled down from 25 nm to 15, 10, 5 nm. Figure 3 shows cross-sectional TEM pictures of MOSFET with each eSiGe proximity structure. It is confirmed that the eSiGe proximity to channel is approximately the same as dummy spacer thickness.

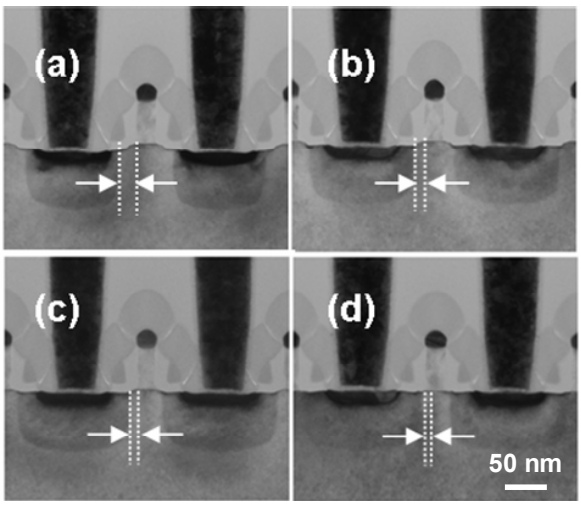



Figure 3. Cross-sectional TEM pictures of MOSFETs with different eSiGe proximity which is controlled by dummy spacer thickness. Here, eSiGe proximity is changed from (a) 25 nm, (b) 15 nm, (c) 10 nm to (d) 5 nm.

$I_{ON}$ versus $L_G$ at $I_{OFF}$= 100 nA/um for each eSiGe proximity (5, 10, 15, 25 nm) are shown in Fig. 4. Here, shorter gate length indicates the suppression of SCE and larger $I_{ON}$ shows the improvement of current drive. In this experiment, identical process condition and device parameters were used for all devices except for dummy spacer width.

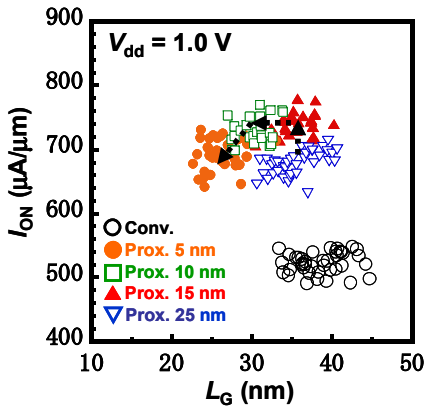



Figure 4. $I_{ON}$-$L_G$ characteristics of each eSiGe proximity device

It can be seen that eSiGe device exhibits higher current drive than that conventional device without SCE degradation. The strain in the channel of each proximity device was measured by NBD (Nano Beam Diffraction) measurement as shown in Fig. 5. Both x-direction compressive and y-direction tensile strain are increased as decreasing proximity. However, eSiGe proximity from 10 nm to 5 nm exhibits decrease of x-direction strain corresponding to degradation of current drive (Fig. 4). One possible cause of strain relaxation could be a generation of crystal defects in eSiGe.

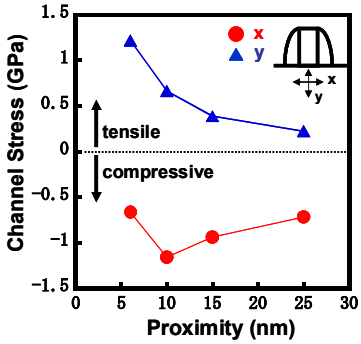



Figure 5. Channel stress vs eSiGe proximity. Channel stress enhancement is observed with reduction of eSiGe proximity.

In following section, device performance dependency on SiGe proximity is analyzed from viewpoint of the mobility enhancement and suppression of boron diffusion.

### *A. Hole mobility enhancement*

15 nm eSiGe proximity device exhibits higher drive current than 25 nm eSiGe proximity device at the same SCE behavior (Fig. 4). A smaller slope in $R_{ON}$ vs $L_G$ plot indicates higher hole mobility in channel. This means hole mobility in 15 nm eSiGe proximity device shows higher than that in 25 nm eSiGe proximity device (Fig. 6). This result exhibits higher drive current is mainly owing to hole mobility improvement by reduction of eSiGe proximity from 25 nm to 15 nm. However, a slope in 10 nm eSiGe proximity device has slight improvement comparing to 15 nm eSiGe proximity device. Furthermore, $I_{ON}$ of 10 nm eSiGe proximity device shows no improvement from 15 nm eSiGe proximity device.

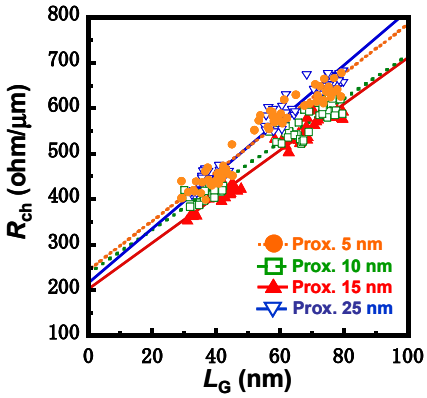



Figure 6. $R_{ch}$-$L_G$ characteristics of each eSiGe proximity deivce

This is caused by boron diffusion modulation in SiGe which is discussed in next section in detail. Finally, extreme proximity 5 nm shows degradation in current drive and $R_{ON}$-$L_G$ slope. This is explained by strain reduction which is shown in Fig. 6.

### *B. Diffusion of source and drain boron*

Figure 7 shows $V_{TH}$ roll-off characteristics of 15 to 5 nm eSiGe proximity device. Here, it is obvious that reduction of eSiGe proximity improves short channel immunity from 15 nm to 5 nm.

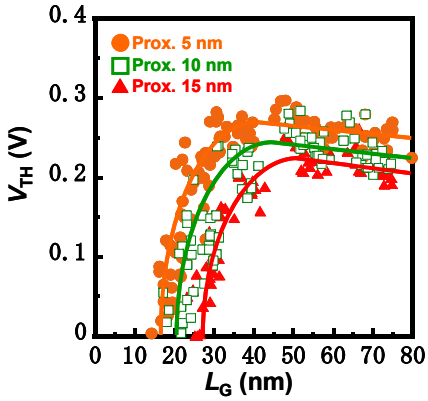



Figure 7. $V_{TH}$ roll-off characteristics of each eSiGe proximity device.

This is because the suppression of boron diffusion in eSiGe. In 15 nm eSiGe proximity device, extension region is mainly in Si. However, in 5 and 10 nm eSiGe proximity device extension region is in SiGe region as shown in Fig. 8.

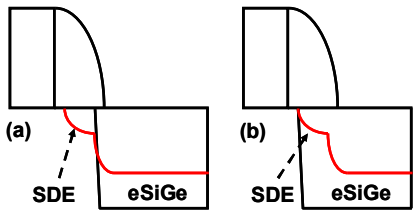



Figure 8. Schematic of correlation between eSiGe and SDE positions. Here, eSiGe proximity is (a) 15 nm (b) 5, 10 nm.

The boron profile by SIMS in Si and SiGe is shown in Fig. 9. The boron profile in SiGe is shallower and more abrupt than that in Si. This result indicates the formation of shallower junction in SiGe than that in Si with same implantation and annealing condition.

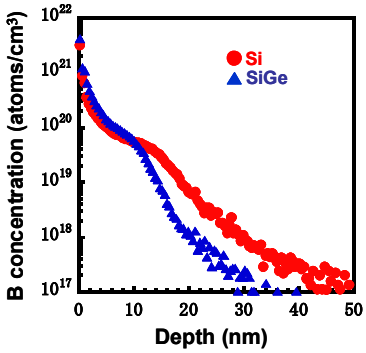



Figure 9. SIMS depth profiles of boron in Si and SiGe regions.

The extension sheet resistance (Rs) and junction depth (Xj) in both Si and SiGe are plotted in Fig. 10. Here, Xj is defined as the depth from surface at boron concentration is 5e18 (atom/cm$^{-3}$). Activation annealing condition is same for all samples with changing implantation energy. In Rs-Xj plot, SDE in SiGe shows shallower Xj at same extension sheet resistance. There are two reasons to explain this result. One is the reduction of boron diffusion in SiGe, and the other is the higher boron activation rate in SiGe.

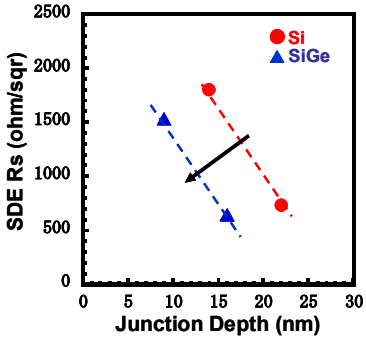



Figure 10. Xj-SDE Rs relationships. Suppression of Boron diffusion and higher activation in SiGe region improves Xj-Rs relationships in eSiGe devices.

In order to investigate the impact of boron diffusion difference between eSiGe and conventional device, 2D SDE profile is simulated by TCAD where boron diffusivity is calibrated by SIMS data. Figure 11 shows junction profile simulation results for each eSiGe proximity devices using same implantation and annealing conditions. Here, obvious SDE shape modulation is observed. As explained at Fig. 8, SDE in close proximity device is wrapped around SiGe region. Then boron diffusion is suppressed for both vertical and lateral direction. This is the reason of SCE suppression which is observed in Fig. 7.

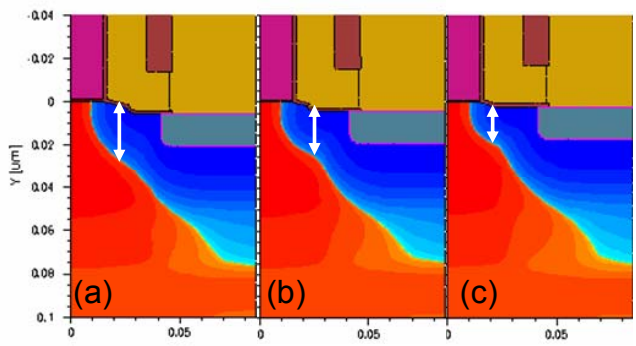



Figure 11. Boron profiles for each device by TCAD simulation. eSiGe Proximity is (a) 15 nm (b) 10 nm (c) 5 nm

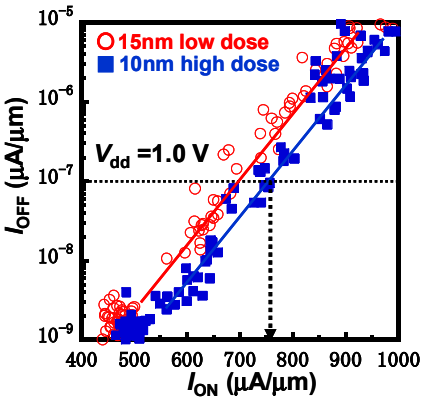



Figure 13. $I_{ON}$-$I_{OFF}$ characteristics at the same $I_{GD}$.

### C. *SDE Optimization*

Previous discussion suggests the best performance should be achieved by 10 nm eSiGe proximity device from the viewpoint of channel strain and SCE as shown Fig. 4, 6, 7. However, current drive with 10 nm eSiGe proximity device is comparable to that with 15 nm eSiGe proximity device as shown in Fig. 5. This is because the suppression of boron diffusion in eSiGe causes small gate and source/drain overlap. In order to increase the overlap, higher SDE implantation dosage was applied to 10 nm eSiGe proximity device. As shown in Fig. 12, optimized 10 nm eSiGe proximity device exhibits higher current drive than 15 nm eSiGe proximity device at the same $I_{GD}$, where the extension overlap is matched. This enhancement is achieved by parasitic resistance reduction.

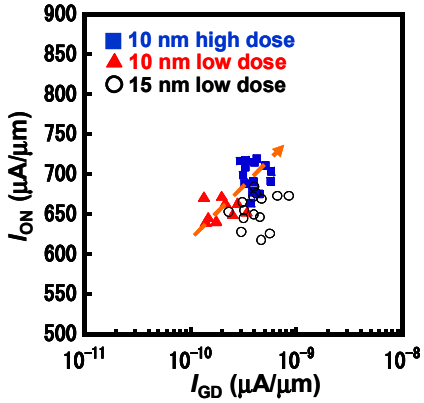



Figure 12. $I_{ON}$-$I_{GD}$ characteristics. 10 nm eSiGe proximity device with higher SDE implantation dosage exhibits improved drive current at the same $I_{GD}$.

This result suggests the importance of SDE optimization considering boron diffusion modulation in case of eSiGe proximity optimization. As a result of optimization, the device with 10 nm eSiGe proximity exhibits 15% drive current improvement in $I_{ON}$-$I_{OFF}$ plot compared to the device with 15 nm eSiGe proximity as shown Fig. 13.

## IV. Conclusion

The eSiGe proximity to channel is key optimization point to achieve high performance pMOFET. In this optimization, it is found that boron diffusion modulation in SiGe plays the important role to dominate SCE and parasitic resistance. After the optimization of eSiGe proximity and SDE implantation, high drive current of 755 μA/μm at $V_{dd}$= 1.0 V, $I_{OFF}$= 100 nA/mm, 30 nm gate length, is demonstrated.

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