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INTRODUCTION TO SEMICONDUCTOR MANUFACTURING TECHNOLOGY

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AUSTIN COMMUNITY COLLEGE

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**To my wife, Liu Huang
and my son, Jarry Xiao**

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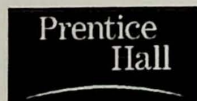
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8.2 ION IMPLANTATION BASICS

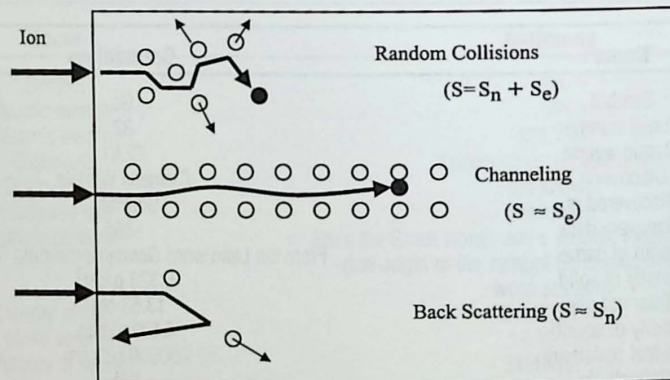
8.2.1 Stopping Mechanisms

When ions bombard and penetrate the silicon substrate, they collide with lattice atoms. The ions gradually lose their energy, and eventually stop inside the silicon. There are two stop mechanisms. One is when the implanted ions collide with nuclei of the lattice atoms, are scattered significantly by the collision, and transfer energy to the lattice atoms. This is called *nuclear stopping*. In this "hard" collision, lattice atoms can get enough energy to break free from the lattice binding energy, which causes crystal structure disorder and damage. Another stop mechanism is when incidental ions collide with electrons of the lattice atoms. The incident ion path in the electronic collision is almost unchanged, energy transfer is very small, and crystal structure damage is negligible. This "soft" collision is called *electronic stopping*. The total stopping power, which is the energy loss of the ion per unit distance it travels inside the substrate, can be expressed as:

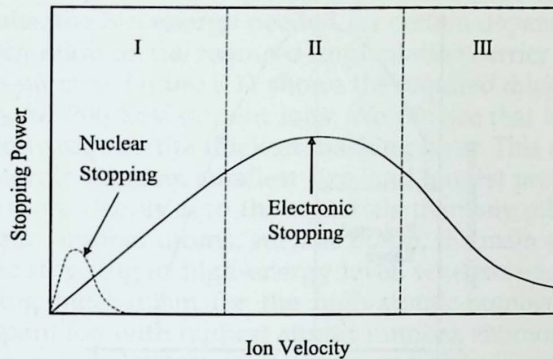
$$S_{total} = S_n + S_e$$

Here S_n is the nuclear stopping power and S_e is the electronic stopping power. Figure 8.6 illustrates the stopping mechanisms, and Figure 8.7 shows the relationship between stopping power and ion velocity.

Figure 8.6
Different stopping mechanisms.



The ion energy of the ion implantation process ranges from ultralow energy of 0.5 keV for ultrashallow junction (USJ) to high energy of 1 MeV for well implantation, which is located in region I of Figure 8.7. From the far-left side of the figure, we can see that the main stopping mechanism is nuclear stopping for the low-energy and high-atomic-number ion implantation processes. For high-energy, low-atomic-number ion implantation, electronic stopping mechanism is more important.

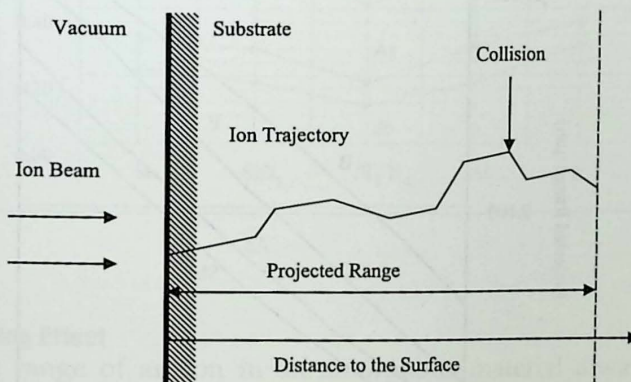
**Figure 8.7**

Different stopping mechanisms.

Source: Redrawn from S.A. Cruz, "On the Energy Loss of Heavy Ions in Amorphous Materials"

8.2.2 Ion Range

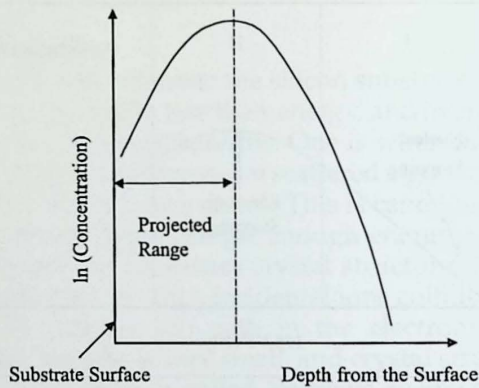
Energetic ions penetrate the target, gradually lose their energy through collisions with the atoms in the substrate, and eventually rest inside the substrate. Figure 8.8 shows the trajectory of an ion inside the substrate and the definition of the ion projected range.

**Figure 8.8**

Ion trajectory and projected range.

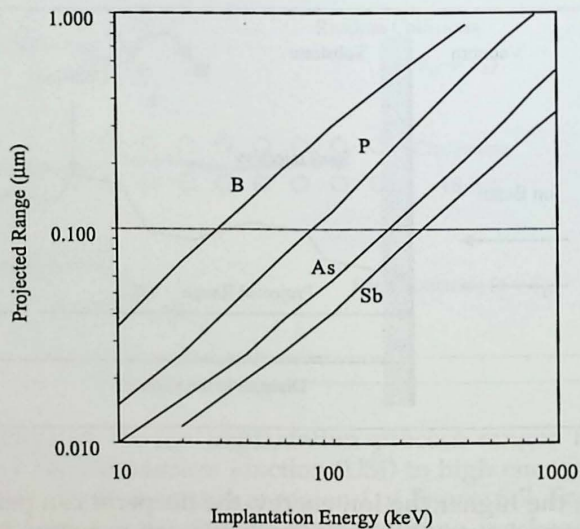
Generally, the higher the ion energy, the deeper it can penetrate into the substrate. However, even with the same implantation energy, ions do not stop exactly at the same depth in the substrate, because each ion has different collisions with different atoms. The projected ion range always has a distribution, as illustrated in Figure 8.9.

Figure 8.9
Distribution of the
projected ion range.



Higher-energy ion beams can penetrate deeper into the substrate, and therefore have a longer projected ion range. Since smaller ions have smaller collision cross sections, smaller ions at the same energy level can penetrate deeper into the substrate and the mask materials. Figure 8.10 illustrates the projected range at different energy level for boron, phosphorus, arsenic, and antimony ions in the silicon substrate.

Figure 8.10
Projected range
of dopant ions in
silicon.



Projected ion range is an important parameter for ion implantation, because it indicates the ion energy needed for certain dopant junction depth. It also gives information on the required implantation barrier thickness for the ion implantation process. Figure 8.11 shows the required thickness of different barrier materials for 200-keV dopant ions. We can see that for ion energy of 200 keV, boron ions require the thickest masking layer. This is because boron has the lowest atomic number, smallest size, and longest projection range, so it can penetrate more deeply into the materials than any other dopant ions. For the low-atomic-number atoms, such as boron, the main stopping mechanism is electronic stopping at high-energy level, whereas nuclear stopping is the main stopping mechanism for the high-atomic-number dopant atoms. Similarly, the dopant ion with highest atomic number, antimony, has the highest stopping power and shortest projection range, therefore requires thinnest masking materials.

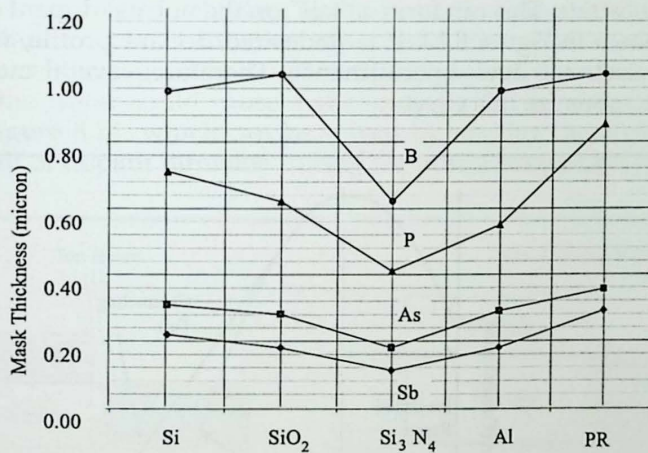
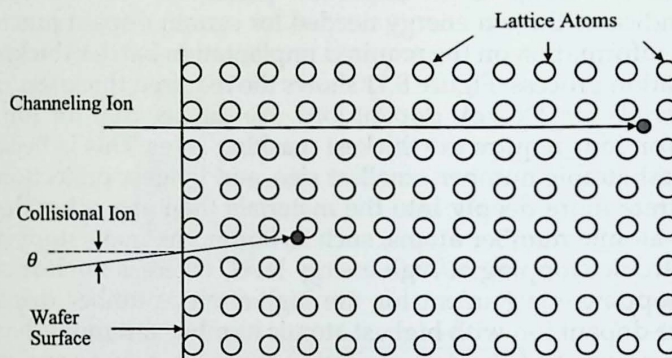


Figure 8.11
Required barrier
thickness for
200-keV dopant
ions.

8.2.3 Channeling Effect

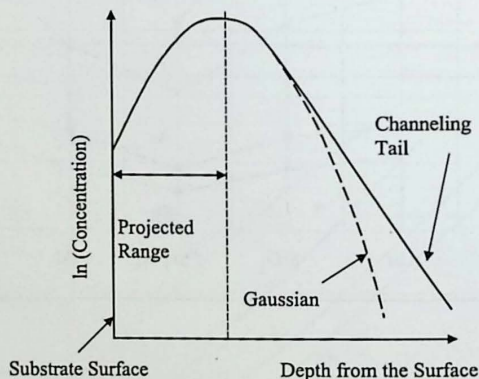
The projected range of an ion in an amorphous material always follows Gaussian distribution, also called normal distribution. In single-crystal silicon, the lattice atoms have orderly arrangement, and lots of channels can be seen at certain angles. If an ion with the right implantation angle enters the channel, it can travel a long distance with very little energy loss, as illustrated in Figure 8.12. This is called *channeling effect*.

Figure 8.12
Channeling effect.



The channeling effect causes some ions to penetrate deeply into the single-crystal substrate. This can form a "tail" on the normal dopant distribution curve, as shown in Figure 8.13. It is undesired dopant profile, which could affect microelectronic device performance. Therefore, several methods have been used to minimize this effect.

Figure 8.13
Dopant distribution with channeling effect.



Question

The channeling effect allows an ion to penetrate deeply into single-crystal silicon substrate with relatively low energy. Why don't people try to apply this effect to create deep dope junctions without very high ion energy?

Answer

If all ions of the ion beam are perfectly vertically implanted into the substrate, the channeling effect might really be applied for the deep junction formation with relatively low energy. However, ions always expel each other due to the Coulomb force of the same kind of charge, so the ion beam can't be perfectly parallel. This means that many ions collide with the wafer surface at a small tilt angle and will start to have a lot of nuclear collisions with lattice atoms immediately after they penetrate into the substrate. The result is some ions channeling deep into the substrate, and many ions stopped, as in the normal Gaussian distribution.

One way to minimize the channeling effect is ion implantation on a tilted wafer, typically with a tilt angle of $\theta = 7^\circ$. By tilting the wafer, the ions impact with the wafer at an angle and cannot reach the channel, as shown in Figure 8.12. The incident ions will have nuclear collisions right away, and effectively reduce the channeling effect. Most ion implantation processes use this technique to minimize the channeling effect, and most wafer holders of ion implanters have the capability to adjust tilting angle of the wafer.

Tilting the wafer could cause a shadowing effect by the photoresist, as shown in Figure 8.14, which can be solved by rotating the wafer and/or a small amount of dopant diffusion during the postimplantation annealing.

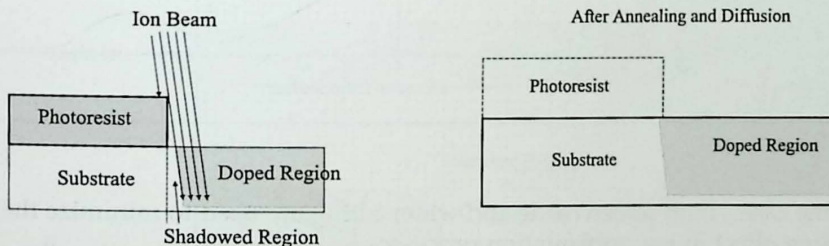
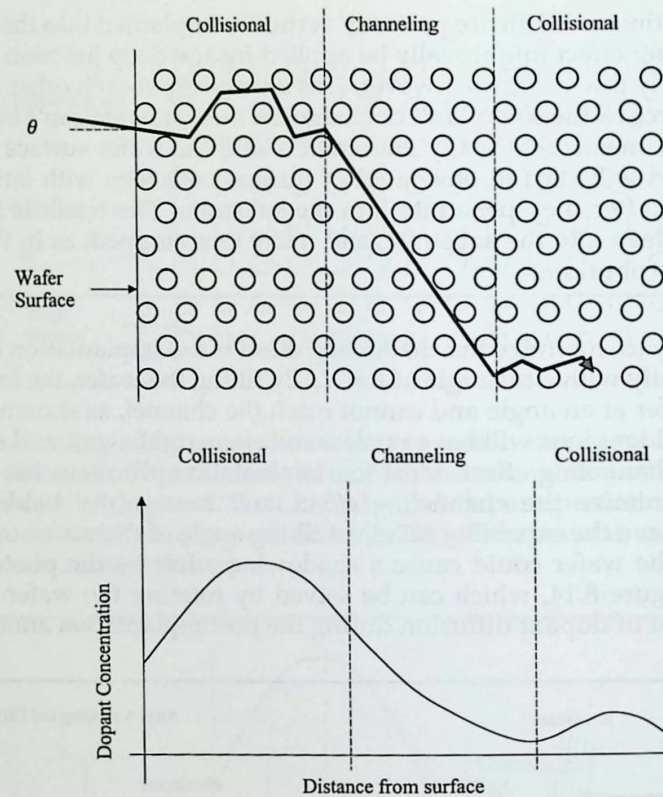


Figure 8.14
Shadowing effect
and diffusion
treatment.

If the tilt angle is too small, sometime the dopant concentration in silicon can form a hump distribution due to the channeling effect, as shown in Figure 8.15.

Another widely used method to deal with the channeling problem is implantation through a thin layer of screen silicon dioxide. Thermally grown silicon dioxide is an amorphous material. The passing implantation ions collide with and scatter silicon and oxygen atoms in the screen layer before they enter the single-crystal silicon substrate. Due to collisional scattering, the pitch angle of ions to the silicon crystal will distribute in a wider range, thus reducing the chance of channeling. The screen oxide also can prevent the silicon substrate from contacting and being contaminated by masking photoresist. In

Figure 8.15
Postcollision chan-
neling effect.



some cases, both screen oxide and wafer tilting are used to minimize the channeling effect in ion implantation processes.

The problem with the screen layer is that some atoms in that layer can get high enough energy from the energetic ions to implant into the silicon. This is called the *recoil effect*. For a silicon dioxide screen layer, recoiling oxygen atoms can be implanted into the silicon substrate, forming a high-oxygen-concentration region in the silicon substrate near the silicon-oxide interface, which can degrade the carrier mobility and introduce deep-level trap. Therefore, in some implantation processes, screen oxide can't be used. In some cases, post-implantation oxidation and sacrificial oxide strip is needed to remove the oxygen-rich silicon layer. During the oxidation process, implantation-caused crystal damage can be annealed, and the oxide layer grows into the silicon substrate to consume the oxygen-rich region. Oxide stripping can remove the surface defect and the high-oxygen-concentration layer. However, for ultrashallow junction (USJ) implantation, this technique is inapplicable, since

oxidation can cause too much dopant diffusion and consumes the shallow silicon junction from the substrate.

High-current silicon or germanium ion implantation can heavily damage the single-crystal lattice structure and create an amorphous layer near the wafer surface. Si or Ge amorphous implantation process can completely eliminate the channeling effect because, in an amorphous substrate, the dopant junction profile formed by ion implantation always follows Gaussian distribution, which is predictable, repeatable, and controllable. The trade-off for the preamorphous implantation solution is that it increases the production cost by adding an extra ion implantation step.

8.2.4 Damage and Annealing

In an ion implantation process, ions gradually lose their energy by colliding with lattice atoms, transferring their energy to these atoms in the process. The transferred energy is high enough for these atoms to break free from the lattice-binding energy, typically about 25 eV. These freed atoms also collide with other lattice atoms while traveling inside the substrate, and knock them free from the lattice by transferring enough energy to them. These processes continue until none of the freed atoms have enough energy to free other lattice atoms. One energetic ion can cause thousands of displacements of lattice atoms. Damage caused by an energetic implanted ion is shown in Figure 8.16.

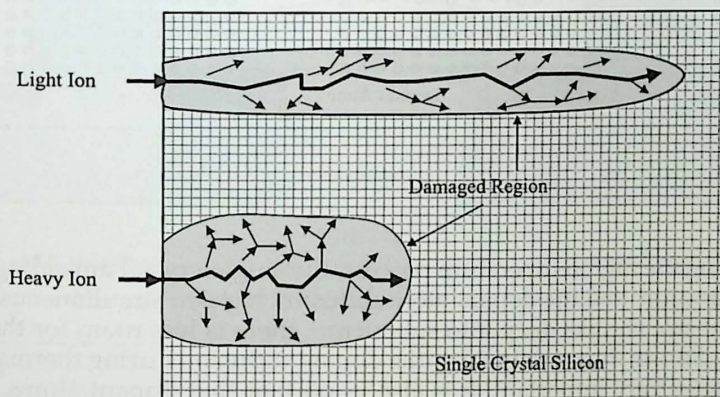


Figure 8.16
Damage caused by one ion.

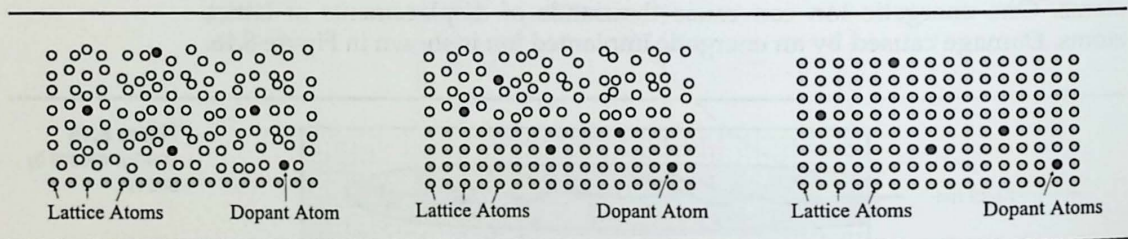
The damage created by one ion can be quickly self-annealed by the thermal movement of the atoms inside the substrate at the room temperature. However, in an ion implantation process, the amount of ions is so large that it always causes such substantial lattice damage in the single-crystal substrate that the layer close to the surface becomes amorphous, and the self-annealing process can't repair the crystal damage in a short time. The damage effect is

related to the dose, energy, and mass of the ion species; it increases when dose and ion energy increase. If the implantation dose is high enough, the substrate crystal structure can be completely destroyed and become amorphous near the substrate surface within the ion range.

To achieve device requirement, the lattice damage must be repaired in an annealing process to restore the single-crystal structure and activate the dopant. Only when dopant atoms are at the single-crystal lattices can they effectively provide electrons or holes as the majority carriers for electric current. In a high-temperature process, atoms get energy from the heat and start rapid thermal motion. When they find the sites with the lowest free energy, which are located at single-crystal lattices, they stay there. Since the undamaged substrate underneath is single-crystal silicon, the silicon and dopant atoms in the damaged amorphous layer reconstruct the single-crystal structure there by falling into the lattice grids and being bonded by the lattice energy. Figure 8.17 illustrates the crystal recovery and dopant activation in the thermal annealing process.

Figure 8.17

Postimplantation annealing process.



During the high-temperature process, the single-crystal annealing, dopant atom activation, and the dopant atom diffusion happen simultaneously. When IC feature size shrinks deep into submicron, there is less room for the dopant atoms to diffuse; thus, minimizing the dopant diffusion during thermal annealing becomes very important. It is also important that dopant atoms in amorphous silicon have free thermal movement without any restriction; thus, they can diffuse much faster than they can in the single-crystal lattice, because the lattice binding energy severely restricts the movement of the dopant atoms. At a lower temperature, the diffusion process outpaces the annealing process; when the temperature is high enough, such as $> 1000^{\circ}\text{C}$, the annealing process is faster than the diffusion process. This is because the annealing activation energy ($\sim 5\text{ eV}$) is higher than the diffusion activation energy (3 to 4 eV).

Furnaces have been widely used for the postimplantation annealing process for a long time. Furnace annealing is a batch process, which normally operates from 850 to 1000 °C for about 30 minutes. Since the furnace annealing process takes a long time, the dopant atom diffusion can be quite substantial; thus for devices with small feature size it becomes unacceptable. Only for some noncritical implantation with large feature size, such as well implantation processes, furnaces may still be useful for the postimplantation annealing and dopant drive-in. For the critical doping processes such as source/drain implantation annealing, it can cause too much dopant diffusion and results in intolerable device performance for submicron microelectronic transistors.

Rapid thermal process (RTP) developed to anneal implantation-caused damages while minimizing dopant diffusion to meet the requirements of shrinking IC devices. RTP is a single-wafer system with temperature ramp rate up to 250 °C/sec and good temperature and temperature uniformity control at about 1100 °C. With the RTP system, the rapid thermal annealing (RTA) process can operate up to 1150 °C; at that temperature, the implantation damage can be annealed in less than 20 seconds. The RTA system can process a wafer in about a minute, from wafer in through temperature ramp up, anneal, wafer cool-down, and wafer out. For a comparison of furnace and RTP annealing, see Figure 8.18.

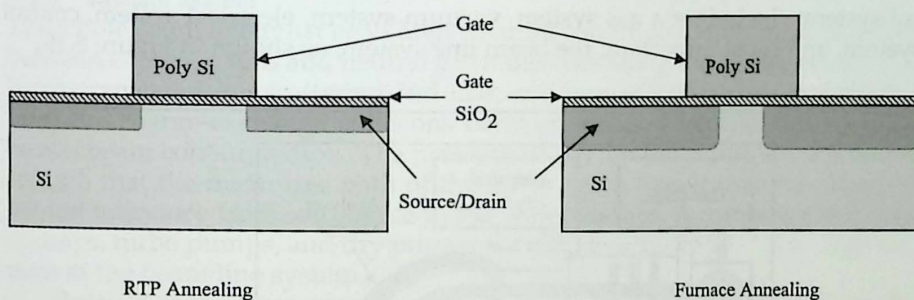


Figure 8.18
Dopant diffusion in
furnace and RTP
annealing
processes.

Question

Why can't the furnace temperature be ramped up and cooled down as quickly as a RTP system?

Answer

A furnace needs high power to ramp up temperature rapidly. It is difficult to ramp up temperature very fast without large temperature oscillation, due to temperature overshoot and undershoot.

Because of the slow temperature ramp rate, usually less than $10\text{ }^{\circ}\text{C}/\text{min}$, it takes a long time to ramp up the process tube from the idle temperature, normally between 650 and $850\text{ }^{\circ}\text{C}$, to the required annealing temperature, such as $1000\text{ }^{\circ}\text{C}$. Even as the temperature ramps up, part of the damage has already annealed. The wafers must be loaded into and unloaded from the furnace very slowly to prevent wafer warping from thermal stress caused by sudden temperature change. Because the furnace maintains high temperature during idle time, the wafers at the two ends of the wafer loader will have different annealing time due to the slow pushing and pulling, which could cause wafer-to-wafer nonuniformity.

RTA systems can ramp up wafer temperature from room temperature to $1100\text{ }^{\circ}\text{C}$ very quickly, normally within 10 seconds, with precise control of wafer temperature and temperature uniformity within the wafer. At about $1100\text{ }^{\circ}\text{C}$, the single-crystal lattice can be recovered in 10 seconds, with minimum dopant diffusion. RTA process has better wafer-to-wafer uniformity control than the furnace annealing process.

8.3 ION IMPLANTATION HARDWARE

An ion implanter is normally a very large piece of equipment, most likely the largest process equipment one can find in a semiconductor fab. It has several subsystems, including a gas system, vacuum system, electrical system, control system, and most important, the beam line system, as shown in Figure 8.19.

Figure 8.19
Schematic of an ion implanter.

