# A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 $\mu m^2$ SRAM Cell

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## I. Abstract

A 65nm generation logic technology with 1.2nm physical gate oxide, 35nm gate length, enhanced channel strain, NiSi, 8 layers of Cu interconnect, and low-k ILD for dense high performance logic is presented. Transistor gate length is scaled down to 35nm while not scaling the gate oxide as a means to improve performance and reduce power. Increased NMOS and PMOS drive currents are achieved by enhanced channel strain and junction engineering. 193nm lithography along with APSM mask technology is used on critical layers to provide aggressive design rules and a 6-T SRAM cell size of 0.57$\mu m^2$. Process yield, performance and reliability are demonstrated on a 70 Mbit SRAM test vehicle with >0.5 billion transistors.

## II. Introduction

The continuous push for improving performance and density of leading edge microprocessors provides the driving force for Si scaling following Moore's Law. The resulting increases in transistor counts and higher clock frequency, however, lead to higher chip power dissipation. While more power efficient microprocessor designs are clearly needed to counter the power dissipation problem, the new challenge for Si process is to place power dissipation as a key consideration, along with performance and density, for development of future process technologies.

## III. Key Technology Features

For this 65nm technology we use 1.2nm SiON gate oxide, which is not scaled from Intel's previous 90nm technology [1,2] in order to avoid an increase in gate oxide leakage. Maintaining constant gate oxide thickness while scaling gate length to 35nm provides ~20% reduction in gate capacitance, a significant factor in improving performance and reducing active power. Transistor drive currents are increased by means of ultra-shallow junctions and enhanced channel strain. Interconnect density and performance are improved with an added interconnect layer and by use of a low-k carbon-doped oxide layer and a lower-k etch stop layer for low capacitance, and Cu interconnect for low resistance. 193nm lithography combined with APSM mask technology enables aggressive design rule scaling (Table 1). The SRAM cell size is scaled to 0.57 $\mu m^2$ with stable low voltage operating characteristics. Figure 1 shows how contacted gate pitch and 6-T SRAM cell size values for this technology continue to stay on historic trend lines.

## IV. Transistor

A physical gate length of 35nm is achieved for this 65nm technology. Figure 2 shows gate length scaling trend for Intel's process technologies, where the 65nm technology follows the expected 0.7 scaling from 90nm technology. The gate length scaling is achieved, without a gate oxide thickness scaling, using ultra-shallow source-drains, with improved thermal cycles and co-implants. Figures 3 and 4 show cross-sections TEMs of NMOS and PMOS transistors with 35nm gate lengths and 220nm contacted gate pitches.

Drive currents are increased by optimization and enhancements of strain silicon techniques, first implemented in the 90nm generation [1,2]. For PMOS, we have adopted the same uniaxial strain approach using epitaxial SiGe film for source-drains, but significantly increased channel strain by 60%, by increasing Ge content in the SiGe film and optimizing the source-drain recess geometry. For NMOS, we have enhanced the channel strain by 80% from the use of tensile cap films. In addition, the ultra-shallow source-drains with abrupt junction play a significant role in controlling short channel effects and providing low Rext. Figures 5 and 6 show transistor I-V and subthreshold characteristics. Sub-threshold slopes are maintained at ~100mV/decade at 35nm gate lengths. Figures 7 and 8 show record $I_{ON}$-$I_{OFF}$ characteristics and are compared against record 90nm generation results. At 1.2V $V_{DD}$ and 100 nA/$\mu$m $I_{OFF}$ values, NMOS and PMOS saturated drive currents are 1.46 mA/$\mu$m and 0.88 mA/$\mu$m respectively. NiSi is used for low resistance polycide and source-drain salicide. Figure 9 shows low polycide sheet rho values down to 35nm gate lengths.

## V. Interconnects

8 layers of dual damascene Cu interconnects with low-k carbon-doped oxide (k=2.9) inter-level dielectric are used for this 65nm technology. A single SiCN etch stop layer (lower k than SiN used in previous technology generations) is used for each interconnect layer to reduce total capacitance by about 5% and minimize process complexity. Tungsten plugs are used for contacts to polysilicon gates and to source-drains. Metal pitches increase progressively from bottom to top to provide optimal density and performance (Table 1). To minimize interconnect RC delay and to improve density and electro-migration capability, aggressive metal aspect ratios of 1.8 are used. The aggressive design rules and metal aspect ratios for lower interconnect layers necessitate the use of 193nm lithography. As a comparison, the number of 193nm lithography layers for interconnect went from 2 in Intel's 90nm technology to 7 in 65nm technology. Low k inter-level dielectrics patterning with 193nm lithography present significant challenges due to different resist and their interaction with etch processes. Figure 10 shows a cross-section of the 8 interconnect layers. Figure 11 shows total RC delay by layer as a function of pitch and compares this technology against previous Intel generations.



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## VI. SRAM Test Vehicle

A fully functional 70 Mbit SRAM without redundancy, with >0.5 billion transistors and incorporating all of the features described in this paper, has been fabricated on this technology. The aggressive design rules allow for a small $0.57\mu m^2$ 6-T SRAM cell that is also compatible with high performance logic processing. A top view of the cell after poly patterning is shown in Figure 12. In addition to small size, this cell has a robust static noise margin down to 0.7V $V_{DD}$ to allow low voltage operation (Fig. 13). Figure 14 is a Shmoo plot for the 70 Mb SRAM operating frequency vs voltage, showing the SRAM operates at 3.43 GHz at 1.2V. A die photo is shown in Figure 15.

## VII. Conclusion

We have developed an industry leading 65nm CMOS technology for high performance microprocessors with excellent transistor and interconnect performance, along with aggressive dimensional scaling. A high performance, high density 70 Mbit SRAM test vehicle has been successfully fabricated utilizing all of the 65nm process features. This 65nm technology is on track for high volume manufacturing in 2005.

## References


[1] K. Mistry, et al., *Symp. VLSI Tech. Dig.*, 2004.

[2] T. Ghani, et al., *IEDM Tech. Dig.*, pp. 197-200, 2003.


| Layer | Pitch (nm) | Thick (nm) | AspectRatio |
|---|---|---|---|
| Isolation | 220 | 320 | - |
| Polysilicon | 220 | 90 | - |
| Contacted gate pitch | 220 | - | - |
| Metal 1 | 210 | 170 | 1.6 |
| Metal 2 | 210 | 190 | 1.8 |
| Metal 3 | 220 | 200 | 1.8 |
| Metal 4 | 280 | 250 | 1.8 |
| Metal 5 | 330 | 300 | 1.8 |
| Metal 6 | 480 | 430 | 1.8 |
| Metal 7 | 720 | 650 | 1.8 |
| Metal 8 | 1080 | 975 | 1.8 |

Table 1: Layer pitch, thickness and aspect ratio

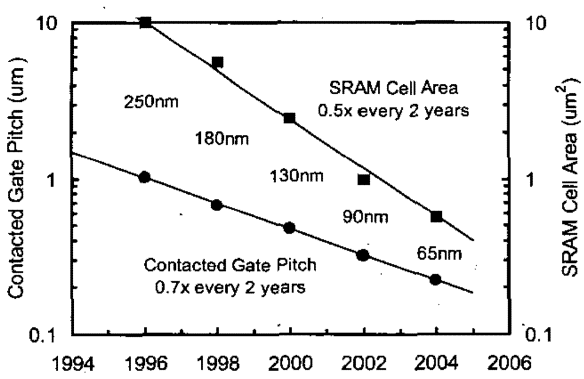


Figure 1: Intel contacted gate pitch and SRAM area trends

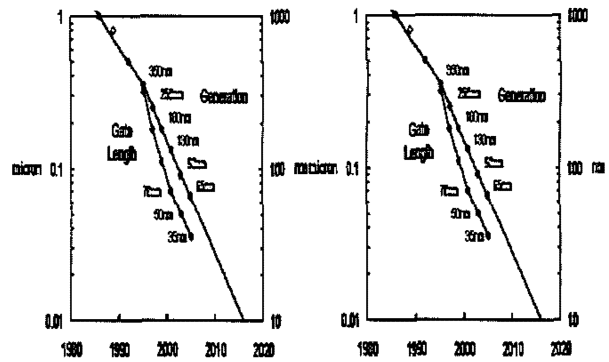


Figure 2: Transistor size trend for technology nodes.

Figure 3: TEM cross section of 35nm NMOS

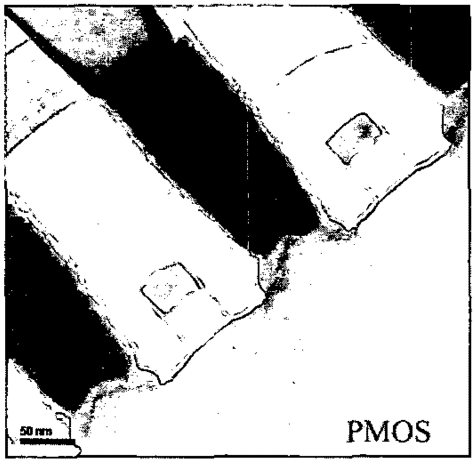


Figure 4: TEM cross section of 35nm PMOS

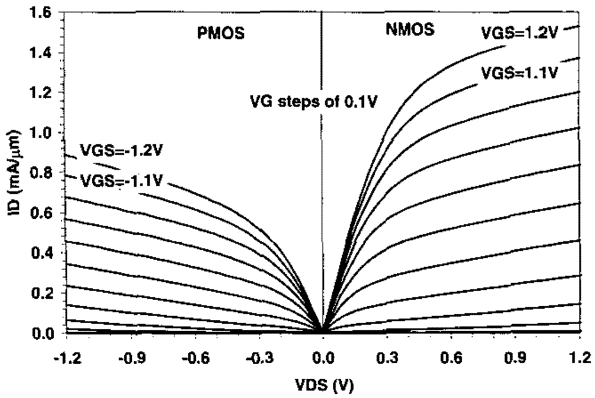


Figure 5: Transistor I-V curves

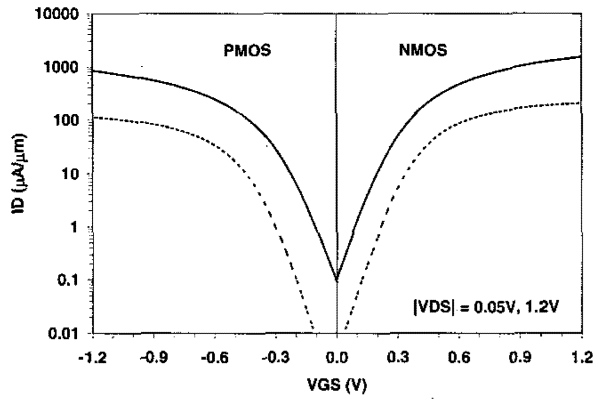


Figure 6: Sub-threshold curves for 35nm Lgate devices

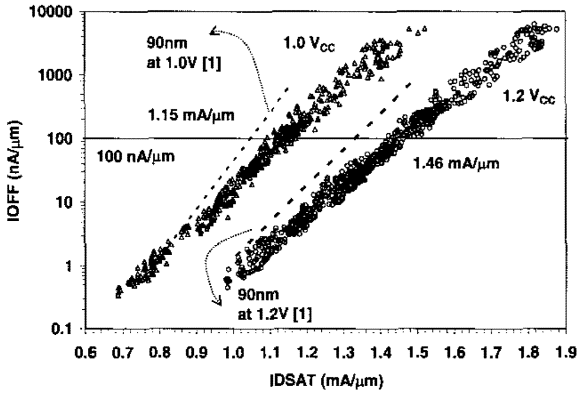


Figure 7: NMOS IDSAT vs IOFF at 1.0V and 1.2V

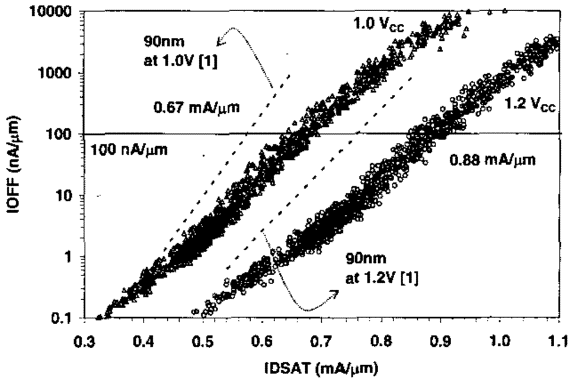


Figure 8: PMOS IDSAT vs IOFF at 1.0V and 1.2V.

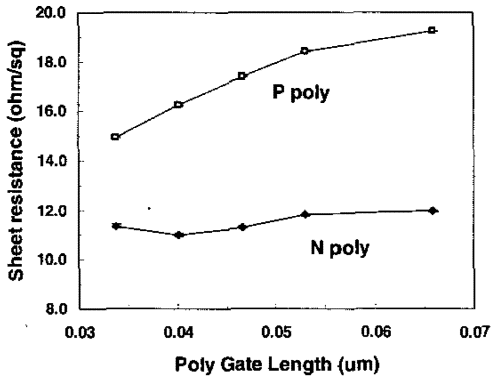


Figure 9: NiSi polycide resistance vs gate size

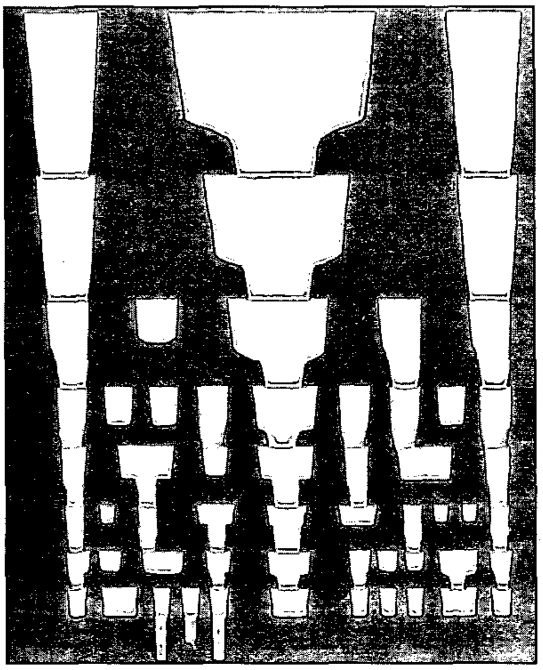

Figure 10: Cross-section: the dual damascene interconnects

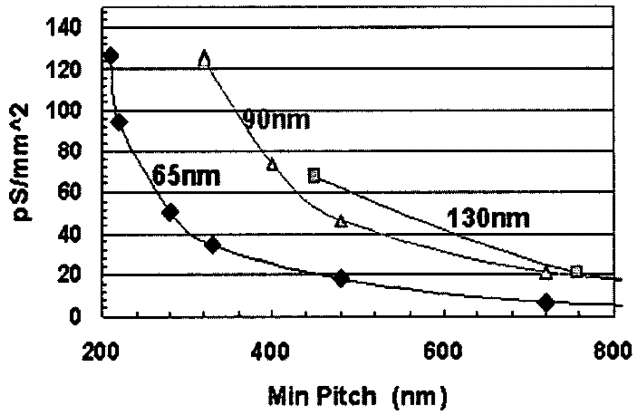


Figure 11: Interconnect RC delay for 1mm wire vs pitch

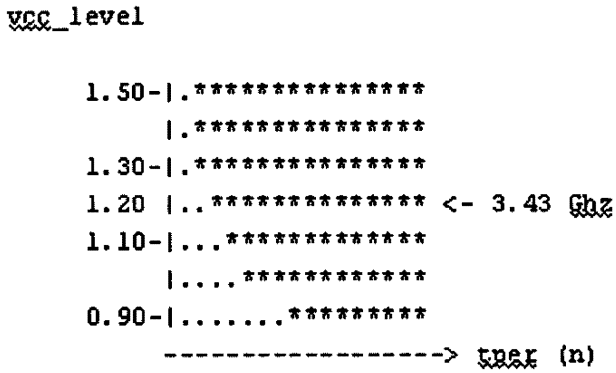


Figure 14: Shmoo plot for SRAM Fmax and Vcc

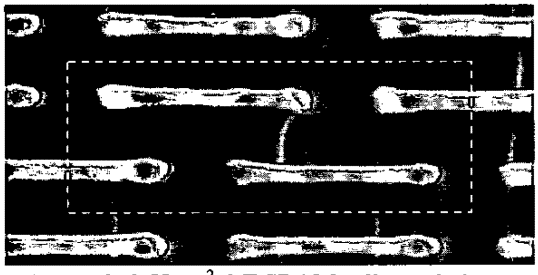

Figure 12: 0.57μm$^2$ 6-T SRAM cell at poly layer

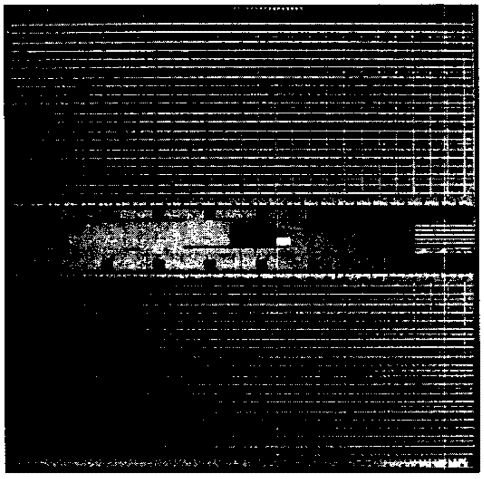

Figure 15: 70Mb SRAM test vehicle

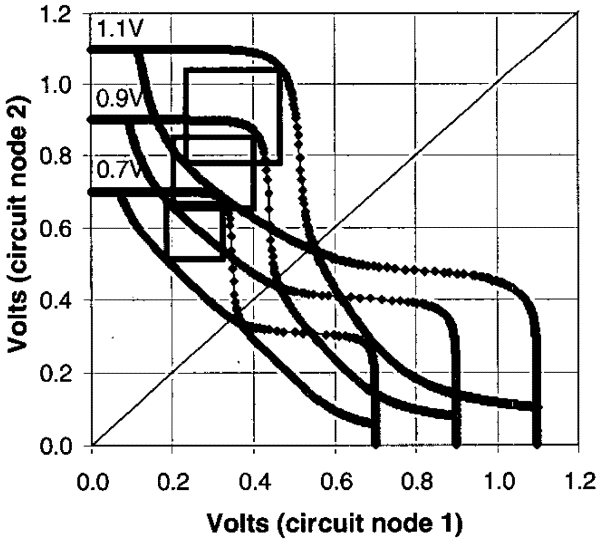


Figure 13: 0.57 μm$^2$ SRAM cell butterfly curve