

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner

v.

Daedalus Prime LLC,

Patent Owner

Patent No. 11,251,281 B2

Filing Date: May 22, 2020

Issue Date: February 15, 2022

Title: CONTACT RESISTANCE REDUCTION EMPLOYING
GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Inter Partes Review No. IPR2023-01121

PETITION FOR *INTER PARTES* REVIEW

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TABLE OF AUTHORITIES

Cases

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TABLE OF EXHIBITS

Exhibit	Description of Exhibit
1001	U.S. Patent No. 11,251,281 to Glass et al. (“’281 Patent”).
1002	Declaration of Dr. Scott E. Thompson, Ph.D. (“Thompson”).
1003	U.S. Patent Appl. Pub. No. 2008/0121932 A1 to Ranade (“ <i>Ranade</i> ”).
1004	U.S. Patent Appl. Pub. No. 2010/0123198 A1 to Kim et al. (“ <i>Kim</i> ”).
1005	U.S. Patent No. 7,611,943 to Liu (“ <i>Liu</i> ”).
1006	U.S. Patent Appl. Pub. No. 2010/0276761 A1 to Tung et al. (“ <i>Tung</i> ”).
1007	U.S. Patent No. 7,361,958 to Brask et al. (“ <i>Brask</i> ”).
1008	U.S. Patent Appl. Pub. No. 2009/0096002 A1 to Yu et al. (“ <i>Yu</i> ”).
1009	M.-H. Chi, <i>Challenges in Manufacturing FinFET at 20nm Node and Beyond</i> , Technology Development, GlobalFoundries (2012).
1010	U.S. Patent No. 6,413,802 to Hu et al.
1011	B. Doyle et al., <i>Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout</i> , Digest of the 2003 Symposium on VLSI Technology, pp. 133-34 (2003).
1012	M.C. Ozturk & J. Liu, <i>Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond</i> , 2005 AIP Conference Proceedings, International Conference on Characterization and Metrology for ULSI Technology, vol. 788, at 222-31 (Mar. 2005).
1013	U.S. Patent Appl. Pub. No. 2009/0075029 A1 to Thomas et al.
1014	G. Eneman et al., <i>Scalability of the Si_xGe_{1-x} Source/Drain Technology for the 45-nm Technology Node and Beyond</i> , IEEE Transactions on Electron Devices, vol. 53, no. 7, pp. 1647-56 (July 2006).

Exhibit	Description of Exhibit
1015	D.K. Sadana et al., <i>Applications of Epitaxy for Semiconductor Technology</i> , ECS Transactions, 218th ECS Meeting, vol. 33, no. 6, pp. 59-70 (Oct. 2010).
1016	U.S. Patent No. 7,767,560 to Jin et al.
1017	U.S. Patent No. 7,8,211,772 to Kavalieros et al.
1018	U.S. Patent No. 7,288,443 to Zhu.
1019	U.S. Patent Appl. Pub. No. 2010/0148217 A1 to Simonelli et al.
1020	U.S. Patent Appl. Pub. No. 2007/0187767 A1 to Yasutake.
1021	J.-P. Han et al., <i>Novel Enhanced Stressor With Graded Embedded SiGe Source/Drain for High Performance CMOS Devices</i> , Technical Digest of the 2006 IEEE International Electron Devices Meeting (IEDM), pp. 437-440 (2006).
1022	U.S. Patent Appl. Pub. No. 2007/0122953 A1 to Liu et al.
1023	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice, and Modeling</i> (1st ed. 2000) (excerpted).
1024	S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (excerpted).
1025	U.S. Patent No. 6,949,482 to Murthy et al.
1026	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> (1st ed. 2000) (excerpted).
1027	U.S. Patent No. 8,358,012 to Haran et al.
1028	U.S. Patent Appl. Pub. No. 2008/0067545 A1 to Rhee et al.
1029	E. Bucher et al., <i>Work Function and Barrier Heights of Transition Metal Silicides</i> , Applied Physics A, no. 40, pp. 71-77 (1986).

Exhibit	Description of Exhibit
1030	E.D. Marshall et al., <i>Metal-Germanium Contacts and Germanide Formation</i> , Materials Research Society Symposia Proceedings, vol. 47: Symposium C – Thin Films: The Relationship of Structure to Properties, pp. 161-166 (1985).
1031	R. Braunstein et al., <i>Intrinsic Optical Absorption in Germanium-Silicon Alloys</i> , Physical Review, vol. 109, no. 3, pp. 695-710 (1958).
1032	J. Weber & M.I. Alonso, <i>Near-Band-Gap Photoluminescence of Si-Ge Alloys</i> , Physical Review B, vol. 40, no. 8, pp. 5683-5693 (1989).
1033	V.E. Houtsma, <i>Gate Oxide Reliability of Poly-Si and Poly-SiGe CMOS Devices</i> , Doctoral Dissertation, University of Twente (1999) (excerpted).
1034	U.S. Patent No. 5,644,166 to Honeycutt et al.
1035	<i>FinFETs and Other Multi-Gate Transistors</i> (J.-P. Colinge ed., 2008) (excerpted).
1036	U.S. Patent No. 8,652,894 to Lin et al.
1037	S. Thompson et al., <i>A Logic Nanotechnology Featuring Strained-Silicon</i> , IEEE Electron Device Letters, vol. 25, no. 4, pp. 191-93 (Apr. 2004).
1038	J. Kavalieros et al., <i>Tri-Gate Transistor Architecture With High-k Gate Dielectric Metal Gates and Strain Engineering</i> , 2006 IEEE Symposium on VLSI Technology Digest of Technical Papers, pp. 1-2 (June 2006).
1039	Prosecution File History, U.S. Patent No. 11,251,281 (“File History”).
1040	Amendment to European Patent Application No. 11851579.0 (June 23, 2015).
1041	S. Gannavaram et al., <i>Low Temperature ($\leq 800^{\circ}\text{C}$) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for Sub-70 nm CMOS</i> , Technical Digest of the 2000 International Electron Devices Meeting (IEDM), pp. 437-40 (2000).

Exhibit	Description of Exhibit
1042	U.S. Patent No. 9,245,805 to Yeh et al.
1043	English Translation of Korean Patent Application Serial No. 10-20080115801 to Kim et al. (“Korean <i>Kim</i> ”).
1044	P. Ranade et al., <i>A Novel Elevated Source/Drain PMOSFET Formed by Ge-B/Si Intermixing</i> , IEEE Electron Device Letters, vol. 23, no. 4, pp. 218-20 (Apr. 2002).
1045	U.S. Patent Appl. Pub. No. 2008/0054347 A1 to Wang.
1046	U.S. Patent Appl. Pub. No. 2007/0235802 A1 to Chong et al.
1047	S. Natarajan et al., <i>A 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors, Enhanced Channel Strain and 0.171μm² SRAM Cell Size in a 291Mb Array</i> , Technical Digest of the 2008 IEEE International Electron Devices Meeting (IEDM), pp. 1-3 (2008).
1048	K. Mistry et al., <i>A 45nm Logic Technology with High-k + Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging</i> , Technical Digest of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (2007).
1049	K.-M. Tan et al., <i>Strained p-Channel FinFETs With Extended Π-Shaped Silicon–Germanium Source and Drain Stressors</i> , IEEE Electron Device Letters, vol. 28, no. 10, pp. 905-08 (Oct. 2007).
1050	S. Zaima & Y. Yasuda, <i>Study of Reaction and Electrical Properties at Ti/SiGe/Si(100) Contacts for Ultralarge Scale Integrated Applications</i> , Journal of Vacuum Science & Technology B, vol. 16, pp. 2623-28 (1998).
1051	S. Gaudet et al., <i>Thin Film Reaction of Transition Metals with Germanium</i> , Journal of Vacuum Science & Technology A, vol. 24, no. 3, pp. 474-486 (2006).

Exhibit	Description of Exhibit
1052	Memorandum from Katherine K. Vidal to the Members of the Patent Trial and Appeal Board on Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (June 21, 2022).
1053	C.C. Wang et al., <i>Boron Diffusion in Strained and Strain-Relaxed SiGe</i> , Materials Science and Engineering B, vols. 124-125, pp. 39-44 (2005).
1054	H. Okamoto et al., <i>A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-Node High-Performance pMOSFET Technology</i> , Proceedings of the 2008 38th European Solid-State Device Research Conference (ESSDERC), pp. 326-29 (Sept. 2008).
1055	H. Xiao, <i>Introduction to Semiconductor Manufacturing Technology</i> (2001) (excerpted).
1056	R. Wittman, <i>Miniaturization Problems in CMOS Technology: Investigation of Doping Profiles and Reliability</i> , Doctoral Dissertation, Wien University Austria (Jan. 2007) (excerpted).
1057	P. Bai et al., <i>A 65nm Logic Technology Featuring 35 nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell</i> , Technical Digest of the 2004 International Electron Devices Meeting (IEDM), pp. 657-660 (2004).
1058	S. Thompson, et al., <i>A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 μm^2 SRAM Cell</i> , Technical Digest of the 2002 International Electron Devices Meeting (IEDM), pp. 61-64 (2002).
1059	S.E. Thompson & S. Parthasarathy, <i>Moore's Law: The Future of Si Microelectronics</i> , Materials Today, vol. 9, no. 6, pp. 20-25 (June 2006).
1060	Y. Sun et al., <i>Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors</i> , Journal of Applied Physics, vol. 101, 104503, pp. 1-22 (2007).

Exhibit	Description of Exhibit
1061	U.S. Patent No. 8,362,575 to Kwok et al.
1062	U.S. Patent Appl. Pub. No. 2007/0123042 A1 to Rim et al.

CLAIM LISTING

Element	Claim Language
[1.0]	An integrated circuit structure, comprising:
[1.1]	a fin comprising silicon;
[1.2]	a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;
[1.3]	a first dielectric spacer along the first side of the gate electrode;
[1.4]	a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer,
[1.5]	wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[1.6]	a second dielectric spacer along the second side of the gate electrode;
[1.7]	a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer,
[1.8]	wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

Element	Claim Language
[1.9]	a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;
[1.10]	a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[1.11]	a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;
[1.12]	a first contact plug in the first opening and on the first germanide layer; and
[1.13]	a second contact plug in the second opening and on the second germanide layer.
5	The integrated circuit structure of claim 1, further comprising: an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region.
6	The integrated circuit structure of claim 1, further comprising: a gate dielectric layer, wherein the gate electrode is on the gate dielectric layer, wherein the gate dielectric layer comprises a high-k dielectric material, and wherein the gate electrode comprises a metal layer.

Element	Claim Language
7	The integrated circuit structure of claim 1, wherein the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets.
[8.0]	An integrated circuit structure, comprising:
[8.1]	a body comprising silicon;
[8.2]	a gate electrode over the body, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;
[8.3]	a first dielectric spacer along the first side of the gate electrode;
[8.4]	a first source or drain region in the body proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer,
[8.5]	wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[8.6]	a second dielectric spacer along the second side of the gate electrode;
[8.7]	a second source or drain region in the body proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer,
[8.8]	wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

Element	Claim Language
[8.9]	a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;
[8.10]	a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[8.11]	a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;
[8.12]	a first contact plug in the first opening and on the first germanide layer; and
[8.13]	a second contact plug in the second opening and on the second germanide layer.
[12.0]	A computing device, comprising:
[12.1]	a board; and
[12.2]	a component coupled to the board, the component including an integrated circuit structure, comprising:
[12.3]	a fin comprising silicon;
[12.4]	a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;
[12.5]	a first dielectric spacer along the first side of the gate electrode;

Element	Claim Language
[12.6]	a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer,
[12.7]	wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[12.8]	a second dielectric spacer along the second side of the gate electrode;
[12.9]	a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer,
[12.10]	wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[12.11]	a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;
[12.12]	a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[12.13]	a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;
[12.14]	a first contact plug in the first opening and on the first germanide layer; and

Element	Claim Language
[12.15]	a second contact plug in the second opening and on the second germanide layer.
13	The computing device of claim 12, further comprising: a memory coupled to the board.
14	The computing device of claim 12, further comprising: a communication chip coupled to the board.
15	The computing device of claim 12, further comprising: a camera coupled to the board.
16	The computing device of claim 12, further comprising: a battery coupled to the board.
17	The computing device of claim 12, further comprising: an antenna coupled to the board.
18	The computing device of claim 12, wherein the component is a packaged integrated circuit die.
19	The computing device of claim 12, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.
20	The computing device of claim 12, wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box.

I. INTRODUCTION

Titled “Contact Resistance Reduction Employing Germanium Overlayer Pre-Contact Metalization,” the ’281 Patent¹ describes field-effect transistors (“FETs”) with a germanium layer over their source/drain regions to lower contact resistance—an approach others had taught. This Petition, supported by Dr. Scott Thompson’s declaration, requests *inter partes* review of challenged claims 1, 5-8, and 12-20 and demonstrates their unpatentability.

II. RELIEF REQUESTED

Petitioner requests *inter partes* review on the following grounds:

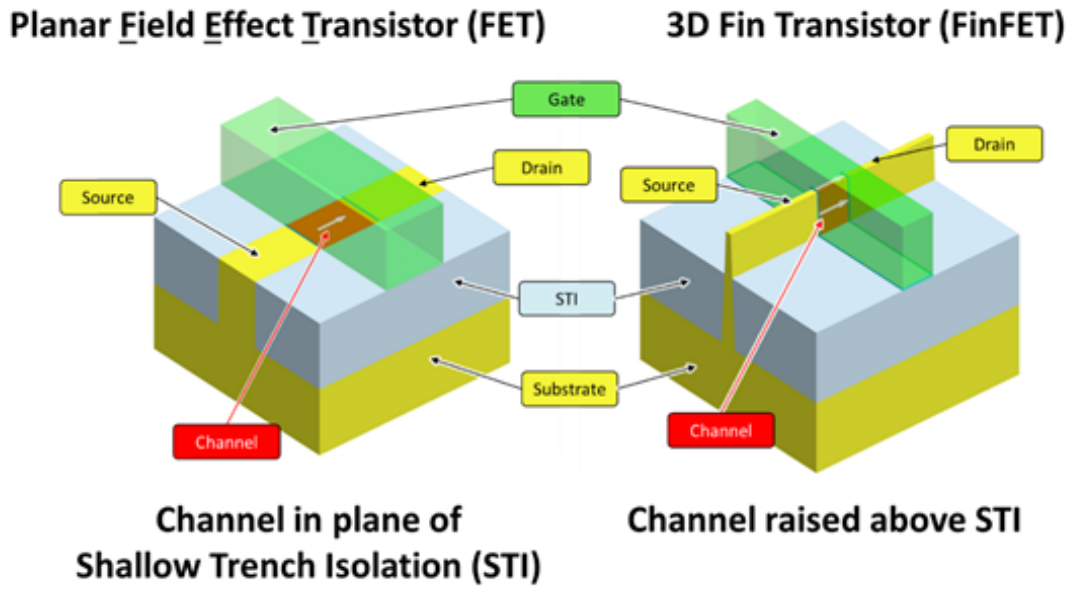
Ground	References	Basis	Claims
1A	<i>Ranade, Kim</i>	§103	1, 5-8, 12-20
1B	<i>Ranade, Kim, Liu</i>	§103	12-20
2A	<i>Tung, Brask, Yu</i>	§103	1, 5-8, 12-20
2B	<i>Tung, Brask, Yu, Liu</i>	§103	12-20

III. STATE OF THE ART

A. Planar and Non-Planar FETs

A FET is a switch operated by voltage applied to a “gate” between “source” and “drain” regions. Thompson ¶51. When turned on, current flows between the source/drain regions through a “channel” under the gate. *Id.* The figures below illustrate two types of FETs: a planar FET and a non-planar “FinFET.” *Id.* ¶50.

¹ U.S. Patent No. 11,251,281 (EX1001).

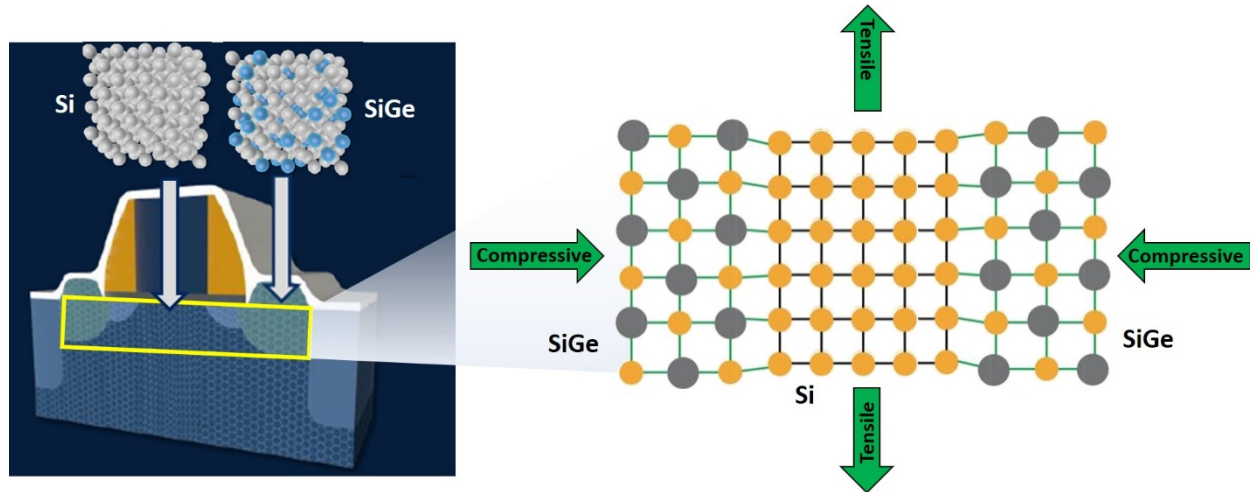


The operation of both is the same, as is the underlying physics. *Id.* ¶51. And except for forming the fin shape in the latter, their fabrication is the same. *Id.* ¶52; *see also* EX1009 at 1; EX1010 at Abstract, 2:11-14, 5:37-40; EX1011 at 1.

B. SiGe/Strained Silicon Technology

Integrated circuits include p-type FETs (“pFETs”), where positive charges generate a “1” logic, and n-type FETs (“nFETs”), where negative charges generate a “0” logic. Thompson ¶¶55-56. PFETs were once much slower than nFETs. *Id.* ¶¶54-58. What Dr. Thompson calls SiGe/Strained Si technology changed this. *See id.* Because Ge atoms are larger than Si atoms, using silicon-germanium (“Si_xGe_{1-x}” or “SiGe”) source/drain regions strains the Si channel region (illustrated below), which improves pFET charge carrier mobility and thus

operating speed. *Id.* ¶¶57-60; *see also* EX1012 at 9; EX1013 ¶0007. By 2004, SiGe source/drain regions had doubled pFET speeds. Thompson ¶¶56-58.



SiGe/Strained Si technology was well-known by December 2010. *See* '281 Patent at 4:67-5:7. Four generations of high-volume commercial devices already used it. Thompson ¶¶64-65. And because smaller transistors experience less strain at a given Ge concentration, Ge concentration increased as transistors shrank. *Id.* ¶61. The industry knew further scaling required even “higher germanium concentrations in the S/D area.” EX1014 at 5; *see also* EX1015 at 7.

To continue this trend and add strain while increasing Ge concentration, a person of ordinary skill in the art (“POSITA”) would have appreciated the need to minimize dislocations in the SiGe source/drain regions. Thompson ¶62; *see also* Ranade ¶0040; EX1016 at 3:30-44, 3:60-64, 4:2-8, 4:28-60; EX1013 ¶¶0030-0032; EX1017 at 2:10-22. And a POSITA would have known to achieve this by grading the Ge concentration. Thompson ¶¶62-63; *see also* EX1018 at 1:56-64; EX1019 at

Title, Abstract, ¶¶0001, ¶0044, ¶¶0053-0058, Figs. 14, 15; EX1013 ¶¶0008, ¶0032, ¶0042; EX1020 ¶¶0083-0095; *Ranade* ¶0040; EX1021 at 2-3, Figs. 1-4, 6, 7; EX1016 at Abstract, 4:38-5:19, 7:61-8:31; EX1017 at 2:10-22, 5:56-6:6, 6:38-7:11, Fig. 5b; EX1022 ¶¶0059-0060.

C. Schottky Barrier Engineering

An electrode contacts source/drain regions to pass electricity. Thompson ¶68. The electrical resistance at the interface between the electrode and underlying semiconductor is called contact resistance. *Id.* A POSITA would have sought lower contact resistance to avoid slower switching speeds and increased power consumption and heating. *Id.* ¶66.

The equation governing contact resistance dictates that lowering the so-called the “Schottky” energy barrier reduces contact resistance—something the ’281 Patent itself acknowledges. *Id.* ¶¶68-73; *see also* ’281 Patent at 4:10-16, 12:17-22, 14:41-57; EX1023 at 10-12; EX1024 at 7. A POSITA would have known this. *See* EX1025 at 8:34-9:63, Figs. 5-8; EX1020 ¶¶0039-0045, ¶0086; EX1012 at 3-4, 6-7.

Since the 1980s, long before SiGe/Strained Si technology, the industry used metal-silicon compounds called “silicides” to lower the Schottky barrier height for silicon source/drain regions. Thompson ¶¶87-90. Silicides are formed by metalizing a Si layer—depositing a metal layer (e.g., Ti, Co, Ni) on a layer of Si

and applying enough heat for the Si and metal atoms to bond. *Id.* ¶89. The textbook figure below shows a “Titanium silicide contact.” *Id.* ¶¶88-89; *see also* EX1026 at 20-21, 41-45, Figs. 9.19-9.22, 12.9, 12.14.

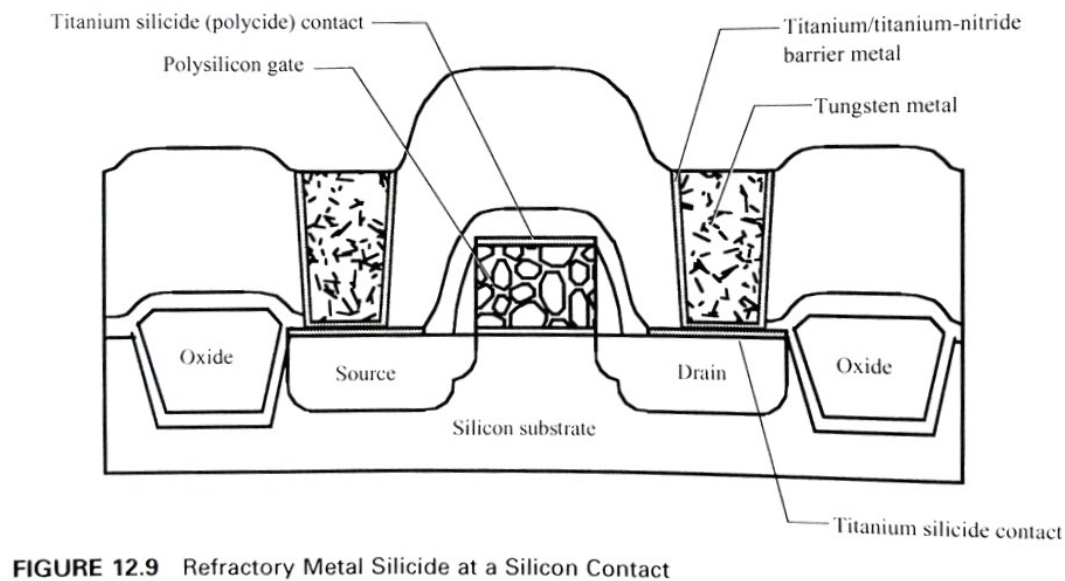
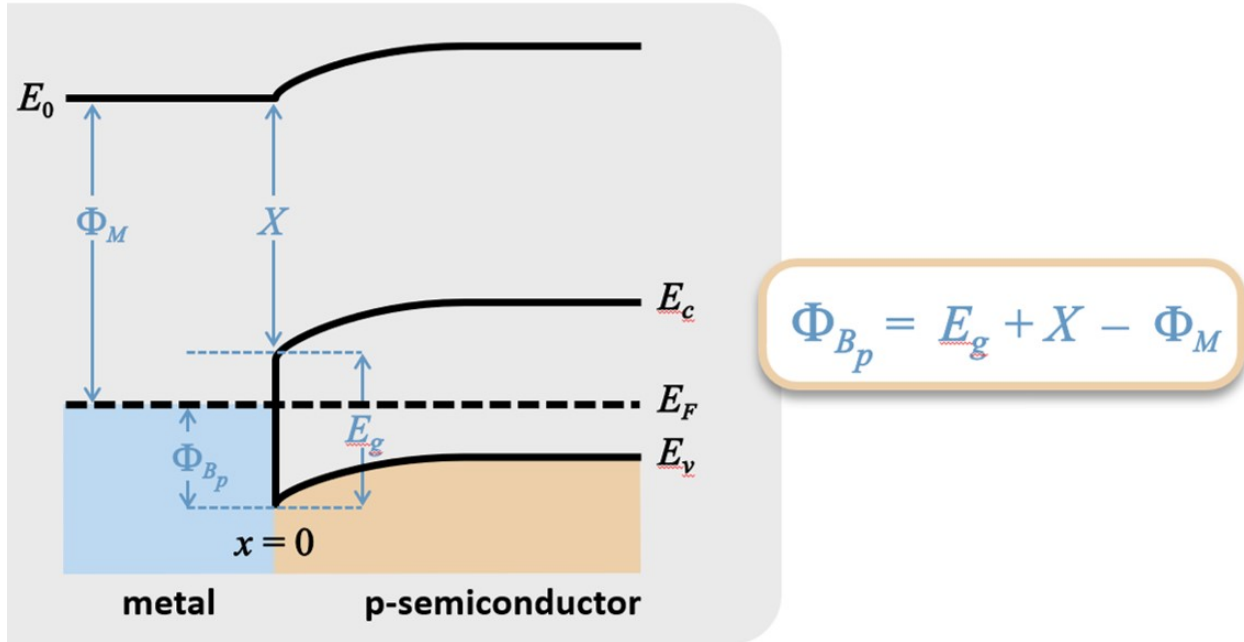


FIGURE 12.9 Refractory Metal Silicide at a Silicon Contact

EX1026, Fig. 12.9

This technique remained pervasive as the industry shifted to SiGe source/drain regions. Thompson ¶90; *see also* EX1025 at Abstract, 2:66-3:13, 8:34-9:63; EX1027 at 1:10-14; *Kim* ¶0007, ¶¶0050-0051, ¶0074; EX1028 ¶0021, ¶¶0024-0025, ¶0042; *Tung* ¶0005, ¶¶0029-0031, ¶0034, ¶0061, ¶0078; EX1020 ¶¶0023-0025, ¶¶0039-0045, ¶0050, ¶0066, ¶0086; EX1022 ¶0086, ¶0096; EX1012 at 6.



As the energy diagram above illustrates, the Schottky barrier height (Φ_{Bp}) for a pFET source/drain region depends on the bandgap (E_g) and electron affinity (χ) of the source/drain semiconductor, and the work function (Φ_M) of the metal. Thompson ¶¶69-72. A POSITA would have understood the electron affinity (χ) of SiGe and the work function (Φ_M) of a metal-SiGe compound remain nearly unchanged no matter the Ge concentration. Thompson ¶74; *see also* EX1024 at 11; EX1029 at Tbl. 1; EX1030 at Fig. 1. On the other hand, a POSITA would have known the SiGe bandgap (E_g) varies with Ge concentration as shown below. Thompson ¶¶74-76; *see also* EX1031 at Fig. 17; EX1032 at 7, Fig. 9; EX1012 at 4, 6-7, Fig. 12; EX1033 at 15-16, Fig. 1.5.

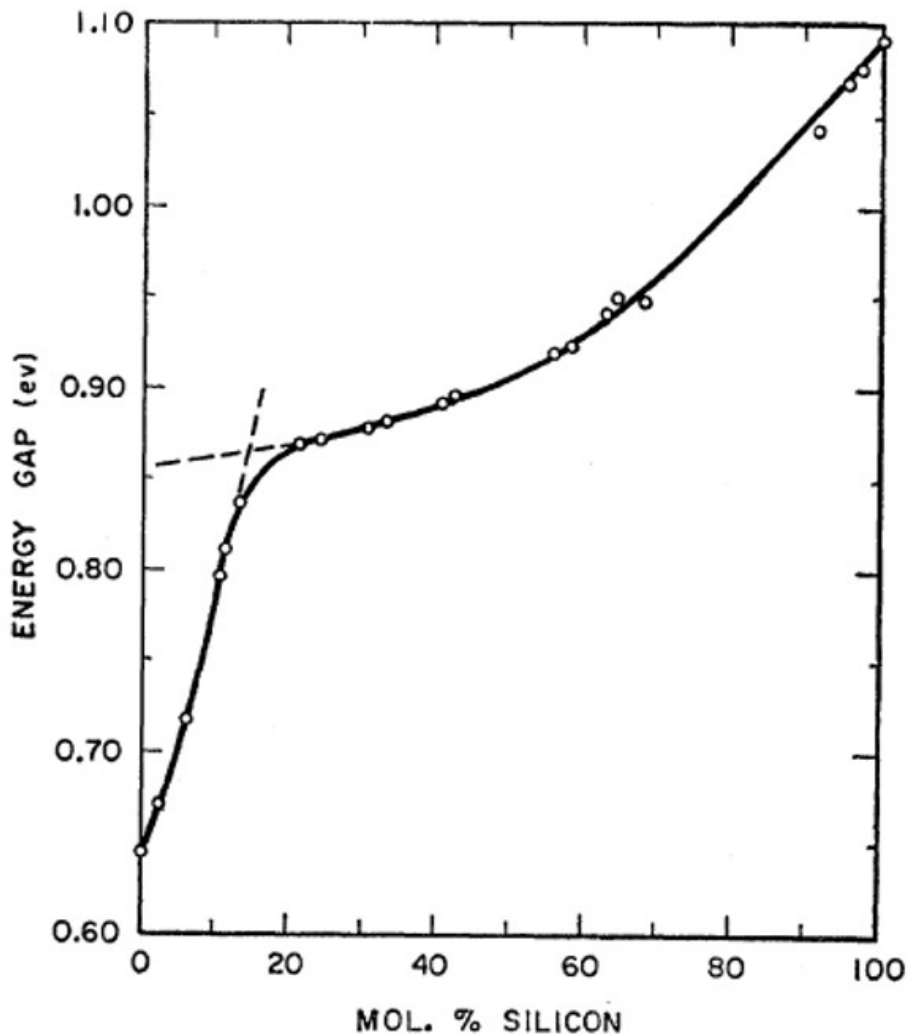


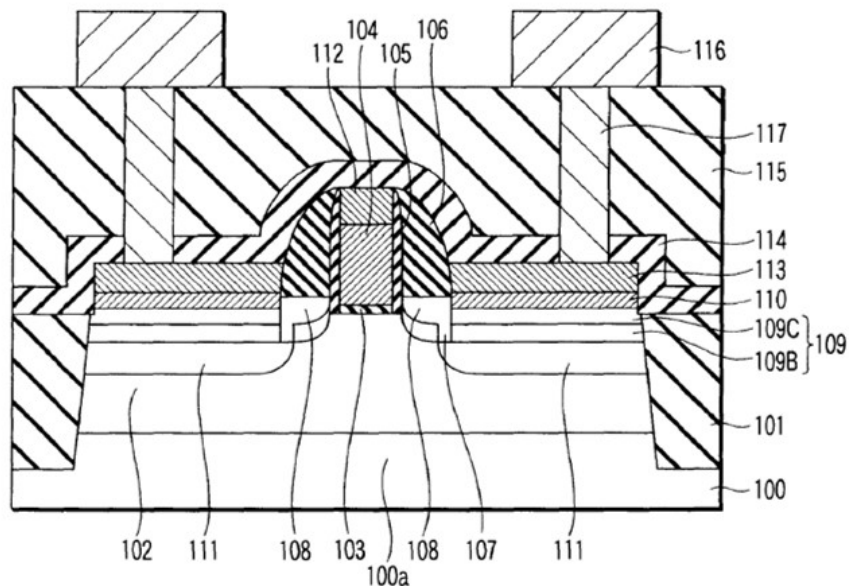
FIG. 17. Composition dependence of energy gap in Ge-Si alloys at 296°K, based on one-phonon Macfarlane-Roberts expression; see Eq. (1) in text.

EX1031, Fig. 17

The SiGe bandgap notably drops around 15 at. % Si (i.e., 85 at. % Ge),² where a “crossover from ... Si-like” behavior to “Ge-like” behavior occurs. EX1032 at 7. A POSITA thus would have expected using a Ge overlayer (e.g., more than about 85% Ge) on the source/drain regions to further reduce Schottky

² All percentages in this Petition are atomic percentages.

barrier height and lower contact resistance significantly. Thompson ¶¶67, ¶¶76-80; *see also* EX1020 ¶¶0042-0045, ¶0086; Kim ¶¶0072-0074; Tung ¶¶0058-0061, ¶¶0078-0081; EX1034 at 1:8-15, 4:46-53, 7:20-43.



This approach was known. One example, shown above, teaches p-type SiGe source/drain regions 109 and a Ge overlayer 110. EX1020 ¶0086, ¶0090, ¶¶0094-0095, Fig. 16. SiGe layer 109C is graded such that the Ge concentration at its lower interface with SiGe layer 109B “is approximately 10 to 30 at %” and the Ge concentration at its upper interface with Ge capping layer 110 “is approximately 100 at %.” *Id.* ¶0085. Ge overlayer 110 reacts with a metal to form germanide layer 113 and create a low-resistance contact. *Id.* ¶0024.

This structure was derived by applying the basic Schottky barrier engineering principles noted above. *Id.* ¶¶0042-0045. Predictably, “as compared with the conventional technology where the silicide film is formed on the silicon

layer or the silicon germanium layer, the contact resistance in the source/drain layer can be reduced in this embodiment where the germanide layer is formed on the germanium layer.” *Id.* ¶¶0045; *see also* EX1022 ¶¶0060, ¶¶0086. Dr. Thompson explains that using such a Ge overlayer is a “proposal I would have expected my graduate students to provide if I asked on an exam how to reduce the source/drain contact resistance of a SiGe pFET.” Thompson ¶76.

D. Characteristics of Epitaxial SiGe Source/Drain Regions

As shown below, epitaxially grown SiGe source/drain regions have either a diamond shape or a rectangular shape, depending on wafer orientation. Thompson ¶94; *see also* EX1035 at 50, Fig. 2.37; *Tung* ¶¶0058; EX1036 at 5:29-43, 10:6-24, Fig. 5A.

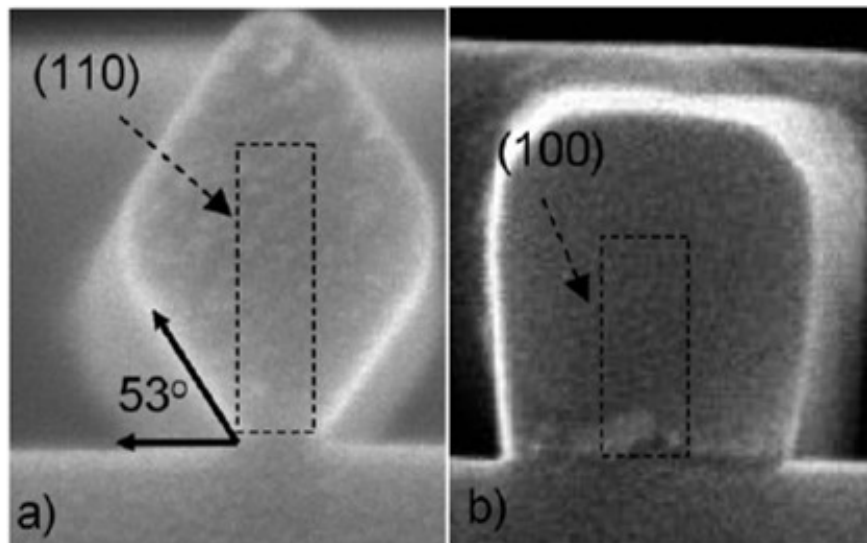


Fig. 2.37. Cross sectional SEM images on fins after epitaxial growth. a) (110) side wall surface result in diamond-shaped fin; b) (100) sidewall surface result in square-shaped fin.

EX1035, Fig. 2.37

A POSITA also would have understood that, to be commercially viable, strain engineering requires FET channels aligned with the $\langle 110 \rangle$ axis on “industry-standard Si wafers with (001) surface and wafer notch on the $[110]$ axis.” EX1037 at 2; *see also* Thompson ¶¶95; EX1038 at 1, Fig. 4b. For such an orientation, a POSITA would have understood SiGe naturally grows in a diamond shape (see below). Thompson ¶¶95-96; *see also* EX1038 at Fig. 7b; EX1035 at 50, Fig. 2.37; EX1036 at 5:29-43, 10:6-24, Fig. 5A.

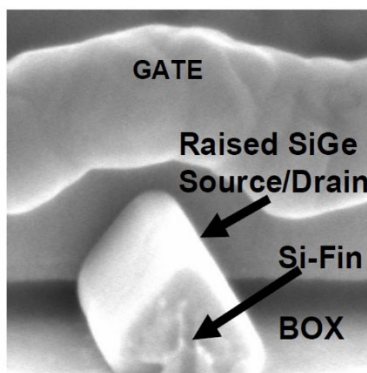
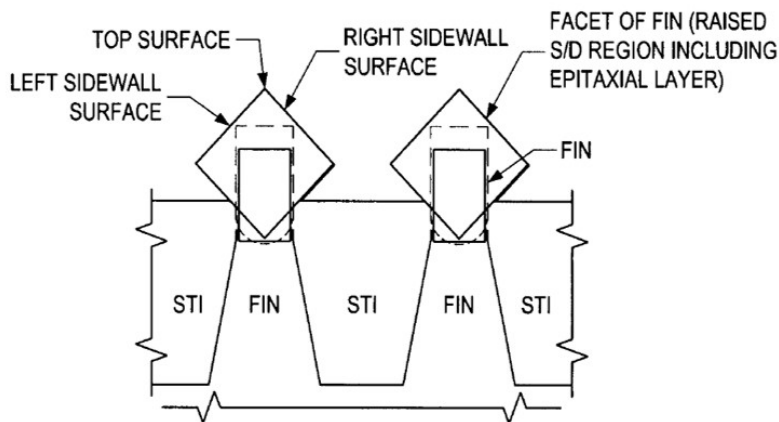


Fig. 7b Y-dir. cross-section of PMOS Trigate with SiGe raised source/drain

EX1038, Fig. 7b



EX1036, Fig. 5A

Thus, a POSITA would have understood epitaxial SiGe source/drain regions grown using the industry-standard wafer and channel orientation, which is necessary for effective strain engineering, naturally grow in a diamond shape. Thompson ¶¶97.

IV. THE '281 PATENT

The '281 Patent centers on a Ge capping layer that reduces Schottky barrier height: “[A]n intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance.” '281 Patent at 2:27-34; *see also id.* at 3:51-57 (characterizing this as “a bilayer construction” comprising “SiGe (for the source/drain regions) capped with an overlayer of a boron doped germanium layer”).

The '281 Patent tries to distinguish itself from prior art based on this Ge capping layer. *See id.* at 2:43-56, 14:15-27, Fig. 7. The patent purports to “marry superior contact properties of germanium with superior semiconductor transistor properties of Si and SiGe to provide next generation low resistance contacts.” *Id.* at 3:6-9. Specifically, “an overlayer or cap of boron doped germanium can be formed directly over the source/drain regions,” and a “contact metal (or series of metals) can then be deposited and a subsequent reaction (annealing) can be carried out to form metal germanide source and drain contacts.” *Id.* at 3:24-30. The specification attributes alleged improvements to the well-known principles described in Section III.C. *Compare id.* at 4:10-16, 10:53-11:3, 12:17-22, 14:41-57, with Section III.C; EX1020 ¶¶0039-0045, ¶¶0085-0086; Thompson ¶¶66-80.

The embodiment below shows a transistor in which SiGe source/drain regions 318/320 are formed “using any number of conventional techniques,” such

as “epitaxially depositing a silicon or silicon germanium material (e.g., with a germanium concentration in the range of, for instance, 10 to 70 atomic %).” ’281 Patent at 4:27-34; *see also id.* at 7:55-9:26, Figs. 3A-3B. Boron-doped “germanium layers” 317/319 are then deposited on source/drain regions 318/320. *Id.* at 9:41-45, Fig. 3C. These “germanium layers” contain at least 90% Ge. *Id.* at 9:45-55; *see also id.* at 3:17-27, 7:11-20, 10:53-11:3, 12:31-41, 16:26-29, 16:52-57, 17:4-7, 17:29-33, 17:46-52, 18:16-18. After depositing a “metal and annealing to form silicide/germanide” layers 325/327, contact plugs 329/331 are formed. *See id.* at 11:66-12:17, Figs. 3H, 3I. “The boron doped germanium layer 317/319 allows for metal-germanide formation,” which “significantly lower[s] Schottky-barrier height and improve[s] contact resistance (including R_{ext}) over that in conventional metal-silicide systems.” *Id.* at 12:17-22.

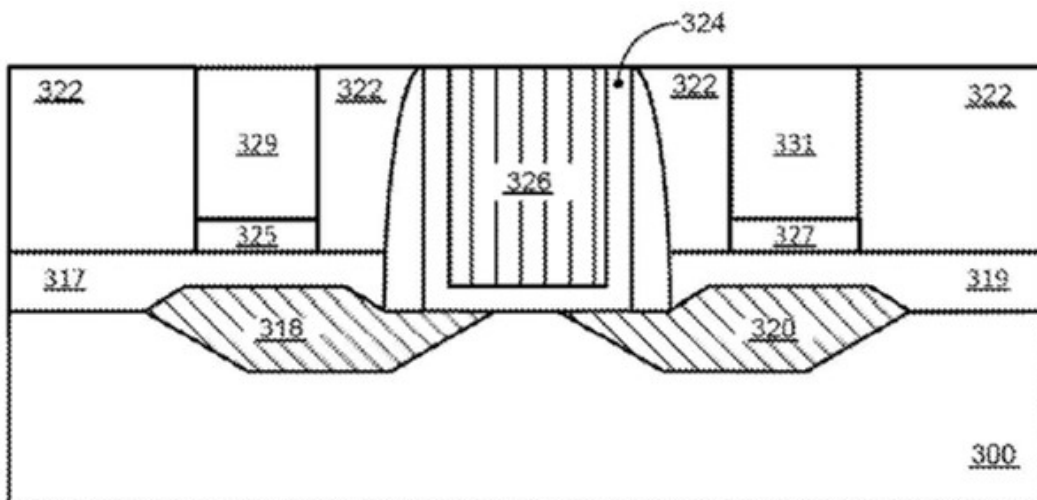


FIG. 3I

Prosecution of the '281 Patent was uneventful. *See* Thompson ¶113. The Examiner issued the claims without any substantive rejections. *See generally* File History.

V. LEVEL OF ORDINARY SKILL

A POSITA would have had at least a Master's degree in electrical engineering, physics, materials science, or a related field and at least two years of work experience in integrated circuit device design or manufacturing, although additional education could substitute for professional experience and significant work experience could substitute for formal education. Thompson ¶46.

VI. CLAIM CONSTRUCTION

The Board construes claims under the standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). A POSITA would have understood “germanide layer” refers to a “germanium layer metalized with one or more metals.” Thompson ¶¶123-129.

According to the '281 Patent, a nominal “germanium” layer has at least 90% Ge. *See* '281 Patent at 3:19-27, 9:44-52. The '281 Patent describes a “germanide layer” as such a germanium layer once it is metalized (made metallic by annealing the Ge layer with a metal to induce a chemical reaction between them). *Id.* at Title, 3:27-30, 12:11-22, 14:41-48. And it distinguishes “germanides” from “industry standard silicides” based on the presence of this Ge layer. *Id.* at

22:43-64, 14:15-18, Fig. 7; *see also* EX1025 at 2:66-3:9 (same inventors referring to a “nickel silicon germanium *silicide*” formed by directly metalizing SiGe source/drain regions); EX1020 ¶0045 (comparing “the conventional technology where the silicide film is formed on the silicon layer or the silicon germanium layer” with a “germanide layer ... formed on the germanium layer”). Moreover, the title, abstract, and every description characterizes the invention as providing a Ge layer and metalizing it to form a germanide layer. *See* ’281 Patent at Title, Abstract, 1:41-44, 1:45-48, 1:49-52, 2:27-30, 2:38-64, 3:24-26, 3:33-36, 3:51-57, 3:62-65, 4:3-9, 4:23-27, 4:65-67, 5:8-13, 5:29-33, 5:59-63, 6:20-25, 6:51-57, 6:63-65, 7:11-20, 7:32-36, 9:27-30, 9:33-39, 9:44-55, 9:60-65, 10:4-7, 10:43-49, 10:53-11:6, 11:60-12:2, 12:17-22, 12:31-41, 12:44-58, 13:64-14:3, 14:15-27, 14:41-48, 16:24-31, 16:34-57, 16:62-17:7, 17:29-33, 17:35-52, 17:56-67, 18:16-20, 18:24-27. During prosecution of a related European application, the applicant emphasized: “It is clear that according to the invention” the devices “comprise a heavily doped germanium layer. More specifically, there is a germanium layer that is ‘pure’, that is, close to 100% (ie over 90% according to the specification).” EX1040 at 1-2; *see also Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1374 (Fed. Cir. 2005) (using applicant’s statements to the EPO to construe claim).

Because the ’281 Patent “repeatedly and consistently characterizes” a germanide layer as a germanium layer metalized with one or more metals, “it is

proper to construe [it] in accordance with that characterization.” *WARF v. Apple Inc.*, 905 F.3d 1341, 1351 (Fed. Cir. 2018); *see also In re Abbott Diabetes Care, Inc.*, 696 F.3d 1142, 1150 (Fed. Cir. 2012); *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 790 (Fed. Cir. 2021).

In a related ITC proceeding, Patent Owner argued “germanide layer” means “thickness of material, comprising germanium and a metal.” This position lack merit. Thompson ¶¶130-134. First, a layer without chemical bonding between metal and semiconductor atoms would qualify. Such a layer would undermine the purpose of the invention and raise, not lower, contact resistance. *Id.* ¶131. Second, it encompasses admitted prior art—“industry standard silicides” formed “without the intermediate boron doped germanium layer between the source/drain regions and contact metal.” ’281 Patent at 2:43-56; *see also id.* at 3:6-9, 3:24-30, 10:53-11:3, 14:15-27, 14:41-57, Fig. 7; Thompson ¶132. Third, as noted above, every description of every embodiment hinges on the Ge layer and its metalization to lower Schottky barrier height and reduce contact resistance. Patent Owner’s proposed construction would eliminate this fundamental feature of the ’281 Patent and result in a structure not described. Thompson ¶133.

VII. OVERVIEW OF ASSERTED PRIOR ART

A. *Ranade* (U.S. Patent Application Pub. No. 2008/0121932)

Ranade is prior art under pre-AIA §102(b). It describes planar FETs and non-planar FinFETs. *Ranade* ¶¶0010, ¶¶0025, ¶¶0044. As Figure 2N shows below,³ *Ranade*'s devices include a gate electrode 260 and $\text{Si}_x\text{Ge}_{1-x}$ epitaxial source/drain regions 220 made of “a graded epitaxial layer” to “minimize[] surface defects.” *Id.* ¶¶0040; *see also id.* ¶¶0042. Specifically, “the pair of source/drain regions 220 is a crystalline silicon/germanium region of the stoichiometry $\text{Si}_x\text{Ge}_{1-x}$, where $0 \leq x \leq 1$,” meaning the Ge concentration may vary within a range of 0 to 100%. *Id.* ¶¶0040; *see also* Thompson ¶137.

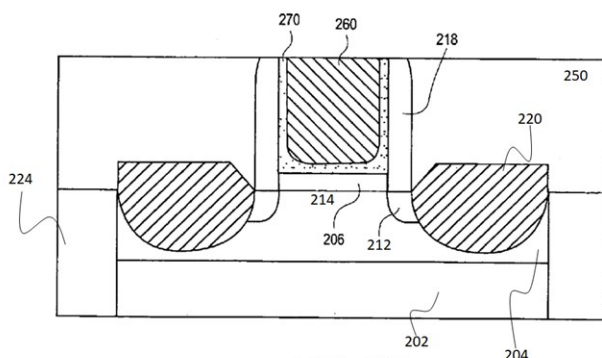


FIG. 2N

B. *Kim* (U.S. Patent Application Pub. No. 2010/0123198)

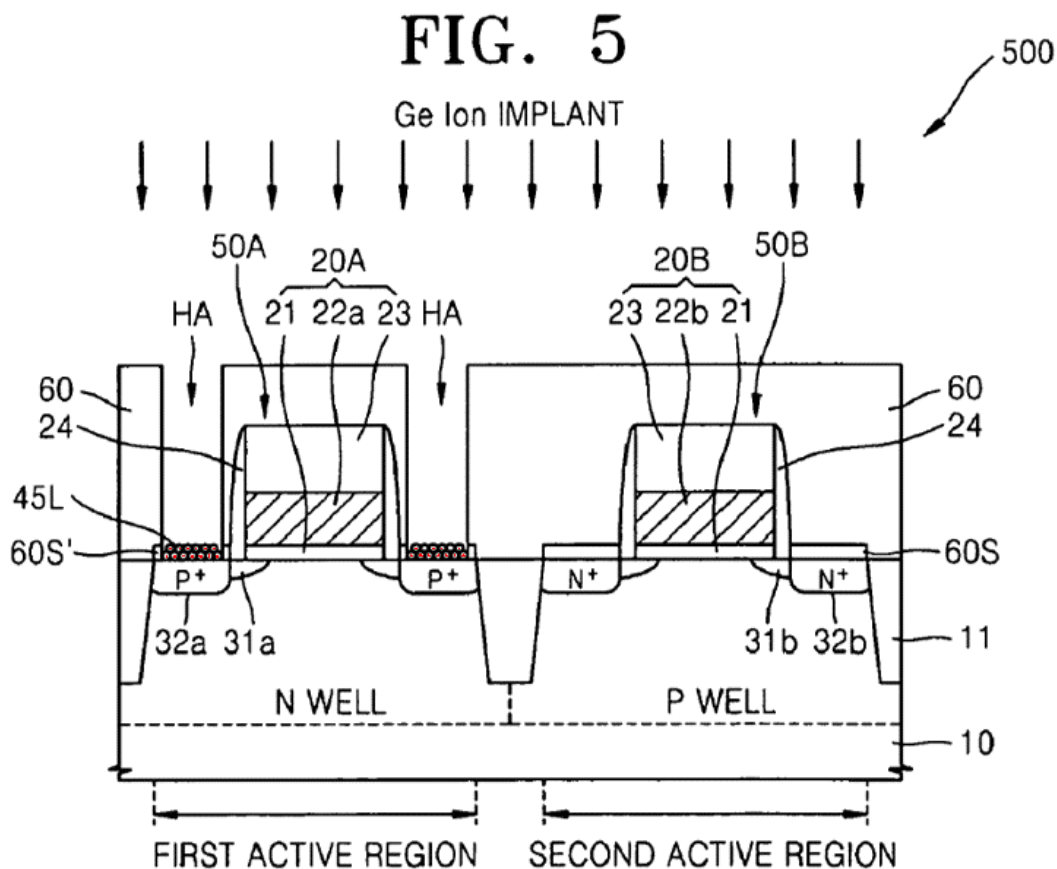
Kim is prior art under pre-AIA §§102(a) and (e). “In order to provide a low resistance contact to a CMOS transistor,” *Kim* explains “the P-channel and N-channel MOSFETs need to be provided with a contact having a low Schottky

³ Annotated with more references for clarity.

barrier.” *Kim* ¶0007; *see also id.* ¶0050. *Kim* describes two processes for forming such contacts: Ge Overlayer Metalization and Direct Metalization. Thompson ¶¶141-145.

1. Ge Overlayer Metalization

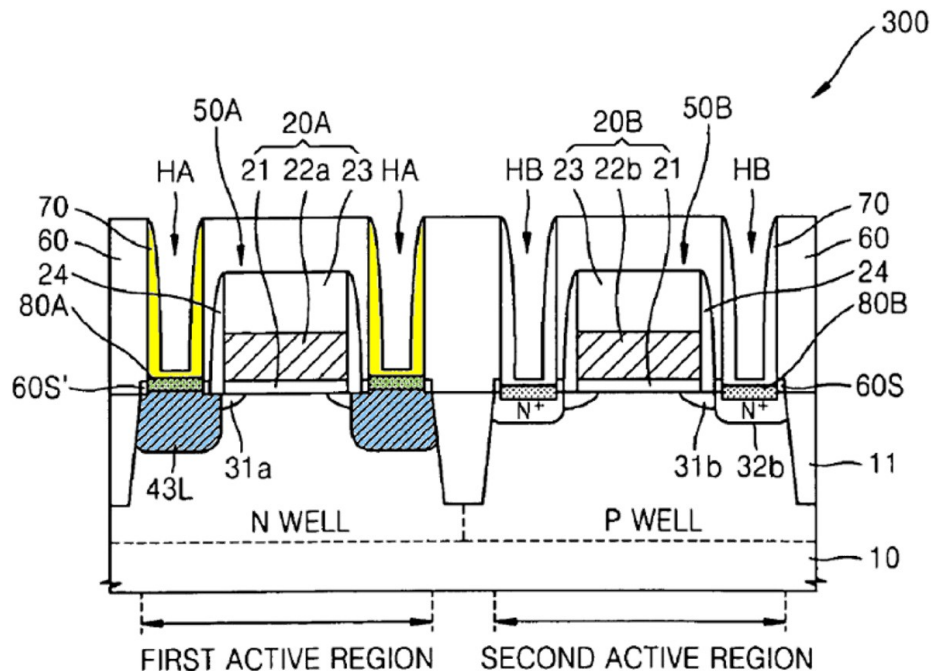
Figure 5 below shows what Dr. Thompson calls *Kim*’s Ge Overlayer Metalization. A thin Ge overlayer 45L (red below) is metalized by reacting it with metal layer 70 (e.g., Ti, not shown). *Kim* ¶¶0070-0073; *see also* Thompson ¶¶142-143. *Kim* explains “a $M(Si_{1-y}Ge_y)$ film” 80A results, where the metal “M” may be titanium. *Kim* ¶0047, ¶0071, ¶0073.



2. Direct Metalization

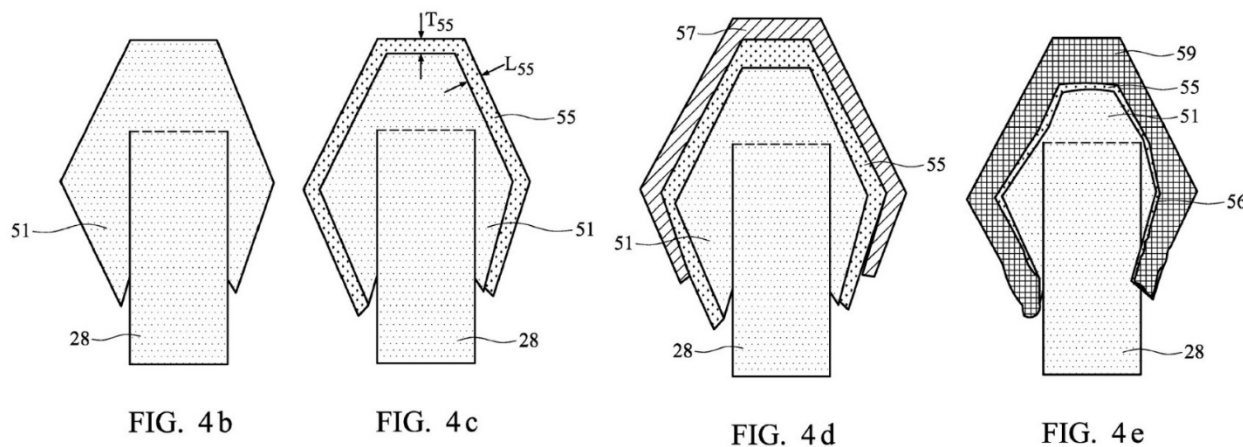
Figure 3F below shows what Dr. Thompson calls *Kim's* Direct Metalization. Instead of metalizing a Ge overlayer as above, exposed SiGe source/drain regions 43L (blue) are metalized by reacting them with metal layer 70 (yellow). *Kim* ¶0050; *see also id.* ¶0046, Fig. 3F. This creates metal-semiconductor film 80A (green)—a “M(Si_{1-y}Ge_y) film containing Ge due to the exposed SiGe epitaxial layer 43L,” where “M” represents the metal of metal layer 70 (e.g., Ti). *Id.* ¶0067; *see also id.* ¶¶0046-0050, ¶0057, ¶¶0063-0067, ¶0071, Fig. 3F; Thompson ¶¶144-145.

FIG. 3F



C. *Tung* (U.S. Patent Application Pub. No. 2010/0276761)

Tung is prior art under pre-AIA §§102(a) and (e). It teaches FinFET “structures and methods of fabrication thereof with low resistance contacts for non-planar semiconductor structures.” *Tung* ¶0006; *see also id.* ¶0005, ¶0034, ¶0061; Thompson ¶¶147-152.

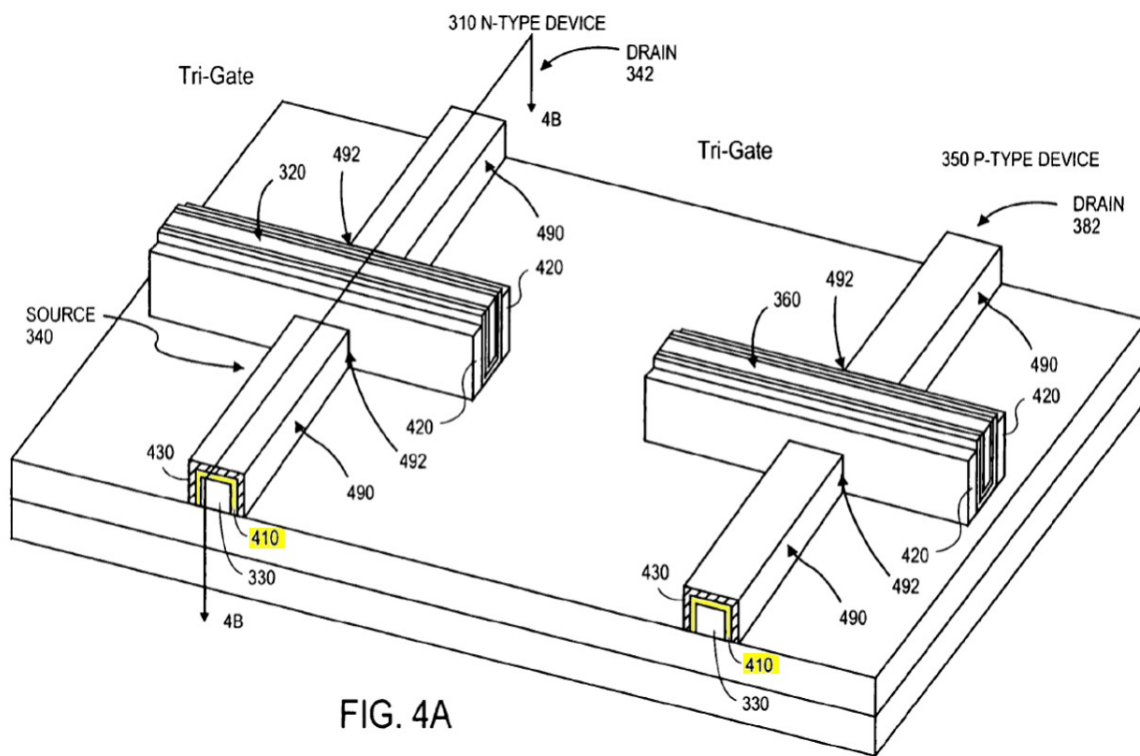


As in Figure 4b, SiGe semiconductor material 51 grows over fin 28 in the source/drain areas. *Tung* ¶0040, ¶0074, ¶0076, Figs. 4b, 13. As in Figure 4c, “another selective epitaxial growth is used to form a doped semiconductor layer 55” in the source/drain areas, which may be “doped SiGe, or doped Ge.” *Id.* ¶0041; *see also id.* ¶0034, ¶0058, ¶0078, Figs. 4c, 14. Then, as in Figure 4d, “metal 57 [e.g., Ti] is deposited” over doped semiconductor layer 55. *Id.* ¶0042; *see also id.* ¶¶0079-0080, Figs. 4d, 15. “[M]etal 57 is annealed to form ... layer 59,” and any unreacted metal 57 “is removed by an etching process.” *Id.* ¶0043; *see also id.* ¶0081, Figs. 4e, 16. During annealing, “metal 57 (FIG. 4d) reacts with the doped

semiconductor layer 55” to form layer 59, as in Figure 4e. *Id.* ¶0043; *see also id.* ¶0045, ¶¶0063-0064, ¶0081.

D. *Brask* (U.S. Patent No. 7,361,958)

Brask is prior art under pre-AIA §102(b). As highlighted below, *Brask* teaches FinFETs with raised source/drain fin regions 410 made by growing $\text{Si}_x\text{Ge}_{1-x}$ ($0 \leq x \leq 0.99$) on fins 330/370. *Brask* at 10:20-49, Figs. 4A, 4B. According to *Brask*, this $\text{Si}_x\text{Ge}_{1-x}$ film 410 may “be graded.” *Id.* at 10:20-29.



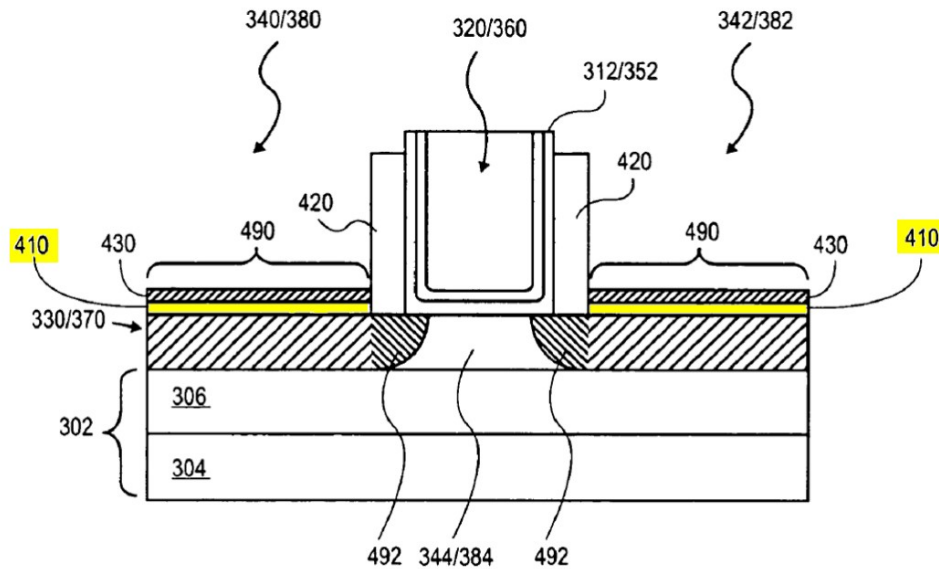


FIG. 4B

E. Yu (U.S. Patent Application Pub. No. 2009/0096002)

Yu is prior art under pre-AIA §102(b). It describes source/drain contacts for a FinFET. As Figures 9A and 9B show below, *Yu*'s contacts include source/drain contact plugs 901 "formed so as to be in contact with at least three surfaces of the fin 201." *Yu* ¶0037. With this approach, "the contact resistance of the device may be reduced," and "variations in the contact resistances due to mis-alignments of the contacts 901" are reduced "since there is more leeway for variation when the width of the contacts 901 are larger than the width of the fin 201." *Id.*

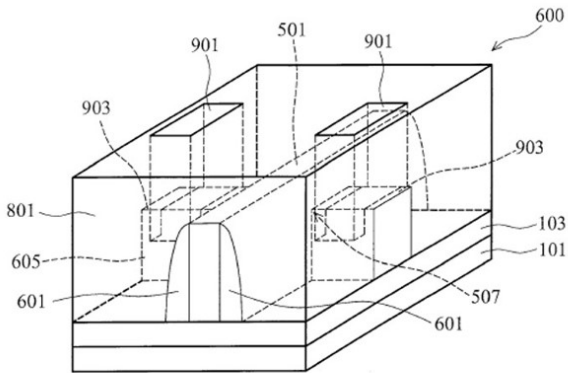


FIG. 9A

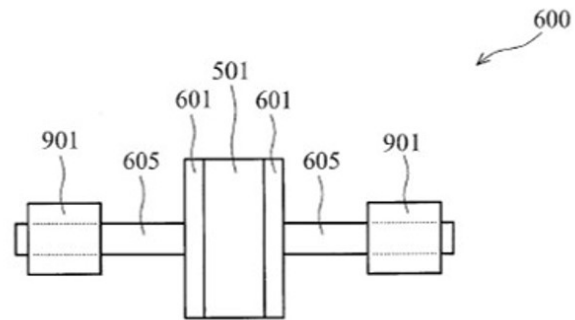


FIG. 9B

F. *Liu* (U.S. Patent No. 7,611,943)

Liu is prior art under pre-AIA §102(b). As Figures 10 and 11 illustrate, *Liu* confirms that FinFETs were used for computing devices, including smartphones. *Liu* at 1:29-32, 1:47-50, 33:10-37:40, Figs. 10, 11.

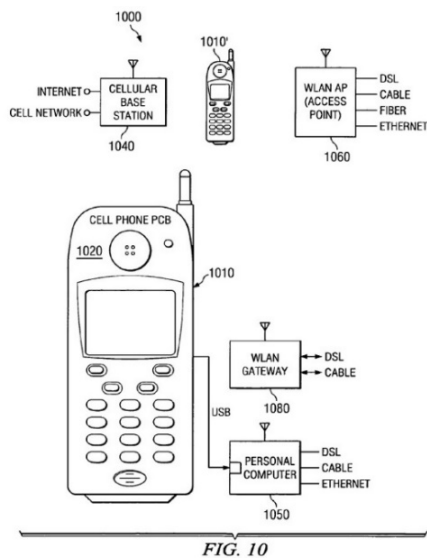


FIG. 10

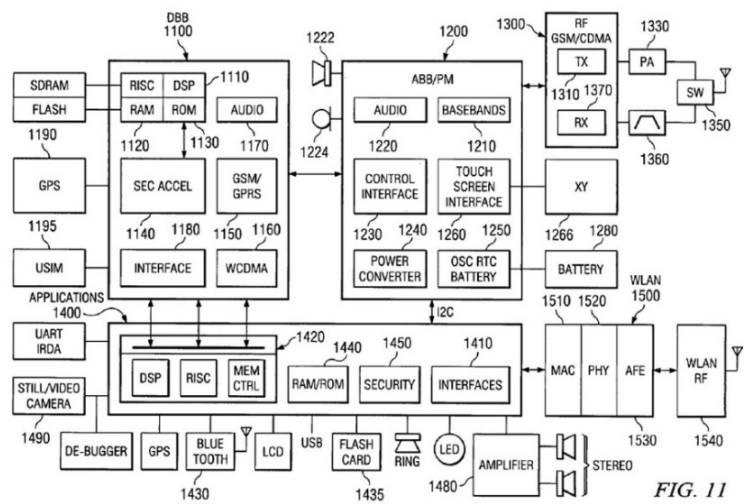


FIG. 11

VIII. THE CHALLENGED CLAIMS ARE UNPATENTABLE

The '281 Patent purports to provide low-resistance contacts to SiGe source/drain regions by adding a Ge overlayer. The principles that suggest using a Ge overlayer, and the Ge overlayer itself, were known. Thompson ¶165.

The '281 Patent's alleged improvements stem from three principles: (1) high Ge concentration in the Ge overlayer to lower Schottky barrier height; (2) high boron concentration in the Ge overlayer to reduce contact resistance, and (3) boron diffusion suppression due to high Ge concentration in the Ge overlayer. Thompson ¶166; *see also* '281 Patent at 2:40-64, 4:10-16, 10:53-11:3, 14:41-57. These are the foundational principles underlying all of SiGe/Strained Si technology. Thompson ¶166; *see also* EX1012 at 5; EX1041 at 1-2, Fig. 3. The '281 Patent claims an obvious and known structure based on these principles. Thompson ¶167.

Not only does the '281 Patent claim a prior-art solution, but it describes a known result. *Id.* ¶168; *compare also* '281 Patent at 2:43-64 (reducing Schottky barrier height from 0.5 eV to 0.2 eV), *with* EX1012 at 9 (“[W]e expect a barrier height change of approximately 0.3 eV.”), *and* EX1020 ¶0045 (“ $\phi_B=0.2$ eV is achieved” by forming a “germanide layer on [a] germanium layer”).

Because these principles, structures, and benefits were known, a POSITA would have found the challenged claims obvious. Thompson ¶169.

A. Ground 1A: The *Ranade-Kim* Combination

1. A POSITA Would Have Found the *Ranade-Kim* Combination Obvious

Kim recognizes the need to reduce source/drain contact resistance, *Kim* ¶¶0006-0007, and instructs the reader to do so by forming a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film over p-type source/drain regions to “reduce the height of Schottky barriers,” *id.* ¶0050. A POSITA would have found it obvious to apply such a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film to *Ranade*’s source/drain regions to reduce contact resistance. Thompson ¶¶170-174.

a. A POSITA would have wanted to apply *Kim*’s contacts to *Ranade*’s FinFET

Ranade describes a FinFET with SiGe source/drain regions but does not provide details about source/drain contacts, including contact materials. Thompson ¶¶176-177. As the literature commonly does, *Ranade* focuses on the transistor itself and simply relies on a POSITA’s general understanding of “typical process steps to complete the formation of a MOS-FET, ... such as a silicidation step.”⁴ *Ranade* ¶0041; *see also* Thompson ¶¶177-178; *Brask* at 27:20-27, Fig. 5Z; EX1042 at 4:43-48; *Tung* ¶0023, ¶0036, ¶0064; EX1018 ¶0043; EX1027 ¶0021.

⁴ “Silicidation” refers to the process of depositing metal on a semiconductor layer and annealing to induce a chemical reaction between the semiconductor atoms and metal atoms. Thompson ¶¶88-90, ¶125.

Like *Ranade*, *Kim* discloses FinFETs with SiGe source/drain regions, but it further describes source/drain contacts that include a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film. Since *Ranade*'s FinFETs require source/drain contacts to operate, a POSITA would have found it obvious to follow *Ranade*'s instructions and apply a "silicidation" process—like the ones *Kim* describes—to contact *Ranade*'s FinFETs. Compare *Ranade* ¶¶0041, with *Kim* ¶¶0050, 0072-0074; see also Thompson ¶179.

Kim teaches two silicidation processes: Ge Overlayer Metalization and Direct Metalization. *Supra* Section VII.B; *Kim* ¶¶0066-0069, 0072-0074. In both, the result is a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film that "reduce[s] sheet resistance." *Kim* ¶0050. A POSITA seeking to implement *Ranade*'s FinFET as instructed would have wanted to apply either technique to reduce contact resistance. Thompson ¶¶181-185.

b. A POSITA would have reasonably expected to succeed

It was well known to form contact plugs and metal-semiconductor compounds like *Kim*'s $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film to contact source/drain regions. Thompson, ¶¶187-188. It was also well-known that metal-semiconductor compounds like *Kim*'s $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film reduce contact resistance in SiGe pFETs. *Id.* ¶¶189-190; see also *Kim* at Abstract, ¶¶0003, ¶¶0010, ¶¶0050, ¶¶0071, ¶¶0074; EX1027 at 1:10-14; *supra* Section III.C.

A POSITA would have understood such metal-semiconductor compounds are formed by depositing a metal onto a semiconductor, then annealing to cause

atoms near the metal-semiconductor interface to react. Thompson ¶¶92, ¶¶125-126; *see also Kim* ¶0050; EX1027 at 1:10-25; EX1020 ¶0024. This technique was routine. Thompson ¶¶188-189; *see also* EX1026 at 20, 41-43, Figs. 9.19-9.22, 12.9. *Kim* also expressly states that its teachings apply to FinFETs. Thompson ¶¶191-193; *see also Kim* ¶0033; Korean *Kim* ¶0023. A POSITA thus would have reasonably expected to succeed when applying *Kim*'s $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ films to *Ranade*'s FinFET. Thompson ¶¶186-190.

A POSITA also would have reasonably expected such combination to reduce contact resistance. A POSITA would have understood, as *Kim* teaches, that *Kim*'s $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ films can be applied to FinFETs with SiGe source/drain regions. *Id.* ¶¶192-193; *see also Kim* ¶0033; Korean *Kim* ¶0023. A POSITA would have understood that remains true regardless of the Ge concentration in those regions. Thompson ¶194; *see also* EX1028 ¶¶0024-0025, ¶0042; EX1020 ¶¶0039-0042; EX1027 at 6:40-46. Because $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ metal-semiconductor films like *Kim*'s were widely known and applied to SiGe source/drain regions with various Ge concentrations and geometries, there was no reason to think they would behave any differently when applied to *Ranade*'s FinFET. Thompson ¶195.

c. A POSITA would have found it obvious to combine *Ranade*'s FinFET with *Kim*'s Source/Drain Contacts

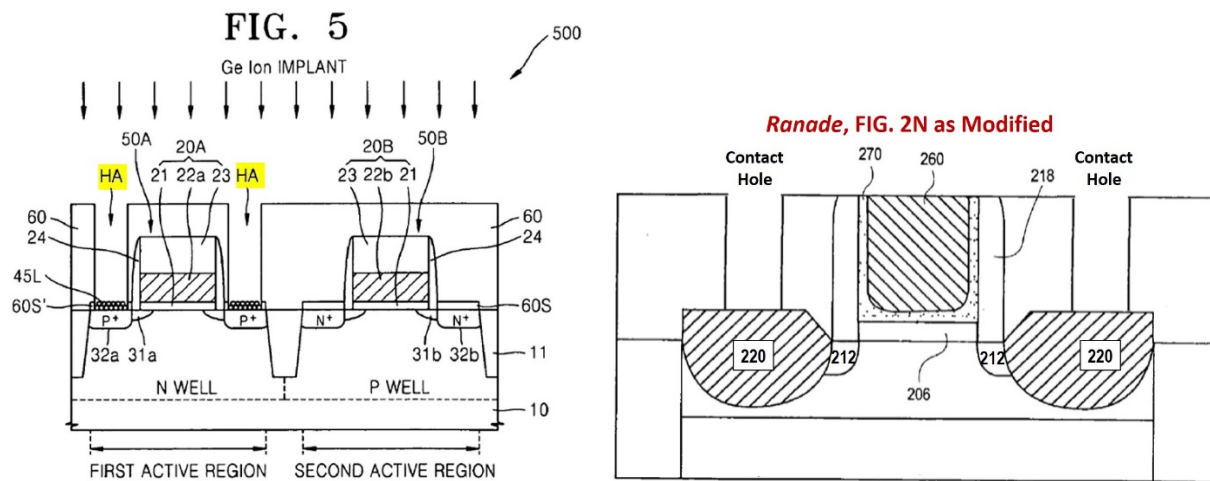
A POSITA would have found *Kim*'s Ge Overlayer Metalization and *Kim*'s Direct Metalization suitable for forming source/drain contacts to *Ranade*'s

FinFET. Thompson ¶¶196-197. Both were known techniques, and a POSITA would have recognized both as obvious ways to implement *Ranade's* FinFET. *Id.*

i. Ge Overlayer Metalization

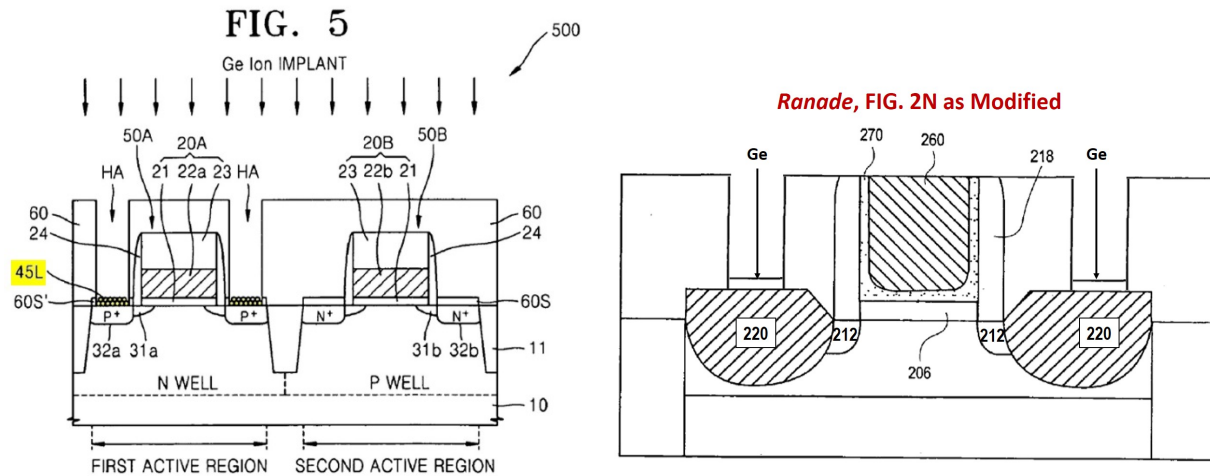
Kim's Ge Overlayer Metalization has five steps⁵: (1) Etch Contact Holes; (2) Form a Ge Overlayer; (3) Deposit Titanium; (4) Anneal to Form a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film; and (5) Form Contact Plugs. Thompson ¶199. Each applies readily to *Ranade's* FinFET.

First, *Kim* teaches contact holes HA etched into interlayer insulating film 60, as Figure 5 shows (below left). *Kim* ¶0072. Applied to *Ranade's* FinFET, it would resemble the figure on the right below. Thompson ¶200, ¶207.

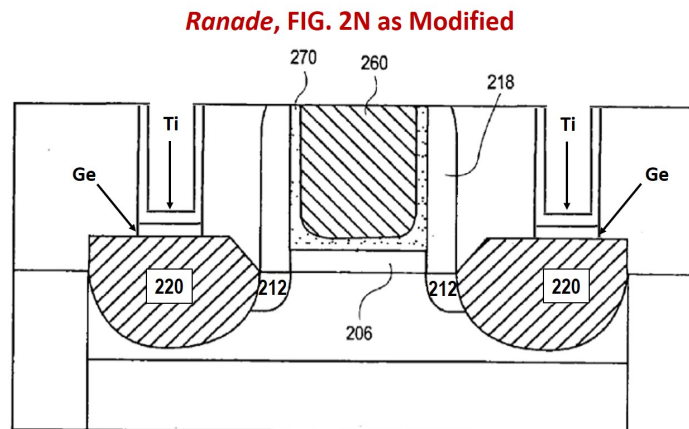


Second, *Kim* teaches forming a thin Ge overlayer 45L on the source/drain regions, as Figure 5 shows (below left). *Kim* ¶¶0072-0074. Applied to *Ranade's* FinFET, it would resemble the figure on the right below. Thompson ¶201, ¶208.

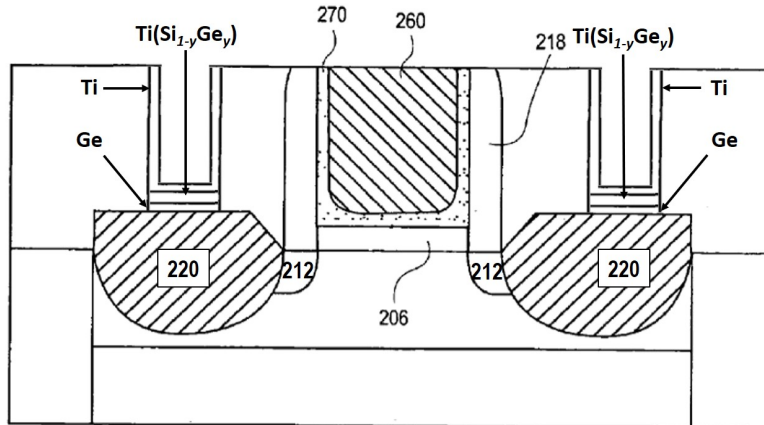
⁵ Same as the '281 Patent. See '281 Patent at Title, 11:60-12:22, 14:41-48, Fig. 7.



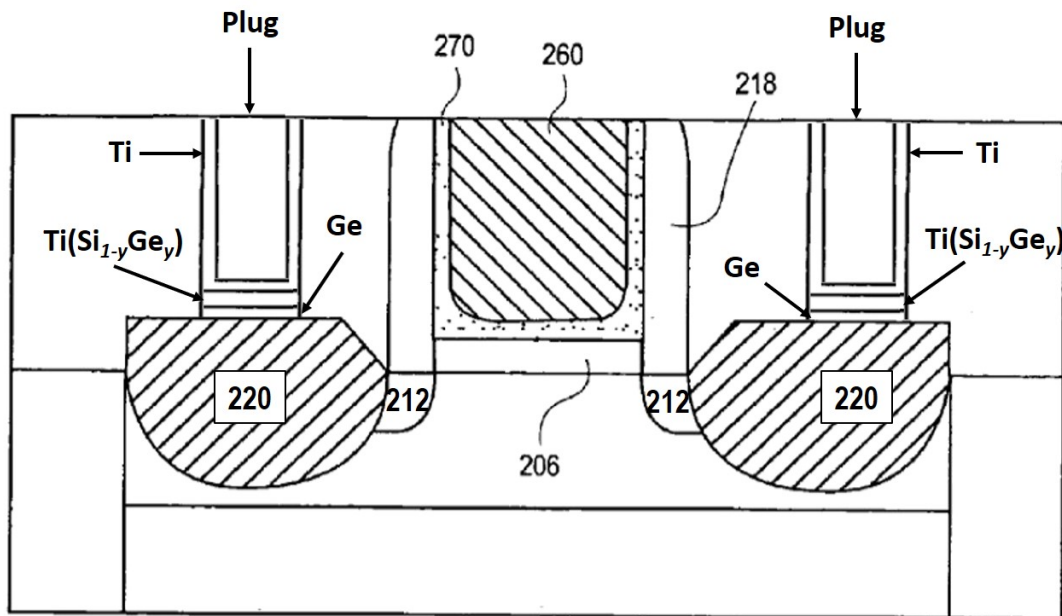
Third, a Ti layer 70 is deposited into contact holes HA. *Kim* ¶¶0047, ¶¶0057, ¶¶0066, ¶¶0071, ¶¶0073. Applied to *Ranade*'s FinFET, it would resemble the figure below. Thompson ¶¶202, ¶¶209.



Fourth, annealing causes Ti layer 70 to chemically react with the thin Ge layer 45L and atoms diffused from the source/drain region such that $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A forms. *Kim* ¶¶0072-0074. Applied to *Ranade*'s FinFET, it would resemble the figure below. Thompson ¶¶203, ¶¶210.

Ranade, FIG. 2N as Modified

Fifth, *Kim* teaches forming “contact plugs” 90 on the $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A in contact holes HA. *Kim* ¶0049, ¶0068, ¶0074. Applied to *Ranade*’s FinFET, it would resemble the figure below. Thompson ¶204, ¶211.

Ranade, FIG. 2N as Modified

Ranade-Kim: First Obvious Implementation (Ge Overlayer Metalization)

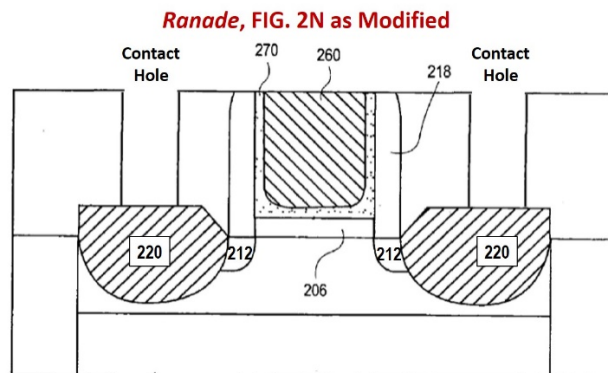
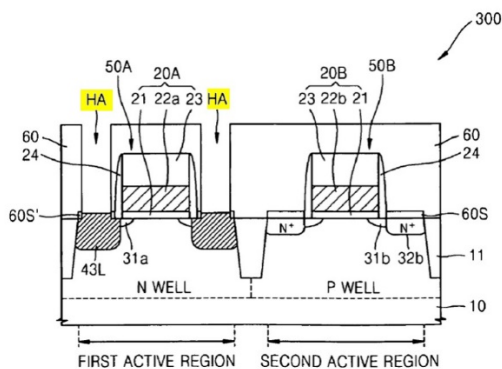
Ranade explains its FinFET is completed using “typical process steps to complete the formation of a MOS-FET, ... such as a silicidation step.” *Ranade* ¶¶0041. *Kim* discloses a silicidation step—Ge Overlayer Metalization. *Kim* ¶¶0072-0074, Fig. 5. A POSITA would have found a combination of *Ranade* and *Kim* resembling the above to be obvious. Thompson ¶212.

ii. Direct Metalization

Kim’s Direct Metalization⁶ has four steps: (1) Etch Contact Holes; (2) Deposit Titanium; (3) Anneal to Form a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film; and (4) Form Contact Plugs. Thompson ¶214; *see also Kim* at Figs. 3D-3F. Each applies readily to *Ranade*’s FinFET.

First, *Kim* teaches contact holes HA etched into interlayer insulating film 60, as Figure 3D shows (below left). *Kim* ¶¶0060-0061. Applied to *Ranade*’s FinFET, it would resemble the figure on the right below. Thompson ¶215, ¶221.

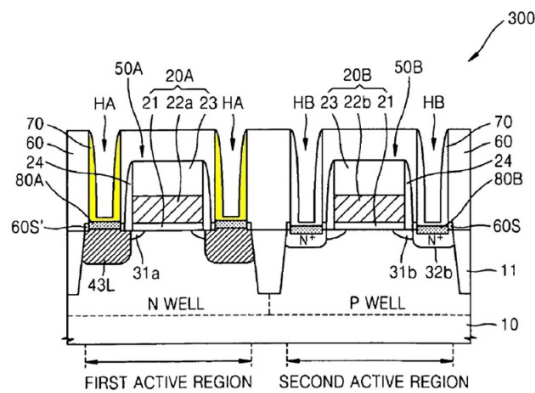
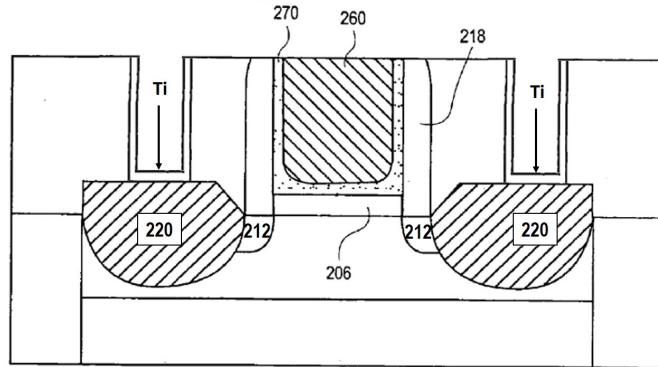
FIG. 3D



⁶ Admitted prior art. *See* '281 Patent at 2:43-64, 14:15-27, Fig. 7.

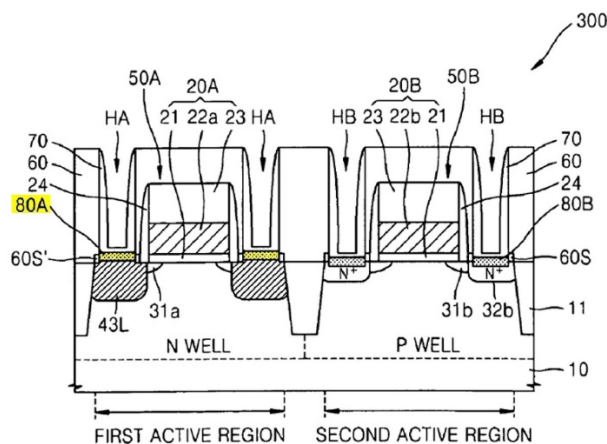
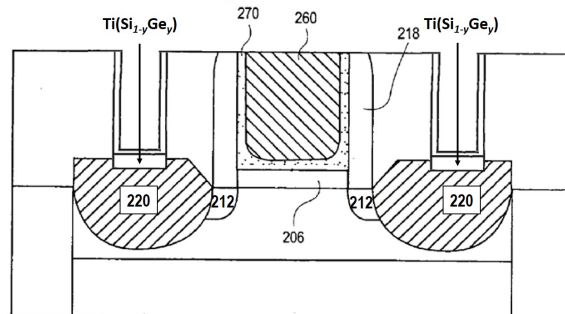
Second, a Ti layer 70 is deposited into contact holes HA, as Figure 3F shows (below left). *Kim* ¶0047, ¶0066. Applied to *Ranade*'s FinFET, it would resemble the figure on the right below. Thompson ¶216, ¶222.

FIG. 3F

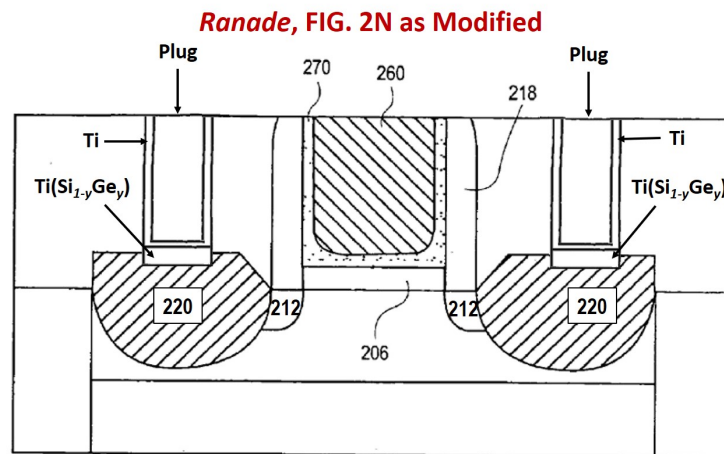
*Ranade, FIG. 2N as Modified*

Third, annealing causes Ti layer 70 to chemically react with SiGe source/drain regions 43L to form $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A (below left). *Kim* ¶¶0047-0050, ¶0067. Applied to *Ranade*'s FinFET, a $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film likewise would form (below right). Thompson ¶217, ¶223.

FIG. 3F

*Ranade, FIG. 2N as Modified*

Fourth, *Kim* teaches forming “contact plugs” on $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A in contact holes HA. *Kim* ¶0049, ¶0068. Applied to *Ranade*’s FinFET, it would resemble the figure below. Thompson ¶218, ¶224.



Ranade-Kim: Second Obvious Implementation (Direct Metalization)

Ranade explains its FinFET is completed using “typical process steps to complete the formation of a MOS-FET, ... such as a silicidation step.” *Ranade* ¶0041. *Kim* discloses a silicidation step—Direct Metalization. *Kim* ¶¶0047-0050, ¶¶0066-00668, Fig. 3F. A POSITA would have found a combination of *Ranade* and *Kim* resembling the above to be obvious. Thompson ¶225.

d. Rationales for combining *Ranade*’s and *Kim*’s teachings

First, a POSITA would have understood the combinations above combine known elements (*Ranade*’s FinFET and *Kim*’s source/drain contacts) according to

known methods (*Kim*'s Ge Overlayer Metalization or Direct Metalization) to yield predictable results (reduced contact resistance). Thompson ¶227.

Second, a POSITA would have understood the combinations above use a known technique (*Kim*'s Ge Overlayer Metalization or Direct Metalization) to improve similar devices (*Ranade*'s and *Kim*'s FinFETs) in the same way (by lowering contact resistance). Thompson ¶228.

Third, a POSITA would have understood the combinations above apply a known technique (*Kim*'s Ge Overlayer Metalization or Direct Metalization) to a known device ready for improvement (*Ranade*'s FinFET) to yield predictable results (reduced contact resistance). Thompson ¶229.

Fourth, a POSITA would have arrived at the combinations above due to a teaching, suggestion, or motivation in the prior art (those in *Ranade* and *Kim* and those discussed in Section III, including the need to reduce contact resistance) to arrive at the claimed invention. Thompson ¶230; *see also Ranade* ¶¶0038, ¶¶0041; *Kim* ¶¶0003-0007, ¶¶0010, ¶¶0047, ¶¶0050, ¶¶0071-0074.

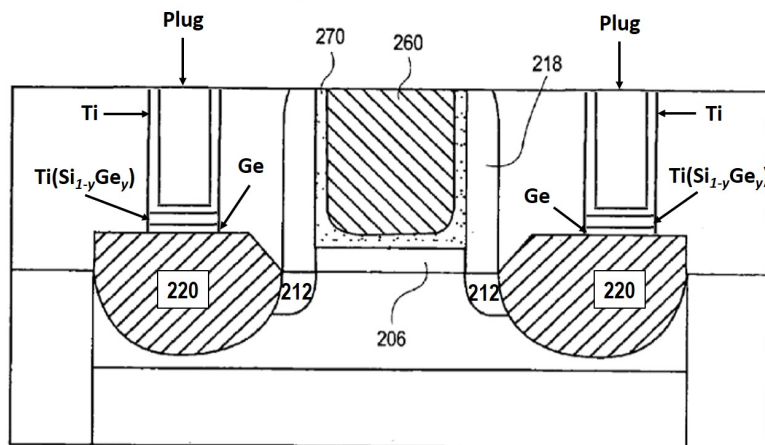
2. Claim 1

Because a POSITA would have wanted to combine *Ranade*'s and *Kim*'s teachings as described above, because a POSITA would have reasonably expected to succeed, and because at least one of the asserted *Ranade-Kim* combinations meets all elements of claim 1, claim 1 is unpatentable. *See Thompson* ¶325.

a. Element [1.0]

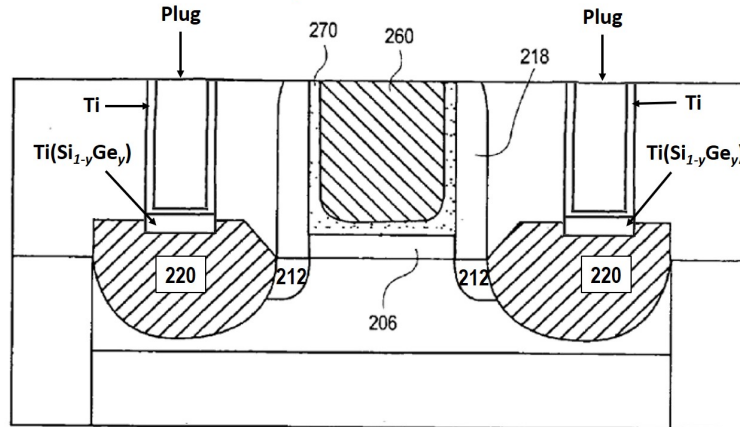
To the extent the preamble is limiting, the *Ranade-Kim* combinations provide “[a]n integrated circuit structure.” Thompson, ¶¶241-243. *Ranade* teaches a non-planar “tri-gate or FIN-FET transistor.” *Ranade* ¶0025, ¶¶0043-0044, Figs. 2N, 3C. Such FinFETs, approximated by the cross-section below, “may be incorporated into an integrated circuit” using “conventional processing steps, as known in the art.” *Id.* ¶0043, ¶0046.

Ranade, FIG. 2N as Modified



First Obvious Combination (Ge Overlayer Metalization)

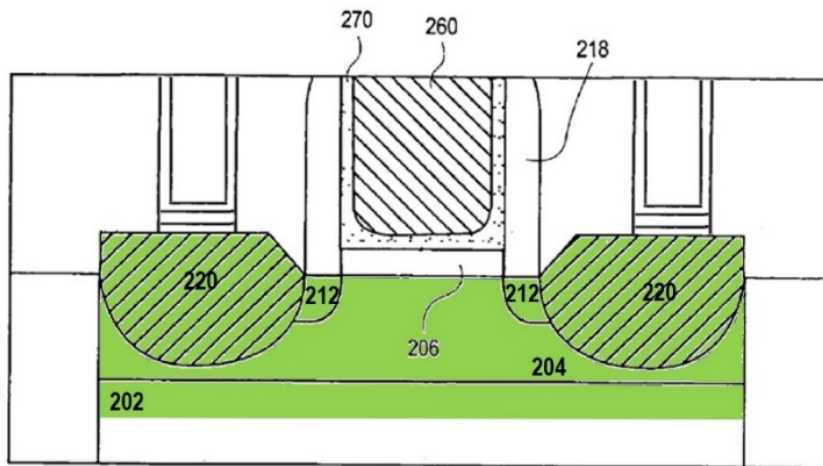
Ranade, FIG. 2N as Modified



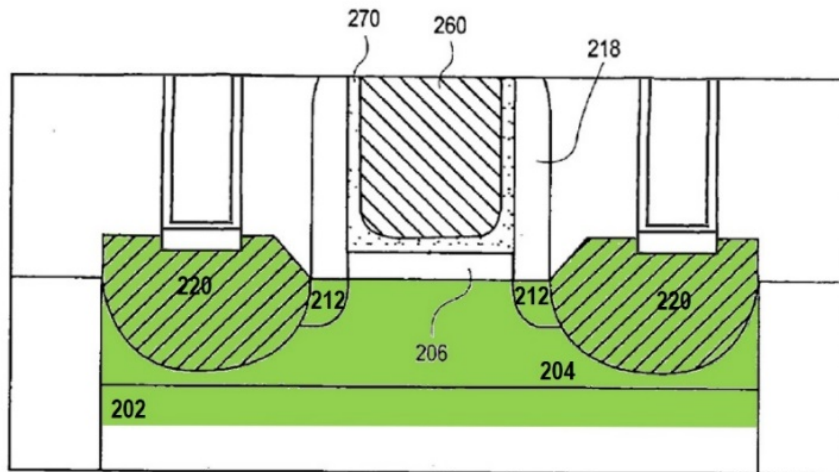
Second Obvious Combination (Direct Metalization)

b. Element [1.1]

The *Ranade-Kim* combinations include “a fin comprising silicon.” Shown in green below, *Ranade* teaches a FinFET with a fin that includes active region 204, epitaxial source/drain regions 220, source/drain tip extensions 212, and part of substrate 202. *Id.* ¶¶248-252.



***Ranade-Kim*: First Obvious Implementation (Ge Overlayer Metalization)**



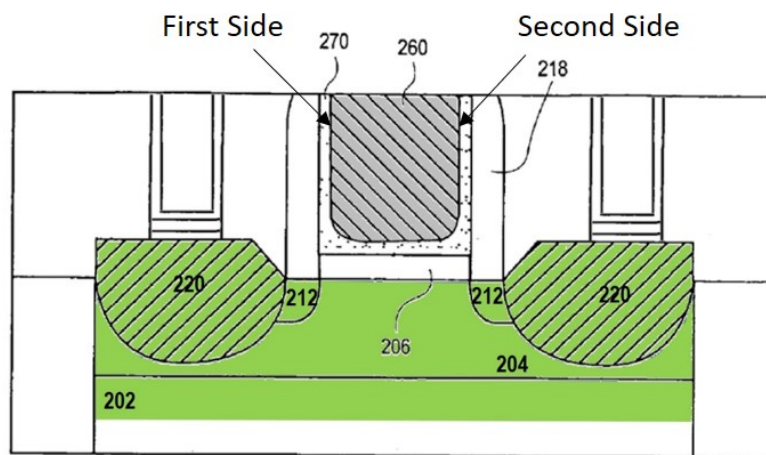
***Ranade-Kim*: Second Obvious Implementation (Direct Metalization)**

Substrate 202 is crystalline silicon or SiGe, and active region 204 and epitaxial source/drain regions 220 are “crystalline silicon/germanium.” *Ranade*

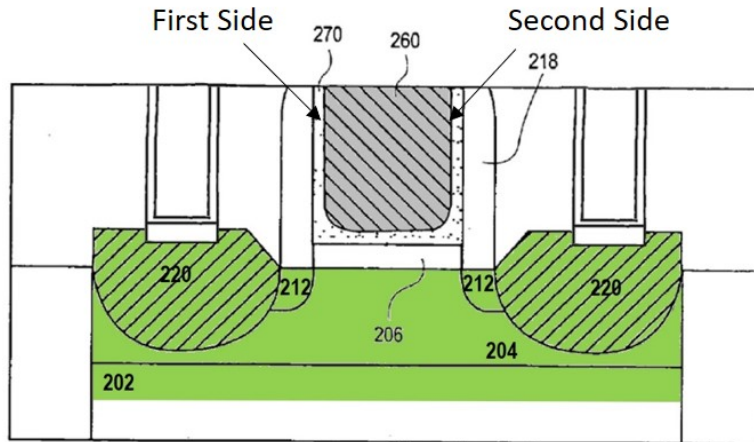
¶¶0026, ¶¶0032, ¶¶0040; *see also id.* ¶¶0016-0017, ¶¶0023. Tip extensions 212 are made of the same material as active region 204 because they are formed “by implanting charge-carrier dopant impurity atoms into active region 204.” *Id.* ¶¶0040. Each of these constituent fin regions (green) comprises silicon.

c. Element [1.2]

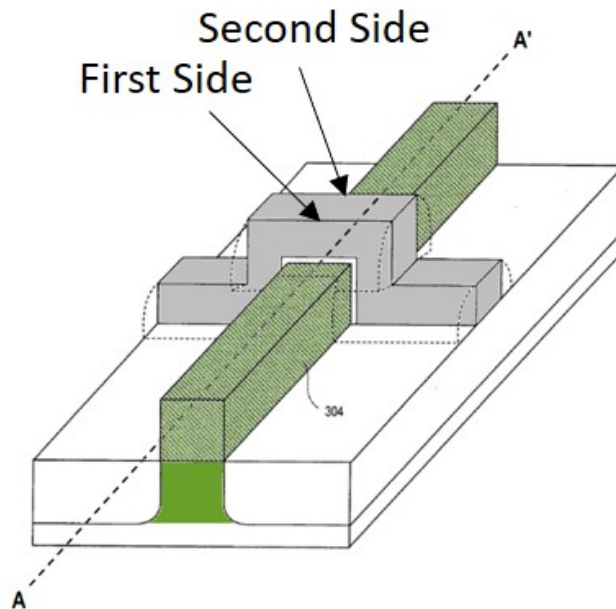
The *Ranade-Kim* combinations include “a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side.” *Ranade* teaches a FinFET with a gate electrode 208/260/308 over the fin. *Ranade* ¶¶0042; *see also id.* ¶¶0015, ¶¶0018-0020, ¶¶0028-0031, ¶¶0033-0037, ¶¶0041-0042, ¶¶0044-0046, Figs. 1A, 1B, 2B-3C. As the figures below show, the *Ranade-Kim* combinations likewise include a gate electrode (gray) over the fin (green). Thompson ¶¶256-259; *see also Kim* ¶¶0033; Korean *Kim* ¶¶0023. The gate electrode also has “a first side” and “a second side opposite the first side.”



Ranade-Kim: First Obvious Combination (Ge Overlayer Metalization)



Ranade-Kim: Second Obvious Combination (Direct Metalization)

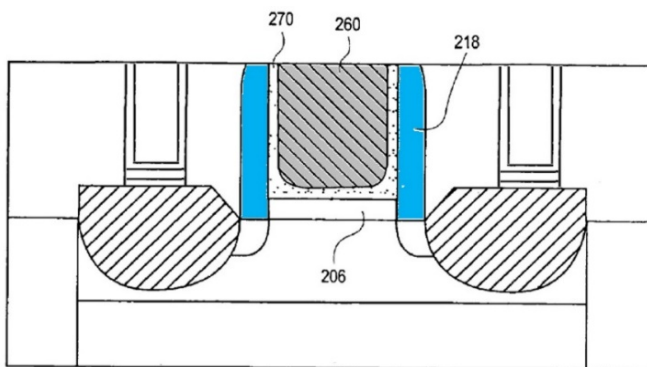


Ranade Fig. 3C⁷

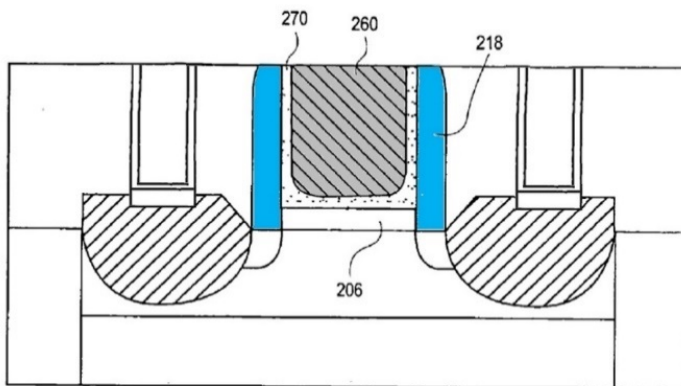
⁷ Figure 3C illustrates a stage of processing analogous to *Ranade's* Figure 2E (before forming tip extensions 212, source/drain regions 220, ILD 250, or replacement gate 260). Thompson ¶250 & n.305; *see also Ranade* ¶¶0025, ¶¶0032, ¶¶0044-0046, Figs. 2E-2N, 3A-3C.

d. Elements [1.3] and [1.6]

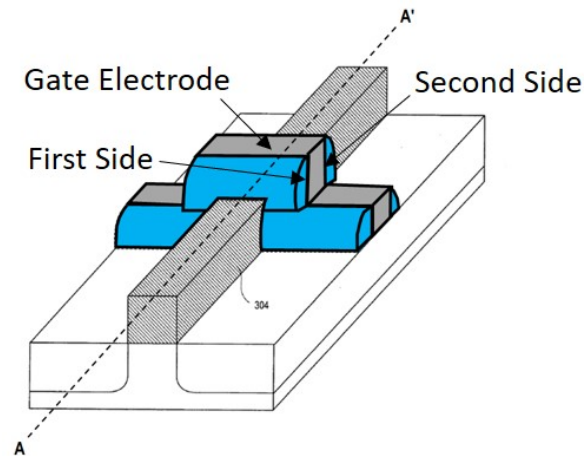
The *Ranade-Kim* combinations include “a [first/second] dielectric spacer along the [first/second] side of the gate electrode.” *Ranade* teaches a FinFET with dielectric spacers (“gate isolation spacers 218” made from “dielectric material 230”) along the sides of its gate electrode. *Ranade* ¶¶0036-0037; *see also id.* ¶¶0020, ¶¶0044-0045, Figs. 2H-2I. As the figures below illustrate, the *Ranade-Kim* combinations likewise include first/second dielectric spacers (blue) along the first/second sides of the gate electrode (gray).



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

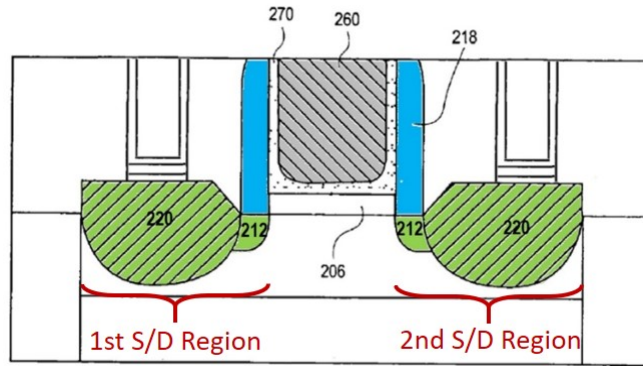


***Ranade* Fig. 3C**

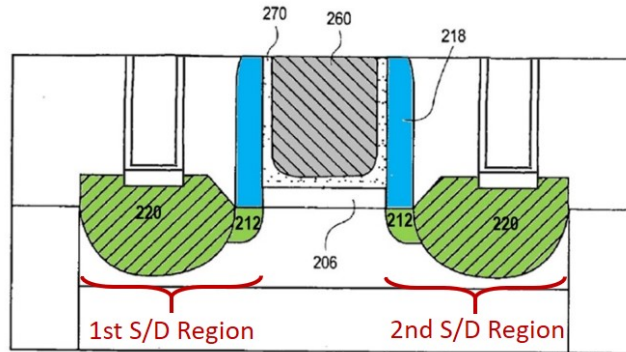
e. Elements [1.4] and [1.7]

The *Ranade-Kim* combinations include “a [first/second] source or drain region in the fin proximate the [first/second] side of the gate electrode, a portion of the [first/second] source or drain region beneath the [first/second] dielectric spacer.” *Ranade* teaches epitaxial source/drain regions 220 and source/drain tip extensions 212, which are together the claimed source/drain regions (green).⁸ See *Ranade* ¶¶0020-0023, ¶¶0031, ¶¶0034-0041, ¶¶0044-0046, Figs. 1B, 2G-3C. As the figures below show, these source/drain regions (green) are proximate to the sides of the gate electrode (gray), and part of each (e.g., source/drain tip extensions 212) lies below its respective dielectric spacer (blue). Thompson ¶¶268-270.

⁸ The '281 Patent says “each of the source and drain regions includ[es] a tip region.” '281 Patent at 17:24-29; see also *id.* at 3:37-65, 4:36-52, 9:8-20, Figs. 1A, 3A, 5A.



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

f. Elements [1.5] and [1.8]

In the *Ranade-Kim* combinations, “the [first/second] source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%.”

According to *Ranade*, “the pair of source/drain regions 220 comprises a **graded** epitaxial layer,” which “is a crystalline silicon/germanium region of the stoichiometry $\text{Si}_x\text{Ge}_{1-x}$, where $0 \leq x \leq 1$.” *Ranade* ¶0040. Epitaxial source/drain regions 220 thus have a graded Ge concentration ranging anywhere between 0 to 100%. Thompson ¶280. As *Ranade* explains, the Ge concentration in epitaxial source/drain regions 220 is increased from a lower concentration compatible with

the Ge concentration in active region 204 (where the channel is) to a higher concentration to compressively stress the channel. *Ranade* ¶¶0023; *see also id.* ¶¶0039-0040, ¶0064; Thompson ¶276, ¶¶280-281. Active region 204 itself can have up to or more than 50% Ge. *See Ranade* ¶¶0032-0033; Thompson ¶248.

In addition to this express disclosure of source/drain regions 220 graded in excess of 50% Ge, a POSITA would have found it obvious. Thompson ¶282. *Ranade*'s first-named inventor even previously described pFET source/drain regions with "a ~50 nm graded Si_{1-x}Ge_x layer at the interface" that had a "Ge mole fraction varying from 80% at the top surface to 1%" below. EX1044 at 1; *see also id.* at Fig. 1.

First, a POSITA would have known SiGe/Strained Silicon technology was ubiquitous. Thompson ¶¶283-285; *see also supra* Section III.B. For example, Intel's 90 nm, 65 nm, 45 nm, and 32 nm processes (released in 2003, 2005, 2007, and 2009, respectively) all used SiGe/Strained Si technology. Thompson ¶285. And Moore's Law was driving the amount of Ge in the source/drain regions higher over time. Thompson ¶280, ¶296; *see also* EX1014 at 4; EX1015 at 7.

Second, consistent with this trend, a POSITA would have been motivated to grade the Ge concentration in *Ranade*'s source/drain regions 220 to a concentration exceeding 50% to increase strain. Thompson ¶283, ¶¶287-288. A POSITA would have known adding more Ge to the source/drain regions strains the channel more

Specifically, a POSITA would have wanted to grade the Ge concentration in source/drain regions 220 (green below) in excess of 50% to provide more stress to active region 204 (peach below) where the pFET channel is located.⁹ Thompson ¶¶289-290; *see also* Ranade ¶0023, ¶0039; *supra* Section III.B.

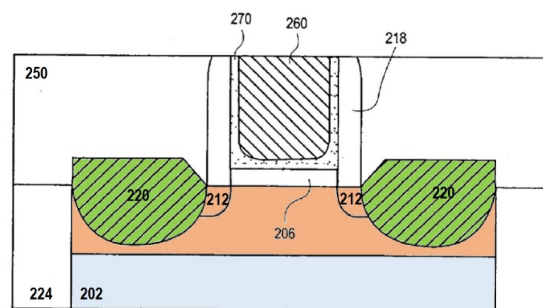
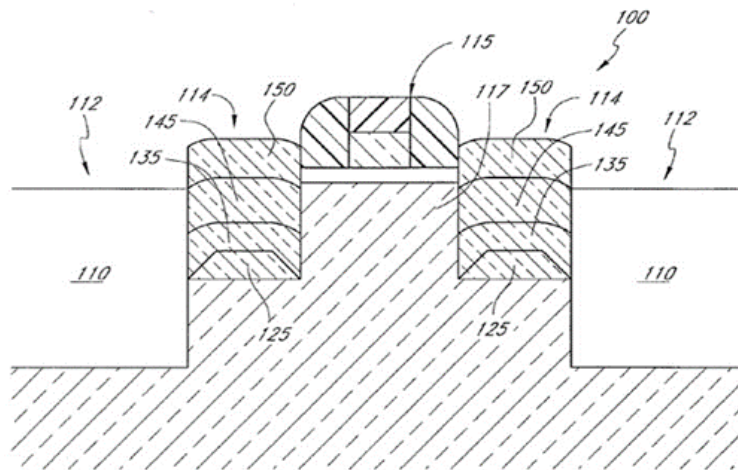


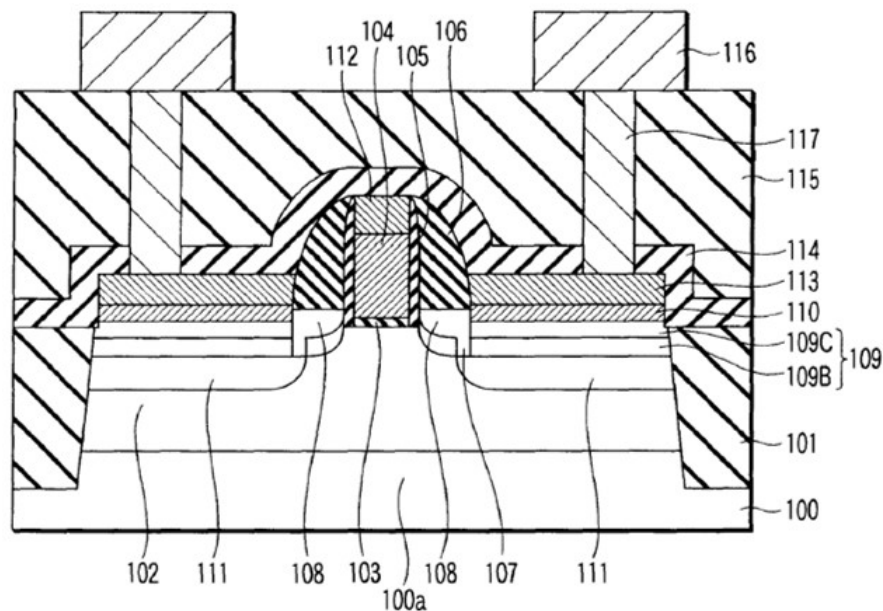
FIG. 2N

⁹ Active region 204 may itself have more than 50% Ge. *Ranade* ¶0023, ¶0032.

As the reference depicted below instructs, Ge grading increases the amount of Ge that can be incorporated into the SiGe crystal without excessive dislocations. EX1013 ¶¶0031-0034, ¶¶0042-0044, Fig. 5D; *see also* Thompson ¶291; *Ranade* ¶0040. For instance, in the figure below “layers 125, 135, 145, etc. may form a continuously graded layer” from as little as “10 atomic %” Ge at the bottom of the source/drain regions to as much as “60 atomic %” or even “100 atomic %” Ge at the top. EX1013 ¶¶0042-0045; Thompson ¶292.



Another exemplary reference confirms the same. *See* Thompson ¶293; EX1020 ¶¶0085-0094, Fig. 16. As shown below, the “germanium concentrations in the silicon germanium layer 109B and the germanium layer 110 are 10 to 30 at % and approximately 100 at %, respectively.” EX10 ¶0085. Between those layers 109B and 110, layer 109C has a graded Ge concentration that “is approximately 10 to 30 at %” at its lower interface with layer 109B and “approximately 100 at %” at its upper interface with layer 110. *Id.*



These and the other exemplary references, including *Ranade*, confirm it was known to grade epitaxial SiGe source/drain regions from as little as 0% Ge to as much as 100% Ge, including in excess of 50%. Thompson ¶294.

Third, a POSITA would have known that grading the Ge concentration in excess of 50% differs only in degree, not in kind, from grading to a concentration less than 50% and does not yield any new or unexpected results. Thompson ¶283, ¶295. “[E]ven a slight overlap in range establishes a *prima facie* case of obviousness.” *Genentech, Inc. v. Hospira, Inc.*, 946 F.3d 1333, 1341 (Fed. Cir. 2020) (quotation omitted). Here, *Ranade* discloses the entire range. *Ranade* ¶0040. Patent Owner may overcome this “presumption of obviousness” only by showing a “critical” result—a “new and unexpected result which is different in kind and not merely in degree from the results of the prior art.” *DuPont de Nemours & Co. v.*

Synvina C.V., 904 F.3d 996, 1006 (Fed. Cir. 2018). Nothing in the '281 Patent or the literature suggests 50% Ge is “critical” or associated with unexpected results. Thompson ¶¶297-299. As Dr. Thompson explains, the difference between 50 and 51% Ge, for example, “is negligible (and well within the range of normal process variation).” *Id.* ¶¶298-299.

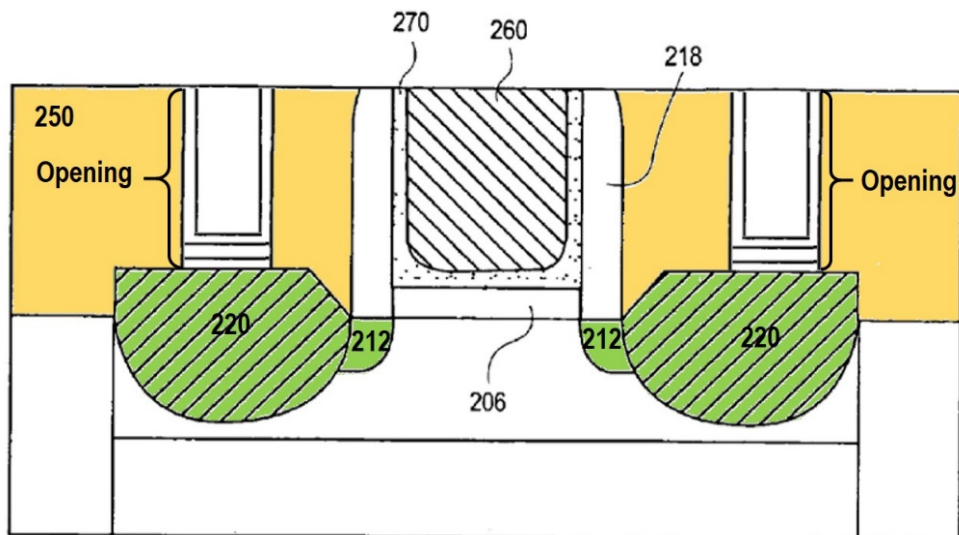
By failing to distinguish source/drain regions with more than 50% Ge and less than 50% Ge, the '281 Patent confirms the lack of criticality. *See* '281 Patent at 3:57-62 (20-100% Ge), 4:29-34 (10-70% Ge), 6:65-7:6 (30-70% Ge). The '281 Patent confirms that source/drain regions at any concentration (including more than 50% Ge) can be formed “using any number of conventional techniques.” *Id.* at 4:27-34. The only examples that specifically mention 50% Ge appear in a long list of permutations with no significance attributed to that value. *See id.* at 16:16-18:29. Because a Ge concentration in excess of 50% Ge is not critical, and because there was a known trend towards increasing the Ge concentration, a POSITA would have found claim elements [1.5] and [1.8] obvious. Thompson ¶283, ¶296, ¶300.

In sum, a POSITA would have understood *Ranade* expressly discloses “the [first/second] source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%.” Further, a

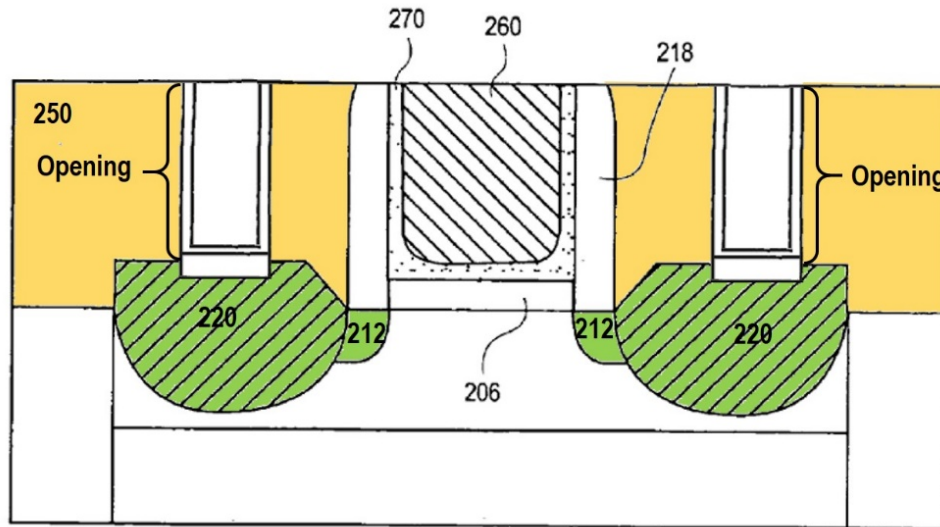
POSITA would have found this feature obvious based on *Ranade*'s teachings viewed with his or her training, experience, and industry trends. Thompson ¶¶300.

g. Element [1.9]

The *Ranade-Kim* combinations include “a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region.” As shown below, *Ranade* teaches “an interlayer dielectric 250” (yellow) over the claimed source/drain regions (green), and *Kim* teaches openings to expose portions of each source/drain region (green). See *Ranade* ¶¶0041, Figs. 2L-2N; *Kim* ¶¶0061-0062, ¶0072, Figs. 3D, 5; Thompson ¶¶305-306.



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

h. Elements [1.10] and [1.11]

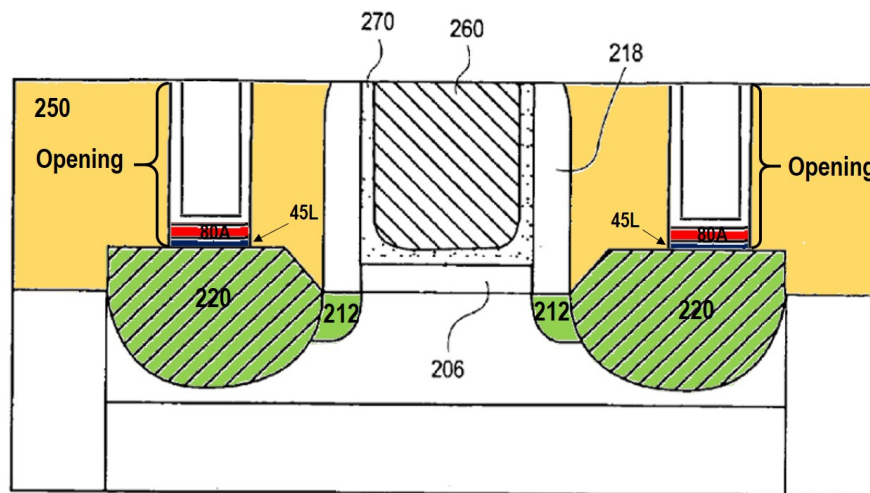
Depending how “germanide layer” is construed and how the phrase “in the first opening and over the portion” is applied, at least one of the asserted *Ranade-Kim* combinations includes “a [first/second] germanide layer in the [first/second] opening and over the portion of the [first/second] source or drain region, the [first/second] germanide layer comprising silicon, germanium and titanium.” Thompson ¶308.

As Section VIII.A.1 explains, a POSITA would have recognized two obvious applications of *Kim*’s teachings to *Ranade*’s FinFET—Ge Overlayer Metalization and Direct Metalization. The Ge Overlayer combination satisfies claim elements [1.10] and [1.11] under either party’s construction of “germanide layer” and any conceivable interpretation of “in the first opening and over the portion.” *Id.* ¶309. The Direct Metalization combination satisfies claim elements

[1.10] and [1.11] under Patent Owner’s construction of “germanide layer” and its apparent interpretation of “in the first opening and over the portion” (by which a germanide layer partially outside the ILD opening and partially within the source/drain region is nevertheless “in” the opening and “over” the contact area).
Id.

i. Ge Overlayer Metalization

The figure below provides an approximate cross-section for the Ge Overlayer Metalization combination. *Supra* Section VIII.A.1.c.i. $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A (red) forms by reacting a Ti layer with a thin Ge Overlayer (dark blue) and atoms that diffuse from the SiGe source/drain regions (green). Thompson ¶310.



Ranade-Kim: First Obvious Combination (Ge Overlayer Metalization)

$\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A (red) is a “germanide layer” under either party’s proposed construction, and it “compris[es] silicon, germanium, and titanium.” $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A (red) also satisfies any conceivable interpretation of the

phrase “in the first opening and over the portion” because it lies wholly within the ILD opening and wholly above the source/drain regions. Thus, the Ge Overlayer Metalization combination satisfies claim elements [1.10] and [1.11]. Thompson ¶¶311-314.

For comparison, annotated Figure 5F of the '281 Patent appears below.

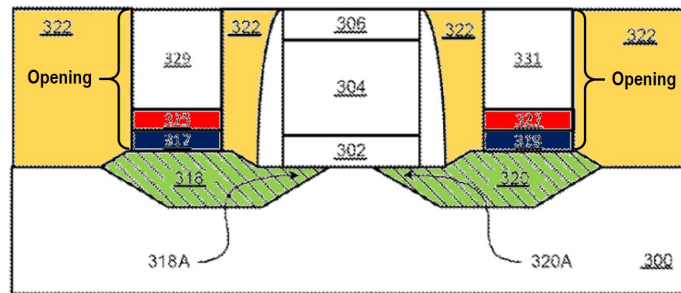
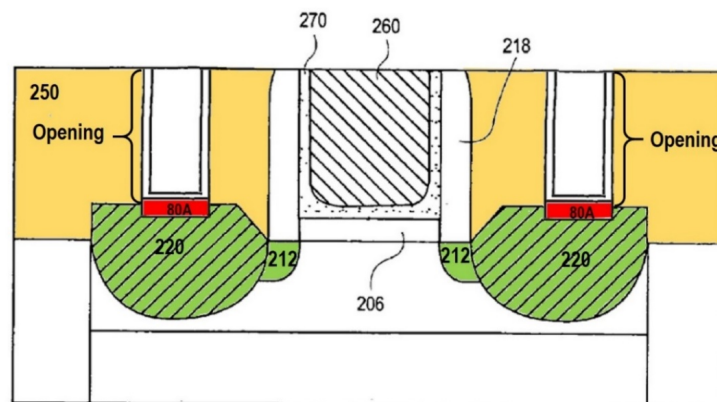


FIG. 5F

ii. Direct Metalization

The figure below provides an approximate cross-section for the Direct Metalization combination. *Supra* Section VIII.A.1.c.ii. $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ film 80A (red) forms by chemically reacting *Ranade*'s SiGe source/drain regions (green) with a Ti layer. Thompson ¶315.



Ranade-Kim: Second Obvious Combination (Direct Metalization)

Ti(Si_{1-y}Ge_y) film 80A (red) is a “thickness of material, comprising germanium and a metal” (Patent Owner’s construction of “germanide layer”), and it “compris[es] silicon, germanium, and titanium.” Also, under Daedalus’s apparent interpretation of “in the first opening and over the portion,” it is “in the first opening and over the portion of the first source or drain region” because it lies at least partially within the ILD opening and at least partially extends above the source/drain regions. Thus, the Direct Metalization combination satisfies limitations [1.10] and [1.11] under Patent Owner’s proposed construction of “germanide layer” and apparent interpretation of “in the first opening and over the portion of the first source or drain region.” Thompson ¶¶316-318.

For comparison, annotated Figure 5F of the '281 Patent appears below.

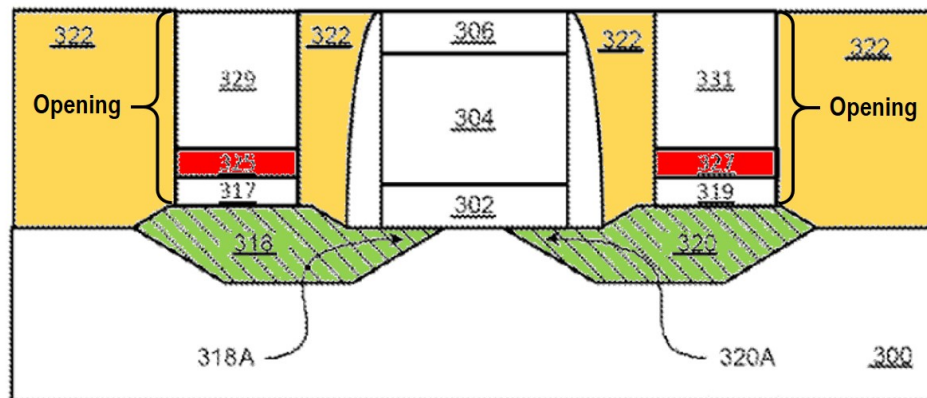
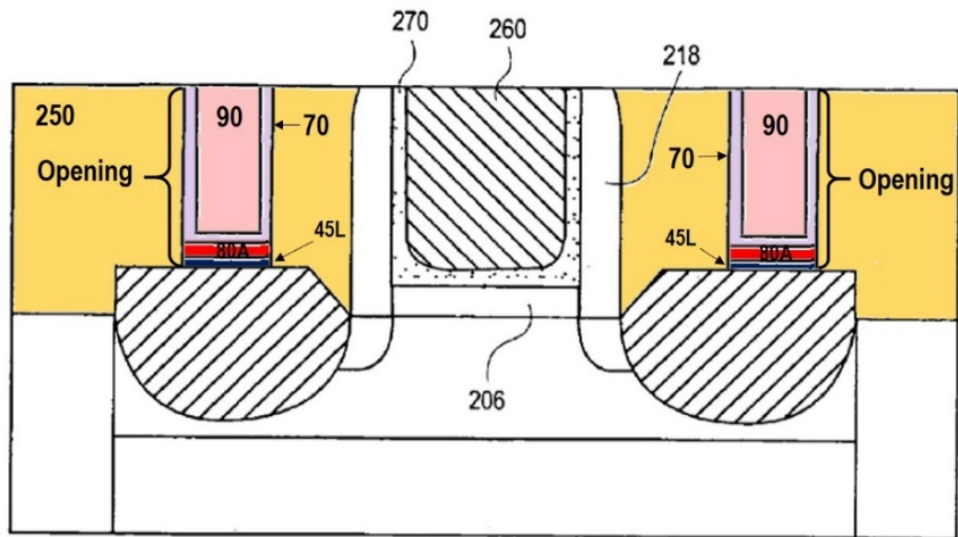


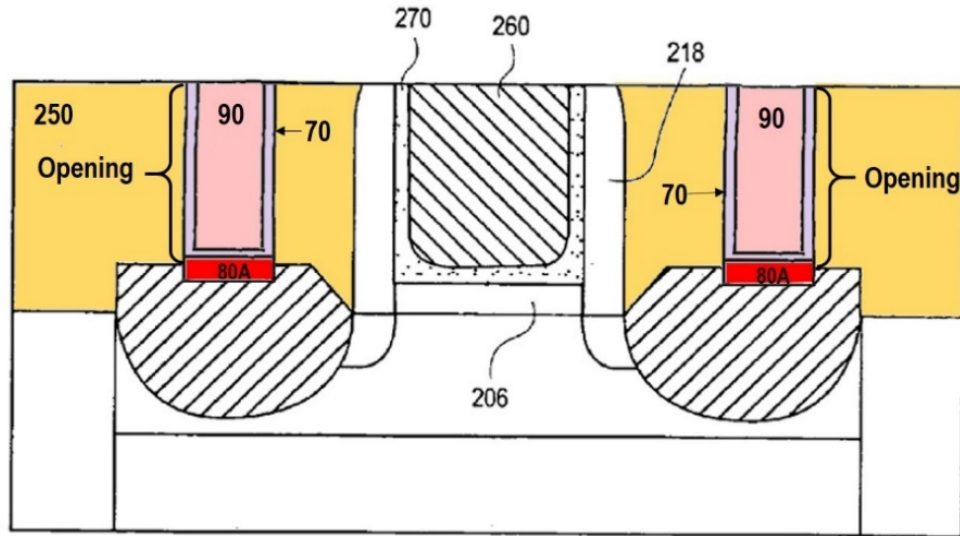
FIG. 5F

i. Elements [1.12] and [1.13]

Subject to the caveats in Section VIII.A.2.h, at least one of the asserted *Ranade-Kim* combinations includes “a [first/second] contact plug in the [first/second] opening and on the [first/second] germanide layer.” As the figures below illustrate, the *Ranade-Kim* combinations include source/drain “contact plugs 90” (pink) in the openings of interlayer dielectric 250 (yellow) and on the $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)$ germanide film 80A (red). See *Kim* ¶¶0049-0050, ¶0058, ¶0068, Figs. 1F, 2D; *Ranade* ¶0041, Figs. 2L-2N; Thompson ¶322. Such contact plugs were nearly universal in the industry. See Thompson ¶¶91-93, ¶322; EX1026 at 20-21, 41-45, Figs. 9.19-9.22, 12.9, 12.14.



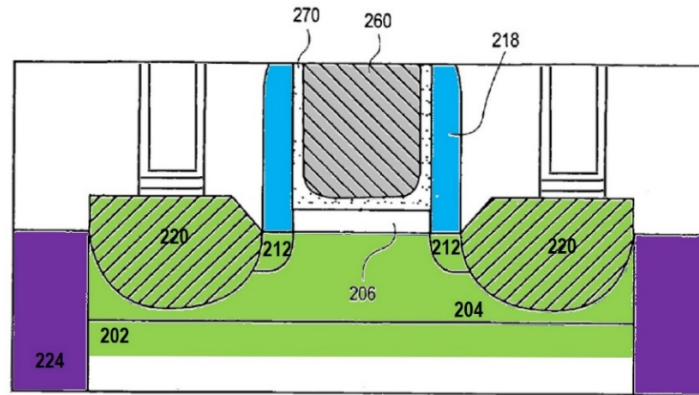
***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



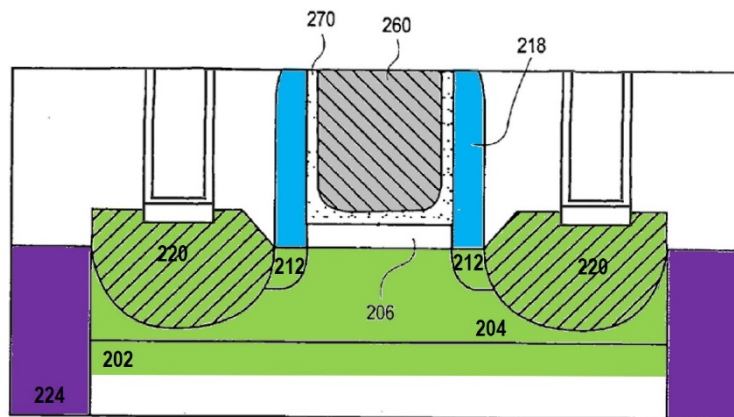
***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

3. Claim 5

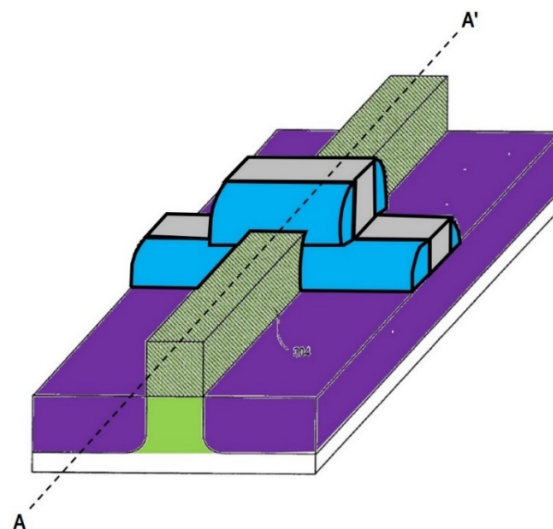
The *Ranade-Kim* combinations include “an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region.” As shown below, *Ranade* teaches “shallow trench isolation regions 224 and 226” (purple) through which the fin (green) protrudes and over which portions of the gate electrode (gray) and dielectric spacers (blue) are formed. *Ranade*, ¶0030; see also *id.* ¶0031, Figs. 2C, 2C’, 2J-2K, 3A-3C. A portion of the gate electrode (gray) and a portion of the dielectric spacers (blue) lie over the isolation region (purple). Thompson ¶¶328-330.



Ranade-Kim: First Obvious Combination (Ge Overlayer Metalization)

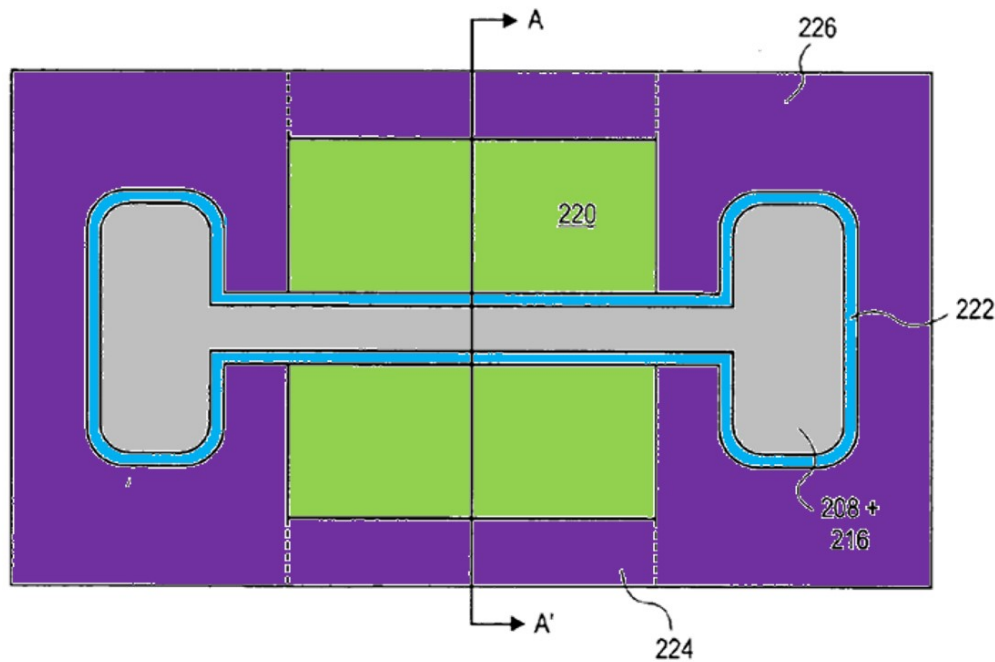


Ranade-Kim: Second Obvious Combination (Direct Metalization)



Ranade Fig. 3C

Ranade's Figure 2C' confirms this feature. Although it shows a planar device, the only difference for a FinFET would be that the green region corresponds to one or more fin rather than wider planar source/drain regions. Thompson ¶331. The figures above confirm the fins (green) extend through the isolation regions (purple). And *Ranade* further explains the gate structure (including gate electrode (gray) and gate isolation spacers (blue)) must be formed on top of isolation region 226 (purple). *Ranade* ¶0030; *see also* Thompson ¶331.

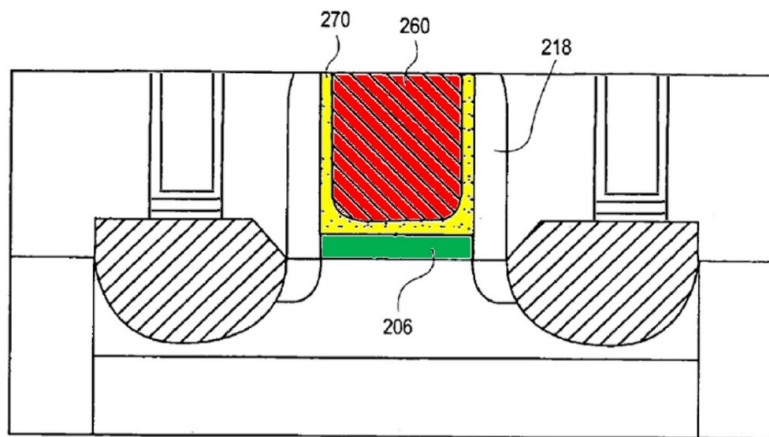


Ranade, Fig. 2C'

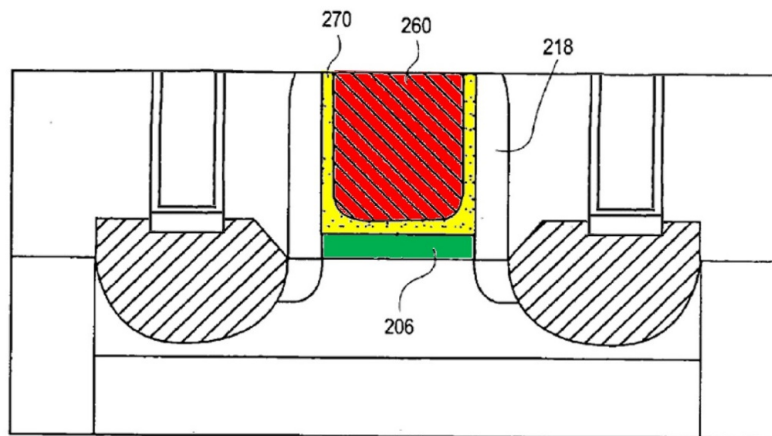
4. Claim 6

The *Ranade-Kim* combinations include “a gate dielectric layer, wherein the gate electrode is on the gate dielectric layer, wherein the gate dielectric layer

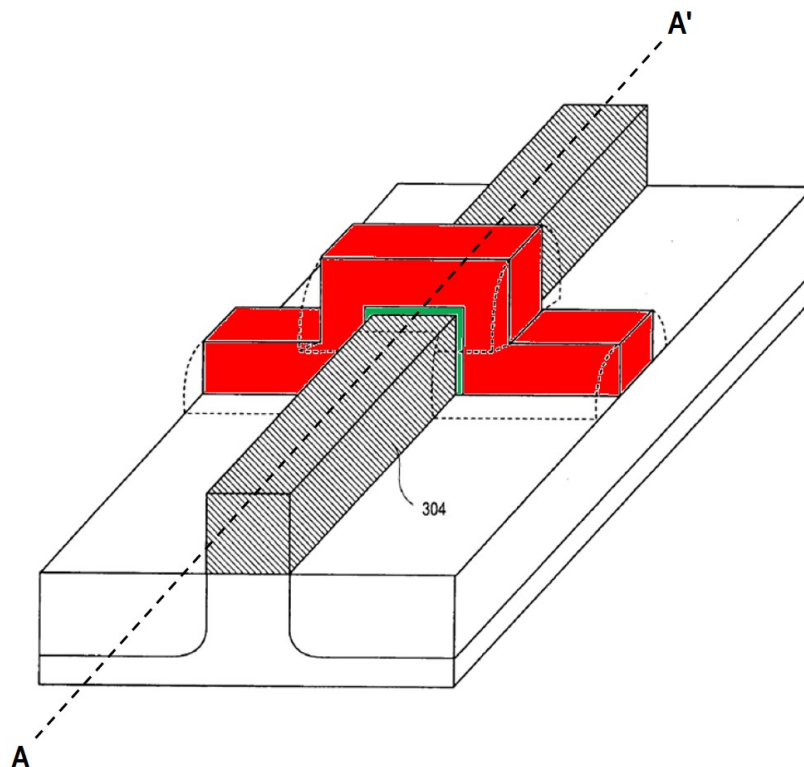
comprises a high-k dielectric material, and wherein the gate electrode comprises a metal layer.” As shown below, *Ranade*’s FinFET includes a gate electrode (red) “formed above gate dielectric layer 206” (green). *Ranade* ¶¶0028; *see also id.* ¶¶0015, ¶¶0042, ¶¶0044-0045, Figs. 2M-2N, 3A-3C. It may also lie on “additional gate dielectric layer 270” (yellow). *Id.* ¶¶0042. Gate dielectric layers 206 and 270 may be high-k dielectrics. *Id.* ¶¶0011, ¶¶0015, ¶¶0018, ¶¶0024, ¶¶0027, ¶¶0042, ¶¶0044-0045. Gate electrode 208 and alternative gate electrode 260 may be metals. *Id.* ¶¶0019, ¶¶0028, ¶¶0042, ¶¶0044-0045; *see also* Thompson ¶¶335-336.



Ranade-Kim: First Obvious Combination (Ge Overlayer Metalization)



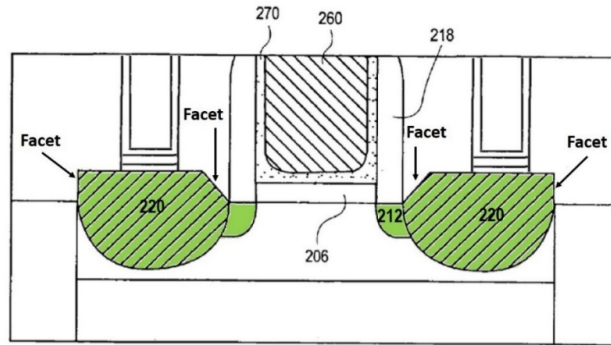
Ranade-Kim: Second Obvious Combination (Direct Metalization)



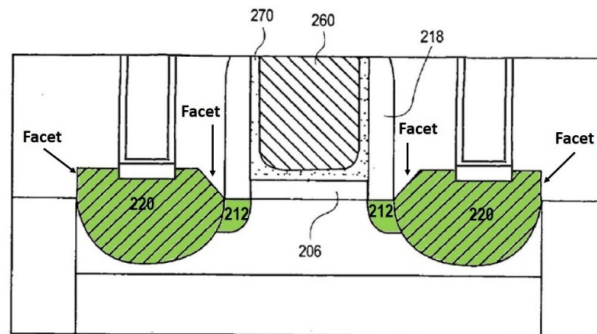
Ranade, Fig. 3C

5. Claim 7

In the *Ranade-Kim* combinations, “the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets.” A POSITA would have understood a “facet” refers to a semiconductor crystal surface. *Id.* ¶342. The ’281 Patent does not actually mention facets; it simply notes the source/drain regions are epitaxial. ’281 Patent at 4:29-34, 5:45-53, 13:43-47. So are *Ranade*’s source/drain regions 220. *Ranade* ¶0040. A POSITA would have known that, by definition, epitaxial films are crystalline and thus terminated by facets as shown below. Thompson ¶347.



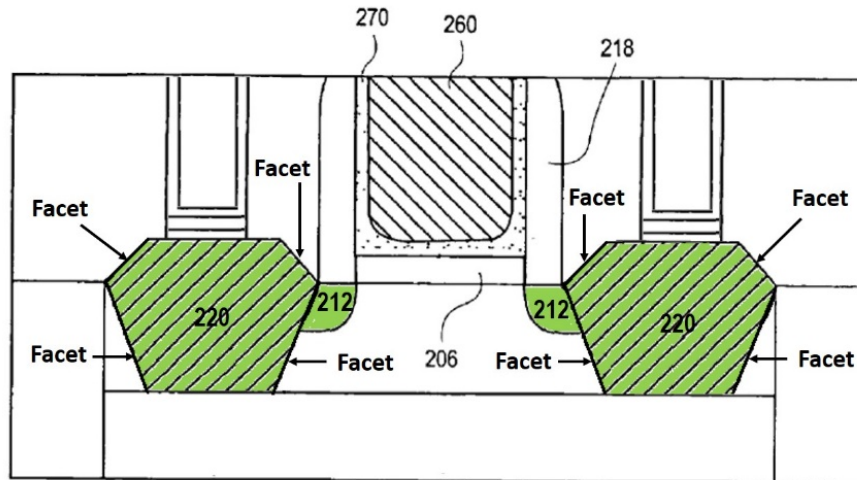
Ranade-Kim: First Obvious Combination (Ge Overlayer Metalization)



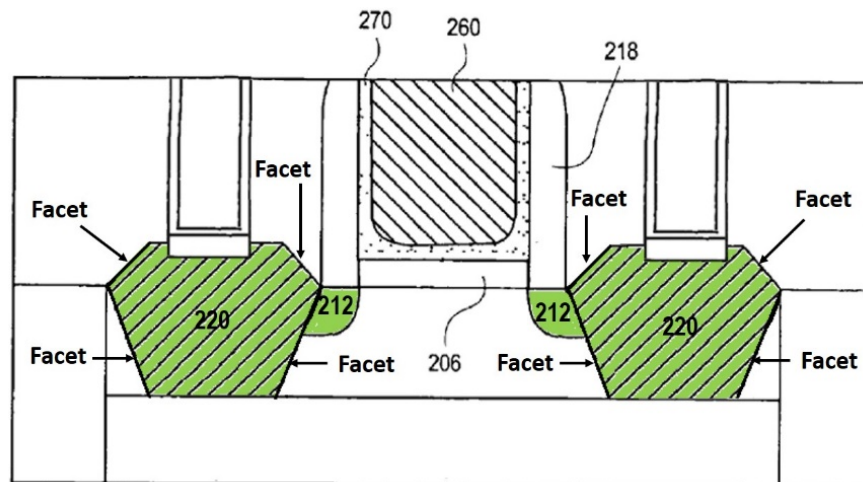
Ranade-Kim: Second Obvious Combination (Direct Metalization)

The '281 Patent also briefly mentions “an ammonia etch to form [a] faceted fin recess” where epitaxial growth takes place. '281 Patent at 7:27-32; *see also id.* at Figs. 3A, 5A. So does *Ranade*. *Ranade* ¶¶0031, ¶¶0038, Fig. 2D', 2J. A POSITA would have understood this ensures $\langle 111 \rangle$ crystal facets along the sides of the fin. Thompson ¶¶343-345. As shown above, the source/drain regions (green) in the *Ranade-Kim* combinations comprise epitaxial source/drain regions 220 and source/drain tip extensions 212, which include at least two facets. Thompson ¶348. By applying *Ranade*'s ammonia etch (which *Ranade* expressly does not illustrate), epitaxial source/drain regions 220 would further include the facets below. *Id.* ¶345,

¶349; *see also Ranade* ¶0031, ¶0038, Figs. 2D', 2J; EX1047 at Fig. 2; EX1048 at Fig. 6.



Ranade-Kim: First Obvious Combination (Ge Overlayer Metalization)



Ranade-Kim: Second Obvious Combination (Direct Metalization)

A POSITA would have understood *Ranade*'s Figure 3C below shows *Ranade*'s FinFET at a stage of processing analogous *Ranade*'s Figure 2E. Thompson ¶341. Faceted epitaxial source/drain regions 220 replace the exposed

parts of active region 304 not covered by the gate in the manner described above.

See id.; *Ranade* ¶¶0038-0040, ¶0044, Figs. 2I-2K.

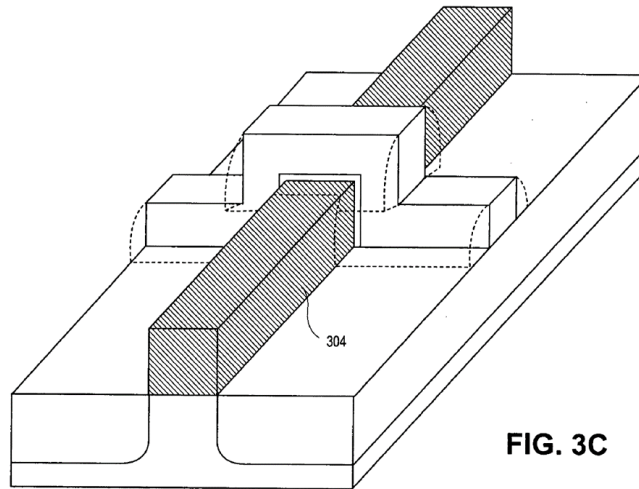


FIG. 3C

In addition to these express disclosures, a POSITA also would have understood epitaxially grown SiGe fin regions have either a faceted diamond shape or a faceted rectangular shape, depending on wafer and channel orientation. *Supra* Section III.D; Thompson ¶346. A POSITA would have understood *Ranade*'s source/drain regions 220 use (100) surface-oriented wafers and “naturally grow in a diamond shape” as illustrated below. EX1036 at 10:25-26; *see also id.* at 1:27-43, 5:21-6:7, 7:42-50, 10:1-40, 10:61-66, 12:12-20, Fig. 5A; EX1038 at Fig. 7b; *supra* Section III.D; Thompson ¶346.

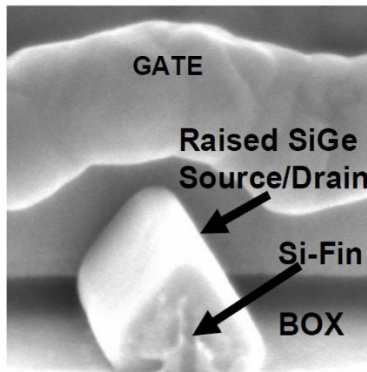
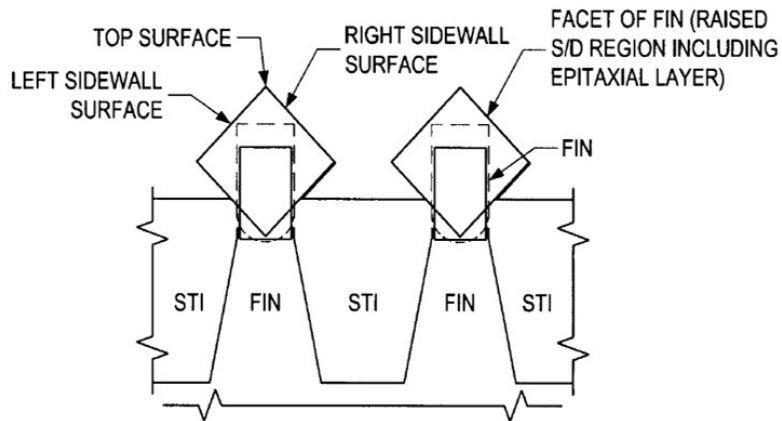


Fig. 7b Y-dir. cross-section of PMOS Trigate with SiGe raised source/drain

EX1038, Fig. 7b



EX1036, Fig. 5A

Thus, in addition to satisfying claim 7 based on *Ranade*'s express disclosure of facets, a POSITA also would have found it obvious from his or her training and experience. Thompson ¶¶350-351.

6. Claim 8

Claim 8 is identical to claim 1, except limitations [8.1], [8.2], [8.4], and [8.7] recite a "body" instead of a "fin." The '281 Patent uses the term "body" only once, equating it with a "fin." '281 Patent at 13:35-38; *see also* Thompson ¶353; *Brask* at 5:26-30, 18:3-16, Figs. 3, 5I. Thus, a POSITA would have understood there is no meaningful difference between claims 1 and 8, and at least one of the asserted *Ranade-Kim* combinations satisfies claim 8 for the reasons stated in Sections VIII.A.2.a-i. Thompson ¶¶352-366; *see also Mycogen Plant Sci., Inc. v. Monsanto Co.*, 243 F.3d 1316, 1329 (Fed. Cir. 2001) ("It is not unusual that separate claims

may define the invention using different terminology, especially where (as here) independent claims are involved.”).

7. Claims 12-20

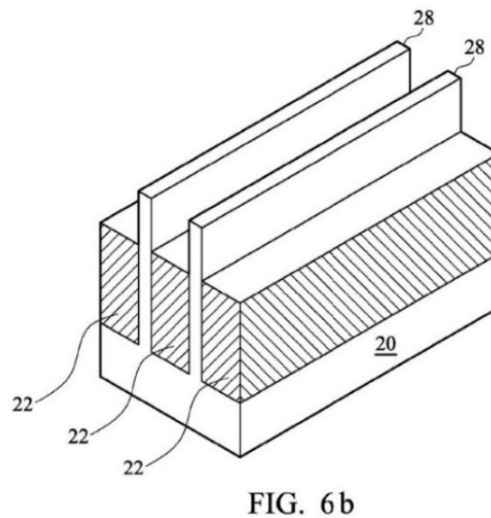
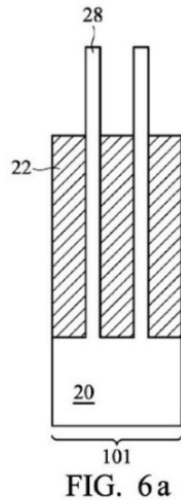
At least one of the *Ranade-Kim* combinations satisfies claims 12-20 for the reasons in Section VIII.C *infra*.

B. Ground 2A: The *Tung-Brask-Yu* Combination

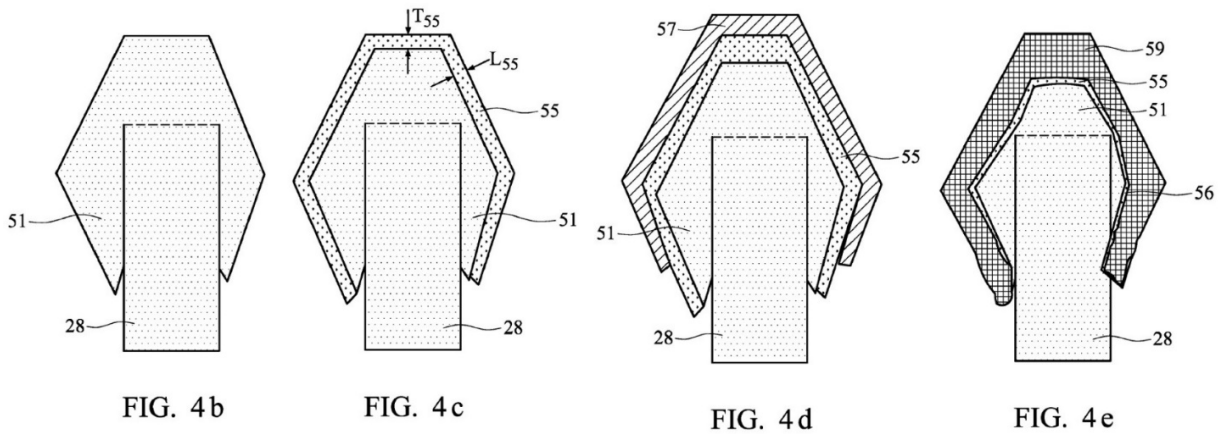
1. A POSITA Would Have Found the *Tung-Brask* Combination Obvious

a. A POSITA would have found it obvious to use *Brask*’s graded source/drain region in *Tung*’s FinFET

Tung teaches “structures and methods of fabrication thereof with low resistance contacts for non-planar semiconductor structures” (FinFETs). *Tung* ¶0006; *see also id.* ¶0005, ¶0021, ¶¶0027-0032, ¶0034, ¶0039, ¶0061. Over each fin 28 lies a semiconductor material 51, a doped semiconductor layer 55, and a metal-semiconductor contact layer 59. *Supra* Section VII.C. As explained below, a POSITA would have found it obvious to grade the Ge concentration of *Tung*’s SiGe semiconductor material 51 from a level compatible with the underlying Si fin 28 to a level compatible with the overlying doped SiGe or Ge semiconductor layer 55. *See* Thompson ¶¶521-522; EX1019 ¶0020, ¶0038, ¶0044, ¶¶0053-0058; EX1020 ¶¶0004-0005, ¶0034, ¶¶0085-0094; EX1013 at Abstract, ¶¶0003-0008, ¶¶0030-0032, ¶0042, ¶0063; EX1045 ¶¶0022-0024; EX1022 ¶¶0059-0060.



Tung teaches a FinFET that begins with a fin region 28 made of silicon (above). *Tung* ¶¶0048-0051, Figs. 6a-6b. To form *Tung*'s source/drain regions, SiGe semiconductor material 51 selectively grows over fin 28 as in Figure 4b below. *Id.* ¶¶0040, ¶¶0074, ¶¶0076. A doped semiconductor layer 55 (e.g., SiGe or Ge) then selectively grows over SiGe layer 51 as in Figure 4c below. *Id.* ¶¶0034, ¶¶0041, ¶¶0058, ¶¶0078. After depositing a metal layer 57 (e.g., Ti) over doped semiconductor layer 55 as in Figure 4d below, the structure is annealed so metal layer 57 “reacts with the doped semiconductor layer 55” to form a metal-semiconductor layer 59 (e.g., TiSiGe) as in Figure 4e. *Id.* ¶¶0041-0043, ¶¶0045, ¶¶0061-0064, ¶¶0080-0081; *see also* Thompson ¶¶523-527.



Because the interface between doped semiconductor layer 55 and metal-semiconductor layer 59 defines the Schottky barrier height and “determines the source/drain series resistance of the transistor,” *Tung* ¶0034, a POSITA would have desired using more than about 85% Ge in doped semiconductor layer 55 to minimize contact resistance. *See* Thompson ¶¶532-534; *supra* Section III.C. *Tung* expressly teaches that layer 55 may be “doped SiGe, or doped Ge.” *Tung* ¶0058, ¶0078.

Since a POSITA would have wanted to use such a large amount of Ge in doped semiconductor layer 55 to minimize contact resistance, he or she would have understood from basic principles of epitaxy that SiGe layer 51 should be graded from a Ge amount compatible with underlying fin 28 to an amount compatible with doped semiconductor layer 55. Thompson ¶¶539-540; *see also supra* Section III.B; EX1019 ¶0020, ¶0038, ¶0044, ¶¶0053-0058; EX1020

¶¶0004-0005, ¶0034, ¶¶0085-0094; EX1013 at Abstract, ¶¶0003-0008, ¶¶0030-0032, ¶0042, ¶0063; EX1045 ¶¶0022-0024; EX1022 ¶¶0059-0060.

Brask expressly discloses such a layer. Specifically, *Brask* discloses a $\text{Si}_x\text{Ge}_{1-x}$ semiconductor film 410 ($0 \leq x \leq 0.99$) on fins 330/370, which is highly analogous to *Tung*'s semiconductor material 51. *Brask* at 10:20-49, Figs. 4A, 4B; *see also* Thompson ¶¶535-538. According to *Brask*, this $\text{Si}_x\text{Ge}_{1-x}$ film may “be graded.” *Brask* at 10:20-29.

As Figures 4A and 4B illustrate below, *Brask* teaches the same basic FinFET as *Tung*. Thompson ¶¶536-537; *see also* EX1012 at 10, Fig. 18; EX1049 at 1-4, Figs. 1-2; EX1038 at 1, Figs. 7a-7b.

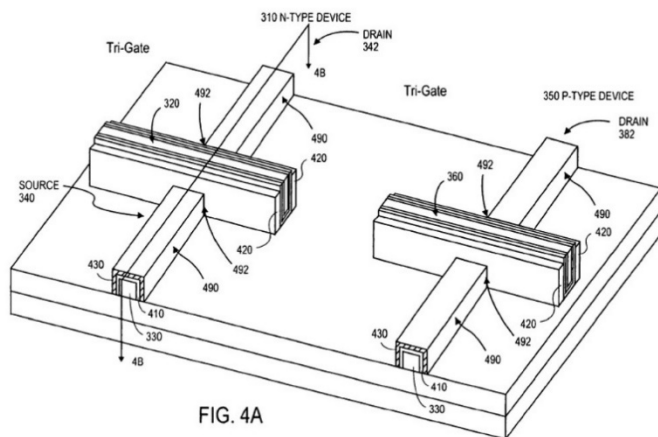


FIG. 4A

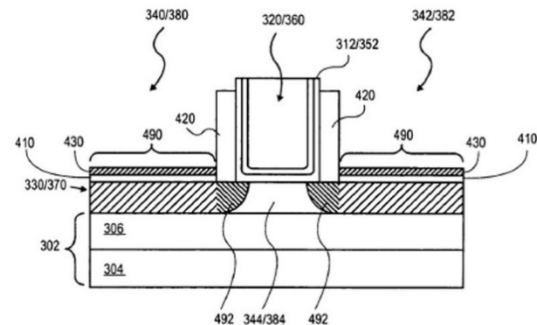


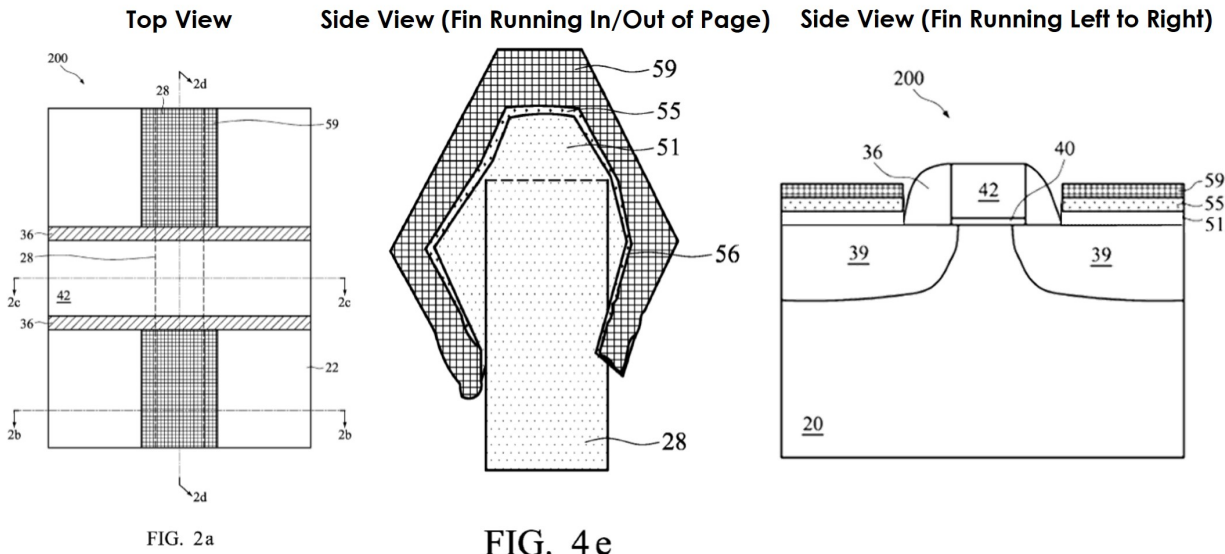
FIG. 4B

Like *Tung*'s fin 28, *Brask*'s FinFET has a silicon fin 330/370. *Tung* ¶¶0048-0052, Figs. 5-6b; *Brask* at 5:30-34, 12:51-56, 15:21-34, Figs. 4A-4B, 5E-5F. Both have source/drain extensions. *Tung* ¶0057, ¶0073, Figs. 2d, 11c; *Brask* at 9:61-10:11, 11:15-31, Fig. 4B. Both have raised SiGe source/drain regions

(*Tung*'s semiconductor material 51 and *Brask*'s semiconductor film 410). *Tung* ¶¶0039-0041, ¶¶0074-0078, Figs. 2a-2d, 4a-4c, 8, 11a-11c, 13-14; *Brask* at 10:20-49, Figs. 4A-4B. And both include a metal-semiconductor contact layer (*Tung*'s layer 59 and *Brask*'s layer 430). *Tung* ¶¶0042-0045, ¶¶0059-0065, ¶¶0079-0081, Figs. 2a-2d, 4d, 4e, 9a-11c, 15-16; *Brask* at 10:50-64, Figs. 4A-4B.

Since their FinFETs are highly analogous, a POSITA would have looked to *Brask*'s teachings to better understand how *Tung*'s SiGe semiconductor layer 51 may be structured. And since *Tung*'s SiGe semiconductor layer 51 corresponds to *Brask*'s semiconductor film 410, a POSITA would have understood its Ge concentration may “be graded” in a range between 1 and 100%. *Brask* at 10:24-29; *see also* Thompson ¶¶537-538.

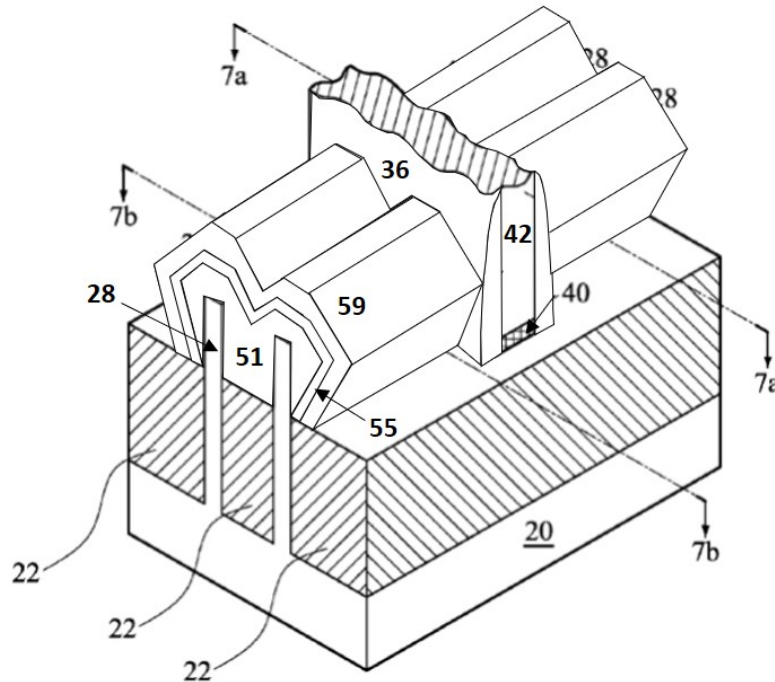
Tung's SiGe layer 51 sits between a fin region 28 with little or no Ge and semiconductor layer 55 with much more Ge. To avoid unwanted dislocations and preserve strain, a POSITA would have known to grade the Ge concentration of *Tung*'s SiGe layer 51 from an amount compatible with the underlying fin region to an amount compatible with the overlying semiconductor layer. Thompson ¶539. This approach and its benefits were already well-known. *Id.* ¶546; *see also supra* Section III.B; EX1019 ¶¶0020, ¶¶0038, ¶¶0044, ¶¶0053-0058; EX1020 ¶¶0004-0005, ¶¶0034, ¶¶0085-0094; EX1013 at Abstract, ¶¶0003-0008, ¶¶0030-0032, ¶¶0042, ¶¶0063; EX1045 ¶¶0022-0024; EX1022 ¶¶0059-0060.



Tung-Brask Combination

Applying these considerations, a POSITA would have found it obvious to create the structure above. Thompson ¶¶541-542. The left figure (Fig. 2a) shows *Tung*'s device from above. The middle figure (Fig. 4e) shows a side view along the fin (cross-section "2b" in Fig. 2a). And the right figure (Fig. 2d, modified to show SiGe layer 51¹⁰) shows a side view with the fin running left-to-right (cross-section "2d" in Fig. 2a). In an orthographic view, it would resemble the structure below (although the fins might not merge, *see Tung* ¶¶0058, ¶¶0078). Thompson ¶543.

¹⁰ See *Tung* ¶¶0033, ¶¶0074, Fig. 4e.



b. Rationales for applying *Brask's* teachings to *Tung's* FinFET

First, a POSITA would have understood the combination above combines known elements (*Brask's* graded Ge concentration in raised SiGe source/drain regions and *Tung's* raised source/drain regions) according to known methods (graded SiGe epitaxy) to yield predictable results (low-defect SiGe source/drain regions, a highly strained channel, and low contact resistance). Thompson, ¶546.

Second, a POSITA would have understood the combination above uses a known technique (graded SiGe epitaxy) to improve similar devices (*Tung's* and *Brask's* FinFETs, which include equivalent raised SiGe source/drain regions) in the same way (by minimizing crystal defects, enhancing channel strain, and ensuring low contact resistance). Thompson ¶547.

Third, a POSITA would have understood the combinations above apply a known technique (graded SiGe epitaxy) to a known device ready for improvement (*Tung*'s FinFET) to yield predictable results (low-defect SiGe source/drain regions, a highly strained channel, and low contact resistance). Thompson ¶548.

Fourth, a POSITA would have arrived at the combinations above due to a teaching, suggestion, or motivation in the prior art (those in *Tung* and *Brask* and those discussed in Section III, including the desire for a high Ge concentration) to arrive at the claimed invention. Thompson ¶549; *see also Ranade* ¶¶0038-0040; *Brask* at 10:29-49; *supra* Sections III.B, III.C.

c. A POSITA would have found it obvious to apply *Yu*'s source/drain contacts to *Tung*'s FinFET (including when implemented according to *Brask*)

A POSITA would have found it obvious to implement the *Tung-Brask* combination described in Section VIII.B.1.a-b with source/drain contact structures as taught by *Yu*.

Tung and *Brask* focus on the transistor structure itself, not the source/drain contacts required to operate the transistor. *Tung* simply notes that “[c]ontacts (not shown) are subsequently formed.” *Tung* ¶0064; *see also id.* ¶0023. Omitting source/drain contacts when describing a transistor structure is common in the literature. Thompson ¶¶552-553; *see also Tung* ¶0023, ¶0036, ¶0064; *Brask* at 27:20-27. Because a POSITA would have understood source/drain contacts must

be added for the *Tung-Brask* FinFET to operate, he or she would have added them to TiSiGe layer 59. *Tung* ¶0005, ¶0064; Thompson ¶554.

Yu describes source/drain contacts for FinFETs like the ones *Tung* and *Brask* describe. See *Yu* at Title, ¶¶0001-0005, ¶¶0018-0043, Figs. 5-10B; Thompson ¶555. Like the *Tung* and *Brask* FinFETs, *Yu*'s FinFET has a fin 201 capped with a Ti-based metal-semiconductor compound 605 in source/drain regions 603. See *Yu* ¶¶0021, ¶¶0028-0031, Figs. 5-7. *Yu* describes how to form source/drain contacts to such fins by referring to Figures 8, 9A, and 9B below.

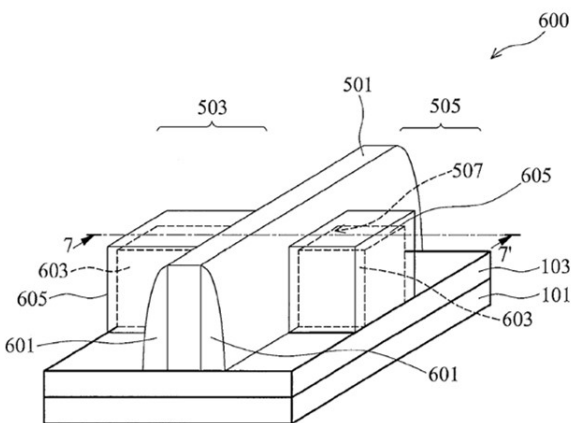


FIG. 6

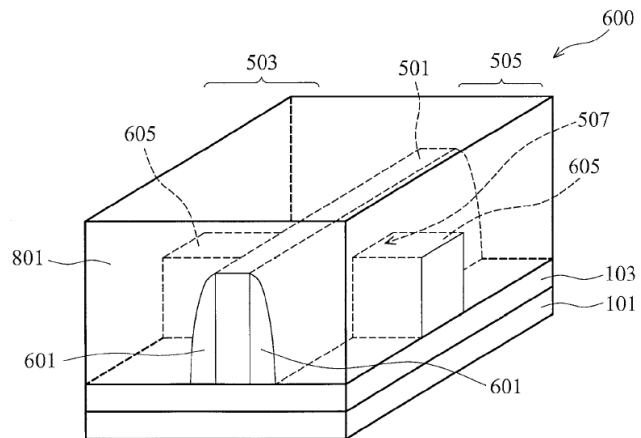


FIG. 8

After forming inter-layer dielectric (“ILD”) 801 over the FinFET, source/drain contact plugs 901 are deposited in an opening through ILD 801. *Yu* ¶¶0034-0039. Contact plugs 901 are “in contact with at least three surfaces of the fin 201,” which “allows for a larger area of contact between the silicide contacts 605 and the contact 901 than contacts that only contact the top surface of the fin

201.” *Id.* ¶0037. Using this approach, “the contact resistance of the device may be reduced,” and “variations in the contact resistances due to mis-alignments of the contacts 901” are reduced “since there is more leeway for variation when the width of the contacts 901 are larger than the width of the fin 201.” *Id.*; see also Thompson ¶557.

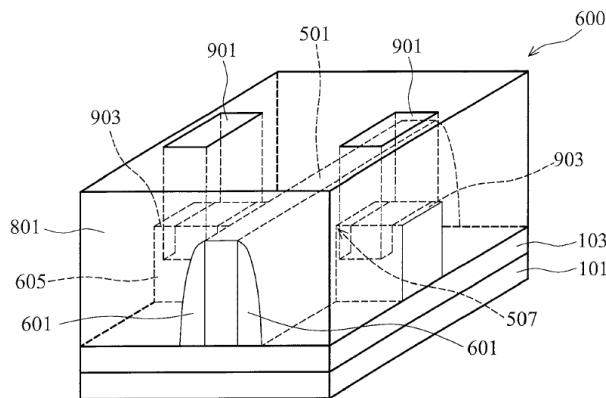


FIG. 9A

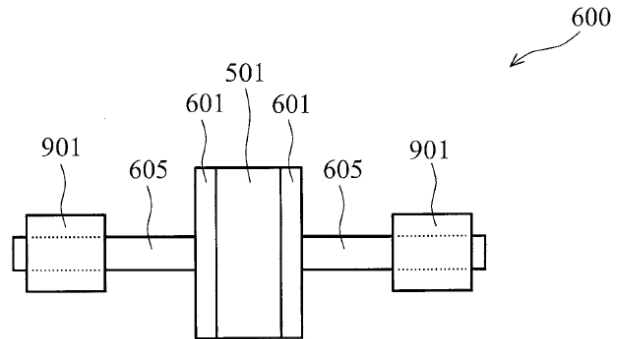
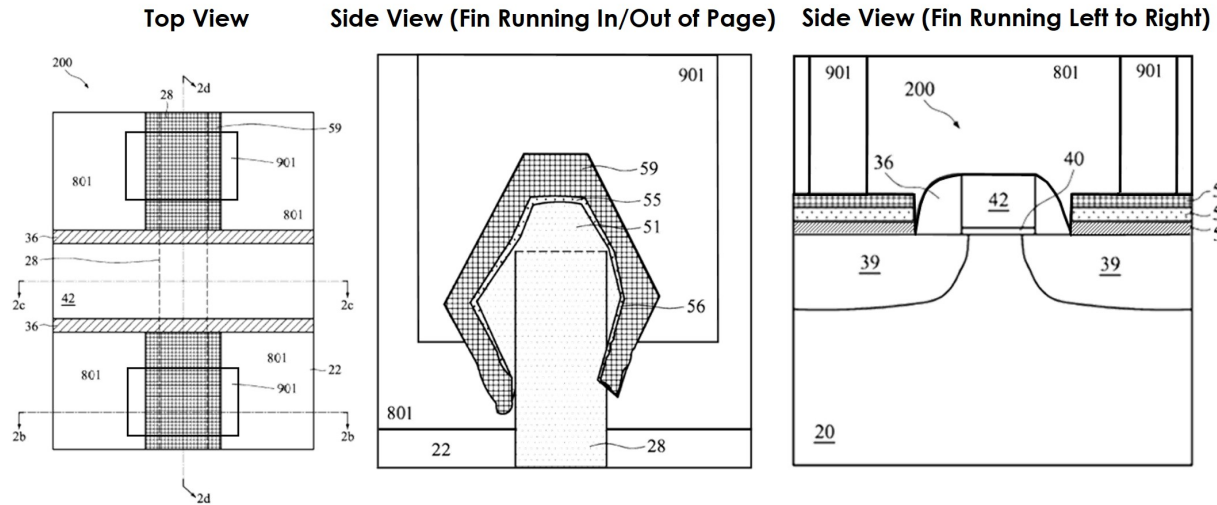


FIG. 9B

Because *Yu* describes source/drain contacts to reduce contact resistance and minimize variations due to misalignment in devices like the *Tung* and *Brask* FinFETs, and because the *Tung* and *Brask* FinFETs need such source/drain contacts to operate effectively, a POSITA would have found it obvious to apply *Yu*'s contacts to the *Tung-Brask* FinFET as illustrated below. Thompson ¶¶559-560.



The figure on the left (modeled on *Tung*'s Fig. 2a) shows an approximate a plan-view cross-section of the *Tung-Brask-Yu* device, with the fin running up/down and the gate running left/right. The middle figure (modeled on *Tung*'s Fig. 4e) shows an approximate side view looking along the fin direction (i.e., cross-section that cuts the fin laterally denoted "2b" in the left-hand figure). And the figure on the right (modeled on *Tung*'s Fig. 2d) shows an approximate side view with the fin running in the left/right direction (i.e., cross-section that cuts the fin longitudinally denoted "2d" in the left-hand figure). Thompson ¶560.

d. Rationales for applying *Yu*'s teachings to the *Tung-Brask* FinFET

First, a POSITA would have understood the combinations above combine known elements (*Yu*'s source/drain contacts and FinFETs like those in *Tung* and *Brask*) according to known methods (photolithography and deposition techniques

for making contacts) to yield predictable results (a FinFET with low contact resistance and improved tolerance for misalignment). Thompson, ¶562.

Second, a POSITA would have understood the combinations above use known techniques (photolithography and deposition techniques for making contacts) to improve similar devices (*Tung*'s, *Brask*'s, and *Yu*'s FinFETs) in the same way (ensuring low-resistance contacts and improved tolerance for misalignment). Thompson, ¶563.

Third, a POSITA would have understood the combinations above apply known techniques (photolithography and deposition techniques for making contacts) to a known device ready for improvement (*Tung*'s FinFET, including as modified by *Brask*) to yield predictable results (low contact resistance and improved tolerance for misalignment). Thompson ¶564.

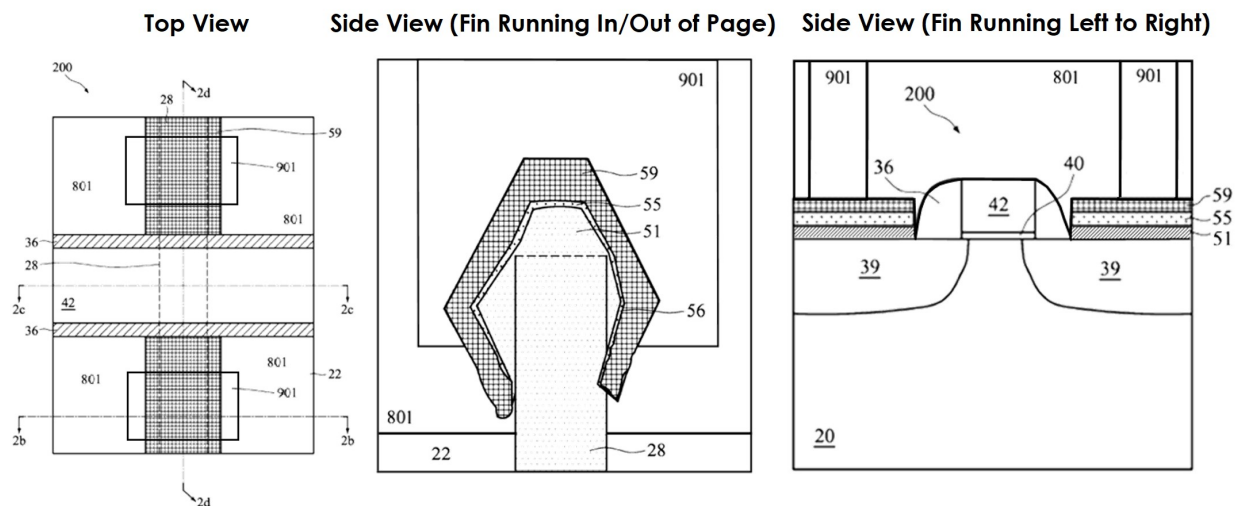
Fourth, a POSITA would have arrived at the combinations above due to a teaching, suggestion, or motivation in the prior art (those in *Tung*, *Brask*, and *Yu* and those discussed in Section III, including the need for low-resistance source/drain contacts) to arrive at the claimed invention. Thompson ¶565; *see also Tung* ¶¶0005-0006, ¶0027, ¶0032, ¶0034, ¶0042, ¶0064, ¶0078; *Brask* at 27:20-27; *Yu* at Abstract, ¶¶0004-0005, ¶0010, ¶¶0034-0040; *supra* Section III.C.

2. Claim 1

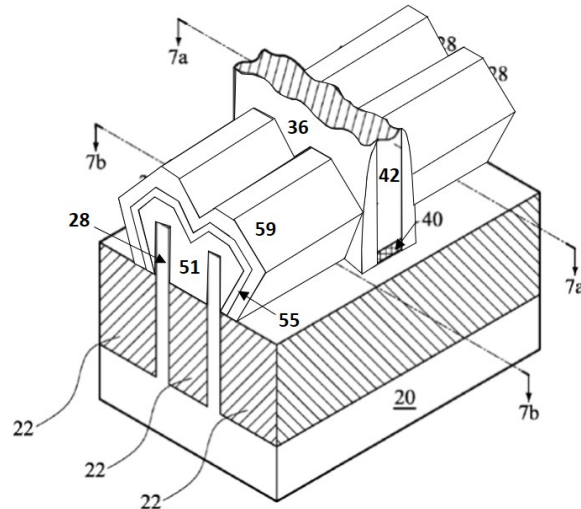
Because a POSITA would have wanted to combine *Tung*'s, *Brask*'s, and *Yu*'s teachings, because a POSITA would have reasonably expected to succeed, and because the *Tung-Brask-Yu* combination meets all elements of claim 1, claim 1 is unpatentable. *See* Thompson ¶¶623.

a. Element [1.0]

To the extent the preamble is limiting, the *Tung-Brask-Yu* combination provides “[a]n integrated circuit structure.” *Tung* describes FinFET “[s]emiconductor devices [that] comprise integrated circuits.” *Tung* ¶0003. As Section VIII.B.1 explains, a POSITA would have found it obvious to apply *Brask*'s and *Yu*'s teachings to *Tung*'s FinFET (below), which is an integrated circuit structure. Thompson ¶¶575-578.



***Tung-Brask-Yu* Combination**



***Tung-Brask-Yu* Combination (Before Application of *Yu*)**

b. Element [1.1]

The *Tung-Brask-Yu* combination includes “a fin comprising silicon.” The claimed fin (green below) comprises fin 28 (e.g., Si), semiconductor material 51 (graded SiGe), and doped semiconductor layer 55 (e.g., >85% Ge or even pure Ge). *Tung* ¶¶0048-0051, ¶0058, ¶0074, ¶0078; *see also* Thompson ¶¶76-80, ¶¶533-534, ¶540, ¶580; *supra* Section III.C. Because each constituent portion of the fin includes silicon, the fin comprises silicon. Thompson ¶¶580-581.

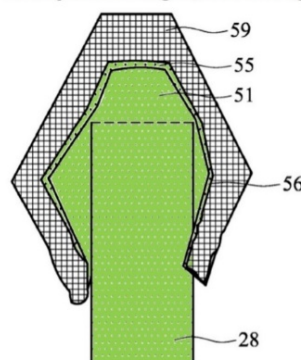
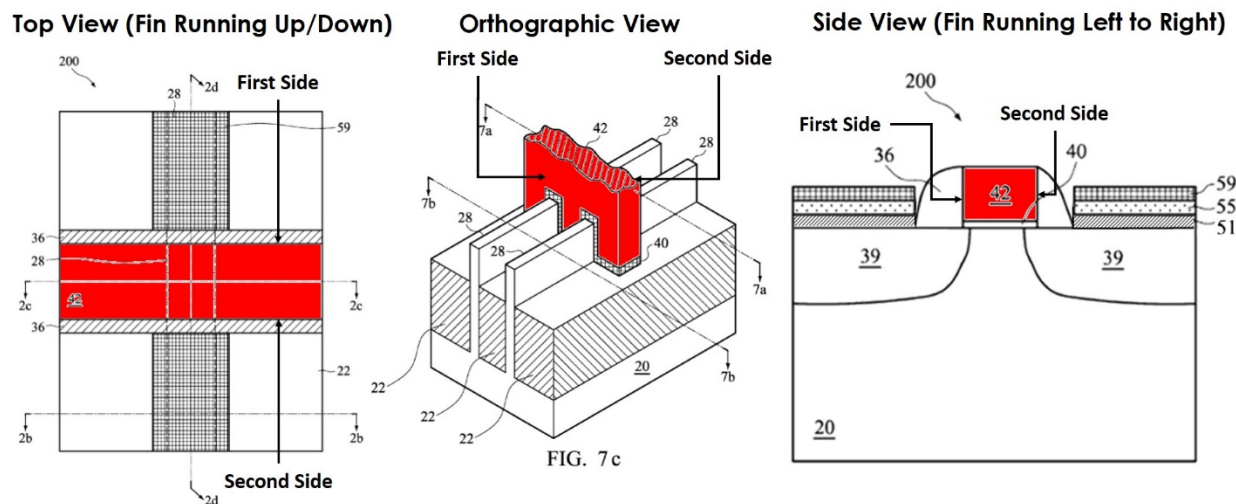


FIG. 4e

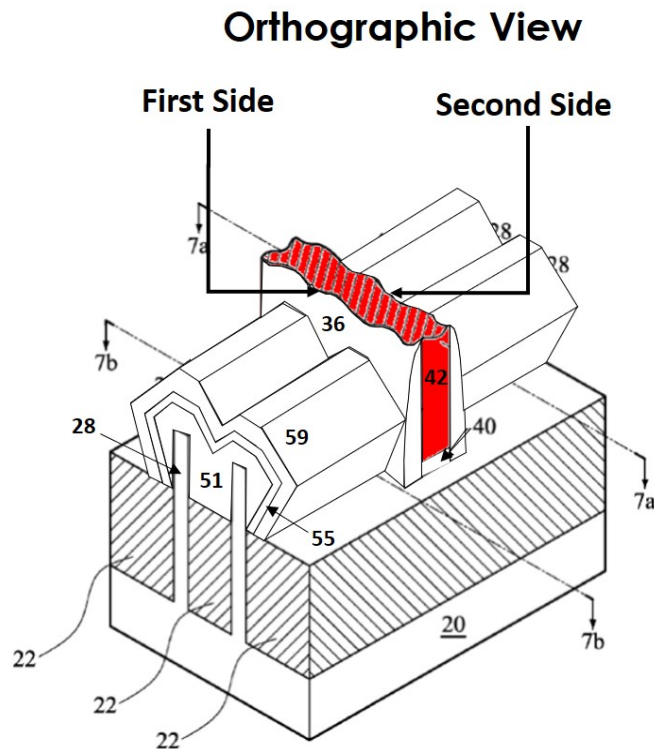
c. Element [1.2]

The *Tung-Brask-Yu* combination includes “a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side.” As the images below show, “[a] gate electrode 42 [red] is disposed over the fin 28.” *Tung* ¶0023; *see also id.* ¶0033, ¶¶0053-0055, Figs. 2a, 2d, 7a, 7c, 11c; Thompson ¶¶583-585.



***Tung* Implemented According to *Brask* (*Yu*'s Additions Not Shown)**

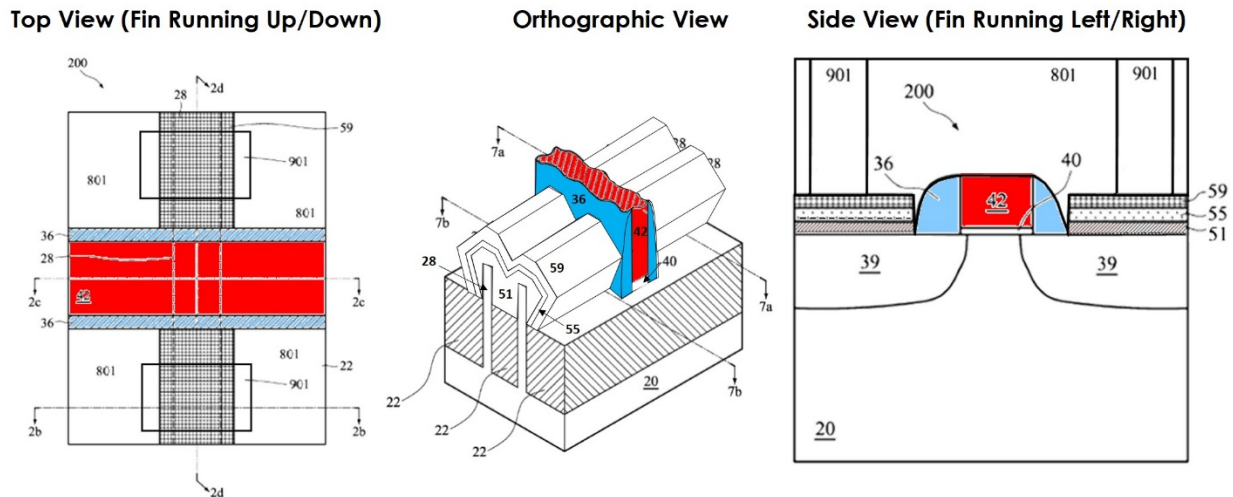
The figure in the middle above represents the *Tung-Brask* combination as it would appear earlier in manufacturing than in the other two figures. The equivalent image at the later stage of processing would resemble the structure below (although the fins might not merge, *see Tung* ¶0058, ¶0078). Thompson ¶584.



Gate electrode 42 (red) lies over the fin and has a first side (nearest one of the source/drain regions) and a second side (nearest the other source/drain region) opposite the first side. Thompson ¶586.

d. Elements [1.3] and [1.6]

The *Tung-Brask-Yu* combination includes “a [first/second] dielectric spacer along the [first/second] side of the gate electrode.” As the figures below illustrate, the FinFET includes typical dielectric gate spacers 36 “formed on the sidewalls of the gate dielectric 40 and the gate electrode 42” to isolate gate electrode 42 from other conductive regions. *Tung* ¶0055; *see also id.* ¶0023, ¶0065, ¶0070, Figs. 2a, 2d, 11c; Thompson ¶¶588-589. As shown below, dielectric gate spacers 36 (blue) lie along the first and second sides of gate electrode 42 (red).



Tung Implemented According to *Brask* and *Yu*

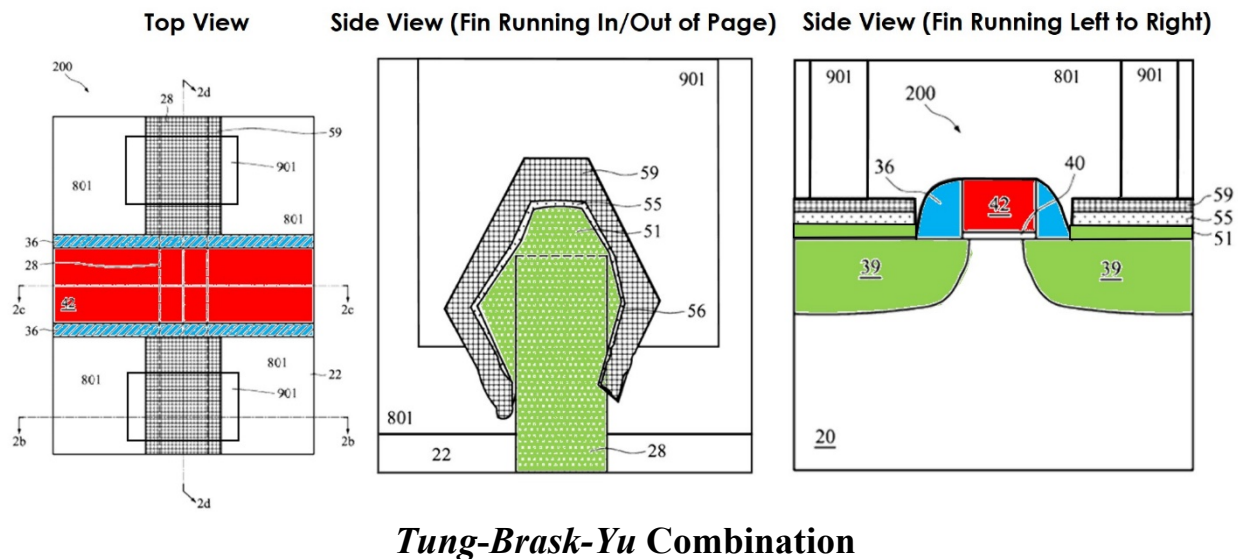
e. Elements [1.4] and [1.7]

The *Tung-Brask-Yu* combination includes “a [first/second] source or drain region in the fin proximate a [first/second] side of the gate electrode, a portion of the [first/second] source or drain region beneath the [first/second] dielectric spacer.”

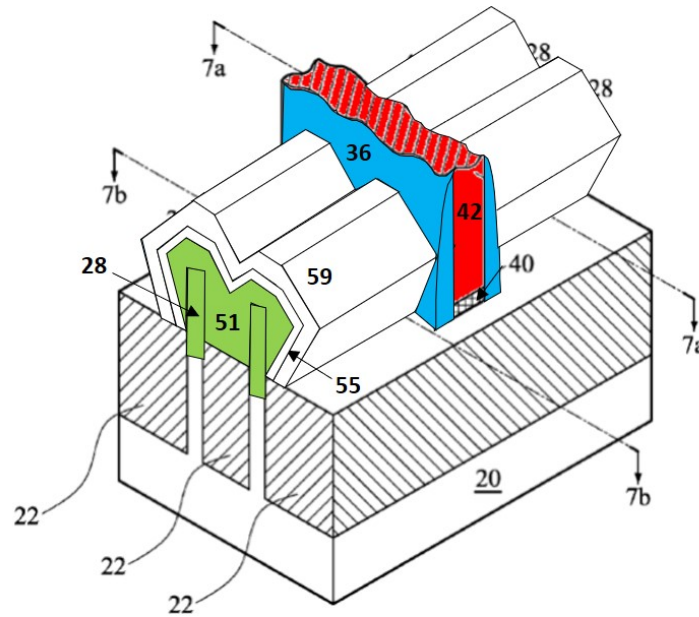
Each “source or drain region” in the *Tung-Brask-Yu* combination has at least two components. First, *Tung* teaches “source/drain regions 39 ... disposed within the *fin*s 28.” *Tung* ¶0033. This includes source/drain extension regions (not identified by number but extending under gate spacers 36).¹¹ *Id.* ¶0057, ¶0073. Second, *Tung* teaches *semiconductor material 51* is a “raised source/drain” region of “source/drain regions 39.” *Id.* ¶0074; see also *id.* ¶0033, ¶0072, ¶0075. The

¹¹ See *supra* note 8.

figures below illustrate the claimed source/drain regions (green),¹² each proximate to one side of the gate electrode (red). Thompson ¶¶592-593; *see also Tung* ¶0033, ¶0074, Figs. 2a, 2d, 7c, 11c. As shown on the right, a portion of each source/drain region (e.g., a source/drain tip extension) lies beneath the dielectric spacer (blue) on its respective side of the gate electrode (red). Thompson, ¶593; *see also Tung* ¶0033, ¶0057, ¶0073, ¶0078.



¹² Optionally, *doped semiconductor layer 55* may be considered a third part of each claimed “source or drain region.” Thompson ¶593 & n.628; *Tung* ¶0033.



Tung-Brask-Yu Combination (Before Applying Yu)

f. Elements [1.5] and [1.8]

In the *Tung-Brask-Yu* combination, “the [first/second] source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%.” As Figures 4e and 11a illustrate, “semiconductor material 51 forms the source/drain regions 39 (raised source/drain)” and “is formed of a material different from that of substrate 20, for example, silicon germanium (SiGe).” *Tung* ¶0074; *see also id.* ¶0033, ¶0040, ¶¶0057-0058, ¶¶0074-0078, Figs. 4b-4e, 11a, 13-16.

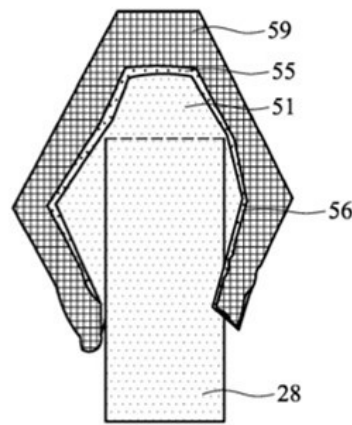


FIG. 4e

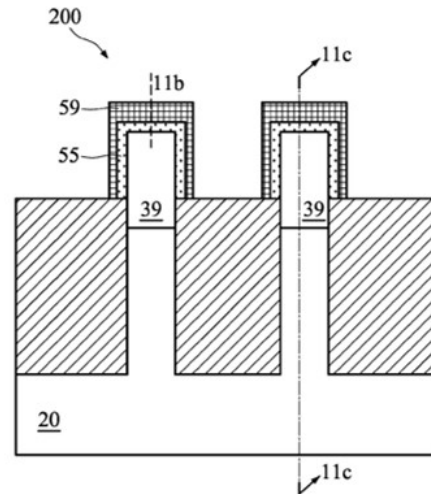


FIG. 11a

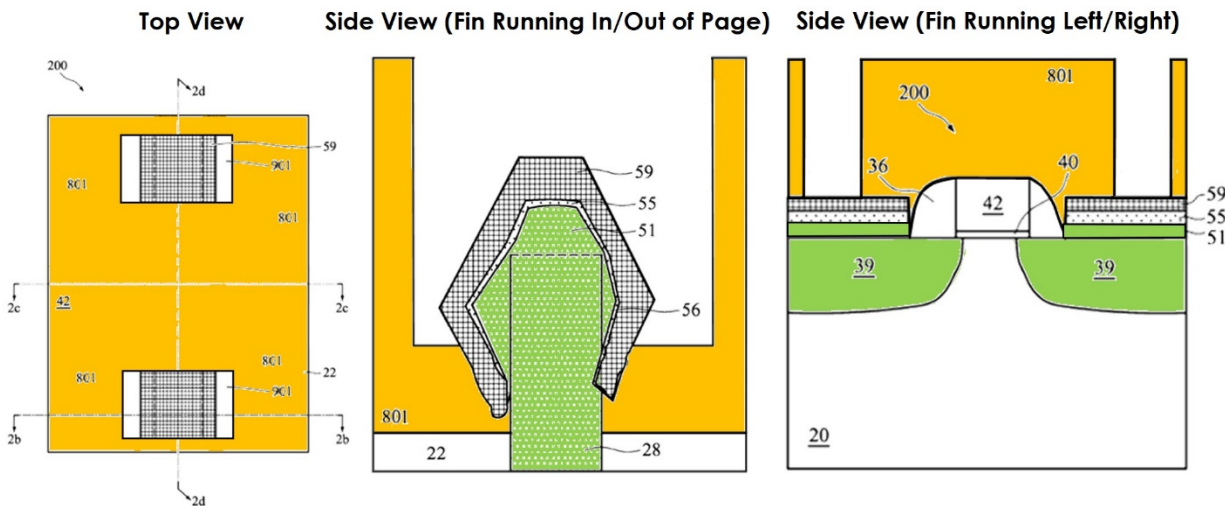
When implemented in the *Tung-Brask-Yu* combination, the Ge concentration of SiGe semiconductor material 51 is graded in excess of 50%. As Section VIII.B.1.a explains, a POSITA would have found it obvious from basic strain engineering principles and *Brask* (because *Brask*'s SiGe raised source/drain layer 410 corresponds to *Tung*'s SiGe raised source/drain layer 51 and can be graded over a range between 1 and 100% Ge) to grade the Ge concentration of *Tung*'s semiconductor material 51 from a level compatible with the underlying fin 28 to a level compatible with the overlying doped semiconductor layer 55 (e.g., >85% Ge), thereby exceeding 50%. Thompson ¶¶596-599; *see also Tung* ¶0058, ¶0078; *Brask* at 10:20-29; EX1020 ¶0042, ¶¶0085-0092; *supra* Section III.B.

Additionally, there is a presumption of obviousness since *Brask*'s disclosed range of 1 to 100% Ge encompasses the claimed range of >50% Ge. *See DuPont*, 904 F.3d at 1006. As Section VIII.A.2.f explains, these ranges differ only in

degree, not in kind, and the claimed range does not yield new or unexpected results. Thompson ¶¶295-299; *see also Genentech*, 946 F.3d at 1341.

g. Element [1.9]

The *Tung-Brask-Yu* combination includes “a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region.” As the images below show, the FinFET includes *Yu*’s interlayer dielectric (ILD) 801 (orange) over the source/drain regions (green) with openings exposing part of each source/drain region. Thompson ¶¶604-608; *see also Tung* ¶0064; *Yu* ¶¶0034-0036, Figs. 8-9B.



***Tung-Brask-Yu* Combination**

h. Elements [1.10] and [1.11]

The *Tung-Brask-Yu* combination includes “a [first/second] germanide layer in the [first/second] opening and over the portion of the [first/second] source or drain region, the [first/second] germanide layer comprising silicon, germanium and titanium.”

Tung’s “doped semiconductor layer 55 comprises ... doped SiGe, or doped Ge.” *Tung* ¶¶0058, ¶¶0078. As Section III.C explains, a POSITA would have found it obvious to use such a layer with >85% Ge to minimize contact resistance. Thompson ¶¶76-80, ¶¶533-534, ¶¶540, ¶¶580. *Tung* further explains “metal 57 comprises a suitable metal,” such as “Ti,” and “is deposited over the doped semiconductor layer 55.” *Tung* ¶¶0042, ¶¶0060-0061, ¶¶0080. During annealing, the metal atoms in layer 57 react with the semiconductor atoms in doped semiconductor layer 55 (and atoms diffused from semiconductor material 51 when layer 55 is thin enough). *Id.* ¶¶0041-0045, ¶¶0063-0065, ¶¶0081; *see also* Thompson ¶¶611; EX1050 at 4-6, Fig. 1; EX1051 at 2-3, Fig. 5. Thus, a TiSiGe layer 59 forms. Thompson ¶¶611. TiSiGe layer 59 is a “germanide layer,”¹³ and it comprises Ge, Si, and Ti. *Id.* ¶¶613-616.

¹³ Although *Tung* calls layer 59 a metal “silicide” layer, “silicide” is being used generically. *See* Thompson ¶¶612. A POSITA would not have understood the metal-semiconductor compound that results when metalizing a doped Ge semiconductor

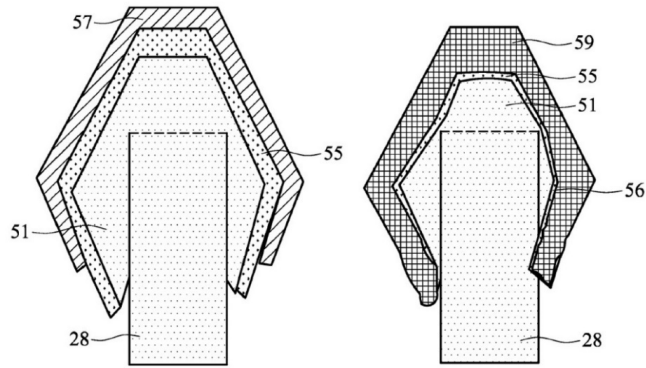
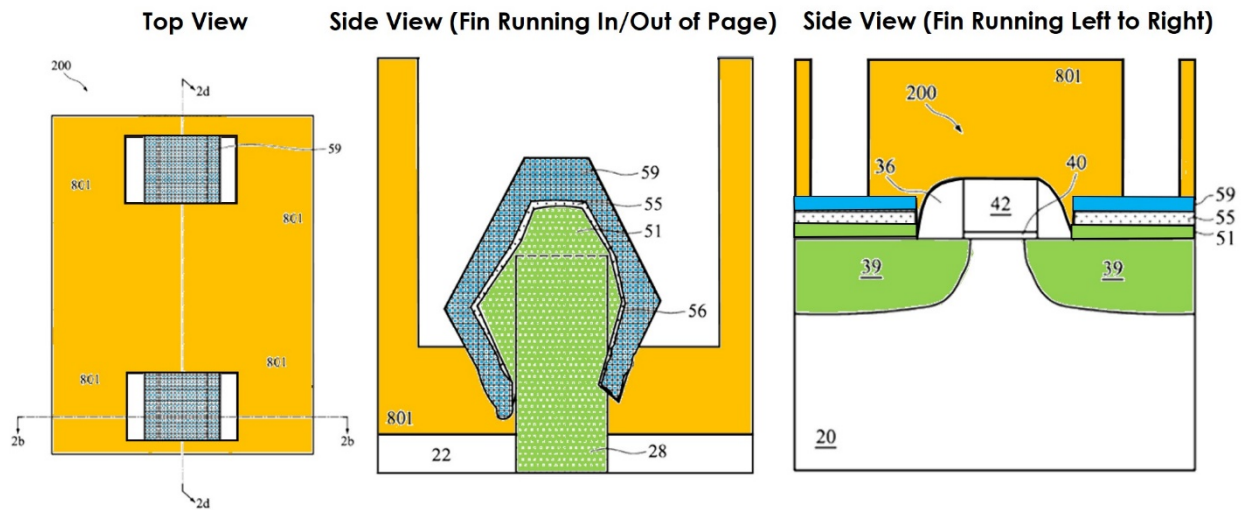


FIG. 4d

FIG. 4e

The annotated figures below confirm this TiSiGe germanide layer (blue) lies in the openings of the ILD layer 801 (orange) and over the exposed portions of the source/drain regions (green). Thompson ¶¶613-615.

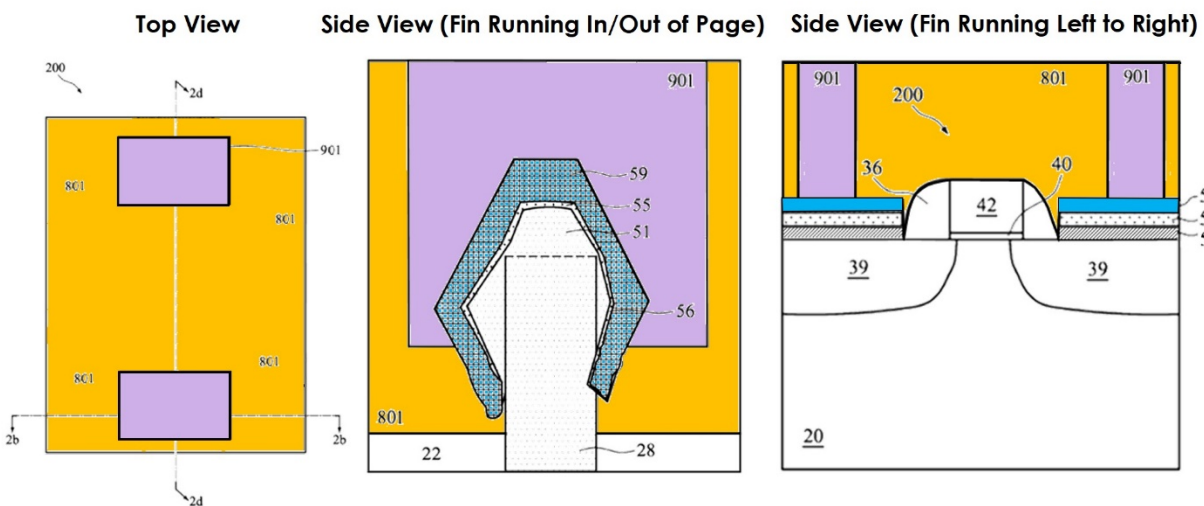


Tung-Brask-Yu Combination

layer 55, *see Tung* ¶0058, ¶0078, to be a “silicide” in a strict sense. *See Thompson* ¶¶125-126, ¶612.

i. Elements [1.12] and [1.13]

The *Tung-Brask-Yu* combination includes “a [first/second] contact plug in the [first/second] opening and on the first germanide layer.” As the images below show, the FinFET includes contact plugs 901 (purple) formed in the openings of the interlayer dielectric 801 (orange) and on the germanide layers 59 (blue). Thompson ¶¶619-621; *see also Tung* ¶0064; *Yu*, ¶¶0034-0040, Figs. 8-9B.



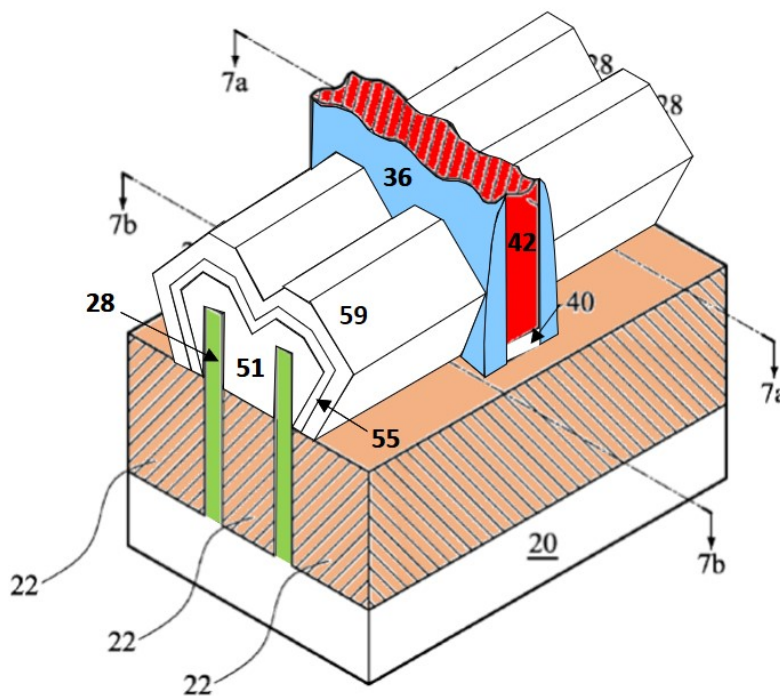
***Tung-Brask-Yu* Combination**

3. Claim 5

The *Tung-Brask-Yu* combination includes “an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region.” As shown below, the *Tung-Brask-Yu* FinFET includes isolation regions 22 (peach) through which the fin portion 28 (green) protrudes and over which portions of gate electrode 42 (red) and gate

spacers 36 (blue) lie. Thompson ¶¶626-627; *see also Tung* ¶¶0023-0024, ¶0051, Figs. 2b, 2c, 5-9a, 10, 11a, 13-16. Fin portion 28 (green) extends “above a top surface of the isolation regions 22” (peach) by “between about 20 nm and about 100 nm.” *Tung* ¶0051; *see also id.* at Fig. 6b. Additionally, *Tung*’s Figure 7c (modified below to add features 36, 51, 55, and 59) confirms that gate electrode 42 (red) lies atop isolation regions 22 (peach). *See id.* ¶0053. Gate spacers 36 (blue) are later formed over the structure. *Id.* ¶0065, ¶0073, Figs. 2d, 7c, 11c.

Orthographic View

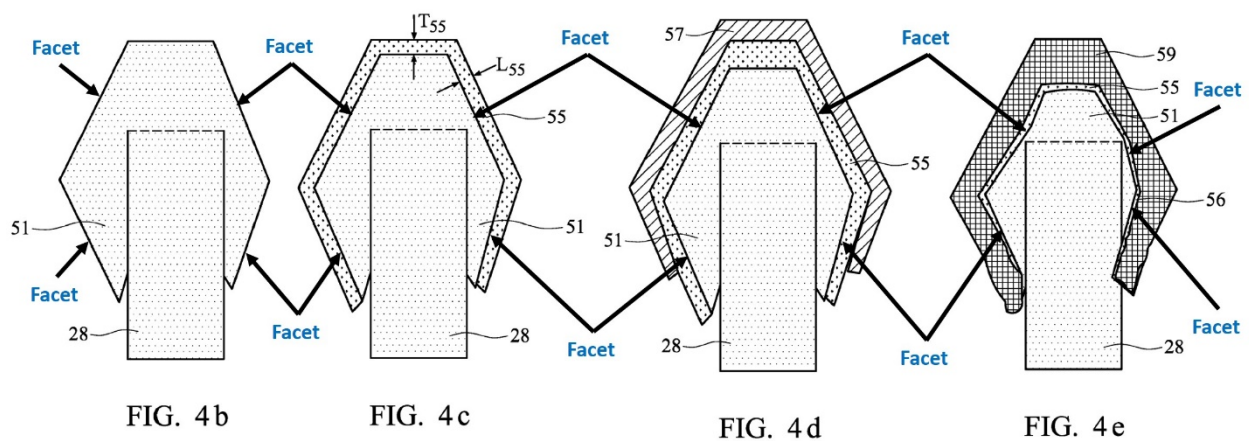


Tung-Brask-Yu Combination (Before Applying Yu)

5. Claim 7

In the *Tung-Brask-Yu* combination, “the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets.” A POSITA would have understood that a “facet” refers to a semiconductor crystal surface. Thompson ¶635. Since semiconductor material 51 (SiGe) is epitaxial, it is, by definition, crystalline and terminated by facets. *Id.* ¶637; *see also Tung* ¶¶0040-0041, ¶¶0057-0058, ¶¶0074-0075, ¶0078.

Tung also makes clear that semiconductor material 51 (SiGe) grows “at different rates on different crystal planes” and that the fin “form[s] facets” with a diamond shape as in Figures 4b-4e below. *Tung* ¶0040, ¶0078; *see also* Thompson ¶637. Semiconductor material 51 is shown below with four facets along (111) crystal planes.¹⁴ *Id.* ¶0040; *see also* Thompson ¶637; *supra* Section III.D.



¹⁴ A POSITA would have known grading the Ge concentration in this layer, as *Brask* instructs, would not change this. Thompson ¶637.

6. Claim 8

Claim 8 is identical to claim 1, except limitations [8.1], [8.2], [8.4], and [8.7] recite a “body” instead of a “fin.” The ’281 Patent uses the term “body” only once, equating it with a “fin.” ’281 Patent at 13:35-38; *see also* Thompson ¶¶640 & n.677; *Brask* at 5:26-30, 18:3-16, Figs. 3, 5I. Thus, a POSITA would have understood there is no meaningful difference between claims 1 and 8, and the asserted *Tung-Brask-Yu* combination satisfies claim 8 for the reasons in Sections VIII.B.2.a-i. Thompson ¶¶639-653; *see also Mycogen*, 243 F.3d at 1329 (Fed. Cir. 2001).

7. Claims 12-20

The *Tung-Brask-Yu* combination satisfies claims 12-20 for the reasons in Section VIII.C *infra*.

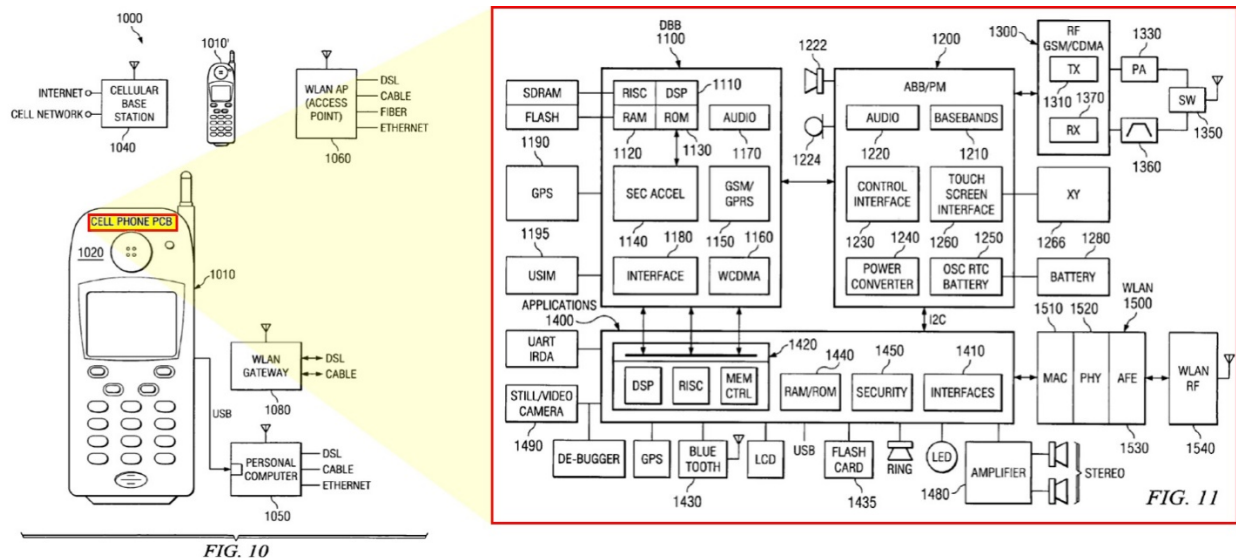
C. Claims 12-20: The *Ranade-Kim* and *Tung-Brask-Yu* Combinations, Alone (Grounds 1A and 2A) or Further in View of *Liu* (Grounds 1B and 2B)

It was beyond question that FinFETs would go into computing devices. *See* Thompson ¶¶369, 433, 656, 720. Computing devices that use integrated circuits made of FETs (their primary application) were known long before December 2010. *Id.* Although the section below discusses disclosures in *Liu* that demonstrate why claims 12-20 would have been obvious, a POSITA would have understood simply from his or her knowledge of the electronics industry that a typical computer or

smartphone had the additional features recited in those claims. A POSITA would have found claims 12-20 obvious even without recourse to *Liu*. *See id.*

1. A POSITA Would Have Found It Obvious to Deploy the *Ranade-Kim* and *Tung-Brask-Yu* FinFETs in Systems Like the Ones *Liu* Describes

Liu confirms that FETs, including FinFETs, “are widely used in the electronics industry.” *Liu* at 1:47-50; *see also id.* at 32:22-40, Fig. 8. A POSITA would have known they are fundamental building blocks of integrated circuits, which, after packaging, become “chips” that are added to other circuit elements on a circuit board for use in devices like smartphones. Thompson ¶¶369, ¶¶656; *see also id.* ¶¶434-436; *Liu* at 1:29-61, 5:27-6:9, 6:55-56, 32:22-40, 33:11-37:59. *Liu*’s Figures 10 and 11 below illustrate such a system. *Liu* at 33:10-37:40, Figs. 10-11.



***Liu* Fig. 10**

Liu Fig. 11

A POSITA would have found it obvious to incorporate the *Ranade-Kim* and *Tung-Brask-Yu* FinFETs in such a system because it would have involved

(1) combining prior art elements (FETs) according to known methods (semiconductor fabrication) to yield predictable results (a computing device); (2) using known a technique (using FinFETs) to improve similar devices (computing devices) in the same way; (3) applying a known technique (using FinFETs) to a known device (a computing device) ready for improvement to yield predictable results; and/or (4) applying *Liu*'s teachings, suggestions, and motivations to arrive at the claimed application of the FinFET structures discussed in Sections VIII.A and VIII.B. Thompson ¶¶232-238, ¶¶567-573.

2. Claim 12

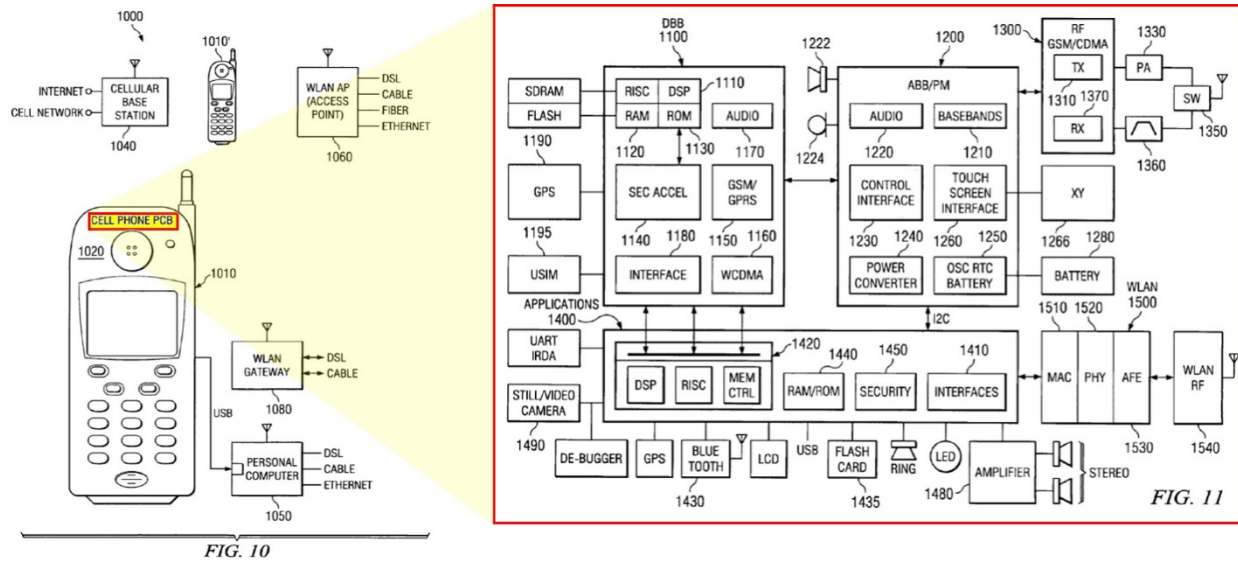
a. Element [12.0]

To the extent the preamble is limiting, the *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, provide for “[a] computing device.” A POSITA would have understood FinFETs are intended almost exclusively for such applications. Thompson ¶369, ¶656. *Liu* further discloses a “wireless handset” that uses FinFET-based integrated circuits. *Liu* at 32:23-40, 33:11-37:59, Figs. 8, 10-11; *see also* Thompson ¶¶445-446, ¶¶729-730.

b. Element [12.1]

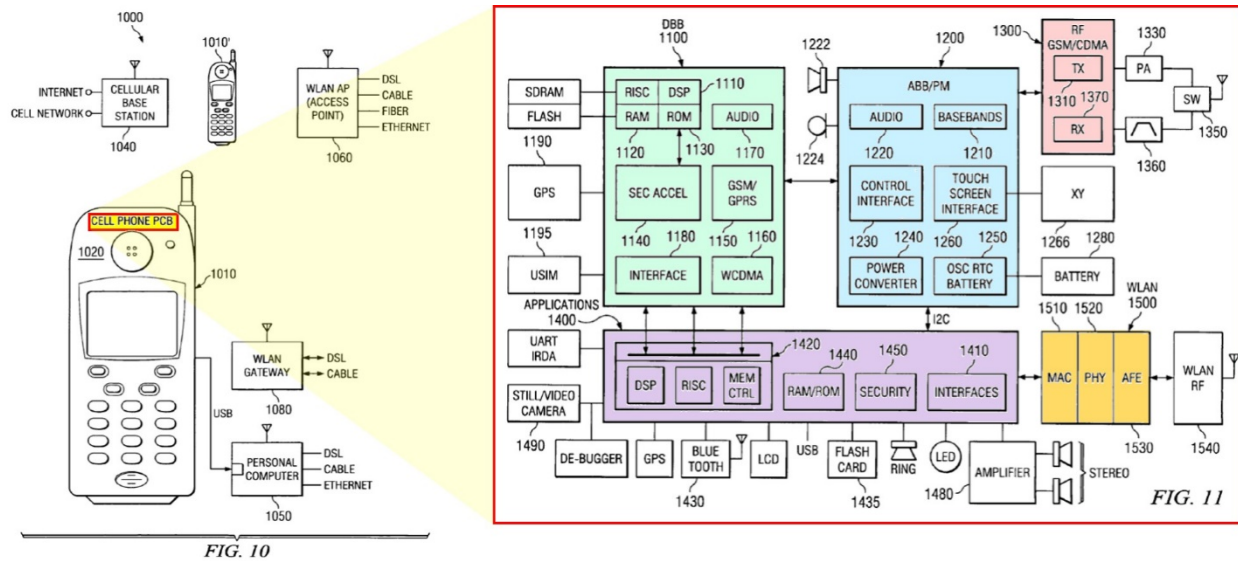
The *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, provide for “[a] board.” A POSITA would have understood FinFETs are intended almost exclusively for such applications. Thompson ¶373, ¶660. *Liu* further

discloses a “cell phone printed circuit board” (red) in a “wireless handset.” *Liu*, 33:46-34:2, Figs. 10-11; *see also* Thompson ¶450, ¶734.



c. Element [12.2]

The *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, provide for “a component coupled to the board, the component including an integrated circuit structure.” A POSITA would have understood FinFETs are intended almost exclusively for such applications. Thompson ¶377, ¶664. *Liu* further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. *Liu*’s PCB includes FinFET-based integrated circuits, such as digital baseband chip 1100 (green), analog baseband chip 1200 (blue), GSM chip 1300 (red), applications processor chip 1400 (purple), and WLAN chip 1500 (orange). *Id.* at 6:48-51, 32:23-40, 34:23-30, 35:14-20, 35:64-67, 36:15-16, 37:14-17, Figs. 8, 10-11; *see also* Thompson ¶454, ¶738.



d. Elements [12.3] through [12.15]

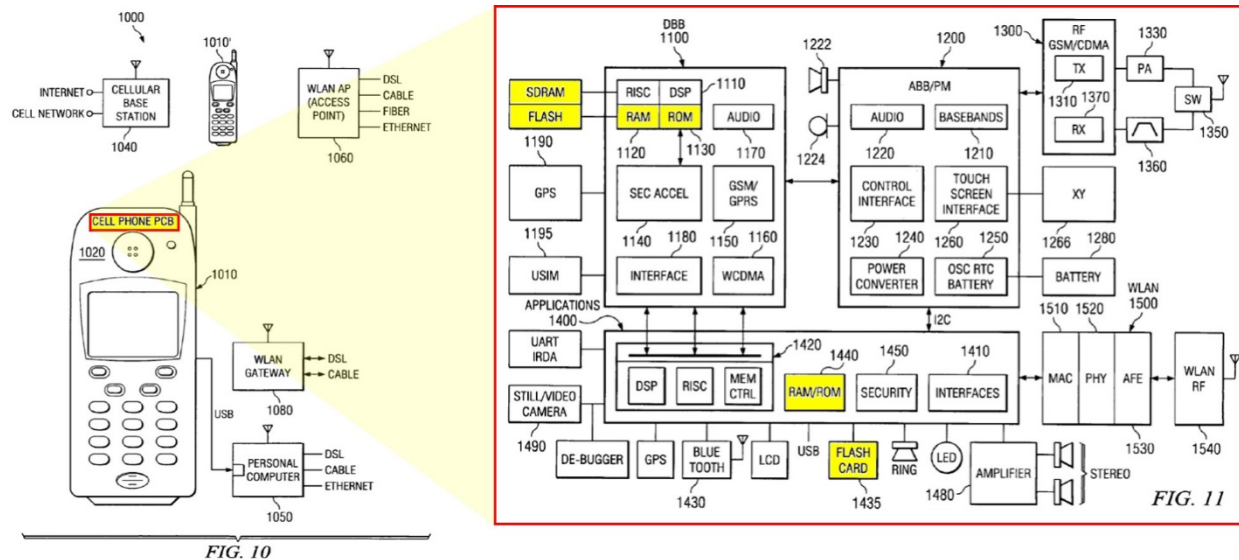
The *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, satisfy elements [12.3] through [12.15] for the reasons in Sections VIII.A.2.a-i and VIII.B.2.a-i. See Thompson ¶¶379-392, ¶¶456-469, ¶¶666-679, ¶¶740-753.

3. Claim 13

The *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, provide for “a memory coupled to the board.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed to going into chips that go on circuit boards and exchange information with a memory. Thompson ¶¶395-396, ¶¶682-683.

Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. Coupled to the PCB are various memories (yellow below), including off-chip Flash and SDRAM and memory elements 1120,

1130, 1435, and 1440. *Id.* at 34:28-33, 36:24-33, Figs. 10-11; *see also* Thompson ¶¶472-473, ¶¶756-757.



4. Claim 14

The *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, provide for “a communication chip coupled to the board.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits, including communication chips, that go onto circuit boards in smartphones and computers. Thompson ¶¶400-401, ¶¶687-688.

Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. Coupled to the PCB are various communication chips (circled in red; relevant functional blocks highlighted in

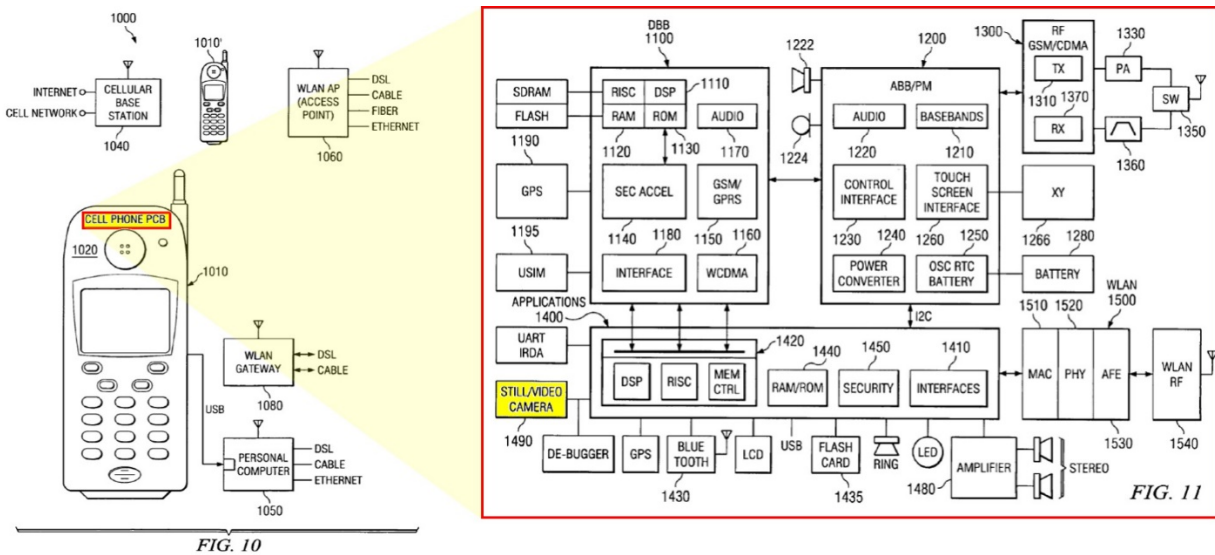
¶¶478-479, ¶¶762-763.



5. Claim 15

¶¶692-693.

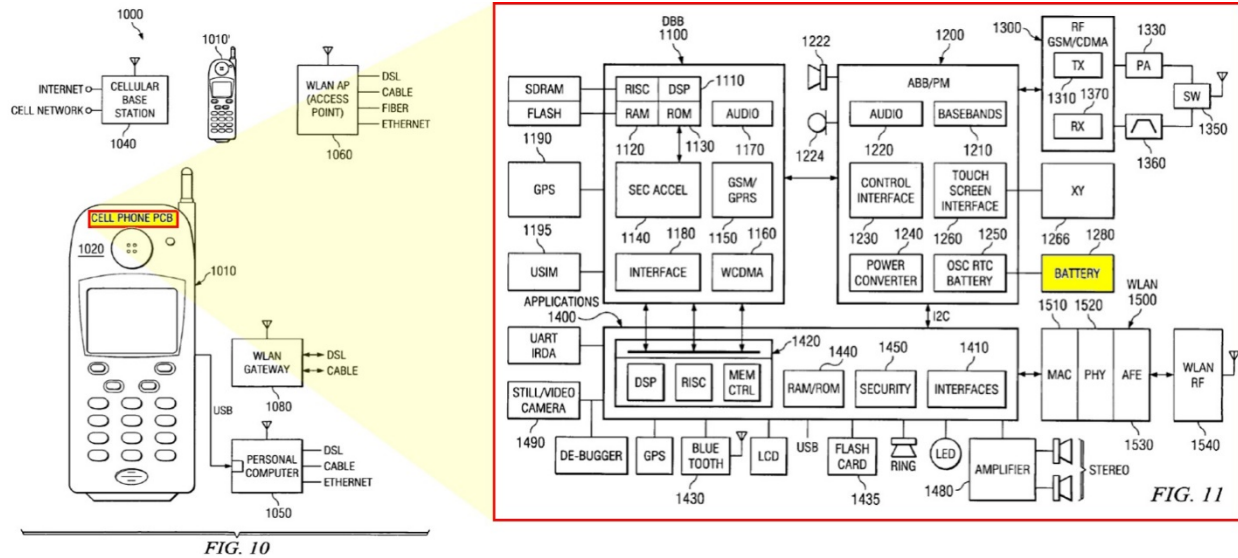
(yellow). *Id.* at 36:60-65, Figs. 10-11; *see also* Thompson ¶¶484-485, ¶¶768-769.



6. Claim 16

The *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, provide for “a battery coupled to the board.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a battery. Thompson ¶¶410-411, ¶¶697-698.

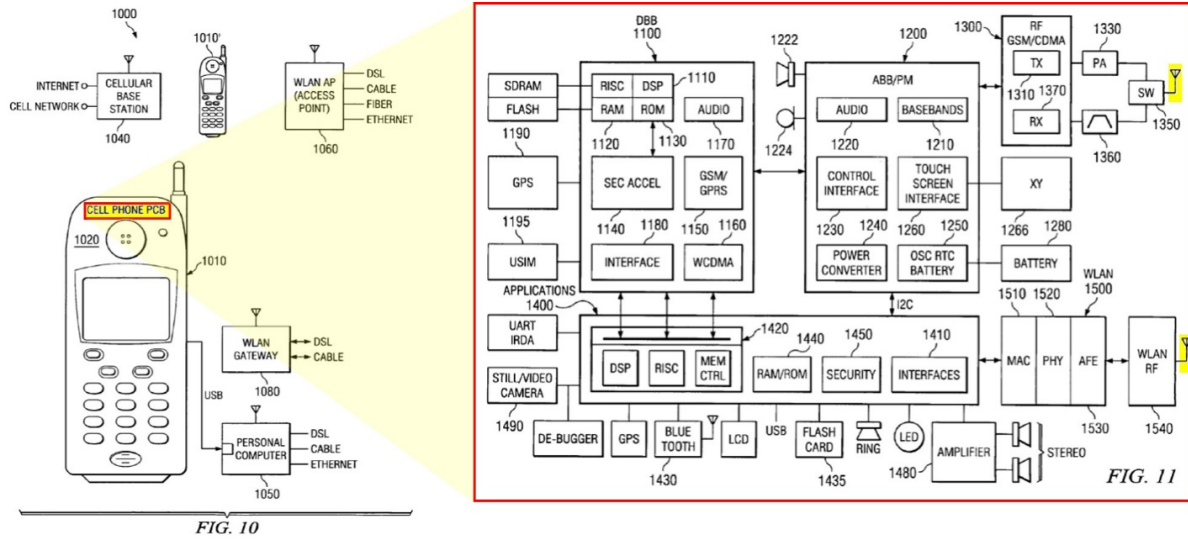
Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. Coupled to the PCB is a battery 1280 (yellow). *Id.* at 35:54-63, Figs. 10-11; *see also* Thompson ¶¶490-491, ¶¶774-775.



7. Claim 17

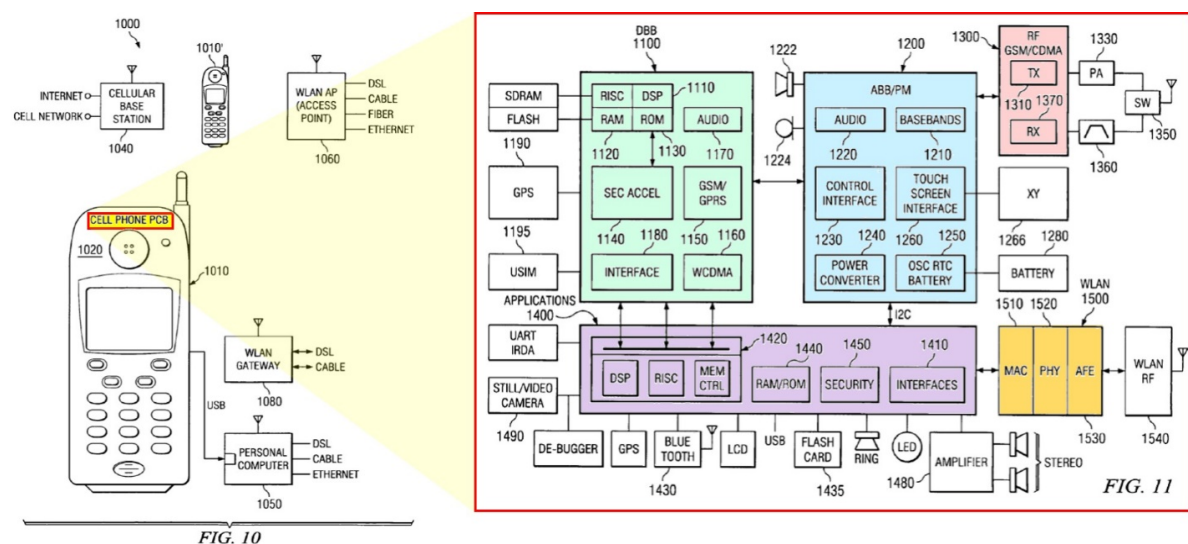
The *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, provide for “an antenna coupled to the board.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to an antenna. Thompson ¶¶415-416, ¶¶702-703.

Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. Coupled to the PCB are a wireless antenna and WLAN antenna (yellow). *Id.* at 36:4-7, 37:26-27; *see also id.* at 5:62-65, Figs. 10-11; Thompson ¶¶496-497, ¶¶780-781.



8. Claim 18

The *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, provides that “the component is a packaged integrated circuit die.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits that go onto circuit boards as packaged integrated circuit dies. Thompson ¶¶420-421, ¶¶707-708.



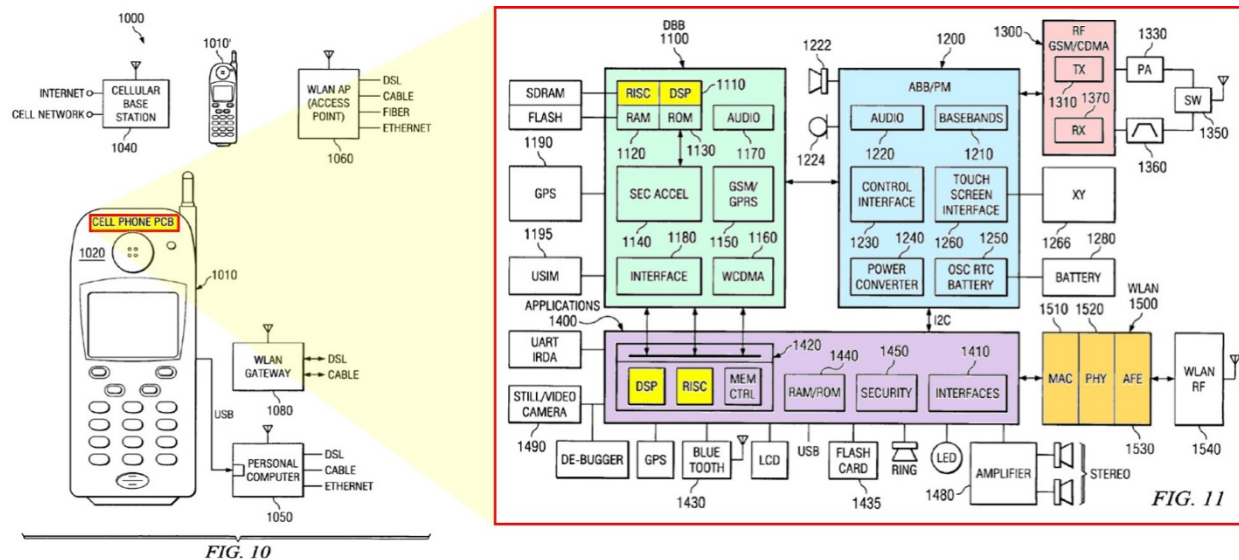
Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. As shown above, the PCB includes FinFET-based integrated circuits 1100 (green), 1200 (blue), 1300 (red), 1400 (purple), and 1500 (orange). *Id.* at 6:48-51, 32:23-40, 34:23-30, 35:14-20, 35:64-67, 36:15-16, 37:14-17, Figs. 8, 10-11; Thompson ¶¶502-503, ¶¶786-787. A POSITA would have understood these are packaged dies (chips/chiplets) because unpackaged integrated circuits are used only for testing or to be packaged. Thompson ¶504, ¶788.

9. Claim 19

The *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, provide that “the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.” A POSITA, applying common knowledge about the electronics industry, would have understood such FinFETs are designed for use in integrated circuits (including processors, communications chips, and digital signal processors (DSPs)) that go onto circuit boards of smartphones, computers, and the like. Thompson ¶¶425-426, ¶¶712-713.

Liu further discloses a “cell phone printed circuit board (PCB)” in a “wireless handset.” *Liu* at 33:46-34:2. As shown below, coupled to the PCB are communication chips 1100 (green), 1200 (blue), 1300 (red), 1400 (purple), and

1500 (orange). *Id.* at 34:33-42, 35:14-20, 35:64-36:36, 37:14-36, Figs. 10, 11; Thompson ¶¶509-510, ¶¶793-794.



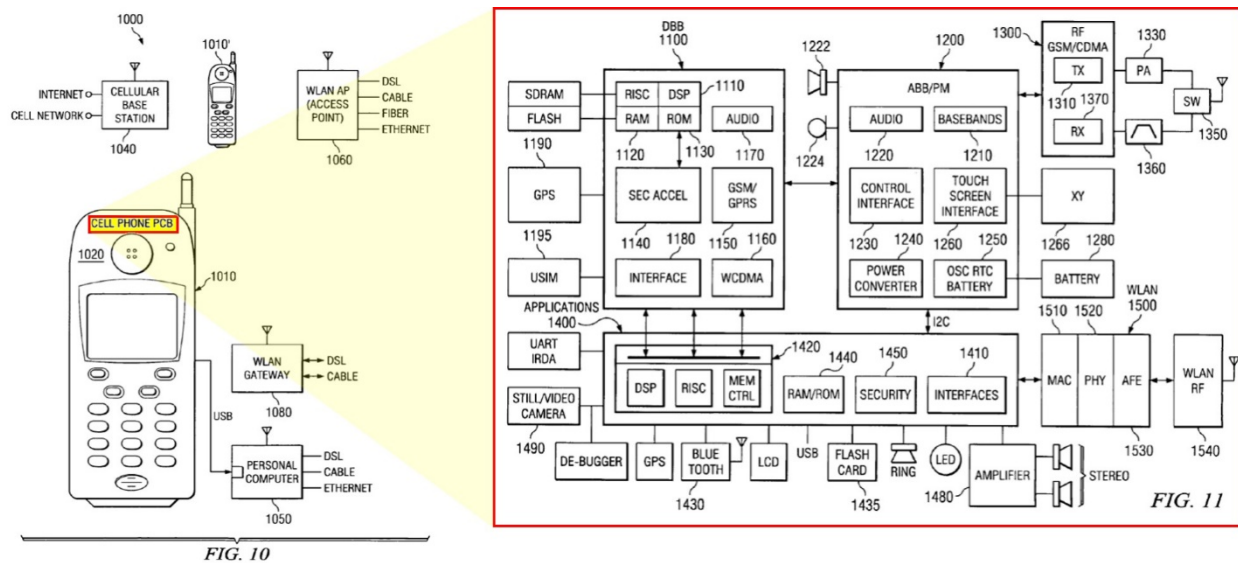
Additionally, highlighted in yellow, the component may be “a RISC processor (such as MIPS core, ARM processor, or other suitable processor)” or “a digital signal processor (DSP).” *Liu* at 34:23-30, 36:18-31; *see also* Thompson ¶511, ¶795.

10. Claim 20

The *Ranade-Kim* and *Tung-Brask-Yu* combinations, alone or in view of *Liu*, provide that “the computing device is selected from the group consisting of a mobile phone, a laptop, a desktop computer, a server, and a set-top box.” A POSITA, applying common knowledge about the electronics industry, would have

understood such FinFETs are designed for use in integrated circuits that go onto the circuit boards of such devices. Thompson ¶¶430-431, ¶¶717-718.

Liu further discloses FinFETs for use in a “cell phone printed circuit board (PCB)” in a “wireless handset,” as shown below. *Liu* at 33:46-34:2; *see also id.* at 6:48-51, 32:23-40, Figs. 8, 10-11; Thompson ¶¶516-517, ¶¶800-801. *Liu* also describes using such components in other computing devices like “radios and televisions, fixed and portable entertainment units, routers, pagers, personal digital assistants (PDA), organizers, scanners, faxes, copiers, household appliances, [and] office appliances.” *Liu* at 34:3-22; *see also* Thompson ¶518, ¶802.



IX. TRIAL SHOULD BE INSTITUTED

Because no substantive action has occurred in the related district court proceeding, which remains stayed, all *Fintiv* factors weigh against discretionary

denial under §314(a). *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, at 5-6 (P.T.A.B. Mar. 20, 2020). “The PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding.” EX1057 at 6.

Likewise, there is no reason to deny institution under §314(a) based on Samsung’s IPR2023-00653. It is stayed pending voluntary dismissal. Patent Owner has not filed a preliminary response, nor has the Board taken any substantive action. All *General Plastics* factors weigh against denial. *See General Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357 *et seq.*, Paper 19, at 8-10 (P.T.A.B. Sept. 6, 2017).

Finally, there is no reason to deny institution under §325(d). Neither the art nor the arguments in this Petition are the same or substantially the same as previously presented to the Office. *See Advanced Bionics, LLC. v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, at 7-9 (P.T.A.B. Feb. 13, 2020). Although *Kim* is cited by the ’281 Patent, it was not discussed during prosecution or considered in combination with the asserted references in this Petition. Although Samsung’s IPR2023-00653 relies on *Tung*, the Board has not considered the merits of those arguments, nor are they the same or substantially the same in this Petition.

X. MANDATORY NOTICES**A. Real Party-in-Interest**

The real parties-in-interest are Taiwan Semiconductor Manufacturing Company Ltd. and TSMC North America.

B. Related Matters

The '281 Patent is, or has been, involved in the following:

Name	Number	Court	Filed
Semiconductor Devices, Mobile Devices Containing the Same, and Components Thereof	Inv. No. 337-TA-1336	ITC	9/12/2022
Daedalus Prime LLC v. Samsung Electronics Co., Ltd.	2:22-cv-00352	EDTX	9/12/2022
Taiwan Semiconductor Mfg. Co. Ltd. v. Daedalus Prime LLC et al.	1:22-cv-01647	DDE	12/30/2022
Samsung Electronics Co., Ltd. v. Daedalus Prime LLC	IPR2023-00653	PTAB	3/6/2023

C. Lead and Back-Up Counsel, and Service Information

Lead Counsel	Back-Up Counsel
J. Preston Long (Reg.# 65,125) jp.long@finnegan.com FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, LLP 901 New York Ave. N.W. Washington, DC 20001 Tel: (202) 408-4347	Grace K. Mills (Reg.# 66,946) gracie.mills@finnegan.com FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, LLP 901 New York Ave. N.W. Washington, DC 20001 Tel: (202) 408-4389

Back-Up Counsel	Back-Up Counsel
Clement J. Naples (Reg.# 50,663) clement.naples@lw.com LATHAM & WATKINS LLP 1271 6th Ave. New York, NY 10020 Tel: (859) 899-8739	Thomas W. Yeh (<i>pro hac vice</i> to be filed) thomas.yeh@lw.com LATHAM & WATKINS LLP 355 South Grand Ave. Suite 100 Los Angeles, CA 90071 Tel: (213) 891-8763

D. Lead and Back-Up Counsel, and Service Information

Petitioner consents to service by e-mail at the following addresses:

- jp.long@finnegan.com;
- gracie.mills@finnegan.com;
- clement.naples@lw.com;
- thomas.yeh@lw.com;
- DaedalusPrimeIPRs@finnegan.com.

XI. PAYMENT OF FEES

The Office may charge additional fees to Deposit Account No. 06-0916.

XII. TIME FOR FILING PETITION

This Petition is being filed more than nine months after the '281 Patent was granted, *see* 37 C.F.R. §42.102(a)(1), and within one year of Petitioner being served with a complaint alleging infringement, *see* 37 C.F.R. §42.101(b).

XIII. GROUNDS FOR STANDING

Under 37 C.F.R. §42.104(a), Petitioner certifies the '281 Patent is available for *inter partes* review and Petitioner is not barred or estopped from requesting such review on any grounds identified in this Petition.

XIV. CERTIFICATION UNDER 37 C.F.R. §42.24(d)

As calculated by the “Word Count” feature of Microsoft Word for Microsoft 365, this Petition contains 13,299 words, excluding this Certification and the following: Table of Contents, Table of Authorities, List of Exhibits, Claim Listing, Mandatory Notices Under 37 C.F.R. §42.8, and Certificate of Service.

XV. CONCLUSION

For the reasons above, claims 1, 5-8, and 12-20 are unpatentable. Trial should be instituted and the challenged claims cancelled.

Dated: June 22, 2023

Respectfully submitted,

/ J. Preston Long, Reg.# 65,125 /

J. Preston Long, Ph.D.
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, LLP
901 New York Ave. N.W.
Washington, DC 20001
Tel: (202) 408-4347

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), **Petition for *Inter Partes* Review, Petitioner's Power of Attorney, and the associated Exhibits 1001-1062** were served via FedEx on June 22, 2023, on the correspondence address of record below indicated in the Patent Office's public PAIR system for U.S. Patent No. 11,251,281.

Ian MacKinnon, Esq.
Kinney & Lange, P.A.
312 South Third Street
Minneapolis, MN 55415
Telephone: (612) 337-7208

Courtesy copies have been concurrently served on litigation counsel at:

Michael T. Renaud
MINTZ, LEVIN, COHN, FERRIS,
GLOVSKY AND POPEO
One Financial Center, Suite 100
Boston, Massachusetts 02111
(617) 542-6000

Dated: June 22, 2023

By: /Lauren K. Young/
Lauren K. Young
Litigation Legal Assistant
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.