UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner

v.

Daedalus Prime LLC,

Patent Owner

Patent No. 11,251,281 B2
Filing Date: May 22, 2020
Issue Date: February 15, 2022

Title: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Inter Partes Review No. IPR2023-01121

DECLARATION OF DR. SCOTT E. THOMPSON, PH.D., IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 11,251,281

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I, Dr. Scott E. Thompson, Ph.D., declare as follows:

I. Introduction

1. My name is Dr. Scott E. Thompson. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited (TSMC) in connection with a petition for *inter partes* review of U.S. Patent No. 11,251,281 ('281 Patent), which I have been told TSMC is submitting to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 1, 5-8, and 12-20 of the '281 Patent ("Challenged Claims").

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the bases for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the '281 Patent is unpatentable for at least the reasons I discuss below.

II. Background and Qualifications

A. Education and Career

5. I have over 30 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of transistors.

6. I received a Ph.D. degree in Electrical Engineering from the University of Florida in 1992. Before that, I received a Master of Science degree in 1988 and a Bachelor of Electrical Engineering with Highest Honors in 1987, both from the University of Florida.

7. I was employed at Intel Corporation ("Intel") from 1992 to 2004. During that time, I worked on evaluating, implementing, and ramping into high-volume production new materials, process architectures, and transistor structures. I was the yield manager and overall program manager for Intel's 90 nanometer (nm) process.

8. Of specific relevance to this case, I played a key role at Intel in the development of a form of strained silicon using silicon germanium ("SiGe") implemented in the source and drain regions of p-type field effect transistors ("pFETs") that I refer to as "SiGe/Strained Silicon" technology in this report. The

original SiGe/Strained Silicon technology concept was developed around the year 2000 (about a decade before the earliest claimed priority date for the ’281 Patent). SiGe/Strained Silicon is now a nearly universal technology that speeds up transistors and hence all types of integrated circuits. Modern integrated circuits use both nFETs (negative charge flows) and pFETs (positive charge flows). Before the development of SiGe/Strained Silicon, pFETs were about half the speed of nFETs. SiGe/Strained Silicon improved pFET speed to equal that of nFETs, which provides a large benefit to power and performance.

9. Through my work in the industry, I was aware of a report that TSMC had adopted a strained silicon technology in 2003.[1] By 2010, TSMC had added many inventions to the field of SiGe/Strained Silicon. Today, TSMC is the undisputed leader in producing integrated circuits, as even Intel’s current CEO has acknowledged.[2]

[1] *See* https://www.eetimes.com/tsmc-to-offer-strained-silicon-at-90-and-65-nm-nodes/.

[2] *See How Intel Plans to Catch Samsung and TSMC and Regain Its Dominance in the Chip Market*, CNBC (Nov. 6, 2021) (“‘We had some missteps,’ said Pat Gelsinger, who took over as Intel’s CEO in February 2021. . . . Gelsinger has an ambitious roadmap to catch and surpass . . . TSMC by 2025.”), *available at* https://www.cnbc.com/2021/11/06/how-intel-plans-to-catch-up-to-samsung-and-tsmc-with-44-billion-of-new-global-chip-fabs.html; *see also* Vested Finance, *The Empires that TSMC Built*, *available at* https://vestedfinance.com/in/blog/the-empires-that-tsmc-built/.

10. Working at Intel, I announced the SiGe/Strained Silicon technology to the industry in 2002.[3] I managed a team of about 100 engineers that developed and implemented the SiGe/Strained Silicon technology in planar pFETs that went into high-volume manufacturing in 2003 as part of Intel's 90 nm process. A "planar" transistor is fabricated on a flat surface. My team was responsible for fabricating, ramping into production, and transferring the SiGe/Strained Silicon technology to Intel's design and fabrication sites worldwide. The SiGe/Strained Silicon technology has been used by Intel for its entire microprocessor product line since the 90 nm process, including its latest 7th generation of SiGe/Strained Silicon. Within a few years after 2002, every advanced computer chip manufacturer was using SiGe/Strained Silicon technology.[4]

11. My work on the SiGe/Strained Silicon technology helped me earn an **I**nstitute of **E**lectrical and **E**lectronics **E**ngineers (IEEE) Fellow rank (awarded in 2006), along with numerous industry awards for our Intel development team. In 2008, I and key members of the Intel SiGe/Strained Silicon development team were awarded the SEMI AWARD NORTH AMERICA for "Process Integration of

[3] *See* EE Times, *Industry Reacts to Intel's Strained Silicon Move* (August 16, 2002), *available at* https://www.eetimes.com/industry-reacts-to-intels-strained-silicon-move/#.

[4] *See* EE Times, *Industry Reacts to Intel's Strained Silicon Move* (August 16, 2002), *available at* https://www.eetimes.com/industry-reacts-to-intels-strained-silicon-move/#.

Strain-enhanced Mobility Techniques for CMOS Transistors."[5] This award is the highest honor achievable through SEMI, a 2,000-member trade organization.

12. In 2007, my Intel colleague Mark Bohr described my role and how Intel came to invent the SiGe/Strained Silicon technology.[6] At Intel, I worked on several generations of Intel's planar transistors, each of which implemented SiGe/Strained Silicon technology after 2002.

13. I have given invited talks and organized and taught international courses on SiGe/Strained Silicon technology. For example, I was asked to give a lecture on strained silicon at the 2006 International Electron Devices Meeting.

14. I have also developed and taught graduate level courses on SiGe/Strained Silicon technology at the University of Florida, including a course entitled "EEE500: Future of Nano/Micro Electronics."

15. As a professor at the University of Florida, I have been awarded over $4 million in research funding largely directed towards understanding the scalability of SiGe/Strained Silicon transistors. I have received research funding

[5] *See* https://www.semi.org/en/semi-organization/awards/north-american-semi-award/recipients.

[6] *See* https://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.488.9606&rep=rep1&type=pdf. As explained by Mark, "By early 2002 [Scott Thompson] became the 90 nm program manager and was responsible for getting strained silicon transistors along with copper plus low-k interconnects to meet performance, yield and reliability requirements in time for the first product shipments in 2003."

from the National Science Foundation, Semiconductor Research Corporation, and other agencies. I currently have a research contract to investigate strain in bipolar transistors (a type of transistor based on a different principle of operation than planar FETs or FinFETs).

16. As a result of my industry work, I am familiar with various areas of advanced computer chip technology. I have worked extensively on the use of shallow trench isolation ("STI") in manufacturing processors, novel low resistance source and drain regions, silicides (titanium, cobalt, and nickel silicide), and low resistance tungsten plugs. Throughout 1991-2004, I was part of the Intel development team that introduced titanium, cobalt and nickel silicide into the production of high-performance microprocessors.[7] My work experience has also extended to layout design rules, oxide and nitride spacer formation, gate and fin patterning, gate oxides, gate electrodes, contacts, silicide, copper interconnects, process integration (lithography, etch, diffusion, thin film deposition, and chemical mechanical polishing), and yield and reliability.

[7] *See, e.g.*, S. Thompson, et al., *A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 µm^2 SRAM Cell*, Technical Digest of the 2002 International Electron Devices Meeting (IEDM), pp. 61-64 (2002); A. Brand et al., *Intel's 0.25 Micron, 2.0Volts Logic Process Technology*, Intel Technology Journal (Q3 1998).

17. In addition, I am familiar with FinFET technology and manufacturing techniques. A "FinFET" (a combination of "Fin" and **F**ield **E**ffect **T**ransistor (FET)) is a three-dimensional transistor fabricated on vertical fins instead of a flat surface like a planar transistor. I have given numerous invited talks and organized and taught international courses on FinFETs, including, for example, courses at IEEE's International Electron Device Meetings in 2009 and 2015.

18. In 2015, I taught a course on future FinFET technologies and FinFET design for 7 nm and 5 nm processes. I have also developed and taught graduate level courses on FinFETs, transistor layout, and fabrication at the University of Florida, including a course covering FinFET technologies and another course covering scaling and limits of FinFETs and transistor options that might replace FinFETs during the next decade.

19. I have experience analyzing transmission electron microscope ("TEM") images at Intel and other places in industry, including as a consultant of Chipworks, an independent reverse engineering firm that merged with TechInsights, another independent reverse engineering firm. I helped Chipworks staff understand features of transistors in electron micrographs (pictures obtained using electrons to image transistor structures).

20. I also co-founded a low power transistor technology company called SuVolta in 2009 that developed transistors that could operate at ultra-low power

for internet-of-things applications. SuVolta's intellectual property was sold to Fujitsu and included patents on both planar FETs and FinFETs that could operate at ultra-low power.

21. As the co-founder and Chief Technology Officer of SuVolta, and as an inventor myself, I am familiar with patents, the patent process, patent claims, and patent analysis.

B. Publications

22. I am a named inventor on over 100 granted United States patents and have authored over 60 peer-reviewed academic journal publications. I have co-authored a book on strained silicon transistors titled *Strain Effects in Semiconductors: Theory and Device Applications* (2009). I have patents and publications on SiGe/Strained Silicon technology, shallow trench isolation, FinFETs, and planar nanoscale transistors, all of which are relevant technologies in this case. A few examples relevant to this case are:

- My work on the SiGe/Strained Silicon technology is described in the frequently cited IEEE peer-reviewed paper S. Thompson, et al., *A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 μm^2 SRAM Cell*, Technical Digest of the 2002 International Electron Devices Meeting (IEDM), pp. 61-64 (2002).

- The history of the SiGe/Strained Silicon invention is explained in the frequently cited IEEE peer-reviewed paper S.E. Thompson et al., *Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap*, IEEE Transactions on Electron Devices, vol. 53, no. 5, pp. 1010-20 (May 2006).

- My work on shallow trench isolation is described in a 1998 paper published in the Intel Technology Journal: A. Brand et al., *Intel's 0.25 Micron, 2.0 Volts Logic Process Technology,* Intel Technology Journal, Q3 (1998).

- My work on FinFETs is described in, for example, the paper S. Suthram et al., *Understanding Strain Effects on Double-Gate FinFET Drive-Current Enhancement, Hot-Carrier Reliability and Ring-Oscillator Delay Performance via Uniaxial Wafer Bending Experiments,* 2008 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), pp. 163-164 (2008).

23. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, attached to this report as Appendix A.

24. Additional details about my employment history, fields of expertise, awards, publications, and other activities are further included in my curriculum vitae, attached as Appendix A.

25. I am being compensated for services provided in this matter at my standard consulting rate, plus travel expenses. My compensation is in no way conditioned on the outcome of this investigation or any issue therein, nor is it contingent upon the results of my study or the substance of my testimony. Similarly, my compensation is in no way dependent upon and in no way affects the substance of my statements in this declaration.

26. I have no financial interest in TSMC or any of its subsidiaries. I also do not have any financial interest in the Patent Owner. I do not have any financial interest in the ’281 Patent and have not had any contact with any of the named inventors of the ’281 Patent (Glenn A. Glass, Anand S. Murthy, Tahir Ghani) about the ’281 Patent or any issues in this Investigation.

III. Materials Reviewed

27. In forming my opinions regarding the ’281 Patent, I reviewed the references listed in Appendix B.

IV. Legal Standards

28. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the ’281 Patent are patentable, I have been told that I am obliged to follow existing law.

A. Anticipation

29. I have been told the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §102, a provision in the patent law regarding anticipation. I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication.

30. I have been told that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

B. Obviousness

31. I have been told that under 35 U.S.C. §103(a), "[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in Section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

32. When considering the issues of obviousness, I have been told that I am to do the following:

a. Determine the scope and content of the prior art;

b. Ascertain the differences between the prior art and the claims at issue;

c. Resolve the level of ordinary skill in the pertinent art; and

d. Consider evidence of secondary indicia of non-obviousness (if available).

33. I have been told that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged invention, which I have assumed is just before the earliest claimed priority date of the ’281 Patent.

34. I have been told that obviousness is a determination of law based on underlying determinations of fact. I have been told that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and any objective indications of non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the ’281 Patent).

35. I have been told that a prior-art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also have been told that a person of ordinary skill in the art is presumed to know all relevant prior art. I have been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

36. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I have been

told that the following principles may be considered, and I have been asked to consider them:

a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

b. The substitution of one known element for another is likely to be obvious if it yields predictable results;

c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a "reasonable expectation of success"—not "absolute predictability" of success—in achieving the claimed invention by combining prior art references.

37. I have been told that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the

claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

38. I have been told the reasons a person of ordinary skill in the art would have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I have been told that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I have been told it would be improper to consider only the specific problem the patentee was trying to solve.

39. I have been told that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been told that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I have been told that in many fields there may be little discussion of obvious combinations, and, in these fields, market demand—not scientific literature—may drive design trends. I have been told that when there was a design need or market pressure and there were a

finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

40. I have been told that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to combine them. But I also understand that any "teaching, suggestion, or motivation" present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I have been told this "teaching, suggestion, or motivation" test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

41. I have been told that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

42. When considering the obviousness of claimed ranges (e.g., material compositions), I have been told obviousness depends on whether a person of ordinary skill in the art would have appreciated that new and unexpected properties (as compared with known ranges and trends) resulted from the claimed range. I have been told that when the general conditions of a claim are disclosed in the

prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. For example, I have been told that if the prior art teaches the material composition in a device can be modified to affect the device properties, it is not inventive to discover the optimum or workable ranges of material composition by routine experimentation. I have also been told the prior art does not need to provide the exact method of optimization, and a claim to a device does not become nonobvious simply because the patent's specification provides a more comprehensive explication of the known relationships between the material composition and device properties.

43. I have been told that the outcome of optimizing a material composition may only be patentable if the claimed ranges are "critical" and produce a new and unexpected result that differs in kind, not merely in degree, from the results of the prior art. I have been told that when obtaining the claimed composition was within the capabilities of a person of ordinary skill in the art and does not produce any unexpectedly beneficial properties, the optimization of a composition known to affect device properties would have been obvious.

44. In addition, I have been told that any allegedly new and unexpected result must be "commensurate in scope" with the claimed range, meaning the new and unexpected result must apply across the entire range recited in the claim.

45. I have been told that, even if a claimed range of material compositions and a prior art range of material compositions do not overlap, the claimed range would have been obvious so long as the two ranges have only minor differences such that a person of ordinary skill in the art would have expected them to have the same properties.

V. Level of Ordinary Skill in the Art

46. I have been told that the parties agreed as to the level of ordinary skill in the art in the related ITC Investigation. I agree with that definition. A person having ordinary skill in the art in reference to the ’281 Patent would have possessed at least a Master’s degree in electrical engineering, physics, materials science and engineering, or a related field, and at least two years of work experience in integrated circuit device design or manufacturing. Additional education could substitute for professional experience, and significant work experience could substitute for formal education.

47. I have not analyzed the priority date of the ’281 Patent, but I note that the earliest claim of priority listed on the face of the ’281 Patent is December 21, 2010, the filing date of U.S. Patent Application Serial No. 12/975,278. Because all the prior art discussed in this declaration predates December 21, 2010, I have been asked for simplicity to treat December 21, 2010, as the priority date for the ’281

Patent. I have also treated this date as the date from which to assess the knowledge available to a person of ordinary skill in the art.

VI. Technological Background

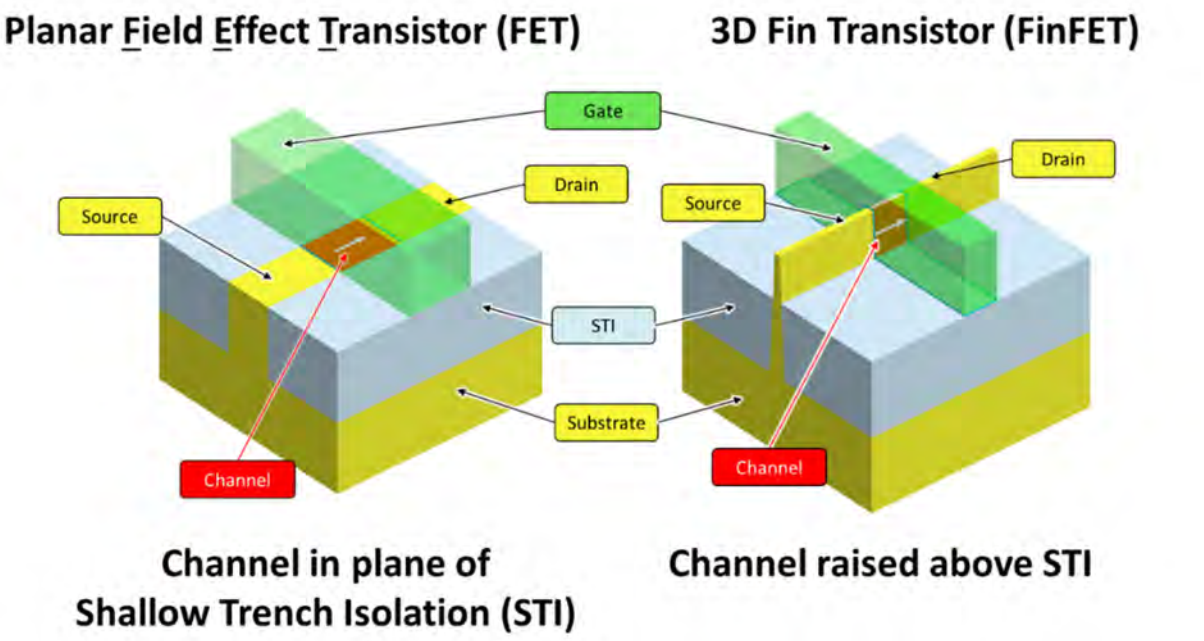
48. I understand that December 21, 2010, may be the earliest claimed priority date for the '281 Patent. In my opinion, all the elements in the '281 Patent were well known before this date. For example, as explained below, FinFETs were invented around 1999 and were on the International Technology Roadmap for adoption at least by 2007.[8] Further, SiGe/Strained Silicon technology was in widespread use well before 2010. And the aspects of SiGe/Strained Silicon technology described in the '281 Patent—including graded-composition SiGe source/drain regions and the use of a Ge capping layer on top of SiGe source/drain regions—were known (and, in the case of graded-composition SiGe, in commercial production) prior to December 21, 2010.

49. A person of ordinary skill in the art in the timeframe relevant to the '281 Patent would have been familiar with the background information described in subsections A through G below.

[8] *See* International Technology Roadmap for Semiconductors, *Front End Processes* at 2, 4-5, 28, 41, Fig. FEP2 (2009 ed.), *available at* https://www.dropbox.com/sh/ia1jkem3v708hx1/AADTglIZdiamwRIrPXi92ICEa/FEP.pdf?dl=0; International Technology Roadmap for Semiconductors, *Front End Processes* at 32, 59, Fig. FEP4 (2007 ed.), *available at* https://www.dropbox.com/sh/floxh3swiynur47/AACzVnirxru9A01LOPscpiWka/FEP.pdf?dl=0.

A. FinFETs Were Commonplace in the Semiconductor Industry

50. Two types of transistors commonly used by the semiconductor industry are planar Field Effect Transistors (FETs) and Fin-shaped Field Effect Transistors (FinFETs). Other than the "fin" geometry illustrated on the right below, planar FETs and FinFETs are the same. The two diagrams below illustrate a typical planar FET design (on the left) and a typical FinFET design (on the right).



51. The basic operation of both planar FET and FinFET structures is also the same. A "Gate" is positioned between the "Source" and "Drain" regions. During operation of the transistor, current flows between the source and drain regions through a channel underneath the gate represented by the arrow above between "Source" and "Drain." Similarly, the underlying physics of the current flow through the channel is the same whether the channel is in the plane of a

shallow trench isolation ("STI") in the substrate, as in the planar FET, or the channel is in the fin, as in the FinFET. Current flow dictates whether the transistor is "on" (current) or "off" (no current). A typical transistor can be thought of in simple terms as a switch turned off and on by a voltage applied to the gate, and modern computers use billions of transistors to perform very complex operations.

52. The basic fabrication of planar FETs and FinFETs is similar, except for the formation of the fin shape. As one author correctly summarized: "The process flow starts the fin formation similarly as the formation of active area (in planar CMOS) and followed by STI gap-fill and planarization and oxide recessing to reveal the fins. Then the rest of flow proceeds to similar steps (e.g. well, gate, epi-S/D, etc.) as the planar CMOS with gate-last high-k and metal-gate (HKMG) flow."[9] As the original FinFET patent (filed in 2000) states in the very first sentence of its abstract, "A FinFET device is fabricated using conventional planar MOSFET technology."[10] This allowed FinFETs to succeed commercially because they could be integrated using existing planar technology.

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[9] M.-H. Chi, *Challenges in Manufacturing FinFET at 20nm Node and Beyond*, Technology Development at 1 (2012).

[10] *Hu* (US6413802) at Abstract; *see also id.* at 2:11-14 (explaining that FinFETs are just "an extension of conventional planar MOSFET technology"), 5:37-40 (explaining that FinFETs are made using a process that "is compatible with conventional planar MOSFET fabrication techniques"); B. Doyle et al., *Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout*, Digest of the

53. The invention of the FinFET around the year 1999 was led by Chenming Hu, who also served as Chief Technology Officer of TSMC. Dr. Hu was awarded by President Obama the National Medal of Technology and Innovation for his FinFET invention.[11]

54. Both FinFETs and planar FETs include "Source" and "Drain" regions with semiconductor material other than silicon to impart mechanical force that pushes on the channel to alter the lattice constant of the material there. This technology I call SiGe/Strained Silicon technology, as SiGe is nearly universally used in p-type source/drain regions to create the strained channel. SiGe/Strained Silicon was invented about a decade before December 2010 and entered into commercial production by all the leading semiconductor companies shortly after. For example, Intel has used SiGe/Strained Silicon technology since the 90 nm process that I helped to develop went into production in 2003.

B. SiGe/Strained Silicon Was Nearly Universally Used in the Semiconductor Industry

55. Silicon is the standard semiconductor material used to fabricate FETs (e.g., the yellow region in the planar and FinFET transistors above) for integrated circuits (i.e., computer and other chips). To be power-efficient, modern integrated

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2003 Symposium on VLSI Technology at 133 (2003) (explaining that a FinFET "very much resembles [a] bulk transistor from the processing point-of-view").

[11] *See* https://nationalmedals.org/laureate/chenming-hu/.

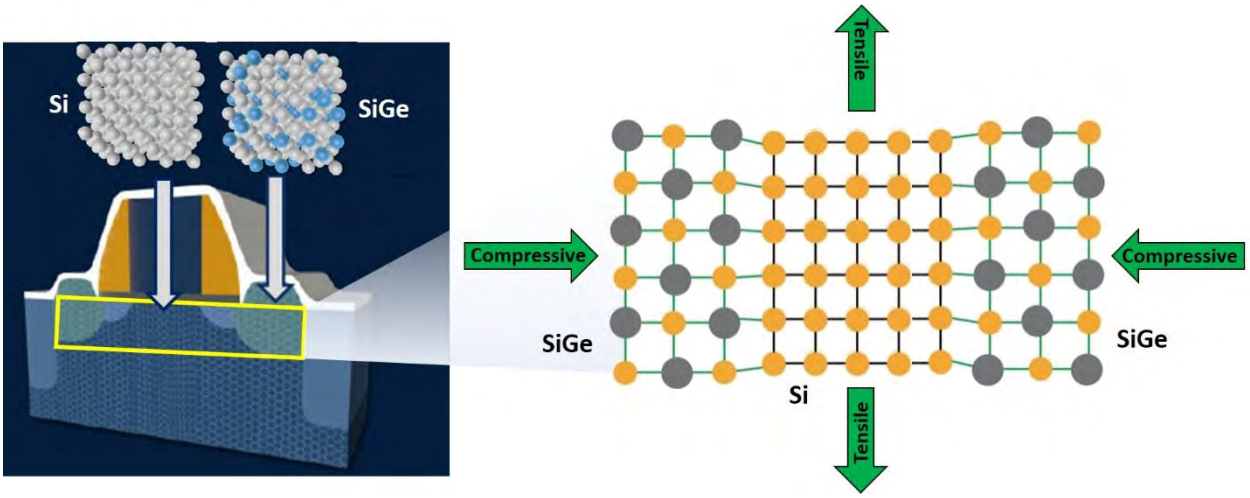
circuits typically include two types of FETs: a pFET, where the positive charge carriers flow to generate a logic “1”, and an nFET, where negative charge carriers flow to generate a logic “0”.

56. Prior to the invention of SiGe/Strained Silicon, the speed of pFETs was approximately half the speed of nFETs. SiGe/Strained Silicon was developed for pFETs to speed up the flow of positive charge from source to drain. pFETs employing SiGe/Strained Silicon often doubled the speed of prior pFETs.

57. The invention of SiGe/Strained Silicon placed a silicon-germanium (“Si_xGe_{1-x}” or, more briefly, “SiGe”) semiconductor compound into the source and drain regions of pFETs. SiGe semiconductor compounds have a larger lattice spacing than silicon. As a result, when SiGe is inserted in the source and drain regions of a transistor, large stresses develop and strain the silicon in the channel region (that is, the crystal lattice is physically compressed). The strain allows the positive charge carriers to move much more quickly from source to drain. This is sometimes referred to as enhanced “channel mobility” or “charge carrier mobility.”

58. I presented the detailed physics of how SiGe source/drain regions improve device performance at the International Electric Device Meeting in 2004. By 2010, this knowledge was well known and widely applied throughout the semiconductor industry.

59. Below are drawings of a FET with SiGe source/drain regions that sandwich a Si channel region. As shown on the right below, the crystalline silicon is a lattice of silicon atoms (shown as orange circles), and the crystalline SiGe is a lattice of a mixture of silicon atoms (orange circles) and germanium atoms (shown as gray circles). The green arrows indicate how the larger germanium atoms in the source/drain regions laterally compress the silicon atoms in the channel region (compressive stress), while pulling them apart in the vertical direction (tensile stress). The figure on the left below shows how the atoms in the silicon regions (dark blue) are deformed by the SiGe source/drain regions (green). In effect, the SiGe source/drain regions "squeeze" the Si channel region.



60. Crystalline germanium has a larger lattice constant than the crystalline silicon.[12] This means the silicon and germanium atoms in crystalline SiGe are

[12] Silicon has a lattice constant of 5.43 Å, and germanium has a lattice constant of 5.65 Å. *Thomas* (US2009/0075029) ¶ [0004].

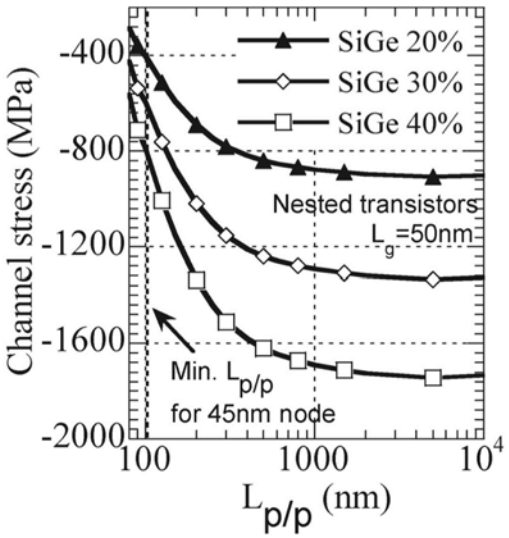
spaced farther apart than the silicon atoms in crystalline silicon. As a result, a given number of atoms of crystalline SiGe occupies a larger volume than the same number of atoms of crystalline silicon. Because of this structural difference between crystalline silicon and crystalline SiGe, SiGe grown in source and drain regions creates a lateral compressive strain on the silicon channel region of the transistor. This allows "holes"—the majority charge carriers in p-type transistors (pFETs)—to move more efficiently through the channel, thereby increasing transistor switching speed.[13] A person of ordinary skill in the art would have understood these principles and would have known that adding more germanium to the source/drain regions creates more strain and enhances this benefit.[14]

61. Prior to December 21, 2010, it was known that increasing the Ge concentration in an FET increased performance. In particular, it was known that increased Ge concentration was required when scaling to smaller transistors (i.e., following Moore's law, by which feature size is reduced every few years for integrated circuits). As was understood, this is because smaller transistors have a smaller-area source, so source/drain regions create less compressive stress for the

[13] *See* M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 229 (Mar. 2005); *Thomas* (US2009/0075029) ¶¶ [0003], [0004], [0030].

[14] *See*, *e.g.*, *Thomas* (US2009/0075029) ¶ [0007].

same Ge concentration. The benefits of increased Ge concentration in ever-smaller FETs was widely reported well before 2010. As a contemporaneous article observed, a "disproportionate reduction in device area per generation with respect to gate length, requires increased strain in the e-SiGe to compensate for the lost volume due to non-scaled gate length."[15] "Ge concentration has increased steadily from <20% in 90 nm pFETs to >35% in 32 nm pFETs, **and this trend is expected to continue to future nodes.**"[16] Discussing the figure below, an earlier article similarly explained that channel stress can be maintained "in the next technology nodes" by "us[ing] higher germanium concentrations in the S/D area."[17]



Eneman, Fig. 10

[15] D.K. Sadana et al., *Applications of Epitaxy for Semiconductor Technology*, ECS Transactions, 218th ECS Meeting, vol. 33, no. 6, at 64 (Oct. 2010).

[16] *Id.*

[17] G. Eneman et al., *Scalability of the Si_xGe_{1-x} Source/Drain Technology for the 45-nm Technology Node and Beyond*, *IEEE Transactions on Electron Devices*, vol. 53, no. 7, at 1651, 1653 (July 2006); *see also id.* at Fig. 10 (shown above).

62. When adding more Ge to the SiGe source/drain regions to achieve more strain, a person of ordinary skill in the art would have known to minimize dislocations in the SiGe in order to maintain the stress applied to the channel region.[18] The best way to do so was known well before December 2010: gradually increase the Ge concentration, and thus lattice constant, from a level compatible with the underlying material to a level that provides a high degree of compressive strain.[19] As one reference explains, graded Si_xGe_{1-x} "minimize[s] the misfit dislocation nucleation and propagation and hence retain[s] maximum strain."[20]

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[18] *See Ranade* ¶¶ [0033], [0040]; *Jin* (US7767560) at 3:30-44, 3:60-64, 4:2-8, 4:28-60; *Thomas* (US2009/0075029) ¶¶ [0030]-[0032]; *Kavalieros* (US8211772) at 2:10-22, 4:58-61; H. Okamoto et al., *A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-Node High-Performance pMOSFET Technology*, Proceedings of the 2008 38th European Solid-State Device Research Conference (ESSDERC), at 327 (Sept. 2008) ("One possible cause of strain relaxation could be a generation of crystal defects in eSiGe.").

[19] *See, e.g.*, *Ranade* ¶¶ [0033], [0040]; J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2-3, Figs. 1-4, 6, 7 (2006); *Thomas* (US2009/0075029) ¶¶ [0008], [0032]-[0034], [0042], [0044]; *Jin* (US7767560) at Abstract, 4:38-5:19, 7:61-8:31; *Kavalieros* (US8211772) at 2:11-22, 5:56-6:6, 6:38-7:11, Fig. 5b; *Simonelli* (US2010/0148217) at Title, Abstract, ¶¶ [0001], [0024], [0044], Figs. 14, 15; *Yasutake* (US2007/0187767) ¶¶ [0083]-[0095]; *Liu '953* (US2007/0122953) ¶¶ [0059], [0060].

[20] J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2 (2006).

Accordingly, "[t]he degree of stress relaxation of graded eSiGe has been proven to be smaller than that of high uniform %Ge eSiGe."[21]

63. Typically, the SiGe is graded from a low Ge concentration at the bottom of the source and drain regions (where it interfaces with the silicon) to a higher Ge concentration when approaching the top of the source/drain regions. As a patent filed in 2004 explained, "[s]ince [the] graded germanium profile does not have a sharp interface (where the dislocations are generated) between SiGe and Si, dislocations are not easily produced[,]" which "reduce[s] leakage of devices caused by dislocations."[22] Another known benefit of "graded germanium profiles" was that it could "optimize stress in order to enhance device performance."[23]

64. As the '281 Patent itself acknowledges, SiGe/Strained Silicon was already in widespread use in transistors by December 2010. Intel and the industry at large had been producing integrated circuits that incorporated SiGe/Strained Silicon for about a decade. Intel, in fact, had four generations of SiGe/Strained Silicon in high-volume manufacturing before 2010 (90 nm, 65 nm, 45 nm, and 32

[21] *Id.*; *see also id.* ("[S]tress relaxation caused by misfits dislocation and defect propagation is much smaller for graded SiGe."); *Ranade* ¶ [0040] (explaining that "the grading process minimizes surface defects").

[22] *Zhu* (US7288443) at 1:56-62.

[23] *Id.* at 1:62-64; *see also* J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2-3 (2006).

nm).[24] By December 2010, essentially the entire industry had adopted SiGe/Strained Silicon technology.

65. Again, a person of ordinary skill in the art would have understood these principles, including how to implement SiGe/Strained Silicon technology to enhance FET device performance, because doing so was ubiquitous at the time.[25]

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[24] *See generally* S. Natarajan et al., *A 32nm Logic Technology Featuring 2nd-Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171 μm^2 SRAM Cell Size in a 291 Mb Array*, Technical Digest of the 2008 International Electron Devices Meeting (IEDM), pp. 1-3 (2008); K. Mistry et al., *A 45nm Logic Technology with High-k + Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193 nm Dry Patterning, and 100% Pb-Free Packaging*, Technical Digest of the 2007 International Electron Devices Meeting (IEDM), pp. 247-250 (2007); P. Bai et al., *A 65nm Logic Technology Featuring 35 nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell*, Technical Digest of the 2004 International Electron Devices Meeting (IEDM), pp. 657-660 (2004); S. Thompson, et al., *A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 μm^2 SRAM Cell*, Technical Digest of the 2002 International Electron Devices Meeting (IEDM), pp. 61-64 (2002).

[25] *See Ranade* at Abstract, ¶¶ [0010], [0014], [0023], [0038]-[0040], [0047]; J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2-3, Figs. 1-16 (2006); *Simonelli* (US2010/0148217) at Title, ¶¶ [0020], [0024], [0038], [0042], [0044], [0053], [0058]; *Kim* at ¶¶ [0054], [0064]; *Thomas* (US2009/0075029) at Title, Abstract, ¶¶ [0003]-[0005], [0007], [0008], [0029]-[0032], [0044], [0063]; *Murthy* (US6949482) at 1:41-2:20, 6:60-7:10; *Yasutake* (US2007/0187767) ¶¶ [0004], [0005], [0023], [0034], [0038], [0041], [0048], [0049], [0056]-[0058], [0068], [0071], [0075], [0082], [0093]; *Kavalieros* (US8211772) at Abstract, 1:55-63, 2:11-22, 2:59-67, 4:56-57; *Jin* (US7767560) at Title, Abstract, 1:9-13, 1:45-57, 2:44-51, 3:10-5:19, 5:48-6:1, 6:61-7:13, 8:62-10:27, 10:50-67, Figs. 4E, 4F; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and*

One reference, for example, remarks that "[c]hannel strain engineering" with epitaxial SiGe (eSiGe) source/drain regions "has been pursued aggressively in scaled CMOS technologies."[26] Intel's 90 nm, 65 nm, 45 nm, and 32 nm processes—released in 2003, 2005, 2007, and 2009, respectively—all used SiGe/Strained Silicon technology.[27] Consistent with my explanation above, the trend was towards using more Ge at each new process node as the devices became smaller, facilitated by using a graded Ge concentration.

C. Ge Capping Layers Were Known for Reducing Source/Drain Contact Resistance Via Lower Schottky Barrier Height

66. For any FET device, one of the design goals is to minimize source/drain contact resistance at the interface between the source/drain regions (which are made of a semiconductor material) and their respective electrical

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Beyond, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 229-30 (Mar. 2005); S. Gannavaram et al., *Low Temperature (≤800°C) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for Sub-70 nm CMOS*, Technical Digest of the 2000 IEEE International Electron Devices Meeting (IEDM) at 437-38, Figs. 4, 12 (2000); H. Okamoto et al., *A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-Node High-Performance pMOSFET Technology*, Proceedings of the 2008 38th European Solid-State Device Research Conference (ESSDERC), at Abstract, 326-29, Figs. 1, 5 (Sept. 2008).

[26] J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2, Figs. 1-16 (2006).

[27] *See supra* note 2424.

contacts (which are made of metal). Excessive contact resistance will lower switching speeds and increase power consumption and heating, which are detrimental to device performance and reliability. And when channel resistance is reduced, as has been the trend over time (especially with SiGe/Strained Si technology), it becomes even more important to use low-resistance source/drain contacts because the contact resistance should be kept much smaller than the channel resistance.[28]

67. Prior to December 2010, it was widely reported that a Ge capping layer, formed on top of SiGe source/drain regions in a pFET, could provide benefits by reducing the source/drain contact resistance.

68. Source/drain contact resistance refers to the electrical resistance caused at the interface between the metallic source/drain electrodes and the source/drain semiconductor material that directly touches it. As I teach my own students, the mathematical expression for the source/drain contact resistance (or the contact resistance at any metal-semiconductor interface) is:

$$R_c = \frac{\rho_0}{A} e^{\left(\frac{2\sqrt{\varepsilon m^*}}{\hbar} \frac{\Phi_B}{\sqrt{N_D}}\right)}$$

[28] *See* S.E. Thompson & S. Parthasarathy, *Moore's Law: The Future of Si Microelectronics*, Materials Today, vol. 9, no. 6, at 23-24 (June 2006).

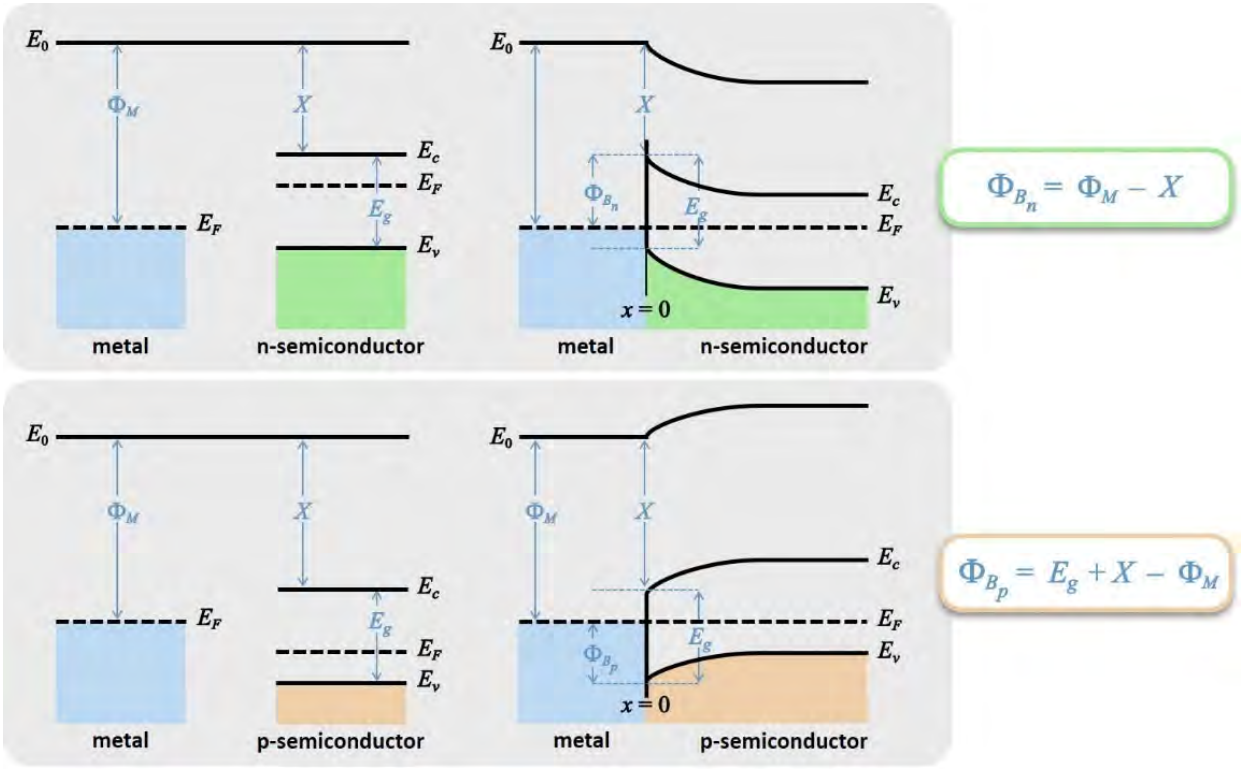
where ρ_0 is the resistivity of a perfect ohmic contact, A is the surface area of the interface between the metal and semiconductor, ε is the dielectric constant of the semiconductor, m^* is the effective mass of the majority charge carriers in the semiconductor, $\hbar$ is Dirac's constant, ϕ_B is the Schottky barrier height, and N_D is the doping concentration of the semiconductor at the interface between the metal and semiconductor.[29]

69. A person of ordinary skill would have understood from this equation that one of the most obvious ways to reduce contact resistance at a metal-semiconductor interface is to reduce the Schottky barrier height.[30] I prepared the diagram below to illustrate the well-understood concept of Schottky barrier heights, discussed in any textbook that addresses metal-semiconductor interfaces:

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[29] *See* J.D. Plummer et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling* at 688-90 (2000); S.M. Sze, *Physics of Semiconductor Devices* (2d ed. 1981) at 304; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 223-24 (Mar. 2005); *Murthy* (US6949482) at 8:35-56; *Yasutake* (US2007/0187767) ¶¶ [0043], [0044].

[30] *See Kim* ¶¶ [0003]-[0008], [0010], [0050], [0051], [0058], [0074]; *Haran* (US8358012) at Title, 1:7-25, 3:17-22; *Tung* ¶¶ [0005], [0006], [0021], [0027], [0029]-[0032], [0034], [0039], [0061], [0070], [0078]; *Murthy* (US6949482) at Abstract, 2:66-3:13, 8:34-9:63, Figs. 5-8; *Yasutake* (US2007/0187767) ¶¶ [0005], [0024], [0025], [0039]-[0045], [0050], [0066], [0070], [0086], [0093]; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, pp. 222-231, at 226 (Mar. 2005).



$\boldsymbol{\Phi_{B_n}}$: *n type Schottky barrier height*	$\boldsymbol{\chi}$: *semiconductor electron affinity*
$\boldsymbol{\Phi_{B_p}}$: *p type Schottky barrier height*	$\boldsymbol{E_c}$: *semiconductor conduction band edge*
$\boldsymbol{\Phi_M}$: *metal work function*	$\boldsymbol{E_v}$: *semiconductor valence band edge*
$\boldsymbol{E_F}$: *Fermi level*	$\boldsymbol{E_g}$: *semiconductor band gap* $(E_c - E_v)$

70. The figure on the top-left above shows energy diagrams for a metal and an n-type semiconductor isolated from one another. The figure on the top-right shows an energy diagram for the same metal and n-type semiconductor when they contact one another at an interface (x=0). Similarly, the figure on the bottom-left above shows energy diagrams for a metal and a p-type semiconductor isolated from one another. The figure on the bottom-right shows an energy diagram for the

same metal and p-type semiconductor when they contact one another at an interface (x=0). The variables in the diagram are as shown below the diagram.

71. The Fermi level is the highest energy level that an electron can occupy at absolute zero temperature. Although the Fermi levels for a metal and a semiconductor typically differ when the two materials are isolated from one another, they do not differ when the metal and semiconductor are joined at a metal-semiconductor interface. In the upper-left figure above, the Fermi level of the n-type semiconductor material is higher than the metal, which means the more energetic electrons move from the semiconductor to the metal until an equilibrium obtains and the Fermi levels are equal at the interface (as the upper-right figure above shows). This causes the so-called “band bending” in the upper-right diagram above. Similarly, in the lower-left figure above, the Fermi level of the p-type semiconductor material is lower than in the metal, which means the more energetic electrons move from the metal to the semiconductor to obtain an equilibrium in which the Fermi levels are equal at the interface (as the lower-right figure above shows). This again causes band bending, as the lower-right diagram shows above.

72. As the diagram above also shows, the Schottky barrier height in the case of an n-type semiconductor-metal interface is the difference between the conduction band edge and the Fermi level at the metal-semiconductor interface. Similarly, the Schottky barrier height in the case of a p-type semiconductor-metal

interface is the difference between the Fermi level and the valence band edge at the metal-semiconductor interface. Because the values of the Fermi level and band edges at the semiconductor-metal interface can be difficult to measure directly, the expressions for the n-type and p-type Schottky barrier heights are more commonly written in terms of more fundamental material properties—namely, the metal work function (Φ_M), the semiconductor electron affinity (χ), and the semiconductor band gap (E_g). The basic expressions for the Schottky barrier height are shown in the diagram above and repeated here:

$$\Phi_{B_n} = \Phi_M - \chi$$

$$\Phi_{B_p} = E_g + \chi - \Phi_M$$

73. The ’281 Patent acknowledges these concepts were well known:

> As is known, the Schottky barrier height is the barrier for electrical conduction across a semiconductor-metal junction. The magnitude of the Schottky barrier height reflects a mismatch in the energy position of the metal’s Fermi level and the majority carrier band edge of the semiconductor across the semiconductor-metal interface. For a p-type semiconductor-metal interface, the Schottky barrier height is the difference between the metal Fermi level and the valence band maximum of the semiconductor.[31]

74. A person of ordinary skill in the art would have understood that the electron affinity of silicon (4.05 eV) and the electron affinity of germanium

[31] ’281 Patent at 14:48-57.

(4.00 eV) are very similar,[32] which means the electron affinity in SiGe does not vary much with germanium concentration. A person of ordinary skill in the art also would have understood that the metal work function of $TiSi_2$ (~4.53 eV)[33] and the work function of $TiGe_2$ (~4.57 eV)[34] are very similar, which means the work function in $Ti(Si_xGe_{1-x})_2$ does not vary much with germanium concentration either. The remaining variable for p-type SiGe is the SiGe band gap, which varies significantly at certain germanium concentrations. As one author summarizes, "the bandgap of Ge ($\mathcal{E}_g$=0.66 eV) is much smaller than Si ($\mathcal{E}_g$=1.12 eV). This allows modification of the valence band edge position," as shown below, "by varying the Ge fraction *x*."[35]

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[32] *See, e.g.*, S.M. Sze, Physics of Semiconductor Devices at 850 (2d ed. 1981).

[33] *See, e.g.*, E. Bucher et al., *Work Function and Barrier Heights of Transition Metal Silicides*, Applied Physics A, no. 40, pp. 71-77, at tbl. 1 (1986).

[34] *See, e.g.*, E.D. Marshall et al., *Metal-Germanium Contacts and Germanide Formation*, Materials Research Society Symposia Proceedings, vol. 47: Symposium C – Thin Films: The Relationship of Structure to Properties, pp. 161-166, at Fig. 1 (1985) (showing an n-type Schottky barrier height of 0.57 eV for $TiGe_2$ on n-type Ge, which means the work function of $TiGe_2$ is 4.57 eV because $\Phi_{B_n}(0.57\ eV) + \chi_{Ge}\ (4.00\ eV) = \Phi_{TiGe_2}\ (4.57\ eV)$).

[35] V.E. Houtsma, *Gate Oxide Reliability of Poly-Si and Poly-SiGe CMOS Devices*, Doctoral Dissertation, University of Twente, at 10-11 & Fig. 1.5 (1999); *see also* M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 224, 226-27, Fig. 12 (Mar. 2005).

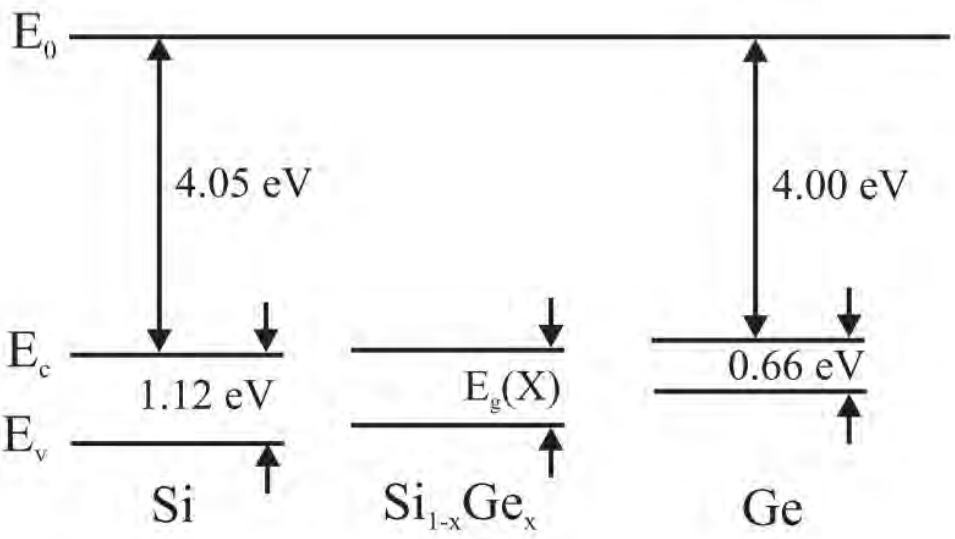


Figure 1.5: Energy band diagram of Si, SiGe and Ge. It can be observed that the bandgap of SiGe can be tuned by changing the Ge fraction.

75. Given the above, a person of ordinary skill in the art would have known the Schottky barrier height of a pFET source/drain contact depends on the SiGe bandgap because it reflects a change in the valence band edge position. A person of ordinary skill in the art also would have known that the SiGe bandgap depends on the Ge concentration according to the well-known figure below[36]:

[36] R. Braunstein et al., *Intrinsic Optical Absorption in Germanium-Silicon Alloys*, Physical Review, vol. 109, no. 3, pp. 695-710, at Fig. 17 (1958); *see also* J. Weber & M.I. Alonso, *Near-Band-Gap Photoluminescence of Si-Ge Alloys*, Physical Review B, vol. 40, no. 8, pp. 5683-5693, at 5689, Fig. 9 (1989); M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, pp. 222-231, at 227, Fig. 12 (Mar. 2005).

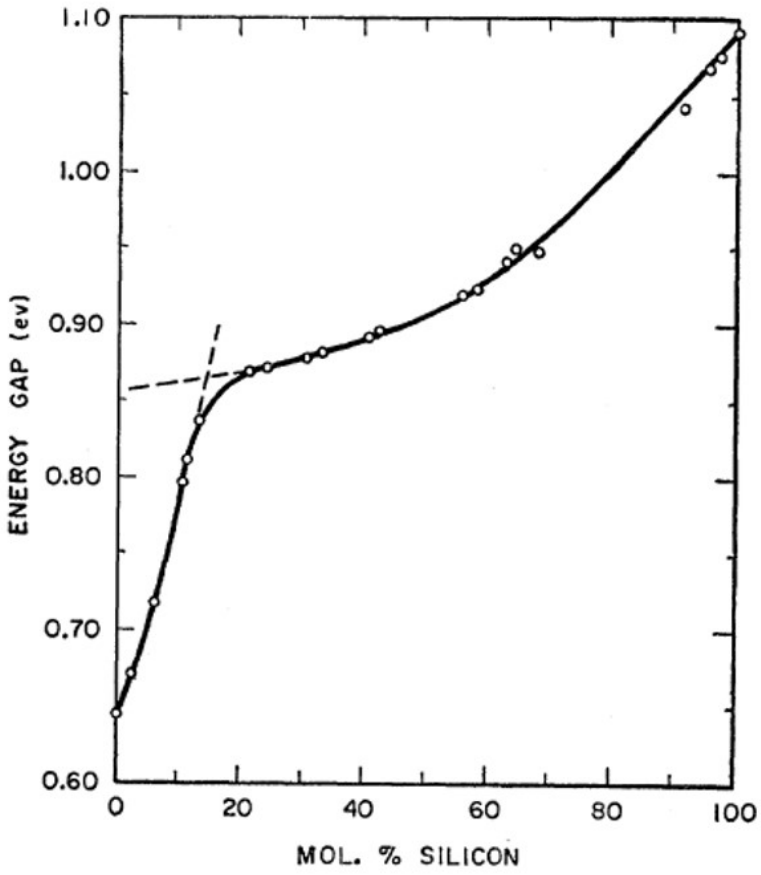


FIG. 17. Composition dependence of energy gap in Ge-Si alloys at 296°K, based on one-phonon Macfarlane-Roberts expression; see Eq. (1) in text.

76. As the figure above illustrates, there is a sharp kink in the Si_xGe_{1-x} bandgap near about 15 atomic % silicon (i.e., about 85 atomic % germanium). At this concentration, a "crossover from the Si-like *X*-conduction band minimum to the Ge-like *L* conduction-band minimum occurs."[37] The SiGe band gap decreases sharply beyond this crossover concentration (i.e., at about 85 atomic % germanium). A person of ordinary skill in the art would have therefore desired

[37] J. Weber & M.I. Alonso, *Near-Band-Gap Photoluminescence of Si-Ge Alloys*, Physical Review B, vol. 40, no. 8, pp. 5683-5693, at 5689 (1989).

using a Ge capping layer having a Ge concentration above the transition at about 85 atomic % to minimize the Schottky barrier height and, with it, the source/drain contact resistance.[38] This is the proposal I would have expected my graduate students to provide if I asked on an exam how to reduce the source/drain contact resistance of a SiGe pFET device.

77. Such Ge capping layers were reported well before December 2010. For example, *Yasutake* (shown below) includes source/drain regions 111 formed using a graded p-type SiGe layer 109 and a germanium capping layer 110.[39] The "germanium concentrations in the silicon germanium layer 109B and the germanium layer 110 are 10 to 30 at % and approximately 100 at %, respectively."[40] In between, SiGe layer 109C is graded, whereby "the germanium concentration of the silicon germanium layer 109C is approximately 10 to 30 at % on an interface between the silicon germanium layer 109C and the silicon-germanium layer 109B, and increased toward the upper portion" of layer 109C.[41] "The germanium concentration of the silicon germanium layer 109C is

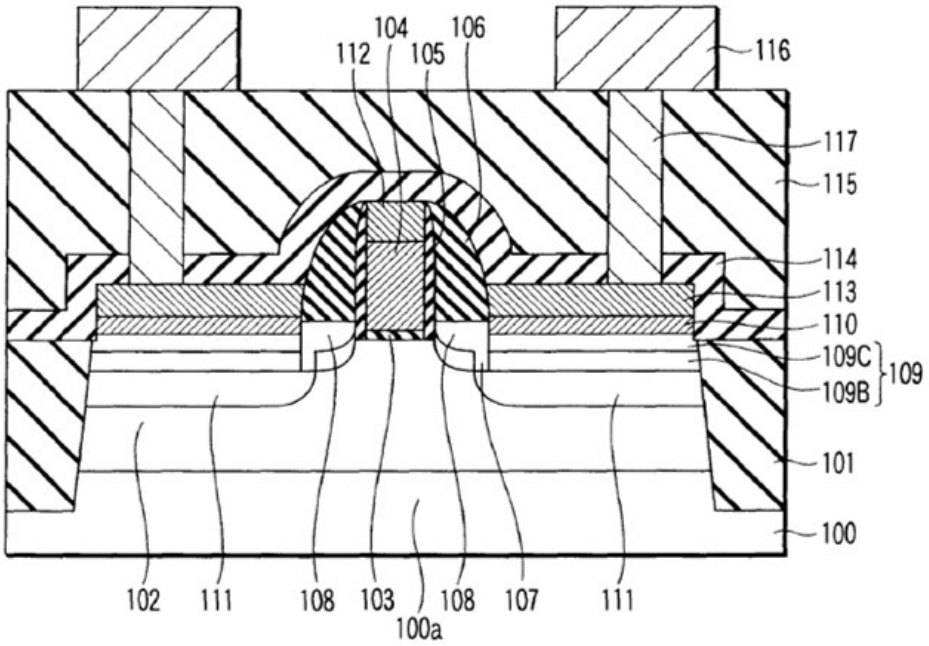
[38] When I refer to a Ge layer in this declaration, I am generally including a SiGe layer with a Ge concentration exceeding about 85 atomic %. I use the term "pure" or "100 atomic %" to refer specifically to a layer of Ge without any Si.

[39] *Yasutake* (US2007/0187767) ¶¶ [0086], [0090], [0094], [0095], Fig. 16.

[40] *Id.* ¶ [0085].

[41] *Id.*; *see also id.* ¶ [0042].

approximately 100 at % on an interface between the silicon germanium layer 109C and the germanium layer 110."[42] This Ge capping layer lowers contact resistance and, when annealed in the presence of a metal, can react with the metal to form a low-resistance germanide layer.[43]



78. As one would expect, *Yasutake* employs the Ge capping layer precisely because of the mathematical expression for contact resistance and the considerations I discuss above.[44] *Yasutake* also explains that, "as compared with the conventional technology where the **silicide film is formed on the silicon layer or the silicon germanium layer**, the contact resistance in the source/drain layer

[42] *Id.* ¶ [0085]; *see also id.* ¶ [0042].

[43] *Id.* ¶ [0024].

[44] *Id.* ¶¶ [0043]-[0045].

can be reduced in this embodiment where the **germanide layer is formed on the germanium layer**."[45]

79. Even before *Yasutake*, others had reported the use of a Ge capping layer to reduce contact resistance in this way. As one example, *Honeycutt* teaches how to use a "layer of germanium in the bottom of the contact opening . . . to form a low resistance contact," as Figures 6 and 8 illustrate below.[46]

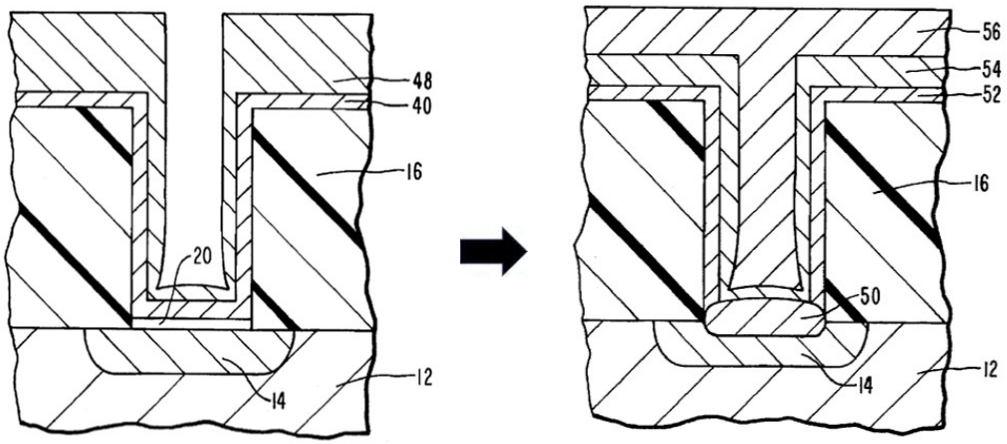


FIG. 6 FIG. 8

80. A low-pressure chemical vapor deposition (LPCVD) process performed using germane (GeH_4) gas deposits about 30 to 100 Å of a germanium layer 40 into a contact opening of an insulating layer 16.[47] The contact hole is formed over active region 14 (e.g., a source/drain region), and the germanium

[45] *Id.* ¶ [0045].

[46] *Honeycutt* (US5644166) at 1:8-15; *see also id.* at Figs. 6, 8.

[47] *Id.* at 6:56-7:28.

layer 40 may be doped in accordance with the active region 14.[48] A titanium layer 48 with approximately the same thickness as the germanium layer 40 is then deposited onto germanium layer 40.[49] Next, this structure is annealed to cause a reaction between the silicon in active region 14, germanium in germanium layer 40, and titanium in titanium layer 48, which results in "a region of titanium germanosilicide ($TiSi_xGe_y$) 50 . . . formed at the bottom of contact openings 18 and a layer of titanium germanide ($TiGe_x$) 52 . . . formed at the sides of contact opening 18."[50]

D. Graded Doping in Source/Drain Regions Was Nearly Universally Used in the Semiconductor Industry

81. "Doping" refers to the act of deliberately adding certain impurities to a semiconductor material to control its conductivity. Adding an atom with one more valence electron than the semiconductor adds mobile electrons and makes the material have "n-type" conductivity. Adding an atom with one less valence electron than the semiconductor material creates "holes," or vacancies, for electrons to move between, and those holes act like mobile positive charges. This makes the material "p-type." In silicon and germanium, the most common n-type

[48] *Id.*; *see also id.* at 7:61-8:2.

[49] *Id.* at 7:29-50.

[50] *Id.* at 8:3-23.

dopants are phosphorous and arsenic, and the most common p-type dopant is boron.[51]

82. A person of ordinary skill in the art would have understood that doping can be performed by two standard methods, sometimes in combination. One process, called in-situ doping, is performed by adding impurities during growth of the semiconductor. The other is called ion implantation, which is performed by injecting energetic ions into the semiconductor material, then performing an activation anneal to incorporate the dopant atoms into the semiconductor crystal and make them electrically active.

83. Although in-situ doping can have a graded or uniform profile, depending on the growth parameters, a person of ordinary skill in the art would have understood that the processes of ion implantation and activation annealing necessarily result in a graded doping profile. Ion implantation for p-type SiGe involves irradiating the source/drain regions with energetic boron ions. Those boron ions are scattered by the Si and Ge atoms in the source/drain regions as they penetrate into the semiconductor lattice, causing the boron atoms to spread out as they penetrate below the surface of the source/drain regions.[52] Activation annealing

[51] Indium may also be used, but it is much less common.

[52] *See generally* H. Xiao, *Introduction to Semiconductor Manufacturing Technology* at 272-82 (2001).

then causes diffusion of those boron atoms—a phenomenon inherently based on the movement of atoms due to a concentration gradient according to Fick's Law. The data below illustrates typical gradients for boron ion implantation at various Ge concentrations[53]:

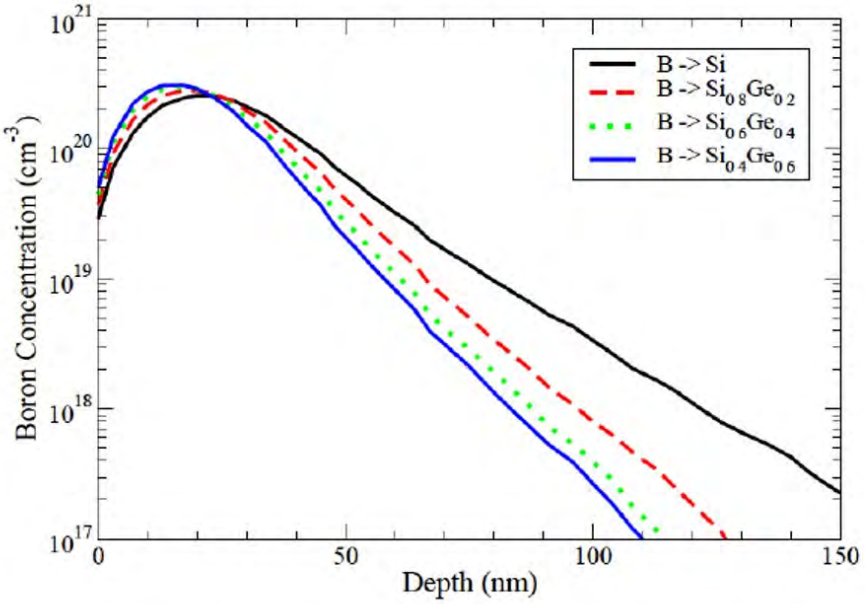


Figure 4.5: Simulated 5keV boron profiles in (100) $Si_{1-x}Ge_x$ with x = 0, 20%, 40%, 60% using a dose of $10^{15}cm^{-2}$ and a tilt of 7°.

***Wittman* at Fig. 4.5**

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[53] R. Wittman, *Miniaturization Problems in CMOS Technology: Investigation of Doping Profiles and Reliability*, Doctoral Dissertation, Wien University Austria, at Fig. 4.5 (Jan. 2007); *see also* P. Ranade et al., *A Novel Elevated Source/Drain PMOSFET Formed by Ge-B/Si Intermixing*, IEEE Electron Device Letters, vol. 23, no. 4, at 218, Figs. 1, 2 (Apr. 2002); C.C. Wang et al., *Boron Diffusion in Strained and Strain-Relaxed SiGe*, Materials Science and Engineering B, vols. 124-125, at Figs. 2, 5 (2005); J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 3, Fig. 5 (2006); H. Okamoto et al., *A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-Node High-Performance pMOSFET Technology*, Proceedings of the 2008 38th European Solid-State Device Research Conference (ESSDERC), at 328, Fig. 9 (Sept. 2008).

84. As I explain in Section VI.B, SiGe source/drain regions provide beneficial strain to the channel region to enhance channel mobility. In addition to this benefit, a person of ordinary skill in the art would have understood that SiGe source/drain regions provide two other benefits. First, "the retarded diffusion of boron in SiGe," which is proportional to the Ge concentration, "is an extra benefit for device scaling."[54] This allows better control over doping profiles to help mitigate short-channel effects (SCEs) that can damage a device. Second, increasing the doping concentration at the metal-semiconductor interface reduces the source/drain contact resistance.[55] As I explain in Section VI.C, a person of ordinary

[54] C.C. Wang et al., *Boron Diffusion in Strained and Strain-Relaxed SiGe*, Materials Science and Engineering B, vols. 124-125, at 39 (2005); *see also* H. Okamoto et al., *A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-Node High-Performance pMOSFET Technology*, Proceedings of the 2008 38th European Solid-State Device Research Conference (ESSDERC), at 328 (Sept. 2008) ("The boron profile in SiGe is shallower and more abrupt than that in Si. This result indicates the formation of shallower junction in SiGe than that in Si with same implantation and annealing condition. . . . There are two reasons to explain this result. One is the reduction of boron diffusion in SiGe, and the other is the higher boron activation rate in SiGe."), Fig. 11.

[55] *See Chong* (US2007/0235802) ¶¶ [0055], [0095], [0096], [0124]; J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2 (2006); *Simonelli* (US2010/0148217) ¶¶ [0054], [0057], [0058]; *Tung* ¶¶ [0005], [0027], [0034], [0065], [0069]; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, pp. 222-231, at 223-26 (Mar. 2005).

skill in the art would have understood that the source/drain contact resistance is proportional to $e^{1/\sqrt{N_D}}$, where N_D is the doping concentration near the metal-semiconductor interface.[56] This suggests increasing dopant concentrations at the metal-semiconductor interface (at the top of the source/drain regions). That is, "the doping density at the metal-semiconductor interface must be sufficiently high to achieve an excellent ohmic contact."[57]

85. A common technique used by those in the art before December 2010 was to employ a graded source/drain dopant profile, such that more dopant appears at the source/drain contact interface to reduce contact resistance and less dopant appears deeper within the source/drain regions to prevent SCEs.[58] *Chong* (US2007/0235802) explains, for example:

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[56] *See* J.D. Plummer et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling* at 688-90 (2000); M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 223-24 (Mar. 2005); *Murthy* (US6949482) at 8:35-56; *Yasutake* (US2007/0187767) ¶¶ [0043], [0044]; S.M. Sze, *Physics of Semiconductor Devices* (2d ed. 1981) at 304.

[57] M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 223 (Mar. 2005); *see also id.* ("To lower the contact the resistance, we need a small Schottky barrier height at the interface and a sufficiently high doping level under the metal contact."), Fig. 5.

[58] *See Chong* (US2007/0235802) at Abstract, ¶¶ [0055], [0095], [0096], [0107]-[0110], [0124], Fig. 6A; J.-P. Han et al, *Novel Enhanced Stressor with Graded*

> In general, the B concentration in the stressor region should be as high as possible to reduce the series resistance. However, if it is too high, the transistor may suffer from severe short channel effects. Hence, the graded (e.g. B) impurity stressor gives the flexibility to tune the active carrier profile in the S/D region such that the boron concentration at the near surface regions is extremely high (1E20 to 2E21/cm^3) and boron concentration at the middle and lower portion of the S/D region is relatively low (1E18 to 1E20/cm^3). The lowest portion of the S/D region should ideally be graded to reduce the junction capacitance.[59]

86. A person of ordinary skill in the art would have understood that it was routine in the semiconductor industry to apply a graded boron doping profile to FET source/drain regions to reduce contact resistance and mitigate SCEs in SiGe pFETs.[60]

Embedded SiGe Source/Drain for High Performance CMOS Device, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2-3, Fig. 5 (2006); *Yasutake* (US2007/0187767) ¶ [0059]; *Tung* ¶¶ [0005], [0027], [0031], [0034], [0065], [0069], Figs. 11b, 12b; S. Gannavaram et al., *Low Temperature (≤ 800°C) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for Sub-70 nm CMOS*, Technical Digest of the 2000 International Electron Devices Meeting (IEDM) at 437-38, Fig. 7 (2000); H. Okamoto et al., *A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-Node High-Performance pMOSFET Technology*, Proceedings of the 2008 38th European Solid-State Device Research Conference (ESSDERC), at Abstract, 326-29 & Fig. 7 (Sept. 2008) ("[B]oron diffusion is suppressed for both vertical and lateral direction. This is the reason of SCE suppression which is observed in Fig. 7.").

[59] *Chong* (US2007/0235802) ¶ [0124].

[60] *See supra* note 58.

E. Forming Metal-Semiconductor Compounds on Source/Drain Regions Was Nearly Universal in the Semiconductor Industry

87. Silicides were pervasive in the semiconductor industry long before December 2010. Since the 1980s, they have been used to form low-resistance contacts to Si source/drain regions by lowering the Schottky barrier height. Silicides also have been taught in textbooks since at least the 1990s.

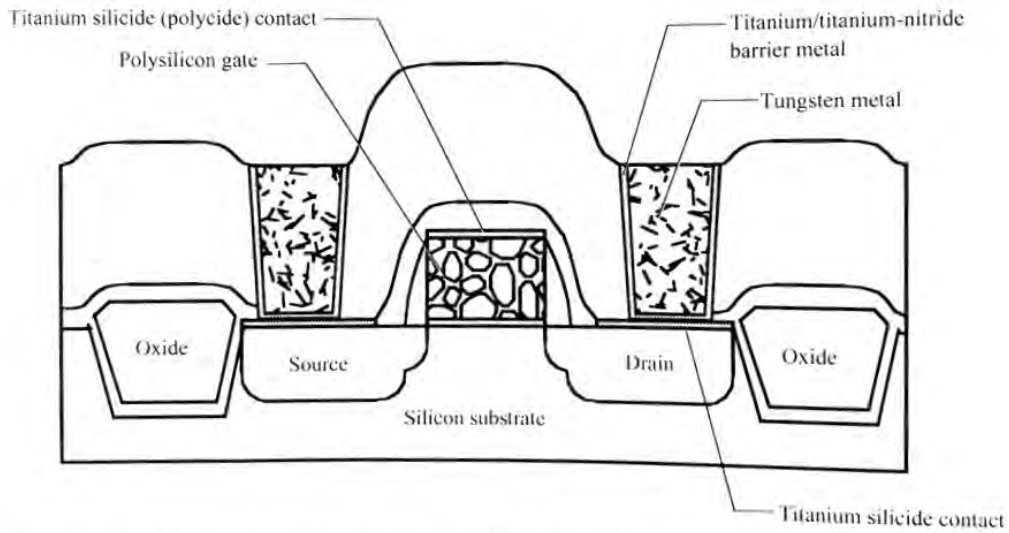


FIGURE 12.9 Refractory Metal Silicide at a Silicon Contact

88. As just one example, the 2000 textbook Semiconductor Manufacturing Technology[61] was "written for students in two and four-year technology programs at community colleges and universities"[62] and explains that "[r]efractory metals react with silicon when alloyed together to form a silicide."[63]

[61] M. Quirk & J. Serda, *Semiconductor Manufacturing Technology* (1st ed. 2000).

[62] *Id.* at Back Cover.

[63] *Id.* at 309.

"A silicide," the textbook explains, "is a metal compound that is thermally stable and provides for low electrical resistivity at the silicon/refractory metal interface (see Figure 12.9),"[64] as shown above.

89. A silicide is a metal compound formed by metalizing a silicon layer, such as at the top of the source/drain. This is accomplished by placing a metal layer (usually titanium, cobalt or nickel) on the silicon layer, then applying sufficient heat so the semiconductor atoms bond with the metal atoms. For instance, in the example shown in Figure 12.9 above from the textbook, a titanium metal layer is deposited on top of silicon source/drain regions. Next, heat is applied to form a silicide. The silicide in this example is titanium silicide (that is, a layer of silicon that has been metalized with titanium).[65]

90. This process did not change when the industry shifted to SiGe source/drain regions for pFET devices. For example, a person of ordinary skill in the art would have understood that "[m]etal semiconductor alloys such as metal silicides, metal germanides, metal germano-silicides reduce contact resistance between a metal structure such as a metal contact via structure and a semiconductor region such as a source region, a drain region, and a gate conductor

[64] *Id.* at 309; *see also id.* at 214-15, 309-13, Figs. 9.19-9.22, 12.9, 12.14.

[65] *See id.* at 214, Fig. 9.19.

line."[66] A person of ordinary skill in the art also would have understood that the same process that applied to silicon also applied to SiGe:

> Formation of metal semiconductor alloys requires an interdiffusion between a metal and a semiconductor material. Typically, the metal is provided as a metal layer, which is deposited after deposition of a dielectric material layer overlying a semiconductor layer and formation of holes within the dielectric material layer to expose the semiconductor material on the top surface of the semiconductor layer. The interface between the metal layer and the underlying semiconductor material is subjected to an anneal at an elevated temperature, typically from 400 degrees Celsius to 700 degrees Celsius, to effect the interdiffusion of the metal and the semiconductor material.[67]

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[66] *Haran* (US8358012) at 1:10-14; *see also id.* at Title, 1:7-25, 3:17-22; *Kim* ¶¶ [0003]-[0008], [0010], [0050], [0051], [0058], [0074]; *Tung* ¶¶ [0005], [0006], [0021], [0027], [0029]-[0032], [0034], [0039], [0061], [0070], [0078]; *Rhee* (US2008/0067545) ¶¶ [0021], [0024], [0025], [0042]; *Simonelli* (US2010/0148217) ¶¶ [0024], [0043]; *Murthy* (US6949482) at Abstract, 2:66-3:13, 8:34-9:63, Figs. 5-8; *Yasutake* (US2007/0187767) ¶¶ [0005], [0024], [0025], [0039]-[0045], [0050], [0066], [0070], [0086], [0093]; *Liu '953* (US2007/0122953) ¶¶ [0086], [0096]; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, pp. 222-231, at 226 (Mar. 2005).

[67] *Haran* (US8358012) at 1:10-25; *see also id.* at 10:38-11:12, Figs. 14-15; *Kim* ¶¶ [0047]-[0051], [0057], [0066], [0067]; *Tung* ¶¶ [0042]-[0045], [0063]-[0065], [0067], [0068], [0081]; *Rhee* (US2008/0067545) ¶ [0042], Fig. 7; *Simonelli* (US2010/0148217) ¶ [0043]; *Murthy* (US6949482) at 7:11-8:5, Figs. 4a-4c; *Yasutake* (US2007/0187767) ¶¶ [0024], [0036], [0050], [0066], [0080], [0093], Fig. 8; *Honeycutt* (US5644166) at 1:8-15, 4:46-53, 5:6-45, 7:20-43, 7:61-8:42; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 226 (Mar. 2005); S.

A person of ordinary skill in the art would have understood that it was routine in the semiconductor industry to apply this technique to MOSFET source/drain regions to lower Schottky barrier height and reduce contact resistance in SiGe pFETs.[68]

F. Stacking a Metal Plug on a Metal-Semiconductor Layer Was Almost Universal for Source/Drain Contacts in the Industry

91. A person of ordinary skill in the art would have understood that source/drain contacts are necessary for any FET device structure because, without them, the device would be unable to operate. A person of ordinary skill in the art also would have understood that omitting discussion or illustration of interlayer dielectrics, electrical contact structures, and related processes was typical when describing a transistor device structure itself. This can be commonly seen in many

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Gaudet et al., *Thin Film Reaction of Transition Metals with Germanium*, Journal of Vacuum Science & Technology A, vol. 24, no. 3 at 475-76, Fig. 5 (2006); S. Zaima & Y. Yasuda, *Study of Reaction and Electrical Properties at Ti/SiGe/Si(100) Contacts for Ultralarge Scale Integrated Applications*, Journal of Vacuum Science & Technology B, vol. 16, at 2625-27, Fig. 1 (1998) ("Silicon atoms preferentially react with Ti atoms at annealing temperatures below 300 °C and Ge atoms start to react above 400 °C.").

[68] *See, e.g.*, *Haran* (US8358012) at 1:10-25, 10:38-11:12, Figs. 14-15; *Kim* ¶¶ [0007], [0008], [0047]-[0051], [0057], [0066], [0067]; *Tung* ¶¶ [0005], [0042]-[0045], [0063]-[0065], [0067], [0068], [0081]; *Simonelli* (US2010/0148217) ¶ [0043]; *Murthy* (US6949482) at Abstract, 2:66-3:13, 7:11-8:5, 8:34-9:63, Figs. 4a-8; *Yasutake* (US2007/0187767) ¶¶ [0005], [0043]-[0045]; *Honeycutt* (US5644166) at 1:8-15.

exemplary prior-art patents and other publications.[69] For example, *Brask* explains the following when describing the figure below:

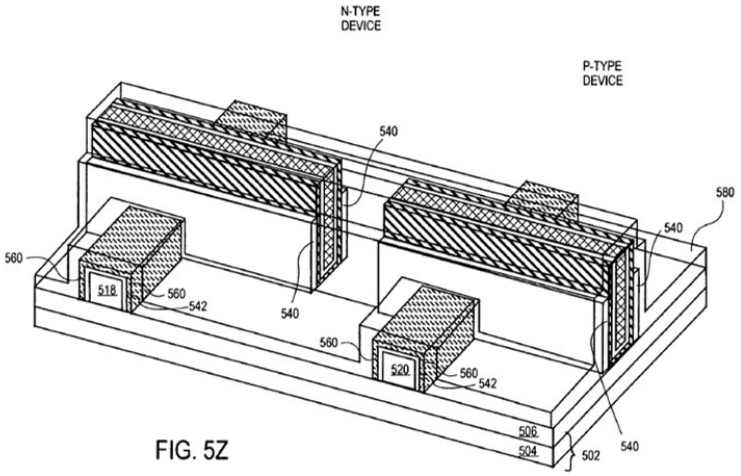


FIG. 5Z

> At this point, the fabrication of an n type and p type nonplanar device having a metal gate electrode and metal oxide dielectric films have been formed. Well known back end processing steps can now be utilized to interconnect the various p type and n type devices together into functional CMOS integrated circuits. The back end of the process includes formation of interlayer dielectric layers and metal interconnects.[70]

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[69] *See*, *e.g.*, *Yeh* (US9245805) at 4:43-48 ("Next, silicide/germanide regions (not shown) may be formed on source/drain regions 142 and 242 by reacting source/drain regions 142 and 242 with a metal(s) to reduce the contact resistances. The formation details of silicide/germanide regions are known in the art, and hence are not repeated herein."); *Tung* ¶¶ [0023] ("A contact (not shown) is disposed on the metal silicide layer 59."), [0036] (same), [0064] (same); *Simonelli* ¶ [0043] (explaining that "device 100 may undergo further MOS processing . . . that may further modify the device and/or provide the necessary electrical interconnections."); *Rhee* (US2008/0067545) ¶ [0018] ("The contact portion of the source/drain region may be in contact with a contact structure."), [0021] ("A contact structure configured to transmit an electrical signal to the source/drain region may be connected to the metal semiconductor compound layer 124 so as to be electrically connected.").

[70] *Brask* at 27:20-27; *see also id.* at Fig. 5Z.

92. As a baseline, the textbook process for forming source/drain contact structures in December 2010 involved the application of silicidation, paired Ti/TiN barrier metals and contact plugs. This technique was pervasive in the semiconductor industry long before December 2010. For example, the textbook from the year 2000 discussed in the previous section (Semiconductor Manufacturing Technology[71]) describes standard "Contact Formation" and "Local Interconnect" processes and structures below[72]:

	Process Step	Description
1.	Titanium Deposition	The wafer is cleaned thoroughly to remove contaminants and oxides from the silicon. Titanium (Ti) is deposited on wafers using a sputtering process. *Sputtering* is a *physical vapor deposition* (*PVD*) process that is performed in a plasma process chamber where energetic argon ions bombard a metal target to release metal atoms, which deposit onto a wafer.
2.	Anneal	The wafer is inserted in the RTP tool. The high temperature triggers a chemical reaction between titanium and silicon that forms $TiSi_2$ (tisilicide).
3.	Titanium Etch	Chemicals etch away the unreacted titanium, leaving behind tisilicide over the active silicon areas.

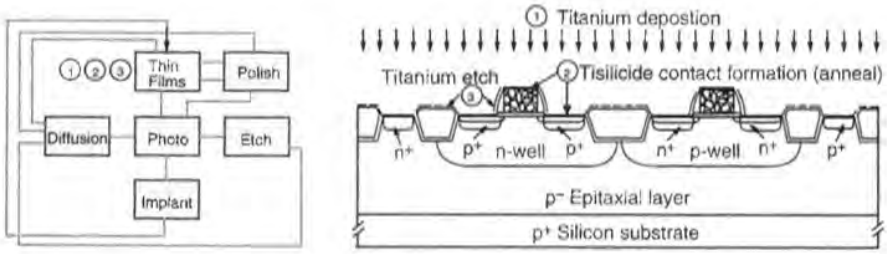


FIGURE 9.19 Contact Formation

[71] M. Quirk & J. Serda, *Semiconductor Manufacturing Technology* (1st ed. 2000).

[72] *Id.* at 214-15, 309-13, Figs. 9.19-9.22, 12.9, 12.14.

Description of LI Oxide Dielectric Formation

	Process Step	Description
1.	Nitride (Si_3N_4) CVD	A barrier layer of silicon nitride is deposited using a CVD process. The nitride provides protection for the active regions from the dopants in the next film layer.
2.	Doped Oxide CVD	The LI dielectric component of the local interconnect structure is formed from CVD oxide (SiO_2). This oxide is lightly doped with phosphorus or boron. The addition of dopants to the oxide improves the dielectric qualities of the glass. An additional RTP step allows the glass to flow and smooth the surface.
3.	Oxide Polish (CMP)	CMP is used to planarize the LI oxide. The resulting thickness of the oxide after polish is ~8000 Å.
4.	9th Mask, LI Etch	The wafer is patterned in photolithography and then etched in the etch bay. Narrow trenches are created in the LI oxide that will serve as the forms for defining the paths for the LI metal.

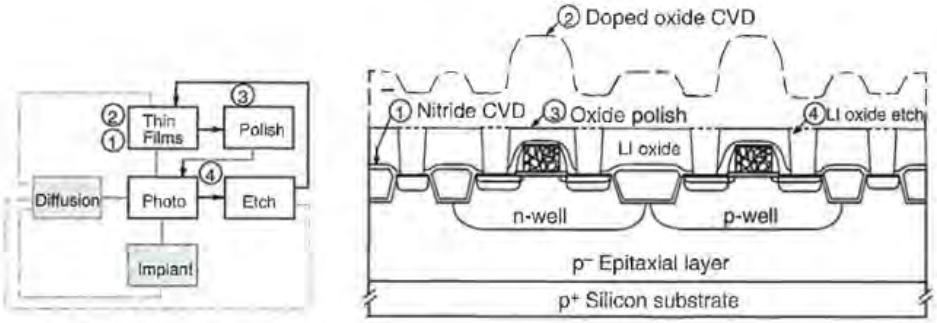


FIGURE 9.21 LI Oxide Dielectric Formation

Description of LI Metal Formation

	Process Step	Description
1.	Titanium Deposition (PVD process)	A thin barrier layer of titanium (Ti) lines the bottom and the inside of the LI walls. The Ti serves as a "double-adhesive tape" to hold the tungsten (W) to the SiO_2.
2.	Titanium Nitride Deposition	Titanium nitride (TiN) is deposited immediately over the Ti to serve as a diffusion barrier for the tungsten metal.
3.	Tungsten Deposition (CVD process polish)	Tungsten fills the LI trenches and coats the entire wafer. Tungsten is preferred over aluminum for LI metal due to its ability to fill holes without leaving voids in the formed metal plug. Another reason is for its good polishing characteristics.
4.	Tungsten polish	The tungsten is polished down to the upper surface of the LI oxide.

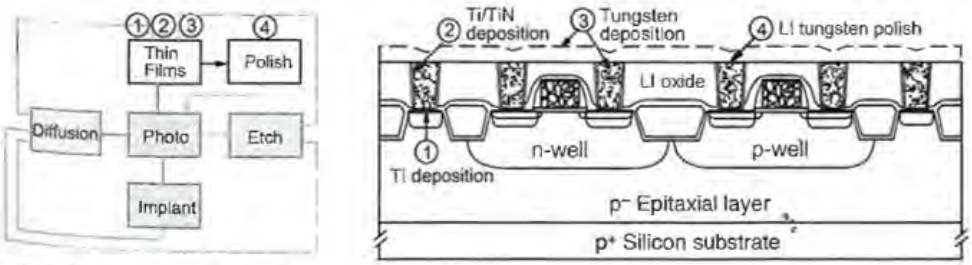


FIGURE 9.22 LI Metal Formation

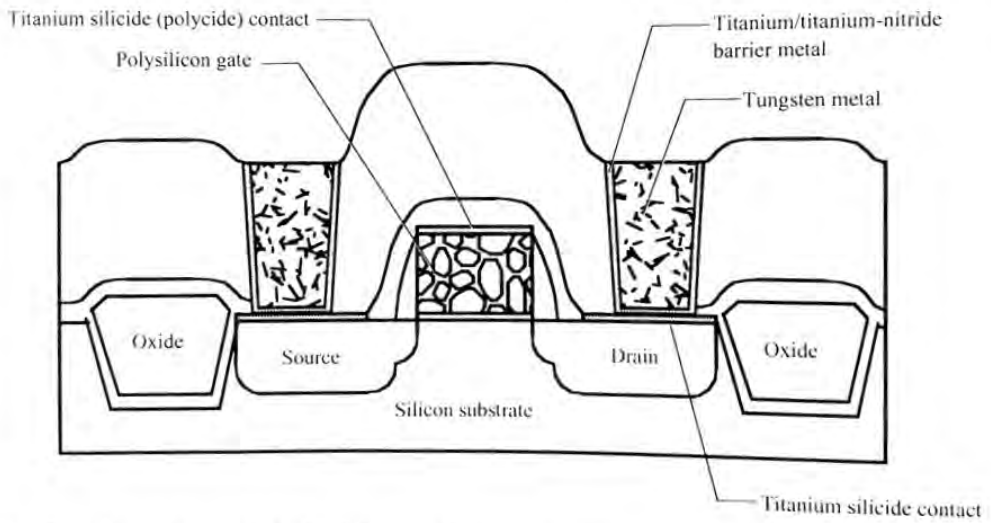


FIGURE 12.9 Refractory Metal Silicide at a Silicon Contact

93. A person of ordinary skill in the art would have had this standard process in mind as a baseline when reviewing any FET structure that omits the source/drain contact structure.

G. Characteristics of Epitaxial SiGe Source/Drain Regions Were Well Known

94. A person of ordinary skill in the art would have understood that epitaxially grown SiGe source/drain regions have either a diamond shape or a rectangular shape, depending on the wafer orientation. The figure below, from a textbook, illustrates this.[73]

[73] *FinFETs and Other Multi-Gate Transistors* at 90 & Fig. 2.37 (J.-P. Colinge ed., 2008); *see also id.* at 100 & Fig. 2.45; *Tung* ¶ [0058] ("Depending on the underlying layer (for example, silicon (100) surface versus silicon (110) versus germanium (100), etc.) and the material being deposited, the doped semiconductor layer 55 may form facets that may merge together or separate out."); K.-M. Tan et

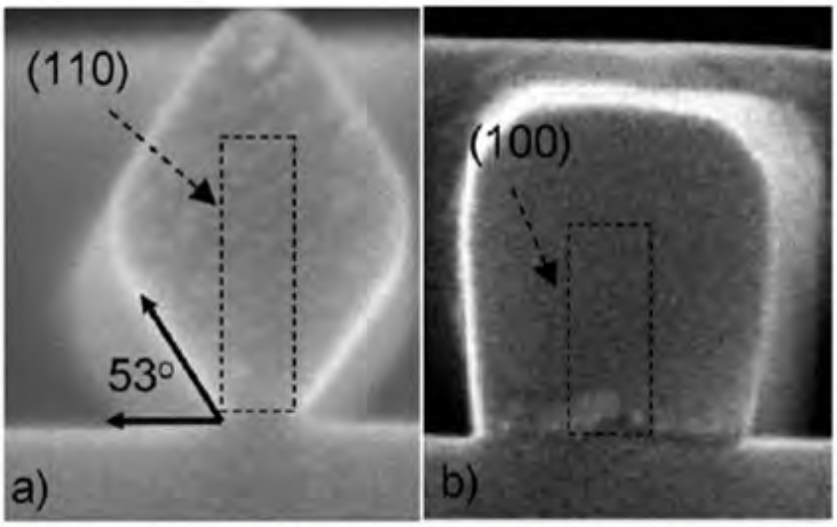


Fig. 2.37. Cross sectional SEM images on fins after epitaxial growth. a) (110) side wall surface result in diamond-shaped fin: b) (100) sidewall surface result in square-shaped fin.

95. A person of ordinary skill in the art also would have understood that, to be commercially viable, SiGe strain engineering requires "industry-standard Si wafers with (001) surface and wafer notch on the [110] axis."[74] This is because channel mobility is only meaningfully enhanced due to strain along the <110> transport plane (that is, with the fin aligned with the <110> Si crystal axis). As shown on the left below, there is "a 100% increase in hole mobility for the <110>

al., Π-*Shaped Silicon–Germanium Source and Drain Stressors*, IEEE Electron Device Letters, vol. 28, no. 10, at Fig. 1.

[74] S.E. Thompson et al., *A Logic Nanotechnology Featuring Strained-Silicon*, IEEE Electron Devices Letters, vol. 25, no. 4, at 192 (Apr. 2004); *see also* Y. Sun et al., *Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors*, Journal of Applied Physics, vol. 101, 104503, at 1 (2007) (noting that (100) surface-oriented Si wafers are "currently the case for all commercial technologies" and that channels oriented along the <110> direction is "generally" the case "for commercial technologies").

transport plane compared to a <100> planar device."[75] And for a FinFET oriented in this way, SiGe naturally grows in a diamond shape, as the figure on the right below confirms.[76]

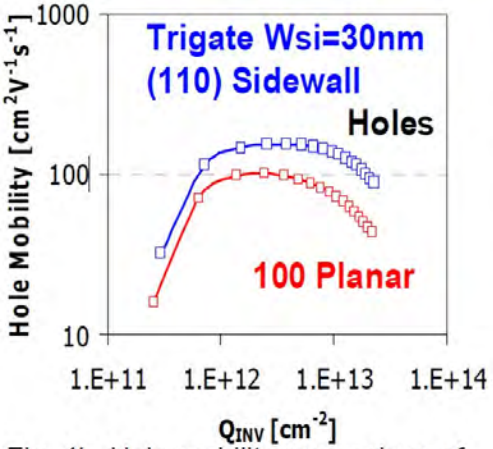


Fig. 4b Hole mobility comparison of a planar <100> vs. a Trigate <110> dominated device.

Kavalieros et al., Fig. 4b

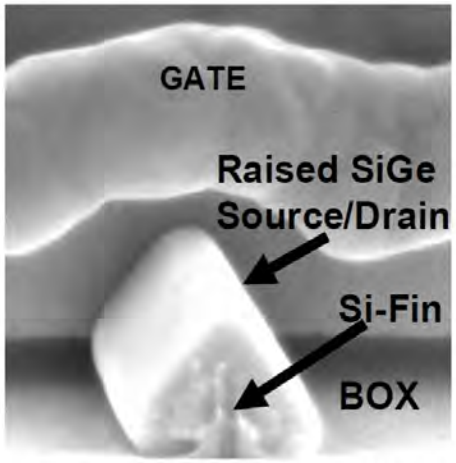


Fig. 7b Y-dir. cross-section of PMOS Trigate with SiGe raised source/drain

Kavalieros et al., Fig. 7b

96. A person of ordinary skill in the art would have understood that such epitaxial SiGe regions "naturally grow in a diamond shape."[77] As one reference explains, "epitaxially growing Si and SiGe facets cannot form a rectangular profile on a silicon substrate having a (001) crystallographic orientation with a notch

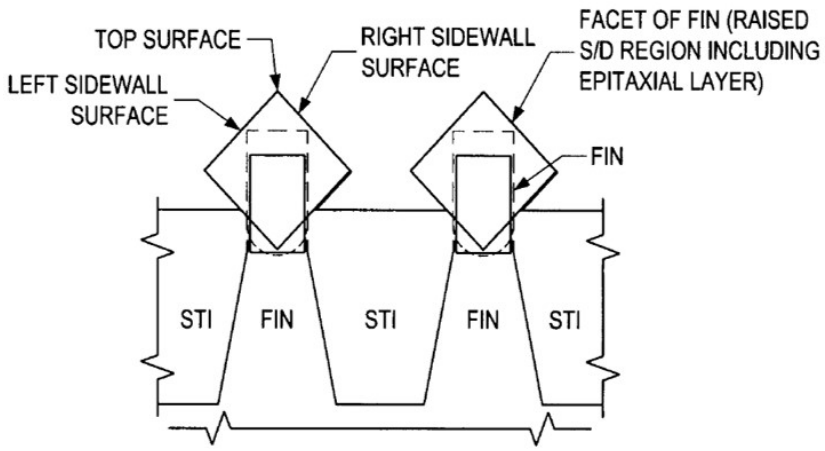
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[75] J. Kavalieros et al., *Tri-Gate Transistor Architecture With High-k Gate Dielectric Metal Gates and Strain Engineering*, 2006 IEEE Symposium on VLSI Technology Digest of Technical Papers, at 1, Fig. 4b (June 2006).

[76] *Id.* at Fig. 7b; *see also FinFETs and Other Multi-Gate Transistors* at 90 & Fig. 2.37 (J.-P. Colinge ed., 2008) ("For (110) sidewall surface, the faceting will result in a diamond shaped surface.").

[77] *Lin '894* (US8652894) at 5:43-45; *see also id.* at 1:27-43, 5:21-6:7, 7:42-50, 10:1-40, 10:61-66, 12:12-20, Fig. 5A; *Kwok* (US8362575) at 1:38-42, 2:39-41, 3:31-50, Figs. 1, 2A, 3-7.

aligned in a <110> direction."[78] Rather, "[w]hen the facets are grown on a silicon substrate having a (001) crystallographic plane orientation, the diamond shaped profile of FIG. 5A [below] may have a top (first) surface with a (001) crystal plane and right/left (second/third) sidewall surfaces with a (111) crystal plane."[79]



***Lin '894*, Fig. 5A**

97. Thus, a person of ordinary skill in the art would have understood that epitaxial SiGe source/drain regions grown using the industry-standard wafer orientation necessary for effective strain engineering naturally grow in a diamond shape.

[78] *Lin '894* (US8652894) at 5:29-32; *see also id.* at 10:9-13, Fig. 5A; *Kwok* (US8362575) at 1:38-42, Figs. 1, 2A, 3-7.

[79] *Lin '894* (US8652894) at 5:36-40; *see also id.* at 10:17-21, Fig. 5A; *Kwok* (US8362575) at 3:31-50, Figs. 1, 2A, 3-7; *Tung* ¶ [0058], Figs. 4b-4e.

VII. The ’281 Patent

A. A Description of the Claimed Embodiments of the ’281 Patent

98. The ’281 Patent is titled “Contact Resistance Reduction Employing Germanium Overlayer Pre-Contact Metalization.” As the title suggests, it is directed to the use of a Ge capping layer to reduce the Schottky barrier height of source/drain contact electrodes—the approach I describe in Section VI.C.

99. The specification describes the invention as a technique “for forming transistor devices having reduced parasitic contact resistance[80] relative to conventional devices.”[81] The technique involves the use of “an intermediate boron doped germanium layer [that] is provided between the source/drain and contact metals to significantly reduce contact resistance.”[82] The patent describes this as “a bilayer construction of boron doped silicon or SiGe (for the source/drain regions) capped with an overlayer of a boron doped germanium layer.”[83] According to the specification, this technique applies to “both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures.”[84]

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[80] The specification uses “parasitic contact resistance” to refer to “external resistance R_{ext},” which is dominated by the contact resistance R_C. ’281 Patent at 1:30-37.

[81] ’281 Patent at 2:22-24.

[82] *Id.* at 2:27-30.

[83] *Id.* at 3:51-57.

[84] *Id.* at 2:30-34; *see also id.* at 3:10-17, 4:59-5:7.

100. The ’281 Patent expressly distinguishes the invention from the prior art based on the addition of a Ge capping layer:

> A standard transistor contact stack typically includes, for example, a silicon or SiGe source/drain layer, a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad. In such configurations, the contact resistance is effectively limited by the silicon or SiGe valence band alignment to the pinning level in the metal. Typically, using industry standard silicides such as nickel (or other suitable silicides, such as titanium, cobalt, or platinum), this results in a band misalignment of about 0.5 eV. Thus, and in accordance with an example embodiment of the present invention, **an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce the band misalignment value**.
>
> In one specific example embodiment, contacts configured with the intermediate boron doped germanium layer exhibit a reduction in the band misalignment value to less than 0.2 eV and a corresponding reduction in contact resistance of about 3x (**relative to a conventional contact stack similarly configured, but without the intermediate boron doped germanium layer between the source/drain regions and contact metal**).[85]

According to the specification, this approach purports to “marry superior contact properties of germanium with superior semiconductor transistor properties of Si and SiGe to provide next generation low resistance contacts.”[86] “In any such implementations” of the invention, the patent explains that “an overlayer or cap of

[85] *Id.* at 2:43-56.

[86] *Id.* at 3:6-9.

boron doped germanium can be formed directly over the source/drain regions" and that a "contact metal (or series of metals) can then be deposited and a subsequent reaction (annealing) can be carried out to form metal germanide source and drain contacts."[87]

101. By contrasting "standard transistors configured with no cap" and "transistor structures configured with in accordance with embodiments of the present invention," Figure 7 of the specification, reproduced below, also underscores the fact that the invention centers on the germanium capping layer, which is what allegedly distinguishes the invention over the prior art.[88]

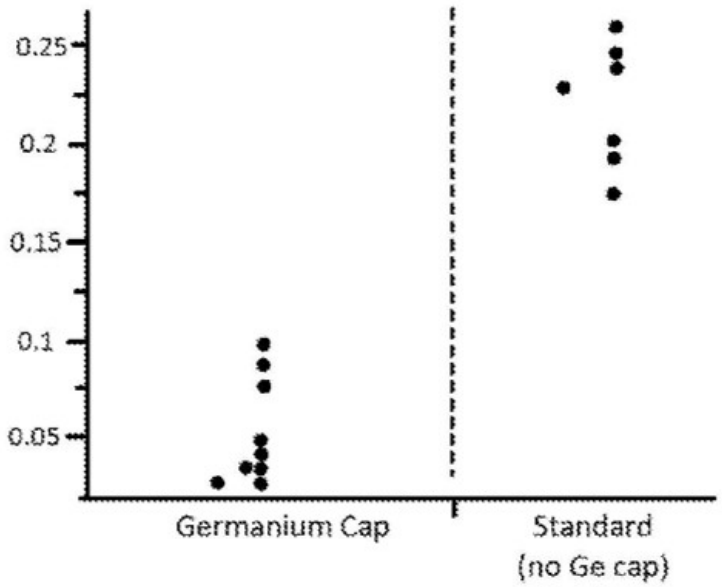


FIG. 7

[87] *Id.* at 3:24-30.

[88] *Id.* at 14:15-18.

102. "The transistor structures associated with the high resistance numbers in excess of 0.18 are all implemented with standard SiGe alloy raised PMOS source/drain regions with contact metal deposited directly thereon," whereas "[t]he transistor structures associated with the resistance numbers of 0.107 and lower are all similarly implemented but with the addition a boron doped germanium cap between the source/drain regions and contact metal, in accordance with various embodiments of the present invention."[89] The specification attributes this improvement to the basic physics of the germanium capping layer:

> Other improvements enabled by using a boron doped germanium cap in accordance with an embodiment of the present invention will be apparent in light of this disclosure. In particular, the resulting germanide materials and Schottky barrier height improvement enables more than a 2× R_{ext} improvement over that in conventional SiGe source/drain PMOS devices, in accordance with some example embodiments of the present invention. As is known, the Schottky barrier height is the barrier for electrical conduction across a semiconductor-metal junction. The magnitude of the Schottky barrier height reflects a mismatch in the energy position of the metal's Fermi level and the majority carrier band edge of the semiconductor across the semiconductor-metal interface. For a p-type semiconductor-metal interface, the Schottky barrier height is the difference between the metal Fermi level and the valence band maximum of the semiconductor.[90]

[89] *Id.* at 14:18-27.

[90] *Id.* at 14:41-57; *see also id.* at 10:53-11:3.

103. The figure below illustrates one example of the invention contemplated by the inventors.

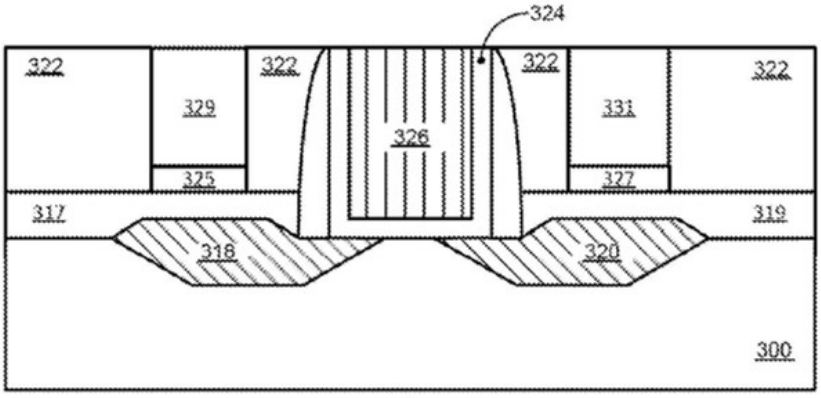


FIG. 3I

104. As the figure above shows, a typical transistor structure is formed on a Si or SiGe substrate 300.[91] After forming a gate stack, a recess etch in substrate 300 defines cavities for growing epitaxial source/drain regions 318 and 320.[92] Boron-doped SiGe source/drain regions 318 and 320 are then grown in the cavities.[93] According to the specification, these source/drain regions "can be formed using any number of conventional techniques," such as "by etching the substrate and then epitaxially depositing a silicon or silicon germanium material (e.g., with a germanium concentration in the range of, for instance, 10 to 70

[91] *See id.* at 6:11-20, 8:43-44. The specification also mentions other options, such as Ge or III-V semiconductors, but subsequent descriptions would be illogical if the substrate 300 in the preferred embodiments were not Si or low-Ge content SiGe for pFETs.

[92] *See* '281 Patent at 7:55-9:12, Fig. 3A.

[93] *See id.* at 9:12-26, Fig. 3B.

atomic %)."[94] The source/drain regions may have a graded Ge concentration and/or a graded boron doping profile.[95]

105. Next, boron doped germanium layers 317 and 319 are deposited directly on source/drain regions 318 and 320.[96] According to the patent, a nominal "germanium layer" is one with at least 90 atomic % germanium:

> In some example embodiments, the boron doped germanium layer 317/319, which may be epitaxially deposited in one or more layers, has a germanium concentration in excess of 90 atomic %, although other suitable concentration levels can be used as will be appreciated in light of this disclosure (e.g., in excess of 91 atomic %, or 92 atomic %, . . . , or 98 atomic %, or 99 atomic %, or truly pure germanium). As previously explained, this germanium concentration may be fixed or graded so as to increase from a base level (near substrate 300) to a high level (e.g., in excess of 90 atomic %).[97]

The specification similarly refers to "nominally pure germanium films" as "those with less than 10% silicon").[98]

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[94] *Id.* at 4:27-34.

[95] *Id.* at 4:6-9, 6:48-62, 14:7-10, 16:52-62, 17:46-56.

[96] *See id.* at 9:41-45, Fig. 3C.

[97] *Id.* at 9:45-55. This accords with my discussion of the SiGe band structure in Section VI.C above, which requires at least about 85 atomic % Ge before meaningful reduction in Schottky barrier height can be obtained. This is why every description of every embodiment in the '281 Patent underscores the fact that the boron doped "germanium layer" has at least 90 atomic % Ge. *See, e.g.*, *id.* at 7:11-20, 9:45-55, 10:53-11:3, 12:31-41, 16:26-29, 16:52-57, 17:4-7, 17:29-33, 17:46-52, 18:16-18.

[98] '281 Patent at 3:19-27.

106. After forming the boron doped germanium capping layers 317 and 319 over the source/drain regions 318 and 320, a standard interlevel dielectric ("ILD") layer 322 is deposited over the device, which can be SiO_2 or a standard combination of low-k dielectrics.[99] After optionally forming a replacement gate with a high-k gate dielectric layer 324 and metal gate electrode layer 326,[100] typical contact trenches are etched into ILD layer 322 above the source/drain regions.[101]

107. Next, a standard salicide (self-aligned silicide) process is performed by depositing a "contact resistance reducing metal and annealing to form silicide/germanide" layers 325/327, followed by deposition of standard contact plugs 329/311 "using conventional deposition processes."[102] The specification explains: "The germanide/metalization 212 of the source and drain contacts can be carried out, for instance, by silicidation with nickel, aluminum, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants to form a low resistance germanide."[103] "The boron doped germanium layer 317/319 allows for metal-germanide formation," which the patent claims to "significantly lower Schottky-

[99] *Id.* at 11:4-24, Fig. 3D.

[100] *Id.* at 11:25-59, Figs. 3E, 3F.

[101] *Id.* at 11:60-66, Fig. 3G.

[102] *Id.* at 11:66-12:11; *see also id.* at Figs. 3H, 3I.

[103] *Id.* at 12:11-17.

barrier height and improved contact resistance (including R_{ext}) over that in conventional metal-silicide systems."[104]

108. The specification also describes a similar embodiment, shown in Figure 5F below, which is formed using a method "similar to the method described" for Figure 3I above, "except that the deposition of the boron doped germanium layer 317/319 on the source/drain regions is carried out after the dielectric 322 is deposited and etched to form the contact trench."[105] "This alternate methodology," the patent states, "provides the same benefit of improved contact resistance."[106]

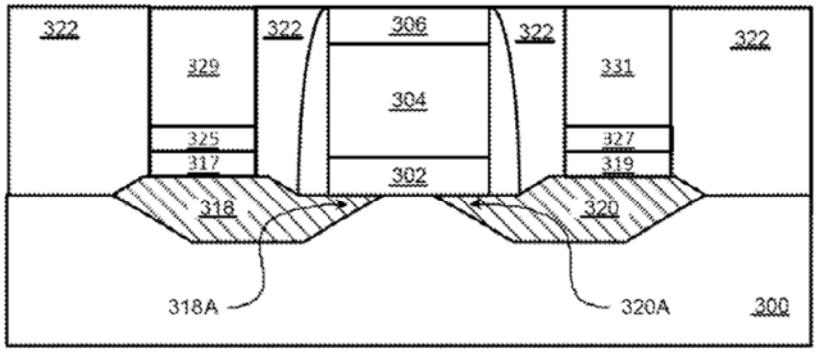


FIG. 5F

109. Although the patent makes clear that the invention can be used with both planar FETs and FinFETs,[107] the specification briefly describes a FinFET

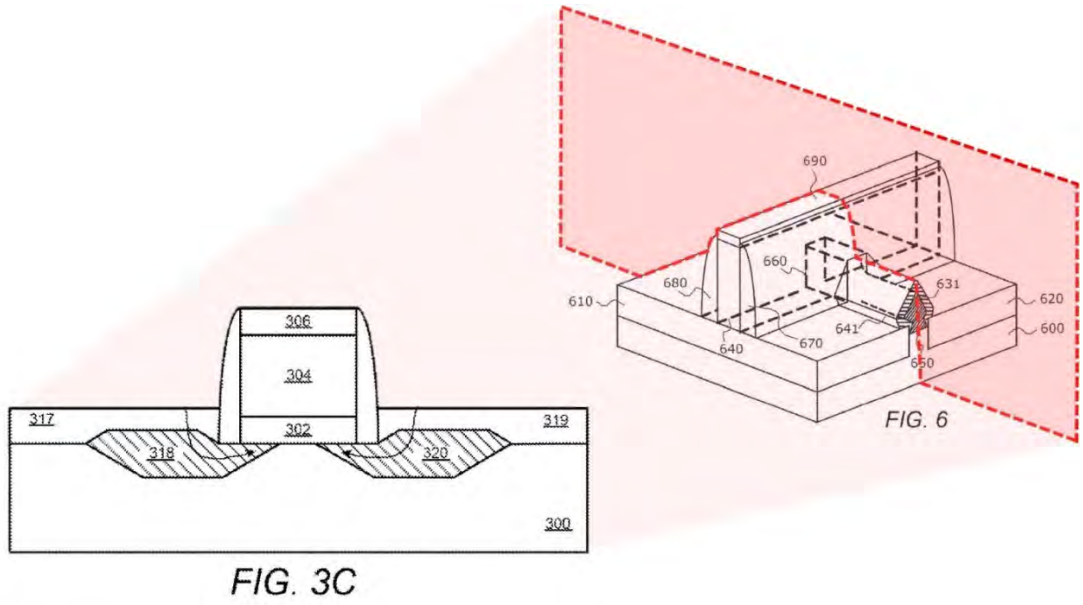
[104] *Id.* at 12:17-22.

[105] *Id.* at 12:46-51.

[106] *Id.* at 12:62-64.

[107] *Id.* at Abstract, 2:30-34, 3:10-14, 9:3-8, 16:28-32.

embodiment as well.[108] I arranged the figures below to show how the FinFET embodiment corresponds to an intermediate structure related to the cross-section from Figure 3 discussed above.



110. After describing the well-known structure of a typical FinFET,[109] the '281 Patent describes Figure 6, which I have reproduced on the right above with annotations. Similar to the cross-section shown in Figure 3C on the left above, Figure 6 depicts a FinFET prior to ILD formation and subsequent processes. Substrate 600 corresponds to substrate 300.[110] Shallow trench isolation (STI) regions 610 and 620 do not exist in the cross-section corresponding to Figure 3C, but such isolation regions were conventional and used in virtually all (if not all)

[108] *See id.* at 13:14-14:14, Fig. 6.

[109] *See id.* at 13:14-32.

[110] *See id.* at 13:58-61.

integrated circuits to separate adjacent FETs.[111] Gate electrode 640, gate spacers 670/680, and hard mask 690 correspond to sacrificial gate electrode 304, spacers 310 (not labeled in Figure 3C), and hard mask 306, respectively.[112] Epitaxial regions 631 correspond to source/drain regions 318 and 320.[113] And cap layer 641 corresponds to boron doped germanium layers 317/319.[114]

111. The FinFET in Figure 6 employs the very same source/drain structure and germanium capping layer as I describe above regarding the structure shown in Figures 3I and 5F:

> [T]he bilayer structure of the epitaxial region 631 and cap layer 641 can be implemented, for instance, using an in situ doped silicon or SiGe (for 631) capped with a boron doped germanium (for 641), with an optional germanium and/or boron graded buffer between the two bilayers. As previously explained, such a buffer may be used to transition from a base level germanium/boron concentration compatible with the epitaxial region 631 to the boron doped germanium cap 641. Alternatively, germanium and/or boron concentration grading can be implemented directly in the epitaxial region 631 and/or the cap 641, rather than in an intervening graded buffer arrangement.[115]

[111] *See id.* at 13:51-58.

[112] *See id.* at 13:40-42.

[113] *See id.* at 13:43-47.

[114] *See id.* at 13:64-14:3.

[115] *Id.* at 13:64-14:10.

112. The specification concludes by describing generic consumer electronics devices, such as personal computers, smartphones, and the like,[116] and then lists specific examples of various embodiments without giving them any particular significance.[117]

B. Challenged Claims and Prosecution History

113. Based on my review of the prosecution file history for the '281 Patent, I understand that the Examiner allowed the claims without making any rejections or raising any substantive issues.

114. Independent claim 1 is best understood with reference to the embodiments described in Figures 3I, 5F, and 6. It recites a FinFET with first and second SiGe source/drain regions, each of which has "a germanium concentration graded to a concentration in excess of 50%." "[O]ver the portion of the first source or drain region" is a "germanide layer comprising silicon, germanium, and titanium"[118]:

> **1**. An integrated circuit structure, comprising:
>
> a fin [660] comprising silicon;

[116] *See id.* at 14:59-16:15.

[117] *See id.* at 16:16-18:29.

[118] I have added the bracketed numbers to claim 1 to illustrate how each of the claimed features relates to the annotated figures below.

a gate electrode [304/326/640] over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;

a first dielectric spacer [310/670/680] along the first side of the gate electrode;

a first source or drain region [318/320/631] in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a second dielectric spacer [310/670/680] along the second side of the gate electrode;

a second source or drain region [318/320/631] in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a dielectric layer [322] over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;

a first germanide layer [325/327] in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second germanide layer [325/327] in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;

a first contact plug [329/331] in the first opening and on the first germanide layer; and

a second contact plug [329/331] in the second opening and on the second germanide layer.[119]

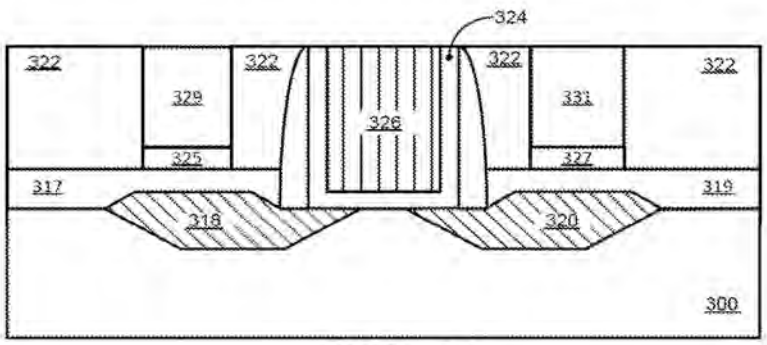


FIG. 3I

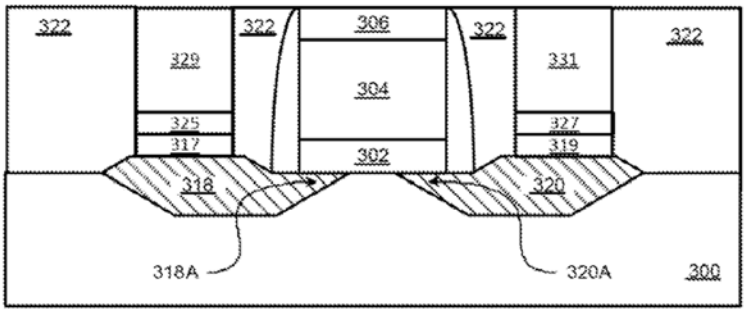


FIG. 5F

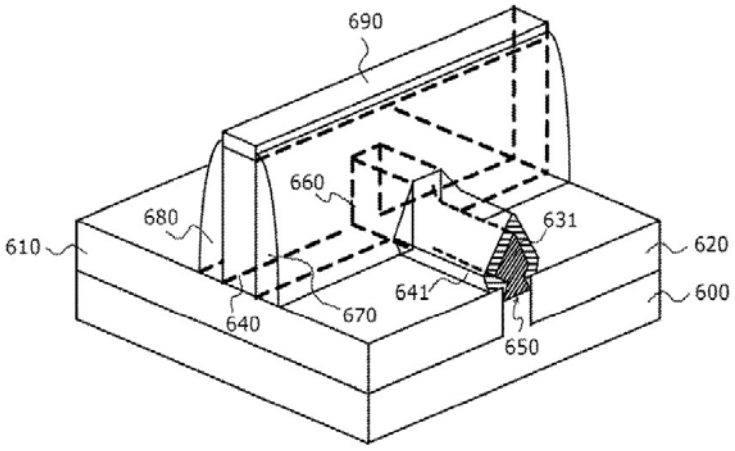


FIG. 6

[119] '281 Patent at 18:40-19:12.

115. Independent claim 8 is similar, except it recites a "body" rather than a "fin." The '281 Patent uses the term "body" only once, equating it with a fin: "As can be seen, the tri-gate device includes a substrate 600 having a semiconductor body or fin 660 (represented by dashed lines) extending from the substrate 600 through isolation regions 610, 620."[120] It is therefore unclear how, if at all, claim 8 differs from claim 1.

116. Dependent claim 5, which depends from claim 1, recites an isolation region.[121]

117. Dependent claim 6, which depends from claim 1, recites a high-k gate dielectric and metal gate electrode.[122]

118. Dependent claim 7, which depends from claim 1, recites that each of the first and second source or drain regions "comprises two or more facets."[123]

119. Independent claim 12 is directed to Figure 8 of the '281 Patent and recites a "computing device" with "a board" and "a component coupled to the board" that includes the same integrated circuit structure recited in claim 1.[124]

[120] *See, e.g.*, *id.* at 13:35-38, Fig. 6.

[121] *Id.* at 19:40-46.

[122] *Id.* at 19:47-52.

[123] *Id.* at 19:53-56.

[124] *Id.* at 20:58-22:4.

120. Dependent claims 13 through 19 recite various standard components of computing devices (e.g., personal computers and smartphones), such as a memory, a communications chip, a camera, a battery, an antenna, a packaged integrated circuit die, a processor, and a DSP.[125] Dependent claim 20 recites that the computing device is a mobile phone, laptop, desk top computer, server, or set-top box.[126]

C. Listing of the Challenged Claims and Claim Language

121. For convenience, the Challenged Claims are reproduced in full below:

Claim	Claim Language
1	An integrated circuit structure, comprising: a fin comprising silicon; a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side; a first dielectric spacer along the first side of the gate electrode; a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; a second dielectric spacer along the second side of the gate electrode;

[125] *Id.* at 22:5-25.

[126] *Id.* at 22:26-29.

Claim	Claim Language
	a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region; a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium; a first contact plug in the first opening and on the first germanide layer; and a second contact plug in the second opening and on the second germanide layer.
5	The integrated circuit structure of claim 1, further comprising: an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region.
6	The integrated circuit structure of claim 1, further comprising: a gate dielectric layer, wherein the gate electrode is on the gate dielectric layer, wherein the gate dielectric layer comprises a high-k dielectric material, and wherein the gate electrode comprises a metal layer.

Claim	Claim Language
7	The integrated circuit structure of claim 1, wherein the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets.
8	An integrated circuit structure, comprising: a body comprising silicon; a gate electrode over the body, the gate electrode having a first side, and the gate electrode having a second side opposite the first side; a first dielectric spacer along the first side of the gate electrode; a first source or drain region in the body proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; a second dielectric spacer along the second side of the gate electrode; a second source or drain region in the body proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region; a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;

Claim	Claim Language
	a first contact plug in the first opening and on the first germanide layer; and a second contact plug in the second opening and on the second germanide layer.
12	A computing device, comprising: a board; and a component coupled to the board, the component including an integrated circuit structure, comprising: a fin comprising silicon; a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side; a first dielectric spacer along the first side of the gate electrode; a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; a second dielectric spacer along the second side of the gate electrode; a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;

Claim	Claim Language
	a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium; a first contact plug in the first opening and on the first germanide layer; and a second contact plug in the second opening and on the second germanide layer.
13	The computing device of claim 12, further comprising: a memory coupled to the board.
14	The computing device of claim 12, further comprising: a communication chip coupled to the board.
15	The computing device of claim 12, further comprising: a camera coupled to the board.
16	The computing device of claim 12, further comprising: a battery coupled to the board.
17	The computing device of claim 12, further comprising: an antenna coupled to the board.
18	The computing device of claim 12, wherein the component is a packaged integrated circuit die.
19	The computing device of claim 12, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.
20	The computing device of claim 12, wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box.

D. Claim Construction

122. I have been told that claim terms are construed with the meanings they would have to a person of ordinary skill in the art in the context of the patent document. In my analysis of the Challenged Claims, I have therefore applied the meanings of the claim terms as understood by a person of ordinary skill in the art in the context of the asserted patent and asserted claims.

123. I have reviewed the Updated Joint Proposed Claim Construction Chart submitted by the parties in the ITC Investigation, and I understand that only one term from the ’281 Patent is in dispute: “germanide layer.” For purposes of this declaration, I believe it is appropriate to affirmatively address the meaning of just that term.

124. After reviewing the parties’ Updated Joint Proposed Claim Construction Chart and considering the plain and ordinary meaning a person of ordinary skill in the art would have given “germanide layer” in the context of the ’281 Patent and Challenged Claims, I agree with the construction proposed by TSMC and the ITC’s investigative staff attorney: “germanium layer metalized with one or more metals.”

125. In semiconductor processing, “silicidation” generally refers to the process of depositing a metal onto a semiconductor layer and annealing the structure to induce a chemical reaction between the semiconductor atoms and

metal atoms. Silicide technology began in the 1980s, became popular in the 1990s, and was standard by the 2000s. In the 1980s and 1990s when silicide technology began, the source/drain regions were silicon, and the resulting "silicides" were metal-silicon compounds. When SiGe strain engineering exploded in the 2000s, many people kept using the term "silicide" to generically refer to the metal-semiconductor compound that results from performing the same process on SiGe source/drain regions.

126. Unlike the term "silicide," the term "germanide" is specific. For example, the term "germanide" has been used—as it is used in the context of the '281 Patent—to describe the metal-germanium compound that results from performing the "silicidation" process on a germanium layer (i.e., a layer of germanium metalized with one or more metals).[127]

127. The '281 Patent explains that a "germanide layer" is what results from metalizing a layer of germanium (in other words, making a layer of germanium metallic by chemically reacting it with a metal via annealing). In fact, the title of

[127] *See Yasutake* ¶ [0045] (contrasting "the conventional technology where the silicide film is formed on the silicon layer or the silicon germanium layer" with the situation where a "germanide layer is formed on the germanium layer"); *Rim* (US2007/0123042) at Abstract, ¶¶ [0004] (explaining a germanide can be formed by using the "salicide process when a metal or metal alloy is formed on a Ge surface"), [0022] (defining "Si-containing materials" to include "Si" and "SiGe"), [0024] (referring to a metal "capable of reacting with a Si-containing material or Ge in forming a silicide or germanide, respectively").

the patent is "Contact Resistance Reduction Employing **Germanium Overlayer Pre-Contact Metalization**." The specification also attributes the formation of "germanide" to metalization of a germanium overlayer:

> The **germanide/metalization** 212 of the source and drain contacts can be carried out, for instance, by silicidation with nickel, aluminum, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants **to form a low resistance germanide**. **The boron doped germanium layer 317/319 allows for metal-germanide formation** (e.g., nickel-germanium). The germanide allows for significantly lower Schottky-barrier height and improved contact resistance (including R_{ext}) over that in conventional metal-silicide systems.[128]

The specification reiterates this point—i.e., that a "germanide layer" results from metalizing a germanium cap layer and not a "conventional SiGe" surface:

> Other **improvements enabled by using a boron doped germanium cap** in accordance with an embodiment of the present invention will be apparent in light of this disclosure. **In particular, the resulting germanide materials and Schottky barrier height improvement enables more than a 2× R_{ext} improvement over that in conventional SiGe source/drain PMOS devices**, in accordance with some example embodiments of the present invention.[129]

[128] '281 Patent at 12:11-22.

[129] *Id.* at 14:41-48.

Additionally, a person of ordinary skill in the art would have understood that the specification distinguishes a "germanide" from "industry standard silicides" based on the use of a germanium layer to form the metal-semiconductor compound:

> A **standard transistor contact stack** typically includes, for example, a silicon or SiGe source/drain layer, a nickel **silicide layer**, a titanium nitride adhesion layer, and a tungsten contact/pad. In such configurations, the contact resistance is effectively limited by the silicon or SiGe valence band alignment to the pinning level in the metal. Typically, using **industry standard silicides** such as nickel (or other suitable silicides, such as titanium, cobalt, or platinum), this results in a **band misalignment of about 0.5 eV**. Thus, and in accordance with an example embodiment of the present invention, **an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce the band misalignment value** and contact resistance.
>
> In one specific example embodiment, contacts configured with the **intermediate boron doped germanium layer exhibit a reduction in the band misalignment** value to **less than 0.2 eV** and a corresponding reduction in contact resistance of about 3× (**relative to a conventional contact stack similarly configured, but without the intermediate boron doped germanium layer** between the source/drain regions and contact metal).[130]

[130] *Id.* at 2:43-64; *see also* Murthy (US6949482) at 2:66-3:9 (two of the named inventors of the '281 Patent referring to a "nickel silicon germanium ***silicide***" (not "nickel germanide") formed by metalizing SiGe source/drain regions without a Ge overlayer); *Yasutake* ¶ 0045 (drawing a distinction between "the conventional technology where the silicide film is formed on the ***silicon layer*** or the ***silicon germanium layer***" with a "germanide layer … formed on the ***germanium layer***").

Additionally, the title, abstract, and every embodiment characterizes the invention as providing a germanium layer on the source/drain region and metalizing it to form a germanide layer.[131]

128. Thus, consistent with how the terms "silicide" and "germanide" have been used in the industry, the specification of the '281 Patent makes clear that the term "germanide layer" means a "germanium layer metalized with one or more metals."

129. Again, a nominally "germanium" layer does not need to be pure germanium because it may have a small amount of impurities. As I explain in Section VII.A above, the specification of the '281 Patent describes a "germanium layer" as a layer of material with at least 90 atomic % germanium:

> In some example embodiments, the boron doped germanium layer 317/319, which may be epitaxially deposited in one or more layers, has a germanium concentration in excess of 90 atomic %, although other suitable concentration levels can be used as will be appreciated in light of this disclosure (e.g., in excess of 91 atomic %, or 92 atomic %, . . . , or 98 atomic %, or 99 atomic %, or truly pure germanium). As previously explained, this germanium concentration may be fixed or

[131] *See id.* at Title, Abstract, 1:41-44, 1:45-48, 1:49-52, 2:27-30, 2:38-64, 3:24-26, 3:33-36, 3:51-57, 3:62-65, 4:3-9, 4:23-27, 4:65-67, 5:8-13, 5:29-33, 5:59-63, 6:20-25, 6:51-57, 6:63-65, 7:11-20, 7:32-36, 9:27-30, 9:33-39, 9:44-55, 9:60-65, 10:4-7, 10:43-49, 10:53-11:6, 11:60-12:2, 12:17-22, 12:31-41, 12:44-58, 13:64-14:3, 14:15-27, 14:41-48, 16:24-31, 16:34-57, 16:62-17:7, 17:29-33, 17:35-52, 17:56-67, 18:16-20, 18:24-27.

> graded so as to increase from a base level (near substrate 300) to a high level (e.g., in excess of 90 atomic %).[132]

The specification also refers to "nominally pure germanium films" as "those with less than 10% silicon").[133] And during prosecution of a foreign relative of the '281 Patent, Intel stated:

> It is clear that according to the invention the source/drain regions comprise a heavily doped germanium layer. More specifically, **there is a germanium layer that is "pure", that is, close to 100% (ie over 90% according to the specification)**. This can be achieved according to embodiments **either by a layered approach (eg SiGe layer topped by germanium layer) or by a graded approach (eg SiGe graded up to 90% or more Germanium)**. **In the latter case, the overall average concentration of Germanium may be 50% or more, but it comprises a layer where the germanium concentration is over 90%**.
>
> * * *
>
> **D1 [US 2005/130454 A1 to Murthy et al.] discloses a transistor having source and drain regions of SiGe**. . . . The preferred range is 10-40% germanium. In the specific embodiment given in paragraphs [0032] to [0035], **silicon germanium is used**. **This is not pure germanium** . . . . Furthermore, the source and drain regions of D1 are not

[132] *Id.* at 9:45-55. This accords with my discussion of the SiGe band structure in Section VI.C, which shows at least about 85 atomic % Ge is needed before a meaningful reduction in Schottky barrier height occurs. Since that is the alleged benefit of the invention, every description of every embodiment underscores the fact that the boron doped "germanium layer" has at least 90 atomic % Ge. *See id.* at 7:11-20, 9:45-55, 10:53-11:3, 12:31-41, 16:26-29, 16:52-57, 17:4-7, 17:29-33, 17:46-52, 18:16-18.

[133] '281 Patent at 3:19-27.

> graded or layered. D1 does not disclose a graded or layered structure resulting in a high purity upper germanium layer, which is highly doped with boron.[134]

These statements affirm the notion that a "germanium layer" is "close to 100% (ie over 90% according to the specification)" and that a SiGe layer without a germanium content "close to 100%" is not a "germanium layer." A person of ordinary skill in the art would have understood that metalizing such a germanium layer creates a "germanide layer."

130. I understand, however, that the Patent Owner has argued "germanide layer" should be construed more broadly as "thickness of material, comprising germanium and a metal." I disagree that a person of ordinary skill in the art would have interpreted the '281 Patent claims in such a way for three main reasons.

131. First, the Patent Owner's proposed construction does not require a metalization layer, by which I mean a layer that has been made metallic via chemical bonding between metal and semiconductor atoms in that layer. The mere presence of germanium and metal in the same layer, regardless of whether metalization occurs, would suffice under the Patent Owner's proposed construction. Such a layer would undermine the very purpose of the invention and raise, not lower, the contact resistance.

[134] Amendment to European Patent Application No. 11851579.0 at 1-2 (June 23, 2015). I have been told that this application was never allowed to issue as a patent.

132. Second, any amount of germanium in the layer, no matter how small, would suffice under the Patent Owner's proposed construction. This would fail to achieve the purported benefits of the patent (reduction of contact resistance and Schottky barrier lowering) and read on "industry standard silicides" formed by metalizing SiGe layers "without the intermediate boron doped germanium layer between the source/drain regions and contact metal."[135]

133. Third, the invention centers around the germanium layer and its metalization to lower the Schottky barrier height and thereby reduce contact resistance. Every description of every embodiment hinges on it.[136] The Patent Owner's proposed construction, however, would eliminate this fundamental feature of the invention and result in a structure not described anywhere in the specification.

134. It is therefore my opinion that the Patent Owner's proposed construction of "germanide layer" (i.e., "thickness of material, comprising

[135] '281 Patent at 2:43-56; *see also id.* at 3:6-9, 3:24-30, 10:53-11:3, 14:15-27, 14:41-57, Fig. 7.

[136] *See id.* at Title, Abstract, 1:41-44, 1:45-48, 1:49-52, 2:27-30, 2:38-64, 3:24-26, 3:33-36, 3:51-57, 3:62-65, 4:3-9, 4:23-27, 4:65-67, 5:8-13, 5:29-33, 5:59-63, 6:20-25, 6:51-57, 6:63-65, 7:11-20, 7:32-36, 9:27-30, 9:33-39, 9:44-55, 9:60-65, 10:4-7, 10:43-49, 10:53-11:6, 11:60-12:2, 12:17-22, 12:31-41, 12:44-58, 13:64-14:3, 14:15-27, 14:41-48, 16:24-31, 16:34-57, 16:62-17:7, 17:29-33, 17:35-52, 17:56-67, 18:16-20, 18:24-27.

germanium and a metal") is too broad and does not naturally align with how a person of ordinary skill in the art would have understood the invention described and claimed in the '281 Patent. Rather, for the reasons I stated above, a person of ordinary skill in the art would have understood that the term "germanide layer" refers to a metalized germanium layer—e.g., a germanium layer made metallic by a chemical reaction caused by annealing a germanium layer in the presence of a metal overlayer.

VIII. Descriptions of Asserted Prior Art References

A. U.S. Patent Application Pub. No. 2008/0121932 A1 ("*Ranade*")

135. *Ranade* was filed on September 18, 2006, and published on May 29, 2008. I have been told this qualifies *Ranade* as prior art.

136. *Ranade* describes "semiconductor devices," including both planar and non-planar (e.g., FinFET) transistors.[137] An example device described by *Ranade* is illustrated in Figure 2N below, onto which I have added additional reference numerals from Figures 2A-2M for clarity.

[137] *Ranade* ¶¶ [0010], [0025].

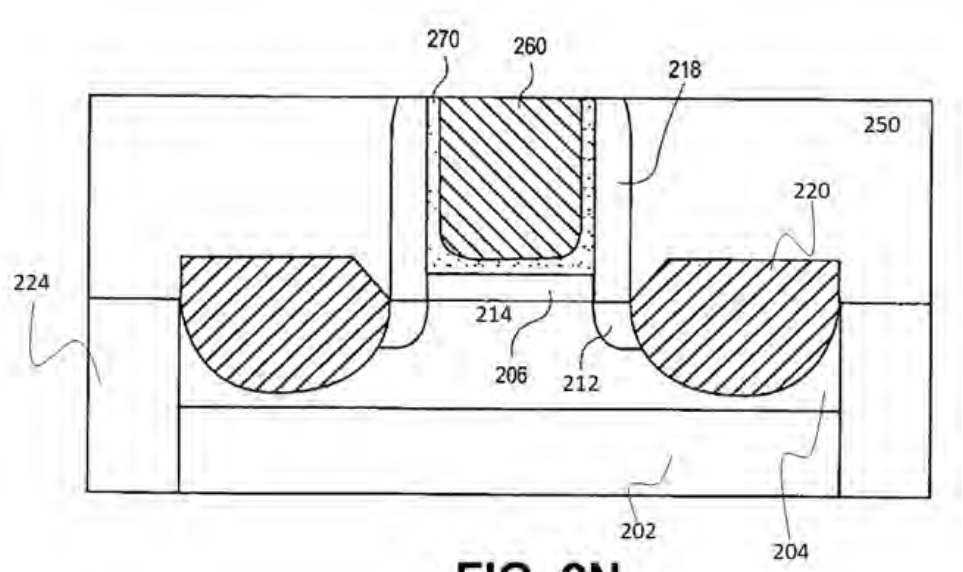


FIG. 2N

137. As shown above, *Ranade*'s semiconductor device includes a gate electrode 260 and Si_xGe_{1-x} epitaxial source/drain regions 220.[138] *Ranade* states that "the pair of source/drain regions 220 comprises a graded epitaxial layer."[139] Such grading, *Ranade* explains, "minimizes surface defects."[140] "In one embodiment," *Ranade* teaches, "the pair of source/drain regions 220 is a crystalline silicon/germanium region of the stoichiometry Si_xGe_{1-x}, where $0 \leqq x \leqq 1$."[141] That is, *Ranade* describes SiGe source/drain regions 220 having a germanium content ranging from 0 to 100 atomic %. *Ranade* also states that "[t]he pair of source/drain regions 220 may incorporate charge-carrier dopant impurity atoms," such as boron:

[138] *Id.* ¶ [0042].

[139] *Id.* ¶ [0040].

[140] *Id.*

[141] *Id.*

> The pair of source/drain regions 220 may be formed by any technique suitable to form a highly uniform (i.e. low surface defect density, e.g. less than 10^6 dislocations/cm^2 at the surface of the pair of source/drain regions 220) crystalline layer. In one embodiment, the pair of source/drain regions 220 comprises a uniform epitaxial layer. In another embodiment, the pair of source/drain regions 220 comprises a graded epitaxial layer, wherein the grading process minimizes surface defects. . . . In one embodiment, the pair of source/drain regions 220 is a crystalline silicon/germanium region of the stoichiometry Si_xGe_{1-x}, where $0 \leqq x \leqq 1$, and the charge-carrier dopant impurity atoms are selected from the group consisting of boron, arsenic, indium or phosphorus.[142]

138. Although Figure 2N depicts a planar FET, *Ranade* explains that the described "invention is not limited to the formation of planar MOS-FETs."[143] Specifically, *Ranade* states that its teachings also apply to "devices with a three-dimensional architecture, such as tri-gate devices" (i.e., a "FIN-FET transistor").[144] *Ranade* describes such a FinFET transistor in Figure 3C, which I have reproduced below. As shown below, *Ranade*'s FinFET includes a "three-dimensional active region 304," which would be subsequently etched away in the source/drain areas and replaced with epitaxial SiGe source/drain regions 220.[145]

[142] *Id.* ¶ [0040].

[143] *Id.* ¶ [0044].

[144] *Id.* ¶¶ [0025], [0043].

[145] *Ranade* ¶ [0046]; *see also id.* ¶¶ [0037]-[0041], Figs. 2I-2K.

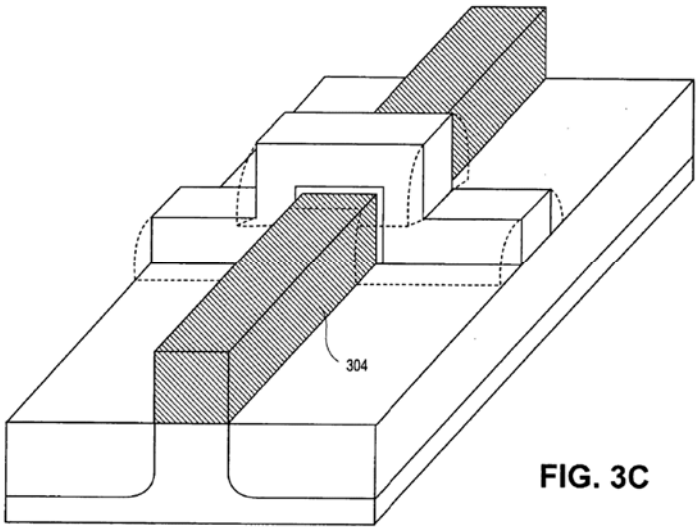


FIG. 3C

B. U.S. Patent Application Pub. No. 2010/0123198 A1 ("*Kim*")

139. *Kim* was filed on November 13, 2009, and published on May 20, 2010. I have been told this qualifies *Kim* as prior art.

140. *Kim* describes "semiconductor devices having low resistance contacts."[146] It teaches that "reduction of contact resistance is an important issue with respect to high integration density of CMOS transistor devices."[147] "In order to provide a low resistance contact to a CMOS transistor," *Kim* explains "the P-channel and N-channel MOSFETs need to be provided with a contact having a low Schottky barrier."[148] "Conventionally," *Kim* states, "a technology for reducing the Schottky barrier of a contact by applying metal silicide films having different

[146] *Kim* at Abstract.

[147] *Id.* ¶ [0006].

[148] *Id.* ¶ [0007].

work functions respectively to P-channel and N-channel MOSFETs has been suggested."[149] Such metal-semiconductor films "reduce the height of Schottky barriers in contact regions and thus reduce sheet resistance."[150]

141. *Kim* describes two processes for forming metal-semiconductor films. In the first process (illustrated in Figure 5), a metal-semiconductor film is formed at the interface between a metal overlayer and an intermediate Ge layer formed on the source/drain regions. I refer to this process as Ge Overlayer Metalization. In the second process (illustrated in Figure 3F), a metal-semiconductor film is formed at the interface of a metal overlayer and exposed SiGe source/drain regions. I refer to this process as Direct Metalization. I summarize both *Kim* processes below, which "may be implemented independently or in combination with the other embodiments" described in *Kim* (e.g., those described with reference to Figures 1F, 2D, and 4).[151]

1. *Kim*'s Ge Overlayer Metalization

142. *Kim*'s Ge Overlayer Metalization is shown in Figure 5 below. In this process, a metal-semiconductor film is formed at the interface between a metal overlayer and a thin, intermediate layer of Ge formed on the source/drain regions.

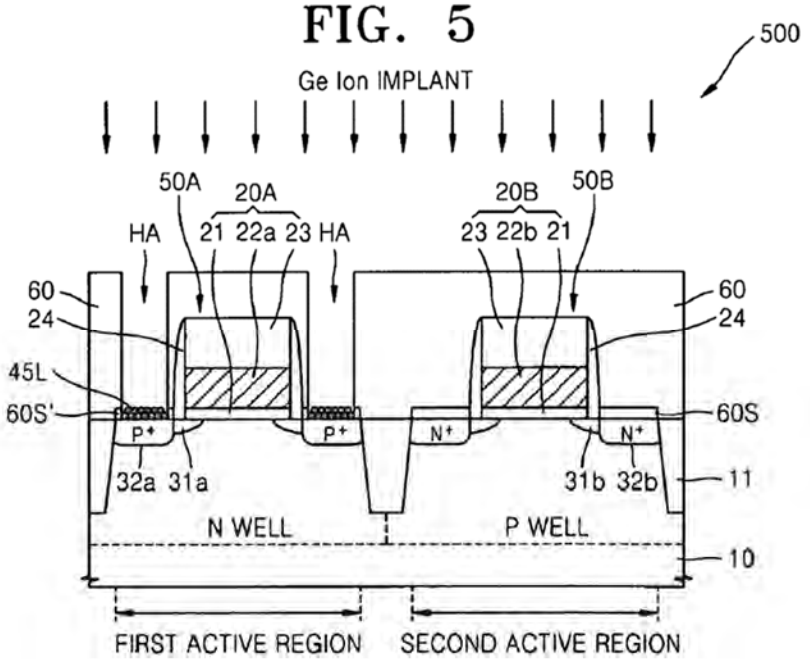
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[149] *Id.*

[150] *Id.* ¶ [0050].

[151] *Id.* ¶ [0074].

FIG. 5



143. As Figure 5 above illustrates, *Kim*'s semiconductor device may include a thin, intermediate Ge layer 45L (which I have annotated in red) formed on the source/drain regions.[152] The intermediate Ge layer 45L may be formed by Ge deposition within contact holes HA in interlayer insulating film 60.[153] *Kim* explains that metal-semiconductor film 80A "may be a M(Si1-yGey) film including the Ge atomic layer 45L."[154] When metal layer 70 is titanium, a person of ordinary skill in the art would have understood from *Kim* that metal-semiconductor films 80A are TiSi1-yGey layers formed because the Ti atoms in metal layer 70 will chemically react with Ge atoms in the thin Ge layer 45L and

[152] *Id.* at ¶ [0073].

[153] *Id.* ¶¶ [0072]-[0074].

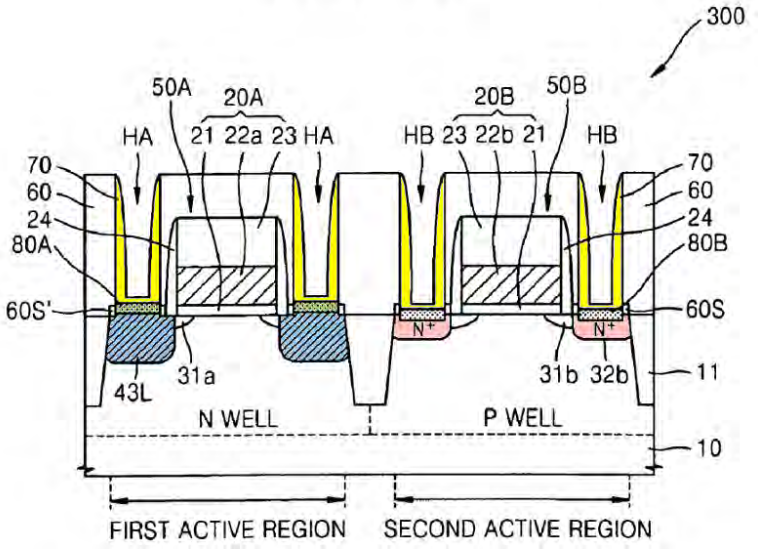
[154] *Id.* ¶ [0073].

also atoms diffused through the thin Ge layer 45L from the source/drain region below.[155] Again, *Kim* explains that "the M(Si1-yGey) film [is] capable of improving contact resistance of the P-channel field-effect transistor 50A."[156]

2. *Kim*'s Direct Metalization

144. Figure 3F, which I have annotated with color below, shows *Kim*'s Direct Metalization for forming metal-semiconductor films:

FIG. 3F



[155] *See id.* ¶¶ [0072]-[0073] (explaining that "the Ge ions may form a Ge atomic layer 45L piled on the first active region as illustrated in FIG. 5" and also may be formed by "pulsed laser ablation deposition (PLAD)" or "gas cluster ion beam (GCIB) deposition"); S. Zaima & Y. Yasuda, *Study of Reaction and Electrical Properties at Ti/SiGe/Si(100) Contacts for Ultralarge Scale Integrated Applications*, Journal of Vacuum Science & Technology B, vol. 16, at 2625-27, Fig. 1 (1998) ("Silicon atoms preferentially react with Ti atoms at annealing temperatures below 300 °C and Ge atoms start to react above 400 °C."); S. Gaudet et al., *Thin Film Reaction of Transition Metals with Germanium*, Journal of Vacuum Science & Technology A, vol. 24, no. 3 at Fig. 5 (2006) (showing reaction temperatures for numerous metal-Ge compounds).

[156] *Kim* ¶ [0073].

As shown above, *Kim*'s semiconductor device includes epitaxial SiGe source/drain regions 43L.[157] Metal-semiconductor films 80A and 80B are formed over SiGe source/drain regions 43L.[158] Specifically, *Kim* teaches that metal layers 70 (yellow) are deposited and annealed to cause a "reaction" with p-type SiGe source/drain regions 43L (blue).[159] *Kim* describes thermal annealing at a temperature as high as "about 650° C."[160] "Due to thermal annealing," *Kim* explains, metal layer 70 (yellow) and SiGe source/drain regions 43L (blue) react to form metal-semiconductor films 80A (green).[161] *Kim* describes each metal-semiconductor film 80A as "a M(Si1-yGey) film containing Ge due to the exposed SiGe epitaxial layer 43L," where "M" represents the metal of metal layer 70.[162] One metal *Kim* discloses for use as metal layer 70 is titanium.[163] When metal layer 70 is titanium, a person of ordinary skill in the art would have understood from *Kim* that metal-semiconductor films 80A are TiSi1-yGey layers because the Ti atoms in metal

[157] *Id.* ¶ [0065].

[158] *Id.* ¶ [0050]; *see also id.* ¶ [0046] (referring to "reaction between the exposed SiGe epitaxial layer" and "reference numeral 70 of FIG. 1E").

[159] *Id.* ¶¶ [0063]-[0067]; *see also id.* ¶¶ [0047]-[0049], [0057].

[160] *Id.* ¶ [0048].

[161] *Id.* ¶ [0067].

[162] *Id.*; *see also id.* ¶¶ [0047]-[0049], [0057], [0071].

[163] *Id.* ¶ [0047].

layer 70 will chemically react with the Si and Ge atoms in the p-type SiGe source/drain regions 43L.[164]

145. *Kim* explains that a metal-semiconductor film 80A—such as a TiSi1-yGey layer—reduces contact resistance:

> [D]uring the silicide reaction between the SiGe epitaxial layer 42L and the barrier metal layers 70, Si having reactivity higher than that of Ge reacts more dominantly than Ge. As a result, concentration of Ge increases, a band gap of contact regions may be reduced. The reduced band gap may reduce the height of Schottky barriers and thus contact resistance of the P-channel field-effect transistor 50A may be considerably reduced.[165]

C. U.S. Patent Application Pub. No. 2010/0276761 A1 ("*Tung*")

146. *Tung* was filed on January 6, 2010, and published on November 4, 2010. I have been told this qualifies *Tung* as prior art.

147. *Tung* teaches FinFET "structures and methods of fabrication thereof with low resistance contacts for non-planar semiconductor structures."[166] In

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[164] *Id.* ¶¶ [0046]-[0048], [0050], [0067]; *see also* S. Zaima & Y. Yasuda, *Study of Reaction and Electrical Properties at Ti/SiGe/Si(100) Contacts for Ultralarge Scale Integrated Applications*, Journal of Vacuum Science & Technology B, vol. 16, at 2625-27, Fig. 1 (1998) ("Silicon atoms preferentially react with Ti atoms at annealing temperatures below 300 °C and Ge atoms start to react above 400 °C."); S. Gaudet et al., *Thin Film Reaction of Transition Metals with Germanium*, Journal of Vacuum Science & Technology A, vol. 24, no. 3 at Fig. 5 (2006) (showing reaction temperatures for numerous metal-Ge compounds).

[165] *Kim* ¶ [0050].

[166] *Tung* ¶ [0006]; *see also id.* ¶¶ [0005], [0021], [0027], [0029], [0032], [0034], [0039], [0061].

particular, *Tung* addresses the subject of "forming metal semiconductor contacts with low contact resistance" in the source/drain regions and explains that "the Schottky barrier height between the source/drain region and the metal silicide needs to be reduced."[167]

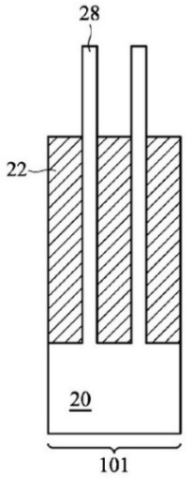


FIG. 6a

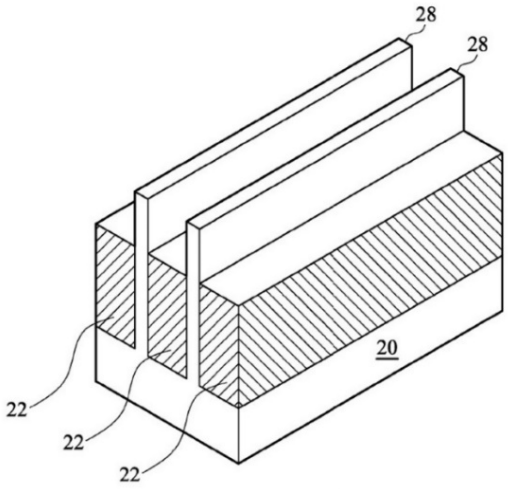


FIG. 6b

148. Referring to Figures 6a and 6b above, *Tung* teaches FinFET structures in which "isolation regions 22 are formed on the substrate 20" in a manner "known in the art."[168] For example, "the isolation regions 22 may be formed by etching substrate 20 to form recesses, and then filling the recesses with dielectric materials."[169] Substrate 20 comprises "bulk silicon" or "bulk silicon germanium (SiGe)."[170] As the figures above illustrate, *Tung* teaches "[t]he fin 28, disposed

[167] *Id.* ¶ [0005].

[168] *Id.* ¶ [0049].

[169] *Id.*

[170] *Id.* ¶ [0048].

between the isolation regions 22, is a continuous piece of underlying semiconductor substrate 20."[171]

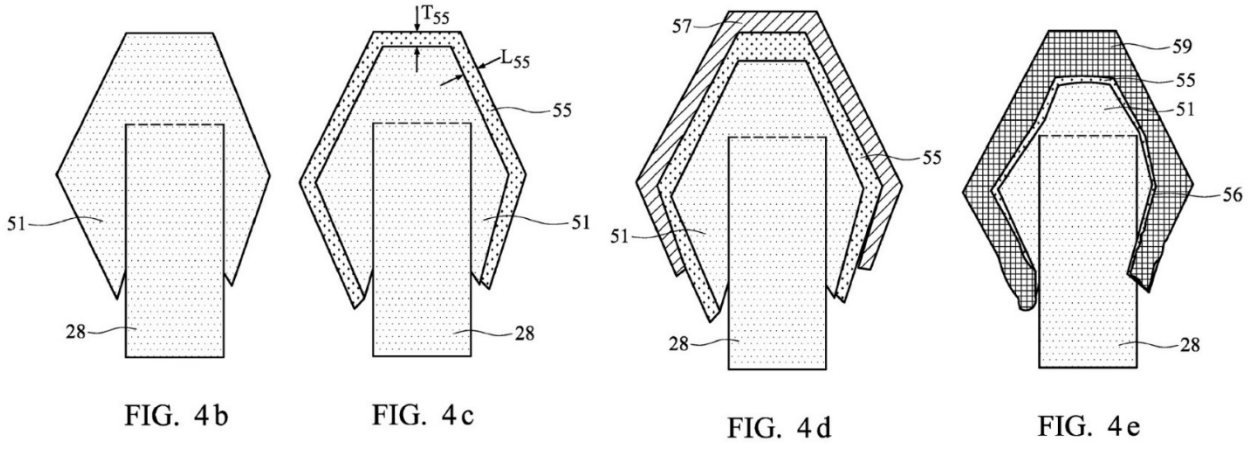


FIG. 4b FIG. 4c FIG. 4d FIG. 4e

149. After forming a gate structure over the channel region,[172] source/drain regions 39, including extension regions, are formed.[173] Specifically, as Figure 4b above illustrates, a semiconductor material 51, such as SiGe, is grown over fin 28.[174] According to *Tung*, semiconductor layer 51 is doped (e.g., with boron) "between about $1\times10^{17}/cm^3$ to about $5\times10^{20}/cm^3$."[175]

150. Next, as Figure 4c above illustrates, "another selective epitaxial growth is used to form a doped semiconductor layer 55."[176] *Tung* teaches that

[171] *Id.* ¶ [0023]; *see also id.* ¶ [0051] ("Fins 28 may be formed by recessing the top surfaces of the isolation regions 22, and hence leaving the fins 28."), Figs. 6a, 6b.

[172] *Id.* ¶¶ [0052]-[0055], [0073], Fig. 7c,

[173] *Id.* ¶¶ [0073], [0074], Figs. 2d, 13.

[174] *Id.* ¶¶ [0040], [0074].

[175] *Id.* ¶ [0076]; *see also id.* ¶ [0040], Figs. 4b, 13.

[176] *Id.* ¶ [0041]; *see also id.* ¶ [0078], Figs. 4c, 14.

doped semiconductor layer 55 may be "doped SiGe" or "doped Ge."[177] For example, it "may be doped (e.g., in-situ doped) with a p-type dopant if a PMOS transistor is being fabricated."[178] The doped semiconductor layer 55 "is heavily doped" to minimize contact resistance—e.g., doped to a concentration "greater than about 5×10^{19} cm^{-3}."[179]

151. After growing semiconductor materials 51 and 55 over fin 28, and as *Tung*'s Figure 4d above illustrates, "a silicide metal 57 is deposited" over doped semiconductor layer 55, which *Tung* teaches may be titanium.[180]

152. Next, as Figure 4e above illustrates, "the silicide metal 57 is annealed to form a metal silicide layer 59[,]" and any "[u]n-reacted silicide metal 57 is removed by an etching process."[181] "During the silicidation anneal, the silicide metal 57 (FIG. 4d) reacts with the doped semiconductor layer 55 and forms a metal silicide layer 59" (e.g., TiSiGe when silicide metal 57 is Ti).[182]

[177] *Id.* ¶ [0078]; *see also id.* ¶ [0058].

[178] *Id.* ¶ [0041].

[179] *Id.* ¶ [0034].

[180] *Id.* ¶ [0042]; *see also id.* ¶¶ [0079]-[0080], Figs. 4d, 15.

[181] *Id.* ¶ [0043]; *see also id.* ¶ [0081], Figs. 4e, 16.

[182] *Id.* ¶ [0043]; *see also id.* ¶¶ [0041], [0045], [0063], [0064], [0081].

D. U.S. Patent No. 7,361,958 ("*Brask*")

153. *Brask* was filed on September 30, 2004, and issued on April 22, 2008. I have been told this qualifies *Brask* as prior art.

154. *Brask* teaches FinFET-based "CMOS integrated circuits with p type and n type nonplanar transistors with metal gate electrodes."[183]

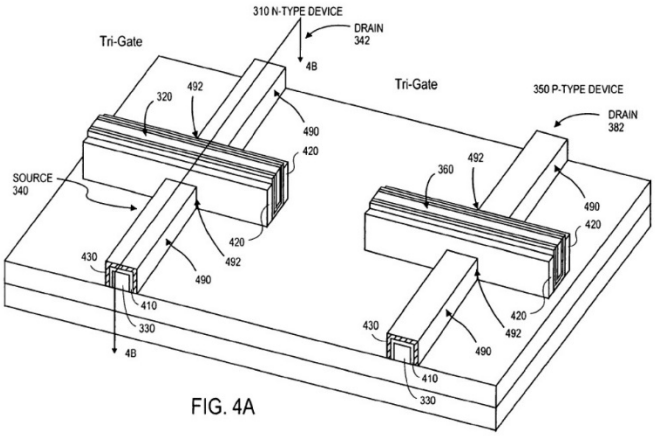


FIG. 4A

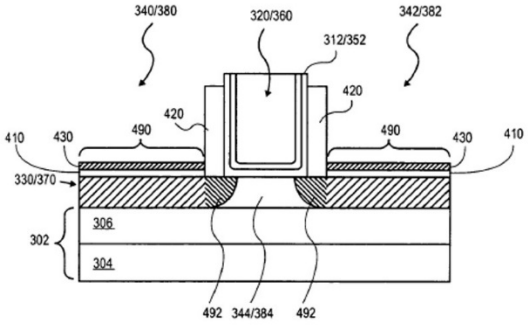


FIG. 4B

155. As *Brask*'s Figures 4A and 4B above illustrate, *Brask* teaches a FinFET device structure with a SiGe fin 330/370 that has a channel region 384 under the gate sandwiched by source/drain regions 490.[184] *Brask*'s FinFET structure also contains source/drain extension regions 492.[185] *Brask*'s FinFET structure further includes raised source/drain regions made using a semiconductor film 410 formed on fin 330/370.[186] According to *Brask*, semiconductor film 410 is

[183] *Brask* at 1:7-11.

[184] *Id.* at 5:26-51, 8:13-41, 9:61-10:11, Figs. 4A, 4B.

[185] *Id.* at 9:61-10:11, 11:15-31, Fig. 4B.

[186] *Id.* at 10:20-49, Figs. 4A, 4B.

a Si_xGe_{1-x} film with 1 to 100 atomic % Ge (i.e., $0 \leq x \leq 0.99$), and it may "be graded" such that the Ge composition varies by location in semiconductor film 410.[187] *Brask*'s FinFET devices also include a metal-semiconductor layer 430 formed on semiconductor film 410 by metalizing semiconductor film 410 with titanium.[188] *Brask* explains that this approach "reduc[es] the source/drain contact resistance to transistors 310 and 350 and improv[es] their electrical characteristics and performance."[189]

E. U.S. Patent Application Pub. No. 2009/0096002 A1 ("*Yu*")

156. *Yu* was filed on October 15, 2007, and published on April 16, 2009. I have been told this qualifies *Yu* as prior art.

157. *Yu* describes "a system and method for forming electrical contacts, and more particularly . . . a system and method for forming electrical contacts to sections raised above a substrate."[190] *Yu* explains that traditional layouts for planar FETs required "the contact width [to be] either less than, or at most equal to, the width of" the underlying structure.[191] But as that width shrank over time, especially by shifting to non-planar FinFETs, "adhering to this layout rule" caused

[187] *Id.* at 10:20-29.

[188] *Id.* at 10:50-64, Figs. 4A, 4B.

[189] *Id.* at 10:43-49.

[190] *Yu* ¶ [0001].

[191] *Id.* ¶ [0003].

"a number of problems."[192] First, "with the reduction of the contact area, the contact resistance of the contact has risen, thereby limiting improvements to the driving current of the device."[193] Second, "mis-alignment of the contacts during the manufacturing process has led to variations in the contact resistance between the device and the contacts, thereby leading to differences in resistance between various devices and reducing the overall circuit yield."[194] And third, "silicide formation" had to be done using "an ultra-shallow junction on the source/drain areas, thereby preventing improvements in the Schottky barrier height."[195] *Yu* provides a simple technique and layout to avoid these issues:

> An advantage of a preferred embodiment of the present invention is a reduction in the contact resistance between the source/drain regions and the contacts, which leads to greater overall device performance. Further, variations in the contact resistances because of contact misalignment is also reduced, creating a more uniform product, and the silicide formation does not require an ultra shallow junction, allowing further improvements in the Schottky barrier height.[196]

158. *Yu*'s source/drain contact formation process begins with an inter-layer dielectric (ILD) 801 formed over the entire FinFET device structure, as Figure 8

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[192] *Id.* ¶ [0004].

[193] *Id.*

[194] *Id.*

[195] *Id.*

[196] *Id.* ¶ [0010]; *see also id.* ¶¶ [0005], [0006].

shows below.[197] "The ILD 801 may be formed by chemical vapor deposition, sputtering, or any other methods known and used in the art for forming an ILD 801" and "typically has a planarized surface."[198] It "may be comprised of silicon oxide," for example.[199]

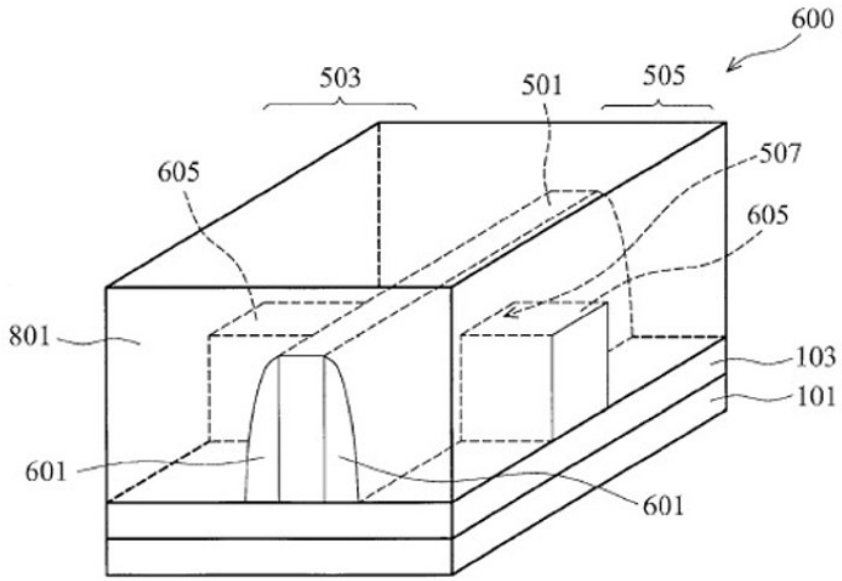


FIG. 8

159. Next, as Figures 9A and 9B below illustrate,[200] *Yu* explains contacts 901 are formed through the ILD down to the metal-semiconductor layer 605.[201]

[197] *Id.* ¶ [0034]; *see also id.* at Fig. 8.

[198] *Id.* ¶ [0034].

[199] *Id.*

[200] Figure 9A provides an orthographic view of *Yu*'s FinFET device after contact plugs 901 have been added, and Figure 9B provides a plan view of the same structure from above. *See id.* ¶¶ [0035], [0040].

[201] *Yu* ¶ [0035]; *see also id.* at Figs. 9A, 9B.

"Contacts 901 may be formed in the ILD 801 in accordance with known photolithography and etching techniques."[202] *Yu* explains: a "mask is patterned to subsequently form openings that are wider than the width of the fin 201."[203]

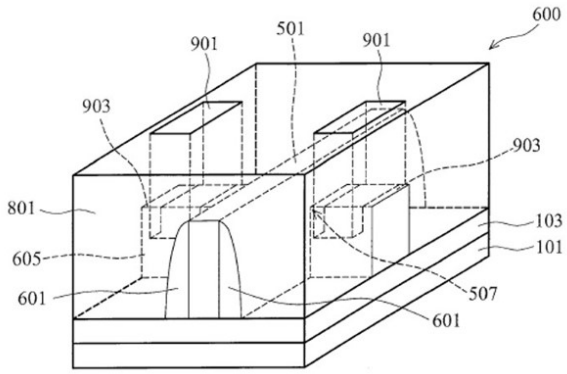


FIG. 9A

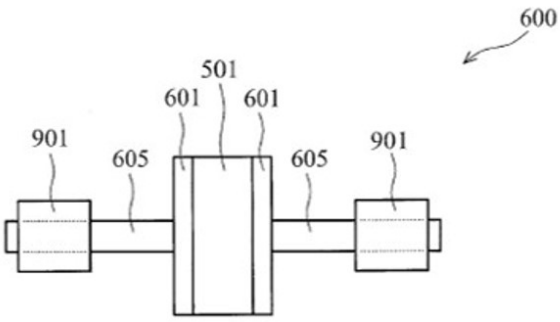


FIG. 9B

To form those openings, an "etch process is continued until an upper surface 903 of the fin 201 containing the source/drain regions 603 and at least a portion of the sidewalls of the fin 201 are exposed, thereby exposing at least three surfaces of the fin 201 (portions of the top surface and portions of at least two sidewalls)."[204] Contacts 901 are then "formed so as to be in contact with at least three surfaces of the fin 201[,]" which "allows for a larger area of contact between the silicide contacts 605 and the contact 901 than contacts that only contact the top surface of the fin 201."[205] "Accordingly, the contact resistance of the device may be

[202] *Id.* ¶ [0035].

[203] *Id.*

[204] *Id.* ¶ [0036].

[205] *Id.* ¶ [0037].

reduced[,]" and "variations in the contact resistances due to mis-alignments of the contacts 901" are reduced "since there is more leeway for variation when the width of the contacts 901 are larger than the width of the fin 201."[206]

160. *Yu* also explains that "contacts 901 may comprise a barrier/adhesion layer (not shown) to prevent diffusion and provide better adhesion between the contacts 901 and the ILD 801."[207] The barrier layer may be "formed of one or more layers of titanium, titanium nitride, tantalum, tantalum nitride, or the like."[208] And "contacts 901 may be formed of any suitable conductive material, such as a highly-conductive, low-resistive metal, elemental metal, transition metal, or the like."[209] "In an exemplary embodiment the contacts 901 are formed of tungsten, although other materials, such as copper, could alternatively be utilized."[210]

F. U.S. Patent No. 7,611,943 ("*Liu*")

161. *Liu* was filed on October 12, 2005, and issued on November 3, 2009. I have been told that this qualifies *Liu* as prior art.

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[206] *Id.*

[207] *Id.* ¶ [0038].

[208] *Id.*

[209] *Id.* ¶ [0039].

[210] *Id.*

162. *Liu* discloses various FET processes and structures, including for FinFETs.[211] *Liu* also explains that such "[f]ield effect transistors (FETs) are widely used in the electronics industry for switching, amplification, filtering, and other tasks related to both analog and digital electrical signals."[212] Moreover, *Liu* teaches that improved FETs may help address the following problem: "wireless mobile product technology continues to demand more applications performance, less power drain on batteries, and lower integrated circuit cost of manufacture."[213] In a section titled "Improved Integrated Circuits and Systems," *Liu* also discloses exemplary systems in which FETs, including FinFETs, may be used.[214]

163. As *Liu*'s Figures 10 and 11 below illustrate, *Liu* confirms that FETs, including FinFETs, are commonly employed in consumer electronics, including in smartphones, for example.[215]

[211] *See Liu* at 32:22-40, Fig. 8.

[212] *Id.* at 1:47-50.

[213] *Id.* at 1:29-32.

[214] *See id.* at 33:10-37:40, Figs. 10, 11.

[215] *See id.* at Figs. 10, 11.

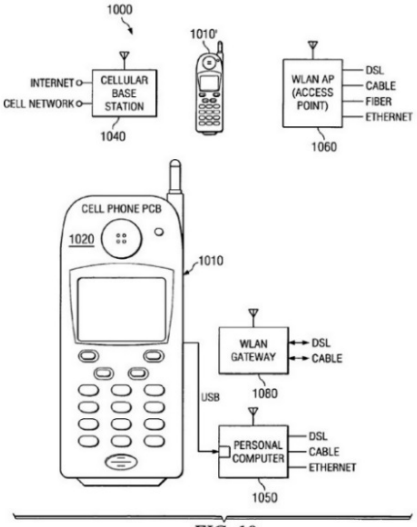


FIG. 10

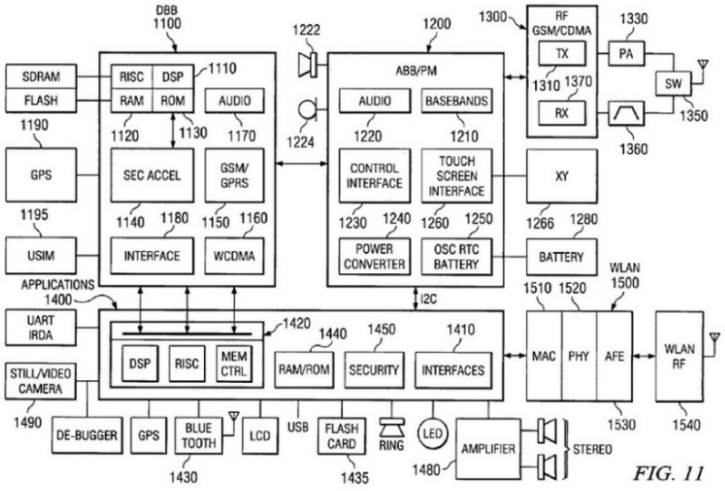


FIG. 11

164. Figure 10 above illustrates a cell phone system, and Figure 11 illustrates integrated circuits for use in such a cell phone system.[216] *Liu* explains that, "[o]n a cell phone printed circuit board (PCB) 1020 in handset 1010, there is provided a processor integrated circuit 1022, an external flash memory 1024, and a serial interface 1026."[217] The integrated circuits in Figure 11 include, for example, various processors, memory, wireless communications chips, a camera interface, GPS circuitry, a battery, various antennas, and more.[218]

IX. Claims 1, 5-8, and 12-20 of the '281 Patent are Unpatentable

165. The '281 Patent aims to provide low-resistance contacts to the SiGe source and drain regions in a P-type transistor. To this end, the '281 Patent

[216] *See id.* at 33:12-15, 33:62-63.

[217] *Id.* at 33:50-53.

[218] *See id.* at 33:10-37:40, Figs. 10, 11.

describes adding a Ge capping layer on top of the SiGe source and drain regions. But the principles that suggest using a Ge capping layer—as well as the Ge capping layer itself and the '281 Patent's explanation of its benefits—were already well established by December 2010.

166. According to the '281 Patent, the alleged improvements derived from using a Ge capping layer stem from three basic principles:

> [T]he combination of **high germanium concentration** (e.g., in excess of 90 atomic % and up to pure germanium) and **high boron concentration** (e.g., in excess of 2E20 cm^{-3}) can be used to realize significantly lower contact resistance in the source and drain regions (and other areas where low contact resistance is desirable, such as ground tap regions), in accordance with some example embodiments. Further, and as previously explained, since **boron diffusion is sufficiently suppressed** by pure germanium, no adverse SCE degradation is realized with subsequent thermal anneals despite any high boron concentration proximate the channel (if applicable). Barrier height lowering is also enabled from the higher concentration of germanium at the contact surface. In some example embodiments, a germanium concentration in excess of 95 atomic % and up to pure germanium (100 atomic %) can be used to achieve such benefits.[219]

[219] '281 Patent at 10:53-11:3; *see also id.* at 2:43-64 (explaining that "the contact resistance is effectively limited by the silicon or SiGe valence band alignment to the pinning level in the metal" and that using a "boron doped germanium layer" will "significantly reduce the band misalignment value and contact resistance"), 4:10-16 (explaining that "a high concentration of boron can be doped in the germanium, which in tum results in lower parasitic resistance" and that, "[i]n addition, the contact resistance is reduced from lowering of Schottky-barrier height"), 14:41-57 (explaining, among other things, that "[t]he magnitude of the Schottky barrier height reflects a mismatch in the energy position of the metal's

These principles—high germanium concentration, high boron concentration, and reduced boron diffusion—were already well-known by December 2010. In fact, these are the three basic principles underlying SiGe/Strained Si technology as a whole. As a paper from 2005 explains, "[h]igh boron activation, smaller bandgap and the ability to reduce boron diffusion" is "the basis for the $Si_{1-x}Ge_x$ source/drain technology."[220]

167. A person of ordinary skill in the art would have understood that the '281 Patent merely describes a structure to reduce contact resistance in view of these basic principles. It proposes the same structure I would have expected one of my graduate students to provide if I had asked on an exam how to minimize the source/drain contact resistance of a SiGe pFET device: SiGe source/drain regions with (1) a germanium layer (e.g., a layer with more than about 85 atomic % Ge) at the metal-semiconductor interface, which provides the lowest bandgap and the

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Fermi level and the majority carrier band edge of the semiconductor across the semiconductor-metal interface," which, "[f]or a p-type semiconductor-metal interface . . . is the difference between the metal Fermi level and the valence band maximum of the semiconductor").

[220] M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 224 (Mar. 2005); *see also* S. Gannavaram et al., *Low Temperature (≤800°C) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for Sub-70 nm CMOS*, Technical Digest of the 2000 IEEE International Electron Devices Meeting (IEDM) at 437-38, Fig. 3 (2000).

highest reduction in boron diffusion, and (2) high levels of doping at the metal-semiconductor interface.

168. Not only does the ’281 Patent identify the same solution as the prior art, but it also describes the same improvement in Schottky barrier height that others described many years earlier, including in the paper I referenced above. The ’281 Patent states:

> A standard transistor contact stack typically includes, for example, a silicon or SiGe source/drain layer, a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad. In such configurations, the contact resistance is effectively limited by the silicon or SiGe valence band alignment to the pinning level in the metal. Typically, using **industry standard silicides** such as nickel (or other suitable silicides, such as titanium, cobalt, or platinum), this **results in a band misalignment of about 0.5 eV**. . . . **[C]ontacts configured with the intermediate boron doped germanium layer exhibit a reduction in the band misalignment value to less than 0.2 eV.**[221]

This is the same expected reduction in Schottky barrier height others had already identified. For example, the 2005 paper I referenced above states: “[W]e expect a barrier height change of approximately 0.3 eV”[222]—the same reduction in Schottky

[221] ’281 Patent at 2:43-64.

[222] M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, pp. 222-231, at 229 (Mar. 2005).

barrier height that the ’281 Patent describes by lowering it from 0.5 eV to 0.2 eV. And *Yasutake* (published in 2007) teaches that a Schottky barrier height “ϕ_B=0.2 eV is achieved” by forming a “germanide layer on [a] germanium layer” to form the metal-semiconductor interface of its source/drain contacts.[223]

169. Because these principles were well established, and because structures to reduce contact resistance based on these principles were clear, a person of ordinary skill in the art would have found the claimed structures in the ’281 Patent obvious. The following sections explain why in greater detail.

A. Ground 1A: The Combination of *Ranade* and *Kim* Would Have Rendered Claims 1, 5-8, and 12-20 Obvious

1. A Person of Ordinary Skill in the Art Would Have Found the Combination of *Ranade* and *Kim* Obvious

170. A person of ordinary skill in the art would have found it obvious to add a source/drain contact structure with a TiSi1-yGey layer over *Ranade*’s p-type Si_xGe_{1-x} source/drain regions because, although not described in detail, *Ranade*’s device structure requires source/drain contacts to operate, and using such source/drain contacts would have been expected to lower the Schottky barrier height and reduce contact resistance.

171. *Kim* recognizes the need to reduce the source/drain contact resistance in semiconductor devices. As *Kim* states, “reduction of contact resistance is an

[223] *Yasutake* (US2007/0187767) ¶ [0045].

important issue with respect to high integration density of CMOS transistor devices."[224] *Kim* also teaches how to reduce source/drain contact resistance: "In order to provide a low resistance contact to a CMOS transistor," *Kim* explains, "the P-channel and N-channel MOSFETs need to be provided with a contact having a low Schottky barrier."[225] And *Kim* describes "a technology for reducing the Schottky barrier of a contact," namely, by forming a M(Si1-yGey) layer "that contact[s] the contact plugs 90" to "reduce the height of Schottky barriers in contact regions and thus reduce sheet resistance."[226]

172. As I describe in Section VIII.B, *Kim* describes two processes for forming these M(Si1-yGey) films: Ge Overlayer Metalization and Direct Metalization. In Ge Overlayer Metalization, a M(Si1-yGey) film is formed at the interface of a metal and an intermediate layer of Ge formed on the source/drain regions. In Direct Metalization, a M(Si1-yGey) film is formed at the interface of a metal layer and the SiGe source/drain regions. In both processes, *Kim* teaches that the M(Si1-yGey) film may be a TiSi1-yGey film.[227]

[224] *Kim* ¶ [0006].

[225] *Id.* ¶ [0007].

[226] *Id.* ¶ [0050].

[227] *See id.* ¶¶ [0049], [0057], [0067], [0071], [0073], [0074].

173. Thus, *Kim* teaches forming a TiSi1-yGey film over the SiGe source/drain regions to reduce contact resistance. A person of ordinary skill in the art would have been motivated to complete *Ranade*'s FinFET by adding a TiSi1-yGey film over its p-type SiGe source/drain regions and would have reasonably expected to succeed in doing so. As I explain further below, a person of ordinary skill in the art would have been motivated by (1) *Ranade*'s reference to—but silence regarding—"typical process steps," including "silicidation"; and (2) *Kim*'s teaching that formation of a TiSi1-yGey film over the source/drain regions reduces contact resistance. As I also explain below, a person of ordinary skill in the art would have reasonably expected to succeed at least because (1) the MSi1-yGey technique *Kim* describes was known prior to December 2010; and (2) the MSi1-yGey technique *Kim* describes would have been implemented with predictable results on *Ranade*'s FinFET devices.

174. Finally, as I explain below, a person of ordinary skill in the art would have recognized at least two obvious modifications to *Ranade*'s semiconductor device based on *Kim*'s MSi1-yGey teachings.

a. A person of ordinary skill in the art would have been motivated to complete *Ranade*'s FinFET device by adding a TiSi1-yGey film and contact plug over *Ranade*'s p-type SiGe source/drain regions

175. A person of ordinary skill in the art would have been motivated to complete *Ranade*'s semiconductor device by adding a TiSi1-yGey film and contact

plug over *Ranade*'s p-type SiGe source and drain regions. As discussed below, a person of ordinary skill in the art would have been motivated by (1) *Ranade*'s reference to—but silence regarding—"typical process steps," including "silicidation"; and (2) *Kim*'s teaching that formation of a TiSi1-yGey film and contact plug over the source/drain regions reduces contact resistance.

i. *Ranade* refers to "typical process steps," including "silicidation"

176. *Ranade* describes and illustrates its semiconductor devices with a focus on the structure of the transistors themselves, not the contact structures required to connect neighboring transistors to one another and to the outside world. *Ranade*'s disclosed FinFET structure includes, for example, source/drain regions and a gate, as Figures 2N and 3C below illustrate.

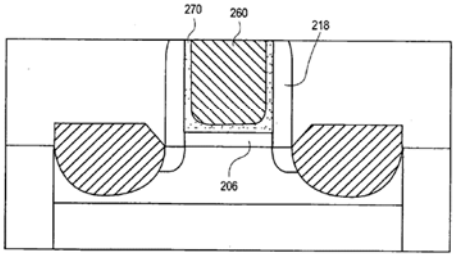


FIG. 2N

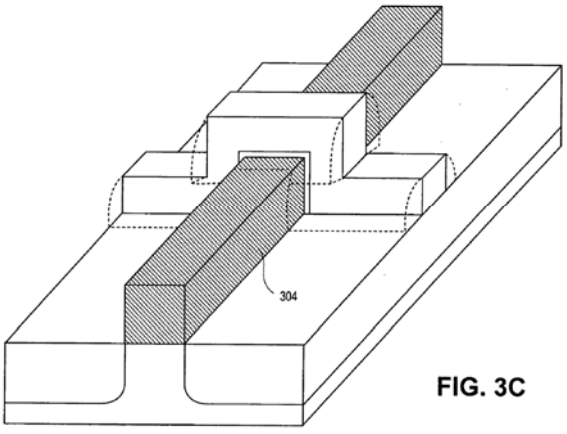


FIG. 3C

177. *Ranade*'s figures do not illustrate contact structures for its disclosed FinFET device, which provide the necessary electrical connections required to connect the source/drain regions to other devices on the wafer and to the outside

world. A person of ordinary skill in the art would have understood that such structures are not the focus of *Ranade*'s invention. As *Ranade* explains, "well-known processing steps . . . are not described in detail in order to not unnecessarily obscure the present invention."[228] Rather, *Ranade* simply states that its devices may "undergo typical process steps to complete the formation of a MOS-FET," including "a silicidation step."[229] This approach was and remains common when describing a transistor structure itself.

178. A person of ordinary skill in the art would have understood that omitting discussion or illustration of metallic contacts and related processes, as *Ranade* does, was typical when describing a transistor device structure. This can be commonly seen in numerous exemplary prior-art patents and other publications.[230]

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[228] *Ranade* ¶ [0009].

[229] *Id.* ¶ [0041].

[230] *See, e.g.*, *Brask* at 27:20-27 ("Well known [interlayer dielectric layers and metal interconnects] can now be utilized to interconnect the various p type and n type devices together into functional CMOS integrated circuits."); *Yeh* (US9245805) at 4:43-48 ("Next, silicide/germanide regions (not shown) may be formed on source/drain regions 142 and 242 by reacting source/drain regions 142 and 242 with a metal(s) to reduce the contact resistances. The formation details of silicide/germanide regions are known in the art, and hence are not repeated herein."); *Tung* ¶¶ [0023] ("A contact (not shown) is disposed on the metal silicide layer 59."), [0036] (same), [0064] (same); *Rhee* (US2008/0067545) ¶ [0018] ("The contact portion of the source/drain region may be in contact with a contact structure."), [0021] ("A contact structure configured to transmit an electrical signal to the source/drain region may be connected to the metal semiconductor compound layer 124 so as to be electrically connected."); *Simonelli* ¶ [0043] (explaining that

179. A person of ordinary skill in the art would have understood that *Ranade*'s semiconductor devices would include the metal contacts necessary to operate. Those metal contacts would include, among other things, a suitable source/drain contact structure to facilitate electrical connection to the source/drain regions. A person of ordinary skill in the art would have recognized that such a source/drain contact structure **must** be added to *Ranade*'s structures for them to operate. Accordingly, a person of ordinary skill in the art seeking to implement *Ranade*'s semiconductor devices would have been motivated to include a low-resistance source/drain contact structure formed using, as *Ranade* states, "typical process steps" like "silicidation."

ii. *Kim* teaches that formation of a TiSi1-yGey film and contact plugs over the source/drain regions reduces contact resistance

180. As *Kim* teaches, "reduction of contact resistance is an important issue with respect to high integration density of CMOS transistor devices."[231] "In order to provide a low resistance contact to a CMOS transistor" *Kim* explains, "the P-channel and N-channel MOSFETs need to be provided with a contact having a low Schottky barrier."[232] To "reduce the height of Schottky barriers in contact

"device 100 may undergo further MOS processing . . . that may further modify the device and/or provide the necessary electrical interconnections.").

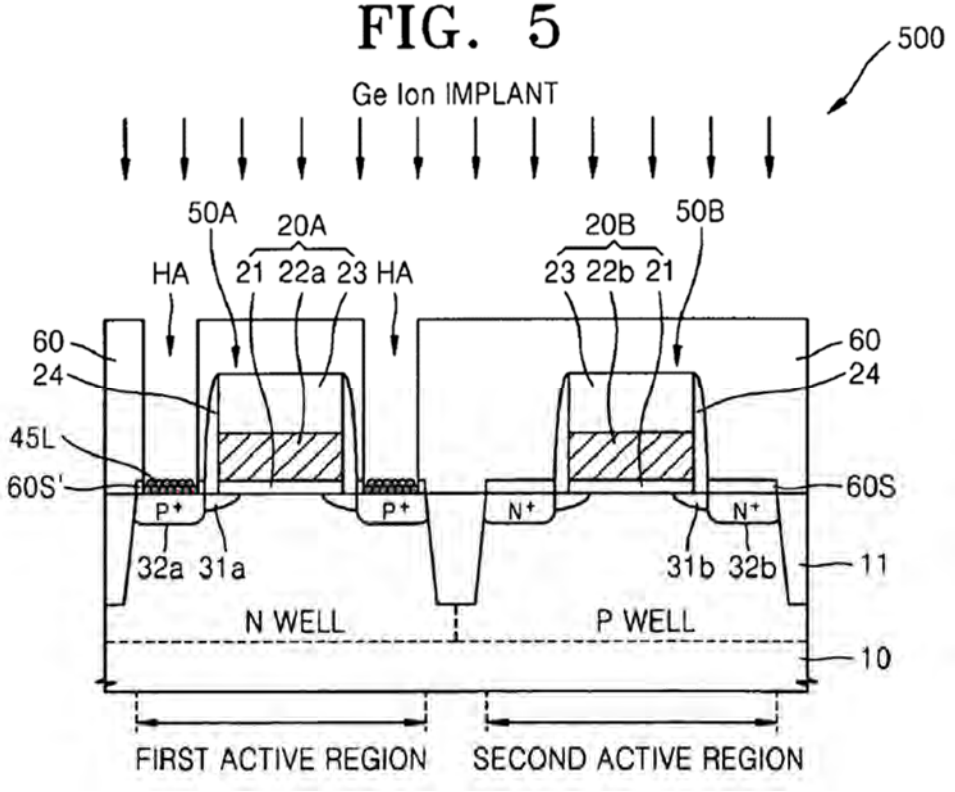
[231] *Kim* ¶ [0006].

[232] *Id.* ¶ [0007].

regions and thus reduce sheet resistance," *Kim* teaches forming a MSi1-yGey film, such as TiSi1-yGey.[233]

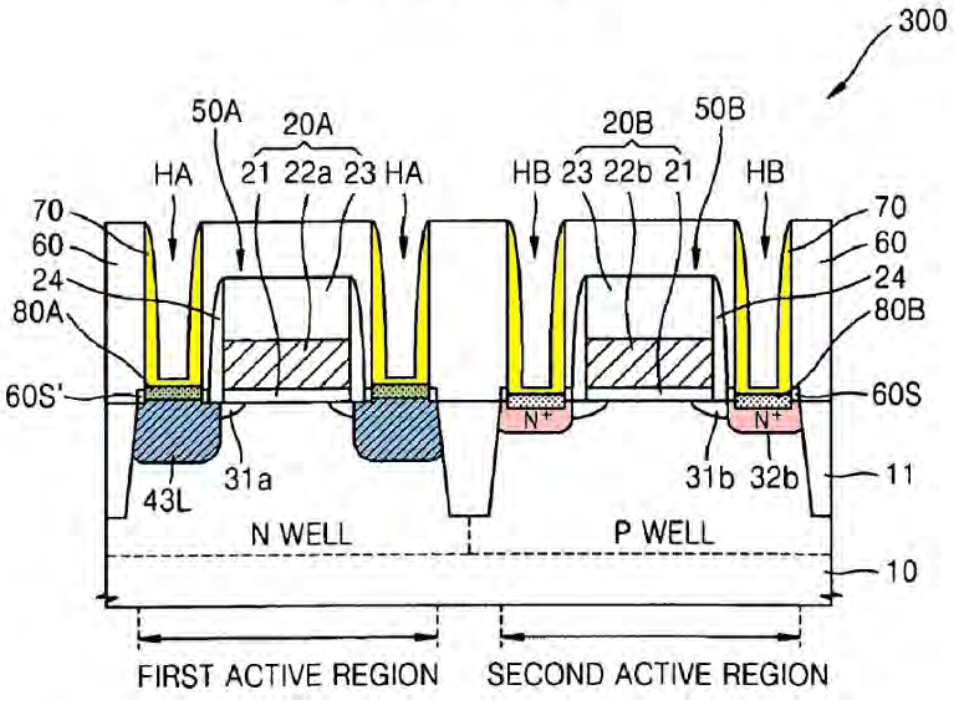
181. As I explain in Section VIII.B, *Kim* describes two basic approaches for forming MSi1-yGey films and contact plugs: Ge Overlayer Metalization and Direct Metalization. In Ge Overlayer Metalization (illustrated in Figure 5 below), a MSi1-yGey film is formed at the interface of a metal and an intermediate Ge layer (red) formed on the source/drain region.In Direct Metalization (illustrated in Figure 3F below), a MSi1-yGey film (green) is formed at the interface of a metal layer and an exposed SiGe source/drain region.

FIG. 5



[233] *Id.* ¶ [0050]; *see also id.* ¶ [0049].

FIG. 3F



182. In both Ge Overlayer Metalization and Direct Metalization, the resulting MSi1-yGey film is described as "a M(Si1-yGey) film containing Ge due to" either Ge atoms in the intermediate Ge layer 45L or Ge atoms in the exposed "SiGe epitaxial layer 43L."[234] One metal "M" *Kim* identifies for metal layer 70 is titanium.[235] When metal layer 70 is titanium, a person of ordinary skill in the art would have understood from *Kim* that metal-semiconductor films 80A are TiSi1-yGey layers formed because the Ti atoms in metal layer 70 will chemically react either with atoms diffused from the source/drain region and the Ge atoms in

[234] *Id.* ¶¶ [0067], [0071], [0073].

[235] *Id.* ¶ [0047].

the thin, intermediate Ge layer 45L (Ge Overlayer Metalization) or with the Si and Ge atoms in the p-type SiGe source/drain regions 43L (Direct Metalization).[236]

183. *Kim* explains that such a TiSi1-yGey film reduces contact resistance to a p-channel FET:

> [D]uring the silicide reaction between the SiGe epitaxial layer 42L and the barrier metal layers 70, Si having reactivity higher than that of Ge reacts more dominantly than Ge. As a result, concentration of Ge increases, a band gap of contact regions may be reduced. The reduced band gap may reduce the height of Schottky barriers and thus contact resistance of the P-channel field-effect transistor 50A may be considerably reduced.[237]

184. Thus, *Kim* teaches forming a TiSi1-yGey film over the source/drain regions of a semiconductor device to reduce contact resistance.

185. *Kim*'s TiSi1-yGey layer is part of a contact structure that facilitates electrical connection to the source/drain regions of a semiconductor device. *Kim* teaches that this TiSi1-yGey layer is desirable because it reduces the contact resistance in the source/drain regions of pFETs like the ones *Ranade* teaches. Accordingly, a person of ordinary skill would have been motivated to add *Kim*'s TiSi1-yGey layer over *Ranade*'s p-type SiGe source/drain regions. A person of ordinary skill in the art would have recognized that *Kim*'s TiSi1-yGey layer would

[236] *See supra* note 164.

[237] *Kim* ¶ [0050].

"reduce the height of Schottky barriers" in *Ranade*'s source/drain regions so the "contact resistance of the P-channel field-effect transistor . . . may be considerably reduced."[238]

b. A person of ordinary skill in the art would have reasonably expected to succeed in completing *Ranade*'s FinFET device by adding a TiSi1-yGey film and contact plugs over *Ranade*'s p-type SiGe source/drain regions

186. As I explain below, a person of ordinary skill in the art would have reasonably expected to succeed in adding *Kim*'s TiSi1-yGey film and contact plugs over *Ranade*'s source/drain regions and to achieve a low Schottky barrier height and low source/drain contact resistance at least because (1) metal-semiconductor layers like *Kim*'s TiSi1-yGey layer were well known prior to 2010 and (2) the metalization techniques *Kim* describes could have been implemented easily and with predictable results on *Ranade*'s FinFET devices.

i. Contact plugs and metal-semiconductor films like *Kim*'s TiSi1-yGey layer were well-known in the semiconductor industry before 2010

187. As I explain in Sections VI.E and VI.F, a person of ordinary skill in the art would have understood that, by December 2010, it was well-known in the semiconductor industry to form contact plugs and metal-semiconductor compounds like *Kim*'s TiSi1-yGey on source/drain regions to lower Schottky

[238] *Id.*

barrier height and reduce contact resistance in SiGe pFETs. One such publication explains: "Metal semiconductor alloys such as metal silicides, metal germanides, metal germano-silicides reduce contact resistance between a metal structure such as a metal contact via structure and a semiconductor region such as a source region, a drain region, and a gate conductor line."[239] Another states: "[I]t is known that . . . forming a silicide film on the source/drain layer of silicon germanium can reduce a resistance of the source/drain layer."[240] A person of ordinary skill in the art would have understood that depositing a metal, such as titanium or nickel, onto the source/drain regions of a device was "a conventional technology . . . to reduce a resistance of the source/drain layer."[241]

188. As I further explain in Sections VI.E and VI.F, techniques for forming contact plugs and metal-semiconductor compounds in a semiconductor device

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[239] *Haran* (US8358012) at 1:10-14; *see also Honeycutt* (US5644166) at 1:8-15, 4:46-53; *Tung* ¶¶ [0005], [0006], [0021], [0027], [0029]-[0032], [0034], [0039], [0061], [0070], [0078]; *Rhee* (US2008/0067545) ¶¶ [0021], [0024], [0025], [0042]; *Murthy* (US6949482) at Abstract, 2:66-3:13, 8:34-9:63, Figs. 5-8; *Yasutake* (US2007/0187767) ¶¶ [0005], [0024], [0025], [0039]-[0045], [0050], [0066], [0070], [0086], [0093]; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, pp. 222-231, at 226 (Mar. 2005); M. Quirk & J. Serda, *Semiconductor Manufacturing Technology* at 214-15, 309-13, Figs. 9.19-9.22, 12.9, 12.14 (1st ed. 2000).

[240] *Yasutake* (US2007/0187767) ¶ [0006].

[241] *Id.* ¶ [0039]; *see also id.* ¶¶ [0005], [0024], [0025], [0039]-[0045], [0050], [0066], [0070], [0086], [0093]; *supra* Sections VI.E, VI.F.

were well known by December 2010. A person of ordinary skill in the art would have understood such metal-semiconductor compounds are formed by depositing a metal onto a semiconductor source/drain region, then heating the structure enough to cause chemical reactions between atoms near the metal-semiconductor interface:

> Formation of metal semiconductor alloys requires an interdiffusion between a metal and a semiconductor material. Typically, the metal is provided as a metal layer, which is deposited after deposition of a dielectric material layer overlying a semiconductor layer and formation of holes within the dielectric material layer to expose the semiconductor material on the top surface of the semiconductor layer. The interface between the metal layer and the underlying semiconductor material is subjected to an anneal at an elevated temperature, typically from 400 degrees Celsius to 700 degrees Celsius, to effect the interdiffusion of the metal and the semiconductor material.[242]

189. A person of ordinary skill in the art also would have known it was routine in the industry to apply this technique to lower Schottky barrier heights and reduce contact resistance in source/drain regions.[243] And a person of ordinary skill in the art would have understood that "[t]he formation details of silicide/germanide regions are known in the art" such that they do not need to be specified.[244]

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[242] *Haran* (US8358012) at 1:10-25; *see also supra* note 67.

[243] *See supra* Sections VI.E, VI.F.

[244] *Yeh* (US9245805) at 4:43-48; *see also Simonelli* (US2010/0148217) ¶ [0043]; *Honeycutt* (US5644166) at 1:8-15, 4:46-53, 5:6-45, 7:20-43, 7:61-8:42; *Yasutake* (US2007/0187767) ¶¶ [0024], [0036], [0050], [0066], [0080], [0093], Fig. 8; *Kim*

190. Thus, by December 2010, a person of ordinary skill in the art would have known that metal-semiconductor films reduce source/drain contact resistance.[245] Moreover, because the basic techniques for forming such metal-semiconductor films were well known and the application of these techniques to source/drain regions was common in the industry,[246] a person of ordinary skill in the art would have found it obvious to apply *Kim*'s TiSi1-yGey film over the source/drain regions in *Ranade*'s FinFET device to reduce contact resistance.

ii. The techniques *Kim* describes would have been implemented with predictable results on *Ranade*'s FinFET device

191. By December 2010, a person of ordinary skill in the art would have understood that *Kim*'s contact plugs and TiSi1-yGey film could be predictably implemented on any FET, including both planar FETs and FinFETs. Accordingly, a person of ordinary skill in the art would have known how to implement *Kim*'s contact plug and TiSi1-yGey films over *Ranade*'s SiGe source/drain regions and

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¶¶ [0047]-[0051], [0057], [0066], [0067]; *Tung* (US2010/0276761) ¶¶ [0042]-[0045], [0063]-[0065], [0067], [0068], [0081]; *Rhee* (US2008/0067545) ¶ [0042], Fig. 7; *Murthy* (US6949482) at 7:11-8:5, Figs. 4a-4c; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 226 (Mar. 2005); M. Quirk & J. Serda, *Semiconductor Manufacturing Technology* at 214-15, 309-13, Figs. 9.19-9.22, 12.9, 12.14 (1st ed. 2000).

[245] *See supra* Sections VI.E, VI.F.

[246] *See id.*

would have recognized that any such implementation would have yielded nothing more than predictable results (e.g., lowering the Schottky barrier height and reducing contact resistance).

192. By its own terms, *Kim*'s invention can be implemented in both planar FETs and FinFETs alike:

> Although a field-effect transistor having a flat channel is described by example herein, it will be understood by one of ordinary skill in the art that many configurations are possible, for example, a metal oxide semiconductor (MOS) transistor having a ***[f]in-type***247 or recessed channel.[248]

193. Moreover, by December 2010, it was widely understood that contact plugs and metal-semiconductor films like *Kim*'s TiSi1-yGey film could be implemented on any type of FET. For example, another document describing

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[247] *Kim* reads: "Although a field-effect transistor having a flat channel is described by example herein, it will be understood by one of ordinary skill in the art that many configurations are possible, for example, a metal oxide semiconductor (MOS) transistor having a ***pin-type*** or recessed channel." *Kim* ¶ [0033]. I am told that *Kim* was originally filed as Korean Patent App. Serial No. 10-2008-0115801. *Kim* ¶ [0001]. Paragraph [0023] of its English translation ("Korean *Kim*"), which I am told is part of the file history in the Korean Intellectual Property Office, reads: "[A]lthough the disclosed embodiments relate to a field effect transistor having a flat channel, this is exemplary, and it will be understood by those skilled in the art that a MOS transistor having a ***fin-shaped*** or recessed channel is also included in the present invention." I have never heard the term "pin-type" in the context of a transistor channel, and a person of ordinary skill in the art would have understood *Kim* refers to a FinFET's raised "fin-type" channel.

[248] *Kim* ¶ [0033].

"metal semiconductor alloy structures for providing low contact resistance" notes: "The structure of the present disclosure can be implemented on any type of field effect transistors including conventional planar field effect transistors and finFETs[.]"[249]

194. Additionally, a person of ordinary skill in the art also would have recognized that the difference in Ge content between *Ranade*'s and *Kim*'s source/drain regions would not have hindered the application of *Kim*'s contact plugs and TiSi1-yGey layer to *Ranade*'s source/drain regions.[250] This is because a person of ordinary skill in the art would have recognized that applying *Kim*'s contact plugs and TiSi1-yGey films to *Ranade*'s SiGe source/drain regions would involve the same, straight-forward processes notwithstanding variations in Ge concentration. One pre-2010 document, for example, describes forming a "metal germanosilicide compound layer" where "the percentage or proportion of germanium to the sum of silicon and germanium [in the source/drain regions] may be about 15~100 percent."[251] *Brask* similarly describes forming a metal-semiconductor alloy over its Si_xGe_{1-x} source/drain regions where "silicon

[249] *Haran* (US8358012) at 14:53-60.

[250] *Kim* states that SiGe source/drain regions 43L in Figure 3F, for example, have a Ge concentration ranging "from about 3% to about 50%," *Kim* ¶ [0063], whereas *Ranade*'s source/drain regions may have a Ge concentration ranging up to 100 atomic %, *Ranade* ¶ [0040].

[251] *Rhee* (US2008/0067545) ¶¶ [0024], [0025]; *see also id.* ¶ [0042].

comprises approximately 1 to 99 atomic percent of the alloy and can even extend to pure (100%) Ge."[252]

195. In view of the widespread application of contact plugs and metal-semiconductor films, including TiSi1-yGey films, on SiGe source/drain regions having various Ge concentrations and geometries, a person of ordinary skill in the art would have reasonably expected to succeed in applying *Kim*'s contact plugs and TiSi1-yGey film to the Si_xGe_{1-x} source/drain regions of *Ranade*'s FinFET. A person of ordinary skill in the art would not have had any reason to think that *Kim*'s metal-semiconductor films would behave any differently than as *Kim* describes when applied to *Ranade*'s FinFET.

c. A person of ordinary skill in the art would have found it obvious to combine *Ranade*'s FinFET with *Kim*'s TiSi1-yGey source/drain contacts

196. As I explain in Section VIII.B, *Kim* describes two processes for forming TiSi1-yGey films: Ge Overlayer Metalization, in which a TiSi1-yGey film is formed at the interface of a metal and an intermediate layer of Ge formed on the source/drain regions, and Direct Metalization, in which a TiSi1-yGey film is formed at the interface of a metal layer and an exposed SiGe source/drain regions.

197. As detailed below, a person of ordinary skill in the art would have found both Ge Overlayer Metalization and Direct Metalization to be obvious and

[252] *Brask* at 10:20-29, 10:50-64, Figs. 4A, 4B.

suitable for forming source/drain contact structures on *Ranade*'s devices. This is because, as *Kim* explains, both processes employ well-known techniques to form TiSi1-yGey films that "reduce the height of Schottky barriers in contact regions," thereby reducing contact resistance.[253] As detailed below, from these two techniques in *Kim*—Ge Overlayer Metalization and Direct Metalization—a person of ordinary skill in the art would have recognized two alternative and obvious modifications of *Ranade*'s FinFET device.

i. *Kim*'s Ge Overlayer Metalization and the First Obvious Modification of *Ranade*

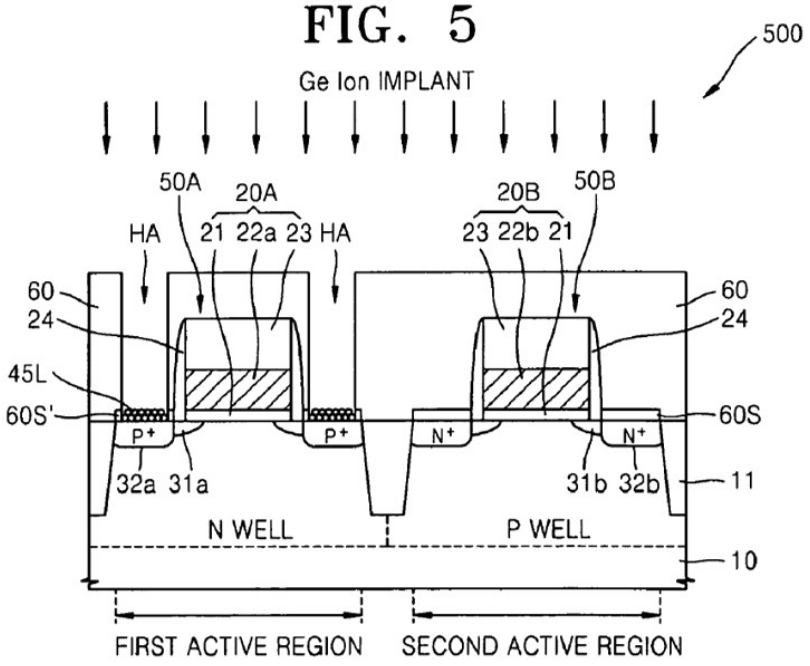
198. As I explain in Section VIII.B, *Kim* describes Ge Overlayer Metalization, discussed further below, for forming contact plugs and a TiSi1-yGey film at the interface of a metal layer and a thin, intermediate Ge Overlayer. *Kim*'s Ge Overlayer Metalization would have led a person of ordinary skill in the art to make the first obvious modification of *Ranade*, discussed below.

199. *Kim*'s Ge Overlayer Metalization for forming a TiSi1-yGey film, described in connection with Figure 5, includes five steps: (1) Etch Contact Holes; (2) Form a Ge Overlayer; (3) Deposit Titanium; (4) Anneal to Form TiSi1-yGey; and (5) Form Contact Plugs. I describe each of these steps below.

[253] *Kim* ¶ [0050]; *see also* Section VI.C above for a discussion of Schottky barriers and the reduction of contact resistance. The '281 Patent itself also recognizes that reducing the Schottky barrier height reduces contact resistance. *See* '281 Patent at 14:48-57.

200. ***Etch Contact Holes.*** As Figure 5 below illustrates, for example, an "interlayer insulating film 60B may be formed on a substrate 10" of *Kim*'s semiconductor device."[254] Using "an appropriate mask," "[f]irst contact holes HA" are etched in the interlayer insulating film 60.[255] The contact holes HA are over source/drain regions 32a, as shown.[256]

FIG. 5



201. ***Form a Ge Overlayer.*** *Kim*'s process continues with the formation of an intermediate Ge Overlayer over source/drain regions 32a. In Figure 5, the

[254] *Kim* ¶¶ [0070], [0072].

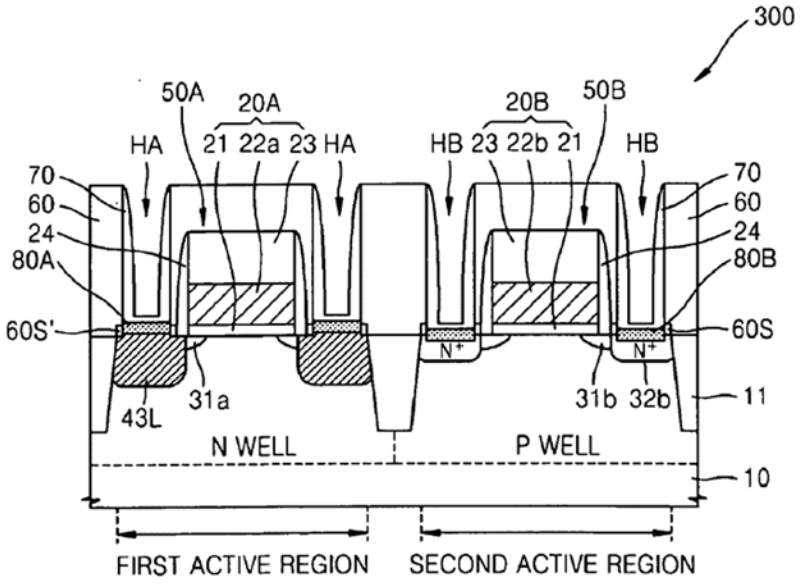
[255] *Id.*

[256] *Id.* ¶¶ [0052], [0072].

intermediate Ge Overlayer 45L is formed, for example, by "pulsed laser ablation deposition (PLAD) and/or a gas cluster ion beam (GCIB) deposition."[257]

202. ***Deposit Titanium.*** *Kim*'s process continues with deposition of metal layer 70 into contact holes HA "as described above with reference to FIG. 3F," shown below.[258] *Kim* identifies titanium for use as metal layer 70, which a person of ordinary skill in the art would have understood to be a conventional choice.[259]

FIG. 3F



203. ***Anneal to Form TiSiGe.*** As in *Kim*'s Direct Metalization, *Kim*'s Ge Overlayer Metalization continues with an annealing step after metal layer 70 has

[257] *Id.* ¶ [0073].

[258] *Kim* ¶¶ [0070], [0073].

[259] *Id.* ¶ [0047].

been deposited into contact holes HA, thereby forming TiSi1-yGey.[260] *Kim* explains: "The silicide film 80A in the first contact holes HA may be a M(Si1-yGey) film including the Ge atomic layer 45L," where "M" represents the metal of metal layer 70.[261] When metal layer 70 is titanium, a person of ordinary skill in the art would have understood from *Kim* that films 80A are TiSi1-yGey layers formed because the Ti atoms in metal layer 70 will chemically react with atoms diffused from the source/drain region and the Ge atoms in the thin, intermediate Ge layer 45L.[262] This is the only source of Si for the TiSi1-yGey layer, and such diffusion would be expected since the disclosed deposition techniques (ion implantation, pulsed laser ablation deposition, and gas cluster ion beam deposition) are typically used to slowly deposit stacked atomic layers like *Kim*'s layer 45L.[263]

204. ***Form Contact Plugs.*** A person of ordinary skill in the art would have understood from *Kim* that "[c]ontact plugs . . . may be formed on the silicide

[260] *Id.* ¶¶ [0071], [0073].

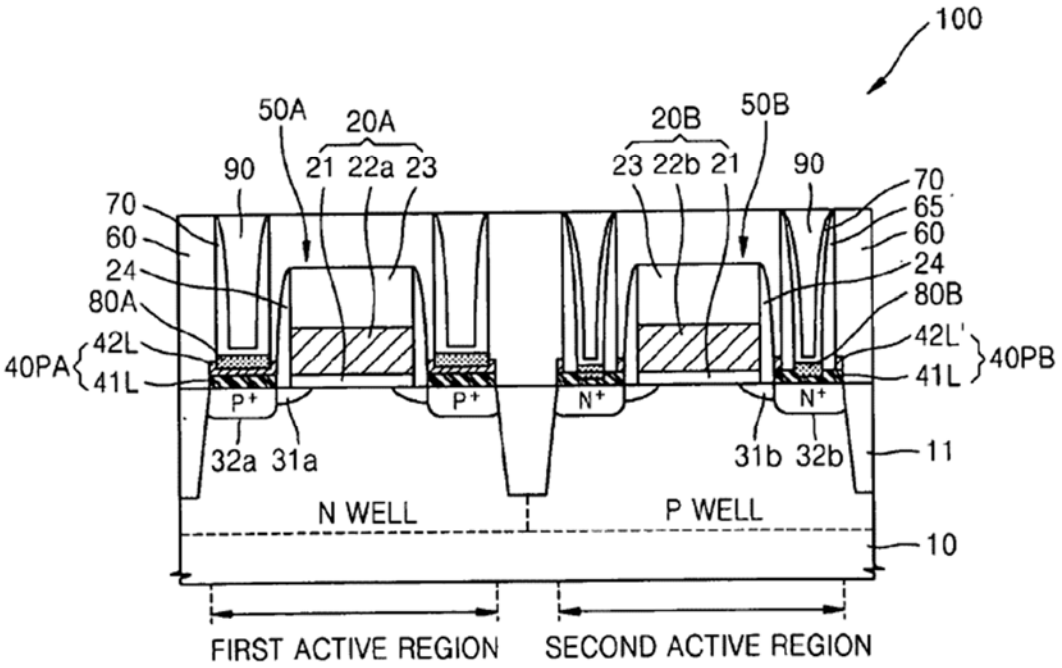
[261] *Id.* ¶ [0073].

[262] *See supra* note 155.

[263] *See Kim* ¶¶ [0072], [0073].

films 80A" in contact holes HA.[264] Although not illustrated in Figure 5, *Kim*'s Figure 1F below illustrates contact plugs 90 formed on TiSi1-yGey films 80A.[265]

FIG. 1F



205. As I explain below, a person of ordinary skill in the art would have been motivated to perform the steps of *Kim*'s Ge Overlayer Metalization—(1) Etch Contact Holes; (2) Form Ge Overlayer; (3) Deposit Titanium; (4) Anneal to Form TiSiGe; and (5) Form Contact Plugs—on *Ranade*'s FinFET device and would have reasonably expected to succeed in doing so.

[264] *Kim* ¶ [0068].

[265] *See id.* ¶ [0049], Fig. 1F.

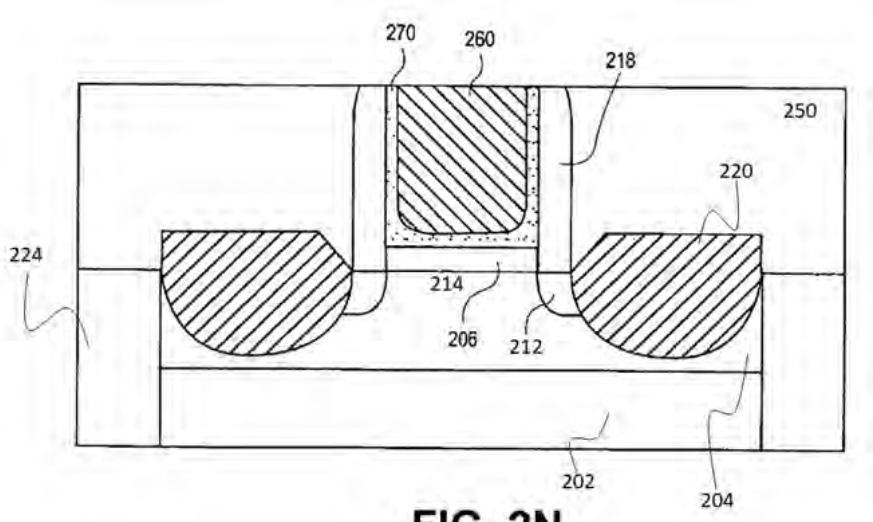


FIG. 2N

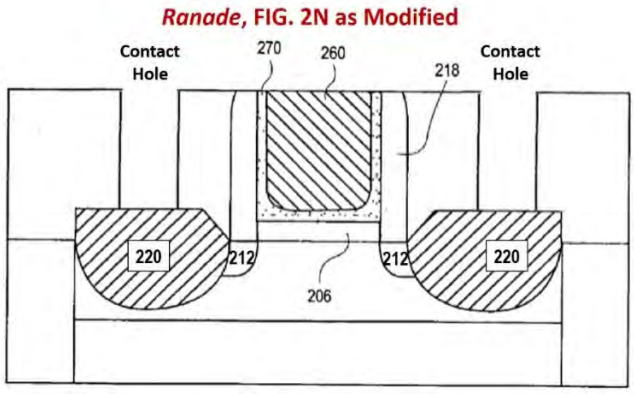
206. Figure 2N above, onto which I have copied additional reference numerals from Figures 2A-2M for clarity, approximates *Ranade*'s FinFET device in cross-section. Like *Kim*'s device, which can also be a FinFET,[266] *Ranade*'s FinFET device includes a substrate 202, epitaxial Si_xGe_{1-x} source/drain regions 220, and an interlayer dielectric 250.[267] Similarly, *Kim*'s device structure includes a substrate 10, an interlayer insulating film 60, and source/drain regions 32a.

207. ***Etch Contact Holes.*** Just as *Kim* teaches etching contact holes HA in *Kim*'s interlayer insulating film 60, a person of ordinary skill in the art would have found it obvious to etch contact holes in *Ranade*'s dielectric layer 250 as illustrated in the figure below (which I created for illustrative purposes by modifying

[266] *See supra* note 247.

[267] *Ranade* ¶¶ [0026], [0040], [0041].

Figure 2N of *Ranade* to reflect *Kim*'s teachings). The contact holes would be formed using, for example, a mask printed with the source/drain contact pattern and a well-known etch technique, as *Kim* recommends.[268] As shown below, the contact holes expose *Ranade*'s Si_xGe_{1-x} source and drain regions 220.



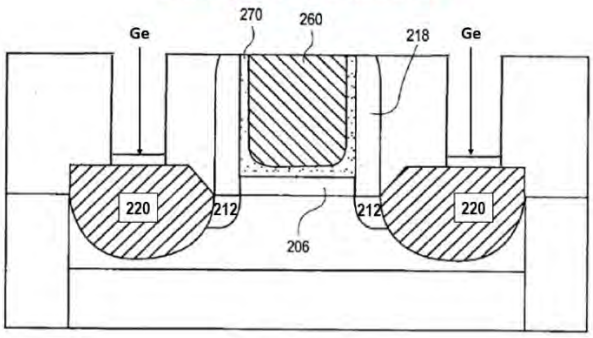
208. ***Form Ge Overlayer.*** Then, just as *Kim* teaches forming a thin, intermediate Ge layer 45L on the source/drain regions 32, a person of ordinary skill in the art would have been motivated to form a Ge Overlayer on *Ranade*'s source/drain regions and would have reasonably expected to succeed in doing so as illustrated in the figure below (which I created for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings). The Ge Overlayer would be formed using, for example, the well-known techniques *Kim* identifies, including pulsed laser ablation deposition and/or gas cluster ion beam deposition.[269] For the reasons I detail in Section VI.C, a person of ordinary skill in

[268] *Kim* ¶¶ [0061], [0062], [0070], [0072].

[269] *Id.* ¶¶ [0070], [0072], [0073].

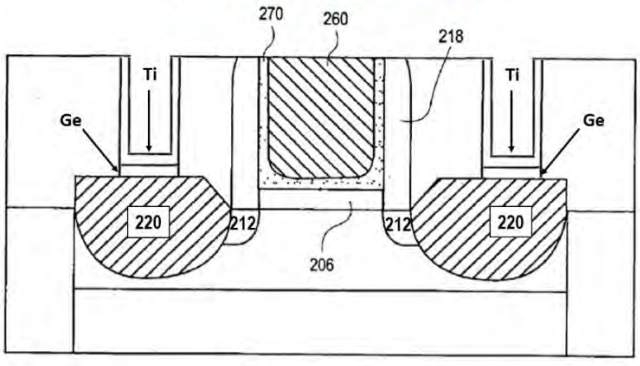
the art would have been motivated to use a Ge Overlayer to minimize the Schottky barrier height and, with it, source/drain contact resistance.

Ranade, FIG. 2N as Modified



209. ***Deposit Titanium*.** Next, just as *Kim* teaches depositing a titanium metal layer 70 into contact holes HA, a person of ordinary skill in the art would have found it obvious to deposit Ti into the contact holes formed in *Ranade*'s dielectric layer 250 as shown in the figure below (which I created for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings). The Ti would be deposited using a well-known deposition technique, as *Kim* recommends.[270]

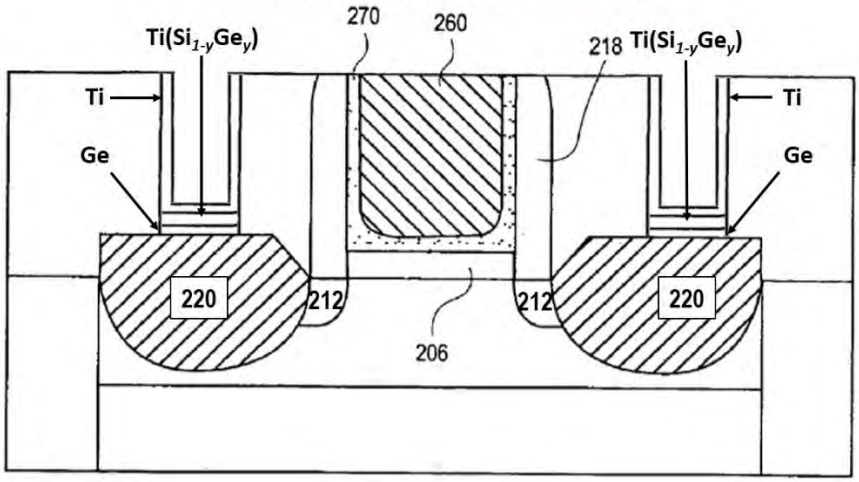
Ranade, FIG. 2N as Modified



[270] *Id.* ¶ [0066].

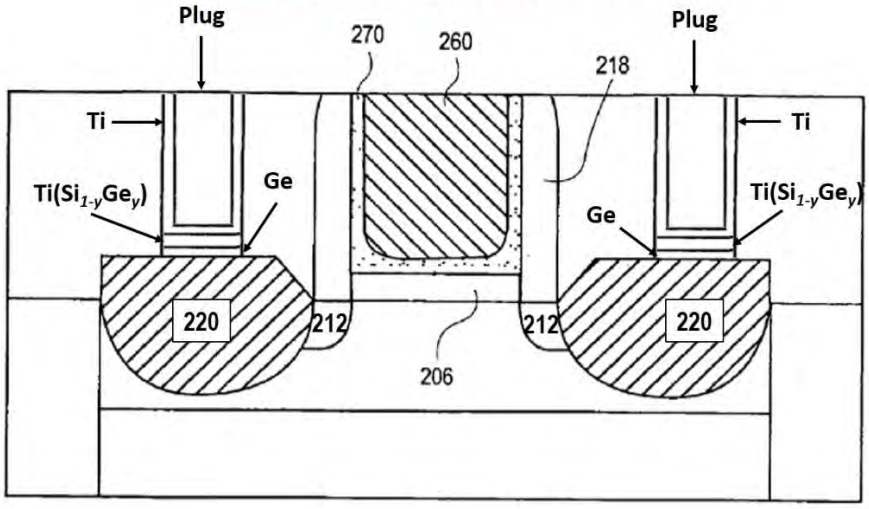
210. ***Anneal to Form TiSiGe.*** Just as *Kim* teaches annealing the deposited metal layer 70 and causing it to react with intermediate Ge layer 45L to form a TiSi1-yGey film 80A, a person of ordinary skill in the art would have found it obvious to anneal the Ti layer above and cause it to react with diffused atoms from *Ranade*'s source/drain region and Ge atoms in the thin Ge Overlayer to form TiSi1-yGey. The figure below (which I created for illustrative purposes by modifying *Ranade*'s Figure 2N to reflect *Kim*'s teachings) shows this chemical reaction.

***Ranade*, FIG. 2N as Modified**



211. ***Form Contact Plugs.*** Finally, just as *Kim* teaches forming contact plugs 90 in the contact holes HA, a person of ordinary skill in the art would have found it obvious to form contact plugs in the contact holes above. The figure below (which I created for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings) illustrates the contact plugs.

***Ranade*, FIG. 2N as Modified**



212. To summarize, *Ranade* explains that its FinFET is completed using "typical process steps to complete the formation of a MOS-FET, . . . such as a silicidation step."[271] *Kim* discloses such a silicidation step—namely, Ge Overlayer Metalization.[272] Accordingly, a POSITA would have found a combination of *Ranade* and *Kim* that resembles the figure above to have been obvious. The figure above (which I created for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings) illustrates the final *Ranade-Kim* combination pursuant to *Kim*'s Ge Overlayer Metalization. I have labeled this figure "***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**." In my analysis below, I use this figure to illustrate how the First Obvious Modification of *Ranade* would have rendered the Challenged Claims obvious.

[271] *Ranade* ¶ [0041].

[272] *Kim* ¶¶ [0072]-[0074], Fig. 5.

ii. *Kim*'s Direct Metalization and the Second Obvious Modification of *Ranade*

213. As I explain in Section VIII.B, *Kim* also describes Direct Metalization for forming contact plugs and a TiSi1-yGey film formed at the interface of a metal layer and SiGe source/drain regions. *Kim*'s Direct Metalization would have led a person of ordinary skill in the art to make the Second Obvious Modification to *Ranade*, discussed below, an alternative to the First Obvious Modification of *Ranade*.

214. *Kim*'s Direct Metalization for forming a TiSi1-yGey film, described in connection with Figures 3D to 3F, includes four steps: (1) Etch Contact Holes; (2) Deposit Titanium; (3) Anneal to Form TiSi1-yGey; and (4) Form Contact Plugs. I describe each of these steps below.

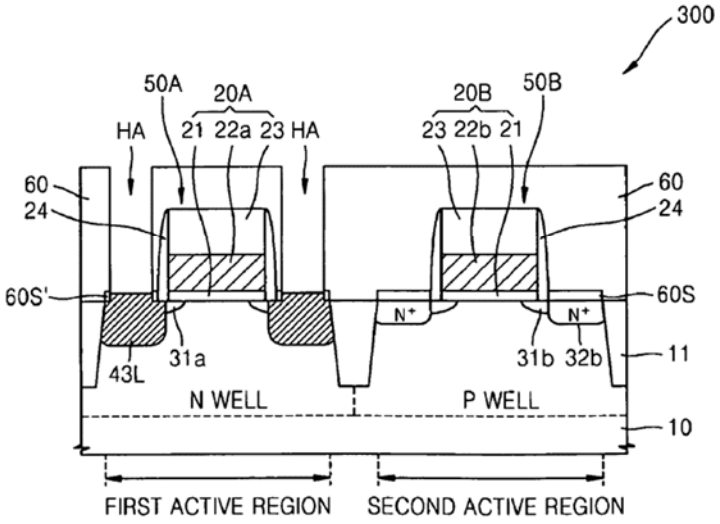
215. ***Etch Contact Holes.*** As Figure 3D below shows, an "interlayer insulating film 60B may be formed on the substrate 10" of *Kim*'s semiconductor device."[273] Using a mask M1, "first contact holes HA" are etched in the interlayer insulating film 60.[274] For this, *Kim* describes several well-known etching techniques, such as "a reactive ion etch."[275]

[273] *Kim* ¶ [0060].

[274] *Id.* ¶ [0061].

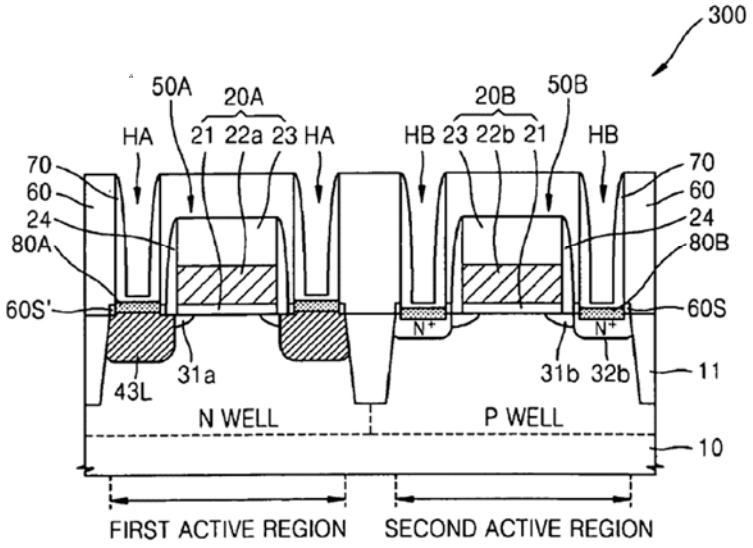
[275] *Id.* ¶ [0062].

FIG. 3D



216. ***Deposit Titanium.*** *Kim*'s process continues with the deposition of a metal layer 70 in the contact holes HA, as Figure 3F below shows.[276] One metal *Kim* identifies for use as metal layer 70 is titanium.[277]

FIG. 3F



[276] *Id.* ¶ [0066].

[277] *Id.* ¶ [0047].

217. ***Anneal to Form TiSi1-yGey.*** Once a titanium metal layer 70 has been deposited into contact holes HA, the metal layer is thermally annealed. "Due to thermal annealing," *Kim* explains, the TiSi1-yGey film "may be formed on the first active region between the barrier metal layers 70 and the SiGe epitaxial layer 43L," as Figure 3F above shows.[278] *Kim* describes such a film as "a M(Si1-yGey) film containing Ge due to the exposed SiGe epitaxial layer 43L," where "M" represents the metal of metal layer 70.[279] Again, *Kim* teaches that metal layer 70 may be titanium.[280] When metal layer 70 is titanium, a person of ordinary skill in the art would have understood from *Kim* that films 80A are TiSi1-yGey layers formed because the Ti atoms in metal layer 70 will chemically react with Si and Ge atoms in the SiGe source/drain regions 43L.[281]

218. ***Form Contact Plugs.*** Finally, *Kim* teaches that "[c]ontact plugs . . . may be formed on the silicide films 80A" in the contact holes HA.[282] Although not

[278] *Id.* ¶ [0067].

[279] *Id.*; *see also id.* ¶¶ [0047]-[0050], [0057], [0071].

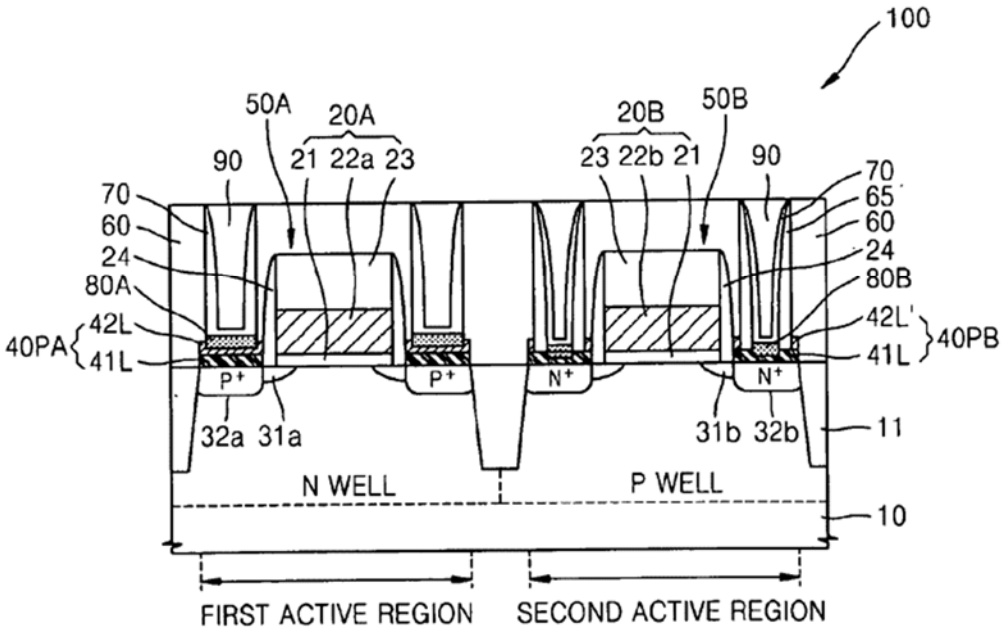
[280] *Id.* ¶ [0047].

[281] *See supra* note 164.

[282] *Kim* ¶ [0068].

illustrated in Figure 3F, Figure 1F below depicts contact plugs 90 formed on the silicide films 80A.[283]

FIG. 1F



219. As I explain below, a person of ordinary skill in the art would have been motivated to perform the steps of *Kim*'s Direct Metalization—(1) Etch Contact Holes; (2) Deposit Titanium; (3) Anneal to Form TiSiGe; and (4) Form Contact Plugs—on *Ranade*'s FinFET device and would have reasonably expected to succeed in doing so. This Second Obvious Modification of *Ranade* would have been an obvious alternative to the First Obvious Modification of *Ranade*.

[283] *Id.* ¶ [0049] (describing contact plugs 90 in Figure 1F), ¶ [0068] (referencing Figure 1F in connection with Figure 3F).

220. Figure 2N below, onto which I have copied additional reference numerals from Figures 2A-2M for clarity, approximates *Ranade*'s FinFET device in cross-section. Like *Kim*'s device, which can also be a FinFET,[284] *Ranade*'s FinFET device includes a substrate 202, epitaxial Si_xGe_{1-x} source/drain regions 220, and an interlayer dielectric 250.[285] Similarly, *Kim*'s device includes a substrate 10, an interlayer insulating film 60, and epitaxial SiGe source/drain regions 43L.

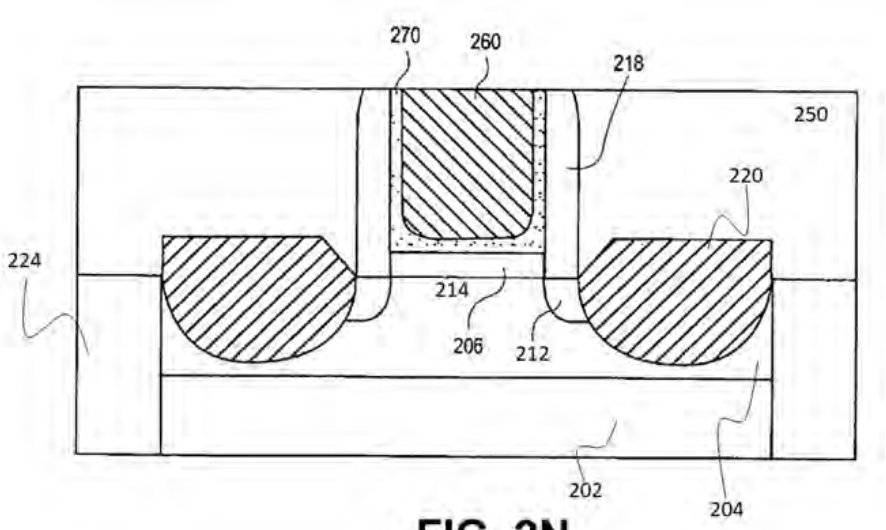


FIG. 2N

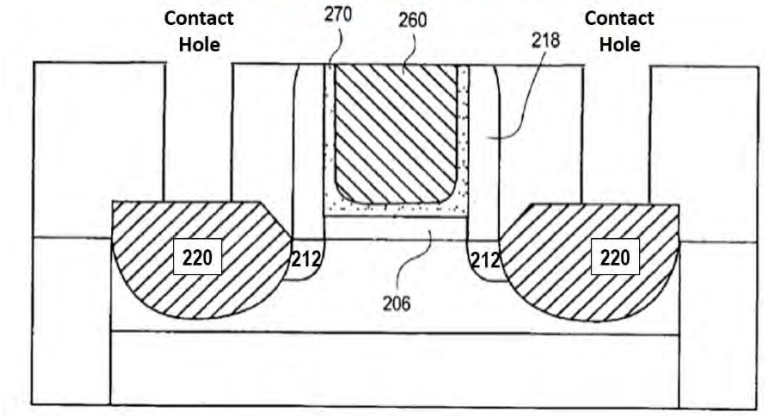
221. ***Etch Contact Holes.*** Just as *Kim* teaches etching contact holes HA in *Kim*'s interlayer insulating film 60, a person of ordinary skill in the art would have found it obvious to etch contact holes in *Ranade*'s dielectric layer 250 as illustrated in the figure below (which I created for illustrative purposes by modifying

[284] *See supra* note 247.

[285] *Ranade* ¶¶ [0026], [0040], [0041].

Figure 2N of *Ranade* to reflect *Kim*'s teachings). The contact holes would be formed using, for example, a mask printed with the source/drain contact pattern and a well-known etch technique, as *Kim* recommends.[286] As shown below, the contact holes expose *Ranade*'s epitaxial Si_xGe_{1-x} source and drain regions 220.

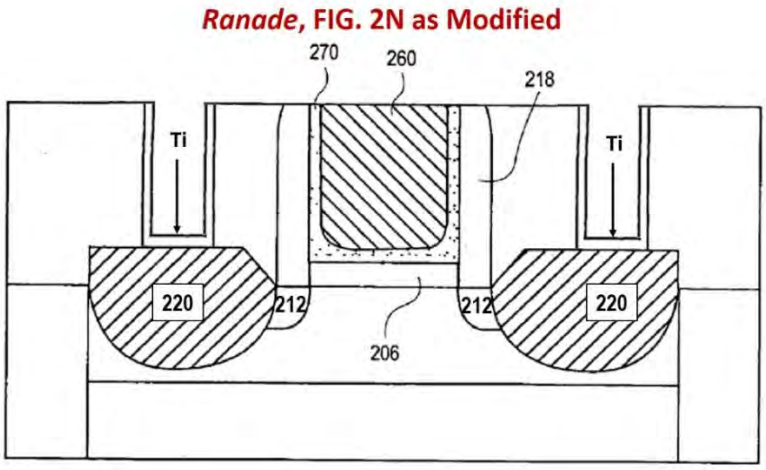
***Ranade*, FIG. 2N as Modified**



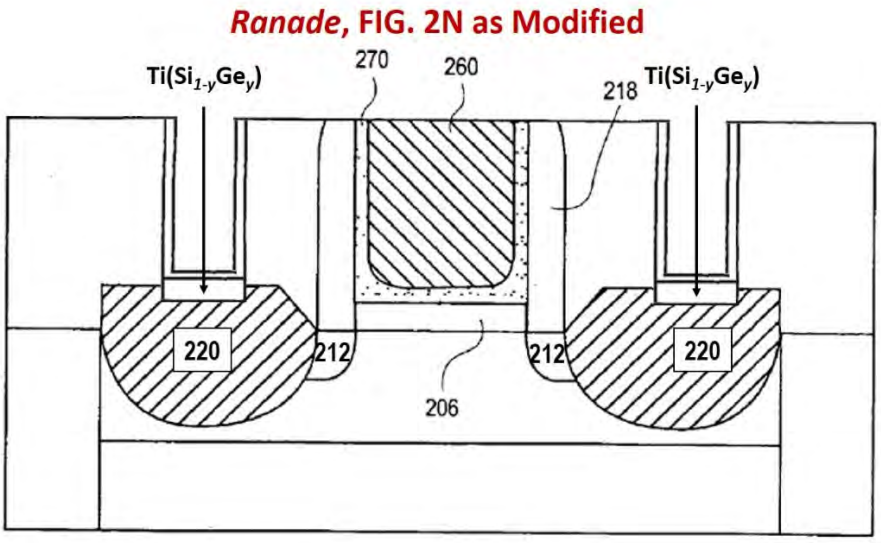
222. ***Deposit Titanium*.** Next, just as *Kim* teaches depositing a titanium metal layer 70 into contact holes HA, a person of ordinary skill in the art would have found it obvious to deposit Ti into the contact holes formed in *Ranade*'s dielectric layer 250 as shown in the figure below (which I created for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings). The Ti would be deposited using a well-known deposition technique, as *Kim* recommends.[287]

[286] *Kim* ¶¶ [0061], [0062].

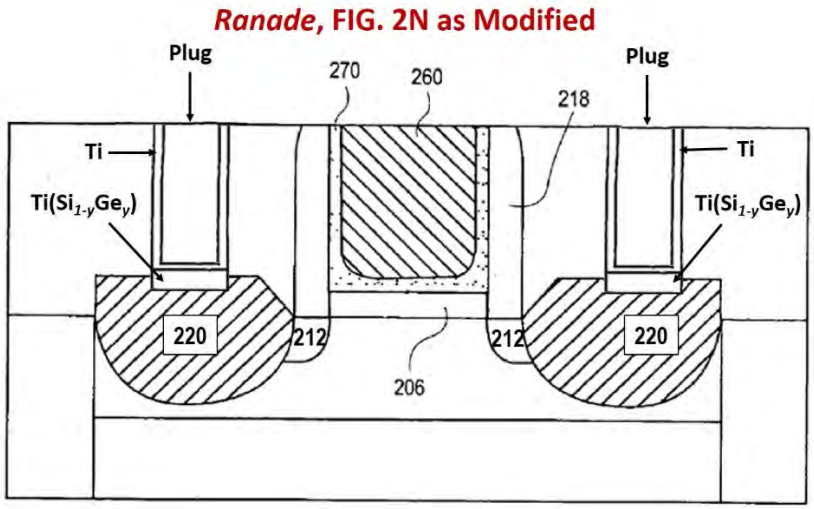
[287] *Id.* ¶ [0066].



223. ***Anneal to Form TiSiGe.*** Just as *Kim* teaches annealing the deposited metal layer 70 and causing it to react with SiGe source/drain regions 43L to form a TiSi1-yGey film 80A, a person of ordinary skill in the art would have found it obvious to anneal the Ti layer above and cause it to react with Si_xGe_{1-x} source/drain regions 220 to form TiSi1-yGey. The figure below (which I created for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings) illustrates this chemical reaction, which involves interdiffusion.



224. ***Form Contact Plugs.*** Finally, just as *Kim* teaches forming contact plugs 90 in contact holes HA, a person of ordinary skill in the art would have found it obvious to deposit contact plugs in the contact holes above. The figure below (which I created for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings) illustrates the contact plugs.



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

225. To summarize, *Ranade* explains that its FinFET is completed using "typical process steps to complete the formation of a MOS-FET, . . . such as a silicidation step."[288] *Kim* discloses such a silicidation step—namely, Direct Metalization.[289] Accordingly, a POSITA would have found a combination of *Ranade* and *Kim* that resembles the figure above to have been obvious. The figure above (which I created for illustrative purposes by modifying Figure 2N of *Ranade*

[288] *Ranade* ¶ [0041].

[289] *Kim* ¶¶ [0048]-[0050], [0066]-[0068], Fig. 3F.

to reflect *Kim*'s teachings) illustrates the final *Ranade-Kim* combination pursuant to *Kim*'s Direct Metalization. I have labeled this figure "***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**." In my analysis below, I use this figure to illustrate how the Second Obvious Modification of *Ranade* would have rendered the Challenged Claims obvious.

d. Exemplary Rationales for Completing *Ranade*'s FinFET Device Using *Kim*'s Teachings

226. In my opinion, a person of ordinary skill in the art would have applied any one or more of the following four rationales among those I have been asked to consider to arrive at such a structure.

227. First, a person of ordinary skill in the art would have considered adding a source/drain contact structure with contact plugs and a TiSi1-yGey layer over *Ranade*'s p-type Si_xGe_{1-x} source/drain regions to be an example of combining known elements in the prior art according to known methods to yield predictable results. A person of ordinary skill in the art would have understood how to combine *Kim*'s contact plugs and TiSi1-yGey layer with *Ranade*'s p-type SiGe source/drain regions using the known methods *Kim* describes—i.e., depositing titanium either onto an intermediate Ge Overlayer (Ge Overlayer Metalization) or directly onto *Ranade*'s p-type SiGe source/drain regions (Direct Metalization) and then annealing and forming contact plugs. A person of ordinary skill in the art also would have understood that doing so should yield predictable results—namely, a

lower Schottky barrier height at the metal-semiconductor interface of *Ranade*'s source/drain contact structures and a FinFET device with reduced contact resistance.

228. Second, a person of ordinary skill in the art would have considered adding a source/drain contact structure with contact plugs and a TiSi1-yGey layer over *Ranade*'s p-type Si_xGe_{1-x} source/drain regions to be an example of using a known technique to improve similar devices the same way. A person of ordinary skill in the art would have understood how to combine *Kim*'s TiSi1-yGey layer with *Ranade*'s p-type SiGe source/drain regions using the known techniques *Kim* describes—i.e., depositing titanium either onto an intermediate Ge Overlayer (Ge Overlayer Metalization) or directly onto *Ranade*'s p-type SiGe source/drain regions (Direct Metalization) and then annealing and forming contact plugs. A person of ordinary skill in the art also would have understood that doing so should improve similar devices the same way—namely, by lowering Schottky barrier height at the metal-semiconductor interface of *Ranade*'s source/drain contact structures, just as with *Kim*'s source/drain contact structures, to provide a FinFET with less contact resistance.

229. Third, a person of ordinary skill in the art would have considered adding a source/drain contact structure with contact plugs and a TiSi1-yGey layer over *Ranade*'s p-type Si_xGe_{1-x} source/drain regions to be an example of applying a

known technique to a known device ready for improvement to yield predictable results. A person of ordinary skill in the art would have understood how to combine *Kim*'s TiSi1-yGey layer with *Ranade*'s p-type SiGe source/drain regions using the known techniques *Kim* describes—i.e., depositing titanium either directly onto an intermediate Ge Overlayer (Ge Overlayer Metalization) or onto *Ranade*'s p-type SiGe source/drain regions (Direct Metalization) and then annealing and forming contact plugs. A person of ordinary skill in the art also would have understood that *Ranade* does not describe a contact structure in detail and would be readily improved by adopting a contact structure like *Kim*'s. Moreover, a person of ordinary skill in the art would have understood that doing so should yield predictable results—namely, a lower Schottky barrier height at the metal-semiconductor interface of *Ranade*'s source/drain contact structures and a FinFET device with reduced contact resistance.

230. Fourth, a person of ordinary skill in the art would have thought to add a source/drain contact structure with contact plugs and a TiSi1-yGey layer over *Ranade*'s p-type Si_xGe_{1-x} source/drain regions due to a teaching, suggestion, or motivation in the prior art to arrive at the claimed invention. A person of ordinary skill in the art would have been familiar with several teachings, suggestions, or motivations in the prior art, including those provided in *Ranade* and *Kim*

themselves[290] and in other references such as those I discuss in Sections VI.C, VI.E, and VI.F above, and including the general need to reduce source/drain contact resistance in FinFETs like *Ranade*'s. In applying those teachings, suggestions, or motivations as I describe above, a person of ordinary skill in the art would have arrived at the claimed invention.

231. Regardless of the rationale a person of ordinary skill in the art would have applied, it is my opinion that he or she would have found the two alternative combinations of *Ranade* and *Kim* discussed above to be obvious.[291]

2. A Person of Ordinary Skill in the Art Would Have Found It Obvious to Use *Ranade*'s FinFETs, as Implemented According to *Kim*, in Typical Computing Devices Like Smartphones

232. By December 2010, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices, like the ones *Ranade* discloses (including as implemented according to *Kim*'s teachings as described above) into smartphones, computers, and other typical consumer

[290] *See, e.g.*, *Kim* ¶¶ [0003]-[0007], [0010], [0047], [0050], [0071], [0074]; *Ranade* ¶¶ [0038], [0041].

[291] *See supra* Sections VI.C, VI.E, VI.F, IX.A.1.a-d.

electronic devices. To provide a frame of reference for the types of features and peripherals in use at the time, the iPhone 4 was released on June 24, 2010.[292]

233. A person of ordinary skill in the art would have found it obvious to implement FinFETs like *Ranade*'s into computing devices like smartphones for at least the following four rationales among those I have been asked to consider.

234. First, a person of ordinary skill in the art would have considered it an example of combining prior art elements according to known methods to yield predictable results. Both *Ranade*'s FinFET devices (including as implemented according to the teachings of *Kim* as described above) and typical integrated circuits used in smartphones and other computing devices were prior art elements known to a person of ordinary skill in the art well before December 2010, and combining them would involve only known methods—namely, standard integrated circuit and consumer electronics manufacturing processes. And the combination would yield only predictable results, such as a smartphone or other computing device that includes a circuit board with integrated circuits containing FinFETs.

235. Second, a person of ordinary skill in the art would have considered it an example of using a known technique to improve similar devices in the same way. A person of ordinary skill in the art would have known how to incorporate

[292] *See* https://www.apple.com/newsroom/2010/06/07Apple-Presents-iPhone-4.

FinFET devices like *Ranade*'s (including as implemented according to the teachings of *Kim* as described above) into the typical integrated circuits used in smartphones and other computing devices, and he or she would have been able to incorporate *Ranade*'s FinFET devices (including as implemented according to the teachings of *Kim* as described above) into such integrated circuits to improve the speed and performance of smartphones and other computing devices, just as any improved FET device would.

236. Third, a person of ordinary skill in the art would have considered this to be an example of applying a known technique—using FET devices like *Ranade*'s FinFETs (including as implemented according to the teachings of *Kim* as described above) in integrated circuits—to a known device, such as a smartphone or computing device, that was ready for improvement. A person of ordinary skill in the art would have recognized that such devices are continually being improved by semiconductor scaling, as well as the fact that *Ranade* and *Kim* would further that trend. For example, a person of ordinary skill in the art would have recognized that using *Ranade*'s FinFETs in smartphones and other computing devices should increase switching speeds and reduce power consumption and heating due to less source/drain contact resistance.

237. Fourth, a person of ordinary skill in the art, knowing of the motivation in the industry to improve smartphones and other computing devices, would have

been led to incorporate *Ranade*'s FinFET devices (including as implemented according to the teachings of *Kim* as described above) into integrated circuits for use in smartphones and other typical computing devices. By doing so, the person of ordinary skill in the art would have arrived at a smartphone or other typical computing device that includes such FinFETs.

238. Regardless of the rationale a person of ordinary skill in the art would have applied, he or she would have found it obvious to use devices like *Ranade*'s (including as implemented according to the teachings of *Kim* as described above) in smartphones or other computing devices. In fact, it would have been a given; it is the primary application of all FETs and the reason FinFETs were developed in the first place.

3. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 1 Obvious

a. Claim Element [1.0]: The Preamble

239. Claim 1 recites "[a]n integrated circuit structure." *Ranade*, as implemented according to by *Kim*, discloses "[a]n integrated circuit structure."

240. *Ranade* teaches a FinFET device that resembles Figure 2N below:

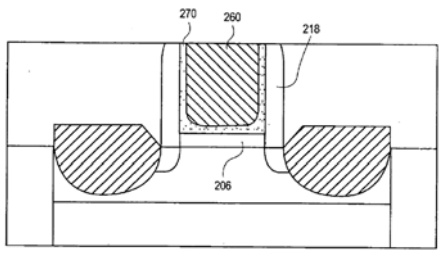


FIG. 2N

241. *Ranade* recognizes that "[s]emiconductor structures having active regions," as shown in *Ranade*'s Figure 2N, "may be used to form semiconductor devices."[293] Although Figure 2N depicts a planar FET device, a person of ordinary skill in the art would have understood that the same teachings apply to *Ranade*'s FinFET device. *Ranade* explains that "[t]he present invention is not limited to the formation of planar MOS-FETs" but also applies to "devices with a three-dimensional architecture, such as tri-gate devices" like the FinFET shown in *Ranade*'s Figure 3C below.[294]

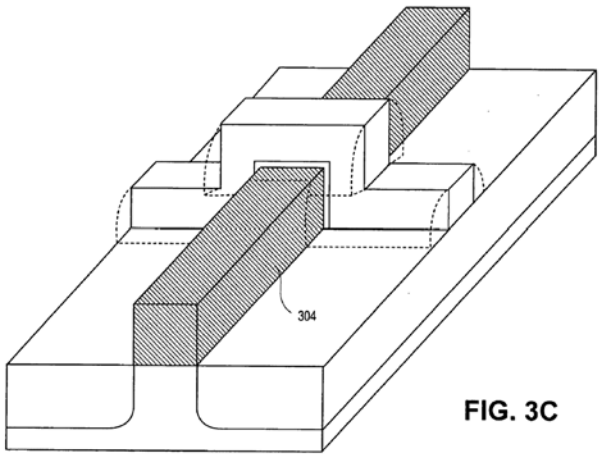


FIG. 3C

242. *Ranade* explains that such semiconductor devices "may be incorporated into an integrated circuit."[295] *Ranade* recognizes that such incorporation into an integrated circuit was well known: "The tri-gate MOS-FET

[293] *Ranade* ¶ [0025].

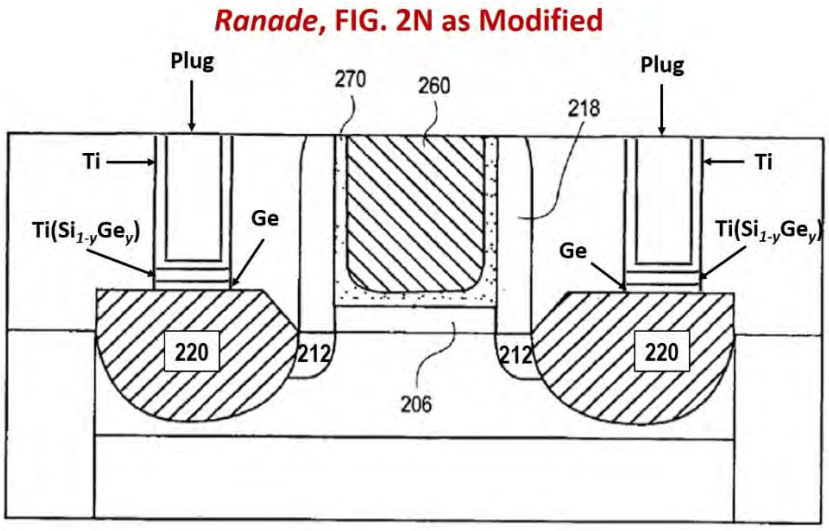
[294] *Id.* ¶ [0044]; *see also id.* ¶ [0025], *supra* note 10 and related text.

[295] *Id.* ¶ [0043].

may be incorporated into an integrated circuit by conventional processing steps, as known in the art."[296]

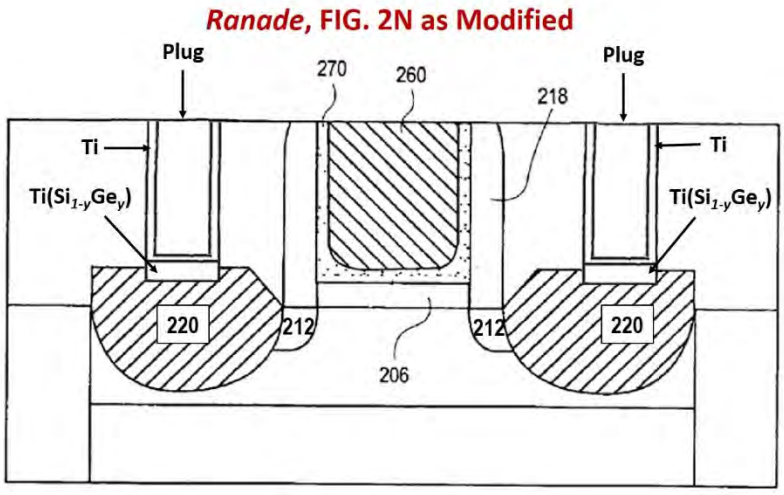
243. Because *Ranade* thus teaches incorporating its FinFET device structure into an integrated circuit "by conventional steps, as known in the art," a person of ordinary skill in the art would have understood *Ranade* teaches "an integrated circuit."

244. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFET device according to either the First Obvious Modification (Ge Overlayer Metalization) or the Second Obvious Modification (Direct Metalization) based on *Kim*, as the figures below illustrate. I created these figures for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings.



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**

[296] *Id.* ¶ [0046].



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

245. A person of ordinary skill in the art would have recognized that *Ranade*'s semiconductor devices, including when implemented according to *Kim* in these ways, would be incorporated into an integrated circuit using "conventional processing steps, as known in the art."[297] Accordingly, a person of ordinary skill in the art would have understood the combination of *Ranade* and *Kim* discloses "an integrated circuit."

b. Claim Element [1.1]: Fin

246. Claim 1 recites "a fin comprising silicon." The asserted combinations of *Ranade* and *Kim* both include "a fin comprising silicon."

[297] *Id.* ¶ [0046]; *see also Kim* at Title, Abstract, ¶¶ [0002]-[0008], [0010]-[0019], [0034]-[0074], Figs. 1A-5 (all describing "semiconductor device[s]" like "field-effect transistors" similar to *Ranade*'s and for use in integrated circuits).

247. *Ranade* teaches a FinFET device similar to what Figure 2N below shows (onto which I have copied additional reference numerals from Figures 2A-2M for clarity).[298] As shown below, the FinFET device includes a substrate 202, an active region 204, source/drain regions 220, and source/drain tip extensions 212.

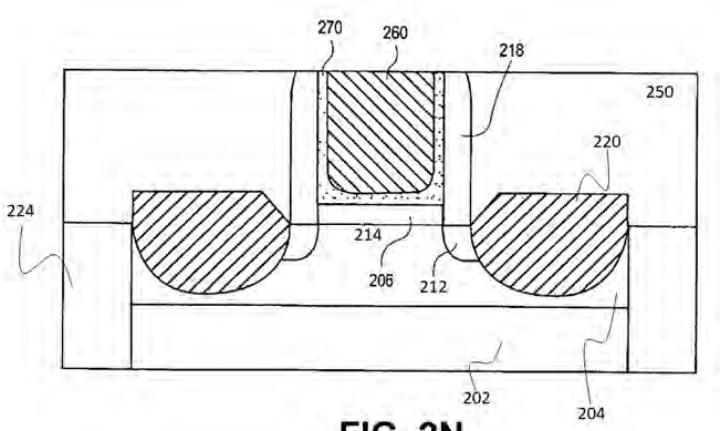


FIG. 2N

248. According to *Ranade*, substrate 202 may be Si or SiGe, and active region 204 is "crystalline silicon/germanium" with "the stoichiometry Si_xGe_{1-x}, where $0 \leqq x \leqq 1$."[299] Epitaxial source/drain regions 220 are also "crystalline silicon/germanium" and similarly have "the stoichiometry Si_xGe_{1-x}, where $0 \leqq x \leqq 1$."[300] According to *Ranade*, "source/drain regions 220 have a composition different from the composition of the semiconductor material of active region 204

[298] *Ranade* ¶ [0025].

[299] *Id.* ¶ [0032]; *see also id.* ¶¶ [0016], [0017], [0026], [0045].

[300] *Id.* ¶ [0040]; *see also id.* ¶ [0023] (describing source/drain regions 120 the same way).

and impart a uniaxial strain to channel region 214," such as compressive strain that would enhance hole mobility in pFET devices.[301] For example, *Ranade* explains that "the lattice constant of the strain-inducing source/drain regions is larger than the lattice constant of the crystalline semiconductor material" in channel region 214 (which is part of active region 204) so as to "impart a compressive uniaxial strain."[302] A person of ordinary skill in the art would have understood this means the Ge concentration *y* in Si_yGe_{1-y} source/drain regions 220 is larger than the Ge concentration *x* in the Si_xGe_{1-x} active region 204 to compressively stress the channel region. *Ranade* further explains that "tip extensions 212 may be formed by implanting charge-carrier dopant impurity atoms into active region 204."[303] A person of ordinary skill in the art would have understood, therefore, that tip extensions 212 are made from the same Si_xGe_{1-x} material as active region 204 and has essentially the same Ge concentration.

249. Thus, *Ranade* teaches that substrate 202, active region 204, source/drain regions 220, and tip extensions 212 all are made of Si_xGe_{1-x}, although

[301] *Id.* ¶ [0040]; *see also id.* ¶ [0023] (explaining that the active region "is comprised of Si_xGe_{1-x}" and the source/drain regions are "comprised of Si_yGe_{1-y} where $x \leqq 1$, $y \leqq 1$ and $x \neq y$"), ¶ [0039] (describing a "strain-inducing source/drain region" that "may impart a uniaxial strain to the channel region"); *Kim* ¶ [0064] (describing "a channel compressive stress effect").

[302] *Ranade* ¶ [0039].

[303] *Id.* ¶ [0040].

the value of *x* differs between substrate 202, source/drain regions 220, and active region 204/tip extensions 212.[304] A person of ordinary skill in the art would have understood that the fin in *Ranade*'s FinFET embodiment includes these regions.

250. A person of ordinary skill in the art would have understood that *Ranade*'s Figure 3C below, for example, shows *Ranade*'s FinFET device at a stage of processing analogous to the one shown in *Ranade*'s Figure 2E—that is, before the tip extensions have been implanted into the active region (Figures 2F and 2G), before the source/drain regions have been regrown (Figures 2H-2K), before the interlayer dielectric has been deposited (Figures 2L and 2M), and before the replacement metal gate process has been performed (Figure 2N).[305] A person of ordinary skill in the art would have understood that the fin includes part of the substrate, the active region, the epitaxial source/drain regions, and the tip extensions once those steps have been completed. Thus, *Ranade* teaches "a fin comprising silicon" as claimed.

[304] *Id.* ¶ [0023]; *see also id.* ¶¶ [0008], [0015] [0018], [0020], [0025], [0031], [0033]-[0039], [0041]-[0046], Figs. 1A, 1B, 2C 2N, 3A-3C.

[305] *Id.* ¶¶ [0025], [0046]; *see also id.* ¶¶ [0032], [0044], [0045], Figs. 2E, 3A-3C.

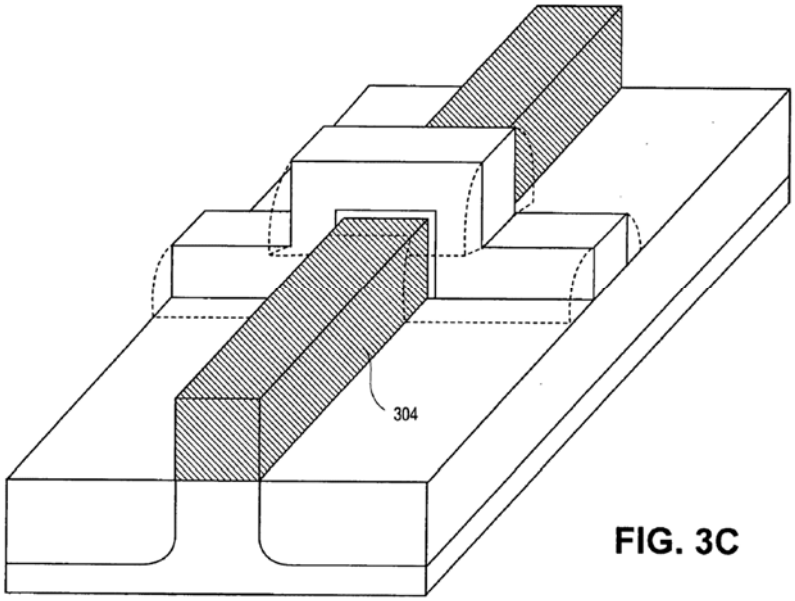
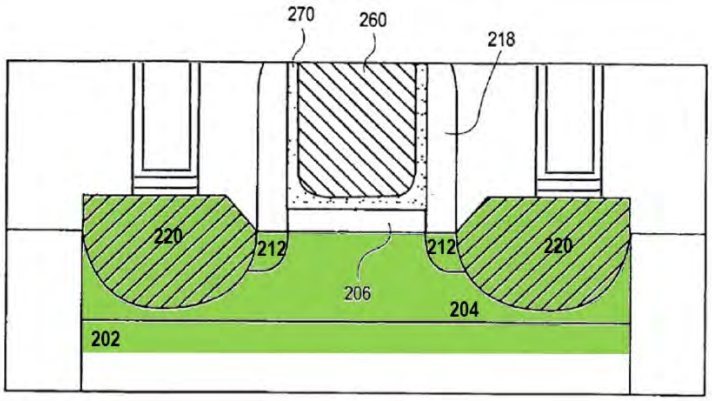
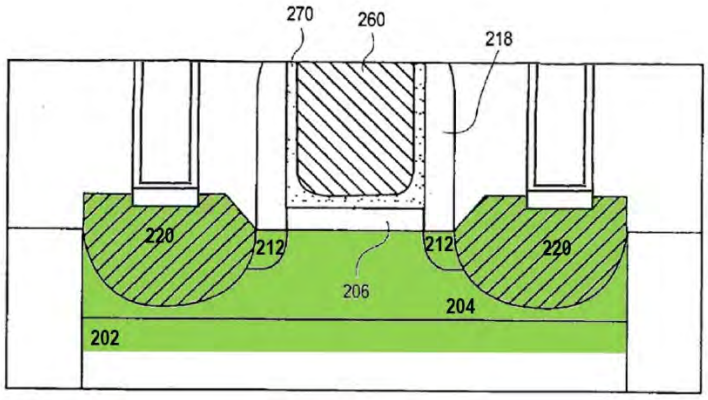


FIG. 3C

251. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFET device according to the First Obvious Modification and the Second Obvious Modification based on *Kim*, as the figures below illustrate. I created these figures for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings, and I have highlighted the components of the fin in green.

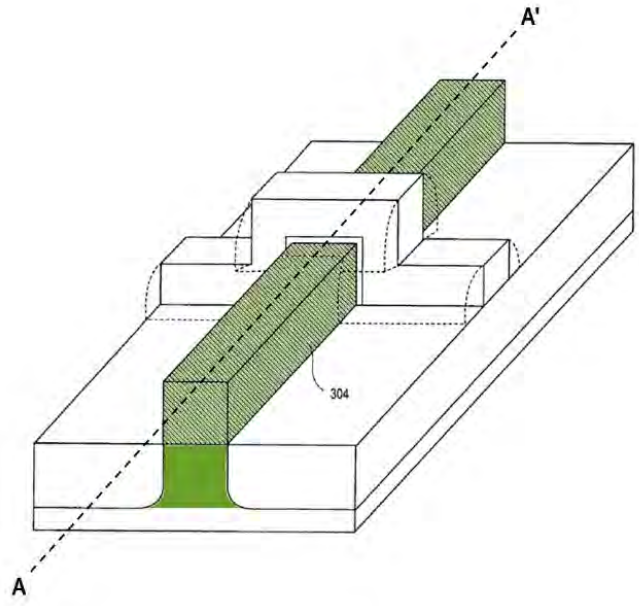


***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

252. To provide an approximate orthographic illustration, I have also annotated *Ranade*'s Figure 3C below in green and added a line A–A' to indicate the location of the cross-section that would correspond to the figures above once the *Ranade-Kim* FinFET device has been completed. A person of ordinary skill in the art would have recognized that *Ranade*'s FinFET, as implemented according to *Kim* (as shown above), includes "a fin comprising silicon."



253. A person of ordinary skill in the art would have known how to apply *Kim*'s teachings to *Ranade*'s FinFET embodiment because *Kim* itself notes that its teachings can be implemented in planar FETs and FinFETs alike:

> Although a field-effect transistor having a flat channel is described by example herein, it will be understood by one of ordinary skill in the art that many configurations are possible, for example, a metal oxide semiconductor (MOS) transistor having a ***[f]in-type*** or recessed channel.[306]

254. Because *Ranade* teaches a FinFET with a Si-containing fin, and because *Ranade*'s FinFET implemented using *Kim*'s teachings as I describe in Section IX.A.1 also includes the same Si-containing fin, a person of ordinary skill in the art would have understood the *Ranade-Kim* combination has "a fin comprising silicon" as claimed.

c. Claim Element [1.2]: Gate Electrode

255. Claim 1 recites "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side." The asserted combinations of *Ranade* and *Kim* both include "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side."

[306] *See Kim* ¶ [0033]; Korean *Kim* ¶ [0023]; *supra* note 247.

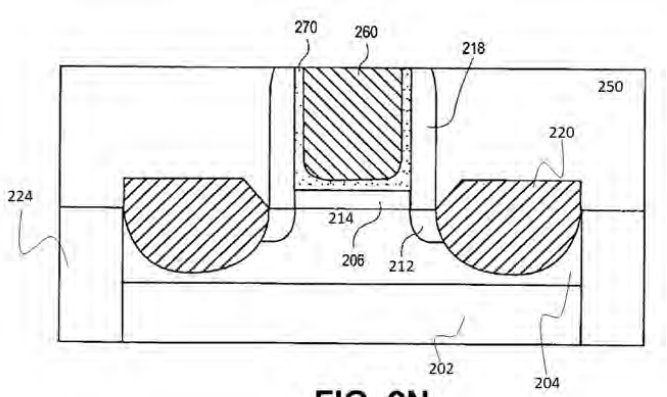


FIG. 2N

256. *Ranade* teaches a FinFET device similar to what Figure 2N above shows (onto which I have copied additional reference numerals from Figures 2A-2M for clarity).[307] As shown, *Ranade*'s FinFET device includes a gate electrode 260 over active region 204, which makes up part of the fin.[308] As shown above, the gate electrode 260 has "a first side" (left side) and "a second side" (right side) that is located "opposite the first side" (or vice versa).

257. *Ranade*'s Figure 3C also illustrates the gate electrode 308, shown in an orthographic view of *Ranade*'s FinFET at an intermediate stage of processing analogous to Figure 3E. A person of ordinary skill in the art would have understood that Figure 3C shows *Ranade*'s FinFET before the tip extensions have been implanted into the active region (Figures 2F and 2G), before the source/drain regions have been regrown (Figures 2H-2K), before the interlayer dielectric has

[307] *Ranade* ¶ [0025].

[308] *Id.* ¶ [0042]; *see also id.* ¶¶ [0015], [0018]-[0020], [0028]-[0031], [0033]-[0037], [0041], [0042], [0044]-[0046], Figs. 1A, 1B, 2B-3C.

been deposited (Figures 2L and 2M), and before the replacement metal gate process has been performed (Figure 2N).[309] As shown below, *Ranade*'s FinFET includes a gate electrode 308 (or a replacement gate) formed over the fin with a first/second sides opposite one another.[310] Thus, *Ranade* teaches "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side" as claimed.

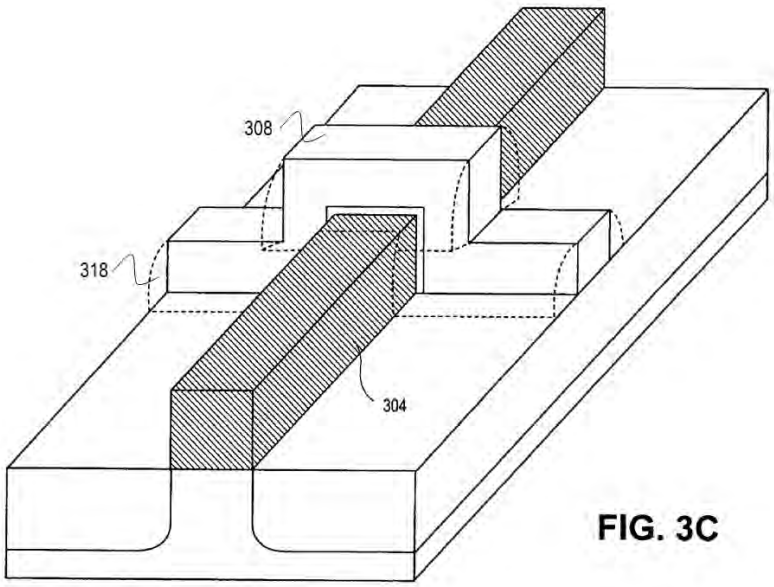


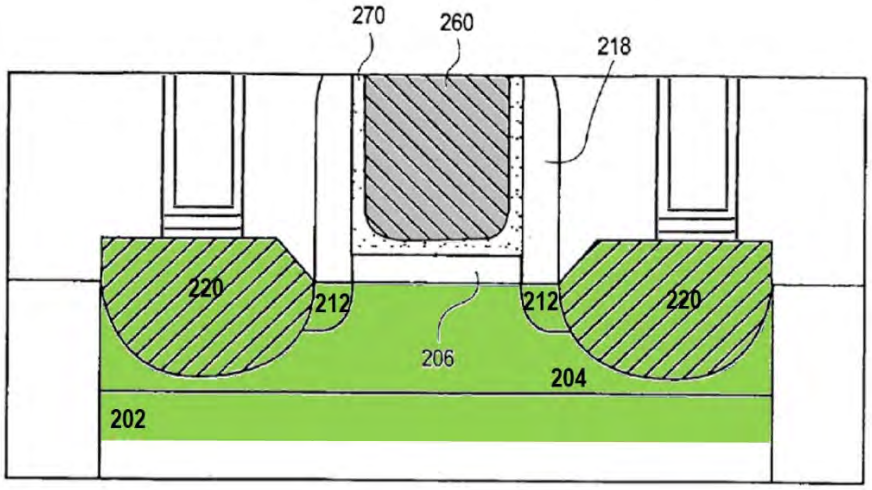
FIG. 3C

258. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFET device according to the First Obvious Modification and the Second Obvious Modification based on *Kim*, as the figures below illustrate. I created these figures for illustrative purposes

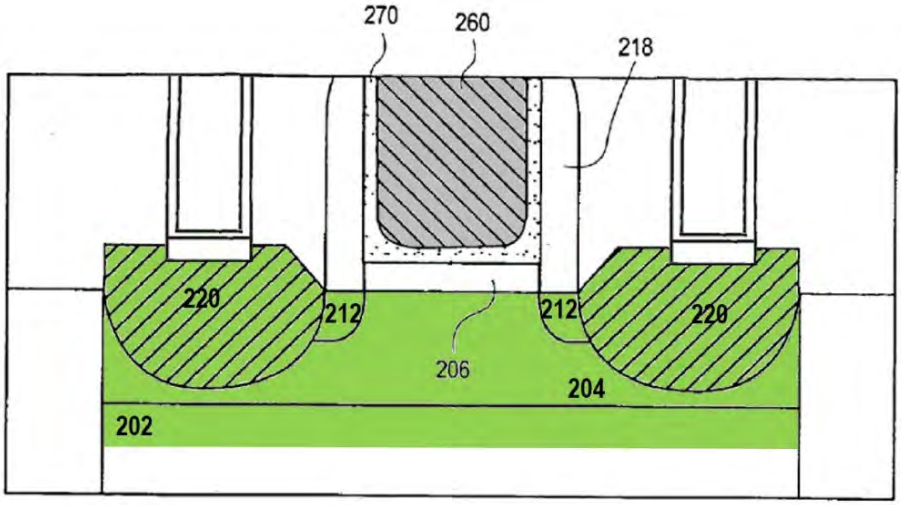
[309] *Id.* ¶¶ [0025], [0046]; *see also id.* ¶¶ [0032], [0044], [0045], Figs. 2E, 3A-3C.

[310] *Id.* ¶¶ [0041], [0044], [0045]; *see also id.* ¶¶ [0035]-[0037], Fig. 3F.

by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings, and I have highlighted the gate electrode in gray and the components of the fin in green.



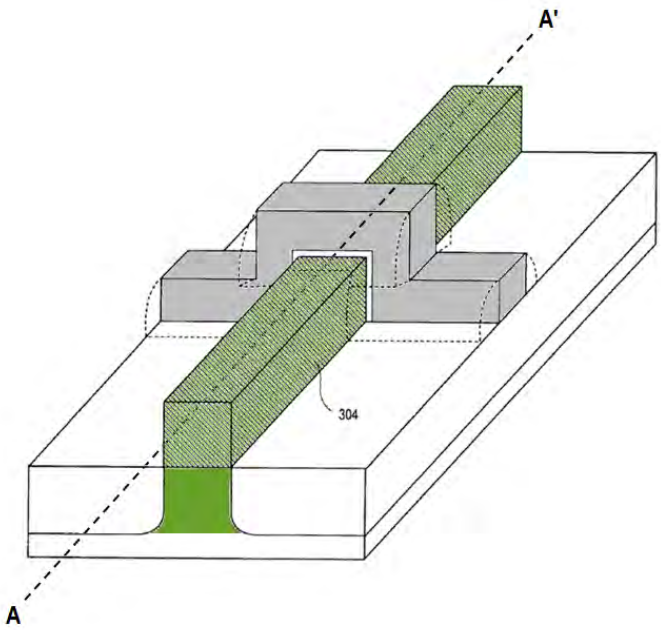
***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

259. To provide an approximate orthographic illustration, I have also annotated *Ranade*'s Figure 3C below to show the gate electrode in gray and the fin

in green.[311] I also added a line A–A' to indicate the approximate cross-section that would correspond to the figures above once the combined *Ranade-Kim* FinFET device has been completed. A person of ordinary skill in the art would have recognized that *Ranade*'s FinFET, as implemented according to *Kim* (shown above), includes "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side."



260. Because *Ranade* teaches a FinFET with a gate electrode over the fin (as would be true in any FinFET), and because *Ranade*'s FinFET implemented using *Kim*'s teachings, as I describe in Section IX.A.1, also includes a gate electrode over the fin, a person of ordinary skill in the art would have understood

[311] The fin shown in Figure 3C will change somewhat once the epitaxial source/drain regions are formed. *See supra* note 305 and related text.

the *Ranade-Kim* combination has "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side" as claimed.

d. Claim Element [1.3]: First Dielectric Spacer

261. Claim 1 recites "a first dielectric spacer along the first side of the gate electrode." The asserted combinations of *Ranade* and *Kim* both include "a first dielectric spacer along the first side of the gate electrode."

262. *Ranade* teaches a FinFET device similar to what Figure 2N below shows (onto which I have copied additional reference numerals from Figures 2A-2M for clarity). As shown, *Ranade*'s FinFET includes "a pair of gate isolation spacers 218 . . . formed from dielectric material layer 230" along the first and second sides of the gate electrode 260.[312]

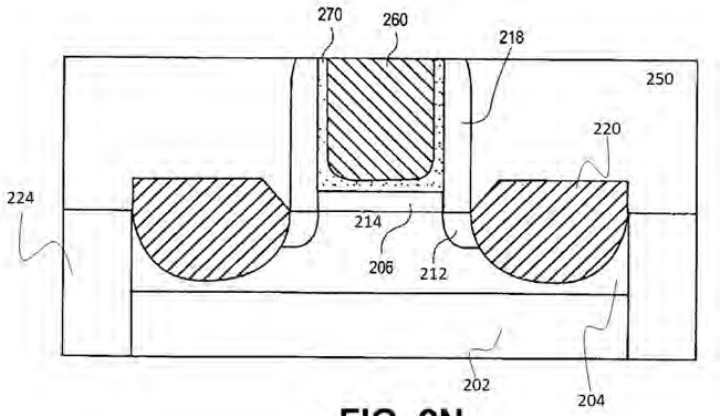


FIG. 2N

[312] *Ranade* ¶ [0037]; *see also id.* ¶ [0020] (describing "gate isolation spacers 118"); ¶ [0045] (describing "a pair of gate isolation spacers 318"), ¶ [0044] (explaining "devices with a three-dimensional architecture, such as tri-gate devices, may benefit from the above process").

263. *Ranade*'s Figure 3C (below) also illustrates gate isolation spacers 318, presented below in an orthographic view an intermediate stage of processing analogous to the cross-section in *Ranade*'s Figure 2E. A person of ordinary skill in the art would have understood that Figure 3C shows *Ranade*'s FinFET before the tip extensions have been implanted into the active region (Figures 2F and 2G), before the source/drain regions have been regrown (Figures 2H-2K), before the interlayer dielectric has been deposited (Figures 2L and 2M), and before the replacement metal gate process has been performed (Figure 2N).[313] As shown below, dotted lines indicate where gate isolation spacers 318 will be formed along the sides of the gate electrode.[314] Thus, *Ranade* teaches "a first dielectric spacer along the first side of the gate electrode," as claimed.

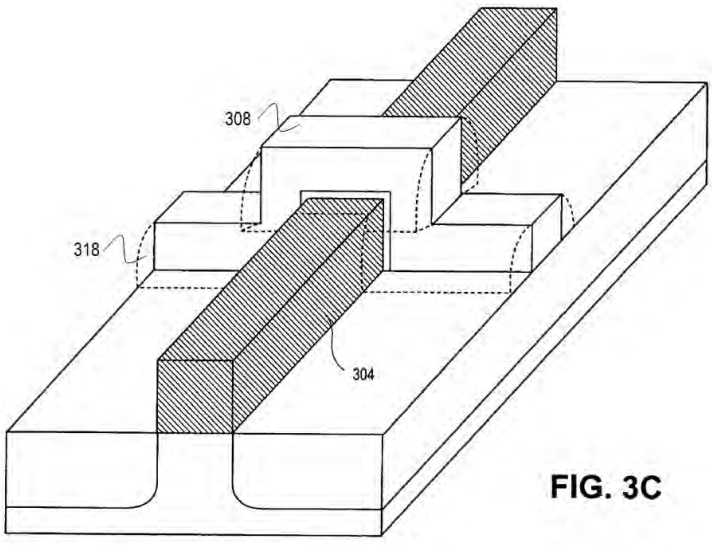
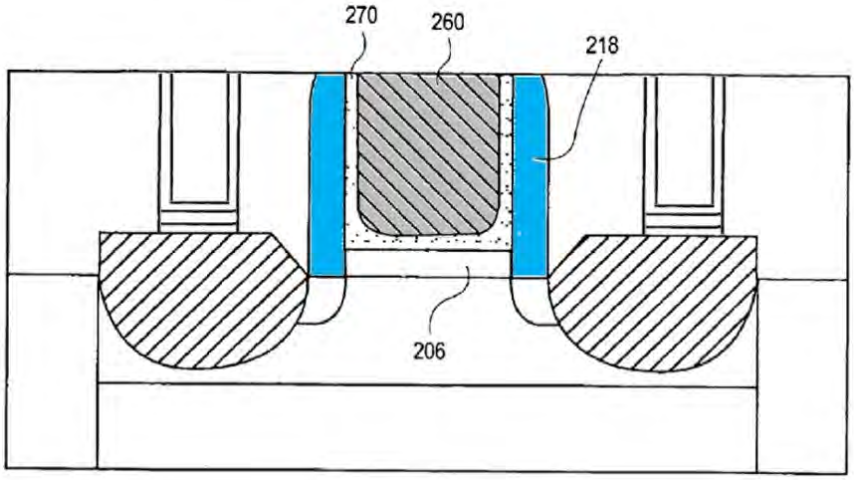


FIG. 3C

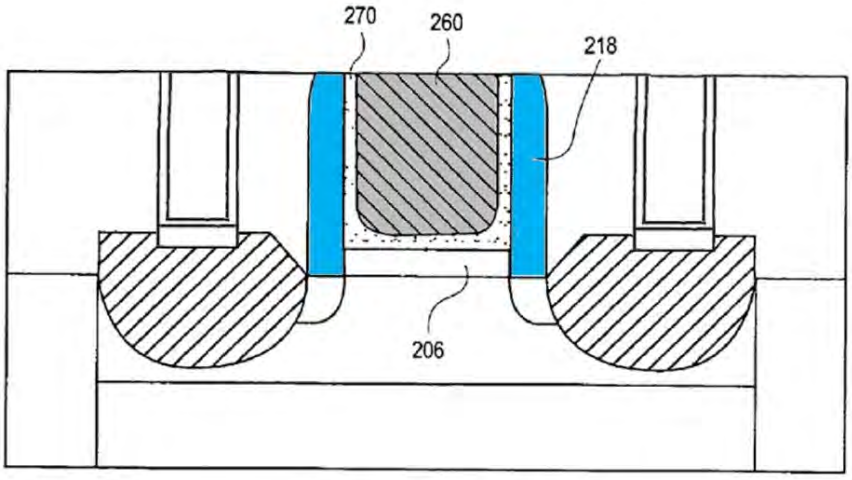
[313] *Id.* ¶¶ [0025], [0046]; *see also id.* ¶¶ [0032], [0044], [0045], Figs. 2E, 3A-3C.

[314] *Id.* ¶¶ [0044], [0045]; *see also id.* ¶¶ [0035]-[0037], Fig. 3F.

264. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFET device according to the First Obvious Modification and the Second Obvious Modification based on *Kim*, as the figures below illustrate. I created these figures for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings, and I have highlighted the gate electrode in gray and the dielectric spacers in blue.

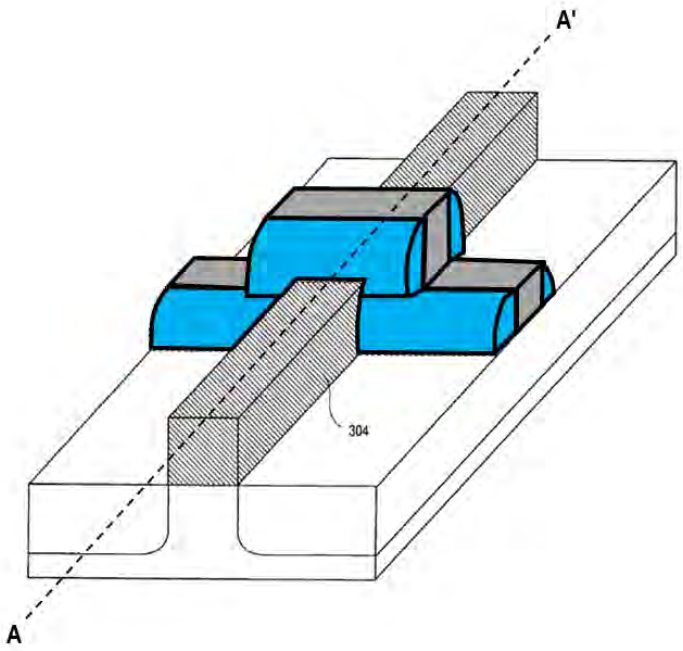


***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

265. To provide an approximate orthographic illustration, I have also annotated *Ranade*'s Figure 3C below to show the gate electrode in gray and the dielectric spacers in blue. I also added a line A–A' to indicate the approximate cross-section that would correspond to the figures above once the combined *Ranade-Kim* FinFET device has been completed.[315] A person of ordinary skill in the art would have recognized that *Ranade*'s FinFET, as implemented according to *Kim* (shown above), includes "a first dielectric spacer along the first side of the gate electrode."



266. Because *Ranade* teaches a FinFET with dielectric spacers formed along the sides of the gate electrode, and because *Ranade*'s FinFET implemented

[315] The fin shown in Figure 3C will change somewhat once the epitaxial source/drain regions are formed. *See supra* note 305 and related text.

using *Kim*'s teachings, as I describe in Section IX.A.1, also includes dielectric spacers formed along the sides of the gate electrode, a person of ordinary skill in the art would have understood the *Ranade-Kim* combination has "a first dielectric spacer along the first side of the gate electrode" as claimed.

e. Claim Element [1.4]: First Source/Drain Region

267. Claim 1 recites "a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer." The asserted combinations of *Ranade* and *Kim* both include "a first source or drain region in the fin proximate a first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer."

268. *Ranade* teaches a FinFET device similar to what Figure 2N below shows (onto which I copied additional reference numerals from Figures 2A-2M for clarity).[316] As shown here, *Ranade*'s FinFET device includes epitaxial source/drain regions 220 and source/drain tip extensions 212, both of which are located proximate to either side of gate electrode 260.[317] And as I discuss in Section IX.A.3.b, epitaxial source/drain regions 220 and source/drain tip extensions 212

[316] *Ranade* ¶ [0025].

[317] *Id.* ¶ [0040]; *see also id.* ¶¶ [0020], [0021], [0023], [0031], [0034], [0035], [0037]-[0041], [0044]-[0046], Figs. 1B, 2G-3C.

constitute parts of the fin, meaning they are in the fin. Together, epitaxial source/drain regions 220 and source/drain tip extensions 212 constitute a "source or drain region" as claimed. Thus, *Ranade* teaches source/drain regions (including source/drain tip extensions 212) that are "in the fin proximate the [first/second] side[s] of the gate electrode."

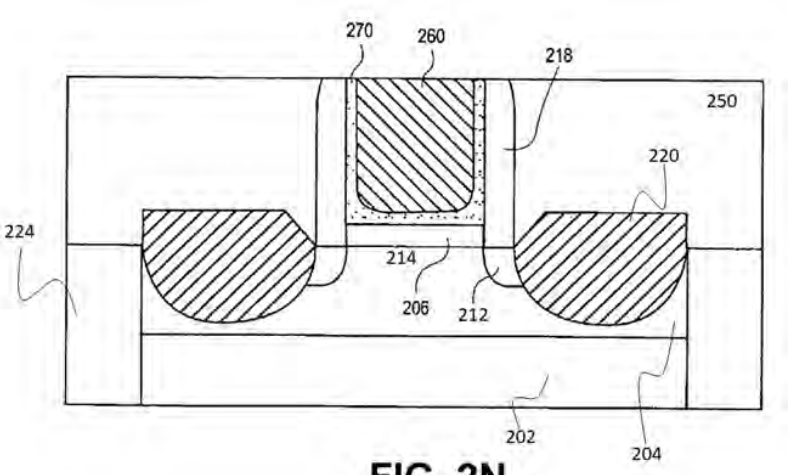


FIG. 2N

269. A person of ordinary skill in the art would have understood that *Ranade*'s Figure 3C below, for example, shows *Ranade*'s FinFET device at a stage of processing analogous to the one shown in *Ranade*'s Figure 2E—that is, before the tip extensions have been implanted into the active region (Figures 2F and 2G), before the source/drain regions have been regrown (Figures 2H-2K), before the interlayer dielectric has been deposited (Figures 2L and 2M), and before the replacement metal gate process has been performed (Figure 2N).[318] A person of

[318] *Id.* ¶¶ [0025], [0046]; *see also id.* ¶¶ [0032], [0044], [0045], Figs. 2E, 3A-3C.

ordinary skill in the art would have understood that the epitaxial source/drain regions 220 are grown to replace the exposed parts of active region 304 shown below that are not covered by the gate electrode or gate isolation spacers.[319]

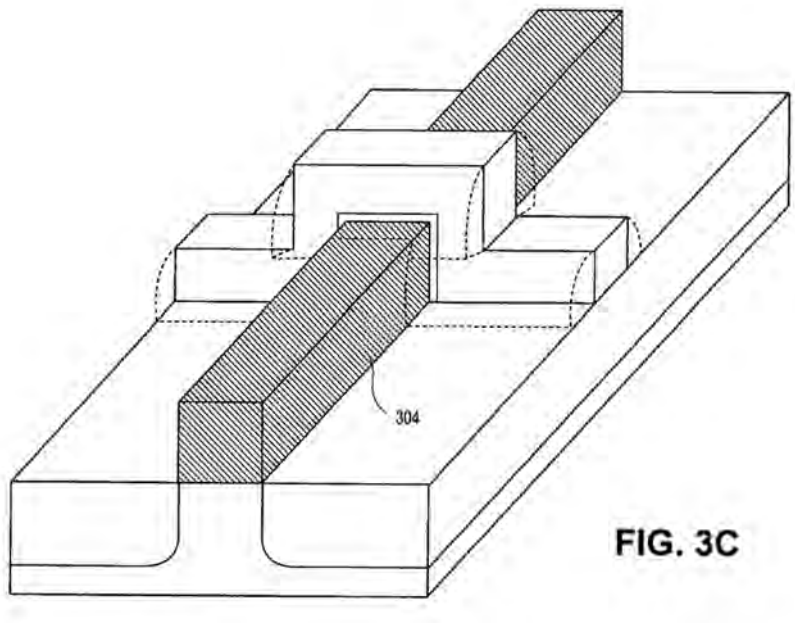
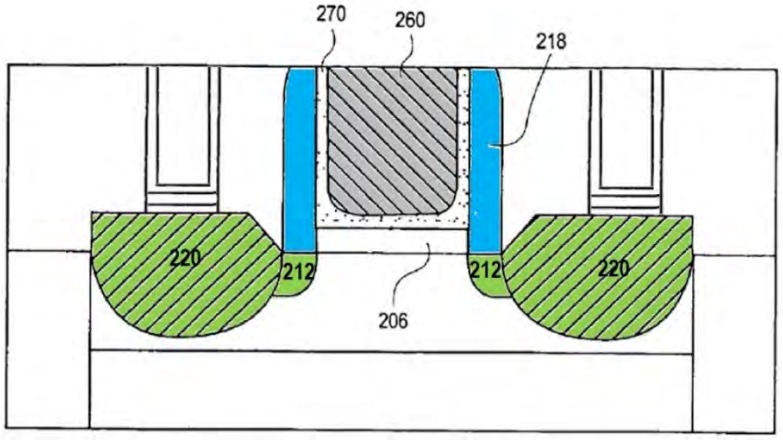


FIG. 3C

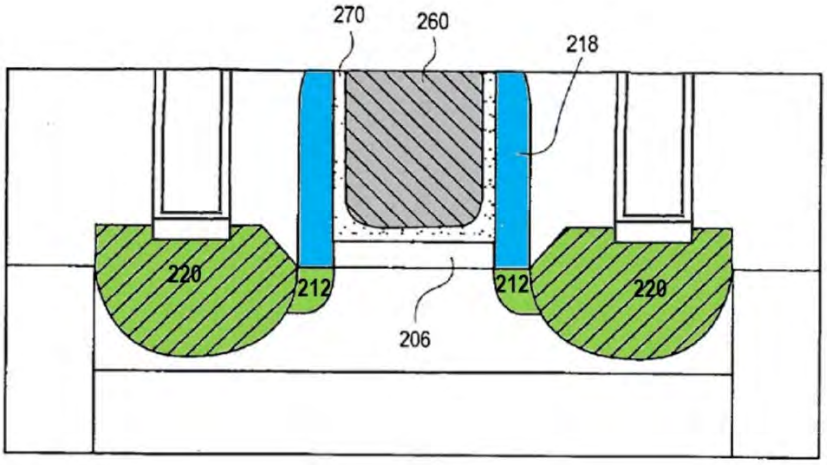
270. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFET device according to the First Obvious Modification and the Second Obvious Modification based on *Kim*, as the figures below illustrate. I created these figures for illustrative purposes by modifying *Ranade*'s Figure 2N to reflect *Kim*'s teachings. I have highlighted the constituent parts of two different source/drain regions in green, the gate electrode in gray, and the dielectric spacers in blue. As shown here, a portion of source/drain regions (e.g., tip extensions 212) lie beneath dielectric spacers 218

[319] *See id.* ¶ [0045], Figs. 3A-3C; *see also id.* ¶¶ [0037]-[0040], Figs. 2I-2K.

such that the First and Second Obvious Modifications each include "a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer."



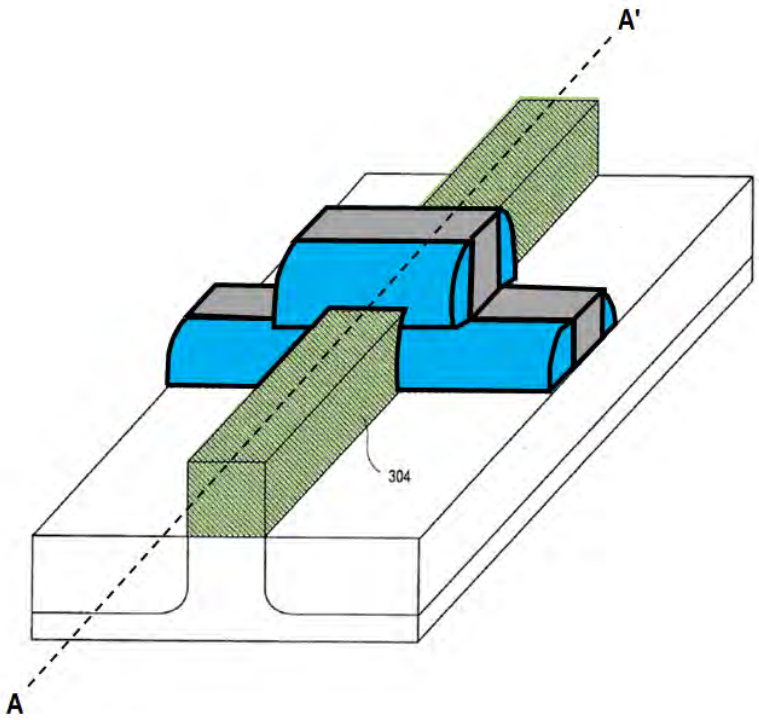
***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

271. To provide an approximate orthographic illustration, I have also annotated *Ranade*'s Figure 3C below to show the gate electrode in gray and the dielectric spacers in blue, and to show the portions of the fin that will be epitaxially

regrown to form the source/drain regions in green.[320] I also added a line A–A' to indicate the approximate cross-section that would correspond to the figures above once the combined *Ranade-Kim* FinFET has been completed.



272. A person of ordinary skill in the art would have recognized that *Ranade*'s FinFET, as implemented according to *Kim* (shown in the figures above), includes "a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region [e.g., tip extensions 212] beneath the first dielectric spacer."

[320] The fin shown in Figure 3C will change somewhat once the epitaxial source/drain regions are formed. *See supra* note 305 and related text.

273. Because *Ranade* teaches a FinFET with source/drain regions in the fin next to the gate electrode (as would be true in any FinFET), because a portion of those source/drain regions (e.g., the tip extensions) are below the dielectric spacers, and because *Ranade*'s FinFET implemented using *Kim*'s teachings as described in Section IX.A.1 has those same features, a person of ordinary skill in the art would have understood the *Ranade-Kim* combination has "a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer," as claimed.

f. Claim Element [1.5]: Graded Germanium Concentration of the First Source or Drain Region

274. Claim 1 recites "wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combinations of *Ranade* and *Kim* both include a structure "wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%."

275. *Ranade* teaches a FinFET device similar to what Figure 2N below shows (onto which I have copied additional reference numerals from

Figures 2A-2M for clarity).[321] As shown here, *Ranade*'s FinFET device includes epitaxial source/drain regions 220 and source/drain tip extensions 212.[322]

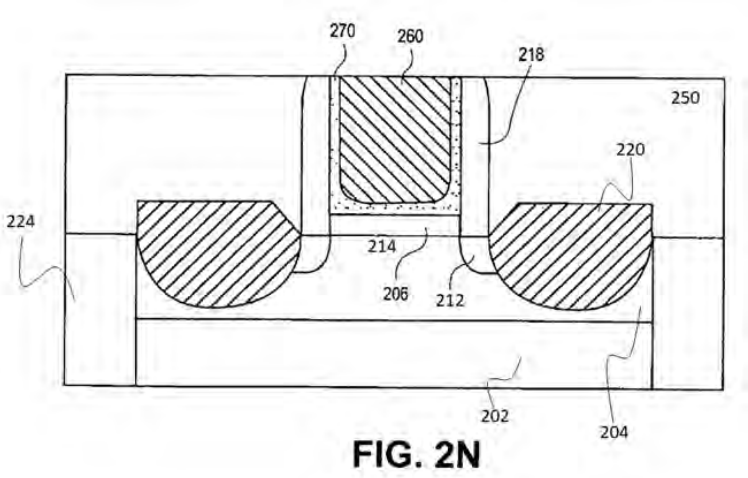


FIG. 2N

276. According to *Ranade*, epitaxial source/drain regions 220 are "crystalline silicon/germanium" and have "the stoichiometry Si_xGe_{1-x}, where $0 \leqq x \leqq 1$."[323] Additionally, "source/drain regions 220 have a composition different from the composition of the semiconductor material of active region 204 and impart a uniaxial strain to channel region 214," such as compressive strain that would enhance hole mobility in pFET devices.[324] For example, *Ranade* explains

[321] *Ranade* ¶ [0025].

[322] *Id.* ¶ [0040]; *see also id.* ¶¶ [0020], [0021], [0023], [0031], [0034], [0035], [0037]-[0041], [0044]-[0046], Figs. 1B, 2G-3C.

[323] *Id.* ¶ [0040]; *see also id.* ¶ [0023].

[324] *Id.* ¶ [0040]; *see also id.* ¶ [0023] (explaining that the active region "is comprised of Si_xGe_{1-x}" and the source/drain regions are "comprised of Si_yGe_{1-y} where $x \leqq 1$, $y \leqq 1$ and $x \neq y$"), ¶ [0039] (describing a "strain-inducing source/drain region" that "may impart a uniaxial strain to the channel region"); *Kim* ¶ [0064] (describing "a channel compressive stress effect").

that "the lattice constant of the strain-inducing source/drain regions is larger than the lattice constant of the crystalline semiconductor material" in channel region 214 (which is part of active region 204) so as to "impart a compressive uniaxial strain."[325] A person of ordinary skill in the art would have understood this means the Ge concentration *y* in Si_yGe_{1-y} epitaxial source/drain regions 220 is larger than the Ge concentration *x* in the Si_xGe_{1-x} active region 204 to compressively stress the channel region. In view of these teachings, *Ranade*'s FinFET is a structure in which "the first source or drain region comprises silicon and germanium."[326]

277. *Ranade* also teaches that the germanium of the source and drain regions "ha[s] a germanium concentration graded to a concentration in excess of 50%" for at least two complementary reasons, both of which I explain below: (1) *Ranade* expressly teaches grading germanium concentration in the source and drain regions over a range exceeding 50 atomic %; and (2) a person of ordinary skill in the art would have found it obvious to grade the germanium concentration of *Ranade*'s SiGe source/drain regions to minimize dislocations and enhance strain to yield better device performance.

[325] *Ranade* ¶ [0039].

[326] *Kim* likewise describes the use of SiGe source/drain regions. *See Kim* ¶ [0063] (describing "SiGe epitaxial layer 43L"), Fig. 3F; *see also id.* ¶ [0074] (explaining "[e]xample embodiments . . . may be implemented independently or in combination with the other embodiments").

278. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s semiconductor devices according to either the First Obvious Modification or the Second Obvious Modification. For the reasons I discuss below, a person of ordinary skill in the art would have recognized that *Ranade*'s FinFET, implemented according to *Kim*, includes a "first source or drain region" that "comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%."

i. *Ranade* expressly teaches grading the germanium concentration in the source/drain regions over a range that exceeds 50 atomic %

279. A person of ordinary skill in the art would have understood *Ranade* teaches that the Ge concentration of source/drain regions 220 includes "a germanium concentration graded to a concentration in excess of 50%" because *Ranade* expressly teaches grading germanium concentration in the source and drain regions over a range that exceeds 50 atomic %.

280. *Ranade* teaches a FinFET with epitaxial Si_xGe_{1-x} source/drain regions 220, whereby the Ge concentration *1-x* is graded over a range anywhere between 0 atomic % to 100 atomic % (namely, "Si_xGe_{1-x}, where $0 \leqq x \leqq 1$"):

> [T]he pair of source/drain regions 220 have a composition different from the composition of the semiconductor material of active region 204 and impart a uniaxial strain to channel region 214. The pair of source/drain regions 220 may be formed by any technique suitable to form a highly uniform (i.e. low surface defect density, e.g. less

> than 10^6 dislocations/cm^2 at the surface of the pair of source/drain regions 220) crystalline layer. In one embodiment, the pair of source/drain regions 220 comprises a uniform epitaxial layer. In another embodiment, **the pair of source/drain regions 220 comprises a graded epitaxial layer, wherein the grading process minimizes surface defects. . . . In one embodiment, the pair of source/drain regions 220 is a crystalline silicon/germanium region of the stoichiometry Si_xGe_{1-x}, where $0 \leqq x \leqq 1$**, and the charge-carrier dopant impurity atoms are selected from the group consisting of boron, arsenic, indium or phosphorus.[327]

Thus, *Ranade* expressly teaches source/drain regions that have a graded Ge concentration that varies over a range that can exceed 50 atomic %.

281. Based on *Ranade*'s express teachings, a person would have understood that *Ranade* teaches source/drain regions with "a germanium concentration graded to a concentration in excess of 50%" as claimed.

ii. A person of ordinary skill in the art would have found it obvious to grade the Ge concentration of *Ranade*'s Si_xGe_{1-x} source/drain regions to exceed 50 atomic %

282. Although *Ranade* expressly teaches Si_xGe_{1-x} source/drain regions that are graded over a range that exceeds 50 atomic % (i.e., over the entire range of 0

[327] *Ranade* ¶ [0040]; *see also* P. Ranade et al., *A Novel Elevated Source/Drain PMOSFET Formed by Ge-B/Si Intermixing*, IEEE Electron Device Letters, vol. 23, no. 4, at 218 (Apr. 2002) (describing a device with source/drain regions that have a "Ge mole fraction varying from ~80% at the top surface to ~1% at 20 nm inside" and boron doping "confined in the $Si_{1-x}Ge_x$ region, with a high surface concentration of 1×10^{21} cm^{-3}"), Figs. 1, 2.

atomic % to 100 atomic %[328]), a person of ordinary skill in the art also would have found it obvious to grade the Ge concentration in *Ranade*'s Si_xGe_{1-x} source/drain regions in excess of 50 atomic %. In fact, the named inventor of *Ranade* and his colleagues recognized a similar approach in another prior-art document, describing pFET source/drain regions with "a ~50 nm graded $Si_{1-x}Ge_x$ layer at the interface" that had a "Ge mole fraction varying from 80% at the top surface to 1%" below.[329]

283. As I explain below, a person of ordinary skill in the art would have been motivated to use such an approach for three reasons. First, a person of ordinary skill in the art would have understood based on his or her training and experience in the field that it would provide Si_xGe_{1-x} source/drain regions with enhanced strain and minimal dislocations, which yields FinFET devices with better performance. Second, a person ordinary skill in the art would have found the claimed compositional range obvious because, by December 2010, the use of SiGe/Strained Silicon technology—including with a graded Ge composition—was ubiquitous. Third, a person ordinary skill in the art would have found it obvious to

[328] The teachings of *Yasutake* and *Thomas*, for example (both discussed below), confirm this is how a person of ordinary skill in the art would have understood *Ranade*'s teachings. *See, e.g.*, *Yasutake* (US2007/0187767) ¶¶ [0085], Fig. 16; *Thomas* (US2009/0075029) ¶ [0042], Fig. 5D.

[329] P. Ranade et al., *A Novel Elevated Source/Drain PMOSFET Formed by Ge-B/Si Intermixing*, IEEE Electron Device Letters, vol. 23, no. 4, at 218 (Apr. 2002); *see also id.* at Fig. 1.

grade *Ranade*'s Ge concentration to an excess of 50 atomic % because he or she would have appreciated that such concentrations differ only in degree, not in kind, from concentrations below 50 atomic %, and that Ge concentrations exceeding 50 atomic % do not produce a new or unexpected result compared to less than 50 atomic %.

284. A person of ordinary skill in the art would have been motivated to grade the Ge concentration in *Ranade*'s Si_xGe_{1-x} source/drain regions to a concentration exceeding 50 atomic % based on his or her knowledge that doing so would provide Si_xGe_{1-x} source/drain regions with enhanced strain, thereby yielding a FinFET with better device performance. As I explain in Section VI.B, by December 2010 a person of ordinary skill in the art would have known two relevant facts: first, that adding more germanium to the source/drain regions creates more strain to enhance pFET performance, and second, that maintaining large amounts of strain requires minimization of dislocations. By December 2010, the best technique for increasing the Ge concentration while minimizing dislocations was well-established: to gradually increase, or "grade," the Ge concentration (and thereby increase the lattice constant) from a base level compatible with the underlying material to a level that provides a high degree of

compressive strain in the channel.[330] As one prior-art reference, titled "Graded High Germanium Compound Films for Strained Semiconductor Devices" explains, it was known that FET device performance "can be improved through implementation of a graded high-germanium content compound, such as a silicon-germanium alloy in the source and drain regions of the transistor."[331]

285. A person ordinary skill in the art also would have found it obvious to grade the Ge concentration in *Ranade*'s Si_xGe_{1-x} source/drain regions in excess of 50 atomic % because, by December 2010, the use of SiGe/Strained Silicon—including with a graded Ge composition—was ubiquitous. As I explain in Section VI.B, by December 2010, SiGe/Strained Silicon technology was nearly universally used in the semiconductor industry to improve the speed of pFETs. As

[330] *See* Section VI.B.

[331] *Simonelli* (US2010/0148217) ¶ [0020]; *see also id.* ¶¶ [0024], [0038], [0042], [0044], [0053], [0058]. Other pre-2010 references also discuss strain engineering with graded SiGe to enhance device performance, including grading to a concentration in excess of 50 atomic % Ge. *See, e.g.*, *Ranade* at Abstract, ¶¶ [0010], [0014], [0023], [0038]-[0040], [0047]; J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2-3, Figs. 1-16 (2006); *Thomas* (US2009/0075029) at Title, Abstract, ¶¶ [0003]-[0005], [0007], [0008], [0029]-[0032], [0044], [0063]; *Yasutake* (US2007/0187767) ¶¶ [0004], [0005], [0023], [0034], [0038], [0041], [0048], [0049], [0056]-[0058], [0068], [0071], [0075], [0082], [0093]; *Kavalieros* (US8211772) at Abstract, 1:55-63, 2:11-22, 2:59-67, 4:56-57; *Jin* (US7767560) at Title, Abstract, 1:9-13, 1:45-57, 2:44-51, 3:10-5:19, 5:48-6:1, 6:61-7:13, 8:62-10:27, 10:50-67, Figs. 4E, 4F.

one example, Intel's 90 nm, 65 nm, 45 nm, and 32 nm processes—released in 2003, 2005, 2007, and 2009, respectively—all used SiGe/Strained Silicon technology.[332] And as I also explain in Section VI.B, Moore's Law was driving the Ge concentrations in SiGe source/drain regions higher and higher over time.

286. Thus, by 2010, a person of ordinary skill in the art would have known that using SiGe/Strained Silicon engineering and grading the Ge concentration in *Ranade*'s Si_xGe_{1-x} source/drain regions to a concentration in excess of 50 atomic % would enhance device performance.

287. Doing so also would have been consistent with *Ranade*'s express teachings, which recognize both the benefits of strain and the desire to minimize dislocations in the source and drain regions. *Ranade* explains, for example, that "the lattice-constant of the semiconductor material of source/drain region is different from the lattice-constant of the [active region] and, thus, the pair of source/drain regions" constitutes "a pair of uniaxial strain-inducing source/drain regions."[333] *Ranade* further explains: "The combination of incorporating an optimal semiconductor material to form an active region and applying uniaxial

[332] *See supra* note 24.

[333] *Ranade* ¶ [0023]; *see also id.* ¶¶ [0014], [0038], [0039].

strain to that active region can lead to increased charge carrier mobility in the channel region."[334] Thus, *Ranade* recognizes the benefits of strain.

288. *Ranade* also recognizes that a graded Ge composition minimizes dislocations in the source/drain regions. According to *Ranade*, "the pair of source/drain regions 220 comprises a graded epitaxial layer" because "the grading process minimizes surface defects."[335] As I explain in Section VI.B, *Ranade* is by no means alone in describing the use of Si_xGe_{1-x} source/drain regions with graded Ge concentration for these reasons. Rather, as various pre-patent publications confirm, it was common in SiGe/Strained Silicon technology to grade the Ge composition in epitaxial Si_xGe_{1-x} source/drain regions across the entire range of available Si_xGe_{1-x} concentrations (i.e., anywhere within the range from 0 atomic % to 100 atomic %).[336]

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[334] *Id.* ¶ [0010]; *see also id.* ¶¶ [0014], [0023], [0038]-[0040], [0047].

[335] *Id.* ¶ [0040].

[336] *See, e.g.*, *Simonelli* (US2010/0148217) at Title, Abstract, ¶¶ [0001], [0018]-[0021], [0024], [0039]-[0040], [0042], [0044], [0051]-[0055], [0057], [0058]; J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2-3, Figs. 1-16 (2006); *Brask* at 5:26-34, 10:20-29; *Thomas* (US2009/0075029) at Title, Abstract, ¶¶ [0003]-[0005], [0007], [0008], [0029]-[0032], [0042], [0044], [0063]; *Yasutake* (US2007/0187767) ¶¶ [0004], [0005], [0023], [0034], [0038], [0041], [0048], [0049], [0056]-[0058], [0068], [0071], [0075], [0082], [0093]; *Kavalieros* (US8211772) at Abstract, 1:55-63, 2:11-22, 2:59-67, 4:56-57; *Jin* (US7767560) at Title, Abstract, 1:9-13, 1:45-57, 2:44-51, 3:10-5:19, 5:48-6:1, 6:61-7:13,

289. *Ranade* does not restrict the amount of Ge used in its graded epitaxial source/drain regions. As Figure 2N below illustrates (onto which I have added additional reference numerals from Figures 2A-2M for clarity), there are three relevant regions in *Ranade*'s device structure. First, the substrate 202 (aqua) may be, for example, a silicon or silicon-on-insulator (SOI) substrate.[337] Second, the active region (peach) may be a graded Si_xGe_{1-x} layer, where $0 \leqq x \leqq 1$.[338] Third, the regrown source/drain regions 220 (green) also may be graded Si_yGe_{1-y} layers, where $0 \leqq y \leqq 1$ and $x \neq y$.[339]

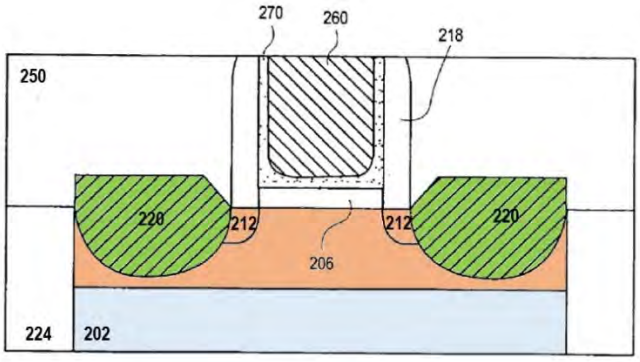


FIG. 2N

8:62-10:27, 10:50-67, Figs. 4E, 4F; *Chong* (US2007/0235802) at Abstract, ¶¶ [0007]-[0008], [0044]-[0052], [0055], [0057], [0084]-[0112], [0123], [0124]; *Wang* (US2008/0054347) ¶¶ [0022]-[0024]; P. Ranade et al., *A Novel Elevated Source/Drain PMOSFET Formed by Ge-B/Si Intermixing*, IEEE Electron Device Letters, vol. 23, no. 4, at 218-19 & Figs. 1, 2 (Apr. 2002).

[337] *Ranade* ¶¶ [0016], [0026].

[338] *Id.* ¶¶ [0032], [0033].

[339] *Id.* ¶¶ [0023], [0040]. For pFETs, a person of ordinary skill would have understood that x<y to provide a larger lattice constant in the source/drain regions and thereby provide compressive stress to the channel region to increase hole mobility. *See id.* ¶ [0039].

290. A person of ordinary skill in the art would have understood from *Ranade*, alone or in view of his or her background knowledge (as described above and in Section VI.B, for example), that it would have been desirable to grade the Ge concentration in the regrown source/drain regions 220 (green) in excess of 50 atomic % and that the amount of Ge in source/drain regions 220 (green) should be larger than the amount of germanium in active region 204 (peach) where the channel is located.[340] Several exemplary disclosures from the prior art confirm this.

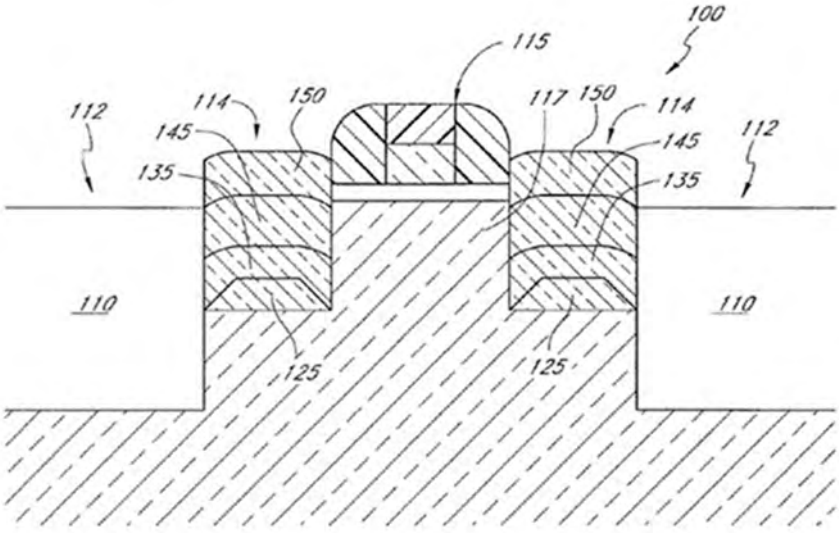
291. As a first example, *Thomas* teaches that "SiGe alloys of uniform composition and thicknesses in the range of about 10-50 nm can be deposited with acceptable dislocation amounts for SiGe with less than about 40 atomic % Ge."[341] Because germanium concentration grading increases the amount of Ge that can be incorporated into the SiGe semiconductor crystal without causing dislocations or other crystal defects, *Thomas* teaches grading above at least 40 atomic %. For example, *Thomas* provides a specific example of grading the Ge concentration up to 60 atomic % or even 100 atomic %.[342] As Figure 5D below illustrates, *Thomas*

[340] *See id.*

[341] *Thomas* (US2009/0075029) ¶ [0031].

[342] *Id.* ¶ [0042].

discloses epitaxial SiGe source/drain regions with a graded germanium concentration that continuously varies over layers 125, 135, 145, etc.[343]



292. As in *Ranade*, the substrate in *Thomas* can be silicon or silicon-on-insulator (SOI).[344] Layer 125 can be a SiGe layer with a germanium concentration "in a range of 10 atomic % to 20 atomic %, and preferably about 15 atomic %."[345] Layer 135 is also a SiGe layer but with a germanium concentration "in a range of 20 atomic % to 100 atomic %, and preferably in a range of about 30 atomic % to 60 atomic %."[346] And so on, where "the layers 125, 135, 145, etc. may form a continuously graded layer" of SiGe.[347] In other words, *Thomas* confirms that

[343] *Id.* ¶¶ [0042]-[0045].

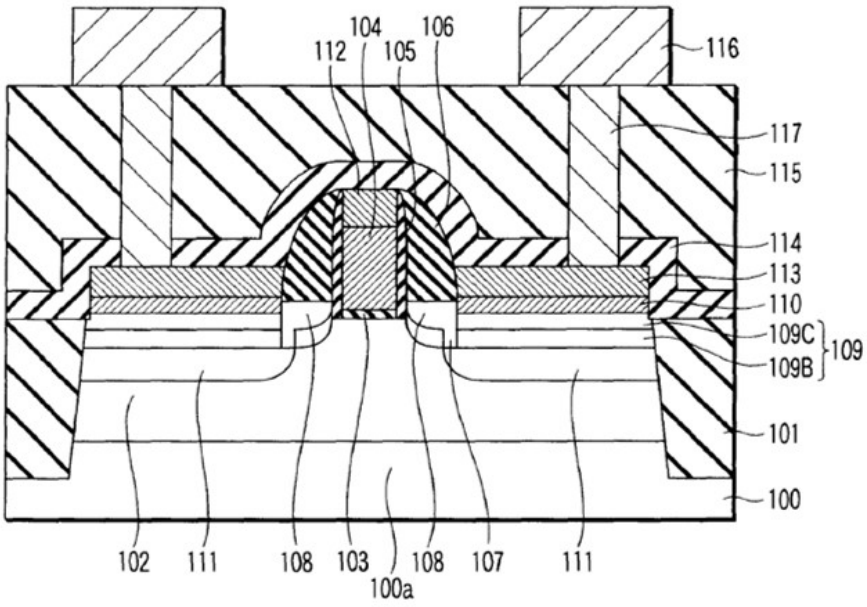
[344] *Id.* ¶ [0026].

[345] *Id.* ¶ [0042].

[346] *Id.*

[347] *Id.* ¶ [0044]; *see also id.* ¶ [0043].

epitaxial SiGe source/drain regions with a Ge concentration graded in excess of 50 atomic % was known in the art.



293. A second example is *Yasutake*, illustrated above, which provides similar disclosures. Like *Ranade*, *Yasutake* discloses a silicon substrate 100 (which can include an n-type well region 102).[348] Source/drain regions 111 span SiGe layer 109 and germanium layer 110.[349] As illustrated in the figure above, SiGe layer 109 may be graded.[350] In particular, the "germanium concentrations in the silicon germanium layer 109B and the germanium layer 110 are 10 to 30 at % and approximately 100 at %, respectively."[351] In between, SiGe layer 109C is graded,

[348] *Yasutake* (US2007/0187767) ¶ [0047].

[349] *Id.* ¶ [0086].

[350] *Id.* ¶¶ [0090], [0094], [0095], Fig. 16.

[351] *Id.* ¶ [0085].

whereby "the germanium concentration of the silicon germanium layer 109C is approximately 10 to 30 at % on an interface between the silicon germanium layer 109C and the silicon-germanium layer 109B, and increased toward the upper portion" of layer 109C.[352] "The germanium concentration of the silicon germanium layer 109C is approximately 100 at % on an interface between the silicon germanium layer 109C and the germanium layer 110."[353] In other words, *Yasutake* also confirms that epitaxial SiGe source/drain regions with a Ge concentration graded in excess of 50 atomic % was known in the art.

294. As these and other exemplary disclosures above demonstrate,[354] a person of ordinary skill in the art would have understood from *Ranade*, alone or in combination with his or her own experience and training, that applying *Ranade*'s teachings to pFET devices would have included the notion of grading the Ge composition of *Ranade*'s Si_xGe_{1-x} source/drain regions from a level compatible with the underlying substrate to a concentration in excess of 50 atomic % Ge

[352] *Id.*

[353] *Id.*

[354] *See, e.g.*, P. Ranade et al., *A Novel Elevated Source/Drain PMOSFET Formed by Ge-B/Si Intermixing*, IEEE Electron Device Letters, vol. 23, no. 4, at 218 (Apr. 2002) (describing a device with source/drain regions that have a "Ge mole fraction varying from ~80% at the top surface to ~1% at 20 nm inside" and boron doping "confined in the $Si_{1-x}Ge_x$ region, with a high surface concentration of 1×10^{21} cm^{-3}"), Figs. 1, 2.

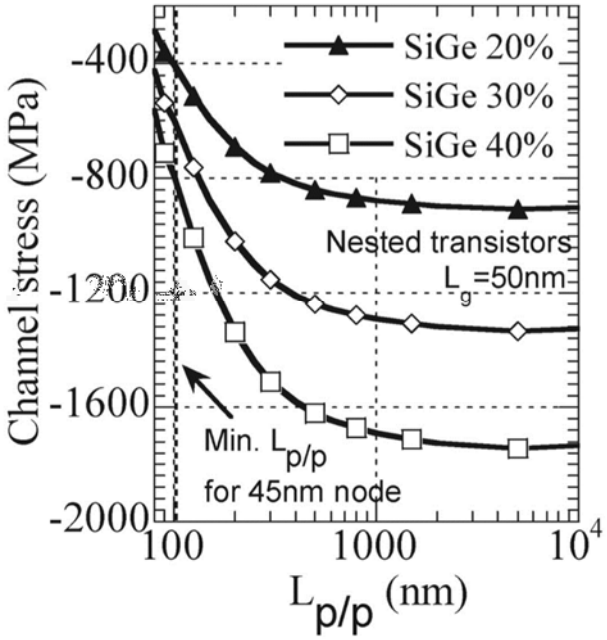
(including up to 100 atomic % Ge).[355] Thus, *Ranade* both expressly teaches and suggests using source/drain regions with "a germanium concentration graded to a concentration in excess of 50%," as claimed.

295. Additionally, a person ordinary skill in the art would have found it obvious to grade the Ge composition in *Ranade*'s source/drain regions in excess of 50 atomic % because he or she would have known that doing so differs only in degree, not in kind, from grading the Ge composition to a concentration less than 50 atomic %, and that doing so does not produce a new or unexpected result.

296. As I explain in Section VI.B, by December 2010 it was already well known that increasing the Ge concentration in Si_xGe_{1-x} source/drain regions improved device performance. In fact, a person of ordinary skill in the art would have known that increased Ge concentration was a natural consequence of FET scaling (i.e., following Moore's law, by which FET feature size is reduced every few years for integrated circuits). This trend was known because smaller transistors have smaller source/drain regions and, therefore, create less compressive stress in the channel region for a given Ge concentration. Increasing the Ge concentration, however, compensates for this reduced stress due to shrinking the transistor. This

[355] *See Ranade* ¶ [0040] (explaining that "the pair of source/drain regions 220 comprises a graded epitaxial layer" and that "the pair of source/drain regions 220 is a crystalline silicon/germanium region of the stoichiometry Si_xGe_{1-x}, where $0 \leqq x \leqq 1$").

trend of increasing Ge concentration from node to node was widely reported long before December 2010, as the example below from 2006 demonstrates.[356]



Additionally, a contemporaneous article confirms that a "disproportionate reduction in device area per generation with respect to gate length, requires increased strain in the e-SiGe to compensate for the lost volume due to non-scaled gate length."[357] It added that "Ge concentration has increased steadily from <20%

[356] *See, e.g.*, G. Eneman et al., *Scalability of the Si_xGe_{1-x} Source/Drain Technology for the 45-nm Technology Node and Beyond*, IEEE Transactions on Electron Devices, vol. 53, no. 7, at 1651, 1653, Fig. 10 (July 2006) (explaining channel stress can be maintained "in the next technology nodes" by "us[ing] higher germanium concentrations in the S/D area" and remarking that "[t]he maximum germanium concentration to be used is limited by the defects generated in the layers, and the maximum leakage that can be allowed").

[357] D.K. Sadana et al., *Applications of Epitaxy for Semiconductor Technology*, ECS Transactions, 218th ECS Meeting, vol. 33, no. 6, at 64 (Oct. 2010).

in 90 nm pFETs to >35% in 32 nm pFETs, **and this trend is expected to continue to future nodes.**"[358] This reflects the contemporaneous knowledge and expectations a person of ordinary skill in the art would have had at the time.

297. A person of ordinary skill in the art, therefore, would have understood that the difference between using less than 50 atomic % Ge in the Si_xGe_{1-x} source/drain regions and more than 50 atomic % Ge in the Si_xGe_{1-x} source/drain regions is not "critical." A person of ordinary skill in the art would have understood that the difference between using less than 50 atomic % Ge and more than 50 atomic % Ge was just a difference of degree, not a difference in kind. Nor does using more than 50 atomic % Ge yield any unexpected results.

298. There is no meaningful difference between less than 50 atomic % Ge and more than 50 atomic % Ge. these ranges. The amount of stress a pair of SiGe source/drain regions applies to the channel region lies along a continuum as Ge concentration changes. For example, the difference in how much of stress a pair of source/drain regions with 50 at. % Ge applies to the channel and how much stress a pair of source/drain regions with 51 at. % Ge applies to the channel is negligible (and well within the range of normal process variation).

[358] *Id.*

299. The ’281 Patent confirms this by disclosing not just source/drain regions with more than 50 atomic % Ge, but also source/drain regions with ***less*** than 50 at. % Ge.[359] The specification also confirms that SiGe source/drain regions with more than 50 at. % Ge can be formed “using any number of conventional techniques.”[360] As this statement from the ’281 Patent confirms, grading the source/drain Ge concentration to an excess of 50 atomic % was known.[361] And as far as I can tell, every example in the ’281 Patent that mentions source/drain regions with 50 atomic % Ge appears to be an afterthought, appearing in a long list of permutations at the end of the specification with no explication.[362] The ’281

[359] *See* ’281 Patent at 3:57-62 (“[I]n some example embodiments, the germanium concentration is in the range of 20 atomic% to 100 atomic %[.]”), 4:29-24 (“[T]he source region 110 and the drain region 112 are formed by etching the substrate and then epitaxially depositing a silicon or silicon germanium material (e.g., with a germanium concentration in the range of, for instance, 10 to 70 atomic %).”), 6:65-7:6 (“[T]he source/drain material is a boron doped SiGe layer having a fixed concentration of germanium (e.g., in the range of 30 to 70 atomic %)[.]”).

[360] ’281 Patent at 4:27-34.

[361] *See supra* Section VI.B (discussing examples); *see also, e.g.*, *Ranade* ¶ [0040]; *Brask* at 10:20-29; *Thomas* (US2009/0075029) ¶¶ [0008], [0042]; *Yasutake* (US2007/0187767) ¶¶ [0034], [0042], [0056], [0062], [0085], [0090]; *Kavalieros* (US8211772) at 6:60-7:11, Fig. 5B; *Jin* (US7767560) at 7:4-13, 7:61-8:18, Fig. 2; P. Ranade et al., *A Novel Elevated Source/Drain PMOSFET Formed by Ge-B/Si Intermixing*, IEEE Electron Device Letters, vol. 23, no. 4, at 218, Fig. 1 (Apr. 2002).

[362] *See* ’281 Patent at 16:16-18:29.

Patent does not suggest any critical distinction for with the 50% value, and I am not aware of one.

300. In sum, a person of ordinary skill in the art would have understood that *Ranade* expressly discloses "the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." Additionally, a person of ordinary skill in the art would have found that *Ranade*, viewed in light of his or her training and experience, suggests "the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%."

g. Claim Element [1.6]: Second Dielectric Spacer

301. Claim 1 recites "a second dielectric spacer along the second side of the gate electrode." The asserted combinations of *Ranade* and *Kim* both include "a second dielectric spacer along the second side of the gate electrode" for the same reasons I discuss in Section IX.A.3.d regarding claim element [1.3].

h. Claim Element [1.7]: Second Source or Drain Region

302. Claim 1 recites "a second source or drain region in the fin proximate a second side of the gate electrode, a portion of the first source or drain region beneath the second dielectric spacer." The asserted combinations of *Ranade* and *Kim* both include "a second source or drain region in the fin proximate a second side of the gate electrode, a portion of the first source or drain region beneath the

second dielectric spacer" for the same reasons I discuss in Section IX.A.3.e regarding claim element [1.4]. The source/drain regions in FET devices like this are identical, which is why they are generally referred to as "source/drain" regions.

i. Claim Element [1.8]: Graded Germanium Concentration of the Second Source or Drain Region

303. Claim 1 recites "wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combinations of *Ranade* and *Kim* both teach "wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%" for the same reasons I discuss in Section IX.A.3.f regarding claim element [1.5]. The source/drain regions in FET devices like this are identical, which is why they are generally referred to as "source/drain" regions.

j. Claim Element [1.9]: Interlayer Dielectric

304. Claim 1 recites "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region." The asserted combinations of *Ranade* and *Kim* both include "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a

portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region."

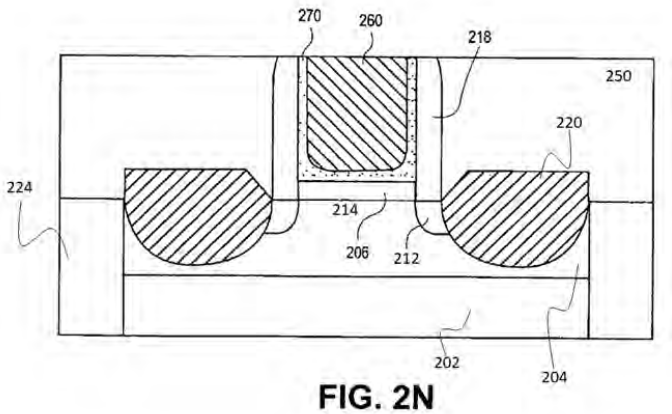


FIG. 2N

305. *Ranade* teaches a FinFET device similar to what Figure 2N above shows (onto which I copied additional reference numerals from Figures 2A-2M for clarity).[363] As shown, *Ranade*'s FinFET includes a dielectric layer 250.[364] But as I explain in Section IX.A.1, *Ranade*'s figures do not illustrate source/drain contacts for its disclosed FinFET device, which provide the necessary electrical connections required to connect the source/drain regions to other devices on the wafer and to the outside world. Rather, *Ranade* simply states that its devices may "undergo typical process steps to complete the formation of a MOS-FET."[365]

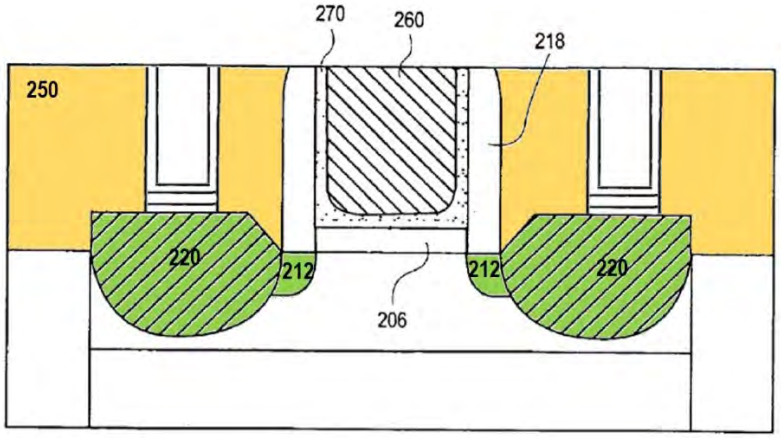
306. As I explain in Section IX.A.1, a person of ordinary skill in the art would have wanted to implement *Ranade*'s FinFETs according to either the First

[363] *Ranade* ¶ [0025].

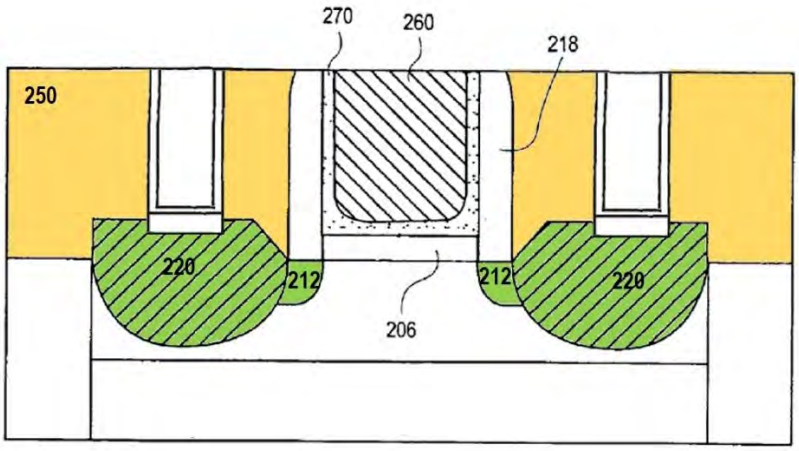
[364] *Id.* ¶ [0041]; *see also id.* at Figs. 2L-2N.

[365] *Id.* ¶ [0041].

Obvious Modification or the Second Obvious Modification by following *Kim*'s teachings. As the illustrations below demonstrate, both the First Obvious Modification and the Second Obvious Modification include an interlayer dielectric, which, for the reasons I explain in Section VI.F, was essentially universal for such devices at the time.



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

As shown here, the First and Second Obvious Modifications both have a dielectric layer 250 (yellow) located over the source/drain regions (green). The dielectric

layer 250 has openings to expose only a portion of each source/drain region. Thus, *Ranade*'s FinFET implemented according to either the First or Second Obvious Modification includes "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region."

307. Thus, *Ranade*'s FinFETs implemented according to either the First Obvious Modification or the Second Obvious Modification includes "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region."

k. Claim Element [1.10]: First Germanide Layer

308. Claim 1 recites "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium." Depending on how "germanide layer" is construed and how the phrase "in the first opening and over the portion" is applied, at least one of the asserted combinations of *Ranade* and *Kim* includes "a first

germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium."

309. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFETs according to either the First Obvious Modification or the Second Obvious Modification. The First Obvious Modification (Ge Overlayer Metalization) satisfies claim element [1.10] under either party's construction of "germanide layer"[366] and any conceivable interpretation of "in the first opening and over the portion." The Second Obvious Modification (Direct Metalization) satisfies claim element [1.10] under the Patent Owner's construction of "germanide layer"[367] and its apparent interpretation of "in the first opening and over the portion" (by which a germanide layer partially outside the ILD opening and partially within the source/drain region is nevertheless "in" the opening and "over" the contact area). The subsections below provide my analysis of each combination.

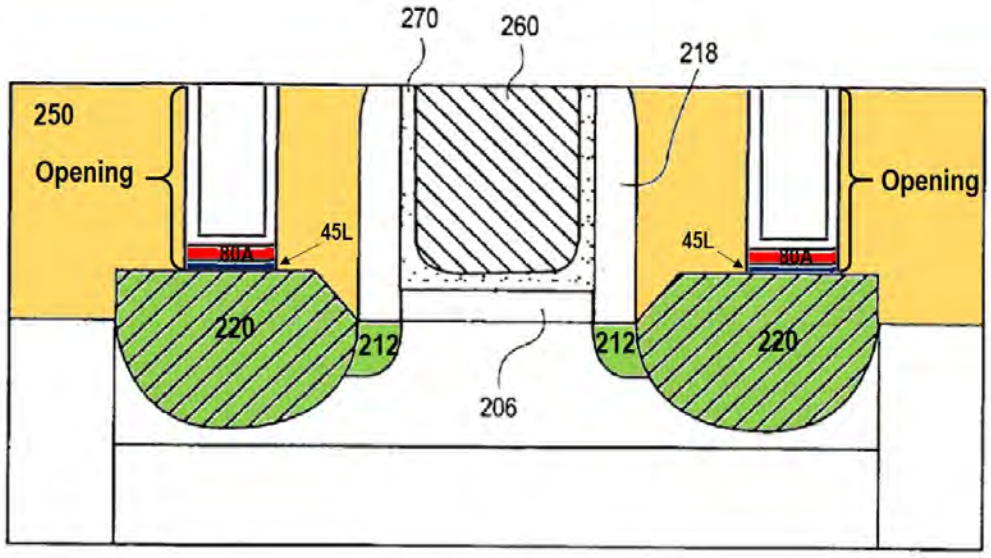
i. First Obvious Modification

310. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFETs according to the First Obvious Modification, as the figure below illustrates (which I created for

[366] *See supra* Section VII.D.

[367] *See id.*

illustrative purposes by modifying *Ranade*'s Figure 2N to reflect *Kim*'s teachings). According to the First Obvious Modification (Ge Overlayer Metalization), a TiSi1-yGey film (red) forms by reacting a thin, intermediate Ge Overlayer (dark blue), plus any Si and Ge atoms that may diffuse from the SiGe source/drain regions (green), with a Ti metal layer.[368]



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**

311. Under Daedalus's broad construction of "germanide layer," the TiSi1-yGey film 80A above (red) constitutes "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium," because it is a "thickness of material, comprising germanium and a metal," because it is located in the opening

[368] *See Kim* ¶¶ [0072]-[0074], Fig. 5; *supra* Section IX.A.1.c.i.

of the ILD layer, and because it further comprises silicon, germanium, and titanium.

312. Under what I believe to be the correct claim construction of "germanide layer," the TiSi1-yGey film above constitutes "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium," because it is a "germanium layer metalized with one or more metals [Ti]," because it is located in the opening of the ILD layer, and because it further comprises silicon, germanium, and titanium.

313. As I explain in Section IX.A.1, a person of ordinary skill in the art would have been motivated to make this combination due to (1) *Ranade*'s reference to—but silence regarding—additional steps for making low-resistance source/drain contacts; and (2) *Kim*'s teaching that forming a TiSi1-yGey film over the source/drain regions reduces source/drain contact resistance. As I also explain in Sections VI.C-E and IX.A.1, a person of ordinary skill in the art would have reasonably expected to succeed at least because (1) the TiSi1-yGey technique *Kim* describes (Ge Overlayer Metalization) was known in the semiconductor industry prior to December 2010; and (2) it would have been implemented with predictable results on *Ranade*'s FinFETs.

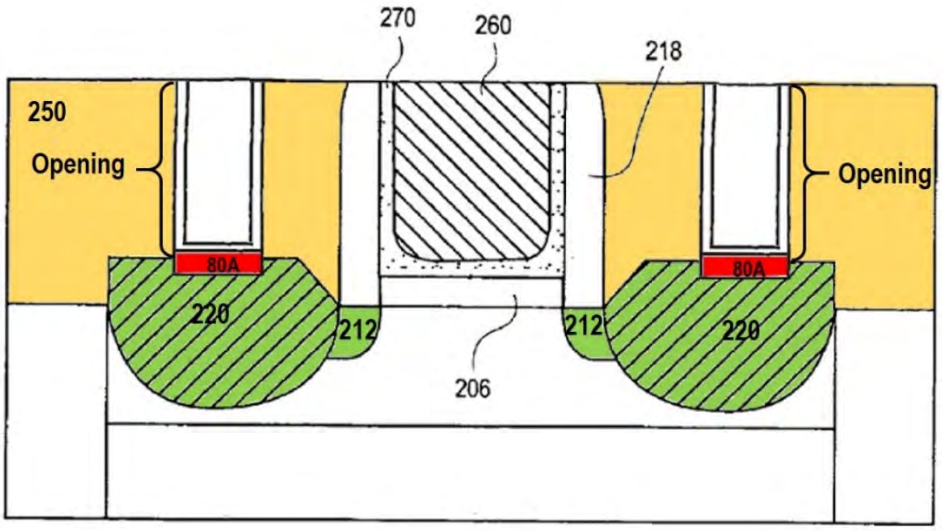
314. Thus, the First Obvious Modification (Ge Overlayer Metalization) satisfies claim element [1.10] because it includes "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium" under either party's construction of "germanide layer"[369] and any conceivable interpretation of the phrase "in the first opening and over the portion."

ii. Second Obvious Modification

315. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFETs according to the Second Obvious Modification, as the figure below illustrates (which I created for illustrative purposes by modifying *Ranade*'s Figure 2N to reflect *Kim*'s teachings). According to the Second Obvious Modification (Direct Metalization), a TiSi1-yGey film (red) forms by reacting the SiGe source/drain regions (green) directly with a Ti layer. In particular, the TiSi1-yGey film (red) is formed because the Ti atoms in the Ti layer chemically react with Si and Ge atoms in the p-type SiGe source/drain regions 220.[370]

[369] *See id.*

[370] *See supra* note 164.



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

316. Under Daedalus's broad construction of "germanide layer," the TiSi1-yGey film 80A above (red) constitutes "a first germanide layer" because it is a "thickness of material, comprising germanium and a metal." It also further "compris[es] silicon, germanium, and titanium" as claimed. And under Daedalus's apparent interpretation of the phrase "in the first opening and over the portion," the TiSi1-yGey film 80A above (red) is "in the first opening and over the portion of the first source or drain region" because it is at least partially located in the opening of the ILD layer and at least partially extends above the source/drain contact areas.

317. As I explain in Section IX.A.1, a person of ordinary skill in the art would have been motivated to make this combination due to (i) *Ranade*'s reference to—but silence regarding—additional steps for making low-resistance source/drain

contacts; and (ii) *Kim*'s teaching that forming a TiSi1-yGey film over the source/drain regions reduces source/drain contact resistance. As I also explain in Sections VI.E, VI.F, and IX.A.1, a person of ordinary skill in the art would have reasonably expected to succeed at least because (1) the TiSi1-yGey technique *Kim* describes (Direct Metalization) was routine in the semiconductor industry prior to December 2010; and (2) it would have been implemented with predictable results on *Ranade*'s FinFETs.

318. Thus, under the Patent Owner's broad construction of "germanide layer"[371] and its apparent interpretation of the phrase "in the first opening and over the portion," the Second Obvious Modification (Ge Overlayer Metalization) satisfies claim element [1.10].

l. Claim Element [1.11]: Second Germanide Layer

319. Claim 1 recites "a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium." Subject to the same caveats about how "germanide layer" is construed and how the phrase "in the first opening and over the portion" is applied, at least one of the asserted combinations of *Ranade* and *Kim* includes "a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer

[371] *See supra* Section VII.D.

comprising silicon, germanium and titanium" for the same reasons I discuss in Section IX.A.3.k regarding claim element [1.10].

m. Claim Element [1.12] First Contact Plug

320. Claim 1 recites "a first contact plug in the first opening and on the first germanide layer." Subject to the caveats I set out in Section IX.A.3.k about how "germanide layer" is construed, at least one of the asserted combinations of *Ranade* and *Kim* includes "a first contact plug in the first opening and on the first germanide layer."

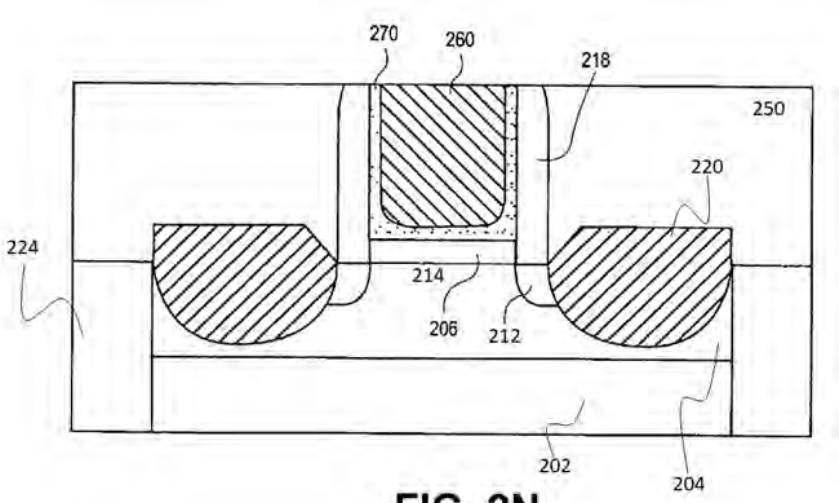


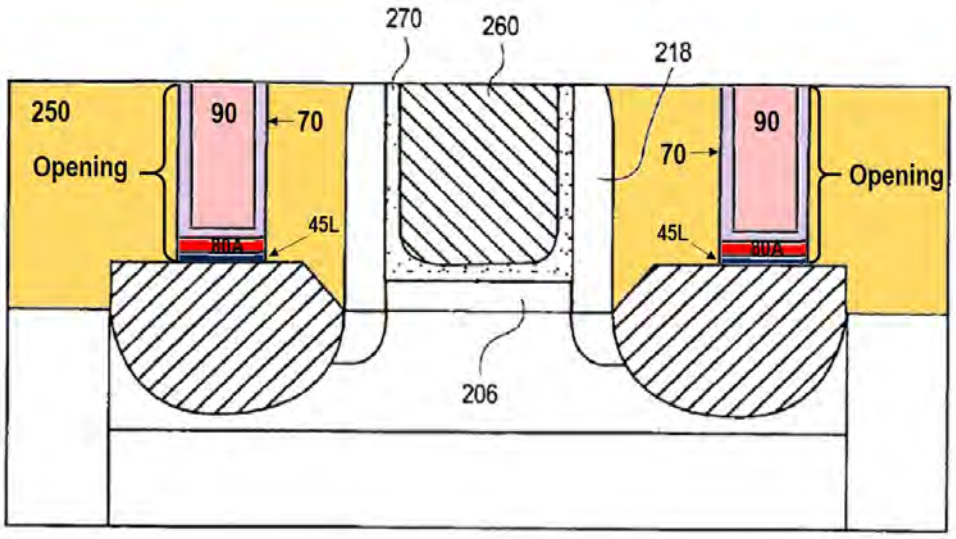
FIG. 2N

321. *Ranade* teaches a FinFET similar to what Figure 2N above shows (onto which I copied additional reference numerals from Figures 2A-2M for clarity).[372] But as I explain in Section IX.A.1, *Ranade*'s figures do not illustrate the necessary interconnections to connect the source/drain regions to other devices on

[372] *Ranade* ¶ [0025].

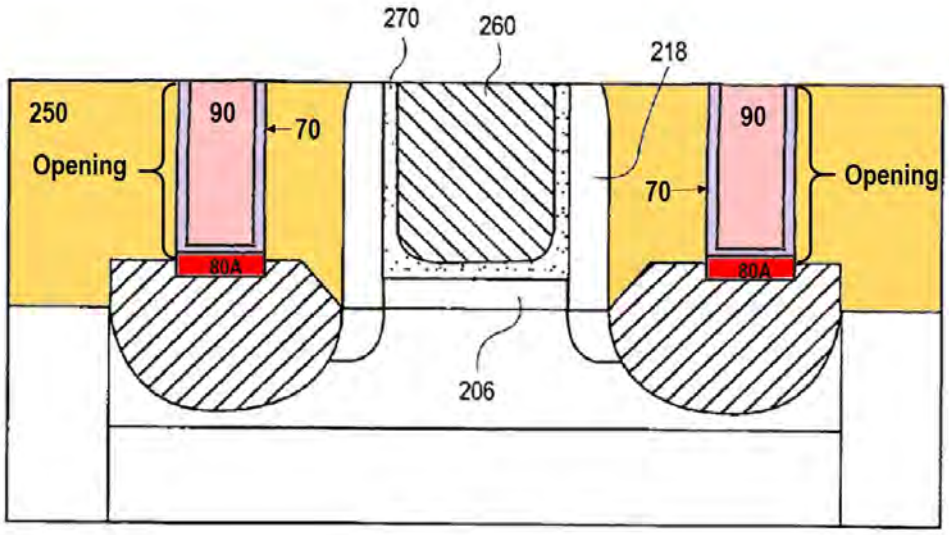
the wafer and to the outside world. Rather, *Ranade* simply states that its devices may "undergo typical process steps to complete the formation of a MOS-FET."[373]

322. As I explain in Section IX.A.1, a person of ordinary skill in the art would have wanted to implement *Ranade*'s FinFETs according to either the First Obvious Modification or the Second Obvious Modification by following *Kim*'s teachings. As the illustrations below demonstrate, both the First Obvious Modification and the Second Obvious Modification include contact plugs, which, for the reasons I explain in Section VI.F, were essentially universal for such devices at the time.



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**

[373] *Id.* ¶ [0041].



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

As shown here, the First and Second Obvious Modifications both have *Kim*'s contact plugs 90 (pink)[374] located in the openings of interlayer dielectric 250.[375] The contact plugs 90 are surrounded by barrier metals 70 (purple)[376] and located on the TiSi1-yGey layers 80A (red).[377] Thus, subject to the construction of "germanide layer" as discussed in Section IX.A.3.k, *Ranade*'s FinFET implemented according to at least one of the asserted combinations of *Ranade* and *Kim* includes "a first contact plug in the first opening and on the first germanide layer."

---

[374] *See Kim* ¶¶ [0049], [0050], [0058], [0068], Figs. 1F, 2D.

[375] *See Ranade* ¶ [0041], Figs. 2L-2N.

[376] *See Kim* ¶¶ [0046]-[0048], [0050], [0057], [0066], [0067], [0071], [0073], Figs. 1F, 2D, 3F.

[377] *See id.* ¶¶ [0048]-[0051], [0057], [0058], [0067], [0068], [0071], [0073], Figs. 1F, 2D, 3F, 4, 5.

323. Thus, and again subject to the caveats I set out in Section IX.A.3.k about how "germanide layer" is construed, at least one of the First Obvious Modification (Ge Overlayer Metalization) and Second Obvious Modification (Direct Metalization) includes "a first contact plug in the first opening and on the first germanide layer."

n. Claim Element [1.13] Second Contact Plug

324. Claim 1 recites "a second contact plug in the second opening and on the second germanide layer." Subject to the caveats I set out in Section IX.A.3.k about how "germanide layer" is construed, at least one of the First Obvious Modification (Ge Overlayer Metalization) and Second Obvious Modification (Direct Metalization) includes "a second contact plug in the second opening and on the second germanide layer" for the same reasons discussed in Section IX.A.3.m for claim element [1.12].

o. A Person of Ordinary Skill in the Art Would Have Found Claim 1 Obvious

325. Because a person of ordinary skill in the art would have been motivated to make the combinations of *Ranade* and *Kim* described above, because he or she would have reasonably expected to succeed in doing so, and because at

least one of those combinations satisfies each element of claim 1,[378] it is my opinion that claim 1 would have been obvious.

4. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 5 Obvious

326. Claim 5 depends from claim 1. I understand that means claim 5 requires all the same features as claim 1, plus the additional features recited in claim 5. At least one of the asserted combinations of *Ranade* and *Kim* includes all the features recited in claim 1 for the reasons I provide in Sections IX.A.3.a-n above.

327. Claim 5 further recites "an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region." The asserted combinations of *Ranade* and *Kim* both provide a FinFET that includes "an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region" as claimed.

[378] There may be differences between the First Obvious Modification (Ge Overlayer Metalization) and Second Obvious Modification (Direct Metalization) depending on the construction of "germanide layer" and how the phrase "in the first opening and over the portion" is applied. *See, e.g.*, *supra* Section IX.A.3.k.

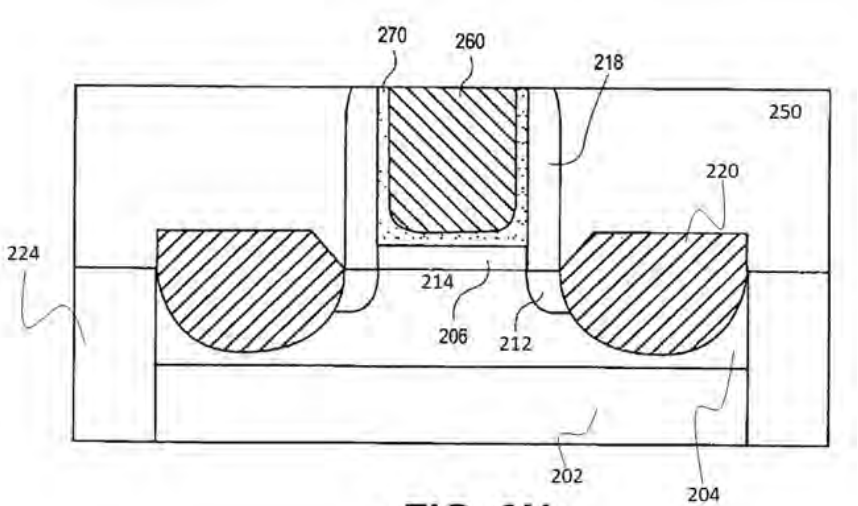


FIG. 2N

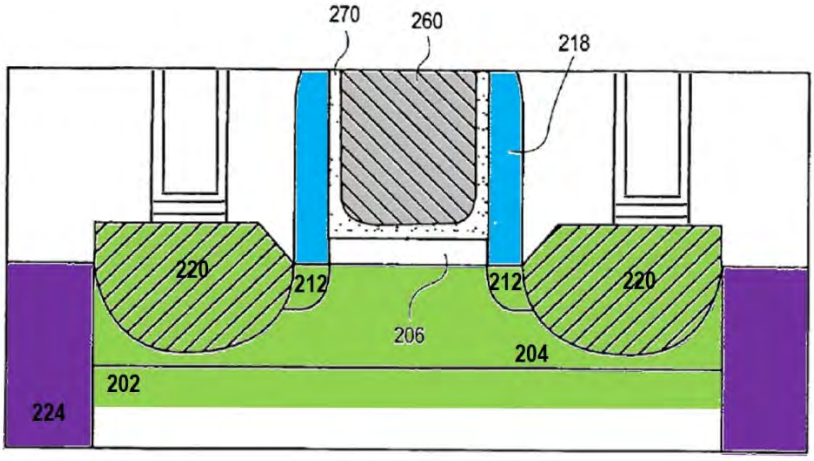
328. *Ranade* teaches a FinFET device similar to what Figure 2N above shows (onto which I have copied additional reference numerals from Figures 2A-2M for clarity).[379] As shown, *Ranade*'s FinFET device includes "shallow trench isolation regions 224 and 226" that are "formed in substrate 202."[380]

329. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFETs according to the First Obvious Modification and the Second Obvious Modification. I created the figures below for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings. As these figures make clear, parts of the fin (green) protrude through the isolation region (purple). Further, a portion of the gate

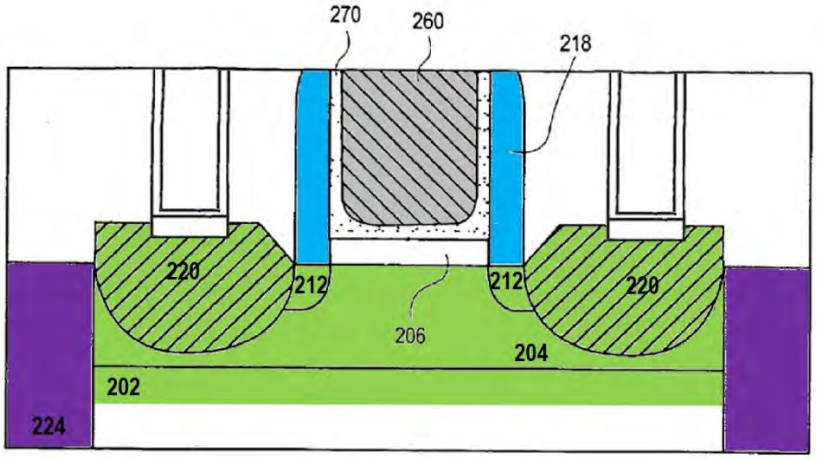
[379] *Ranade* ¶ [0025].

[380] *Id.* ¶ [0030]; *see also id.* ¶¶ [0031], [0041], Figs. 2C, 2C', 2D, 2L-2N, 3A-3C.

electrode (gray) and a portion of the first and second dielectric spacers (blue) lie over the isolation region (purple).



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**

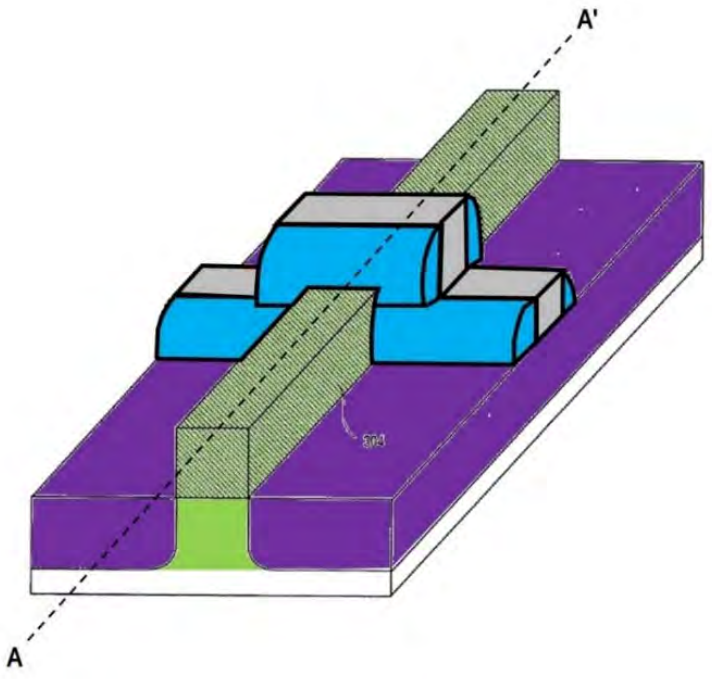


***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

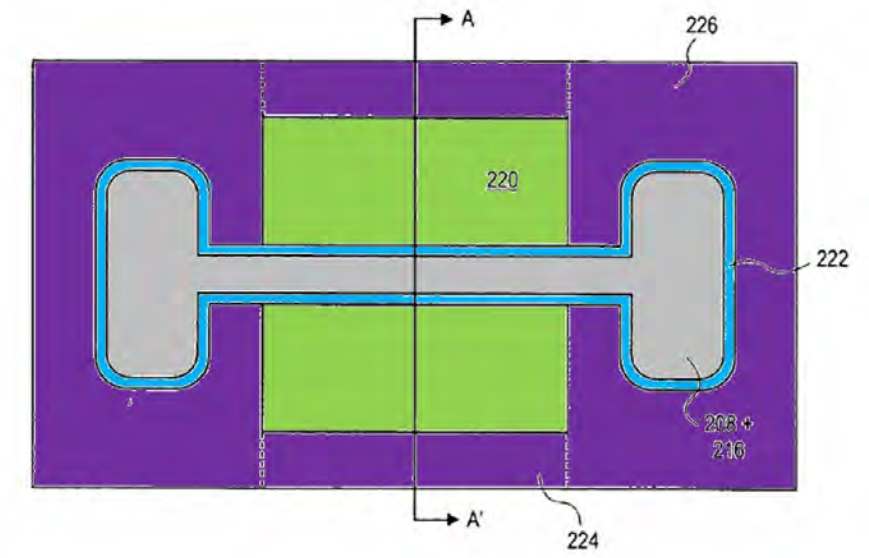
330. To provide an approximate orthographic illustration, I have also annotated *Ranade*'s Figure 3C below to show the gate electrode in gray, the dielectric spacers in blue, the fin in green, and the isolation regions in purple.[381] I

[381] The fin shown in Figure 3C will change somewhat once the epitaxial source/drain regions are formed. *See supra* note 305 and related text.

also added a line A–A' to indicate the approximate cross-section that would correspond to the figures above once the combined *Ranade-Kim* FinFET device has been completed. A person of ordinary skill in the art would have recognized that *Ranade*'s FinFET, even once implemented according to *Kim* (as shown above), would still include an isolation region (purple), wherein the fin (green) protrudes through the isolation region (purple), and wherein a portion of the gate electrode (gray), a portion of the first dielectric spacer (blue), and a portion of the second dielectric spacer (also blue) are over the isolation region (purple). This is a basic characteristic of FinFETs made from a single-crystal substrate (as opposed to a silicon-on-insulator (SOI) substrate, for example) to isolate the devices from one another.



331. Additionally, the figure below based on *Ranade*'s Figure 2C' confirms this feature is present.



Although the figure above shows a planar layout, the only real difference for a FinFET would be that the green region corresponds to one or more fin rather than raised planar source/drain regions. Figures 2N, 3C, and 2C' above confirm that such fins (green) extend through isolation regions 224 and 226 (purple). Moreover, *Ranade* explains that the gate structure (including gate electrode 208 (gray) and gate isolation spacers 222 (blue)) must be formed on top of isolation region 226 (purple):

> As would be apparent to one of ordinary skill in the art, **shallow-trench isolation regions 224 and 226 would typically have been formed in substrate 202 prior to the formation of dielectric layer 206**. For example, in accordance with an embodiment of the present invention, shallow-trench isolation regions 224 and 226 are formed by filling trenches created in substrate 202 with a dielectric

> material, e.g. a silicon dioxide material deposited by a chemical vapor deposition process.[382]

332. Because *Ranade* teaches a FinFET with a gate electrode and dielectric spacers over isolation regions and a fin that protrudes through the isolation regions, and because *Ranade*'s FinFET implemented using *Kim*'s teachings, as I describe in Section IX.A.1, also includes each of these, a person of ordinary skill in the art would have understood the *Ranade-Kim* combinations each have "an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region" as claimed.

5. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 6 Obvious

333. Claim 6 depends from claim 1. I understand that means claim 6 requires all the same features as claim 1, plus the additional features recited in claim 6. At least one of the asserted combinations of *Ranade* and *Kim* includes all the features recited in claim 1 for the reasons I provide in Sections IX.A.3.a-n.

334. Claim 6 further recites "a gate dielectric layer, wherein the gate electrode is on the gate dielectric layer, wherein the gate dielectric layer comprises a high-k dielectric material, and wherein the gate electrode comprises a metal layer." The asserted combinations of *Ranade* and *Kim* both provide a FinFET that

[382] *Ranade* ¶ [0030].

includes "a gate dielectric layer, wherein the gate electrode is on the gate dielectric layer, wherein the gate dielectric layer comprises a high-k dielectric material, and wherein the gate electrode comprises a metal layer" as claimed.

335. By December 2010, so-called high-k metal gates were common, and claim 6 merely recites a high-k metal gate. *Ranade* teaches a FinFET device similar to what Figure 2N below shows (onto which I have copied additional reference numerals from Figures 2A-2M for clarity).[383]

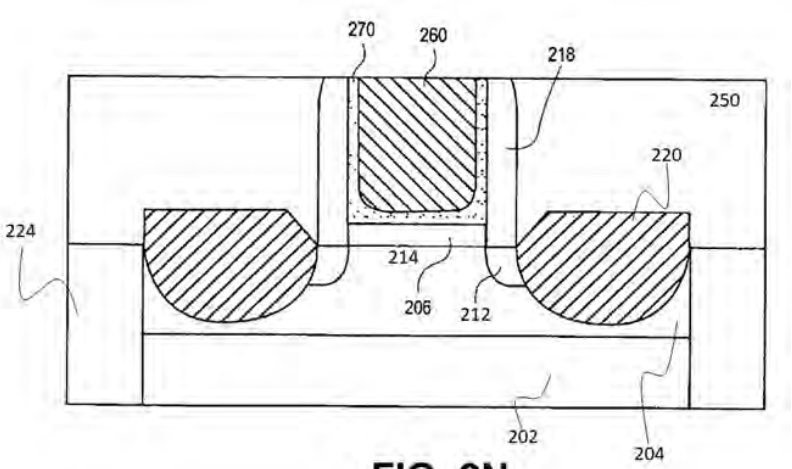


FIG. 2N

As shown here, *Ranade*'s FinFET includes "[a] gate electrode 208" (or replacement gate electrode 260) "formed above gate dielectric layer 206."[384] According to *Ranade*, gate dielectric layer 206 may be a high-k dielectric, or it can be made of two layers—a lower layer 206A of silicon dioxide or silicon oxynitride

[383] *Ranade* ¶ [0025].

[384] *Id.* ¶ [0028]; *see also id.* ¶¶ [0011], [0018], [0020], [0024], [0026], [0027], [0030]-[0032], [0042], Figs. 1A-2C, 2D-2N.

and an upper layer 206B of high-k dielectric material.[385] Either a gate electrode 208 or replacement gate electrode 260 may be applied above of that.[386] Gate electrode 208 may be "a metal layer."[387] Or, as Figure 2N above shows, "gate electrode 208 may be removed and replaced with an alternative gate electrode 260," and "an additional dielectric layer 270 may be added to gate dielectric layer 206."[388] Additional gate dielectric layer 270 may be a high-k dielectric material,[389] and alternative gate electrode 260 may be a metal.[390]

336. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFETs according to the First Obvious Modification and the Second Obvious Modification. I created the figures below for illustrative purposes by modifying Figure 2N of *Ranade* to reflect *Kim*'s teachings. As these figures makes clear, both asserted combinations of *Ranade* and *Kim* have a gate dielectric layer (green and yellow), and the gate electrode (gray) is on the gate dielectric layer (green and yellow).[391] Additionally,

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[385] *Id.* ¶ [0027]; *see also id.* ¶¶ [0011], [0015], [0018], [0020], [0024], [0026], [0042], [0045], Figs. 1B, 2A', 2N, claims 6, 7, 13, 14.

[386] *See id.* ¶¶ [0015], [0028], [0042], Figs. 1B, 2M, 2N.

[387] *Id.* ¶ [0019]; *see also* Figs. 1B, 2M, 2N.

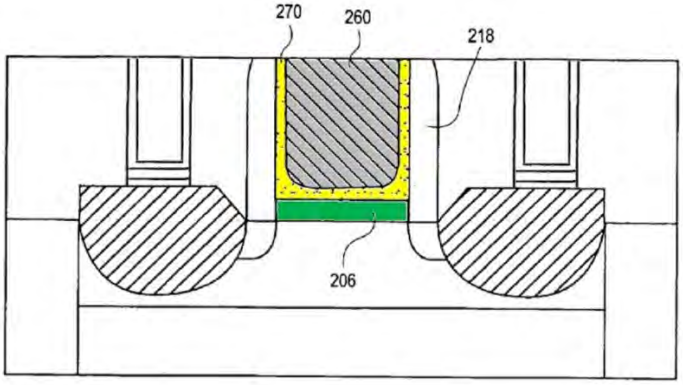
[388] *Id.* ¶ [0042]; *see also id.* at Fig. 2N.

[389] *Id.* ¶ [0042]; *see also id.* ¶¶ [0011], [0018], [0024], [0027], claims 6, 7, 13, 14.

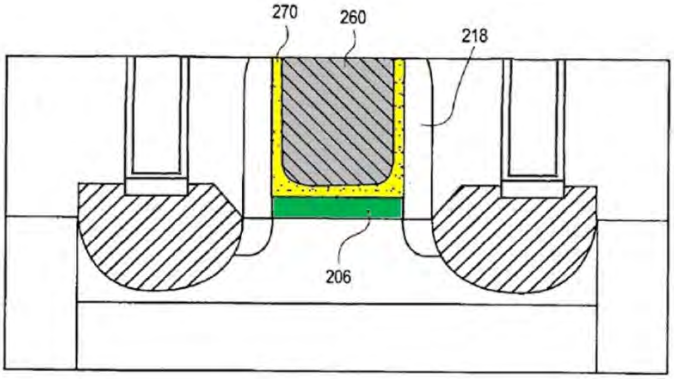
[390] *Id.* ¶ [0042]; *see also id.* ¶¶ [0019], [0028].

[391] *See id.* ¶¶ [0015], [0028], [0042], Figs. 1B, 2M, 2N.

the gate dielectric layer (green and yellow) includes a high-k dielectric material, and the gate electrode includes a metal layer.[392]



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

337. Because *Ranade* teaches a FinFET with a metal gate electrode located on a high-k gate dielectric, and because *Ranade*'s FinFET implemented using *Kim*'s teachings as described in Section IX.A.1 also includes these features, a person of ordinary skill in the art would have understood the *Ranade-Kim* combinations each have "a gate dielectric layer, wherein the gate electrode is on the gate dielectric layer, wherein the gate dielectric layer comprises a high-k

[392] *See id.* ¶¶ [0011], [0018], [0024], [0027], [0042], claims 6, 7, 13, 14.

dielectric material, and wherein the gate electrode comprises a metal layer" as claimed.

6. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 7 Obvious

338. Claim 7 depends from claim 1. I understand that means claim 7 requires all the same features as claim 1, plus the additional features recited in claim 7. At least one of the asserted combinations of *Ranade* and *Kim* includes all the features recited in claim 1 for the reasons I provide in Sections IX.A.3.a-n above.

339. Claim 7 further recites "the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets." The asserted combinations of *Ranade* and *Kim* both provide a FinFET that includes "the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets" as claimed.

340. *Ranade* teaches a FinFET device similar to what Figure 2N below shows (onto which I have copied additional reference numerals from Figures 2A-2M for clarity).[393] As shown here, *Ranade*'s FinFET device includes

[393] *Ranade* ¶ [0025].

source/drain regions that comprise epitaxial source/drain regions 220 and source/drain tip extensions 212.[394]

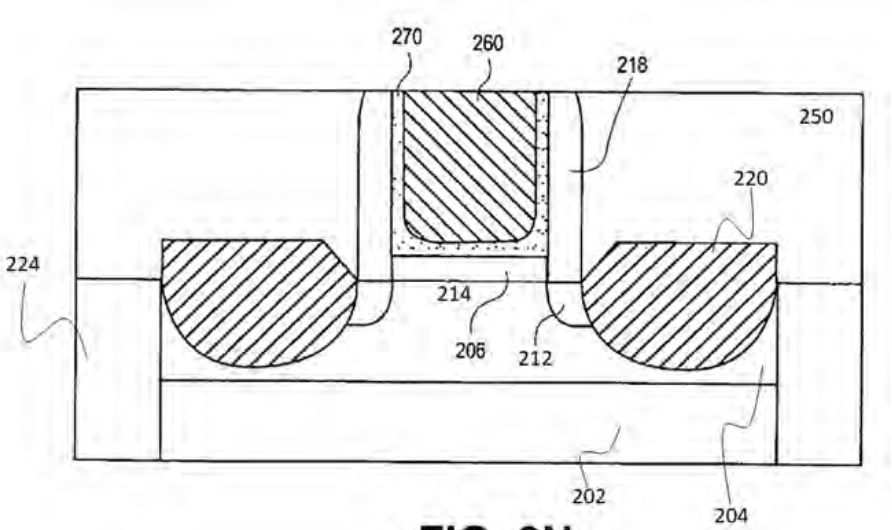


FIG. 2N

341. A person of ordinary skill in the art would have understood that *Ranade*'s Figure 3C below shows *Ranade*'s FinFET device at a stage of processing analogous to the one shown in *Ranade*'s Figure 2E—that is, before the tip extensions have been implanted into the active region (Figures 2F and 2G), before the source/drain regions have been regrown (Figures 2H-2K), before the interlayer dielectric has been deposited (Figures 2L and 2M), and before the replacement metal gate process has been performed (Figure 2N).[395] A person of ordinary skill in the art would have understood that epitaxial source/drain regions 220 are grown to

[394] *Id.* ¶ [0040]; *see also id.* ¶¶ [0020], [0021], [0023], [0031], [0034], [0035], [0037]-[0041], [0044]-[0046], Figs. 1B, 2G-3C.

[395] *Id.* ¶¶ [0025], [0046]; *see also id.* ¶¶ [0032], [0044], [0045], Figs. 2E, 3A-3C.

replace the exposed parts of active region 304 shown below that are not covered by gate electrode 308 or gate isolation spacers 318.[396]

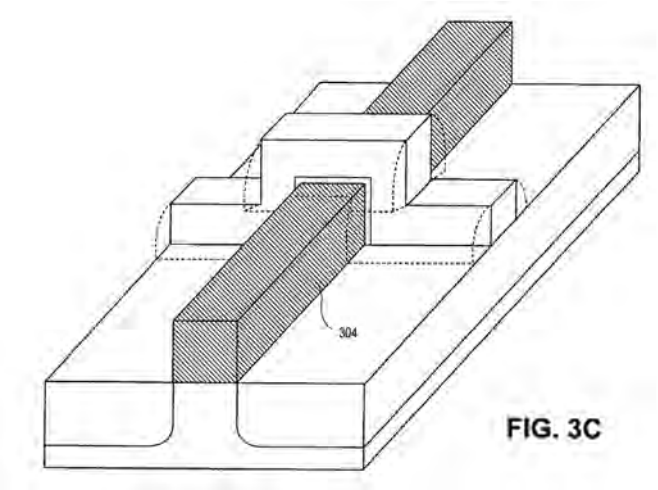


FIG. 3C

342. *Ranade* teaches that the first and second source/drain regions have two or more facets. A person of ordinary skill in the art would have understood that a "facet" here refers to the surface of a semiconductor crystal plane. Figure 3C, for example, is a simplified cartoon that depicts the fin with a rectangular or square cross-section having two facets (one on each side).[397]

343. The specification of the '281 Patent does not mention the shape of the fins. It only briefly mentions using "an ammonia etch to form faceted fin

[396] *See id.* ¶ [0045], Figs. 3A-3C; *see also id.* ¶¶ [0037]-[0040], Figs. 2I-2K.

[397] *See id.* ¶¶ [0031], [0038] (describing embodiments in which the epitaxial SiGe source/drain regions are grown in trenches formed with <111> facets, which a person of ordinary skill in the art would have understood translates into epitaxial source/drain regions with <111> crystal facets), Fig. 2D'; *see also Simonelli* (US2010/0148217) ¶¶ [0036]-[0040], Figs. 4, 5; *Haran* at 6:20-65, Fig. 6.

recess."[398] *Ranade* expressly teaches the same thing. It describes how to grow epitaxial SiGe source/drain regions 220 in trenches formed with <111> facets by treating the substrate with tetramethylammonium hydroxide (TMAH) or ammonium hydroxide (NH_4OH).[399] A person of ordinary skill in the art would have understood this process translates into epitaxial source/drain regions with <111> crystal facets for both planar and FinFET embodiments.

344. The profile that results from this treatment appears in *Ranade*'s Figure 2D', shown below on the left, and in Figure 3A in the '281 Patent, shown below on the right.

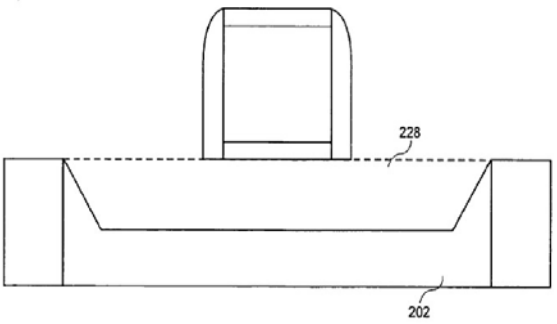


FIG. 2D'

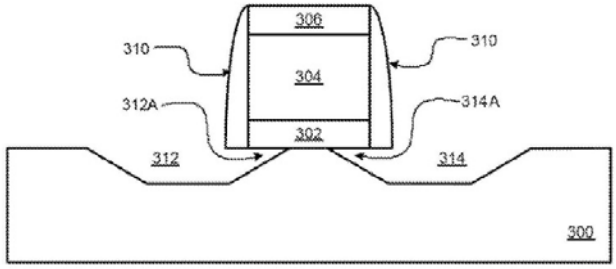


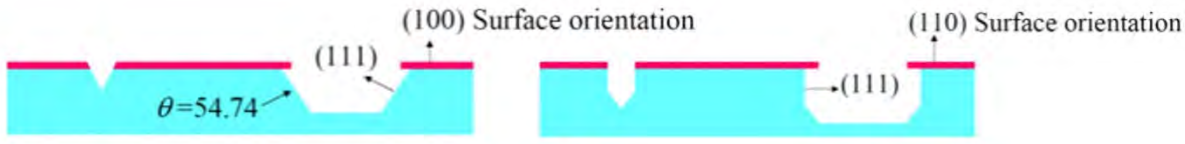
FIG. 3A

The profile in the figures above is characteristic of what results when applying TMAH or NH_4OH to an industry-standard Si wafer oriented with a (100) surface and a notch on the [110] axis. As shown below, this profile only results for (100) oriented surfaces. Thus, a person of ordinary skill in the art would have understood

[398] '281 Patent at 7:27-32, Figs. 3A, 5A.

[399] *Ranade* ¶¶ [0031], [0038], Fig. 2D'.

that *Ranade*'s epitaxial source/drain regions 220, like the source/drain regions in the '281 Patent, have at least two <111> facets along the sides of the fin and a top surface.[400]

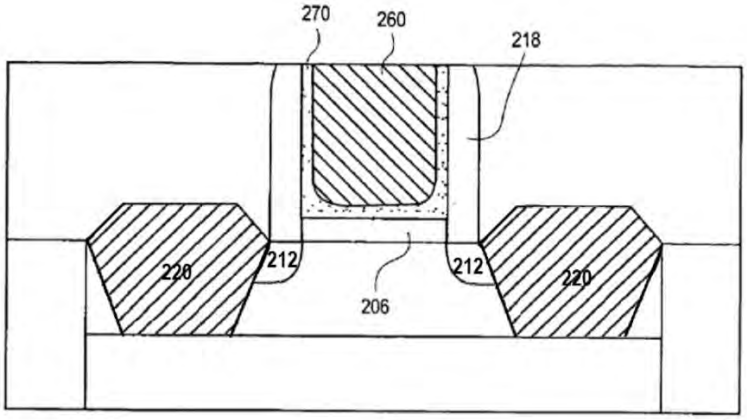


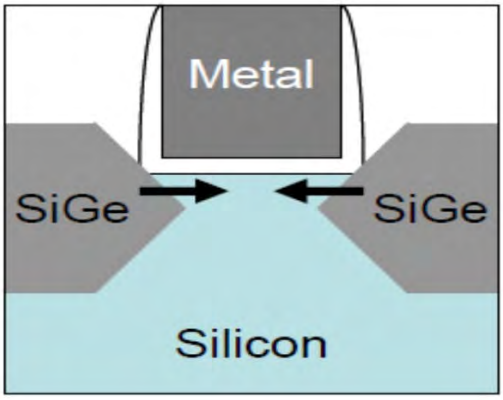
345. Similarly, *Ranade* explains that "a wet etch step utilizing aqueous solutions of NH_4OH or tetramethylammonium hydroxide is used to form etched-out regions 240" that would "assume a tapered profile" not shown in 2J "[f]or illustrative purposes."[401] A person of ordinary skill in the art, however, would have immediately understood from this statement that *Ranade* is describing the faceted shapes shown below for epitaxial source/drain regions 220. The *Ranade-Kim* combinations would include the same.

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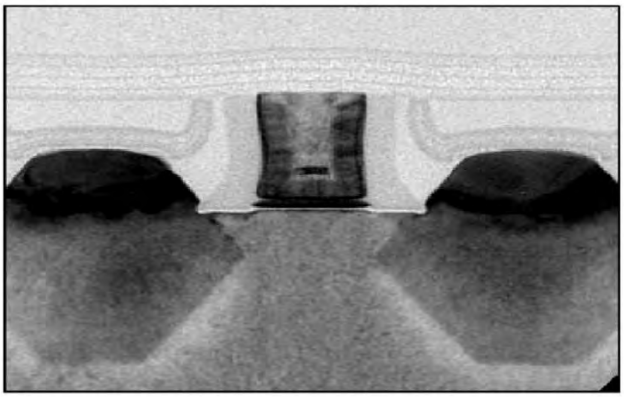
[400] *See FinFETs and Other Multi-Gate Transistors* at 90, 100, Figs. 2.37, 2.45 (J.-P. Colinge ed., 2008); *Tung* ¶ [0058]; *Lin '894* (US8652894) at 1:27-43, 5:21-6:7, 7:42-50, 10:1-40, 10:61-66, 12:12-20, Fig. 5A; *Kwok* (US8362575) at 1:38-42, 2:28-3:50, Figs. 1, 2A, 3-7; *supra* Section VI.G.

[401] *Id.* ¶ [0038]; *see also id.* at Fig. 2J; S. Natarajan et al., *A 32nm Logic Technology Featuring 2nd-Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171 μm^2 SRAM Cell Size in a 291 Mb Array*, Technical Digest of the 2008 International Electron Devices Meeting (IEDM), at Fig. 2 (2008); K. Mistry et al., *A 45nm Logic Technology with High-k + Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193 nm Dry Patterning, and 100% Pb-Free Packaging*, Technical Digest of the 2007 International Electron Devices Meeting (IEDM), at Fig. 6 (2007).





Natarajan et al., Fig. 2

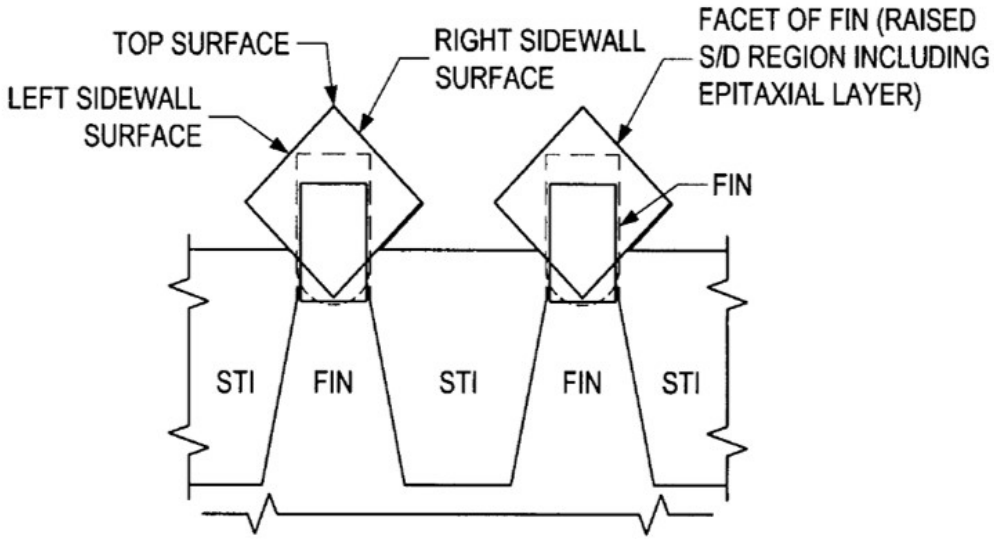


Mistry et al., Fig. 6

346. In addition to these express disclosures, a person of ordinary skill in the art would have known that for epitaxial SiGe source/drain fin regions like the ones *Ranade* teaches, the source/drain regions "naturally grow in a diamond shape," as the figure below illustrates.[402] "[T]he substrate, channel, and facet each have a different crystallographic orientation (e.g., wafer (001)/channel (110)/facet

[402] *Lin '894* (US8652894) at 10:25-26; *see also id.* at 1:27-43, 5:21-6:7, 7:42-50, 10:1-40, 10:61-66, 12:12-20, Fig. 5A; *Kwok* (US8362575) at 1:38-42, Figs. 1, 2A, 3-7; *supra* Section VI.G.

(111)).”[403] Again, *Ranade*’s Figure 3C is a simplified cartoon that illustrates *Ranade*’s FinFET before the source/drain regions have been regrown (Figures 2H-2K).[404] Once regrown, a person of ordinary skill in the art would have understood that *Ranade*’s source/drain regions 220 would have diamond-shaped facets like the ones above.[405] And a person of ordinary skill in the art further would have appreciated that source/drain extension regions 212 are not recessed or regrown because they are underneath the gate sidewalls and therefore retain the square/rectangular facets of the original fin 304 shown in Figure 3C.[406]



***Lin ’894,* Fig. 5A**

[403] *Lin ’894* (US8652894) at 10:21-24; *see also Kwok* (US8362575) at 1:38-42.

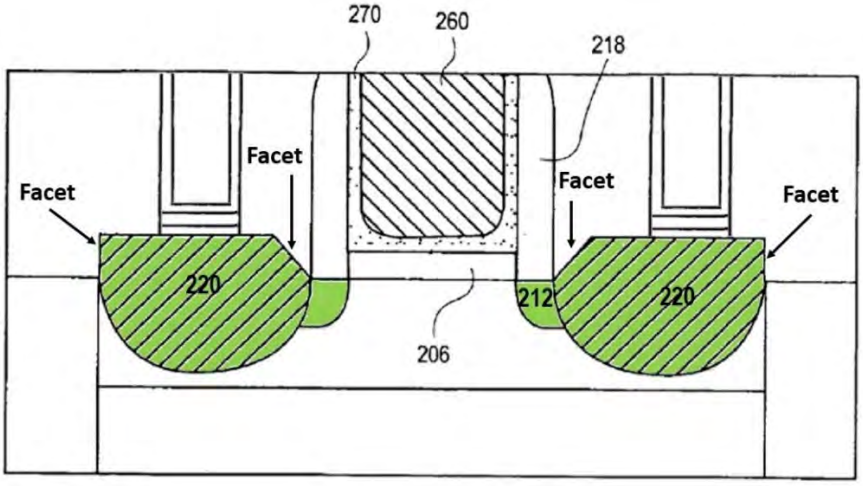
[404] *See Ranade* ¶¶ [0036]-[0040], [0043]-[0046], Figs. 2E, 2H-2K, 3A-3C.

[405] *See Lin ’894* (US8652894) at 1:27-43, 5:21-6:7, 7:42-50, 10:1-40, 10:61-66, 12:12-20, Fig. 5A; *Kwok* (US8362575) at 1:38-42, 2:28-3:50, Figs. 1, 2A, 3-7.

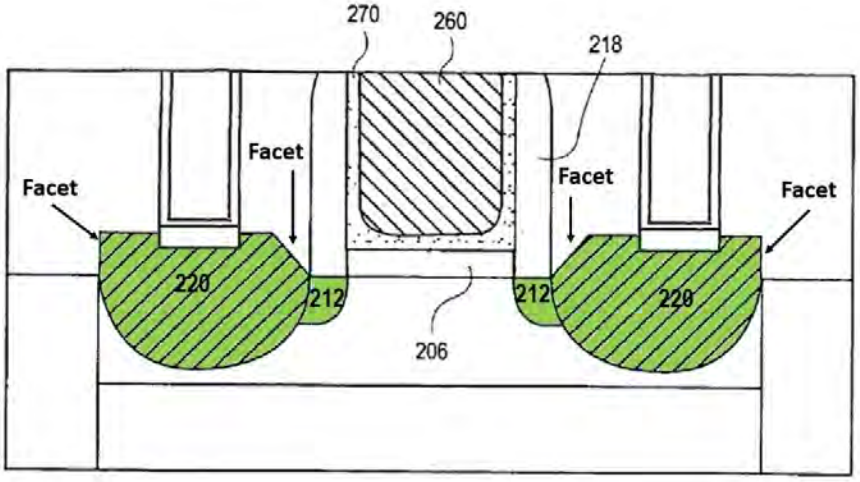
[406] *See Ranade* ¶¶ [0038]-[0040], [0043]-[0046], Figs. 2J-2K, 3C; *Lin ’894* (US8652894) at Figs. 5A, 5B.

347. Both *Ranade*'s regrown epitaxial source/drain regions 220 (diamond-shaped) and source/drain extensions 212 (square/rectangular-shaped) satisfy the claim language. A person of ordinary skill in the art would have understood from his or her training that either a diamond or square/rectangular shape fin is raised above the substrate surface and has at least two facets. Consistent with the figures above, a person of ordinary skill in the art would have understood from his or her training and *Ranade*'s teachings that at the epitaxially grown SiGe source/drain regions 220 in *Ranade*'s FinFET would have had at least two facets. Accordingly, by teaching epitaxially grown SiGe source/drain regions 220, *Ranade*'s FinFET includes "the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets." A person of ordinary skill in the art would have understood that epitaxial films are, by definition, crystalline films, and therefore terminated by crystal facets.

348. As I explain in Section IX.A.1, a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFET device according to the First Obvious Modification and the Second Obvious Modification, as the figures below illustrate. I created these figures for illustrative purposes by modifying *Ranade*'s Figure 2N to reflect *Kim*'s teachings. I have highlighted the constituent parts of two different source/drain regions in green. I have also labeled the facets of the source/drain regions.



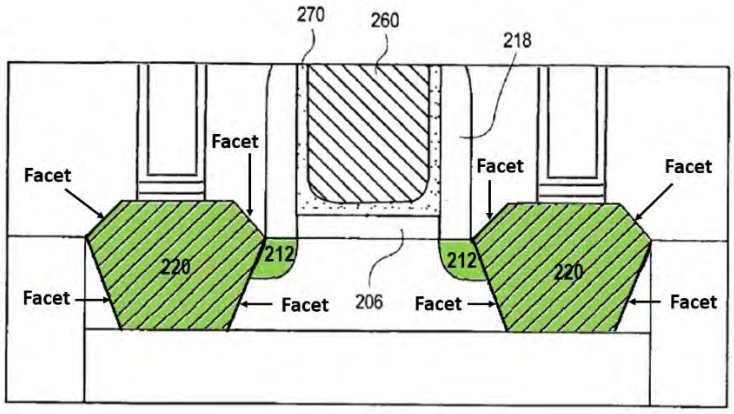
***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



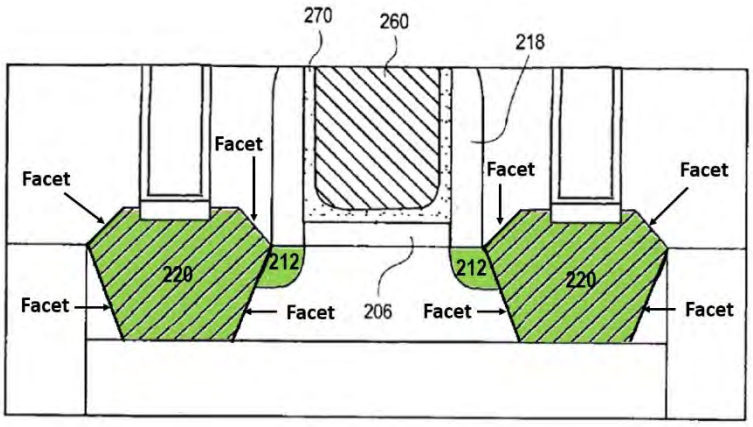
***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

349. Had the substrate in the example below been treated with tetramethylammonium hydroxide or ammonium hydroxide, as *Ranade* further teaches, the facets of epitaxial source/drain regions 220 would appear as below.[407]

[407] *Ranade* ¶ [0038]; *see also id.* at Fig. 2J; S. Natarajan et al., *A 32nm Logic Technology Featuring 2nd-Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171 μm² SRAM Cell Size in a 291 Mb Array*, Technical Digest of the 2008 International Electron Devices Meeting (IEDM), at



***Ranade-Kim*: First Obvious Combination (Ge Overlayer Metalization)**



***Ranade-Kim*: Second Obvious Combination (Direct Metalization)**

350. For all the reasons stated above, a person of ordinary skill in the art would have recognized that *Ranade*'s FinFET, as implemented according to *Kim* (shown above), includes "the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets."

Fig. 2 (2008); K. Mistry et al., *A 45nm Logic Technology with High-k + Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193 nm Dry Patterning, and 100% Pb-Free Packaging*, Technical Digest of the 2007 International Electron Devices Meeting (IEDM), at Fig. 6 (2007).

351. Because *Ranade* discloses source/drain regions with at least two crystal facets (as would be expected for any FinFET), and because *Ranade*'s FinFET implemented using *Kim*'s teachings as described in Section IX.A.1 has those same features, a person of ordinary skill in the art would have understood each of the *Ranade-Kim* combinations satisfies "the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets" as claimed.

7. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 8 Obvious

a. Claim Element [8.0]: The Preamble

352. Claim 8 recites "[a]n integrated circuit structure." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.0].[408]

b. Claim Element [8.1]: Body

353. Claim 6 recites "a body comprising silicon." A person of ordinary skill in the art would have understood the '281 Patent uses the term "body" only

[408] *See supra* Section IX.A.3.a.

once, equating it with a "fin."[409] Thus, the asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.1].[410]

c. Claim Element [8.2]: Gate Electrode

354. Claim 8 recites "a gate electrode over the body, the gate electrode having a first side, and the gate electrode having a second side opposite the first side." A person of ordinary skill in the art would have understood the '281 Patent uses the term "body" only once, equating it with a "fin."[411] Thus, the asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.2].[412]

d. Claim Element [8.3]: First Dielectric Spacer

355. Claim 8 recites "a first dielectric spacer along the first side of the gate electrode." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.3].[413]

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[409] *See* '281 Patent at 13:35-38 ("As can be seen, the **tri-gate device** includes a substrate 600 having a semiconductor **body or fin 660** (represented by dashed lines) extending from the substrate 600 through isolation regions 610, 620."); *see also id.* at Fig. 6.

[410] *See supra* Section IX.A.3.b.

[411] *See supra* note 409.

[412] *See supra* Section IX.A.3.c.

[413] *See supra* Section IX.A.3.d.

e. Claim Element [8.4]: First Source or Drain Region

356. Claim 8 recites "a first source or drain region in the body proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer." A person of ordinary skill in the art would have understood the '281 Patent uses the term "body" only once, equating it with a "fin."[414] Thus, the asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.4].[415]

f. Claim Element [8.5]: Graded Germanium Concentration of the First Source or Drain Region

357. Claim 8 recites "wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.5].[416]

g. Claim Element [8.6]: Second Dielectric Spacer

358. Claim 8 recites "a second dielectric spacer along the second side of the gate electrode." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.6].[417]

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[414] *See supra* note 409.

[415] *See supra* Section IX.A.3.e.

[416] *See supra* Section IX.A.3.f.

[417] *See supra* Sections IX.A.3.d, IX.A.3.g.

h. Claim Element [8.7]: Second Source or Drain Region

359. Claim 8 recites "a second source or drain region in the body proximate a second side of the gate electrode opposite the first side, a portion of the second source or drain region beneath the second dielectric spacer." A person of ordinary skill in the art would have understood the '281 Patent uses the term "body" only once, equating it with a "fin."[418] Thus, the asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.7].[419]

i. Claim Element [8.8]: Graded Germanium Concentration of the Second Source or Drain Region

360. Claim 8 recites "wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.8].[420]

j. Claim Element [8.9]: Interlayer Dielectric

361. Claim 8 recites "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the

[418] *See supra* note 409.

[419] *See supra* Sections IX.A.3.e, IX.A.3.h.

[420] *See supra* Sections IX.A.3.f, IX.A.3.i.

dielectric layer having a second opening exposing only a portion of the second source or drain region." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.9].[421]

k. Claim Element [8.10]: First Germanide Layer

362. Claim 8 recites "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium." Subject to the same caveats set forth in Section IX.A.3.k regarding the construction of "germanide layer" and how the phrase "in the first opening and over the portion" is applied, at least one of the asserted combinations of *Ranade* and *Kim* includes this feature for the same reasons I provide for claim element [1.10].[422]

l. Claim Element [8.11]: Second Germanide Layer

363. Claim 8 recites "a second germanide layer in the first opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium." Subject to the same caveats set forth in Section IX.A.3.k regarding the construction of "germanide layer" and how the phrase "in the first opening and over the portion" is applied, at least one of the

[421] *See supra* Section IX.A.3.j.

[422] *See supra* Section IX.A.3.k.

asserted combinations of *Ranade* and *Kim* includes this feature for the same reasons I provide for claim element [1.11].[423]

m. Claim Element [8.12]: First Contact Plug

364. Claim 8 recites "a first contact plug in the first opening and on the first germanide layer." Subject to the same caveats regarding the construction of "germanide layer" set forth in Section IX.A.3.k, at least one of the asserted combinations of *Ranade* and *Kim* includes this feature for the same reasons I provide for claim element [1.12].[424]

n. Claim Element [8.13]: Second Contact Plug

365. Claim 8 recites "a second contact plug in the second opening and on the second germanide layer." Subject to the same caveats regarding the construction of "germanide layer" set forth in Section IX.A.3.k, at least one of the asserted combinations of *Ranade* and *Kim* includes this feature for the same reasons I provide for claim element [1.13].[425]

o. A Person of Ordinary Skill in the Art Would Have Found Claim 8 Obvious

366. Because a person of ordinary skill in the art would have been motivated to make the combinations of *Ranade* and *Kim* described above, because

[423] *See supra* Sections IX.A.3.k, IX.A.3.l.

[424] *See supra* Section IX.A.3.m.

[425] *See supra* Sections IX.A.3.m, IX.A.3.n.

he or she would have reasonably expected to succeed in doing so, and because at least one of those combinations satisfies each element of claim 8,[426] it is my opinion that claim 8 would have been obvious.

8. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 12 Obvious

a. Claim Element [12.0]: The Preamble

367. Claim 12 recites "[a] computing device." The asserted combinations of *Ranade* and *Kim* are both structures used in "a computing device."

368. As I explain in Section IX.A.3.a, the asserted combinations of *Ranade* and *Kim* are both components of "an integrated circuit device."[427] And as I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

369. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of

[426] There may be differences between the First Obvious Modification (Ge Overlayer Metalization) and Second Obvious Modification (Direct Metalization) depending on the construction of "germanide layer." *See, e.g., supra* Section IX.A.3.k.

[427] *See, e.g.*, *Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

integrated circuits, which, after they are packaged, are called "chips."[428] A person of ordinary skill in the art also would have understood that semiconductor chips are combined with other electronic circuit elements onto a circuit board for use in consumer electronic devices. And a person of ordinary skill in the art would have understood that many of the most popular consumer electronic devices were computing devices, such as smartphones, tablets, personal computers, and the like. In short, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade* and *Kim* are both FET structures used in computing devices because such FET structures are designed for use in the integrated circuits that make computing devices function.

370. Accordingly, a person of ordinary skill in the art would have understood the combination of *Ranade* and *Kim* would go into "[a] computing device."

b. Claim Element [12.1]: Board

371. Claim 12 recites "a board." The asserted combinations of *Ranade* and *Kim* are both structures used in semiconductor chips that would be incorporated onto "a board."

[428] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

372. The asserted combinations of *Ranade* and *Kim* are both components of "an integrated circuit device."[429] As I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

373. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[430] A person of ordinary skill in the art also would have understood that semiconductor chips are combined with other electronic circuit elements onto a circuit board for use in consumer electronic devices. And a person of ordinary skill in the art would have understood that many of the most popular consumer electronic devices were computing devices, such as smartphones, tablets, personal computers, and the like. In short, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade* and *Kim* are both FET structures that would go

[429] *See, e.g.*, *Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

[430] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

onto a circuit board because such FET structures form part of the integrated circuits that go into the circuit boards that make computing devices function.

374. Accordingly, a person of ordinary skill in the art would have understood the combination of *Ranade* and *Kim* would go into a semiconductor chip that gets incorporated into "a board."

c. Claim Element [12.2]: Integrated Circuit Structure

375. Claim 12 recited "a component coupled to the board, the component including an integrated circuit structure." The asserted combinations of *Ranade* and *Kim* are both structures that would constitute part of "a component coupled to the board."

376. The asserted combinations of *Ranade* and *Kim* are both components of "an integrated circuit device."[431] As I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

377. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of

[431] *See, e.g.*, *Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

integrated circuits, which, after they are packaged, are called "chips."[432] A person of ordinary skill in the art also would have understood that semiconductor chips are combined with other electronic circuit elements onto a circuit board for use in consumer electronic devices. A person of ordinary skill in the art would have understood that such semiconductor chips constitute a "component coupled to the board." In short, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade* and *Kim* are both FET structures that would go onto a component coupled to a circuit board because such FET structures form part of the integrated circuits coupled to the circuit boards in computing devices.

378. Accordingly, a person of ordinary skill in the art would have understood the combination of *Ranade* and *Kim* go into "a component coupled to the board, the component including an integrated circuit structure."

d. Claim Element [12.3]: Fin

379. Claim 12 recites "a fin comprising silicon." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.1].[433]

[432] *See, e.g., Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

[433] *See supra* Section IX.A.3.b.

e. Claim Element [12.4]: Gate Electrode

380. Claim 12 recites "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.2].[434]

f. Claim Element [12.5]: First Dielectric Spacer

381. Claim 12 recites "a first dielectric spacer along the first side of the gate electrode." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.3].[435]

g. Claim Element [12.6]: First Source or Drain Region

382. Claim 12 recites "a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.4].[436]

h. Claim Element [12.7]: Graded Germanium Concentration of the First Source or Drain Region

383. Claim 12 recites "wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a

[434] *See supra* Section IX.A.3.c.

[435] *See supra* Section IX.A.3.d.

[436] *See supra* Section IX.A.3.e.

concentration in excess of 50%." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.5].[437]

i. Claim Element [12.8]: Second Dielectric Spacer

384. Claim 12 recites "a second dielectric spacer along the second side of the gate electrode." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.6].[438]

j. Claim Element [12.9]: Second Source or Drain Region

385. Claim 12 recites "a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.7].[439]

k. Claim Element [12.10]: Graded Germanium Concentration of the Second Source or Drain Region

386. Claim 12 recites "wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.8].[440]

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[437] *See supra* Section IX.A.3.f.

[438] *See supra* Sections IX.A.3.d, IX.A.3.g.

[439] *See supra* Sections IX.A.3.e, IX.A.3.h.

[440] *See supra* Sections IX.A.3.f, IX.A.3.i.

l. Claim Element [12.11]: Interlayer Dielectric

387. Claim 12 recites "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region." The asserted combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.9].[441]

m. Claim Element [12.12]: First Germanide Layer

388. Claim 12 recites "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium." Subject to the same caveats about how "germanide layer" is construed and how the phrase "in the first opening and over the portion" is applied, at least one of the alleged combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.10].[442]

n. Claim Element [12.13]: Second Germanide Layer

389. Claim 12 recites "a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium." Subject to the same caveats about

[441] *See supra* Section IX.A.3.j.

[442] *See supra* Section IX.A.3.k.

how "germanide layer" is construed and how the phrase "in the first opening and over the portion" is applied, at least one of the alleged combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.11].[443]

o. Claim Element [12.14]: First Contact Plug

390. Claim 12 recites "a first contact plug in the first opening and on the first germanide layer." Subject to the same caveats about how "germanide layer" is construed, at least one of the alleged combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.12].[444]

p. Claim Element [12.15]: Second Contact Plug

391. Claim 12 recites "a second contact plug in the second opening and on the second germanide layer." Subject to the same caveats about how "germanide layer" is construed, at least one of the alleged combinations of *Ranade* and *Kim* include this feature for the same reasons I provide for claim element [1.13].[445]

q. A Person of Ordinary Skill in the Art Would Have Found Claim 12 Obvious

392. Because a person of ordinary skill in the art would have been motivated to make the combinations of *Ranade* and *Kim* described above, because he or she would have reasonably expected to succeed in doing so, and because at

[443] *See supra* Sections IX.A.3.k, IX.A.3.l.

[444] *See supra* Section IX.A.3.m.

[445] *See supra* Sections IX.A.3.m, IX.A.3.n.

least one of those combinations satisfies each element of claim 12,[446] it is my opinion that claim 12 would have been obvious.

9. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 13 Obvious

393. Claim 13 depends from claim 12. I understand that means claim 13 requires all the same features as claim 12, plus the additional features recited in claim 13. At least one of the asserted combinations of *Ranade* and *Kim* includes all the features recited in claim 12 for the reasons I provide in Sections IX.A.8.a-p above.

394. Claim 13 further recites "a memory coupled to the board." The asserted combinations of *Ranade* and *Kim* both suggest "a memory coupled to the board."

395. The asserted combinations of *Ranade* and *Kim* are both components of "an integrated circuit device."[447] As I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s

[446] There may be differences between the First Obvious Modification (Ge Overlayer Metalization) and Second Obvious Modification (Direct Metalization) depending on the construction of "germanide layer." *See, e.g., supra* Section IX.A.3.k.

[447] *See, e.g., Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

teachings) into smartphones, computers, and other typical consumer electronic devices.

396. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[448] A person of ordinary skill in the art further would have understood that such chips are combined with other electronic circuit elements, including memory, onto a circuit board for use in computing devices. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in chips that go onto circuit boards and exchange information with a memory.

397. Because at least one of the asserted the combinations of *Ranade* and *Kim* teaches every feature recited in claim 13 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 13 would have been obvious.

[448] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

10. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 14 Obvious

398. Claim 14 depends from claim 12. I understand that means claim 14 requires all the same features as claim 12, plus the additional features recited in claim 14. At least one of the asserted combinations of *Ranade* and *Kim* includes all the features recited in claim 12 for the reasons I provide in Sections IX.A.8.a-p above.

399. Claim 14 further recites "a communication chip coupled to the board." The asserted combinations of *Ranade* and *Kim* both suggest "a communication chip coupled to the board."

400. The asserted combinations of *Ranade* and *Kim* both components of "an integrated circuit device."[449] As I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

401. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of

[449] *See, e.g.*, *Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

integrated circuits, which, after they are packaged, are called "chips."[450] A person of ordinary skill in the art also would have understood that such chips are used in smartphones and computers, for example, which contain circuit boards with at least one communication chip. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits, including communication chips, that go onto circuit boards in smartphones and computers.

402. Because at least one of the asserted combinations of *Ranade* and *Kim* teaches every feature recited in claim 14 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 14 would have been obvious.

11. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 15 Obvious

403. Claim 15 depends from claim 12. I understand that means claim 15 requires all the same features as claim 12, plus the additional features recited in claim 15. At least one of the asserted combinations of *Ranade* and *Kim* includes all

[450] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

the features recited in claim 12 for the reasons I provide in Sections IX.A.8.a-p above.

404. Claim 15 further recites "a camera coupled to the board." The asserted combinations of *Ranade* and *Kim* both suggest "a camera coupled to the board."

405. The asserted combinations of *Ranade* and *Kim* are both components of "an integrated circuit device."[451] As I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

406. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[452] A person of ordinary skill in the art further would have understood that such chips are used in smartphones and computers, for example, which contain a camera coupled to the circuit board. A person of ordinary skill in the art would have understood that

[451] *See, e.g.*, *Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

[452] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a camera.

407. Because at least one of the asserted combinations of *Ranade* and *Kim* teaches every feature recited in claim 15 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 15 would have been obvious.

12. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 16 Obvious

408. Claim 16 depends from claim 12. I understand that means claim 16 requires all the same features as claim 12, plus the additional features recited in claim 16. At least one of the asserted combinations of *Ranade* and *Kim* includes all the features recited in claim 12 for the reasons I provide in Sections IX.A.8.a-p above.

409. Claim 16 further recites "a battery coupled to the board." The asserted combinations of *Ranade* and *Kim* both suggest "a battery coupled to the board."

410. The asserted combinations of *Ranade* and *Kim* are both components of "an integrated circuit device."[453] As I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

411. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[454] A person of ordinary skill in the art further would have understood that such chips are used in smartphones and computers, for example, which contain a battery coupled to the circuit board. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade* and *Kim* are both FET

[453] *See, e.g.*, *Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

[454] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

structures designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a battery.

412. Because at least one of the asserted combinations of *Ranade* and *Kim* teaches every feature recited in claim 16 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 16 would have been obvious.

13. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 17 Obvious

413. Claim 17 depends from claim 12. I understand that means claim 17 requires all the same features as claim 12, plus the additional features recited in claim 17. At least one of the asserted combinations of *Ranade* and *Kim* includes all the features recited in claim 12 for the reasons I provide in Sections IX.A.8.a-p above.

414. Claim 17 further recites "an antenna coupled to the board." The asserted combinations of *Ranade* and *Kim* both suggest "an antenna coupled to the board."

415. The asserted combinations of *Ranade* and *Kim* are both components of "an integrated circuit device."[455] As I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor

[455] *See, e.g.*, *Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

416. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[456] A person of ordinary skill in the art further would have understood that such chips are used in smartphones and computers, for example, which contain an antenna coupled to the circuit board. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to an antenna.

417. Because at least one of the asserted combinations of *Ranade* and *Kim* teaches every feature recited in claim 17 and a person of ordinary skill in the art

[456] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

would have found it obvious to combine their teachings, it is my opinion that claim 17 would have been obvious.

14. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 18 Obvious

418. Claim 18 depends from claim 12. I understand that means claim 18 requires all the same features as claim 12, plus the additional features recited in claim 18. At least one of the asserted combinations of *Ranade* and *Kim* includes all the features recited in claim 12 for the reasons I provide in Sections IX.A.8.a-p above.

419. Claim 18 further recites "wherein the component is a packaged integrated circuit die." As I explain in Section IX.A.8.c for claim element [12.2], the asserted combinations of *Ranade* and *Kim* both suggest "a component coupled to the board, the component including an integrated circuit structure." The asserted combinations of *Ranade* and *Kim* also both suggest "the component is a packaged integrated circuit die."

420. The asserted combinations of *Ranade* and *Kim* are both components of "an integrated circuit device."[457] As I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ

[457] *See, e.g.*, *Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

421. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[458] A person of ordinary skill in the art further would have understood such chips are packaged to be combined with other electronic circuit elements onto a circuit board for use in consumer electronic devices. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. Moreover, a person of ordinary skill in the art would have understood that unpackaged integrated circuits (i.e., processed wafers and unpackaged dies) are used only for testing or to be packaged into integrated circuits. In short, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits that go onto circuit boards as packaged integrated circuit dies.

[458] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

422. Because at least one of the asserted combinations of *Ranade* and *Kim* teaches every feature recited in claim 18 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 18 would have been obvious.

15. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 19 Obvious

423. Claim 19 depends from claim 12. I understand that means claim 19 requires all the same features as claim 12, plus the additional features recited in claim 19. At least one of the asserted combinations of *Ranade* and *Kim* includes all the features recited in claim 12 for the reasons I provide in Sections IX.A.8.a-p above.

424. Claim 19 further recites "wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor." As I explain in Section IX.A.8.c for claim element [12.2], a person of ordinary skill in the art would have understood the asserted combinations of *Ranade* and *Kim* both suggest a "component including an integrated circuit structure." The asserted combinations of *Ranade* and *Kim* also both suggest "the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor."

425. The asserted combinations of *Ranade* and *Kim* are both components of "an integrated circuit device."[459] As I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

426. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[460] A person of ordinary skill in the art further would have understood that such chips, including processors, communications chips, and digital signal processors (DSPs), are coupled to the circuit boards of smartphones and computers. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combinations of

[459] *See, e.g.*, *Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

[460] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

Ranade and *Kim* are both FET structures designed for use in integrated circuits, including processors, communications chips, and digital signal processors (DSPs), that go onto circuit boards of smartphones, computers, and the like.

427. Because at least one of the asserted combinations of *Ranade* and *Kim* teaches every feature recited in claim 19 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 19 would have been obvious.

16. The Combination of *Ranade* and *Kim* Would Have Rendered Claim 20 Obvious

428. Claim 20 depends from claim 12. I understand that means claim 20 requires all the same features as claim 12, plus the additional features recited in claim 20. At least one of the asserted combinations of *Ranade* and *Kim* includes all the features recited in claim 12 for the reasons I provide in Sections IX.A.8.a-p above.

429. Claim 20 further recites "wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box." The asserted combinations of *Ranade* and *Kim* both suggest "wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box."

430. The asserted combinations of *Ranade* and *Kim* are both components of "an integrated circuit device."[461] As I explain in Section IX.A.2, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Ranade*'s and *Kim*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

431. A person of ordinary skill in the art would have understood that FET devices like those described in *Ranade* and *Kim* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[462] A person of ordinary skill in the art further would have understood that such chips are coupled to the circuit boards of smartphones, computers, and other consumer electronic devices. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade* and *Kim* are both FET

[461] *See, e.g.*, *Ranade* ¶¶ [0025], [0043], [0046]; *Kim* ¶ [0005], [0049].

[462] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

structures designed for use in integrated circuits that go onto the circuit boards of smartphones, laptops, desktop computers, servers, set-top boxes, and the like.

432. Because at least one of the asserted combinations of *Ranade* and *Kim* teaches every feature recited in claim 20 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 20 would have been obvious.

B. Ground 1B: The Combination of *Ranade*, *Kim*, and *Liu* Would Have Rendered Claims 12-20 Obvious

1. A Person of Ordinary Skill in the Art Would Have Found the Combination of *Ranade*, *Kim*, and *Liu* Obvious

433. As I explain in Section IX.A, *Ranade* teaches FinFET devices, and a person of ordinary skill in the art would have found it obvious to implement *Ranade*'s FinFET devices according to the teachings of *Kim*. A person of ordinary skill in the art also would have found it obvious to employ FinFET devices like the ones *Ranade* teaches (including as implemented according to the teachings of *Kim* as described above) into smartphones, computers, and other consumer electronic devices. Doing so not only would have been obvious in view of references like *Liu*, but also based on common sense and basic knowledge about how FinFET devices and other MOSFETs are used. A person of ordinary skill in the art would have understood that smartphones, computers, and other consumer electronic devices

were (and still are), by far, the primary applications for chips made up of such transistors.

434. *Liu* teaches various FET processes and structures, including FinFETs.[463] *Liu* also explains that such "[f]ield effect transistors (FETs) are widely used in the electronics industry for switching, amplification, filtering, and other tasks related to both analog and digital electrical signals."[464] *Liu* teaches in particular that improved FETs may help address the following problem: "[W]ireless mobile product technology continues to demand more applications performance, less power drain on batteries, and lower integrated circuit cost of manufacture."[465]

435. In a section titled "Improved Integrated Circuits and Systems," *Liu* describes exemplary systems in which FETs, including FinFETs, may be used.[466] As *Liu*'s Figures 10 and 11 below illustrate, a person of ordinary skill in the art would have understood that FETs, including FinFETs, are to be employed in consumer electronics, including in smartphones, computers, and the like.[467] Figure 10 below illustrates a cell phone system that includes a printed circuit

[463] *See Liu* at 32:22-40, Fig. 8.

[464] *Id.* at 1:47-50.

[465] *Id.* at 1:29-32.

[466] *See id.* at 33:10-37:40, Figs. 10, 11.

[467] *See id.* at Figs. 10, 11.

board, and Figure 11 below illustrates the integrated circuits and other components that would be coupled to such a printed circuit board[468]:

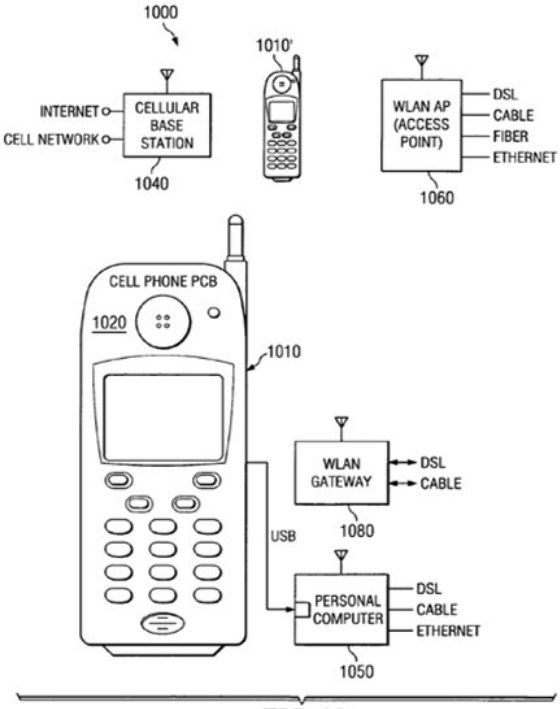


FIG. 10

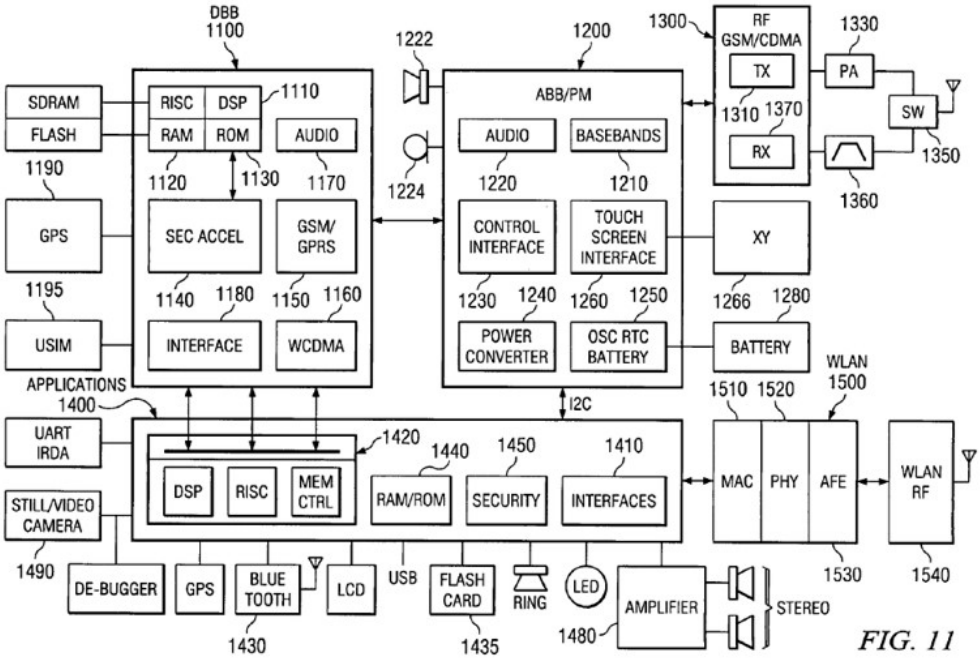


FIG. 11

[468] *See id.* at 33:12-15, 33:62-63.

436. Referring to Figure 10, *Liu* explains: "On a cell phone printed circuit board (PCB) 1020 in handset 1010, there is provided a processor integrated circuit 1022, an external flash memory 1024, and a serial interface 1026."[469] *Liu* further explains that Figure 11 illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[470] The integrated circuits in Figure 11 include various processors, memory, wireless communications chips, a camera interface, GPS circuitry, a battery, various antennas, and more.[471] A person of ordinary skill in the art would have understood that such systems were typical by December 2010. To provide a frame of reference for the types of features and peripherals in use at the time, the iPhone 4 was released on June 24, 2010.[472]

437. To a person of ordinary skill in the art, implementing FinFETs into computing devices like those described in *Liu* would have been obvious according to at least four of the various obviousness rationales I have been asked to consider.

438. First, a person of ordinary skill in the art would have considered implementing FinFETs into computing devices like those described in *Liu* to be example of combining prior art elements according to known methods to yield

[469] *Id.* at 33:50-53; *see also id.* at 33:54-34:22.

[470] *Id.* at 33:62-63.

[471] *Id.* at 34:23-37:40.

[472] *See* https://www.apple.com/newsroom/2010/06/07Apple-Presents-iPhone-4.

predictable results. Both FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) and typical integrated circuits used in consumer electronic devices like *Liu*'s were prior art elements known to a person of ordinary skill in the art by December 2010. Combining them would have required nothing more than well-known methods.[473] Additionally, a person of ordinary skill in the art would have understood that deploying FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in the integrated circuits of *Liu*'s cell phone system would yield a predictable result—namely, a cell phone system like the one *Liu* describes.

439. Second, a person of ordinary skill in the art would have considered implementing FinFETs into computing devices like those described in *Liu* to be an example of using a known technique to improve similar devices in the same way. A person of ordinary skill in the art would have known techniques for incorporating FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) into integrated circuits using known methods.[474] And a person of ordinary skill in the art would have understood that doing so would improve the

[473] *Ranade* itself confirms that its "tri-gate MOS-FET may be incorporated into an integrated circuit by conventional processing steps, as known in the art." *Ranade* ¶ [0046].

[474] *Id.*

integrated circuits in *Liu*'s cell phone system by virtue of using *Ranade*'s FinFET structure as implemented according to *Kim*'s teachings.

440. Third, a person of ordinary skill in the art would have considered implementing FinFETs into computing devices like those described in *Liu* to be an example of applying a known technique (e.g., integrating FinFETs into integrated circuits[475]) to a known device (e.g., the integrated circuits in *Liu*'s cell phone system) ready for improvement. A person of ordinary skill in the art would have recognized several potential improvements to *Liu*'s integrated circuits by incorporating FinFETs like the ones resulting from the asserted combinations of *Ranade* and *Kim*, such as faster switching speeds and less power consumption and heating due to reduced source/drain contact resistance.

441. Fourth, a person of ordinary skill in the art would have implemented FinFETs into computing devices like those described in *Liu* due to a teaching, suggestion, or motivation in the prior art to arrive at the claimed invention. A person of ordinary skill in the art would have been familiar with several teachings, suggestions, and motivations in the prior art, including those provided in *Ranade*, *Kim*, and *Liu* themselves.[476] A person of ordinary skill in the art, being well

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[475] *Id.*

[476] *See, e.g.*, *Ranade* ¶¶ [0010], [0012], [0025], [0040], [0043], [0046], Figs. 2N, 3C; *Kim* ¶¶ [0003]-[0007], [0010], [0047], [0050], [0071], [0074], Figs. 1F, 2D, 3F, 4, 5; *Liu* at 1:29-6:10, 32:23-40, 33:11-37:59, Figs. 8, 10, 11.

acquainted with the ongoing pursuit of semiconductor scaling and Moore's Law, would have been motivated to incorporate FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) into the integrated circuits of *Liu*'s cell phone system. *Liu* itself even recognizes that such FinFETs may be used.[477] By incorporating FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) into computing devices like those described in *Liu*, a person of ordinary skill in the art would have arrived at a combination in which *Liu*'s cell phone system includes integrated circuits made up of FinFETs like the ones resulting from the asserted combinations of *Ranade* and *Kim*.

442. Regardless of the rationale a person of ordinary skill in the art would have applied, he or she would have found it obvious to deploy FinFETs like the ones resulting from the asserted combinations of *Ranade* and *Kim* in the integrated circuits of a system like the one *Liu* describes.

2. The Combination of *Ranade, Kim,* and *Liu* Would Have Rendered Claim 12 Obvious

a. Claim Element [12.0]: The Preamble

443. Claim 12 recites "[a] computing device." The asserted combinations of *Ranade*, *Kim*, and *Liu* teach "a computing device."

[477] *See Liu* at 32:23-40, Fig. 8.

444. As I explain in Section IX.A.8.a, a person of ordinary skill in the art would have understood the FinFET described by the combinations of *Ranade* and *Kim* would go into "[a] computing device." Although a person of ordinary skill in the art would have found this sufficient to satisfy claim element [12.0], *Liu*'s teachings make it explicit.

445. *Liu* teaches "a computing device." For example, *Liu* describes a "wireless handset," shown below, with FinFET-based integrated circuits.[478]

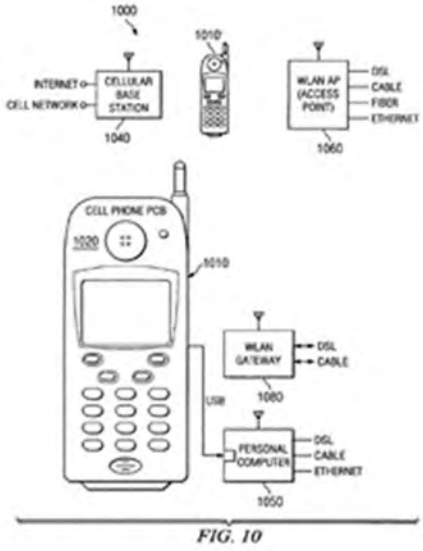


FIG. 10

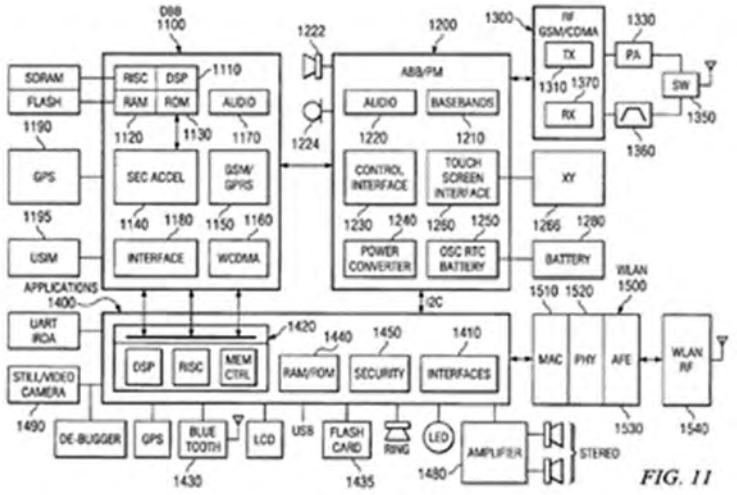


FIG. 11

446. *Liu* also describes other electronic devices that incorporate integrated circuits, including "radios and televisions, fixed and portable entertainment units, routers, pagers, personal digital assistants (PDA), organizers, scanners, faxes, copiers, household appliances, [and] office appliances."[479]

[478] *See Liu* at 6:45-51, 32:23-40, 33:11-37:59, Figs. 8, 10, 11.

[479] *Id.* at 34:3-22.

447. Because *Liu* teaches a "computing device," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in the integrated circuits of *Liu*'s "computing device," a person of ordinary skill in the art would have understood the *Ranade-Kim-Liu* combination includes "[a] computing device" as claimed.

b. Claim Element [12.1]: A Board

448. Claim 12 recites "a board." The asserted combinations of *Ranade*, *Kim*, and *Liu* teach "a board."

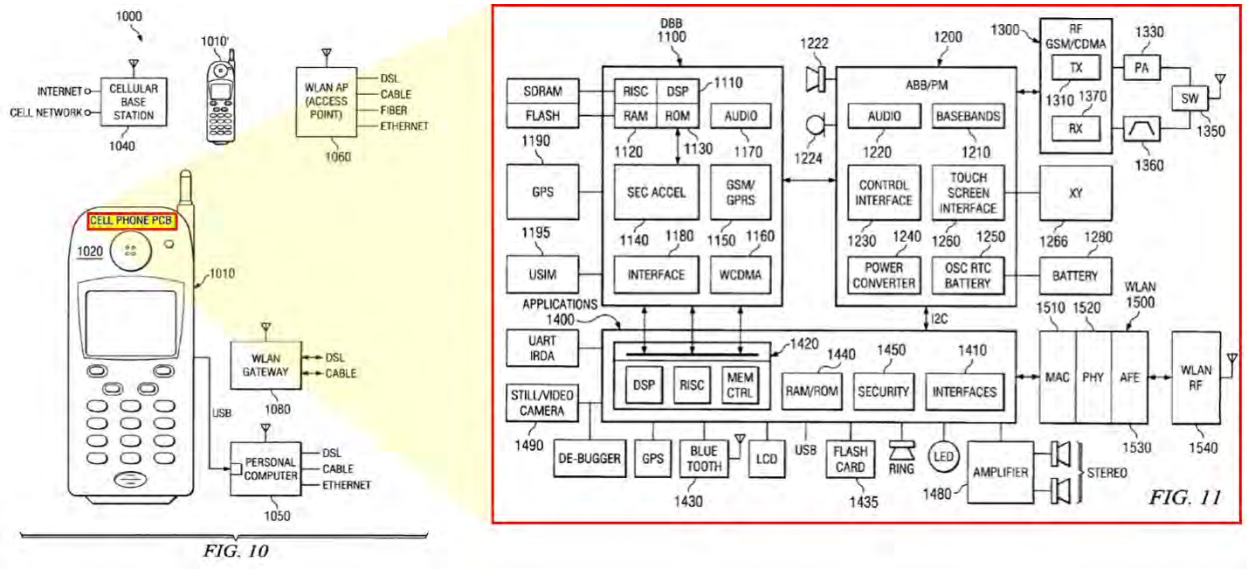
449. As I explain in Section IX.A.8.b, a person of ordinary skill in the art would have understood the FinFET described by the combination of *Ranade* and *Kim* would go into a semiconductor chip that gets incorporated into "a board." Although a person of ordinary skill in the art would have found this sufficient to satisfy claim element [12.1], *Liu*'s teachings make it explicit.

450. *Liu* teaches "a board." For example, *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[480] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[481] "For

[480] *Id.* at 33:46-61.

[481] *Id.* at 33:62-63.

conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[482] I annotated the figures below to show this relationship.



451. Because *Liu* teaches a "a board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in the integrated circuits found on *Liu*'s circuit board, a person of ordinary skill in the art would have understood the *Ranade-Kim-Liu* combination includes "a board" as claimed.

c. Claim Element [12.2]: Integrated Circuit Structure

452. Claim 12 recites "a component coupled to the board, the component including an integrated circuit structure." The asserted combinations of *Ranade*,

[482] *Id.* at 33:66-34:2.

Kim, and *Liu* teach "a component coupled to the board, the component including an integrated circuit structure."

453. As I explain in Section IX.A.8.c, a person of ordinary skill in the art would have understood the FinFET described by the combination of *Ranade* and *Kim* would go into "a component coupled to the board, the component including an integrated circuit structure." Although a person of ordinary skill in the art would have found this sufficient to satisfy claim element [12.2], *Liu*'s teachings make it explicit.

454. *Liu* teaches components (i.e., integrated circuits) coupled to the board that include integrated circuit structures. For example, *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[483] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[484] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[485] Those integrated circuits include a digital baseband chip 1100 (green below), an analog baseband chip 1200 (blue below), a GSM chip 1300 (red

[483] *Id.* at 33:46-61.

[484] *Id.* at 33:62-63.

[485] *Id.* at 33:66-34:2.

below), an applications processor chip 1400 (purple below), and a WLAN chip 1500 (orange below).[486] According to *Liu*, these are "integrated circuits made by any of the improved processes and including the improved transistors illustrated in the other Figures," which includes FinFET structures.[487]

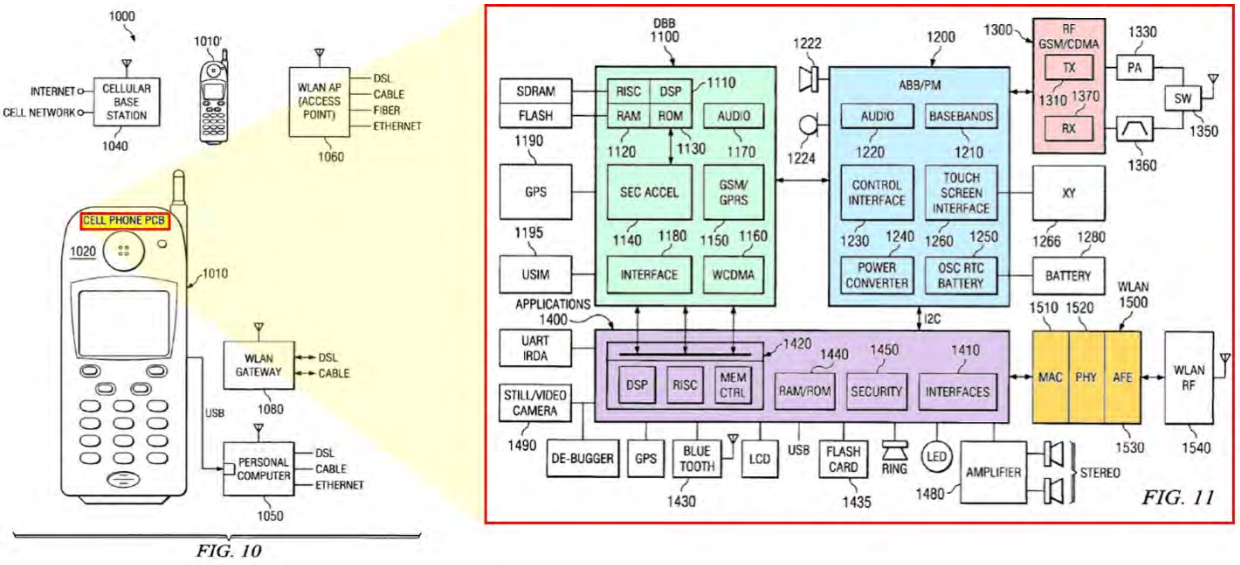


FIG. 10

FIG. 11

455. Because *Liu* teaches integrated circuits coupled to a circuit board and those integrated circuits include FinFET structures, and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in those integrated circuits, a person of ordinary skill in the art would have understood the *Ranade-Kim-Liu* combination includes "a component coupled to the board, the component including an integrated circuit structure" as claimed.

[486] *See id.* at 34:23-30, 35:14-20, 35:64-67, 36:15-16, 37:14-17.

[487] *Id.* at 6:48-51; *see also id.* at 32:23-40, Fig. 8.

d. Claim Element [12.3]: Fin

456. Claim 12 recites "a fin comprising silicon." The asserted combinations of *Ranade*, *Kim*, and *Liu* include this feature for the same reasons I provide for claim element [1.1].[488]

e. Claim Element [12.4]: Gate Electrode

457. Claim 12 recites "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side." The asserted combinations of *Ranade*, *Kim*, and *Liu* include this feature for the same reasons I provide for claim element [1.2].[489]

f. Claim Element [12.5]: First Dielectric Spacer

458. Claim 12 recites "a first dielectric spacer along the first side of the gate electrode." The asserted combinations *Ranade*, *Kim*, and *Liu* include this feature for the same reasons I provide for claim element [1.3].[490]

g. Claim Element [12.6]: First Source or Drain Region

459. Claim 12 recites "a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath

[488] *See supra* Section IX.A.3.b.

[489] *See supra* Section IX.A.3.c.

[490] *See supra* Section IX.A.3.d.

the first dielectric spacer." The asserted combinations of *Ranade, Kim,* and *Liu* include this feature for the same reasons I provide for claim element [1.4].[491]

h. Claim Element [12.7]: Graded Germanium Concentration of the First Source or Drain Region

460. Claim 12 recites "wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combinations of *Ranade, Kim,* and *Liu* include this feature for the same reasons I provide for claim element [1.5].[492]

i. Claim Element [12.8]: Second Dielectric Spacer

461. Claim 12 recites "a second dielectric spacer along the second side of the gate electrode." The asserted combinations of *Ranade*, *Kim*, and *Liu* include this feature for the same reasons I provide for claim element [1.6].[493]

j. Claim Element [12.9]: Second Source or Drain Region

462. Claim 12 recites "a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer." The asserted combinations of *Ranade, Kim*, and *Liu* include this feature for the same reasons I provide for element [1.7].[494]

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[491] *See supra* Section IX.A.3.e.

[492] *See supra* Section IX.A.3.f.

[493] *See supra* Sections IX.A.3.d, IX.A.3.g.

[494] *See supra* Sections IX.A.3.e, IX.A.3.h.

k. Claim Element [12.10]: Graded Germanium Concentration of the Second Source or Drain Region

463. Claim 12 recites "wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combinations of *Ranade*, *Kim*, and *Liu* include this feature for the same reasons I provide for claim element [1.8].[495]

l. Claim Element [12.11]: Interlayer Dielectric

464. Claim 12 recites "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region." The asserted combinations of *Ranade*, *Kim*, and *Liu* include this feature for the same reasons I provide for claim element [1.9].[496]

m. Claim Element [12.12]: First Germanide Layer

465. Claim 11 recites "a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium." Subject to the caveats regarding the construction of "germanide layer" discussed in Section IX.A.3.k, at least one of the asserted

[495] *See supra* Sections IX.A.3.f, IX.A.3.i.

[496] *See supra* Section IX.A.3.j.

combinations of *Ranade*, *Kim*, and *Liu* includes this feature for the same reasons I provide for claim element [1.5].[497]

n. Claim Element [12.13]: Second Germanide Layer

466. Claim 12 recites "a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium." Subject to the caveats regarding the construction of "germanide layer" discussed in Section IX.A.3.k, at least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* includes this feature for the same reasons I provide for claim element [1.11].[498]

o. Claim Element [12.14]: First Contact Plug

467. Claim 12 recites "a first contact plug in the first opening and on the first germanide layer." Subject to the caveats regarding the construction of "germanide layer" discussed in Section IX.A.3.k, at least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* includes this feature for the same reasons I provide for claim element [1.12].[499]

[497] *See supra* Section IX.A.3.k.

[498] *See supra* Sections IX.A.3.k, IX.A.3.l.

[499] *See supra* Section IX.A.3.m.

p. Claim Element [12.15]: Second Contact Plug

468. Claim 12 recites "a second contact plug in the second opening and on the second germanide layer." Subject to the caveats regarding the construction of "germanide layer" discussed in Section IX.A.3.k, at least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* includes this feature for the same reasons I provide for claim element [1.13].[500]

q. A Person of Ordinary Skill in the Art Would Have Found Claim 12 Obvious

469. Because a person of ordinary skill in the art would have been motivated to make the combinations of *Ranade*, *Kim*, and *Liu* described above, because he or she would have reasonably expected to succeed in doing so, and because at least one of those combinations satisfies each element of claim 12,[501] it is my opinion that claim 12 would have been obvious.

3. The Combination of *Ranade*, *Kim*, and *Liu* Would Have Rendered Claim 13 Obvious

470. Claim 13 depends from claim 12. I understand that means claim 13 requires all the same features as claim 12, plus the additional features recited in

[500] *See supra* Sections IX.A.3.m, IX.A.3.n.

[501] There may be differences between the First Obvious Modification (Ge Overlayer Metalization) and Second Obvious Modification (Direct Metalization) depending on the construction of "germanide layer." *See, e.g., supra* Section IX.A.3.k.

claim 13. At least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.B.2.a-p above.

471. Claim 13 further recites "a memory coupled to the board." The asserted combinations of *Ranade*, *Kim*, and *Liu* teach "a memory coupled to the board."

472. As I explain in Section IX.A.9, a person of ordinary skill in the art would have understood the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in chips that go onto circuit boards and exchange information with a memory. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 13, *Liu*'s teachings make it explicit.

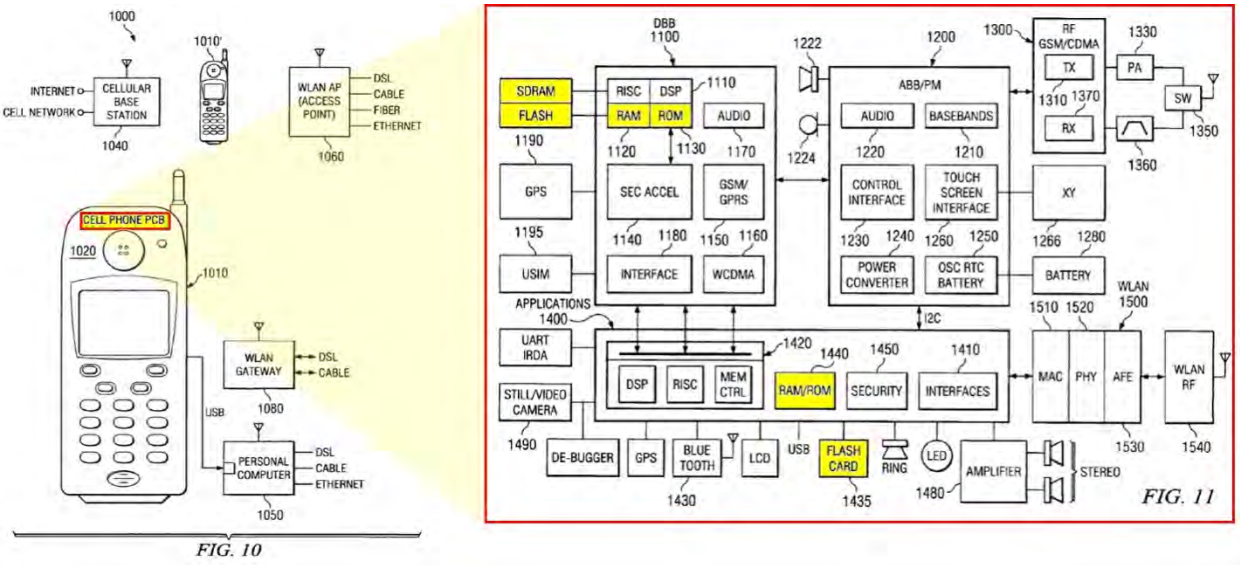
473. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[502] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[503] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[504] Coupled to the

[502] *Id.* at 33:46-61.

[503] *Id.* at 33:62-63.

[504] *Id.* at 33:66-34:2.

printed circuit board are various memories, highlighted in yellow below, including "off-chip Flash memory and SDRAM (synchronous dynamic random access memory)," "[o]n chip RAM 1120 and on-chip ROM 1130," "off-chip memory resources 1435 including as appropriate, mobile DDR (double data rate) DRAM, and flash memory of any of NAND Flash, NOR Flash, and Compact Flash," and "on-chip memory 1440 with RAM and ROM," which includes "frame buffer internal SRAM (static random access memory) in memory area 1440."[505]



474. Because *Liu* teaches a "computing device" that includes "a memory coupled to the board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in the integrated circuits found on the circuit

[505] *Id.* at 34:28-33, 36:24-33.

board of *Liu*'s computing device, a person of ordinary skill in the art would have understood the asserted combinations of *Ranade, Kim,* and *Liu* teach "a memory coupled to the board."

475. Because at least one of the asserted combinations of *Ranade*, *Kim,* and *Liu* teaches every feature recited in claim 13 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 13 would have been obvious.

4. The Combination of *Ranade, Kim,* and *Liu* Would Have Rendered Claim 14 Obvious

476. Claim 14 depends from claim 12. I understand that means claim 14 requires all the same features as claim 12, plus the additional features recited in claim 14. At least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.B.2.a-p above.

477. Claim 14 further recites "a communication chip coupled to the board." The asserted combinations of *Ranade*, *Kim,* and *Liu* teach "a communication chip coupled to the board."

478. As I explain in Section IX.A.10, a person of ordinary skill in the art would have understood the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits, including communication chips, that go onto circuit boards in smartphones and computers. Although a

person of ordinary skill in the art would have found this sufficient to satisfy claim 14, *Liu*'s teachings make it explicit.

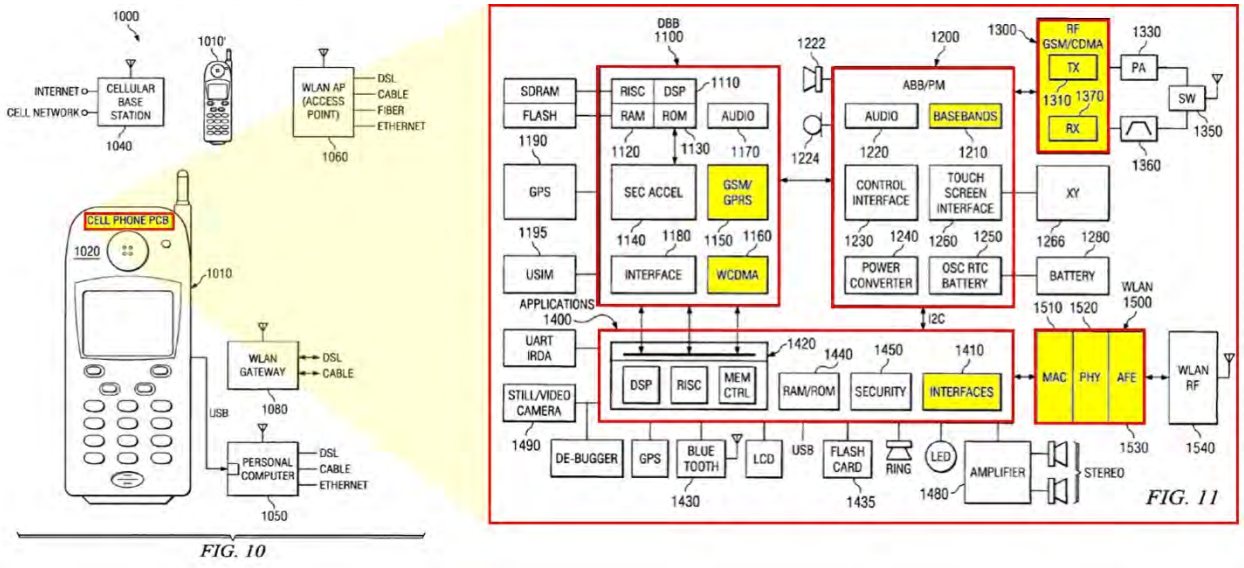
479. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[506] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[507] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[508] Coupled to the printed circuit board are various communications chips, including (1) "integrated circuit 1100," which "supports and provides interfaces for one or more of GSM, GPRS, EDGE, and UMTS (Global System for Mobile communications, General Packet Radio Service, Enhanced Data Rates for Global Evolution, Universal Mobile Telecommunications System) wireless," (2) "mixed-signal integrated circuit 1200," which "includes an analog baseband (ABB) block 1210 for GSM/GPRS/EDGE/UMTS," (3) "integrated circuit 1300," which "includes a GSM/GPRS/EDGE/UMTS RF transmitter block 1310," (4) "integrated circuit chip 1400," which includes "WLAN 802.11a/b/g interface circuit 1410 coupled to a

[506] *Id.* at 33:46-61.

[507] *Id.* at 33:62-63.

[508] *Id.* at 33:66-34:2.

WLAN chip 1500," and (5) "a WLAN integrated circuit 1500," which "includes MAC (media access controller) 1510, PHY (physical layer) 1520 and AFE (analog front end) 1530" and "is coupled by receive (RX), transmit (Tx) and CONTROL lines to an off-chip WLAN RF circuitry 1540."[509] I have highlighted the most relevant functional blocks in Figure 11 below.



480. Because *Liu* teaches a "communication chip coupled to the board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in the integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted

[509] *Id.* at 34:33-42, 35:14-20, 35:64-36:36, 37:14-36.

combinations of *Ranade*, *Kim*, and *Liu* teach "a communication chip coupled to the board."

481. Because at least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* teaches every feature recited in claim 14 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 14 would have been obvious.

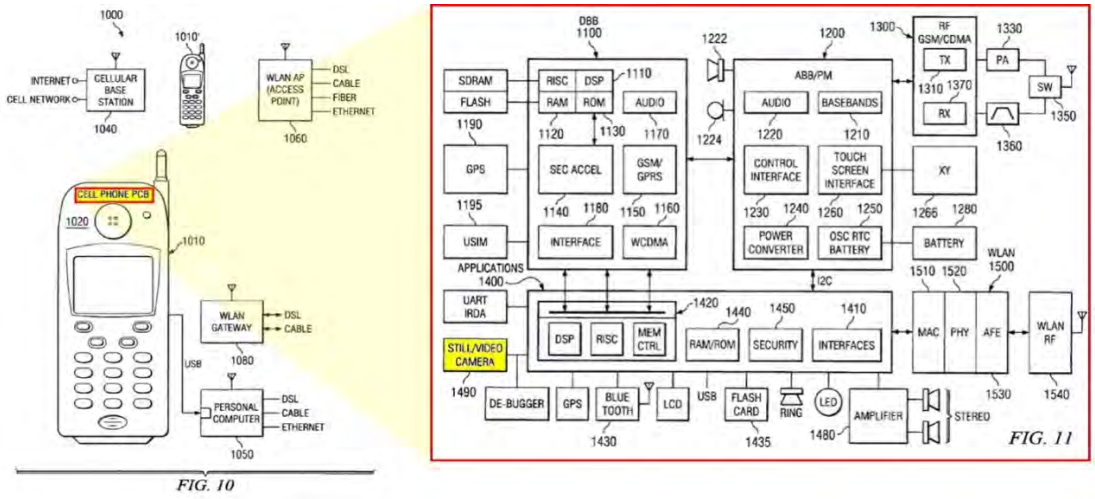
5. The Combination of *Ranade*, *Kim*, and *Liu* Would Have Rendered Claim 15 Obvious

482. Claim 15 depends from claim 12. I understand that means claim 15 requires all the same features as claim 12, plus the additional features recited in claim 15. At least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.B.2.a-p above.

483. Claim 15 further recites "a camera coupled to the board." The asserted combinations of *Ranade*, *Kim*, and *Liu* teach "a camera coupled to the board."

484. As I explain in Section IX.A.11, a person of ordinary skill in the art would have understood the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a camera. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 14, *Liu*'s teachings make it explicit.

485. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[510] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[511] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[512] Coupled to the printed circuit board is a camera, highlighted below in yellow, such as "off-chip still cameras or video cameras 1490" or "a CMOS sensor of radiant energy."[513]



486. Because *Liu* teaches a "camera coupled to the board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in the

[510] *Id.* at 33:46-61.

[511] *Id.* at 33:62-63.

[512] *Id.* at 33:66-34:2.

[513] *Id.* at 36:60-65.

integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade*, *Kim*, and *Liu* teach "camera coupled to the board."

487. Because at least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* has every feature in claim 15 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 15 would have been obvious.

6. The Combination of *Ranade*, *Kim*, and *Liu* Would Have Rendered Claim 16 Obvious

488. Claim 16 depends from claim 12. I understand that means claim 16 requires all the same features as claim 12, plus the additional features recited in claim 16. At least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.B.2.a-p above.

489. Claim 16 further recites "a battery coupled to the board." The asserted combinations of *Ranade*, *Kim*, and *Liu* teach "a battery coupled to the board."

490. As I explain in Section IX.A.12, a person of ordinary skill in the art would have understood the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a battery. Although a person of

ordinary skill in the art would have found this sufficient to satisfy claim 16, *Liu*'s teachings make it explicit.

491. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[514] Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[515] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[516] Coupled to the printed circuit board is "a lithium-ion battery 1280 and backup battery," highlighted below in yellow.[517]

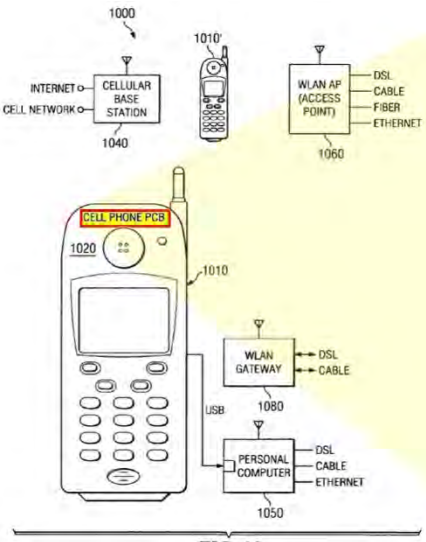


FIG. 10

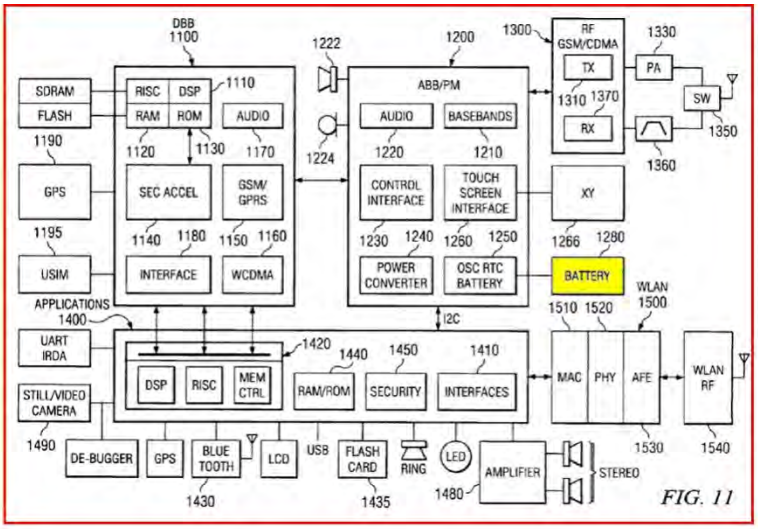


FIG. 11

[514] *Id.* at 33:46-61.

[515] *Id.* at 33:62-63.

[516] *Id.* at 33:66-34:2.

[517] *Id.* at 35:54-63.

492. Because *Liu* teaches a "battery coupled to the board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in the integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade*, *Kim*, and *Liu* teach "battery coupled to the board."

493. Because at least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* has every feature in claim 16 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 16 would have been obvious.

7. The Combination of *Ranade*, *Kim*, and *Liu* Would Have Rendered Claim 17 Obvious

494. Claim 17 depends from claim 12. I understand that means claim 17 requires all the same features as claim 12, plus the additional features recited in claim 17. At least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.B.2.a-p above.

495. Claim 17 further recites "an antenna coupled to the board." The asserted combinations of *Ranade*, *Kim*, and *Liu* teach "an antenna coupled to the board."

496. As I explain in Section IX.A.13, a person of ordinary skill in the art would have understood the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to an antenna. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 17, *Liu*'s teachings make it explicit.

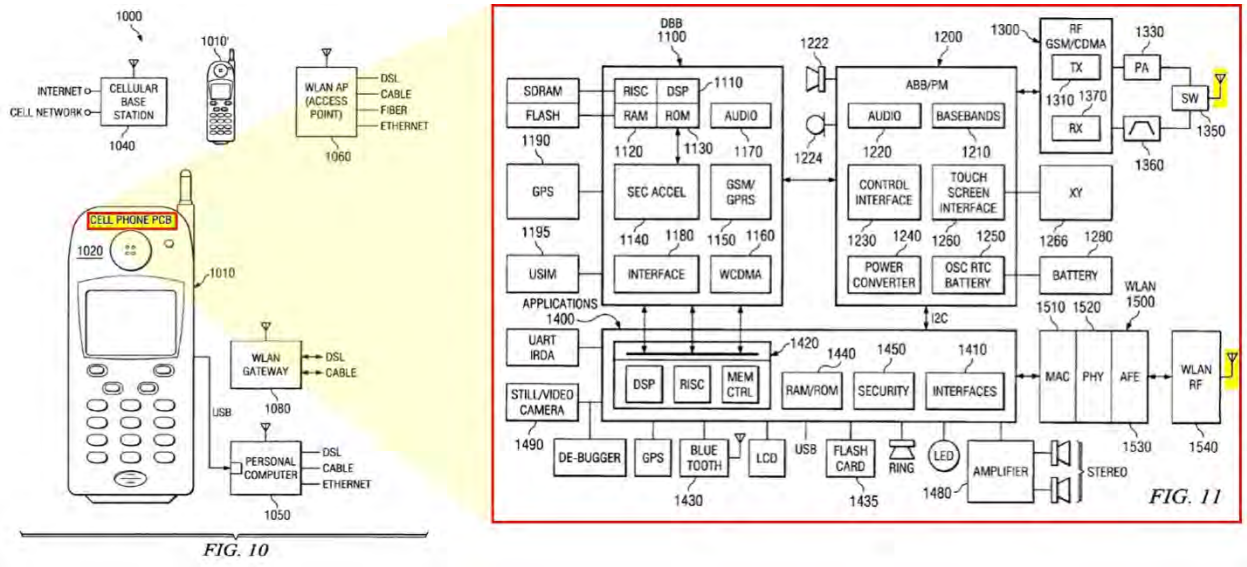


FIG. 10

FIG. 11

497. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 above illustrates.[518] Figure 11 above illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[519] "For conciseness of description," *Liu* explains, "the integrated circuits

[518] *Id.* at 33:46-61.

[519] *Id.* at 33:62-63.

are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[520] Coupled to the printed circuit board is a "wireless antenna" and a "WLAN antenna," both highlighted above in yellow.[521]

498. Because *Liu* teaches "an antenna coupled to the board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in the integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade*, *Kim*, and *Liu* teach "an antenna coupled to the board."

499. Because at least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* has every feature in claim 17 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 17 would have been obvious.

8. The Combination of *Ranade*, *Kim*, and *Liu* Would Have Rendered Claim 18 Obvious

500. Claim 18 depends from claim 12. I understand that means claim 18 requires all the same features as claim 12, plus the additional features recited in claim 18. At least one of the asserted combinations of *Ranade*, *Kim*, and *Liu*

[520] *Id.* at 33:66-34:2.

[521] *Id.* at 36:4-7, 37:26-27; *see also id.* at 5:62-65 (disclosing "a wireless communications device [that] includes an antenna")

includes all the features recited in claim 12 for the reasons I provide in Sections IX.B.2.a-p above.

501. Claim 18 further recites "the component is a packaged integrated circuit die." As I explain above in Section IX.B.2.c, the asserted combinations of *Ranade*, *Kim*, and *Liu* teach "a component coupled to the board, the component including an integrated circuit structure." The asserted combinations of *Ranade*, *Kim*, and *Liu* also teach that "the component is a packaged integrated circuit die."

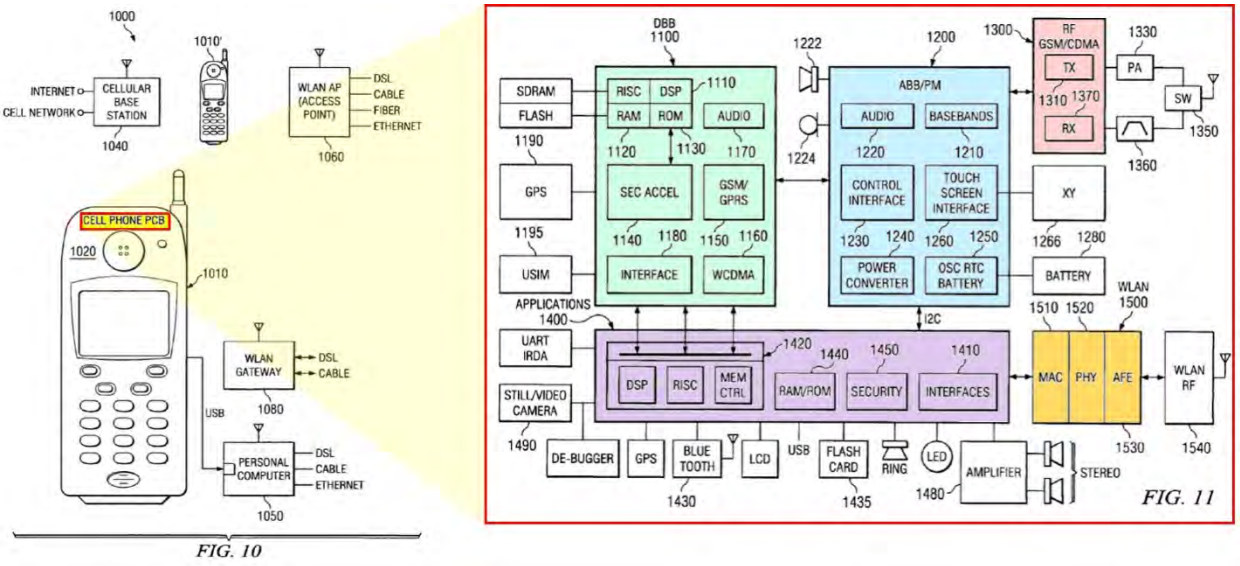
502. As I explain in Section IX.A.14, a person of ordinary skill in the art would have understood the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits that go onto circuit boards as packaged integrated circuit dies. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 18, *Liu*'s teachings make it explicit.

503. *Liu* teaches components (i.e., integrated circuits) coupled to the board that include integrated circuit structures. For example, *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[522] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[523] "For

[522] *Id.* at 33:46-61.

[523] *Id.* at 33:62-63.

conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[524] Those integrated circuits include a digital baseband chip 1100 (green below), an analog baseband chip 1200 (blue below), a GSM chip 1300 (red below), an applications processor chip 1400 (purple below), and a WLAN chip 1500 (orange below).[525] According to *Liu*, these are "integrated circuits made by any of the improved processes and including the improved transistors illustrated in the other Figures," which includes FinFET structures.[526]



[524] *Id.* at 33:66-34:2.

[525] *See id.* at 34:23-30, 35:14-20, 35:64-67, 36:15-16, 37:14-17.

[526] *Id.* at 6:48-51; *see also id.* at 32:23-40, Fig. 8.

504. A person of ordinary skill in the art would have understood that these integrated circuits are packaged dies (specifically, individually packaged chips, chiplets within a single package, or a combination thereof) because unpackaged integrated circuits (i.e., processed wafers and unpackaged dies) are, unlike these integrated circuits, used only for testing or to be packaged into integrated circuits.

505. Because *Liu* teaches "the component is a packaged integrated circuit die," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in the integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade*, *Kim*, and *Liu* teach "the component is a packaged integrated circuit die."

506. Because at least one of the asserted combinations of *Ranade*, *Kim,* and *Liu* has every feature in claim 18 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 18 would have been obvious.

9. The Combination of *Ranade, Kim,* and *Liu* Would Have Rendered Claim 19 Obvious

507. Claim 19 depends from claim 12. I understand that means claim 19 requires all the same features as claim 12, plus the additional features recited in claim 19. At least one of the asserted combinations of *Ranade*, *Kim,* and *Liu*

includes all the features recited in claim 12 for the reasons I provide in Sections IX.B.2.a-p above.

508. Claim 19 further recites "the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor." As I explain in Section IX.B.2.c, the asserted combinations of *Ranade, Kim*, and *Liu* teach "a component coupled to the board, the component including an integrated circuit structure." And as I explain in Section IX.B.4, the asserted combinations of *Ranade*, *Kim*, and *Liu* teach "a communication chip coupled to the board." The asserted combinations of *Ranade, Kim*, and *Liu* also teach that "the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor."

509. As I explain in Section IX.A.15, a person of ordinary skill in the art would have understood the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits, including processors, communication chips, and digital signal processors (DSPs), that go onto circuit boards of smartphones, computers, and the like. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 19, *Liu*'s teachings make it explicit.

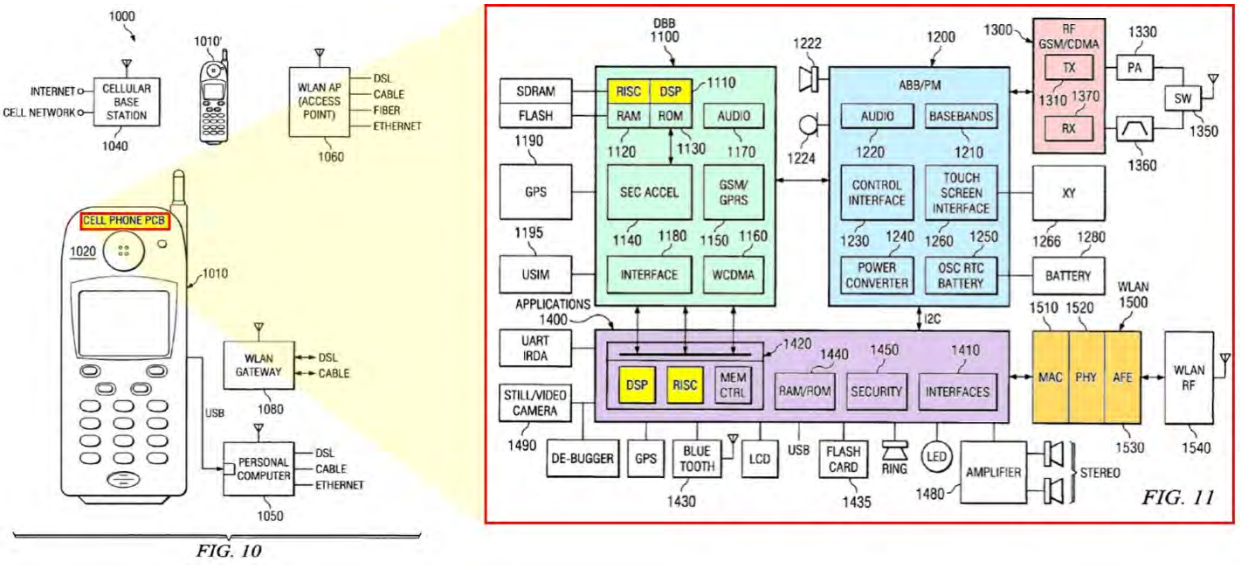
510. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[527] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[528] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[529] Coupled to the printed circuit board are various communications chips, including (1) "integrated circuit 1100" (green below), which "supports and provides interfaces for one or more of GSM, GPRS, EDGE, and UMTS (Global System for Mobile communications, General Packet Radio Service, Enhanced Data Rates for Global Evolution, Universal Mobile Telecommunications System) wireless," (2) "mixed-signal integrated circuit 1200" (blue below), which "includes an analog baseband (ABB) block 1210 for GSM/GPRS/EDGE/UMTS," (3) "integrated circuit 1300" (red below), which "includes a GSM/GPRS/EDGE/UMTS RF transmitter block 1310," (4) "integrated circuit chip 1400" (purple below), which includes "WLAN 802.11a/b/g interface circuit 1410 coupled to a WLAN chip 1500," and (5) "a WLAN integrated circuit 1500" (orange below), which "includes MAC (media

[527] *Id.* at 33:46-61.

[528] *Id.* at 33:62-63.

[529] *Id.* at 33:66-34:2.

access controller) 1510, PHY (physical layer) 1520 and AFE (analog front end) 1530" and "is coupled by receive (RX), transmit (Tx) and CONTROL lines to an off-chip WLAN RF circuitry 1540."[530]



511. According to *Liu*, these communication chips are "integrated circuits made by any of the improved processes and including the improved transistors illustrated in the other Figures," which includes FinFET structures.[531] Thus, *Liu* teaches that the component may be a communications chip. Additionally, as I highlight in yellow above, *Liu* teaches that the component may be "a RISC processor (such as MIPS core, ARM processor, or other suitable processor)" or "a digital signal processor (DSP)."[532]

[530] *Id.* at 34:33-42, 35:14-20, 35:64-36:36, 37:14-36.

[531] *Id.* at 6:48-51; *see also id.* at 32:23-40, Fig. 8.

[532] *Id.* at 34:23-30, 36:18-31.

512. Because *Liu* teaches "the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of *Ranade* and *Kim*) in the integrated circuit components found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade*, *Kim*, and *Liu* teach "the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor."

513. Because at least one of the asserted combinations of *Ranade*, *Kim,* and *Liu* has every feature in claim 19 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 19 would have been obvious.

10. The Combination of *Ranade, Kim,* and *Liu* Would Have Rendered Claim 20 Obvious

514. Claim 20 depends from claim 12. I understand that means claim 20 requires all the same features as claim 12, plus the additional features recited in claim 20. At least one of the asserted combinations of *Ranade*, *Kim,* and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.B.2.a-p above.

515. Claim 20 further recites "the computing device is selected from the group consisting of a mobile phone, a laptop, a desktop computer, a server, and a set-top box." The asserted combinations of *Ranade*, *Kim*, and *Liu* teach "the computing device is selected from the group consisting of a mobile phone, a laptop, a desktop computer, a server, and a set-top box."

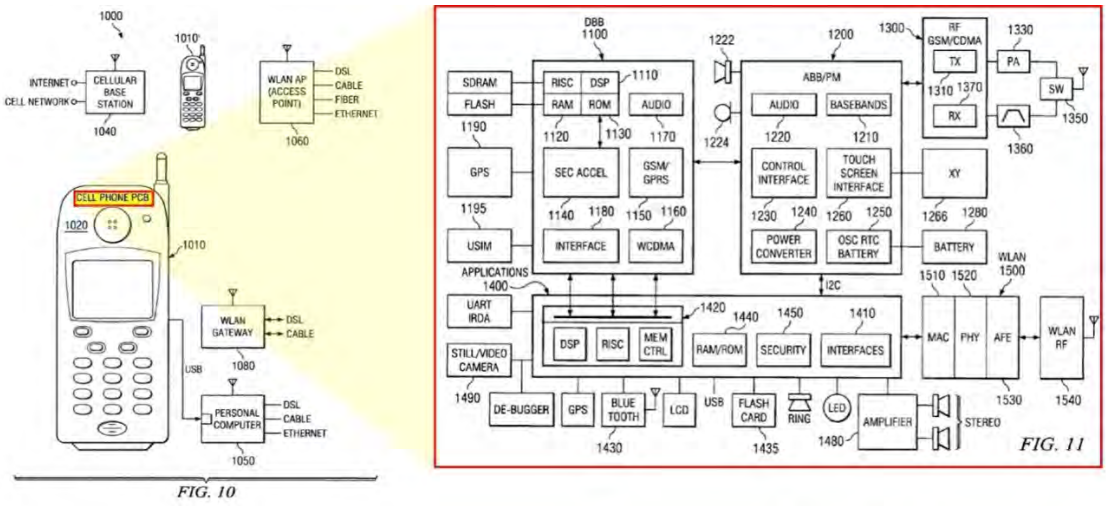
516. As I explain in Section IX.A.16, a person of ordinary skill in the art would have understood the asserted combinations of *Ranade* and *Kim* are both FET structures designed for use in integrated circuits that go onto the circuit boards of smartphones, laptops, desktop computers, servers, set-top boxes, and the like. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 20, *Liu*'s teachings make it explicit.

517. For example, *Liu* describes a "wireless handset," as Figure 10 below illustrates.[533] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[534] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[535] I annotated the figures below to show this relationship.

[533] *Id.* at 33:46-61.

[534] *Id.* at 33:62-63.

[535] *Id.* at 33:66-34:2.



518. According to *Liu*, Figure 11 above depicts "integrated circuits made by any of the improved processes and including the improved transistors illustrated in the other Figures," which includes FinFET structures.[536] Thus, *Liu* teaches the computing device may be a mobile phone. Although I understand that this is sufficient to satisfy claim 20, *Liu* also describes other electronic devices that incorporate integrated circuits, including "radios and televisions, fixed and portable entertainment units, routers, pagers, personal digital assistants (PDA), organizers, scanners, faxes, copiers, household appliances, [and] office appliances."[537]

519. Because *Liu* teaches "the computing device is selected from the group consisting of a mobile phone, a laptop, a desktop computer, a server, and a set-top box," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combinations of

[536] *Id.* at 6:48-51; *see also id.* at 32:23-40, Fig. 8.

[537] *Id.* at 34:3-22.

Ranade and *Kim*) in the integrated circuit components found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combinations of *Ranade, Kim,* and *Liu* teach "the computing device is selected from the group consisting of a mobile phone, a laptop, a desktop computer, a server, and a set-top box."

520. Because at least one of the asserted combinations of *Ranade*, *Kim*, and *Liu* has every feature in claim 20 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 20 would have been obvious.

C. Ground 2A: The Combination of *Tung, Brask,* and *Yu* Would Have Rendered Claims 1, 5-8, and 12-20 Obvious

1. A Person of Ordinary Skill in the Art Would Have Found the Combination of *Tung* and *Brask* Obvious

521. *Tung* describes a FinFET device. On each fin is an epitaxial SiGe source/drain layer, an intermediate doped SiGe or Ge semiconductor layer, and a metal-semiconductor layer. As I explain below, a person of ordinary skill in the art would have understood that the contact resistance in *Tung*'s FinFET is defined by the interface between the metal-semiconductor layer and an intermediate doped semiconductor layer. A person of ordinary skill in the art also would have

understood that using large amounts of Ge in the intermediate doped semiconductor layer would minimize that contact resistance.[538]

522. As I also explain below, a person of ordinary skill in the art would have found it obvious from *Brask* to grade the Ge content in *Tung*'s epitaxial SiGe source/drain regions from a low level compatible with the underlying fin structure to a high level compatible with the overlying doped semiconductor layer.

a. A person of ordinary skill in the art would have understood that using large amounts of Ge in *Tung*'s doped semiconductor layer would minimize source/drain contact resistance

523. *Tung* teaches "structures and methods of fabrication thereof with low resistance contacts for non-planar semiconductor structures" (i.e., for FinFETs).[539] More specifically, *Tung* teaches a structure in which "isolation regions 22 are formed on the substrate 20" in a manner "known in the art."[540] For example, "the isolation regions 22 may be formed by etching substrate 20 to form recesses, and then filling the recesses with dielectric materials."[541] Substrate 20 comprises, for example, "bulk silicon."[542] As the figures below illustrate, *Tung* teaches "[t]he

[538] *See supra* Section VI.C.

[539] *Tung* ¶ [0006]; *see also id.* ¶¶ [0005], [0021], [0027], [0029]-[0032], [0034], [0039], [0061].

[540] *Id.* ¶ [0049].

[541] *Id.*

[542] *Id.* ¶ [0048].

fin 28, disposed between the isolation regions 22, is a continuous piece of underlying semiconductor substrate 20."[543]

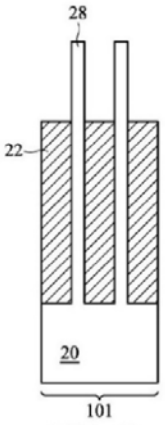


FIG. 6a

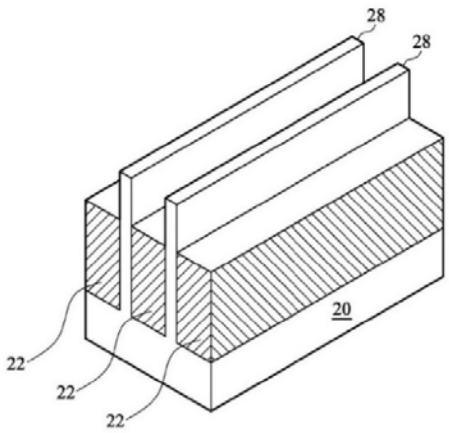


FIG. 6b

524. After forming a gate structure over the channel region of these fins,[544] *Tung* teaches that source/drain regions 39, including extension regions, are formed.[545] For example, semiconductor material 51, such as SiGe, is epitaxially grown over fin 28.[546] Semiconductor material 51, shown in Fig. 4b below, is doped (e.g., with boron) "between about $1\times10^{17}/cm^3$ to about $5\times10^{20}/cm^3$."[547] Next, as Fig. 4c below shows, "another selective epitaxial growth is used to form a doped semiconductor layer 55."[548] Doped semiconductor layer 55 may be "doped SiGe,

[543] *Id.* ¶ [0024]; *see also id.* ¶ [0051] ("Fins 28 may be formed by recessing the top surfaces of the isolation regions 22, and hence leaving the fins 28."), Figs. 6a, 6b.

[544] *See id.* ¶¶ [0052]-[0055], [0073], Fig. 7c.

[545] *See id.* ¶¶ [0073]-[0074], Figs. 2d, 13.

[546] *See id.* ¶¶ [0040], [0074].

[547] *Id.* ¶ [0076]; *see also id.* ¶ [0040], Figs. 4b, 13.

[548] *Id.* ¶ [0041]; *see also id.* ¶ [0078], Figs. 4c, 14.

or doped Ge."[549] It is p-type "if a PMOS transistor is being fabricated."[550] *Tung* also explains that semiconductor layer 55 "is heavily doped" to minimize contact resistance—e.g., to a concentration "greater than about 5×10^{19} cm^{-3}."[551]

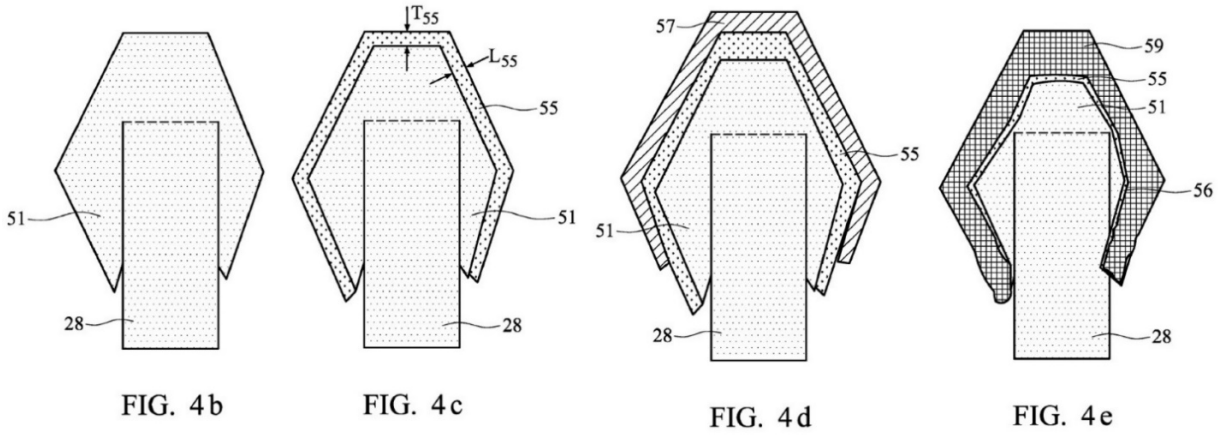


FIG. 4b FIG. 4c FIG. 4d FIG. 4e

525. After growing epitaxial semiconductor layers 51 and 55 over the initial fin 28, and as Figure 4d above shows, "a silicide metal 57 is deposited" over doped semiconductor material 55.[552] *Tung* teaches that metal 57 may be Ti.[553]

526. Next, as Figure 4e above illustrates, *Tung* explains that "silicide metal 57 is annealed to form a metal silicide layer 59[,]" and any "[u]n-reacted silicide metal 57 is removed by an etching process."[554] "During the silicidation

[549] *Id.* ¶ [0078]; *see also id.* ¶ [0058].

[550] *Id.* ¶ [0041].

[551] *Id.* ¶ [0034].

[552] *Id.* ¶ [0042]; *see also id.* ¶¶ [0079]-[0080], Figs. 4d, 15.

[553] *Id.* ¶¶ [0042], [0061], [0080].

[554] *Id.* ¶ [0043]; *see also id.* ¶ [0081], Figs. 4e, 16.

anneal, the silicide metal 57 (FIG. 4d) reacts with the doped semiconductor layer 55 and forms a metal silicide layer 59" (e.g., TiSiGe when metal 57 is Ti).[555]

527. Although *Tung* calls this layer a metal "silicide" layer, this is being used as a generic term in the manner I discuss in Section VII.D. Although *Tung* teaches that doped semiconductor layer 55 can be "doped silicon," it also teaches that doped semiconductor layer 55 can be "doped SiGe" or "doped Ge."[556] A person of ordinary skill would not have understood the metal-semiconductor compound that results when using a doped Ge layer 55, for example, to be a "silicide" in the strict sense of the term. A person of ordinary skill in the art would have understood it is a "germanide" as the '281 Patent uses that term.

528. A person of ordinary skill in the art further would have understood that the source/drain contact resistance in *Tung*'s FinFET is defined by the interface between the metal-semiconductor 59 and the doped semiconductor layer 55. In addition, a person of ordinary skill in the art would have understood

[555] *Id.* ¶ [0043]; *see also id.* ¶¶ [0041], [0045], [0063], [0064], [0081]; S. Zaima & Y. Yasuda, *Study of Reaction and Electrical Properties at Ti/SiGe/Si(100) Contacts for Ultralarge Scale Integrated Applications*, Journal of Vacuum Science & Technology B, vol. 16, at 2625-27, Fig. 1 (1998) ("Silicon atoms preferentially react with Ti atoms at annealing temperatures below 300 °C and Ge atoms start to react above 400 °C."); S. Gaudet et al., *Thin Film Reaction of Transition Metals with Germanium*, Journal of Vacuum Science & Technology A, vol. 24, no. 3 at Fig. 5 (2006) (showing reaction temperatures for numerous metal-Ge compounds).

[556] *Tung* ¶¶ [0058], [0078].

that using large amounts of Ge in the doped semiconductor layer would minimize that contact resistance, as I explain below.

i. The source/drain contact resistance in *Tung*'s FinFET is defined by the interface between the metal-semiconductor layer and the intermediate doped semiconductor layer

529. A person of ordinary skill in the art would have understood that the source/drain contact resistance in *Tung*'s FinFET is defined by the interface between the metal-semiconductor layer 59 and the doped semiconductor layer 55. *Tung* confirms that understanding expressly: "The Schottky barrier height between the doped semiconductor layer 55 and the metal[-semiconductor] layer 59 determines the source/drain series resistance of the transistor."[557] More generally, a person of ordinary skill in the art would have understood that metal-semiconductor layers like *Tung*'s layer 59 reduce contact resistance between a metal and a semiconductor. As one prior-art document explains, "[m]etal semiconductor alloys such as metal silicides, metal germanides, metal germano-silicides reduce contact resistance between a metal structure such as a metal contact via structure and a semiconductor region such as a source region."[558]

[557] *Id.* ¶ [0034].

[558] *Haran* at 1:10-14; *see also supra* Section VI.C.

530. From this knowledge, a person of ordinary skill in the art, who would have sought to minimize *Tung*'s contact resistance, would have found it obvious to form, for example, a TiSiGe metal-semiconductor layer 59 by using a titanium metal layer 57 to metalize part of a doped semiconductor layer 55. A person of ordinary skill in the art would have expected the resulting interface between such a TiSiGe layer 59 and what remains of doped semiconductor layer 55 to provide a low Schottky barrier height in p-type regions and to reduce contact resistance.[559] *Tung* and others also describe how to form such a layer.[560]

[559] *See, e.g.*, *Tung* ¶ [0078] ("[T]he doped semiconductor layer 55 comprises doped SiC, doped SiGe, or doped Ge."), ¶ [0080] ("The silicide metal 57 comprises a suitable metal, such as, for example, . . . Ti . . . ."), ¶ [0043] ("During the silicidation anneal, the silicide metal 57 (FIG. 4d) reacts with the doped semiconductor layer 55 and forms a metal silicide layer 59."); *see also id.* ¶¶ [0005], [0006], [0021], [0027], [0029]-[0032], [0034], [0039], [0061], [0070]; *Kim* ¶¶ [0003]-[0008], [0010], [0050], [0051], [0058], [0074]; *Haran* (US8358012) at Title, 1:7-25, 3:17-22; *Rhee* (US2008/0067545) ¶¶ [0021], [0024], [0025], [0042]; *Simonelli* (US2010/0148217) ¶¶ [0024], [0043]; *Murthy* (US6949482) at Abstract, 2:66-3:13, 8:34-9:63, Figs. 5-8; *Yasutake* (US2007/0187767) ¶¶ [0005], [0024], [0025], [0039]-[0045], [0050], [0066], [0070], [0086], [0093]; *Honeycutt* (US5644166) at 1:8-15, 4:46-53; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 226-27, 230, Fig. 18 (Mar. 2005).

[560] *See Tung* ¶¶ [0042]-[0045], [0063]-[0065], [0067], [0068], [0081]; *Kim* (US2010/0123198) ¶¶ [0047]-[0051], [0057], [0066], [0067], [0070], [0071], [0073], [0074], Figs. 1F, 2D, 3F, 4, 5; *Rhee* (US2008/0067545) ¶ [0042], Fig. 7; *Yasutake* (US2007/0187767) ¶¶ [0024], [0036], [0050], [0066], [0080], [0093], Fig. 8; *Honeycutt* (US5644166) at 1:8-15, 4:46-53, 5:6-45, 7:20-43, 7:61-8:42.

ii. Large amounts of Ge in *Tung*'s doped semiconductor layer would have been expected to minimize source/drain contact resistance

531. A person of ordinary skill in the art would have understood that using large amounts of Ge in *Tung*'s doped semiconductor layer 55 would reduce the Schottky barrier height and, consequently, the source/drain contact resistance in *Tung*'s FinFET.

532. A person of ordinary skill in the art would have understood that the source/drain contact resistance in these types of FET devices depends largely on the Schottky barrier height at the interface between metal-semiconductor (*Tung*'s metal-semiconductor layer 59) and the semiconductor region below (*Tung*'s doped semiconductor layer 55).[561] And as I explain in Section VI.C, a person of ordinary skill in the art also would have known that the Schottky barrier height in pFET source/drain regions depends on the Ge concentration according to the well-known figure below[562]:

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[561] *See Tung* ¶ [0034] ("The Schottky barrier height between the doped semiconductor layer 55 and the metal silicide layer 59 determines the source/drain series resistance of the transistor."); *supra* Section VI.C.

[562] R. Braunstein et al., *Intrinsic Optical Absorption in Germanium-Silicon Alloys*, Physical Review, vol. 109, no. 3, pp. 695-710, at Fig. 17 (1958); *see also* J. Weber & M.I. Alonso, *Near-Band-Gap Photoluminescence of Si-Ge Alloys*, Physical Review B, vol. 40, no. 8, pp. 5683-5693, at 5689, Fig. 9 (1989); M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 227, Fig. 12 (Mar. 2005).

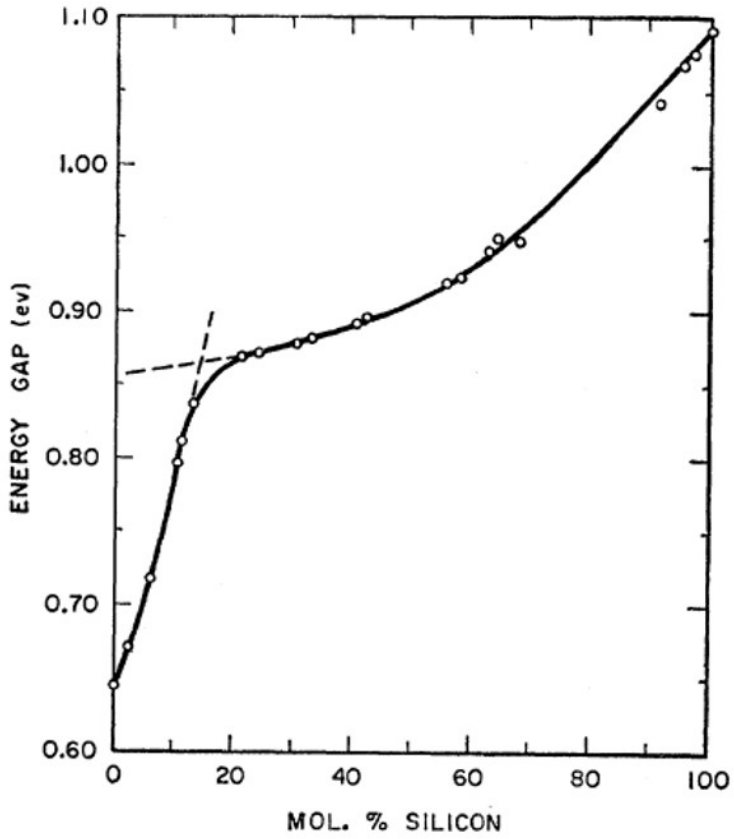


FIG. 17. Composition dependence of energy gap in Ge-Si alloys at 296°K, based on one-phonon Macfarlane-Roberts expression; see Eq. (1) in text.

533. As the figure above illustrates, and as I further explain in Section VI.C, there is a kink in the SiGe bandgap at about 15 atomic % Si (i.e., about 85 atomic % Ge). Because adjusting the SiGe bandgap (i.e, adjusting the Ge concentration) is a clear way to reduce the Schottky barrier height in p-type SiGe material, a person of ordinary skill in the art would have wanted to use a Ge concentration above the transition at about 85 atomic % to minimize the Schottky barrier height in *Tung*'s pFET source/drain regions.[563]

[563] *See* Section VI.C.

534. Thus, knowing that (1) the contact resistance in *Tung*'s device depends primarily on the Schottky barrier height at the interface the metal-semiconductor layer 59 and the doped semiconductor layer 55; and (2) using Ge concentrations above about 85 atomic % in the doped semiconductor layer 55 would minimize the Schottky barrier height and thus contact resistance in *Tung*'s device, a person of ordinary skill in the art would have found it obvious to implement *Tung*'s device using Ge concentrations above about 85 atomic % in the doped semiconductor layer 55. Moreover, *Tung* expressly discloses such embodiments by teaching that doped semiconductor layer 55 comprises "doped SiGe, or doped Ge."[564]

b. A person of ordinary skill in the art would have found it obvious to grade the Ge concentration in *Tung*'s SiGe source/drain regions from a level compatible with the underlying fin to a level compatible with the overlying doped semiconductor layer

535. *Tung* teaches a SiGe semiconductor material 51 in which its source/drain regions are partially formed.[565] To understand what Ge concentrations would have been appropriate for *Tung*'s SiGe semiconductor material 51, a person of ordinary skill in the art would have found it obvious to apply *Brask*'s teachings about such SiGe source/drain compositions. As I explain below, a person of

[564] *Tung* ¶¶ [0058], [0078].

[565] *See id.* ¶¶ [0040], [0074].

ordinary skill in the art would have found it obvious to grade the Ge concentration in *Tung*'s SiGe semiconductor material 51 from a level compatible with the underlying fin 28[566] to a level compatible with the overlying doped semiconductor layer 55.

536. *Brask* teaches the same basic structure as *Tung*, as *Brask*'s Figures 4A and 4B below illustrate:

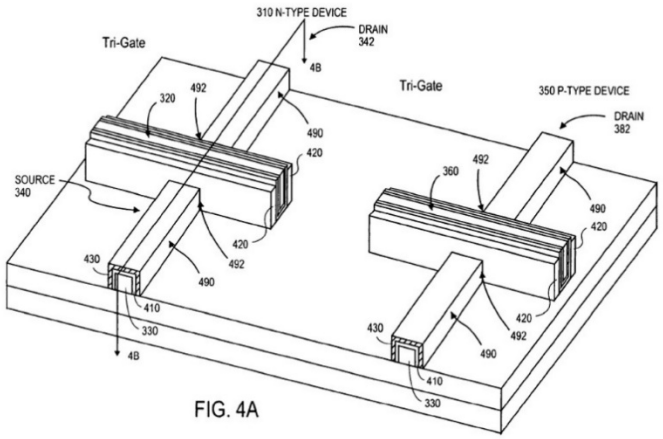


FIG. 4A

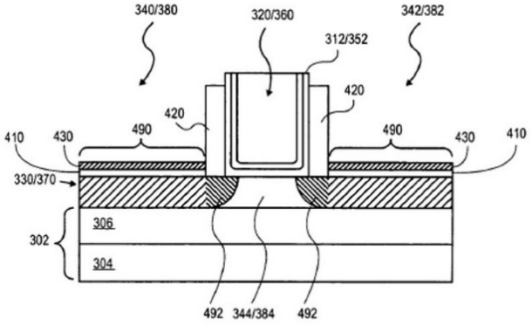


FIG. 4B

537. Like *Tung*'s fin 28, *Brask*'s FinFET has a fin 370 that may be silicon, for example.[567] Also like *Tung*'s fin 28, which contains a channel region under the gate sandwiched by source/drain regions 39, *Brask*'s fin 370 contains a channel

[566] *See id.* ¶¶ [0024] ("The fin 28, disposed between the isolation regions 22, is a continuous piece of underlying semiconductor substrate 20."), [0051] ("Fins 28 may be formed by recessing the top surfaces of the isolation regions 22, and hence leaving the fins 28.").

[567] *Compare id.* ¶¶ [0048]-[0052], Figs. 5, 6a, 6b, *with Brask* at 5:30-34, 12:51-56, 15:21-34, Figs. 4A, 4B, 5E, 5F.

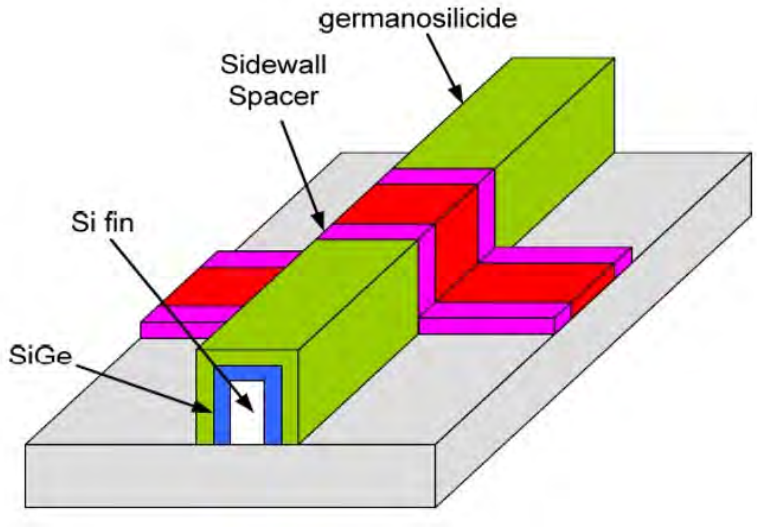
region 384 under the gate sandwiched by source/drain regions 490.[568] Both *Tung*'s FinFET and *Brask*'s FinFET also contain source/drain extension regions.[569] Like *Tung*'s FinFET, which further includes raised Si_xGe_{1-x} source/drain regions grown as semiconductor material 51 on fin 28, *Brask*'s FinFET further includes raised Si_xGe_{1-x} source/drain regions grown as semiconductor film 410 (where x=0 to 0.99, i.e., 1 to 100 atomic % Ge) on fin 370.[570] And both *Tung*'s and *Brask*'s FinFETs include a metal-semiconductor layer (layers 59 and 430, respectively) formed by titanium metalization of a semiconductor layer (layers 55 and 410, respectively) to serve as a source/drain contact metal.[571] In short, *Tung* and *Brask* disclose analogous FinFETs with the same basic structure—one also generally described elsewhere in the SiGe FinFET literature:

[568] *Compare Tung* ¶¶ [0024]-[0027], [0032]-[0034], [0048], [0065], Figs. 2a-2d, 11a-11c, *with Brask* at 5:26-51, 8:13-41, 9:61-10:11, Figs. 4A, 4B.

[569] *Compare Tung* ¶¶ [0057], [0073], Figs. 2d, 11c, *with Brask* at 9:61-10:11, 11:15-31, Fig. 4B.

[570] *Compare Tung* ¶¶ [0039]-[0041], [0074]-[0078], Figs. 2a-2d, 4a-4c, 8, 11a-11c, 13, 14, *with Brask* at 10:20-49, Figs. 4A, 4B.

[571] *Compare Tung* ¶¶ [0042]-[0045], [0059]-[0065], [0079]-[0081], Figs. 2a-2d, 4d, 4e, 9a-11c, 15, 16, *with Brask* at 10:50-64, Figs. 4A, 4B.



538. Describing the figure above, the authors explain:

> FINFET source/drain integration suffers from the same problem mentioned in the previous section for the ultrathin body MOSFET. Basically, the Si fin is so thin that formation of a silicide contact consumes the entire fin reducing the contact area to the cross-sectional area of the fin. The logical solution to this problem is to increase the thickness of the fin by selective deposition of a sacrificial layer. The resulting structure can be viewed as an elevated source/drain FINFET. This approach was implemented in a recent study at IBM using selective Si epitaxy. It should also be possible to use $Si_{1-x}Ge_x$ instead of Si to lower the contact resistance and possibly to introduce compressive strain into the Si channel.[572]

[572] M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 230 (Mar. 2005); *see also id.* at Fig. 18; K.-M. Tan et al., Π-*Shaped Silicon–Germanium Source and Drain Stressors*, IEEE Electron Device Letters, vol. 28, no. 10, at 905-08, Figs. 1, 2 (Oct. 2007); J. Kavalieros et al., *Tri-Gate Transistor Architecture With High-k Gate Dielectric Metal Gates and Strain Engineering*, 2006 IEEE Symposium on VLSI Technology Digest of Technical Papers, at 1, Figs. 7a-7b (June 2006).

539. *Tung* teaches that the semiconductor layer 51 of its source/drain regions "comprises SiGe."[573] Since *Tung* and *Brask* disclose analogous FinFETs, a person of ordinary skill in the art would have found it obvious to look at *Brask*'s teachings to understand additional details suitable for *Tung*'s FinFET. In particular, a person of ordinary skill in the art would have understood *Tung*'s SiGe semiconductor material 51, which is analogous to *Brask*'s semiconductor film 410, may be "silicon germanium where silicon comprises approximately 1 to 99 atomic percent of the alloy and can even extend to pure (100%) Ge."[574] Additionally, a person of ordinary skill in the art would have understood that the germanium content in that layer may "be graded."[575] Thus, following *Brask*'s teachings, a person of ordinary skill in the art would have found it suitable to grade the Ge concentration in *Tung*'s SiGe semiconductor material 51 within the range of 1 to 100 atomic %. Additionally, a person of ordinary skill in the art would have wanted to do so because it has the effect of "reducing the source/drain contact resistance to transistors 310 and 350 and improving their electrical characteristics and performance," which is the purpose of *Tung*'s source/drain structure as well.[576]

[573] *Tung* ¶ [0040].

[574] *Brask* at 10:24-29.

[575] *Id.*

[576] *Id.* at 10:31-49; *see also Tung* ¶¶ [0005], [0006], [0026], [0027], [0032], [0034], [0078].

540. A person of ordinary skill in the art also would have known that grading the Ge concentration in *Tung*'s SiGe semiconductor material 51 would minimize dislocations. He or she would have readily understood there is a lattice mismatch between *Tung*'s fin 28 (typically, silicon or low-Ge content SiGe for pFETs[577]) and *Tung*'s Ge semiconductor layer 55 (which would contain more than about 85 atomic % Ge[578]). *Tung*'s semiconductor material 51 is sandwiched vertically between fin 28 and Ge semiconductor layer 55. From his or her training and experience, a person of ordinary skill in the art would have understood that lattice mismatch between SiGe semiconductor material 51 and the underlying fin 28, or lattice mismatch between SiGe semiconductor material 51 and the overlying Ge semiconductor layer 55, can cause unwanted dislocations in one or more of those layers.[579] It was also known that a graded layer—one that has a Ge

[577] *See Tung* ¶¶ [0048]-[0051]. Although semiconductor material 51 will be grown in the source/drain regions of fin 28, the channel region is made exclusively of the material comprising fin 28. To strain the channel, fin 28 would need to contain less Ge than semiconductor material 51. The specification also mentions other options, such as Ge or III-V semiconductors, but subsequent descriptions would be illogical if the substrate 300 in the preferred embodiments were not Si or low-Ge content SiGe for pFETs.

[578] *See Tung* ¶¶ [0058], [0078]; *supra* Sections VI.C, IX.C.1.a.ii, note 38.

[579] *See* Section VI.B; *Ranade* ¶ [0040]; *Thomas* (US2009/0075029) ¶¶ [0030]-[0032]; *Jin* (US7767560) at 3:30-43, 3:60-64, 4:2-8, 4:28-60; *Kavalieros* (US8211772) at 2:10-22; H. Okamoto et al., *A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-Node High-Performance pMOSFET Technology*, Proceedings of the 2008 38th European

concentration compatible with the underlying fin at its lower surfaces and a Ge concentration compatible with the overlying film at its upper surfaces—minimizes dislocations and preserves strain.[580] Applying this well-known concept to *Tung*'s FinFET (as *Brask* suggests), a person of ordinary skill in the art would have found it obvious to grade the Ge composition in *Tung*'s SiGe semiconductor material 51 from a level compatible with underlying fin 28 up to a level compatible with Ge semiconductor layer 55 (by which I mean a layer with > about 85 atomic % Ge[581]).

541. By December 2010, grading the Ge concentration across *Tung*'s SiGe semiconductor material 51, as *Brask* suggests, would have been feasible because Si_xGe_{1-x} strain engineering was already ubiquitous.[582] And it was a common

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Solid-State Device Research Conference (ESSDERC), pp. 326-329, at 327 (Sept. 2008) ("One possible cause of strain relaxation could be a generation of crystal defects in eSiGe.")

[580] *See, e.g.*, *Ranade* ¶¶ [0033], [0040]; *Yasutake* (US2007/0187767) ¶¶ [0084], [0085], [0090], [0094]; *Thomas* (US2009/0075029) ¶¶ [0030]-[0032], [0042]; *Jin* (US7767560) at 3:39-44, 7:61-8:18; *Kavalieros* (US8211772) at 4:58-61, 6:60-7:11, Fig. 5b; J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2 (2006) (explaining "higher channel stress can be achieved with a graded eSiGe process").

[581] *See supra* Sections VI.C, IX.C.1.a.ii, note 38.

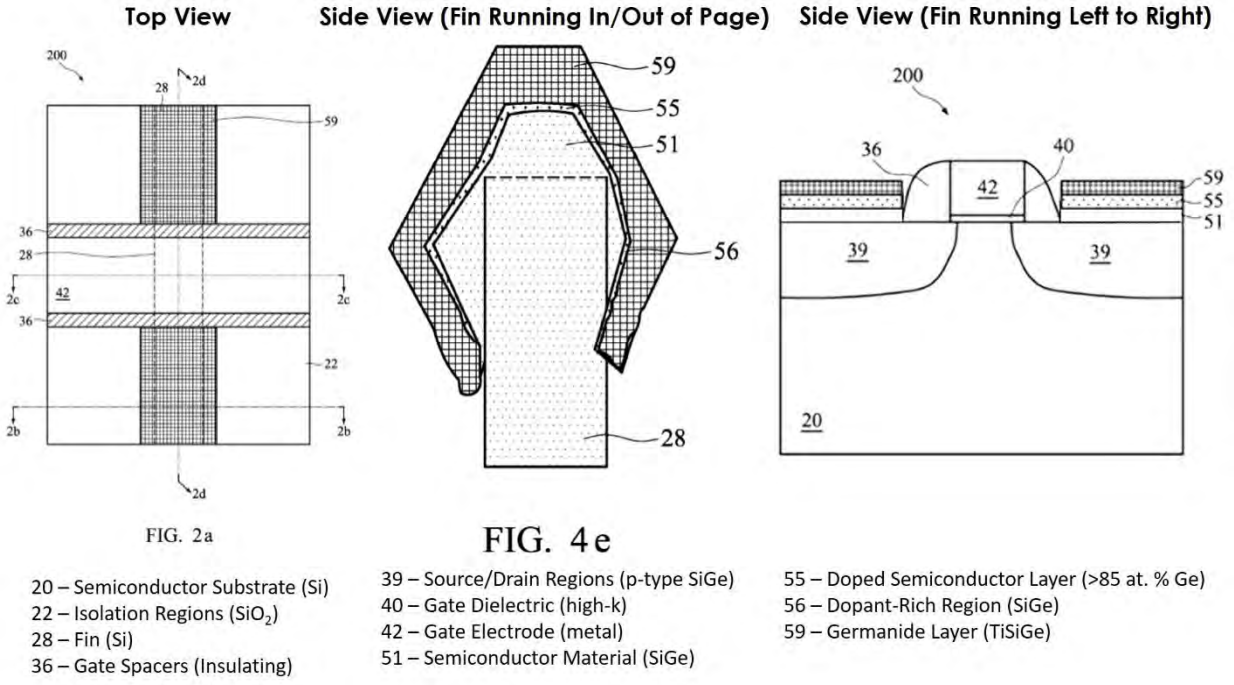
[582] *See* Section VI.B; *Ranade* at Abstract, ¶¶ [0010], [0014], [0023], [0038]-[0040], [0047]; J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2-3, Figs. 1-16 (2006); *Simonelli* (US2010/0148217) at Title, ¶¶ [0020], [0024], [0038], [0042], [0044], [0053], [0058]; *Kim* at ¶¶ [0054], [0064]; *Thomas* (US2009/0075029) at Title,

approach in strain engineering to grade the Ge concentration in epitaxial Si_xGe_{1-x} source/drain regions across the entire range of possible Ge compositions, which *Brask* and others confirm.[583]

Abstract, ¶¶ [0003]-[0005], [0007], [0008], [0029]-[0032], [0044], [0063]; *Murthy* (US6949482) at 1:41-2:20, 6:60-7:10; *Yasutake* (US2007/0187767) ¶¶ [0004], [0005], [0023], [0034], [0038], [0041], [0048], [0049], [0056]-[0058], [0068], [0071], [0075], [0082], [0093]; *Kavalieros* (US8211772) at Abstract, 1:55-63, 2:11-22, 2:59-67, 4:56-57; *Jin* (US7767560) at Title, Abstract, 1:9-13, 1:45-57, 2:44-51, 3:10-5:19, 5:48-6:1, 6:61-7:13, 8:62-10:27, 10:50-67, Figs. 4E, 4F; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 229-30 (Mar. 2005); S. Gannavaram et al., *Low Temperature (≤800°C) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for Sub-70 nm CMOS*, Technical Digest of the 2000 IEEE International Electron Devices Meeting (IEDM) at 437-38, Figs. 4, 12 (2000); H. Okamoto et al., *A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-Node High-Performance pMOSFET Technology*, Proceedings of the 2008 38th European Solid-State Device Research Conference (ESSDERC), at Abstract, 326-29, Figs. 1, 5 (Sept. 2008).

[583] *See Brask* at 5:26-34, 10:20-29; *Ranade* ¶¶ [0032], [0033], [0040]; *Thomas* (US2009/0075029) at Abstract, ¶¶ [0008], [0032]-[0036], [0042]-[0045], [0051], [0056]; J.-P. Han et al, *Novel Enhanced Stressor with Graded Embedded SiGe Source/Drain for High Performance CMOS Device*, Technical Digest of the 2006 International Electron Devices Meeting (IEDM) at 2-3 (2006); *Yasutake* (US2007/0187767) ¶¶ [0034], [0062], [0085], [0090], [0094], [0095]; *Jin* (US7767560) at Abstract, 4:28-5:19, 5:48-6:6, 7:61-8:31; *Simonelli* (US2010/0148217) at Title, Abstract, ¶¶ [0001], [0018]-[0021], [0024], [0039]-[0040], [0042], [0044], [0051]-[0055], [0057], [0058]; *Wang* (US2008/0054347) ¶¶ [0022]-[0024]; *Liu '953* (US2007/0122953) ¶¶ [0059], [0060], [0080]-[0083]; P. Ranade et al., *A Novel Elevated Source/Drain PMOSFET Formed by Ge-B/Si Intermixing*. IEEE Electron Device Letters, vol. 23, no. 4, at 218-19 & Figs. 1, 2 (Apr. 2002).

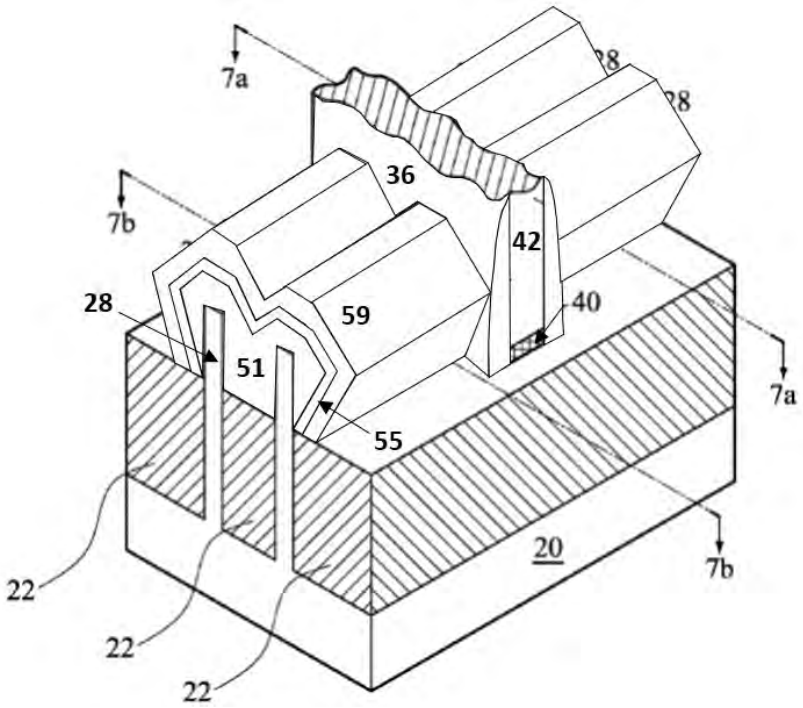
542. Accordingly, a person of ordinary skill in the art would have considered it obvious to create the device structure shown below, which I have labeled "*Tung* Implemented According to *Brask*." The figure on the left (*Tung*'s Fig. 2a) shows the plan view of the device from above. The middle figure (*Tung*'s Fig. 4e) shows a side view of the device looking along the direction of the fin (i.e., the cross-section denoted "2b" in *Tung*'s Fig. 2a). And the figure on the right (*Tung*'s Fig. 2d, modified to include semiconductor material 51[584]) shows a side view of the device with the fin running in the left-right direction, where the fin has been cut down the middle (i.e., the cross-section denoted "2d" in *Tung*'s Fig. 2a).



Tung* Implemented According to *Brask

[584] *See Tung* ¶ [0033].

543. In an orthographic view, it would resemble something like the structure below (a more realistic depiction of *Tung*'s Fig. 16, although the individual fins may or may not merge[585]):



544. For the reasons I explain above, a person of ordinary skill in the art would have found it obvious (1) to implement *Tung*'s FinFET such that doped semiconductor layer 55 has a Ge concentration more than about 85 atomic %[586]; (2) to combine the teachings of *Tung* and *Brask* such that the Ge concentration in the epitaxial SiGe semiconductor material 51 is graded from an amount compatible with fins 28, for example, up to an amount compatible with doped semiconductor

[585] *Id.* ¶¶ [0058], [0078].

[586] *See id.* ¶¶ [0034], [0058], [0078]; *supra* Sections VI.C, IX.C.1.a.ii, note 38.

layer 55[587]; and (3) to follow *Tung*'s instruction that metal layer 57 may be titanium such that metal-semiconductor layer 59 would be TiSiGe.[588]

545. A person of ordinary skill in the art would have considered such a combination of *Tung*'s and *Brask*'s teachings to be obvious according to at least four of the various obviousness rationales I among those have been asked to consider.

546. First, a person of ordinary skill in the art would have considered applying grading *Tung*'s SiGe semiconductor material 51 in the manner described above to be an example of combining prior art elements according to known methods to yield predictable results. The concept of graded Ge concentration in raised SiGe source/drain regions, as *Brask* suggests using, was an element of the prior art, and so were *Tung*'s raised SiGe source/drain regions in semiconductor material 51. A person of ordinary skill in the art would have recognized that these two prior-art elements could be combined according to known methods, such as performing graded SiGe epitaxy. A person of ordinary skill in the art also would

[587] *See Tung* ¶¶ [0033], [0040], [0048]-[0051], [0058], [0074], [0078]; *Brask* at 10:20-29.

[588] *See Tung* ¶¶ [0042], [0043], [0061], [0080], [0081]; *Brask* at 10:50-64; M.C. Ozturk & J. Liu, *Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond*, 2005 International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings, vol. 788, at 230 & Fig. 18 (Mar. 2005).

have expected that doing so would yield predictable results, such as raised SiGe source/drain regions with minimal defects, reduced source/drain contact resistance, and enhanced stress applied to the channel region.

547. Second, a person of ordinary skill in the art would have considered grading *Tung*'s SiGe semiconductor material 51 in the manner described above to be an example of the use of a known technique to improve similar devices in the same way. A person of ordinary skill in the art would have known how to perform graded SiGe epitaxy to grade the Ge concentration in *Tung*'s raised SiGe semiconductor material 51, as *Brask* suggests. A person of ordinary skill in the art also would have recognized that such a technique could be applied to improve *Tung*'s raised SiGe source/drain semiconductor material 51 by minimizing dislocations, reducing source/drain contact resistance, and enhancing strain.

548. Third, a person of ordinary skill in the art would have considered grading *Tung*'s SiGe semiconductor material 51 in the manner described above to be an example of applying a known technique to a device ready for improvement yield predictable results. Again, a person of ordinary skill in the art would have known how to perform graded SiGe epitaxy to grade the Ge concentration in *Tung*'s raised SiGe semiconductor material 51, as *Brask* suggests. A person of ordinary skill in the art also would have understood that *Brask*'s suggestion applies to *Tung*'s SiGe semiconductor material 51, which would have predictably

benefitted from reduced dislocation densities, lower source/drain contact resistance, and enhanced strain.

549. Fourth, a person of ordinary skill in the art would have considered grading the Ge concentration in *Tung*'s raised SiGe semiconductor material 51 due to a teaching, suggestion, or motivation in the prior art to arrive at the claimed invention. A person of ordinary skill in the art would have been familiar with several teachings, suggestions, or motivations in the prior art, including those provided in *Tung* and *Brask* themselves and in other references such as those I discuss in Sections VI.B and VI.C above. In applying those teachings, suggestions, or motivations as I describe above, a person of ordinary skill in the art would have arrived at the claimed invention.

550. Regardless of the rationale a person of ordinary skill in the art would have applied, it is my opinion that he or she would have found the combination of *Tung* and *Brask* discussed above to be obvious.[589]

2. A Person of Ordinary Skill in the Art Would Have Found the Combination of *Tung*, *Brask*, and *Yu* Obvious

551. A person of ordinary skill in the art further would have found it obvious to apply the teachings of *Yu* to provide the necessary source/drain contacts to the *Tung-Brask* FinFET I described above.

[589] *See supra* Sections VI.B, VI.C, IX.C.1.

552. *Tung* and *Brask* describe and illustrate FinFETs by focusing on the structure of the transistor itself, not the metallic interconnections required to connect various transistors to one another on the wafer and to the outside world. *Tung*'s figures, for example, do not illustrate source/drain contacts for its disclosed FinFET, which are needed for electrical connection. A person of ordinary skill in the art would have understood that such structures are not the focus of *Tung*'s invention. *Tung* simply explains that "[a] contact (not shown) is disposed on the metal silicide layer 59."[590] More specifically, *Tung* explains that "[c]ontacts (not shown) are subsequently formed on the metal silicide layer 59 and subsequent processing including metallization proceeds as in conventional processing."[591]

553. Omitting the metal contact structure when describing an FET device was and remains common when describing the FET structure itself. A person of ordinary skill in the art would have understood that omitting discussion or illustration of metallic interconnections and related processes, as *Tung* and *Brask* do, was typical. Numerous prior-art publications, including *Tung* and *Brask* themselves, confirm this.[592] For example, *Brask* explains the following:

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[590] *Tung* ¶ [0023].

[591] *Id.* ¶ [0064]; *see also id.* ¶ [0005].

[592] *See, e.g.*, *Simonelli* ¶ [0043] (explaining that "device 100 may undergo further MOS processing . . . that may further modify the device and/or provide the necessary electrical interconnections."); *Brask* at 27:20-27 ("Well known

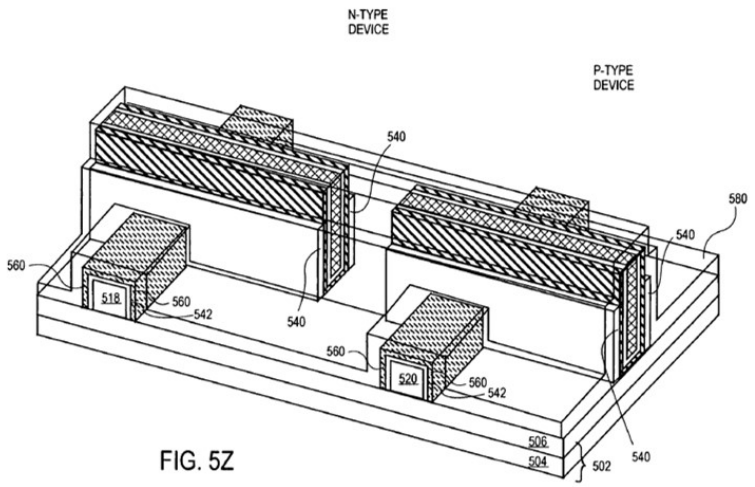


FIG. 5Z

At this point, the fabrication of an n type and p type nonplanar device having a metal gate electrode and metal oxide dielectric films have been formed. Well known back end processing steps can now be utilized to interconnect the various p type and n type devices together into functional CMOS integrated circuits. The back end of the process includes formation of interlayer dielectric layers and metal interconnects.[593]

[interlayer dielectric layers and metal interconnects] can now be utilized to interconnect the various p type and n type devices together into functional CMOS integrated circuits."); *Yeh* (US9245805) at 4:43-48 ("Next, silicide/germanide regions (not shown) may be formed on source/drain regions 142 and 242 by reacting source/drain regions 142 and 242 with a metal(s) to reduce the contact resistances. The formation details of silicide/germanide regions are known in the art, and hence are not repeated herein."); *Tung* ¶¶ [0023] ("A contact (not shown) is disposed on the metal silicide layer 59."), [0036] (same), [0064] (same); *Rhee* (US2008/0067545) ¶ [0018] ("The contact portion of the source/drain region may be in contact with a contact structure."), [0021] ("A contact structure configured to transmit an electrical signal to the source/drain region may be connected to the metal semiconductor compound layer 124 so as to be electrically connected.").

[593] *Brask* at 27:20-27; *see also id.* at Fig. 5Z.

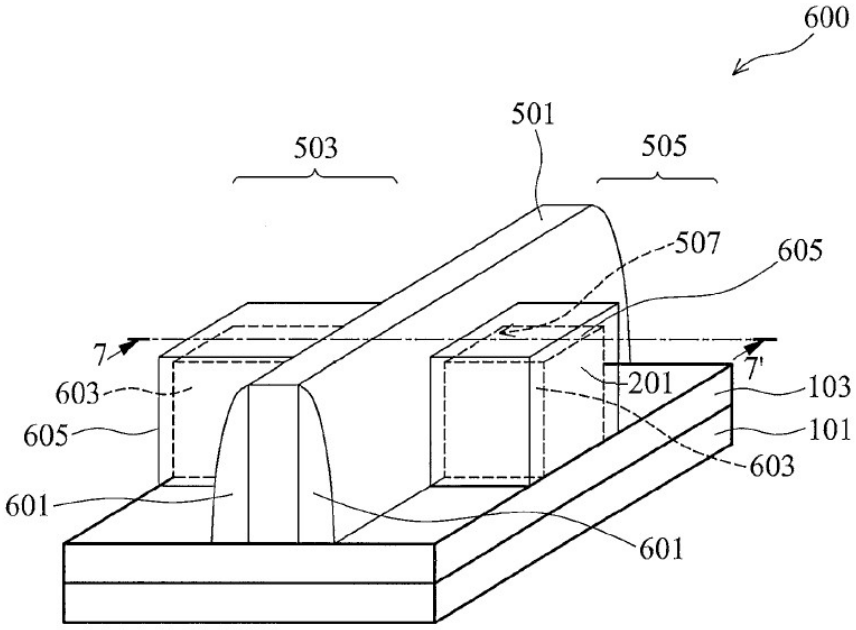
554. A person of ordinary skill in the art would have understood that *Tung*'s and *Brask*'s semiconductor devices would include the interconnections necessary to operate. Those interconnections would include, among other things, a suitable source/drain electrode to facilitate electrical connection to the source/drain regions. A person of ordinary skill in the art would have recognized that such a source/drain electrode structure **must** be added for such devices to operate. Accordingly, a person of ordinary skill in the art seeking to implement the combined *Tung-Brask* FinFET would have been motivated to include low-resistance source/drain contacts, as *Tung* instructs, by adding source/drain contacts to the TiSiGe layer 59.[594]

555. *Yu*, which is titled "System and Method for Source/Drain Contact Processing," focuses on describing a source/drain contact structure for use with a FinFET like *Tung*'s and *Brask*'s (and the combined *Tung-Brask* FinFET discussed in Section IX.C.1). As the figure below illustrates, *Yu* teaches the same basic FinFET structure as *Tung* and *Brask*.[595] Like *Tung*'s FinFET and *Brask*'s FinFET, *Yu*'s FinFET has a fin 201 capped with a titanium-based metal-semiconductor

[594] *See Tung* ¶¶ [0005], [0064].

[595] *Compare Yu* ¶¶ [0018]-[0043], Figs. 5-10B, *with Tung* ¶¶ [0031]-[0034], [0039]-[0065], [0072]-[0082], Figs. 2a-2d, 4e, 7c, 11a, 11c, 16, *and Brask* at 4:62-12:17, Figs. 3-4C.

compound 605 in source/drain regions 603.[596] *Yu* further discusses how to make source/drain contacts to such a device structure.[597]



556. *Yu* describes how to form source/drain contacts by referring to Figures 8, 9A, and 9B below. To begin, *Yu* explains that an inter-layer dielectric (ILD) 801 is formed over the entire device structure, as in Figure 8 below.[598] *Yu* explains that "[t]he ILD 801 may be formed by chemical vapor deposition, sputtering, or any other methods known and used in the art for forming an ILD 801" and "typically has a planarized surface."[599] Additionally, it "may be

[596] *See Yu* ¶¶ [0021], [0028], [0029], [0031], Figs. 5-7.

[597] *Id.* ¶¶ [0034]-[0043], Figs. 8-9B.

[598] *Id.* ¶ [0034]; *see also id.* at Fig. 8.

[599] *Id.* ¶ [0034].

comprised of silicon oxide" and "impart[s] a strain to the channel region 507 of the fin 201, which will increase the overall performance of the device 600."[600]

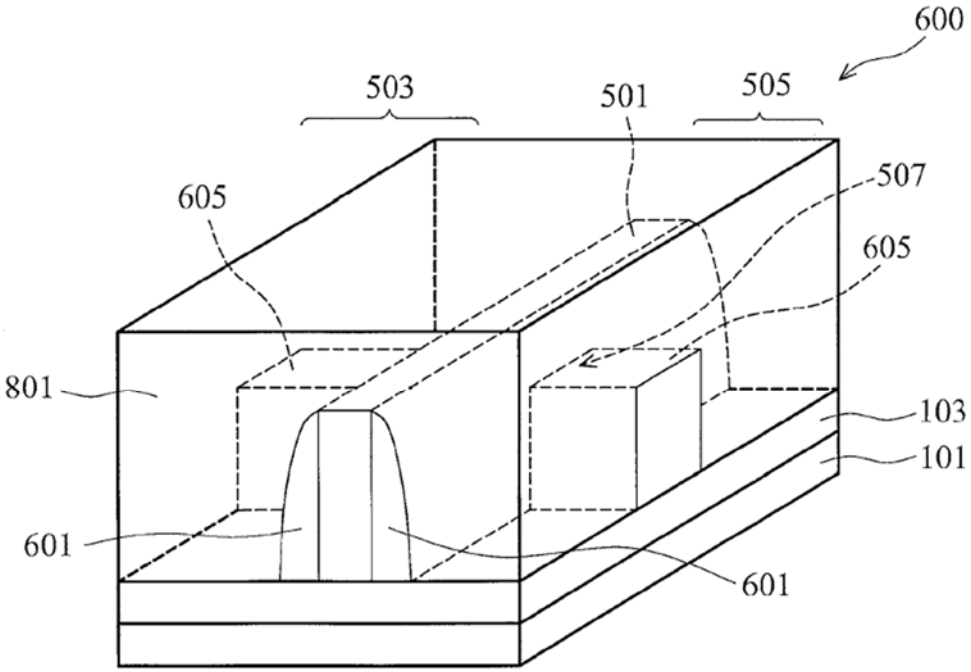


FIG. 8

557. Next, as Figures 9A and 9B below illustrate,[601] *Yu* explains that contacts 901 are formed through the ILD down to the metal-semiconductor layer 605.[602] "Contacts 901 may be formed in the ILD 801 in accordance with known photolithography and etching techniques."[603]

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[600] *Id.*

[601] Figure 9A provides an orthographic view of *Yu*'s FinFET device after contact plugs 901 have been added, and Figure 9B provides a plan-view cross-section of the same structure from above. *See Yu* ¶¶ [0035], [0040].

[602] *Yu* ¶ [0035]; *see also id.* at Figs. 9A, 9B.

[603] *Id.* ¶ [0035].

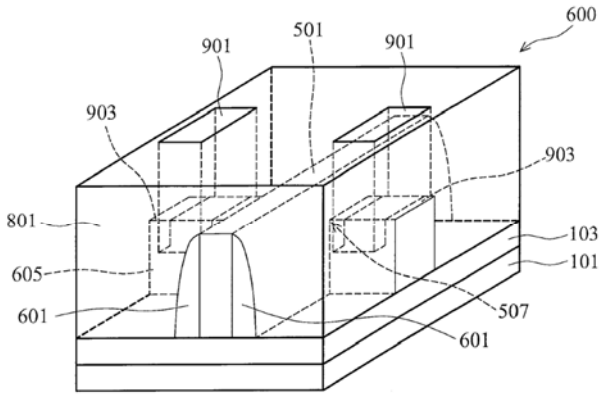


FIG. 9A

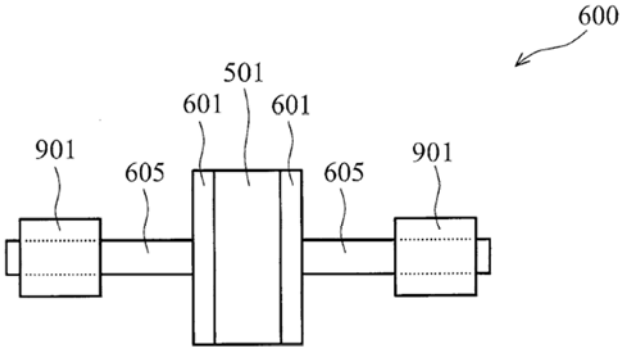


FIG. 9B

According to *Yu*, "photoresist material is utilized to create a patterned mask to define contacts 901[,]" and then "[t]he mask is patterned to subsequently form openings that are wider than the width of the fin 201."[604] More specifically, "the etch process is continued until an upper surface 903 of the fin 201 containing the source/drain regions 603 and at least a portion of the sidewalls of the fin 201 are exposed, thereby exposing at least three surfaces of the fin 201 (portions of the top surface and portions of at least two sidewalls)."[605] Contacts 901 are then "formed so as to be in contact with at least three surfaces of the fin 201[,]" which "allows for a larger area of contact between the silicide contacts 605 and the contact 901 than contacts that only contact the top surface of the fin 201."[606] "Accordingly, the contact resistance of the device may be reduced[,]" and "variations in the contact

[604] *Id.*

[605] *Id.* ¶ [0036].

[606] *Id.* ¶ [0037].

resistances due to mis-alignments of the contacts 901" are reduced "since there is more leeway for variation when the width of the contacts 901 are larger than the width of the fin 201."[607]

558. *Yu* further explains "contacts 901 may comprise a barrier/adhesion layer (not shown) to prevent diffusion and provide better adhesion between the contacts 901 and the ILD 801."[608] As was common, such a barrier layer may be "formed of one or more layers of titanium, titanium nitride, tantalum, tantalum nitride, or the like."[609] And "contacts 901 may be formed of any suitable conductive material, such as a highly-conductive, low-resistive metal, elemental metal, transition metal, or the like."[610] "In an exemplary embodiment the contacts 901 are formed of tungsten, although other materials, such as copper, could alternatively be utilized."[611]

559. In view of these considerations, a person of ordinary skill in the art would have known that *Yu* describes the structure *Tung* alludes to when it states, "Contacts (not shown) are subsequently formed on the metal silicide layer 59."[612]

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[607] *Id.*

[608] *Id.* ¶ [0038].

[609] *Id.*; *see also supra* Section VI.F.

[610] *Yu* ¶ [0039].

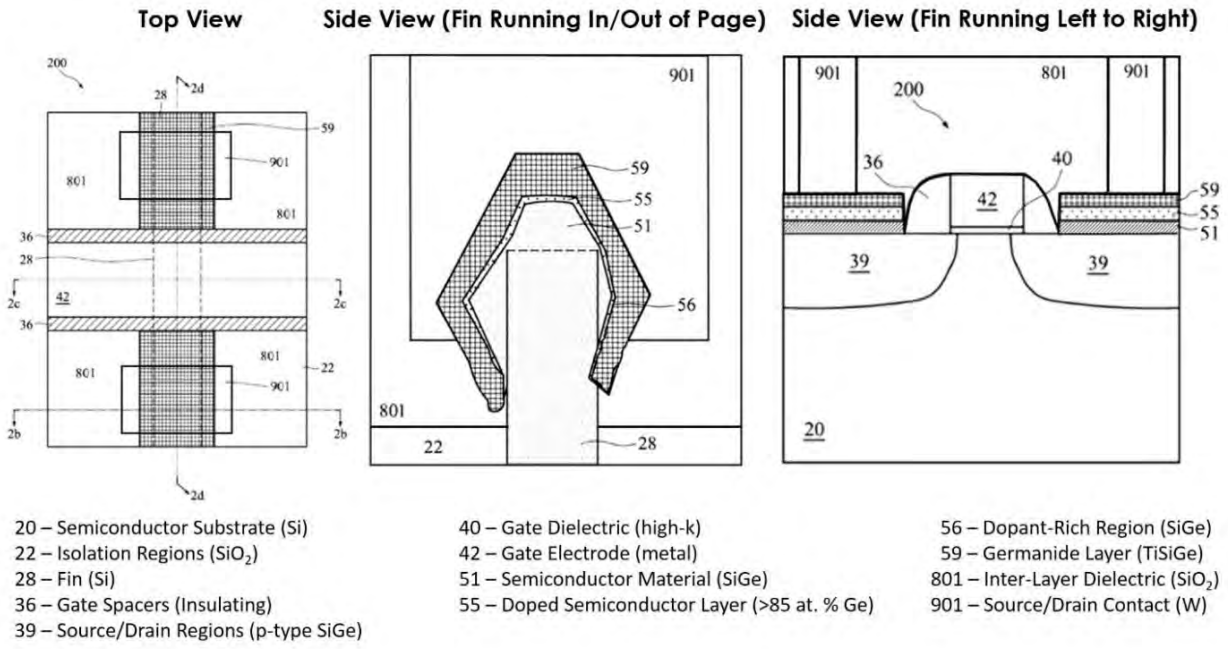
[611] *Id.*; *see also supra* Section VI.F.

[612] *Tung* ¶ [0064].

A person of ordinary skill in the art also would have found *Yu*'s source/drain contact structure, which is wider than the fin, to be desirable for *Tung*'s and *Brask*'s FinFETs (and the combined *Tung-Brask* FinFET discussed in Section IX.C.1) because *Yu*'s source/drain contacts reduce contact resistance and minimize variations in contact resistance due to photolithography misalignment.[613]

560. A person of ordinary skill in the art, therefore, would have found a structure like the exemplary one illustrated below to be obvious by combining *Yu*'s teachings (specifically, *Yu*'s ILD 801 and contacts 901) with the *Tung-Brask* FinFET structure discussed in Section IX.C.1. The figure on the left below (modeled on *Tung*'s Fig. 2a) shows an approximate a plan-view cross-section of the *Tung-Brask-Yu* device, with the fin running up/down and the gate running left/right. The middle figure (modeled on *Tung*'s Fig. 4e) shows an approximate side view looking along the fin direction (i.e., the cross-section denoted "2b" in the figure on the left that cuts laterally through the fin). And the figure on the right (modeled on *Tung*'s Fig. 2d) shows an approximate side view with the fin running in the left/right direction (i.e., the cross-section denoted "2d" in the figure on the left that cuts longitudinally through the middle of the fin).

[613] *Yu* ¶ [0037]; *see also id.* ¶¶ [0004], [0005].



561. In view of the teachings summarized above, a person of ordinary skill in the art would have considered incorporating *Yu*'s teachings in the manner illustrated above to be obvious according to at least four of the obviousness rationales among those I have been asked to consider.

562. First, a person of ordinary skill in the art would have considered the *Tung-Brask-Yu* FinFET to be an example of combining prior art elements according to known methods to yield predictable results. *Tung*'s FinFET structure (including as implemented according to *Brask*'s teachings as discussed in Section IX.C.1) and *Yu*'s FinFET source/drain contacts are prior art elements a person of ordinary skill in the art would have known to combine according to known methods (e.g., applying *Yu*'s ILD and then creating a contact hole and filling it with a contact plug as *Yu* instructs). And a person of ordinary skill in the

art would have expected this to yield predictable results—a completed FinFET device with enhanced channel strain, reduced source/drain contact resistance, and improved tolerance for photolithography misalignment.

563. Second, a person of ordinary skill in the art would have considered the *Tung-Brask-Yu* FinFET to be an example of using a known technique to improve similar devices in the same way. A person of ordinary skill in the art would have known to apply *Yu*'s FinFET source/drain contact structure to the combined *Tung-Brask* FinFET and would have recognized that doing so would improve the combined *Tung-Brask* FinFET by enhancing channel strain, reducing source/drain contact resistance, and improving tolerance for photolithography misalignment.

564. Third, a person of ordinary skill in the art would have considered the *Tung-Brask-Yu* FinFET to be an example of applying a known technique to a known device ready for improvement to yield predictable results. A person of ordinary skill in the art would have understood, as *Tung* and *Brask* expressly acknowledge, that FinFETs like *Tung*'s and *Brask*'s (and the combined *Tung-Brask* FinFET) require source/drain contacts to operate. A person of ordinary skill in the art further would have recognized that *Yu* supplies the necessary source/drain contacts for such FinFETs and that its application to the combined *Tung-Brask* FinFET would predictably enhance channel strain, reduce source/drain contact resistance, and improve tolerance for photolithography misalignment.

565. Fourth, a person of ordinary skill in the art would have thought to implement *Tung*'s and *Brask*'s FinFETs (including the combined *Tung-Brask* FinFET described in Section IX.C.1) according to *Yu*'s teachings based on a teaching, suggestion, or motivation in the prior art. A person of ordinary skill in the art would have been familiar with several teachings, suggestions, or motivations in the prior art, including those from *Tung*, *Brask*, and *Yu* discussed in this section and in view of the teachings I discuss in Section VI.F, as well as the known need to add low-resistance source/drain contacts to such devices. In applying those teachings, suggestions, or motivations as I describe above, a person of ordinary skill in the art would have arrived at the claimed invention.

566. Regardless of the rationale, a person of ordinary skill in the art would have found the combination of *Tung*, *Brask*, and *Yu* discussed above to be obvious.

3. A Person of Ordinary Skill in the Art Would Have Found It Obvious to Use *Tung*'s FinFET, Implemented According to *Brask* and *Yu*, in Computing Devices Like Smartphones

567. By December 2010, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices, like the ones *Tung* discloses (including as implemented according to *Brask*'s teachings as described above) into smartphones, computers, and other typical consumer

electronic devices. To provide a frame of reference for the types of features and peripherals in use at the time, the iPhone 4 was released on June 24, 2010.[614]

568. A person of ordinary skill in the art would have found it obvious to implement FinFETs like *Tung*'s into computing devices like smartphones for at least four of the various obviousness rationales I have been asked to consider.

569. First, a person of ordinary skill in the art would have considered it an example of combining prior art elements according to known methods to yield predictable results. Both *Tung*'s FinFET devices (including as implemented according to the teachings of *Brask* and *Yu* as described above) and typical integrated circuits used in smartphones and other computing devices were prior art elements known to a person of ordinary skill in the art well before December 2010, and combining them would involve only known methods—namely, standard integrated circuit and consumer electronics manufacturing processes. And the combination would yield only predictable results, such as a smartphone or other computing device that includes a circuit board with integrated circuits containing FinFETs.

570. Second, a person of ordinary skill in the art would have considered it an example of using a known technique to improve similar devices in the same

[614] *See* https://www.apple.com/newsroom/2010/06/07Apple-Presents-iPhone-4.

way. A person of ordinary skill in the art would have known how to incorporate FinFET devices like *Tung*'s (including as implemented according to the teachings of *Brask* and *Yu* as described above) into the typical integrated circuits used in smartphones and other computing devices, and he or she would have been able to incorporate *Tung*'s FinFET devices (including as implemented according to the teachings of *Brask* and *Yu* as described above) into such integrated circuits to improve the speed and performance of smartphones and other computing devices, just as any improved FET device would.

571. Third, a person of ordinary skill in the art would have considered this to be an example of applying a known technique—using FET devices like *Tung*'s FinFETs (including as implemented according to the teachings of *Brask* and *Yu* as described above) in integrated circuits—to a known device, such as a smartphone or computing device, that was ready for improvement. A person of ordinary skill in the art would have recognized that such devices are continually being improved by semiconductor scaling, as well as the fact that *Tung* and *Brask* would further that trend. For example, a person of ordinary skill in the art would have recognized that using *Tung*'s FinFETs in smartphones and other computing devices should increase switching speeds and reduce power consumption and heating due to less source/drain contact resistance.

572. Fourth, a person of ordinary skill in the art, knowing of the motivation in the industry to improve smartphones and other computing devices, would have been led to incorporate *Tung*'s FinFET devices (including as implemented according to the teachings of *Brask* and *Yu* as described above) into integrated circuits for use in smartphones and other typical computing devices. By doing so, the person of ordinary skill in the art would have arrived at a smartphone or other typical computing device that includes such FinFETs.

573. Regardless of the rationale, a person of ordinary skill in the art would have found it obvious to use devices like *Tung*'s (including as implemented according to the teachings of *Brask* and *Yu* as described above) in smartphones or other computing devices. In fact, it would have been a given; it is the primary application of all FETs and the reason FinFETs were developed in the first place.

4. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 1 Obvious

a. Claim Element [1.0]: The Preamble

574. Claim 1 recites "[a]n integrated circuit structure." *Tung*, implemented according to the teachings of *Brask* and *Yu*, is "[a]n integrated circuit structure."

575. *Tung* describes "[s]emiconductor devices [that] comprise integrated circuits" like "field-effect transistors (FETs), such as metal oxide semiconductor (MOS) transistors."[615] Figure 4e below illustrates *Tung*'s FinFET.

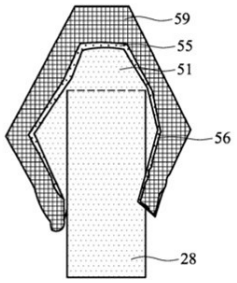
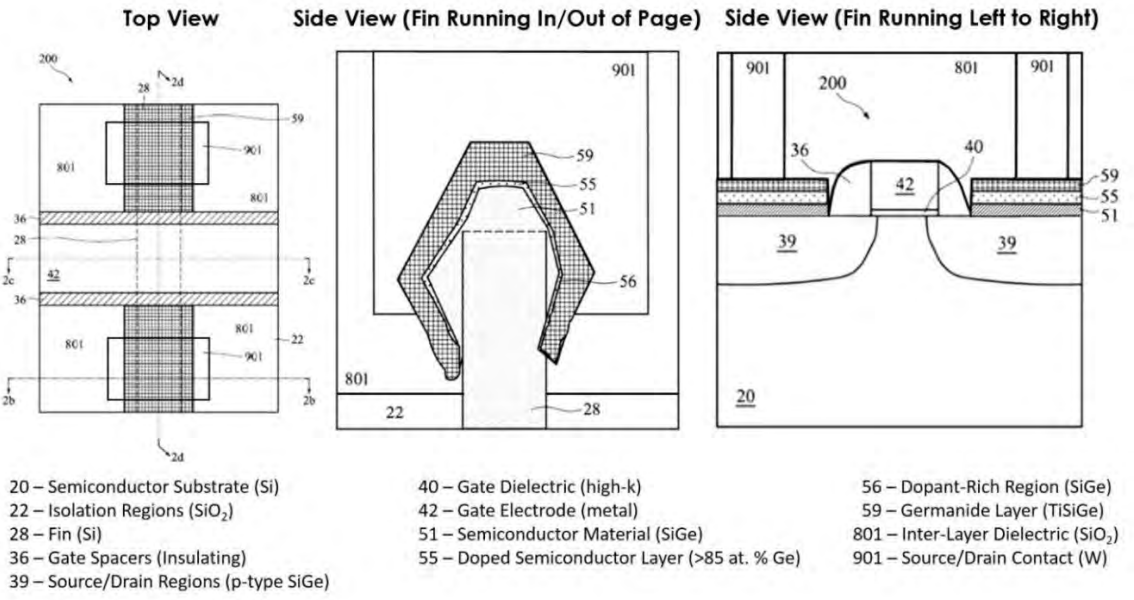


FIG. 4e

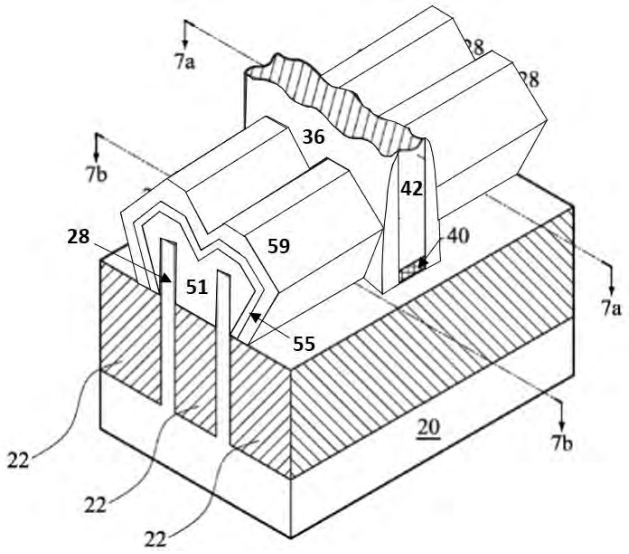
576. As I explain in Sections IX.C.1 and IX.C.2, a person of ordinary skill in the art would have found it obvious to implement *Tung*'s FinFET in the way illustrated below, which is also "[a]n integrated circuit structure" as claimed.



Tung* Implemented According to *Brask* and *Yu

[615] *Tung* ¶ [0003]; *see also id.* at Title, Abstract, ¶¶ [0003]-[0006], [0021]-[0082], Figs. 1a-16.

In an orthographic view, without the additional ILD layer 801 or contact plugs 901 provided by *Yu*, *Tung*'s FinFET would resemble something like the structure below (a more realistic depiction of *Tung*'s Fig. 16, although the individual fins may or may not merge[616]):



577. Because *Tung* teaches a FinFET, and because *Tung*'s FinFET implemented using *Brask*'s and *Yu*'s teachings as I describe in Sections IX.C.1 and IX.C.2 is also a FinFET, a person of ordinary skill in the art would have understood the *Tung-Brask-Yu* combination to provide for "an integrated circuit" as claimed.

578. A person of ordinary skill in the art would have recognized that *Tung*'s semiconductor devices, including when implemented according to *Brask* and *Yu* as described in Section IX.C.1 and IX.C.2, are "[s]emiconductor devices

[616] *Tung* ¶¶ [0058], [0078].

[that] comprise integrated circuits."[617] Since such structures would be incorporated into an integrated circuit, a person of ordinary skill in the art would have understood the combination of *Tung*, *Brask*, and *Yu* contemplates "an integrated circuit."

b. Claim Element [1.1]: Fin

579. Claim 1 recites "a fin comprising silicon." The asserted combination of *Tung*, *Brask*, and *Yu* includes "a fin comprising silicon."

580. I have annotated *Tung*'s Figure 4e below to illustrate the claimed "fin comprising silicon" in the asserted combination of *Tung*, *Brask*, and *Yu*. The claimed "fin" includes at least three layers: fin 28, semiconductor material 51, and doped semiconductor layer 55.

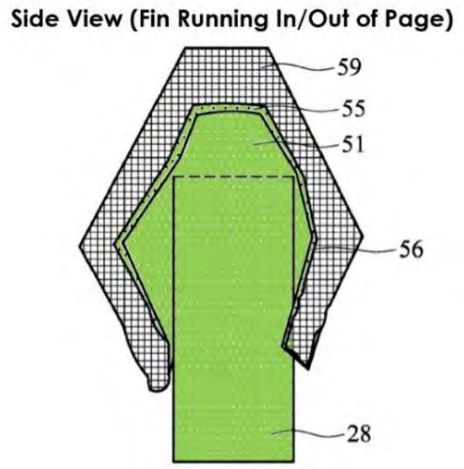


FIG. 4e

[617] *Id.* ¶ [0003].

As shown here, *Tung*'s "fin 28" is made from Si or low-Ge content SiGe for pFETs.[618] Semiconductor material 51 of *Tung*'s FinFET is made of SiGe and, when implemented according to *Brask*, has a graded Ge composition.[619] And doped semiconductor layer 55 is made of a Ge layer (by which I mean a layer with more than about 85 atomic % Ge in the asserted combination).[620] The figure above provides a side view, with the fin direction running into and out of the page. Fin 28 runs the entire length of the transistor, including the channel region under the gate, whereas semiconductor material 51 and doped semiconductor layer 55 are confined to the source/drain areas of the fin on either side of the gate structure.

581. Because *Tung* teaches a FinFET with a Si-containing fin, and because *Tung*'s FinFET implemented using *Brask*'s and *Yu*'s teachings as I describe in Sections IX.C.1 and IX.C.2 also includes a Si-containing fin, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* includes "a fin comprising silicon" as claimed.

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[618] *See Tung* ¶¶ [0023], [0024], [0048]-[0051]; *see also Brask* at 5:26-34 (describing "semiconductor bod[ies]" and "semiconductor film" of Si or SiGe); *Yu* ¶ [0021] (describing fin 201). Although semiconductor material 51 will be grown in the source/drain regions of fin 28, the channel region is made exclusively of the material comprising fin 28. To strain the channel, fin 28 would need to contain less Ge than semiconductor material 51.

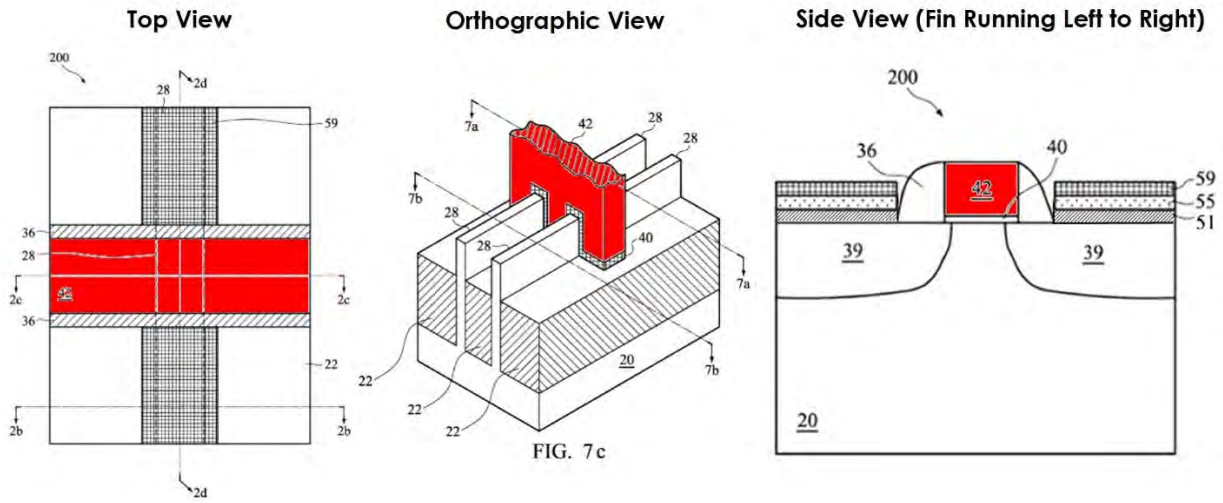
[619] *See supra* Section IX.C.1.b; *Tung* ¶¶ [0039]-[0041], [0074]; *Brask* at 10:20-49.

[620] *See supra* Sections VI.C, IX.C.1.a, note 38; *Tung* ¶¶ [0058], [0078].

c. Claim Element [1.2]: Gate Electrode

582. Claim 1 recites "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side." The asserted combination of *Tung*, *Brask*, and *Yu* includes "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side."

583. Below, I provide several annotated figures to illustrate the claimed "gate electrode over the fin" in red.[621] The figure on the left is an annotated version of *Tung*'s Figure 2a, and the figure in the middle is an annotated version of *Tung*'s Figure 7c. The figure on the right below is based on *Tung*'s Figure 2d, except I have added *Tung*'s semiconductor material 51 to show where it is located.[622]



***Tung* Implemented According to *Brask* (*Yu*'s Additions Not Shown)**

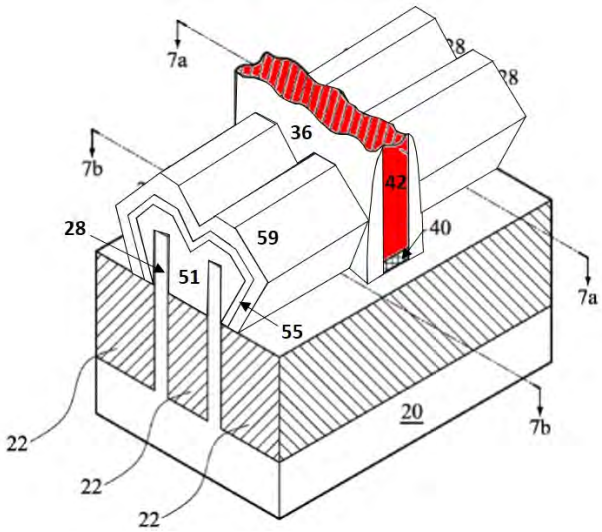
[621] *See Tung* ¶¶ [0025], [0033], [0053]-[0055], [0065], Figs. 2a, 2d, 7a, 7c, 11c; *Brask* at 6:56-7:40, 26:19-51, Figs. 1-4C, 5U-5Z; *Yu* ¶ [0026], Figs. 3-10B.

[622] *See Tung* ¶ [0033] (noting the raised source/drain regions are not shown here).

584. The figures above show a FinFET with a gate electrode 42 (in red) over fin 28. The figure on the left provides a plan-view cross-section of the *Tung-Brask* combination (*Yu*'s contact structure not shown). The figure in the middle provides an orthographic view at an intermediate stage of processing. And the figure on the right provides an approximate side view along the "2d" cross-section of the figure on the left. The figures on the left and right represent the asserted combination of *Tung* and *Brask*. The figure in the middle, however, represents the asserted combination as it would appear before forming sidewalls 36 next to the gate electrode or layers 51, 55, and 59 in the source/drain areas of the device on either side of the gate structure.[623] After performing those steps, the *Tung-Brask* combination (without *Yu*'s contacts yet added) would resemble the structure below (a more realistic depiction of *Tung*'s Fig. 16, although the individual fins may or may not merge[624]):

[623] *See, e.g., Tung* ¶ [0023] ("A gate electrode 42 is disposed over the fin 28."); *see also id.* ¶¶ [0033], [0053]-[0055]; *Brask* at 1:7-11, 6:41-7:3, 8:13-26, 8:42-9:13, Figs. 4A, 4B (describing *Brask*'s "gate electrode[s]").

[624] *Tung* ¶¶ [0058], [0078].



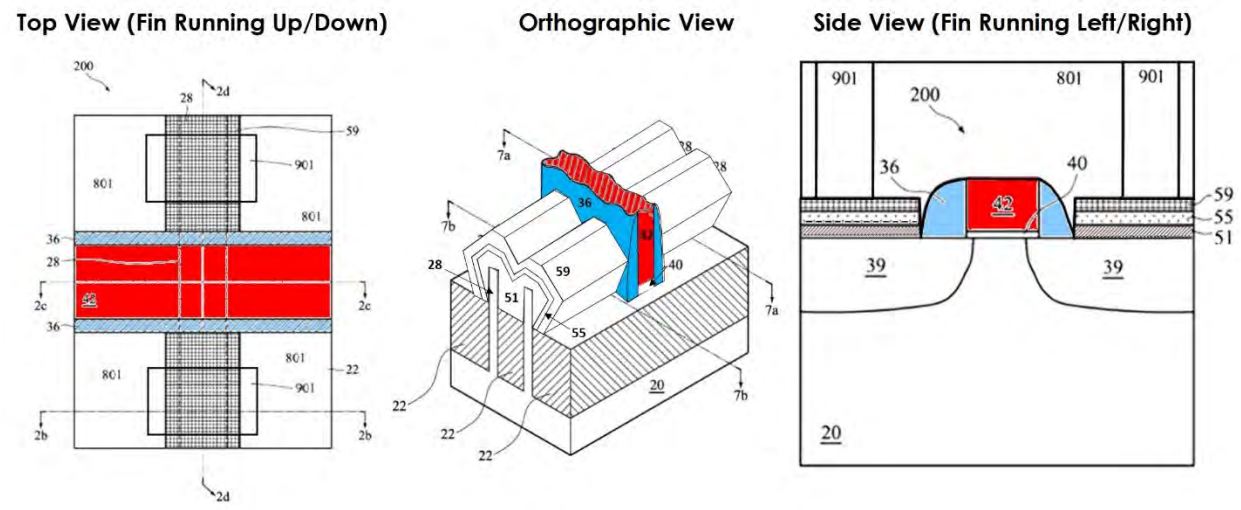
585. As the images above demonstrate, the gate electrode has a first side (the side nearest one of the source/drain regions) and a second side (the side nearest the other source/drain region) that lies opposite the first side.

586. Because *Tung* teaches a FinFET with a gate electrode over the fin and the gate electrode has first/second sides opposite one another, and because the asserted combination of *Tung* and *Yu* described in Sections IX.C.1 and IX.C.2 likewise includes those same features, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* includes "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side" as claimed.

d. Claim Element [1.3]: First Dielectric Spacer

587. Claim 1 recites "a first dielectric spacer along the first side of the gate electrode." The asserted combination of *Tung*, *Brask*, and *Yu* includes "a first dielectric spacer along the first side of the gate electrode."

588. As the figures below illustrate, the asserted combination of *Tung*, *Brask*, and *Yu* is a FinFET device in which standard dielectric gate spacers 36 (blue) are "formed on the sidewalls of the gate dielectric 40 and the gate electrode 42" to isolate gate electrode 42 from other conductive regions.[625] As shown here, dielectric gate spacers 36 (blue) line the first and second sides of gate electrode 42 (red).



589. As I explain in Sections IX.C.1 and IX.C.2, a person of ordinary skill in the art would have found it obvious to implement *Tung*'s FinFET device according to *Brask* and *Yu* as illustrated in the figures above, which I created for illustrative purposes. The figure on the left (modeled after *Tung*'s Fig. 2a) provides an approximate plan-view cross-section of the device, and the figure on the right

[625] *Tung* ¶ [0055]; *see also id.* ¶¶ [0023], [0026], [0036], [0065], [0070], Figs. 2a, 2d, 11c; *Brask* at 9:61-10:49, 21:31-22:45, Figs. 4A, 4B, 5O-5Z; *Yu* ¶ [0027], Figs. 6-10B.

(modeled after *Tung*'s Fig. 2d) provides an approximate side view along the "2d" cross-section of the figure on the left. These figures represent the final structure of the *Tung-Brask-Yu* combination. The figure in the middle (modeled after *Tung*'s Figures 4e, 7C, and 16)[626] represents the *Tung-Brask* combination before *Yu*'s contact structures are added.

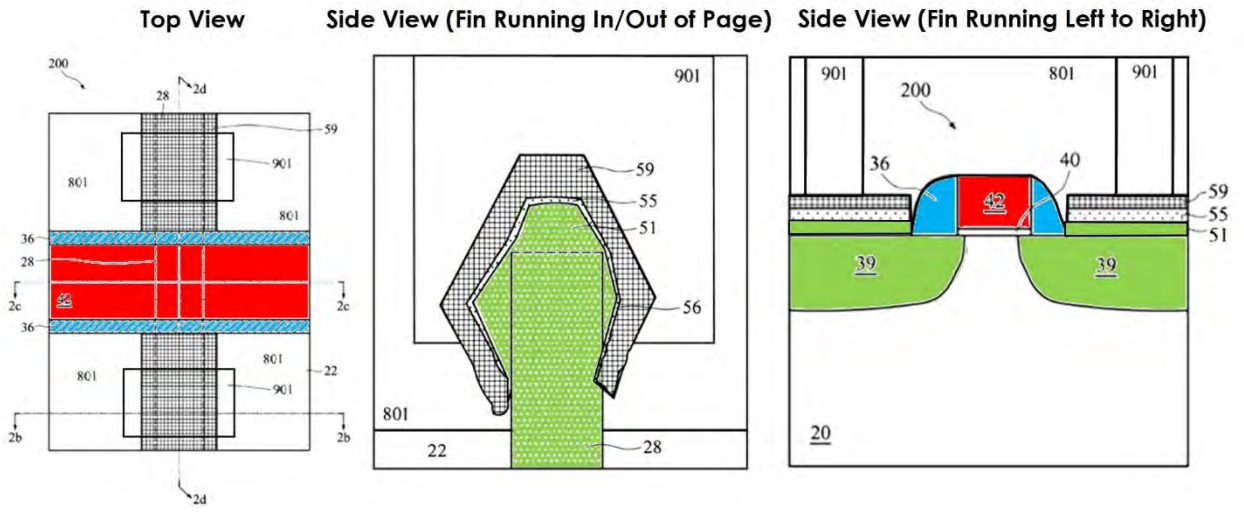
590. Because *Tung* teaches a FinFET with dielectric spacers formed along the sides of the gate electrode, and because the asserted combination of *Tung*, *Brask*, and *Yu* described in Sections IX.C.1 and IX.C.2 likewise includes the same features, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* incldues "a first dielectric spacer along the first side of the gate electrode" as claimed.

e. Claim Element [1.4]: First Source/Drain Region

591. Claim 1 recites "a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer." The asserted combination of *Tung*, *Brask*, and *Yu* includes "a first source or drain region in the fin proximate a first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer."

[626] The individual fins may or may not merge. *Tung* ¶¶ [0058], [0078].

592. Below, I have provided several annotated figures to illustrate the claimed "first source or drain region" in green, the claimed "gate electrode" in red, and the claimed "dielectric spacer" in blue.[627] Although certain features have been added according to the combination described in Sections IX.C.1 and IX.C.2, the figure on the left is based on *Tung*'s Figure 2a, the figure in the middle is based on *Tung*'s Figure 4e, and the figure on the right is based on *Tung*'s Figure 2d.



Tung* Implemented According to *Brask* and *Yu

593. The figures above demonstrate that the FinFET of the asserted combination has first and second source/drain regions (green)[628] proximate to the

[627] *See Tung* ¶¶ [0023], [0033], [0057], [0074], [0078], Figs. 2a-2d, 4a-4e, 6a-9a, 10, 11a, 11c, 16; *Brask* at 7:60-8:12, 20:20-53, 22:52-23:4, Figs. 1, 2A, 3-4C, 5M-5Z; *Yu* ¶¶ [0028], [0029], Figs. 3-10B.

[628] *Tung*'s source/drain regions 39 comprise the p-type portions of fin 28, all of semiconductor material 51, and optionally all of doped semiconductor layer 55. *See supra* Section IX.C.1; *Tung* ¶ [0033] ("[I]in various embodiments, the doped semiconductor layer 55 may be formed as or over a raised source/drain region, and

first and second sides of the gate electrode (red). Additionally, they show that a portion of the source/drain regions (green)[629] lies beneath the dielectric spacers (blue). The figure on the left provides a plan-view cross-section of the device (fin running up/down).[630] The figure in the middle provides an approximate side view along the "2b" cross-section of the figure on the left, (fin running into/out of the page). And the figure on the right provides an approximate side view along the "2d" cross-section of the figure on the left (fin running left/right).

594. Because *Tung* teaches a FinFET with source/drain regions in the fin near the sides of the gate electrode and a portion of the source/drain regions underneath the gate spacers, and because the asserted combination of *Tung*, *Brask*, and *Yu* described in Sections IX.C.1 and IX.C.2 has those same features, a person of ordinary skill in the art would have understood that the combination of *Tung*, *Brask*, and *Yu* includes "a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer" as claimed.

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disposed over the source/drain regions 39."), [0075] ("[E]ach fin 28 forms a separate raised source/drain region comprising the semiconductor material 51.").

[629] The portions of *Tung*'s source/drain regions 39 underneath the gate spacers include the source/drain extension regions. *See Tung* ¶¶ [0057], [0067], [0073], Figs. 2d, 11c; *see also Brask* at 9:61-10:11, 11:15-31, 20:9-53, Fig. 4B.

[630] The source/drain regions in this figure are hidden by TiSiGe layer 59.

f. Claim Element [1.5]: Graded Ge Concentration of the First Source/Drain Region

595. Claim 1 recites "wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combination of *Tung*, *Brask*, and *Yu* is a structure "wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%."

596. *Tung*'s FinFET has "source/drain regions 39" that are "disposed within the fins 28," as Figures 4e and 11a below illustrate.[631]

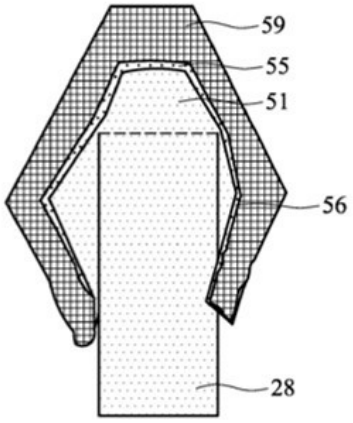


FIG. 4e

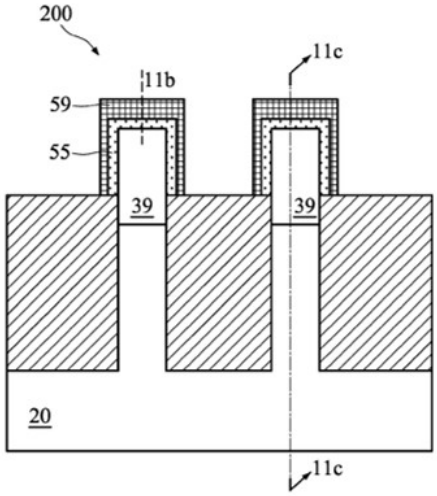


FIG. 11a

As *Tung* explains, semiconductor material 51 forms a "raised source/drain" portion of "the source/drain regions 39."[632] *Tung* also explains that "semiconductor

[631] *Tung* ¶¶ [0023], [0033], [0057].

[632] *Id.* ¶ [0074]; *see also id.* ¶¶ [0033], [0078].

material 51 is formed of . . . silicon germanium (SiGe)."[633] Accordingly, *Tung*'s source/drain regions 39 "comprise[] silicon and germanium" as claimed.

597. The combination of *Tung*, *Brask*, and *Yu* also has "a germanium concentration graded to a concentration in excess of 50%." For the reasons I explain in Section IX.C.1, a person of ordinary skill in the art would have found it obvious to employ a Ge concentration in SiGe semiconductor material 51 that exceeds 50 atomic %. *Tung* confirms that a person of ordinary skill in the art would have understood the source/drain contact resistance depends heavily on the Schottky barrier at the interface between metal-semiconductor layer 59 and doped semiconductor layer 55.[634] And as I explain in Section IX.C.1.a, a person of ordinary skill in the art would have understood that employing large amounts of Ge in doped semiconductor layer 55—in particular, a concentration above about 85 atomic %[635]—would lower the Schottky barrier and thereby minimize the source/drain contact resistance.

598. As I further explain in Section IX.C.1.b, a person of ordinary skill in the art would have found it obvious, as *Brask* instructs, to grade the Ge

[633] *Id.* ¶ [0074].

[634] *Id.* ¶ [0034].

[635] *See id.* ¶¶ [0058], [0078]; *supra* Sections VI.C, IX.C.1.a, note 38.

concentration in SiGe semiconductor material 51.[636] Specifically, a person of ordinary skill in the art would have understood *Brask*'s instruction that SiGe layer 410 (which is analogous to *Tung*'s SiGe semiconductor material 51) may "be graded" refers to the concept of grading the Ge concentration up from a level compatible with the underlying fin region. In *Tung*, where the overlying doped semiconductor layer 55 has a greater concentration to reduce the Schottky barrier height, a person of ordinary skill in the art would have understood that semiconductor material 51 should be graded from a level compatible with underlying Si fin 28, for example, to a level compatible with overlying doped Ge semiconductor layer 55 (by which I mean a layer with more than about 85 atomic % Ge). Again, a person of ordinary skill in the art would have recognized that doing so would minimize dislocations and maintain stress applied to the channel region.[637]

599. Thus, a person of ordinary skill in the art implementing *Tung*'s FinFET would have found it obvious grade the Ge concentration in SiGe semiconductor material 51 "to a concentration in excess of 50%"—namely, to a level compatible with Ge semiconductor layer 55 (having more than about 85 atomic % Ge). The asserted combination of *Tung*, *Brask*, and *Yu* therefore includes

[636] *See, e.g.*, *Brask* at 10:20-49.

[637] *See supra* note 18.

a "first source or drain region" that "comprises silicon and germanium" and has "a germanium concentration graded to a concentration in excess of 50%" as claimed.

g. Claim Element [1.6]: Second Dielectric Spacer

600. Claim 1 recites "a second dielectric spacer along the second side of the gate electrode." The asserted combination of *Tung*, *Brask*, and *Yu* includes "a second dielectric spacer along the second side of the gate electrode" for the same reasons I discuss in Section IX.C.4.d regarding claim element [1.3].

h. Claim Element [1.7]: Second Source/Drain Region

601. Claim 1 recites "a second source or drain region in the fin proximate a second side of the gate electrode, a portion of the first source or drain region beneath the second dielectric spacer." The asserted combination of *Tung*, *Brask*, and *Yu* includes "a second source or drain region in the fin proximate a second side of the gate electrode, a portion of the first source or drain region beneath the second dielectric spacer" for the same reasons I discuss in Section IX.C.4.e regarding claim element [1.4]. The source/drain regions in FET devices like this are identical, which is why they are generally referred to as "source/drain" regions.

i. Claim Element [1.8] Graded Germanium Concentration of the Second Source or Drain Region

602. Claim 1 recites "wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combination of *Tung*, *Brask*, and *Yu*

is a structure "wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%" for the same reasons I discuss in Section IX.C.4.f regarding claim element [1.5]. The source/drain regions in FET devices like this are identical, which is why they are generally referred to as "source/drain" regions.

j. Claim Element [1.9]: Interlayer Dielectric

603. Claim 1 recites "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region." The asserted combination of *Tung*, *Brask*, and *Yu* includes "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region."

604. As I explain in Section IX.C.1, a person of ordinary skill in the art also would have found it obvious to implement the *Tung-Brask* FinFET by applying *Yu*'s source/drain contacts. *Yu*'s source/drain contact structure includes, among other things, an interlayer dielectric layer (ILD) 801 and contact plugs

901—a nearly universal approach at the time.[638] As Figure 9A shows, *Yu*'s contacts 901 are formed in openings of ILD layer 801 and extend down to metal-semiconductor layer 605 on the source/drain regions of the fin.[639] As Figure 9B shows, the contact holes expose only a portion of each source/drain region.

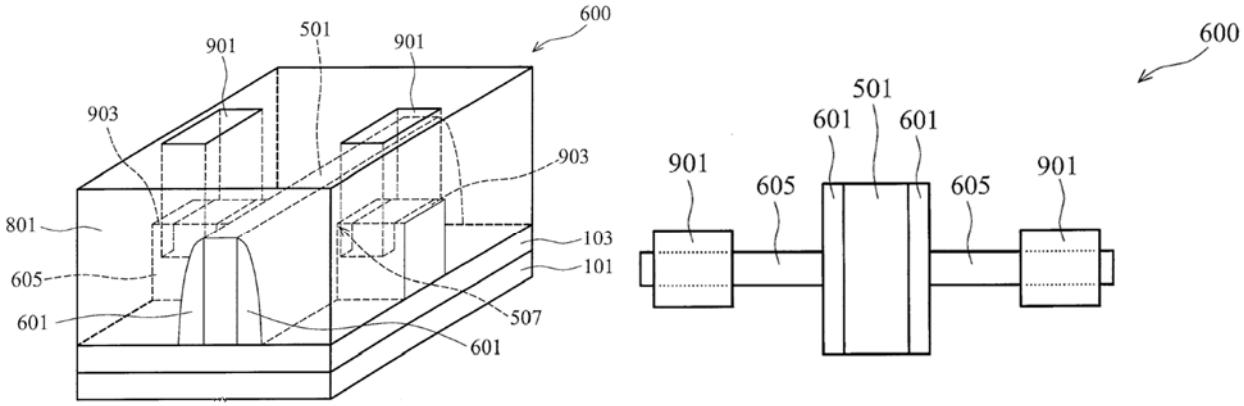


FIG. 9A FIG. 9B

605. *Yu* explains that "photoresist material is utilized to create a patterned mask to define contacts 901."[640] Then, an "etch process is continued until an upper surface 903 of the fin 201 containing the source/drain regions 603 and at least a portion of the sidewalls of the fin 201 are exposed."[641] "Contacts 901 are then formed so as to contact the exposed surfaces of the fin 201."[642]

[638] *See supra* Section VI.F.

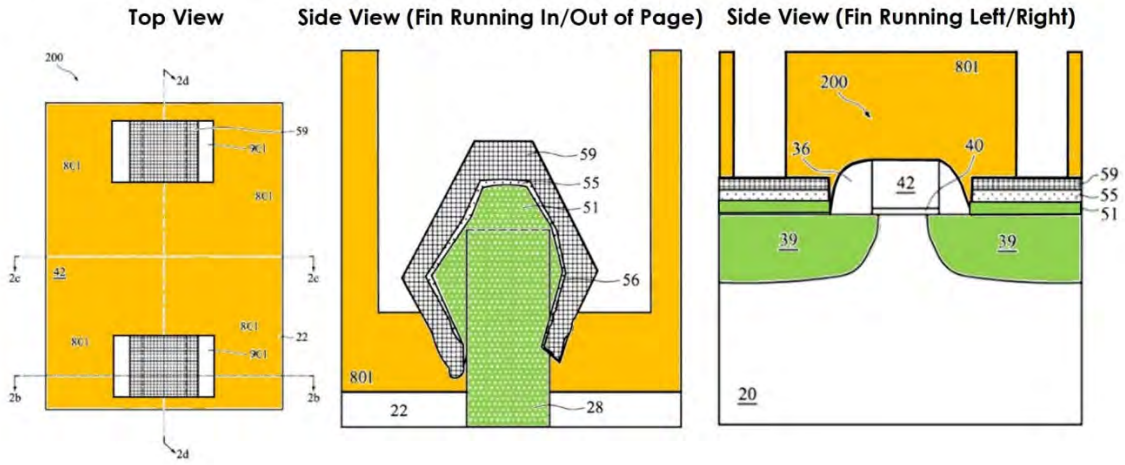
[639] *Yu* ¶¶ [0034]-[0036]; *see also id.* at Figs. 8, 9A, 9B.

[640] *Id.* ¶ [0035].

[641] *Id.* ¶ [0036].

[642] *Id.* ¶ [0037].

606. As I explain in Section IX.C.2, a person of ordinary skill in the art would have understood that *Yu*'s teachings are consistent with *Tung*'s statement that "[c]ontacts (not shown) are subsequently formed on the metal silicide layer 59" by proceeding with "conventional processing."[643] A person of ordinary skill in the art also would have found *Yu*'s FinFET source/drain contacts to be desirable for *Tung*'s and *Brask*'s FinFETs (including the combined *Tung-Brask* FinFET) because *Yu*'s contacts reduce contact resistance and minimize contact resistance variations in due to misalignment during photolithography.[644]



Tung* Implemented According to *Brask* and *Yu

607. A person of ordinary skill in the art thus would have found it obvious to implement the *Tung-Brask* FinFET by applying *Yu*'s FinFET contact structure as illustrated above.[645] These images represent the *Tung-Brask-Yu* FinFET prior to

[643] *Tung* ¶ [0064].

[644] *Yu* ¶ [0037].

[645] *See supra* Section IX.C.2.

depositing contacts 901. The figure on the left (modeled after *Tung*'s Fig. 2a) provides an approximate plan-view cross-section. The figure in the middle (modeled after *Tung*'s Fig. 4e) provides an approximate side view along the "2b" cross-section in the figure on the left. And the figure on the right (modeled after *Tung*'s Fig. 2d) provides an approximate side view along the "2d" cross-section of the figure on the left.

608. As shown above, the *Tung-Brask-Yu* FinFET includes a an interlayer dielectric layer 801 (orange) formed over the source/drain regions (green). The dielectric layer has openings (contact holes) that expose only portions of the source/drain regions (green). Thus, the *Tung-Brask-Yu* FinFET includes "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region."

609. Because *Yu* teaches a FinFET with an interlayer dielectric that has contact openings exposing only a portion of each source/drain region, and because the asserted combination of *Tung*, *Brask*, and *Yu* described in Sections IX.C.1 and IX.C.2 includes those same features, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* includes "a dielectric layer over the first source or drain region and over the second source or

drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region" as claimed.

k. Claim Element [1.10]: First Germanide Layer

610. Claim 1 recites "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium." The asserted combination of *Tung*, *Brask*, and *Yu* includes "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium."

611. As I explain in Section IX.C.1, a person of ordinary skill in the art seeking to minimize contact resistance in *Tung*'s device[646] would have found it obvious to implement metal-semiconductor layer 59 as a TiSiGe layer over *Tung*'s p-type source/drain regions 39. *Tung* explains, for example, that "the doped semiconductor layer 55 comprises . . . doped SiGe, or doped Ge."[647] *Tung* further explains that "[t]he silicide metal 57 comprises a suitable metal," such as "Ti," and

[646] *See, e.g.*, *Tung* ¶¶ [0005], [0006], [0021], [0027], [0029], [0031], [0032], [0034], [0061], [0070], [0078].

[647] *Id.* ¶¶ [0058], [0078]; *see also supra* Sections VI.C, IX.C.1.a.ii, note 38 (explaining why a person of ordinary skill in the art would have been motivated to use a layer with > 85 atomic % Ge as doped semiconductor layer 55).

"is deposited over the doped semiconductor layer 55."[648] Then, *Tung* explains, the device is annealed to cause a reaction between the metal atoms in metal layer 57 and the semiconductor atoms in doped semiconductor layer 55 (and any atoms that may diffuse from semiconductor material 51 if doped semiconductor layer 55 is thin enough).[649] That is, TiSiGe forms because the Ti atoms in titanium metal 57 chemically react with the Si and Ge atoms in doped semiconductor layer 55 and any atoms that may diffuse from semiconductor material 51.

612. Although *Tung* calls this layer a metal "silicide" layer, this is being used as a generic term in the manner I discuss in Section VII.D. Although *Tung* teaches that doped semiconductor layer 55 can be "doped silicon," it also teaches that doped semiconductor layer 55 can be "doped SiGe" or "doped Ge."[650] A person of ordinary skill would not have understood the metal-semiconductor compound that results when using a doped Ge layer 55, for example, to be a

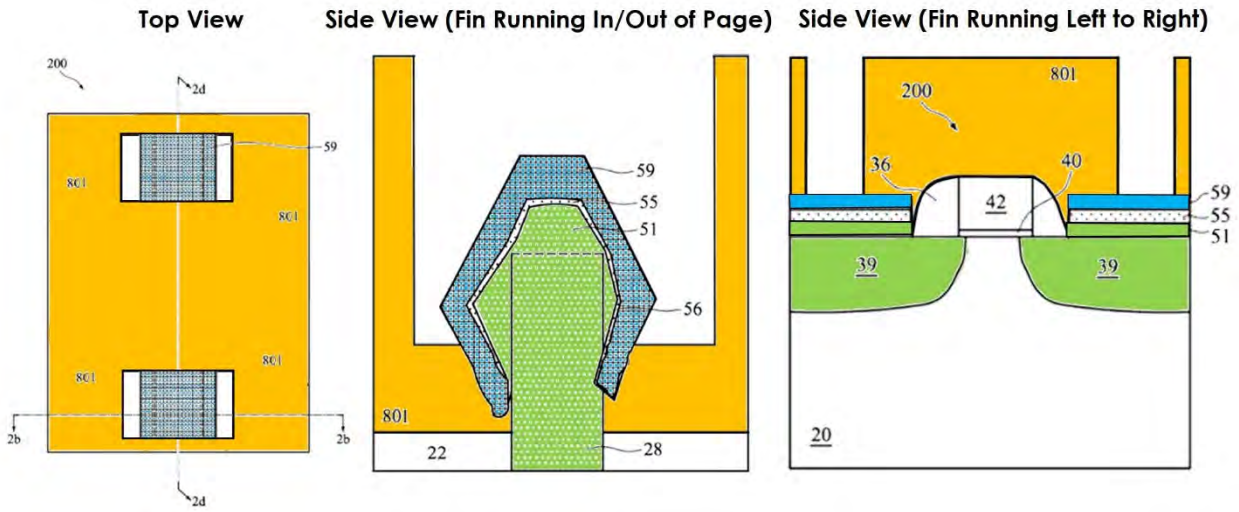
[648] *Tung* ¶¶ [0042], [0060], [0061], [0080].

[649] *Id.* ¶¶ [0041]-[0043], [0045], [0063]-[0065], [0081]; *see also* S. Zaima & Y. Yasuda, *Study of Reaction and Electrical Properties at Ti/SiGe/Si(100) Contacts for Ultralarge Scale Integrated Applications*, Journal of Vacuum Science & Technology B, vol. 16, at 2625-27, Fig. 1 (1998) ("Silicon atoms preferentially react with Ti atoms at annealing temperatures below 300 °C and Ge atoms start to react above 400 °C."); S. Gaudet et al., *Thin Film Reaction of Transition Metals with Germanium*, Journal of Vacuum Science & Technology A, vol. 24, no. 3 at Fig. 5 (2006) (showing reaction temperatures for numerous metal-Ge compounds).

[650] *Tung* ¶¶ [0058], [0078].

"silicide" in the strict sense of the term. A person of ordinary skill in the art would have understood it is a "germanide" as the '281 Patent uses that term.

613. Under what I believe to be the correct claim construction of "germanide layer," such a TiSiGe layer constitutes a "germanide layer" because it is a "a germanium layer[651] metalized with one or more metals [Ti]." Additionally, under Daedalus's proposed construction, it is a "thickness of material, comprising germanium and a metal." A person of ordinary skill in the art would have expected such a layer to lower the Schottky barrier height of *Tung*'s p-type source/drain regions and, consequently, reduce contact resistance.[652]



Tung* Implemented According to *Brask* and *Yu

[651] *See id* ¶¶ [0058], [0078]; *supra* Sections VI.C, IX.C.1.a.ii, note 38 (explaining why a person of ordinary skill in the art would have been motivated to use a layer with > 85 atomic % Ge as doped semiconductor layer 55).

[652] *See supra* Sections VI.C, IX.C.1.a.

614. Above, I provide several figures to illustrate the claimed "germanide layer" of the *Tung-Brask-Yu* FinFET as described in Sections IX.C.1 and IX.C.2. These figures illustrate the FinFET just before depositing *Yu*'s contacts 901. The figure on the left (modeled on *Tung*'s FIG. 2a) provides an approximate plan-view cross-section of the device.[653] The figure in the middle (modeled on *Tung*'s FIG. 4e) provides an approximate side view along the "2b" cross-section of the figure on the left. And the figure on the right (modeled on *Tung*'s FIG. 2d) provides an approximate side view along the "2d" cross-section of the figure on the left. As these figures show, the *Tung-Brask-Yu* FinFET includes a TiSiGe layer 59 (blue) located in the openings of ILD layer 801 (orange; the openings for *Yu*'s contact plugs 901) and over the portions of *Tung*'s p-type source/drain regions (green) in the exposed areas.[654]

615. TiSiGe layer 59 constitutes a "first germanide layer in the first opening and over the portion of the first source or drain region" regardless of how the term "germanide layer" is interpreted.[655] Additionally, TiSiGe layer 59 includes

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[653] The source/drain regions in Figure 2a are under TiSiGe layer 59.

[654] *See supra* Section IX.C.2; *Tung* ¶¶ [0042]-[0045], [0058], [0061], [0078], [0080]; *Brask* at 10:50-64, 23:35-56, Figs. 4A, 4B.

[655] *Tung*'s source/drain regions 39 comprise the p-type portions of fin 28, all of semiconductor material 51, and optionally all of doped semiconductor layer 55. *See supra* Section IX.C.1; *Tung* ¶ [0033] ("[I]in various embodiments, the doped semiconductor layer 55 may be formed as or over a raised source/drain region, and

Ti that has "react[ed] with the [Si and Ge in] doped semiconductor layer 55 and form[ed] a metal silicide layer 59."[656]

616. Thus, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* described in Sections IX.C.1 and IX.C.2 includes a TiSiGe germanide layer located in the source/drain contact openings of the ILD and over the exposed portions of the p-type source/drain regions. A person of ordinary skill in the art, therefore, would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* described in Sections IX.C.1 and IX.C.2 includes "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium" as claimed.

l. Claim Element [1.11]: Second Germanide Layer

617. Claim 1 recites "a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium." For the same reasons I discuss in Section IX.C.4.k regarding claim element [1.10], the asserted combination of *Tung*, *Brask*, and *Yu* includes "a second germanide layer in the second opening and

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disposed over the source/drain regions 39."), [0075] ("[E]ach fin 28 forms a separate raised source/drain region comprising the semiconductor material 51.").

[656] *See supra* note 155.

over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium."

m. Claim Element [1.12] First Contact Plug

618. Claim 1 recites "a first contact plug in the first opening and on the first germanide layer." The asserted combination of *Tung*, *Brask*, and *Yu* includes "a first contact plug in the first opening and on the first germanide layer."

619. As I explain in Section IX.C.2, a person of ordinary skill in the art would have found it obvious to implement the *Tung-Brask* FinFET by applying *Yu*'s source/drain contacts. As Figure 9A shows below, *Yu* explains that metal contacts 901 are deposited into an opening etched through ILD layer 801 to expose metal-semiconductor layer 605 in the source/drain portions of fin.[657]

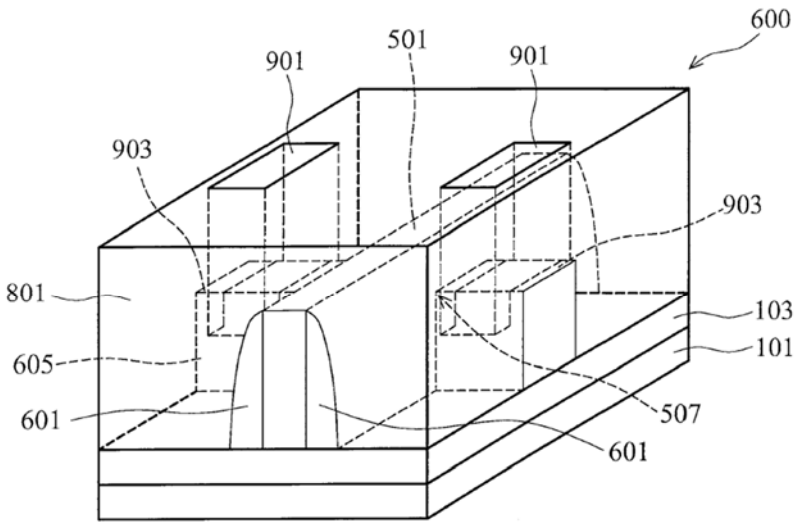
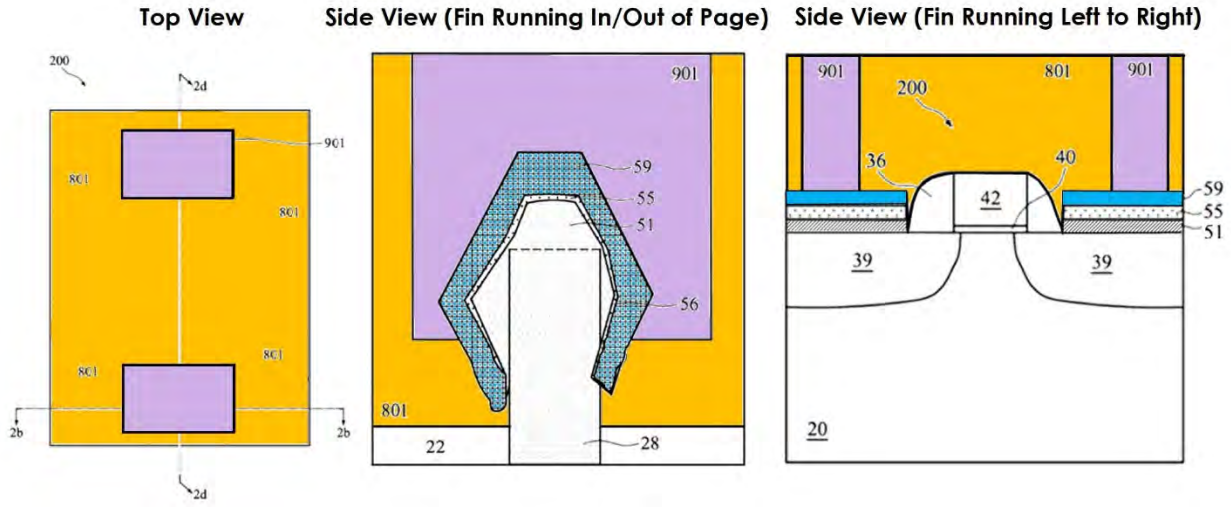


FIG. 9A

[657] *Yu* ¶¶ [0035]-[0040]; *see also id.* at Figs. 8, 9A, 9B.

620. As I also explain in Section IX.C.2, a person of ordinary skill in the art would have understood that *Yu*'s teachings are consistent with *Tung*'s statement that "[c]ontacts (not shown) are subsequently formed on the metal silicide layer 59" by proceeding with "conventional processing."[658] Moreover, a person of ordinary skill in the art would have found *Yu*'s source/drain contact structure, which is wider than the fin, to be desirable for application on *Tung*'s FinFETs (including as implemented according to *Brask*'s teachings as discussed in Section IX.C.1) because it reduces contact resistance and minimizes contact resistance variations due to photolithography misalignment.[659] Accordingly, a person of ordinary skill in the art would have found the *Tung-Brask-Yu* FinFET illustrated below to be obvious.



Tung* Implemented According to *Brask* and *Yu

[658] *Tung* ¶ [0064].

[659] *Yu* ¶ [0037].

621. The figure on the left above (modeled on *Tung*'s FIG. 2a) provides an approximate plan-view cross-section of the device. The figure in the middle (modeled on *Tung*'s FIG. 4e) provides an approximate side view along the "2b" cross-section in the figure on the left. And the figure on the right (modeled on *Tung*'s FIG. 2d) provides an approximate side view along the "2d" cross-section of the figure on the left. As shown above, the *Tung-Brask-Yu* FinFET includes metal contact plugs 901 (purple) formed in openings of the ILD layer 801 (orange) and on the exposed TiSiGe germanide layer 59 (blue) in those areas.[660] Thus, a person of ordinary skill in the art would have understood that the *Tung-Brask-Yu* FinFET includes "a first contact plug in the first opening and on the first germanide layer."

n. Claim Element [1.13] Second Contact Plug

622. Claim 1 recites "a second contact plug in the second opening and on the second germanide layer." The asserted combination of *Tung*, *Brask*, and *Yu* includes "a second contact plug in the second opening and on the second germanide layer" for the same reasons I discuss in Section IX.C.4.m regarding claim element [1.12].

[660] *See Yu* ¶ [0034]-[0040], Figs. 8, 9A, 9B; *Tung* ¶¶ [0042]-[0045], [0058]-[0065], [0078]-[0081], Figs. 2a, 2d, 4e, 11a, 11c, 16.

o. A Person of Ordinary Skill in the Art Would Have Found Claim 1 Obvious

623. Because a person of ordinary skill in the art would have been motivated to combine *Tung*, *Brask*, and *Yu* as I described in Sections IX.C.1 and IX.C.2, because he or she would have reasonably expected to succeed in doing so, and because that combination satisfies each element of claim 1,[661] it is my opinion that claim 1 would have been obvious.

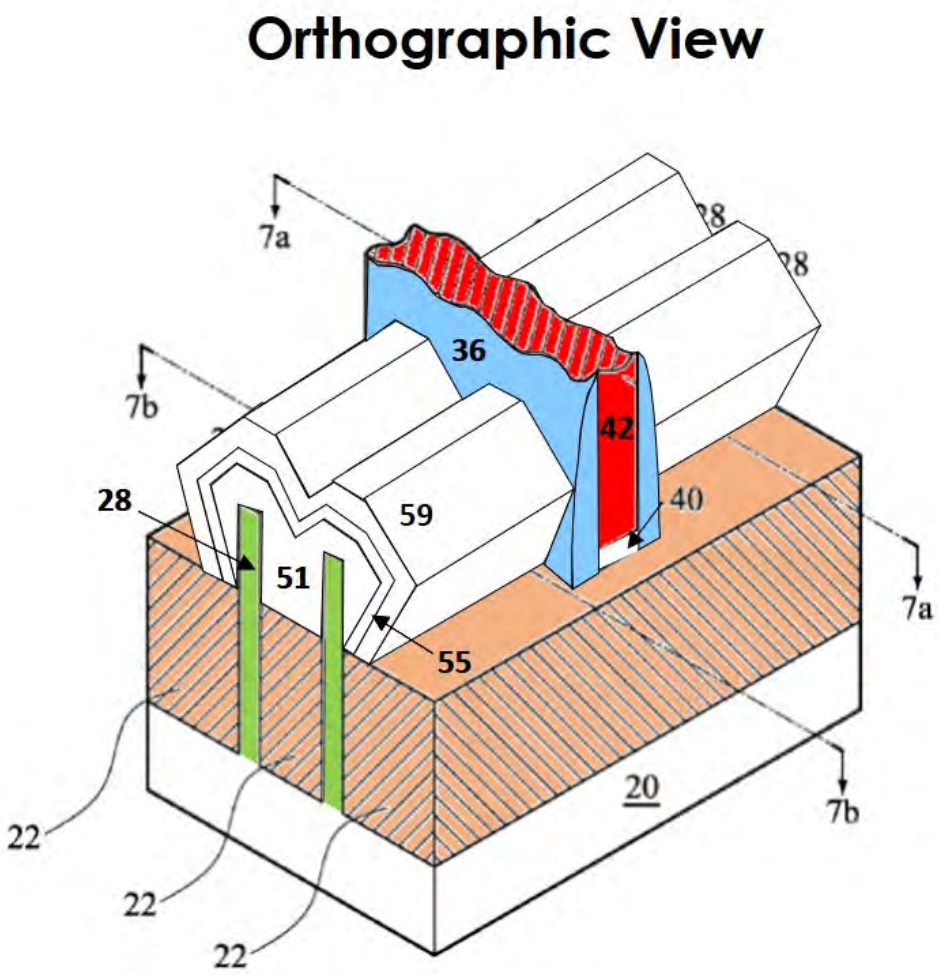
5. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 5 Obvious

624. Claim 5 depends from claim 1. I understand that means claim 5 requires all the same features as claim 1, plus the additional features recited in claim 5. The combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 1 for the reasons I provide in Sections IX.C.4.a-n above.

625. Claim 5 further recites "an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region." The asserted combination of *Tung*, *Brask*, and *Yu* provides a FinFET with "an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric

[661] *See supra* Sections IX.C.2, IX.C.4.a-n.

spacer, and a portion of the second dielectric spacer are over the isolation region" as claimed.



626. The figure above is based on *Tung*'s Figure 7c, except I have added *Tung*'s gate sidewall spacers 36, semiconductor material 51, doped semiconductor layer 55, and metal-semiconductor layer 59.[662] As this figure shows, *Tung*'s

[662] *See Tung* ¶¶ [0033], [0040]-[0045], [0058], [0065], [0074]-[0076], [0078], [0081], Figs. 2a, 4e, 7c, 11a, 16. The individual fins do not necessarily merge as shown, but they may. *See id.* ¶¶ [0058], [0078].

FinFET includes isolation regions 22 (peach),[663] fin portion 28 (green),[664] gate electrode 42 (red),[665] and gate spacers 36 (blue).[666]

627. Since *Tung*'s fin portion 28 (green) extends "above a top surface of the isolation regions 22" (peach) "between about 20 nm and about 100 nm,"[667] a person of ordinary skill in the art would have understood *Tung*'s fins protrude through isolation regions 22 (peach). A person of ordinary skill in the art also would have understood *Tung*'s gate electrode 42 (red) and gate spacers 36 (blue) are formed over the isolation regions 22 (peach). As *Tung*'s Figures 6b and 7c show, for example, gate electrode 42 is formed on top of isolation regions 22,[668] and gate spacers 36 are subsequently formed over the structure after that.[669]

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[663] *See Tung* ¶¶ [0023], [0024], [0047], [0049], [0051], Figs. 2a-2c, 5-9a, 10, 11a, 13-16.

[664] *See id.* ¶¶ [0039], [0051], Figs. 2a-2c, 4a-9a, 10, 11a, 13-16; *Brask* at 5:26-34 (describing "semiconductor bod[ies]" and "semiconductor film" of Si or SiGe); *Yu* ¶ [0021] (describing fin 201). *Tung*'s "fin 28" is only part of the claimed "fin," which further includes semiconductor material 51 and doped semiconductor layer 55. *See Tung* ¶¶ [0039]-[0045], [0058], [0074]-[0081]; *supra* Section IX.C.4.b.

[665] *See Tung* ¶¶ [0023], [0053], [0053]-[0055], [0065], Figs. 2a, 2d, 7c, 11c; *Brask* at 6:56-7:40, 26:19-51, Figs. 1-4C, 5U-5Z; *Yu* ¶ [0026], Figs. 3-10B.

[666] *See Tung* ¶ [0055]; *see also id.* ¶¶ [0023], [0026], [0036], [0065], [0070], Figs. 2a, 2d, 11c; *Brask* at 9:61-10:49, 21:31-22:45, Figs. 4A, 4B, 5O-5Z; *Yu* ¶ [0027], Figs. 6-10B.

[667] *Tung* ¶ [0051]; *see also id.* at Figs. 2b, 2c, 5-9a, 10, 11a, 13-16.

[668] *See id.* ¶ [0053], Figs. 6b, 7c.

[669] *See id.* ¶¶ [0036], [0065], Figs. 2d, 7c, 11c.

628. Because *Tung* teaches a FinFET with a fin that protrudes through isolation regions and a gate electrode and gate spacers formed over isolation regions, and because *Tung*'s FinFET implemented according to *Brask*'s and *Yu*'s teachings as described in Sections IX.C.1 and IX.C.2 includes those same features, a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* includes "an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region" as claimed.

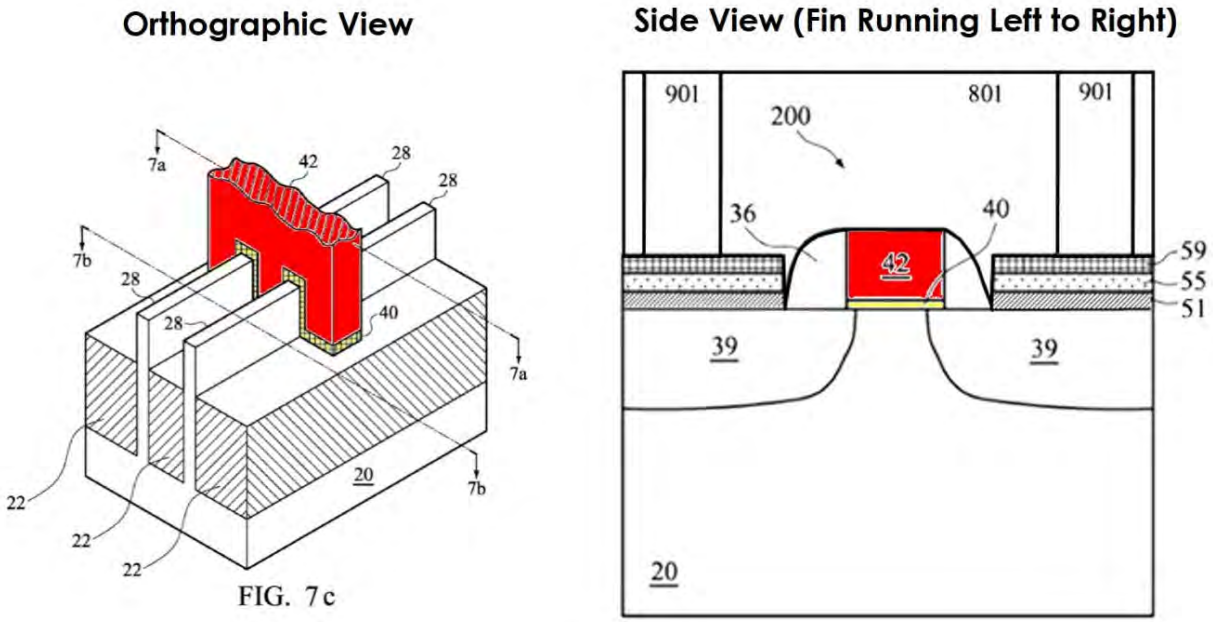
6. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 6 Obvious

629. Claim 6 depends from claim 1. I understand that means claim 6 requires all the same features as claim 1, plus the additional features recited in claim 6. The combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 1 for the reasons I provide in Sections IX.C.4.a-n above.

630. Claim 6 further recites "a gate dielectric layer, wherein the gate electrode is on the gate dielectric layer, wherein the gate dielectric layer comprises a high-k dielectric material, and wherein the gate electrode comprises a metal layer." The asserted combination of *Tung*, *Brask*, and *Yu* provides a FinFET that includes "a gate dielectric layer, wherein the gate electrode is on the gate dielectric

layer, wherein the gate dielectric layer comprises a high-k dielectric material, and wherein the gate electrode comprises a metal layer" as claimed.

631. As *Tung*'s Figures 2d and 7c show below, *Tung*'s FinFET includes a gate dielectric 40 (yellow) underneath gate electrode 42 (red).[670] *Tung* teaches that the "gate dielectric 40 may include . . . high-K dielectrics such as Ta_2O_5. Al_2O_3, HfO, Ta_2O_5 [sic], $SiTiO_3$, HfSiO, HfSiON, ZrSiON, or combinations thereof."[671] *Tung* further teaches that the "gate electrode 42 may be formed of . . . metals such as Ni, Ti, Ta, Hf, or combinations thereof."[672]



[670] *See, e.g.*, *Tung* ¶¶ [0053]-[0055], Figs. 2d, 7c; *see also Brask* at 6:13-7:40, 25:9-34, 26:19-51, Figs. 4A, 4B, 5W; *Yu* ¶¶ [0022]-[0026], Figs. 3-5.

[671] *Tung* ¶ [0054]; *see also Brask* at 6:13-40, 25:9-34; *Yu* ¶¶ [0022], [0023], [0026].

[672] *Tung* ¶ [0055]; *see also Brask* at 6:41-7:40, 26:19-51, *Yu* ¶¶ [0024], [0025].

632. Because *Tung* teaches a FinFET with a high-k gate dielectric layer and a metal gate electrode, and because *Tung*'s FinFET implemented according to *Brask*'s and *Yu*'s teachings as described in Sections IX.C.1 and IX.C.2 includes those same features, a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* includes "a gate dielectric layer, wherein the gate electrode is on the gate dielectric layer, wherein the gate dielectric layer comprises a high-k dielectric material, and wherein the gate electrode comprises a metal layer" as claimed.

7. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 7 Obvious

633. Claim 7 depends from claim 1. I understand that means claim 7 requires all the same features as claim 1, plus the additional features recited in claim 7. The combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 1 for the reasons I provide in Sections IX.C.4.a-n above.

634. Claim 7 further recites "wherein the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets." The asserted combination of *Tung*, *Brask*, and *Yu* provides a FinFET "the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets" as claimed.

635. A person of ordinary skill in the art would have understood that a "facet" here refers to the surface of a semiconductor crystal plane. In the asserted

combination of *Tung*, *Brask*, and *Yu*, the source/drain regions comprise two or more facets.

636. *Tung*'s source/drain regions, for example, include SiGe source/drain material 51 epitaxially grown over rectangular fin 28.[673] In some figures of *Tung*, the source/drain regions are depicted with diamond-shaped facets and in others with rectangular-shaped facets. As I explain in Section VI.G, a person of ordinary skill in the art would have understood that epitaxially grown SiGe source/drain fins, such as these, may have either a diamond or square/rectangular shape.[674] Either way, a person of ordinary skill in the art would have understood that *Tung*'s epitaxial source/drain regions have at least two facets.

637. *Tung* makes clear, however, that SiGe material 51 grows both laterally and vertically "at different rates on different crystal planes," such that it would be

[673] *Tung*'s source/drain regions 39 comprise the p-type portions of fin 28, all of semiconductor material 51, and optionally all of doped semiconductor layer 55. *See* Section IX.C.1; *Tung* ¶ [0033] ("[I]in various embodiments, the doped semiconductor layer 55 may be formed as or over a raised source/drain region, and disposed over the source/drain regions 39."), [0075] ("[E]ach fin 28 forms a separate raised source/drain region comprising the semiconductor material 51.").

[674] *See supra* Section VI.G; *Tung* ¶¶ [0058] ("Depending on the underlying layer (for example, silicon (100) surface versus silicon (110) versus germanium (100), etc.) and the material being deposited, the doped semiconductor layer 55 may form facets that may merge together or separate out."), [0078] (explaining the fin "may grow forming facets" because "different crystal planes may have different growth rates"), Figs. 4b-4e.

faceted with a diamond shape as in Figures 4b-4e below.[675] Figures 4b-4e show SiGe material 51 having a diamond-shaped fin with sloped facets along the (111) crystal planes. A person of ordinary skill in the art would have known that grading the Ge concentration in *Tung*'s SiGe material 51, as *Brask* instructs, would not change this aspect of *Tung*'s FinFET. A person of ordinary skill in the art would have understood that epitaxial films are, by definition, crystalline films, and therefore terminated by crystal facets.

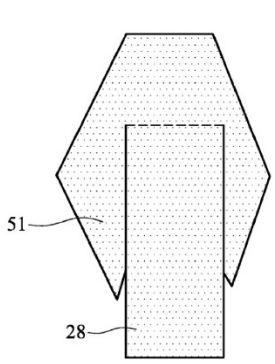


FIG. 4b

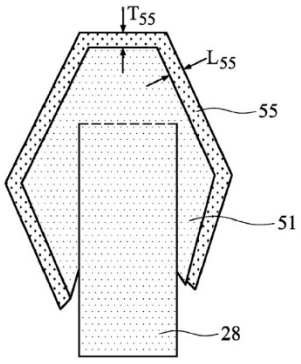


FIG. 4c

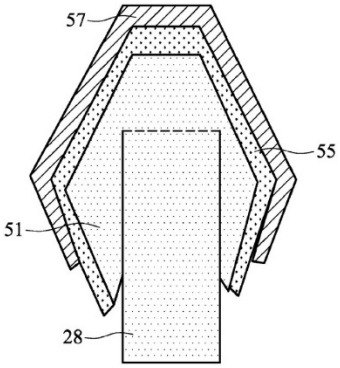


FIG. 4d

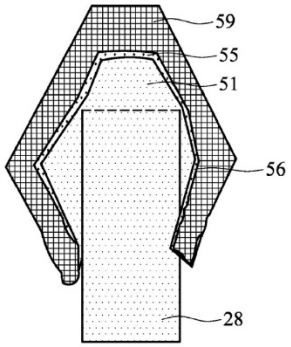


FIG. 4e

638. Because *Tung* teaches a FinFET with source/drain regions that have at least two facets, and because *Tung*'s FinFET implemented by applying *Brask*'s and *Yu*'s teachings as described in Sections IX.C.1 and IX.C.2 would include the same feature, a person of ordinary skill in the art would have understood that the asserted

[675] *Tung* ¶ [0040]; *see also id.* ¶ [0078] (explaining that doped semiconductor layer 55, which optionally is also part of the claimed source/drain regions, likewise "may grow forming facets" because "different crystal planes may have different growth rates"), Figs. 4b-4e.

combination of *Tung*, *Brask*, and *Yu* is a structure "wherein the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets" as claimed.

8. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 8 Obvious

a. Claim Element [8.0]: The Preamble

639. Claim 8 recites "[a]n integrated circuit structure." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.0].[676]

b. Claim Element [8.1]: Body

640. Claim 8 recites "a body comprising silicon." A person of ordinary skill in the art would have understood the '281 Patent uses the term "body" only once, equating it with a "fin."[677] The asserted combination of *Tung*, *Brask*, and *Yu* thus includes this feature for the same reasons I provide for claim element [1.1].[678]

[676] *See supra* Section IX.C.4.a.

[677] *See* '281 Patent at 13:35-38 ("As can be seen, the **tri-gate device** includes a substrate 600 having a semiconductor **body or fin 660** (represented by dashed lines) extending from the substrate 600 through isolation regions 610, 620."); *see also id.* at Fig. 6.

[678] *See supra* Section IX.C.4.b.

c. Claim Element [8.2]: Gate Electrode

641. Claim 8 recites "a gate electrode over the body, the gate electrode having a first side, and the gate electrode having a second side opposite the first side." A person of ordinary skill in the art would have understood the '281 Patent uses the term "body" only once, equating it with a "fin."[679] Thus, the asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.2].[680]

d. Claim Element [8.3]: First Dielectric Spacer

642. Claim 8 recites "a first dielectric spacer along the first side of the gate electrode." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.3].[681]

e. Claim Element [8.4]: First Source or Drain Region

643. Claim 8 recites "a first source or drain region in the body proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer." A person of ordinary skill in the art would have understood the '281 Patent uses the term "body" only once, equating it with a

[679] *See supra* note 677.

[680] *See supra* Section IX.C.4.c.

[681] in Section IX.C.4.d.

"fin."[682] Thus, the asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.4].[683]

f. Claim Element [8.5]: Graded Germanium Concentration of the First Source or Drain Region

644. Claim 8 recites "wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combination of *Tung*, *Brask*, and *Yu* include this feature for the same reasons I provide for claim element [1.5].[684]

g. Claim Element [8.6]: Second Dielectric Spacer

645. Claim 8 recites "a second dielectric spacer along the second side of the gate electrode." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.6].[685]

h. Claim Element [8.7]: Second Source or Drain Region

646. Claim 8 recites "a second source or drain region in the body proximate the second side of the gate electrode opposite the first side, a portion of the second source or drain region beneath the second dielectric spacer." A person of ordinary skill in the art would have understood the '281 Patent uses the term

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[682] *See supra* note 677.

[683] *See supra* Section IX.D.3.e

[684] *See supra* Section IX.D.3.f.

[685] *See supra* Sections IX.C.4.d, IX.C.4.g.

"body" only once, equating it with a "fin."[686] Thus, the asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.7].[687]

i. Claim Element [8.8]: Graded Germanium Concentration of the Second Source or Drain Region

647. Claim 8 recites "wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.8].[688]

j. Claim Element [8.9]: Interlayer Dielectric

648. Claim 8 recites "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region and the dielectric layer having a second opening exposing only a portion of the second source or drain region." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.9].[689]

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[686] *See supra* note 677.

[687] *See supra* Sections IX.C.4.e, IX.C.4.h.

[688] *See supra* Sections IX.C.4.f , IX.C.4.i.

[689] *See supra* Section IX.C.4.j.

k. Claim Element [8.10]: First Germanide Layer

649. Claim 8 recites "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.10].[690]

l. Claim Element [8.11]: Second Germanide Layer

650. Claim 8 recites "a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.11].[691]

m. Claim Element [8.12]: First Contact Plug

651. Claim 8 recites "a first contact plug in the first opening and on the first germanide layer." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.11].[692]

[690] *See supra* Section IX.C.4.k.

[691] *See supra* Sections IX.C.4.k, IX.C.4.l.

[692] *See supra* Section IX.C.4.m.

n. Claim Element [8.12]: First Contact Plug

652. Claim 8 recites "a second contact plug in the second opening and on the second germanide layer." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.12].[693]

o. A Person of Ordinary Skill in the Art Would Have Found Claim 8 Obvious

653. Because a person of ordinary skill in the art would have been motivated to make the combination of *Tung*, *Brask*, and *Yu* described above, because he or she would have reasonably expected to succeed in doing so, and because that combination satisfies each element of claim 8,[694] it is my opinion that claim 8 would have been obvious.

9. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 12 Obvious

a. Claim Element [12.0]: The Preamble

654. Claim 12 recites "[a] computing device." A person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* is a structure used in "a computing device."

655. As I explain in Section IX.C.4.a, the asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." And as I explain in

[693] *See supra* Section IX.C.4.m, IX.C.4.n.

[694] *See supra* Sections IX.C.1, IX.C.2, IX.C.4.a-n, IX.C.8.a-n.

Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

656. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[695] A person of ordinary skill in the art also would have understood that semiconductor chips are combined with other electronic circuit elements onto a circuit board for use in consumer electronic devices. And a person of ordinary skill in the art would have understood that many of the most popular consumer electronic devices were computing devices, such as smartphones, tablets, personal computers, and the like. In short, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* is an FET structure used in computing devices because such FET structures are designed for use in the integrated circuits that make computing devices function.

[695] *See, e.g.*, *Liu* at Title, Abstract, 1:24-25, 1:29-46, 4:48-5:2, 5:27-6:9, 6:55-56, 11:57-12:3, 32:22-40, 32:49-54, 33:11-37:59.

657. Accordingly, a person of ordinary skill in the art would have understood the combination of *Tung*, *Brask*, and *Yu* would go into "[a] computing device."

b. Claim Element [12.1]: Board

658. Claim 12 recites "a board." A person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* is a structure used in semiconductor chips that would be incorporated onto "a board."

659. The asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." As I explain in Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

660. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[696] A person of ordinary skill in the art also would have understood that semiconductor chips are combined with other electronic circuit elements onto a circuit board for use in consumer electronic devices. And a person of ordinary skill

[696] *See supra* note 695.

in the art would have understood that many of the most popular consumer electronic devices were computing devices, such as smartphones, tablets, personal computers, and the like. In short, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure that would go onto a circuit board because such FET structures form part of the integrated circuits that go into the circuit boards that make computing devices function.

661. Accordingly, a person of ordinary skill in the art would have understood the combination of *Tung*, *Brask*, and *Yu* would go into a semiconductor chip that gets incorporated into "a board."

c. Claim Element [12.2]: Integrated Circuit Structure

662. Claim 12 recites "a component coupled to the board, the component including an integrated circuit structure." A person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* is a structure that would constitute part of "a component coupled to the board."

663. The asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." As I explain in Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET

devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

664. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[697] A person of ordinary skill in the art also would have understood that semiconductor chips are combined with other electronic circuit elements onto a circuit board for use in consumer electronic devices. A person of ordinary skill in the art would have understood that such semiconductor chips constitute a "component coupled to the board." In short, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure that would go onto a component coupled to a circuit board because such FET structures form part of the integrated circuits coupled to the circuit boards in computing devices.

665. Accordingly, a person of ordinary skill in the art would have understood the combination of *Tung*, *Brask*, and *Yu* goes into "a component coupled to the board, the component including an integrated circuit structure."

[697] *See supra* note 695.

d. Claim Element [12.3]: Fin

666. Claim 12 recites "a fin comprising silicon." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.1].[698]

e. Claim Element [12.4]: Gate Electrode

667. Claim 12 recites "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.2].[699]

f. Claim Element [12.5]: First Dielectric Spacer

668. Claim 12 recites "a first dielectric spacer along the first side of the gate electrode." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.3].[700]

g. Claim Element [12.6]: First Source or Drain Region

669. Claim 12 recites "a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath

[698] *See supra* Section IX.C.4.b.

[699] *See supra* Section IX.C.4.c.

[700] *See supra* Section IX.C.4.d.

the first dielectric spacer." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.4].[701]

h. Claim Element [12.7]: Graded Germanium Concentration of the First Source or Drain Region

670. Claim 12 recites "wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.5].[702]

i. Claim Element [12.8]: Second Dielectric Spacer

671. Claim 12 recites "a second dielectric spacer along the second side of the gate electrode." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.6].[703]

j. Claim Element [12.9]: Second Source or Drain Region

672. Claim 12 recites "a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer." T The asserted combination of *Tung*, *Brask*,

[701] *See supra* Section IX.C.4.e.

[702] *See supra* Section IX.C.4.f.

[703] *See supra* Sections IX.C.4.d, IX.C.4.g.

and *Yu* includes this feature for the same reasons I provide for claim element [1.7].[704]

k. Claim Element [12.10]: Graded Germanium Concentration of the Second Source or Drain Region

673. Claim 12 recites "wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.8].[705]

l. Claim Element [12.11]: Interlayer Dielectric

674. Claim 12 recites "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons for claim element [1.9].[706]

m. Claim Element [12.12]: First Germanide Layer

675. Claim 12 recites "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising

[704] *See supra* Sections IX.C.4.e, IX.C.4.h.

[705] *See supra* Sections IX.C.4.f, IX.C.4.i.

[706] *See supra* Section IX.C.4.j.

silicon, germanium and titanium." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.10].[707]

n. Claim Element [12.13]: Second Germanide Layer

676. Claim 12 recites "a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons I provide for claim element [1.11].[708]

o. Claim Element [12.14]: First Contact Plug

677. Claim 12 recites "a first contact plug in the first opening and on the first germanide layer." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons for claim element [1.12].[709]

p. Claim Element [12.15]: Second Contact Plug

678. Claim 12 recites "a second contact plug in the second opening and on the second germanide layer." The asserted combination of *Tung*, *Brask*, and *Yu* includes this feature for the same reasons for claim element [1.13].[710]

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[707] *See supra* Section IX.C.4.k.

[708] *See supra* Sections IX.C.4.k, IX.C.4.l.

[709] *See supra* Section IX.C.4.m.

[710] *See supra* Sections IX.C.4.m, IX.C.4.n.

q. A Person of Ordinary Skill in the Art Would Have Found Claim 12 Obvious

679. Because a person of ordinary skill in the art would have been motivated to combine *Tung*, *Brask*, and *Yu* as described above, because he or she would have reasonably expected to succeed in doing so, and because that combination satisfies each element of claim 12, it is my opinion that claim 12 would have been obvious.

10. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 13 Obvious

680. Claim 13 depends from claim 12. I understand that means claim 13 requires all the same features as claim 12, plus the additional features recited in claim 13. The asserted combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.C.9.a-p.

681. Claim 13 further recites "a memory coupled to the board." The asserted combination of *Tung*, *Brask*, and *Yu* suggests "a memory coupled to the board."

682. The asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." As I explain in Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET

devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

683. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[711] A person of ordinary skill in the art further would have understood that such chips are combined with other electronic circuit elements, including memory, onto a circuit board for use in computing devices. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in chips that go onto circuit boards and exchange information with a memory.

684. Because the asserted combination of *Tung*, *Brask*, and *Yu* teaches every feature recited in claim 13 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 13 would have been obvious.

[711] *See supra* note 695.

11. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 14 Obvious

685. Claim 14 depends from claim 12. I understand that means claim 14 requires all the same features as claim 12, plus the additional features recited in claim 14. The combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.C.9.a-p.

686. Claim 14 further recites "a communication chip coupled to the board." The asserted combination of *Tung*, *Brask*, and *Yu* suggests "a communication chip coupled to the board."

687. The asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." As I explain in Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

688. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[712] A person of ordinary skill in the art also would have understood that such chips are

[712] *See supra* note 695.

used in smartphones and computers, for example, which contain circuit boards with at least one communications chip. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits, including communication chips, that go onto circuit boards in smartphones and computers.

689. Because the asserted combination of *Tung*, *Brask*, and *Yu* teaches every feature recited in claim 14 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 14 would have been obvious.

12. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 15 Obvious

690. Claim 15 depends from claim 12. I understand that means claim 15 requires all the same features as claim 12, plus the additional features recited in claim 15. The asserted combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.C.9.a-p.

691. Claim 15 further recites "a camera coupled to the board." The asserted combination of *Tung*, *Brask*, and *Yu* suggests "a camera coupled to the board."

692. The asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." As I explain in Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

693. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[713] A person of ordinary skill in the art further would have understood that such chips are used in smartphones and computers, for example, which contain a camera coupled to the circuit board. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a camera.

[713] *See supra* note 695.

694. Because the asserted combination of *Tung*, *Brask*, and *Yu* teaches every feature recited in claim 15 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 15 would have been obvious.

13. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 16 Obvious

695. Claim 16 depends from claim 12. I understand that means claim 16 requires all the same features as claim 12, plus the additional features recited in claim 16. The asserted combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.C.9. a-p.

696. Claim 16 further recites "a battery coupled to the board." The asserted combinations of combination of *Tung*, *Brask*, and *Yu* suggests "a battery coupled to the board."

697. The asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." As I explain in Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

698. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building

blocks of integrated circuits, which, after they are packaged, are called "chips."[714] A person of ordinary skill in the art further would have understood that such chips are used in smartphones and computers, for example, which contain a battery coupled to the circuit board. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a battery.

699. Because the asserted combination of *Tung*, *Brask*, and *Yu* teaches every feature recited in claim 16 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 16 would have been obvious.

14. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 17 Obvious

700. Claim 17 depends from claim 12. I understand that means claim 17 requires all the same features as claim 12, plus the additional features recited in

[714] *See supra* note 695.

claim 17. The asserted combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.C.9.a-p.

701. Claim 17 further recites "an antenna coupled to the board." The asserted combination of *Tung*, *Brask*, and *Yu* suggests "an antenna coupled to the board."

702. The asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." As I explain in Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

703. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[715] A person of ordinary skill in the art further would have understood that such chips are used in smartphones and computers, for example, which contain an antenna coupled to the circuit board. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other

[715] *See supra* note 695.

consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to an antenna.

704. Because the asserted combination of *Tung*, *Brask*, and *Yu* teaches every feature recited in claim 17 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 17 would have been obvious.

15. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 18 Obvious

705. Claim 18 depends from claim 12. I understand that means claim 18 requires all the same features as claim 12, plus the additional features recited in claim 18. The asserted combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.C.9.a-p.

706. Claim 18 further recites "wherein the component is a packaged integrated circuit die." As I explain in Section IX.C.9.c for claim element [12.2], the asserted combination of *Tung*, *Brask*, and *Yu* provides for "a component coupled to the board, the component including an integrated circuit structure." The asserted combination of *Tung*, *Brask*, and *Yu* also suggests "the component is a packaged integrated circuit die."

707. The asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." As I explain in Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

708. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[716] A person of ordinary skill in the art further would have understood such chips are packaged to be combined with other electronic circuit elements onto a circuit board for use in consumer electronic devices. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. Moreover, a person of ordinary skill in the art would have understood that unpackaged integrated circuits (i.e., processed wafers and unpackaged dies) are used only for testing or to be packaged into integrated circuits. In short, a person of ordinary skill in the art would have

[716] *See supra* note 695.

understood that the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits that go onto circuit boards as packaged integrated circuit dies.

709. Because the asserted combination of *Tung*, *Brask*, and *Yu* teaches every feature recited in claim 18 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 18 would have been obvious.

16. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 19 Obvious

710. Claim 19 depends from claim 12. I understand that means claim 19 requires all the same features as claim 12, plus the additional features recited in claim 19. The asserted combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.C.9.a-p.

711. Claim 19 further recites "wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor." As I explain in Section IX.C.9.c for claim element [12.2], a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* provides for a "component including an integrated circuit structure." The asserted combination of *Tung*, *Brask*, and *Yu* also suggests "the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor."

712. The asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." As I explain in Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

713. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[717] A person of ordinary skill in the art further would have understood that such chips, including processors, communications chips, and digital signal processors (DSPs), are coupled to the circuit boards of smartphones and computers. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits, including processors, communications chips, and digital signal

[717] *See supra* note 695.

processors (DSPs), that go onto circuit boards of smartphones, computers, and the like.

714. Because the asserted combination of *Tung*, *Brask*, and *Yu* teaches every feature recited in claim 19 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim19 would have been obvious.

17. The Combination of *Tung*, *Brask*, and *Yu* Would Have Rendered Claim 20 Obvious

715. Claim 20 depends from claim 12. I understand that means claim 20 requires all the same features as claim 12, plus the additional features recited in claim 20. The asserted combination of *Tung*, *Brask*, and *Yu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.C.9.a-p.

716. Claim 20 further recites "wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box." The asserted combination of *Tung*, *Brask*, and *Yu* suggests "wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box."

717. The asserted combination of *Tung*, *Brask*, and *Yu* is a component of "an integrated circuit device." As I explain in Section IX.C.3, a person of ordinary skill in the art, applying common knowledge about the semiconductor industry and consumer electronic devices, would have found it obvious to employ FinFET

devices (like the ones that result from combining *Tung*, *Brask*, and *Yu*'s teachings) into smartphones, computers, and other typical consumer electronic devices.

718. A person of ordinary skill in the art would have understood that FET devices like those described in *Tung*, *Brask*, and *Yu* are fundamental building blocks of integrated circuits, which, after they are packaged, are called "chips."[718] A person of ordinary skill in the art further would have understood that such chips are coupled to the circuit boards of smartphones, computers, and other consumer electronic devices. A person of ordinary skill in the art would have understood that computing devices like smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors. In short, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits that go onto the circuit boards of smartphones, laptops, desktop computers, servers, set-top boxes, and the like.

719. Because the asserted combination of *Tung*, *Brask*, and *Yu* teaches every feature recited in claim 20 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 20 would have been obvious.

[718] *See supra* note 695.

D. Ground 2B: The Combination of *Tung*, *Brask*, *Yu*, and *Liu* Would Have Rendered Claims 12-20 Obvious

1. A Person of Ordinary Skill in the Art Would Have Found the Combination of *Tung*, *Brask*, *Yu*, and *Liu* Obvious

720. As I explain in Section IX.C, *Tung* teaches FinFET devices, and a person of ordinary skill in the art would have found it obvious to implement *Tung*'s FinFET devices according to the teachings of *Brask* and *Yu*. A person of ordinary skill in the art also would have found it obvious to employ FinFET devices like the ones *Tung* teaches (including as implemented according to the teachings of *Brask* and *Yu* as described above) into smartphones, computers, and other consumer electronic devices. Doing so not only would have been obvious in view of references like *Liu*, but also based on common sense and basic knowledge about how FinFET devices and other MOSFETs are used. A person of ordinary skill in the art would have understood that smartphones, computers, and other consumer electronic devices were (and still are), by far, the primary applications for chips made up of such transistors.

721. As I explain in Section VIII.F, *Liu* describes exemplary systems in which FETs, including FinFETs, may be used.[719] To a person of ordinary skill in the art, implementing FinFETs into computing devices like those *Liu* describes

[719] *See Liu* at 33:10-37:40, Figs. 10, 11.

would have been obvious according to at least four of the various obviousness rationales I have been asked to consider.

722. First, a person of ordinary skill in the art would have considered implementing FinFETs into computing devices like those *Liu* describes to be example of combining prior art elements according to known methods to yield predictable results. Both FinFETs (like the ones resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) and integrated circuits used in consumer electronic devices like *Liu*'s were prior art elements known to a person of ordinary skill in the art by December 2010. Combining them would have required nothing more than well-known methods. Additionally, a person of ordinary skill in the art would have understood that deploying FinFETs (like the one resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in the integrated circuits of *Liu*'s cell phone system would yield a predictable result—namely, a cell phone system like the one *Liu* describes.

723. Second, a person of ordinary skill in the art would have considered implementing FinFETs into computing devices like those *Liu* describes to be an example of using a known technique to improve similar devices in the same way. A person of ordinary skill in the art would have known techniques for incorporating FinFETs (like the ones resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) into integrated circuits using known methods. And a person

of ordinary skill in the art would have understood that doing so would improve the integrated circuits in *Liu*'s cell phone system by virtue of using *Tung*'s FinFET structure as implemented according to *Brask*'s and *Yu*'s teachings.

724. Third, a person of ordinary skill in the art would have considered implementing FinFETs into computing devices like those *Liu* describes to be an example of applying a known technique (e.g., integrating FinFETs into integrated circuits) to a known device (e.g., the integrated circuits in *Liu*'s cell phone system) ready for improvement. A person of ordinary skill in the art would have recognized several potential improvements to *Liu*'s integrated circuits by incorporating FinFETs like the ones resulting from the asserted combination of *Tung*, *Brask*, and *Yu*, such as faster switching speeds and less power consumption and heating due to reduced source/drain contact resistance.

725. Fourth, a person of ordinary skill in the art would have implemented FinFETs into computing devices like those *Liu* describes due to a teaching, suggestion, or motivation in the prior art to arrive at the claimed invention. A person of ordinary skill in the art would have been familiar with several teachings, suggestions, and motivations in the prior art, including those provided in *Tung*, *Brask*, *Yu*, and *Liu* themselves.[720] A person of ordinary skill in the art, being well

[720] *See, e.g.*, *Liu* at 1:29-6:10, 32:23-40, 33:11-37:59, Figs. 8, 10, 11; *Tung* ¶ [0003]; *Brask* at 1:7-11, 2:44-67, 4:62-5:20, 12:18-32, 27:20-27.

acquainted with the ongoing pursuit of semiconductor scaling and Moore's Law, would have been motivated to incorporate FinFETs (like the ones resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) into the integrated circuits of *Liu*'s cell phone system. *Liu* itself even recognizes that such FinFETs may be used.[721] By incorporating FinFETs (like the ones resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) into computing devices like those described in *Liu*, a person of ordinary skill in the art would have arrived at a combination in which *Liu*'s cell phone system includes integrated circuits made up of FinFETs like the ones resulting from the asserted combination of *Tung*, *Brask*, and *Yu*.

726. Regardless of the rationale, a person of ordinary skill in the art would have found it obvious to deploy FinFETs like the ones resulting from the asserted combination of *Tung*, *Brask*, and *Yu* in the integrated circuits of a system like the one *Liu* describes.

2. The Combination of *Tung*, *Brask*, *Yu*, and *Liu* Would Have Rendered Claim 12 Obvious

a. Claim Element [12.0]: The Preamble

727. Claim 12 recites "[a] computing device." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "a computing device."

[721] *See Liu* at 32:23-40, Fig. 8.

728. As I explain in Section IX.C.9.a, a person of ordinary skill in the art would have understood the FinFET described by the combination of *Tung*, *Brask*, and *Yu* would go into "[a] computing device." Although a person of ordinary skill in the art would have found this sufficient to satisfy claim element [12.0], *Liu*'s teachings make it explicit.

729. *Liu* teaches "a computing device." For example, *Liu* describes a "wireless handset," shown below, with FinFET-based integrated circuits.[722]

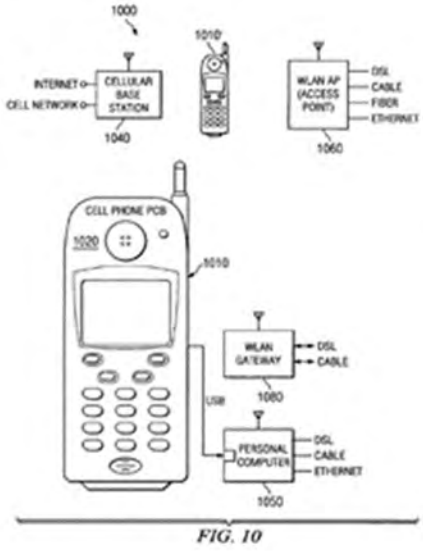


FIG. 10

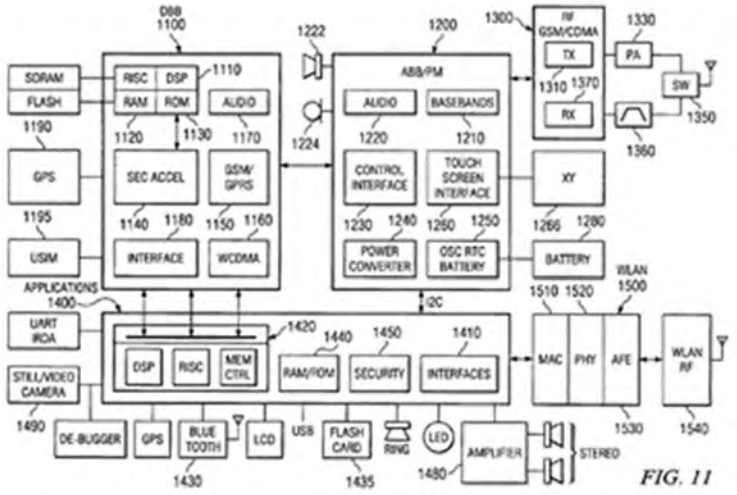


FIG. 11

730. *Liu* also describes other electronic devices that incorporate integrated circuits, including "radios and televisions, fixed and portable entertainment units, routers, pagers, personal digital assistants (PDA), organizers, scanners, faxes, copiers, household appliances, [and] office appliances."[723]

[722] *See id.* at 6:45-51, 32:23-40, 33:11-37:59, Figs. 8, 10, 11.

[723] *Id.* at 34:3-22.

731. Because *Liu* teaches a "computing device," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in the integrated circuits of *Liu*'s "computing device," a person of ordinary skill in the art would have understood the *Tung-Brask-Yu-Liu* combination includes "[a] computing device" as claimed.

b. Claim Element [12.1]: A Board

732. Claim 12 recites "a board." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teach "a board."

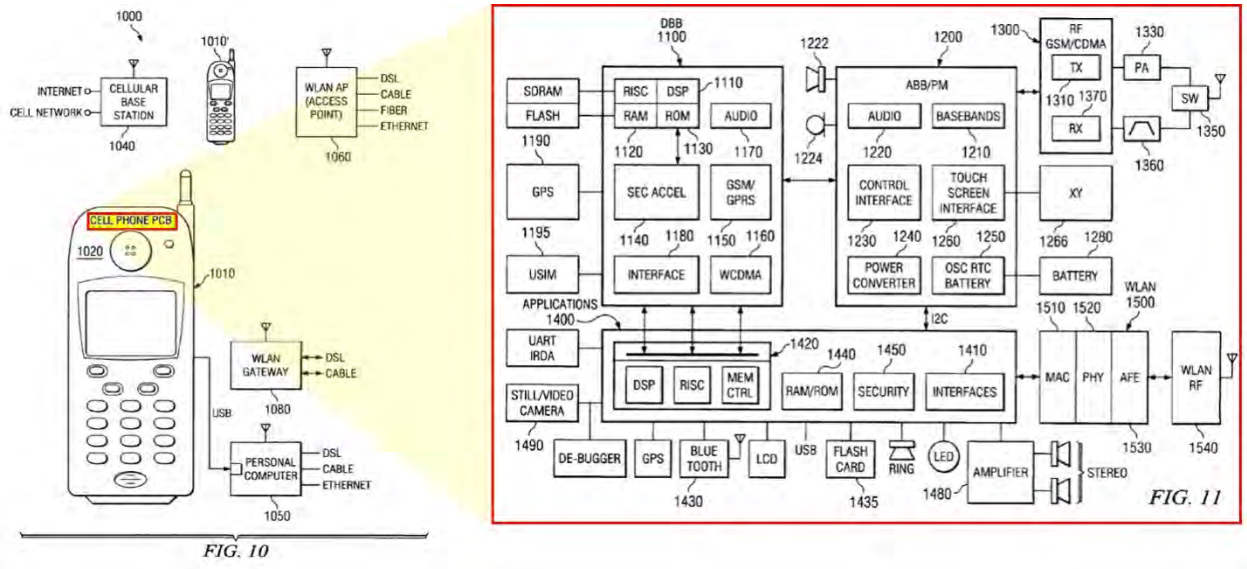
733. As I explain in Section IX.C.9.b, a person of ordinary skill in the art would have understood the FinFET described by the combination of *Tung*, *Brask*, and *Yu* would go into a semiconductor chip that gets incorporated into "a board." Although a person of ordinary skill in the art would have found this sufficient to satisfy claim element [12.1], *Liu*'s teachings make it explicit.

734. *Liu* teaches "a board." For example, *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[724] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[725] "For

[724] *Id.* at 33:46-61.

[725] *Id.* at 33:62-63.

conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[726] I annotated the figures below to show this relationship.



735. Because *Liu* teaches a "a board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in the integrated circuits found on *Liu*'s circuit board, a person of ordinary skill in the art would have understood the *Tung-Brask-Yu-Liu* combination includes "a board" as claimed.

c. Claim Element [12.2]: Integrated Circuit Structure

736. Claim 12 recites "a component coupled to the board, the component including an integrated circuit structure." The asserted combination of *Tung*,

[726] *Id.* at 33:66-34:2.

Brask, *Yu*, and *Liu* includes teaches "a component coupled to the board, the component including an integrated circuit structure."

737. As I explain in Section IX.C.9.c, a person of ordinary skill in the art would have understood the FinFET described by the combination of *Tung*, *Brask*, and *Yu* would go into "a component coupled to the board, the component including an integrated circuit structure." Although a person of ordinary skill in the art would have found this sufficient to satisfy claim element [12.2], *Liu*'s teachings make it explicit.

738. *Liu* teaches components (i.e., integrated circuits) coupled to the board that include integrated circuit structures. For example, *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[727] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[728] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[729] Those integrated circuits include a digital baseband chip 1100 (green below), an analog baseband chip 1200 (blue below), a GSM chip 1300 (red

[727] *Id.* at 33:46-61.

[728] *Id.* at 33:62-63.

[729] *Id.* at 33:66-34:2.

below), an applications processor chip 1400 (purple below), and a WLAN chip 1500 (orange below).[730] According to *Liu*, these are "integrated circuits made by any of the improved processes and including the improved transistors illustrated in the other Figures," which includes FinFET structures.[731]

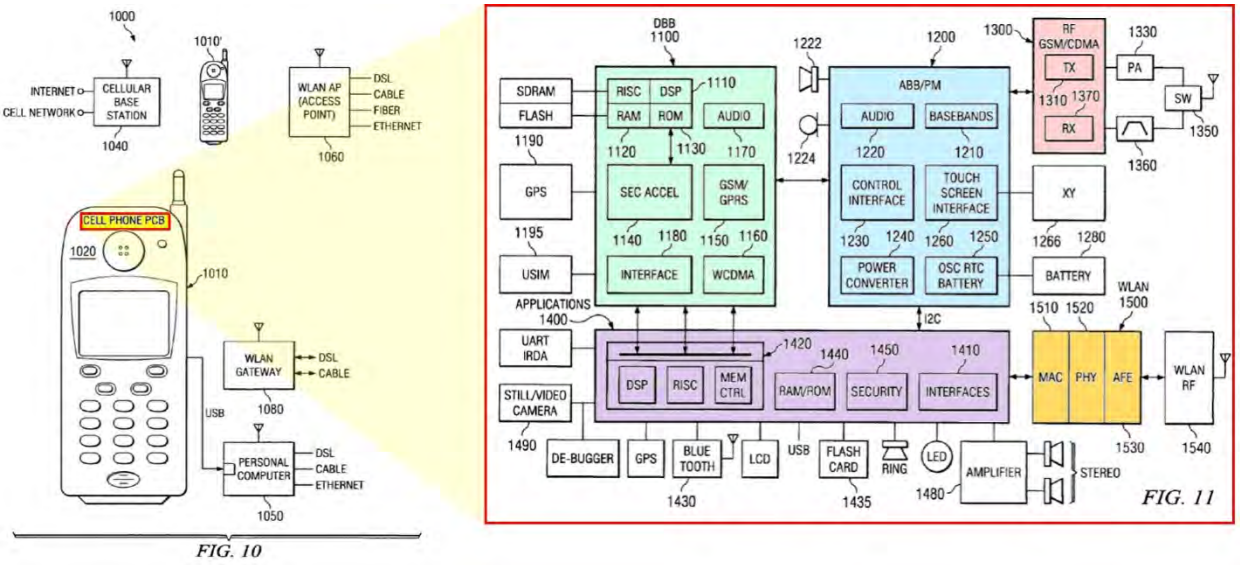


FIG. 10

FIG. 11

739. Because *Liu* teaches integrated circuits coupled to a circuit board and those integrated circuits include FinFET structures, and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the ones resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in those integrated circuits, a person of ordinary skill in the art would have understood the *Tung-Brask-Yu-Liu* combination includes "a component coupled to the board, the component including an integrated circuit structure" as claimed.

[730] *See id.* at 34:23-30, 35:14-20, 35:64-67, 36:15-16, 37:14-17.

[731] *Id.* at 6:48-51; *see also id.* at 32:23-40, Fig. 8.

d. Claim Element [12.3]: Fin

740. Claim 12 recites "a fin comprising silicon." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.1].[732]

e. Claim Element [12.4]: Gate Electrode

741. Claim 12 recites "a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.2].[733]

f. Claim Element [12.5]: First Dielectric Spacer

742. Claim 12 recites "a first dielectric spacer along the first side of the gate electrode." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.3].[734]

g. Claim Element [12.6]: First Source or Drain Region

743. Claim 12 recites "a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath

[732] *See supra* Section IX.C.4.b.

[733] *See supra* Section IX.C.4.c.

[734] *See supra* Section IX.C.4.d.

the first dielectric spacer." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.4].[735]

h. Claim Element [12.7]: Graded Germanium Concentration of the First Source or Drain Region

744. Claim 12 recites "wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element[1.5].[736]

i. Claim Element [12.8]: Second Dielectric Spacer

745. Claim 12 recites "a second dielectric spacer along the second side of the gate electrode." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.6].[737]

j. Claim Element [12.9]: Second Source or Drain Region

746. Claim 12 recites "a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer." The asserted combination of *Tung*, *Brask*,

[735] *See supra* Section IX.C.4.e.

[736] *See supra* Section IX.C.4.f.

[737] *See supra* Sections IX.C.4.d, IX.C.4.g.

Yu, and *Liu* includes this feature for the same reasons I provide for claim element [1.7].[738]

k. Claim Element [12.10]: Graded Germanium Concentration of the Second Source or Drain Region

747. Claim 12 recites "wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.8].[739]

l. Claim Element [12.11]: Interlayer Dielectric

748. Claim 12 recites "a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.9].[740]

[738] *See supra* Sections IX.C.4.e, IX.C.4.h.

[739] *See supra* Sections IX.C.4.f, IX.C.4.i.

[740] *See supra* Section IX.C.4.j.

m. Claim Element [12.12]: First Germanide Layer

749. Claim 12 recites "a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.10].[741]

n. Claim Element [12.13]: Second Germanide Layer

750. Claim 12 recites "a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.11].[742]

o. Claim Element [12.14]: First Contact Plug

751. Claim 12 recites "a first contact plug in the first opening and on the first germanide layer." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.12].[743]

[741] *See supra* Section IX.C.4.k.

[742] *See supra* Sections IX.C.4.k, IX.C.4.l.

[743] *See supra* Section IX.C.4.m.

p. Claim Element [12.15]: Second Contact Plug

752. Claim 12 recites "a second contact plug in the second opening and on the second germanide layer." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes this feature for the same reasons I provide for claim element [1.13].[744]

q. A Person of Ordinary Skill in the Art Would Have Found Claim 12 Obvious

753. Because a person of ordinary skill in the art would have been motivated to combine the teachings of *Tung*, *Brask*, *Yu*, and *Liu* as described above, because he or she would have reasonably expected to succeed in doing so, and because that combination satisfies each element of claim 12,[745] it is my opinion that claim 12 would have been obvious.

3. The Combination of *Tung*, *Brask*, *Yu*, and *Liu* Would Have Rendered Claim 13 Obvious

754. Claim 13 depends from claim 12. I understand that means claim 13 requires all the same features as claim 12, plus the additional features recited in claim 12. The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.D.2.a-p.

[744] *See supra* Sections IX.C.4.m, IX.C.4.n.

[745] *See supra* Sections IX.C.1-3, IX.C.4.a-n, IX.D.1, IX.D.2.a-p.

755. Claim 13 further recites "a memory coupled to the board." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "a memory coupled to the board."

756. As I explain in Section IX.C.10, a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in chips that go onto circuit boards and exchange information with a memory. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 13, *Liu*'s teachings make it explicit.

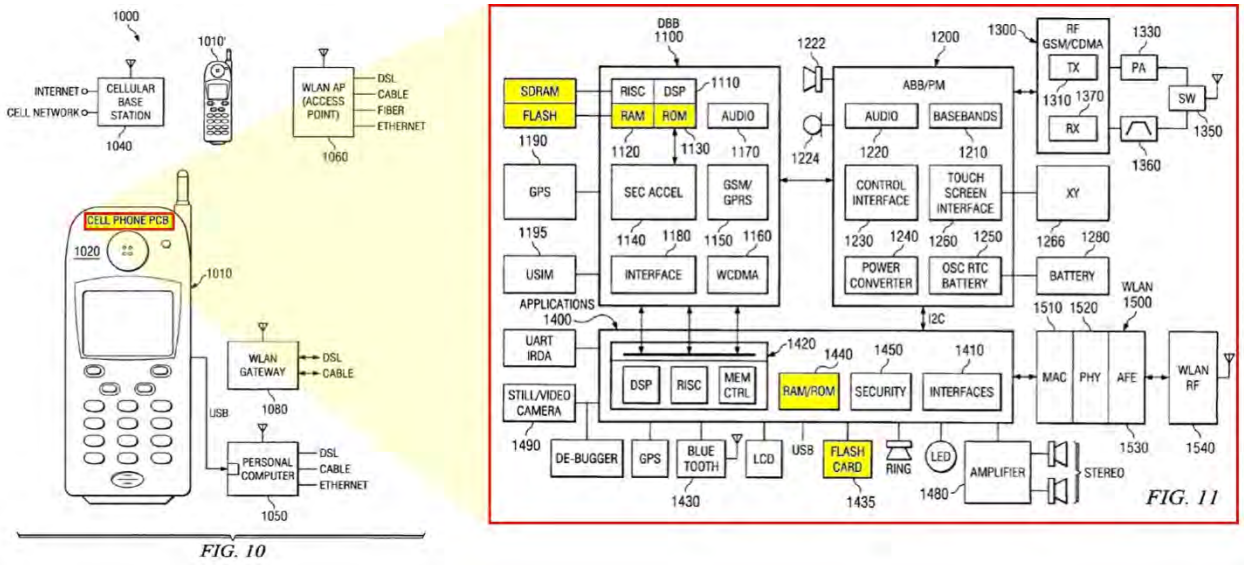
757. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[746] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[747] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[748] Coupled to the printed circuit board are various memories, highlighted in yellow below, including "off-chip Flash memory and SDRAM (synchronous dynamic random access memory)," "[o]n chip RAM 1120 and on-chip ROM 1130," "off-chip memory

[746] *Liu* at 33:46-61.

[747] *Id.* at 33:62-63.

[748] *Id.* at 33:66-34:2.

resources 1435 including as appropriate, mobile DDR (double data rate) DRAM, and flash memory of any of NAND Flash, NOR Flash, and Compact Flash," and "on-chip memory 1440 with RAM and ROM," which includes "frame buffer internal SRAM (static random access memory) in memory area 1440."[749]



758. Because *Liu* teaches a "computing device" that includes "a memory coupled to the board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the one resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in the integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "a memory coupled to the board."

[749] *Id.* at 34:28-33, 36:24-33.

759. Because the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches every feature recited in claim 13 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 13 would have been obvious.

4. The Combination of *Tung*, *Brask*, *Yu*, and *Liu* Would Have Rendered Claim 14 Obvious

760. Claim 14 depends from claim 12. I understand that means claim 14 requires all the same features as claim 12, plus the additional features recited in claim 14. The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.D.2.a-p.

761. Claim 14 further recites "a communication chip coupled to the board." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "a communication chip coupled to the board."

762. As I explain in Section IX.C.11, a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits, including communication chips, that go onto circuit boards in smartphones and computers. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 14, *Liu*'s teachings make it explicit.

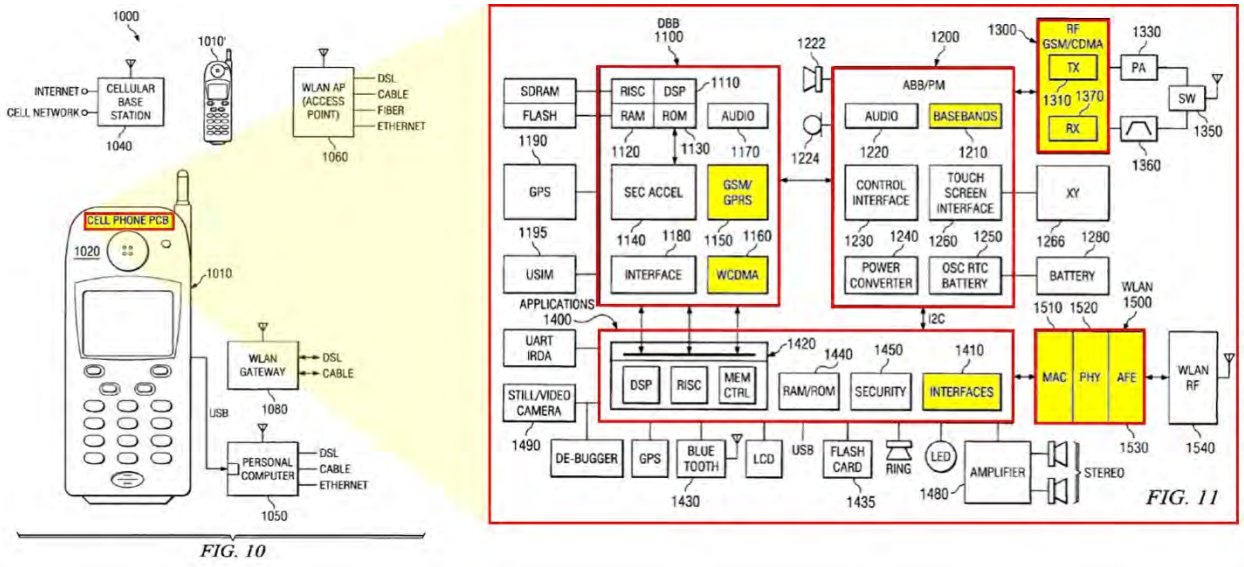
763. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[750] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[751] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[752] Coupled to the printed circuit board are various communications chips, including (1) "integrated circuit 1100," which "supports and provides interfaces for one or more of GSM, GPRS, EDGE, and UMTS (Global System for Mobile communications, General Packet Radio Service, Enhanced Data Rates for Global Evolution, Universal Mobile Telecommunications System) wireless," (2) "mixed-signal integrated circuit 1200," which "includes an analog baseband (ABB) block 1210 for GSM/GPRS/EDGE/UMTS," (3) "integrated circuit 1300," which "includes a GSM/GPRS/EDGE/UMTS RF transmitter block 1310," (4) "integrated circuit chip 1400," which includes "WLAN 802.11a/b/g interface circuit 1410 coupled to a WLAN chip 1500," and (5) "a WLAN integrated circuit 1500," which "includes MAC (media access controller) 1510, PHY (physical layer) 1520 and AFE (analog

[750] *Id.* at 33:46-61.

[751] *Id.* at 33:62-63.

[752] *Id.* at 33:66-34:2.

front end) 1530" and "is coupled by receive (RX), transmit (Tx) and CONTROL lines to an off-chip WLAN RF circuitry 1540."[753] I have highlighted the most relevant functional blocks in Figure 11 below.



764. Because *Liu* teaches a "communication chip coupled to the board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the one resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in the integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "a communication chip coupled to the board."

[753] *Id.* at 34:33-42, 35:14-20, 35:64-36:36, 37:14-36.

765. Because the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches every feature recited in claim 14 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 14 would have been obvious.

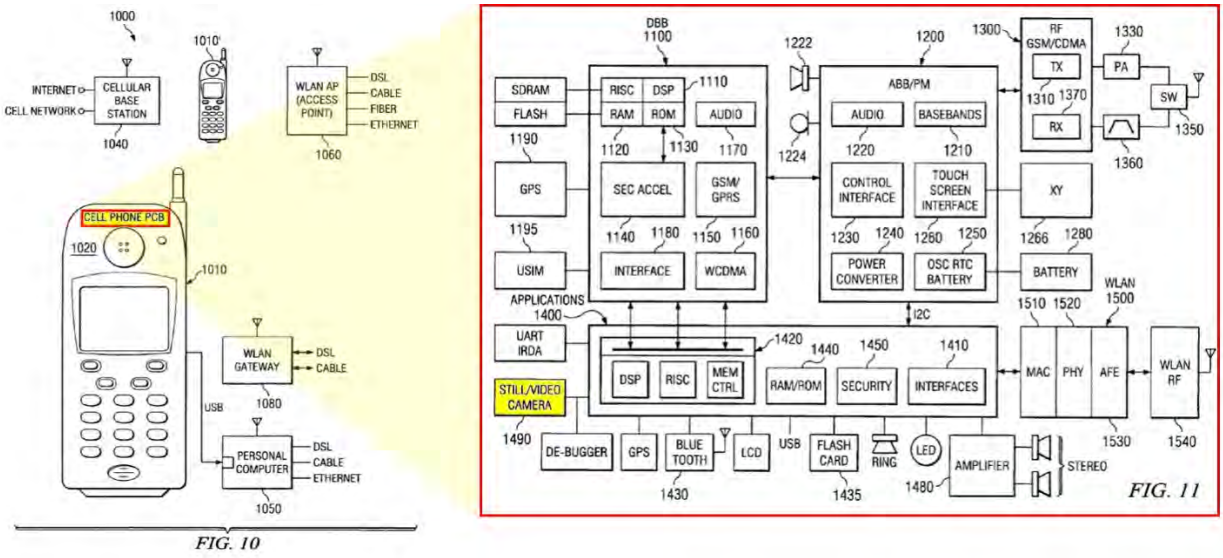
5. The Combination of *Tung*, *Brask*, *Yu*, and *Liu* Would Have Rendered Claim 15 Obvious

766. Claim 15 depends from claim 12. I understand that means claim 15 requires all the same features as claim 12, plus the additional features recited in claim 15. The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.D.2.a-p.

767. Claim 15 further recites "a camera coupled to the board." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "a camera coupled to the board."

768. As I explain in Section IX.C.12, a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a camera. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 15, *Liu*'s teachings make it explicit.

769. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[754] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[755] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[756] Coupled to the printed circuit board is a camera, highlighted below in yellow, such as "off-chip still cameras or video cameras 1490" or "a CMOS sensor of radiant energy."[757]



770. Because *Liu* teaches a "camera coupled to the board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs

[754] *Id.* at 33:46-61.

[755] *Id.* at 33:62-63.

[756] *Id.* at 33:66-34:2.

[757] *Id.* at 36:60-65.

(like the one resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in the integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches a "camera coupled to the board."

771. Because the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches every feature in claim 15 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 15 would have been obvious.

6. The Combination of *Tung*, *Brask*, *Yu*, and *Liu* Would Have Rendered Claim 16 Obvious

772. Claim 16 depends from claim 12. I understand that means claim 16 requires all the same features as claim 12, plus the additional features recited in claim 16. The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.D.2.a-p.

773. Claim 16 further recites "a battery coupled to the board." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "a battery coupled to the board."

774. As I explain in Section IX.C.13, a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to a battery. Although a person of

ordinary skill in the art would have found this sufficient to satisfy claim 16, *Liu*'s teachings make it explicit.

775. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[758] Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[759] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[760] Coupled to the printed circuit board is "a lithium-ion battery 1280 and backup battery," highlighted below in yellow.[761]

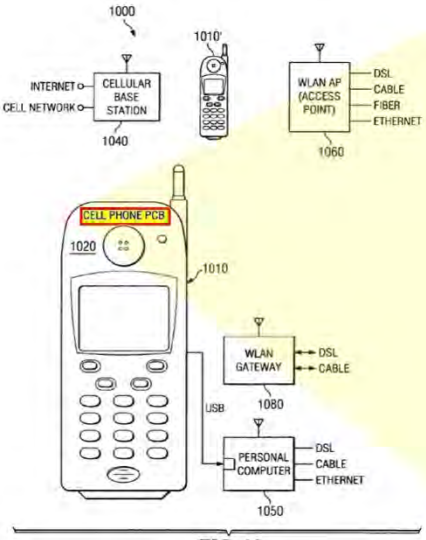


FIG. 10

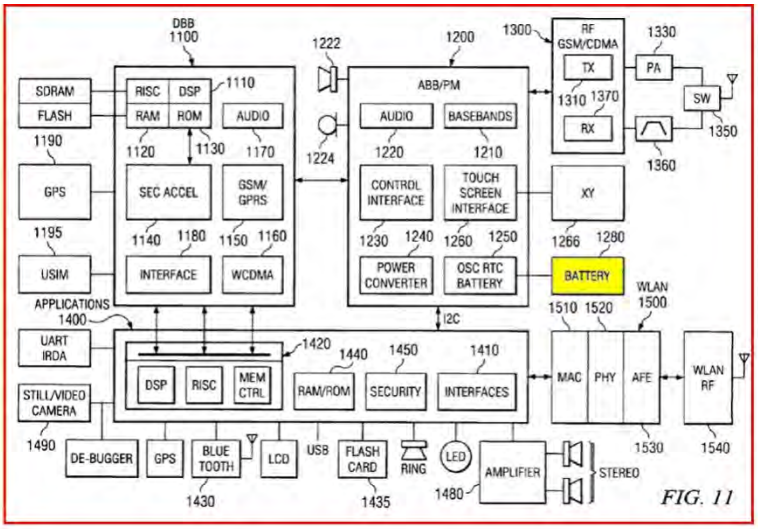


FIG. 11

[758] *Id.* at 33:46-61.

[759] *Id.* at 33:62-63.

[760] *Id.* at 33:66-34:2.

[761] *Id.* at 35:54-63.

776. Because *Liu* teaches a "battery coupled to the board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the one resulting from the asserted combinations of *Tung*, *Brask*, and *Yu*) in the integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches a "battery coupled to the board."

777. Because the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches every feature in claim 16 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 16 would have been obvious.

7. The Combination of *Tung*, *Brask*, *Yu*, and *Liu* Would Have Rendered Claim 17 Obvious

778. Claim 17 depends from claim 12. I understand that means claim 17 requires all the same features as claim 12, plus the additional features recited in claim 17. The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.D.2.a-p.

779. Claim 17 further recites "an antenna coupled to the board." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "an antenna coupled to the board."

780. As I explain in Section IX.C.14, a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* is a FET

structure designed for use in integrated circuits that go onto circuit boards in smartphones and computers that are coupled to an antenna. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 17, *Liu*'s teachings make it explicit.

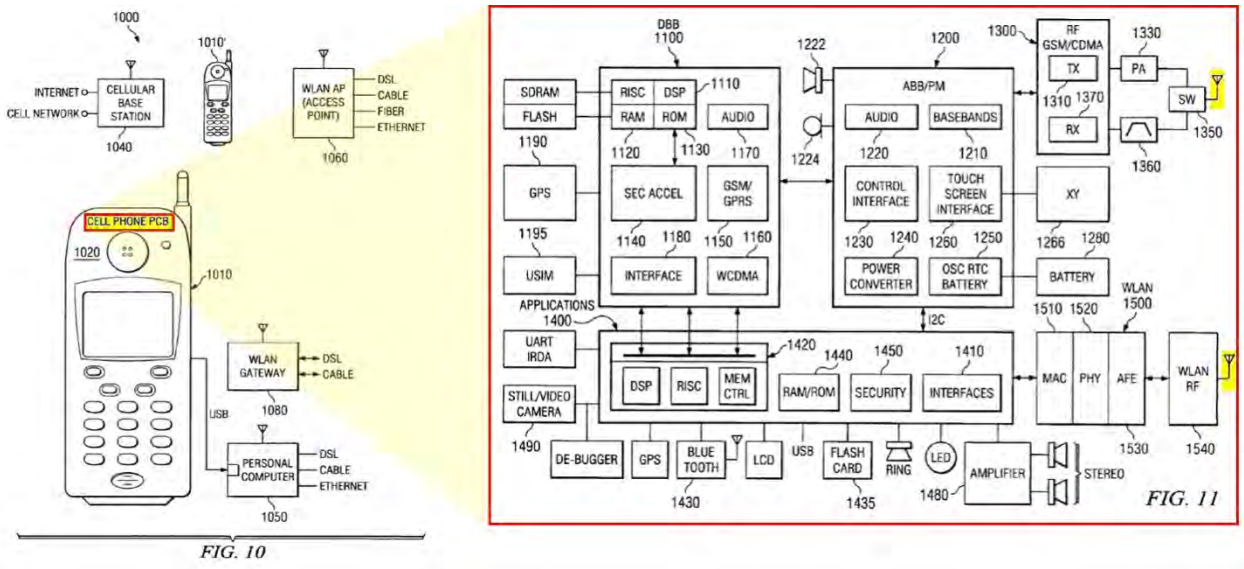


FIG. 10

FIG. 11

781. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 above illustrates.[762] Figure 11 above illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[763] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone

[762] *Id.* at 33:46-61.

[763] *Id.* at 33:62-63.

handsets 1010 and 1010'."[764] Coupled to the printed circuit board is a "wireless antenna" and a "WLAN antenna," both highlighted above in yellow.[765]

782. Because *Liu* teaches "an antenna coupled to the board," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the one resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in the integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "an antenna coupled to the board."

783. Because the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches every feature in claim 17 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 17 would have been obvious.

8. The Combination of *Tung*, *Brask*, *Yu*, and *Liu* Would Have Rendered Claim 18 Obvious

784. Claim 18 depends from claim 12. I understand that means claim 18 requires all the same features as claim 12, plus the additional features recited in

[764] *Id.* at 33:66-34:2.

[765] *Id.* at 36:4-7, 37:26-27; *see also id.* at 5:62-65 (disclosing "a wireless communications device [that] includes an antenna")

claim 18. The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches all the features recited in claim 12 for the reasons I provide in Sections IX.D.2.a-p.

785. Claim 18 further recites "the component is a packaged integrated circuit die." As I explain above in Section IX.D.2.c, the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches teach "a component coupled to the board, the component including an integrated circuit structure." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* also teaches that "the component is a packaged integrated circuit die."

786. As I explain in Section IX.C.15, a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Yu* is a FET structure designed for use in integrated circuits that go onto circuit boards as packaged integrated circuit dies. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 18, *Liu*'s teachings make it explicit.

787. *Liu* teaches components (i.e., integrated circuits) coupled to the board that include integrated circuit structures. For example, *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[766] Additionally, Figure 11 below illustrates "integrated circuit

[766] *Id.* at 33:46-61.

chips for use in the blocks of the communications system 1000 of FIG. 10."[767] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[768] Those integrated circuits include a digital baseband chip 1100 (green below), an analog baseband chip 1200 (blue below), a GSM chip 1300 (red below), an applications processor chip 1400 (purple below), and a WLAN chip 1500 (orange below).[769] According to *Liu*, these are "integrated circuits made by any of the improved processes and including the improved transistors illustrated in the other Figures," which includes FinFET structures.[770]

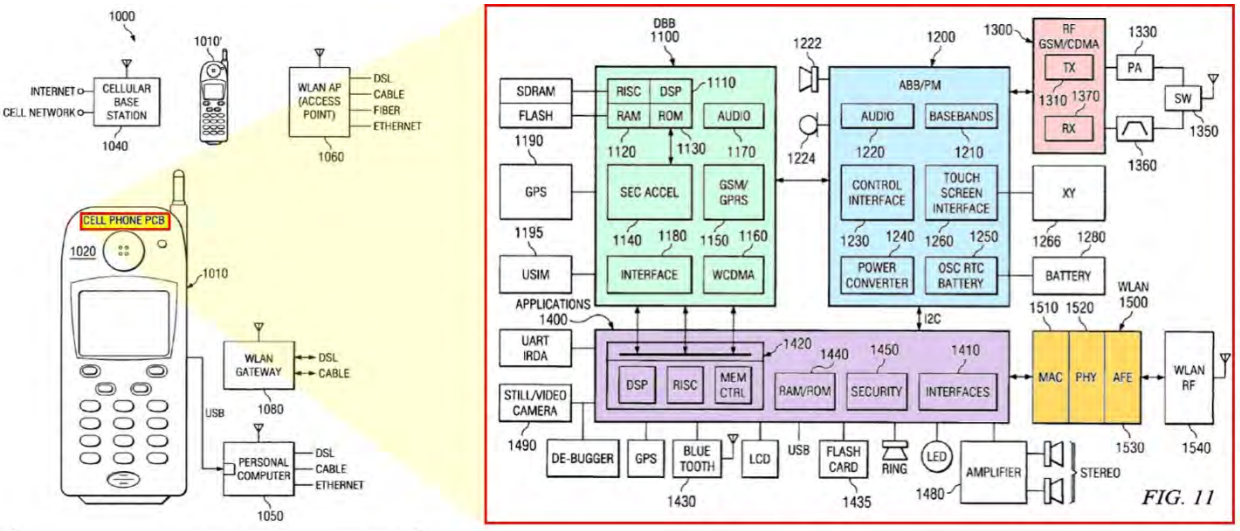


FIG. 10

FIG. 11

[767] *Id.* at 33:62-63.

[768] *Id.* at 33:66-34:2.

[769] *See id.* at 34:23-30, 35:14-20, 35:64-67, 36:15-16, 37:14-17.

[770] *Id.* at 6:48-51; *see also id.* at 32:23-40, Fig. 8.

788. A person of ordinary skill in the art would have understood that these integrated circuits are packaged dies (specifically, individually packaged chips, chiplets within a single package, or a combination thereof) because unpackaged integrated circuits (i.e., processed wafers and unpackaged dies) are used only for testing or to be packaged into integrated circuits.

789. Because *Liu* teaches "the component is a packaged integrated circuit die," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the one resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in the integrated circuits found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "the component is a packaged integrated circuit die."

790. Because the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches every feature in claim 18 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 18 would have been obvious.

9. The Combination of *Tung*, *Brask*, *Yu*, and *Liu* Would Have Rendered Claim 19 Obvious

791. Claim 19 depends from claim 12. I understand that means claim 19 requires all the same features as claim 12, plus the additional features recited in

claim 19. The asserted combination of *Tung*, *Brask, Yu,* and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.D.2.a-p.

792. Claim 19 further recites "the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor." As I explain in Section IX.D.2.c, the asserted combination of *Tung*, *Brask, Yu,* and *Liu* teaches "a component coupled to the board, the component including an integrated circuit structure." And as I explain in Section IX.D.4, the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "a communication chip coupled to the board." The asserted combination of *Tung, Brask, Yu,* and *Liu* also teaches that "the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor."

793. As I explain in Section IX.C.16, a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask,* and *Yu* is a FET structure designed for use in integrated circuits, including processors, communication chips, and digital signal processors (DSPs), that go onto circuit boards of smartphones, computers, and the like. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 19, *Liu*'s teachings make it explicit.

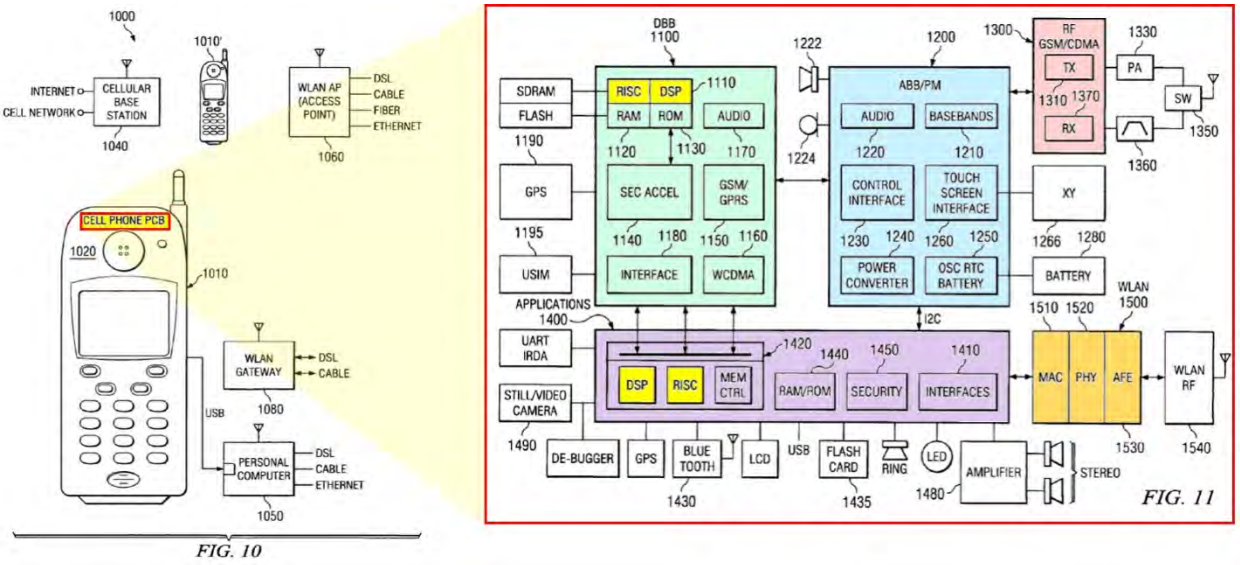
794. *Liu* describes a "cell phone printed circuit board (PCB)" included in the "wireless handset," as Figure 10 below illustrates.[771] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[772] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[773] Coupled to the printed circuit board are various communications chips, including (1) "integrated circuit 1100" (green below), which "supports and provides interfaces for one or more of GSM, GPRS, EDGE, and UMTS (Global System for Mobile communications, General Packet Radio Service, Enhanced Data Rates for Global Evolution, Universal Mobile Telecommunications System) wireless," (2) "mixed-signal integrated circuit 1200" (blue below), which "includes an analog baseband (ABB) block 1210 for GSM/GPRS/EDGE/UMTS," (3) "integrated circuit 1300" (red below), which "includes a GSM/GPRS/EDGE/UMTS RF transmitter block 1310," (4) "integrated circuit chip 1400" (purple below), which includes "WLAN 802.11a/b/g interface circuit 1410 coupled to a WLAN chip 1500," and (5) "a WLAN integrated circuit 1500" (orange below), which "includes MAC (media

[771] *Id.* at 33:46-61.

[772] *Id.* at 33:62-63.

[773] *Id.* at 33:66-34:2.

access controller) 1510, PHY (physical layer) 1520 and AFE (analog front end) 1530" and "is coupled by receive (RX), transmit (Tx) and CONTROL lines to an off-chip WLAN RF circuitry 1540."[774]



795. According to *Liu*, these communication chips are "integrated circuits made by any of the improved processes and including the improved transistors illustrated in the other Figures," which includes FinFET structures.[775] Thus, *Liu* teaches that the component may be a communications chip. Additionally, as I highlight in yellow above, *Liu* teaches that the component may be "a RISC processor (such as MIPS core, ARM processor, or other suitable processor)" or "a digital signal processor (DSP)."[776]

[774] *Id.* at 34:33-42, 35:14-20, 35:64-36:36, 37:14-36.

[775] *Id.* at 6:48-51; *see also id.* at 32:23-40, Fig. 8.

[776] *Id.* at 34:23-30, 36:18-31.

796. Because *Liu* teaches "the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor," and because a person of ordinary skill in the art would have found it obvious to deploy FinFETs (like the one resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in the integrated circuit components found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor."

797. Because the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches every feature in claim 19 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 19 would have been obvious.

10. The Combination of *Tung*, *Brask*, *Yu*, and *Liu* Would Have Rendered Claim 20 Obvious

798. Claim 20 depends from claim 12. I understand that means claim 20 requires all the same features as claim 12, plus the additional features recited in claim 20. The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* includes all the features recited in claim 12 for the reasons I provide in Sections IX.D.2.a-p.

799. Claim 20 further recites "the computing device is selected from the group consisting of a mobile phone, a laptop, a desktop computer, a server, and a

set-top box." The asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "the computing device is selected from the group consisting of a mobile phone, a laptop, a desktop computer, a server, and a set-top box."

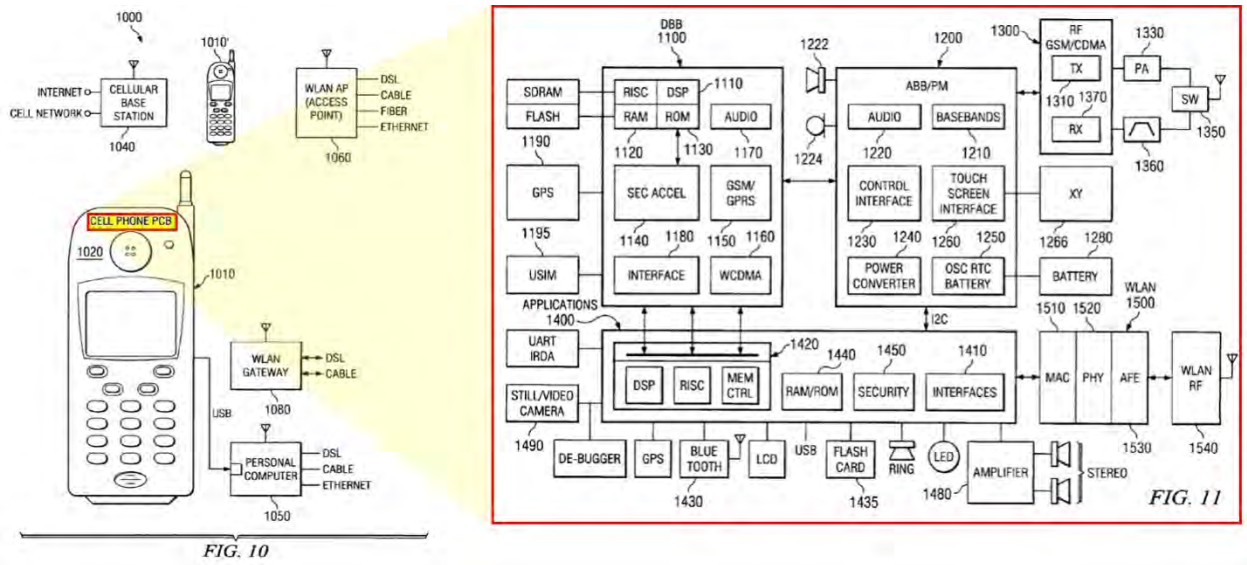
800. As I explain in Section IX.C.17, a person of ordinary skill in the art would have understood the asserted combination of *Tung*, *Brask*, and *Liu* is a FET structure designed for use in integrated circuits that go onto the circuit boards of smartphones, laptops, desktop computers, servers, set-top boxes, and the like. Although a person of ordinary skill in the art would have found this sufficient to satisfy claim 20, *Liu*'s teachings make it explicit.

801. For example, *Liu* describes a "wireless handset," as Figure 10 below illustrates.[777] Additionally, Figure 11 below illustrates "integrated circuit chips for use in the blocks of the communications system 1000 of FIG. 10."[778] "For conciseness of description," *Liu* explains, "the integrated circuits are described with particular reference to use of all of them in the cellular telephone handsets 1010 and 1010'."[779] I annotated the figures below to show this relationship.

[777] *Id.* at 33:46-61.

[778] *Id.* at 33:62-63.

[779] *Id.* at 33:66-34:2.



802. According to *Liu*, Figure 11 above depicts "integrated circuits made by any of the improved processes and including the improved transistors illustrated in the other Figures," which includes FinFET structures.[780] Thus, *Liu* teaches the computing device may be a mobile phone. Although I understand that this is sufficient to satisfy claim 20, *Liu* also describes other electronic devices that incorporate integrated circuits, including "radios and televisions, fixed and portable entertainment units, routers, pagers, personal digital assistants (PDA), organizers, scanners, faxes, copiers, household appliances, [and] office appliances."[781]

803. Because *Liu* teaches "the computing device is selected from the group consisting of a mobile phone, a laptop, a desktop computer, a server, and a set-top box," and because a person of ordinary skill in the art would have found it obvious

[780] *Id.* at 6:48-51; *see also id.* at 32:23-40, Fig. 8.

[781] *Id.* at 34:3-22.

to deploy FinFETs (like the one resulting from the asserted combination of *Tung*, *Brask*, and *Yu*) in the integrated circuit components found on the circuit board of *Liu*'s computing device, a person of ordinary skill in the art would have understood that the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches "the computing device is selected from the group consisting of a mobile phone, a laptop, a desktop computer, a server, and a set-top box."

804. Because the asserted combination of *Tung*, *Brask*, *Yu*, and *Liu* teaches every feature in claim 20 and a person of ordinary skill in the art would have found it obvious to combine their teachings, it is my opinion that claim 20 would have been obvious.

X. Conclusion

805. As discussed above, it is my opinion that the Challenged Claims of the '281 Patent are unpatentable because they would have been obvious to a person of ordinary skill in the art.

806. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I

will appear for cross-examination within the United States during the time allotted for cross-examination.

807. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

808. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 22nd day of June, in Gainesville, FL.

By: 

Dr. Scott E. Thompson, Ph.D.

Appendix A

SCOTT EMMET THOMPSON

Prof. Electrical Engineering and Computer Science Department / Univ. of Florida
IEEE Fellow for contributions on advancing MOSFETs
Former Intel Corporation Fellow and Director of Computer Chip Technology

A. Education and Training

Education

1992 Ph.D. (Electrical Engineering), University of Florida
1988 Master of Science in Electrical Engineering, University of Florida
1987 Bachelor of Electrical Engineering with Highest Honors, University of Florida

B. Professional Experience

- Tenure Full Professor and Faculty/ Electrical and Computer Engineering, University of Florida (2/2004 to present).
- Founder and CTO of SuVolta (a low power chip company) (2009 - 2/2015).
    - Technology sold to Fujitsu and used in Mibeaut image sensor processor
- Researcher on advanced chip technology at University of Florida totaling $4M worth of research contracts.
    - 2019-2021 Research funding from Semiconductor Research Corporation (SRC)
- Consultant in semiconductor/computer chip industry (non litigation) last last 10 years: Cypress Semiconductor, Xperi Corporation, Intermolecular Inc, SuVolta, International Electron Device Meeting.
- **Intel Corporation** 1992 to 2004. Intel Fellow (highest technical level) and Director of computer chip technology (semiconductor manufacturing) including transferring and bringing up new manufacturing facilities worldwide.
- Intel Corporation experience and industry consulting on semiconductor manufacturing, semiconductor technology, yield and quality.
- Developed ultra low power chip technology for image sensors, SOC, RFIC, Memory, CPU, image sensors processors and other chips.
- Developed graduate level courses at University of Florida on advanced semiconductor chip, semiconductor design and packaging technology (chip stacking) and computer chip technology including CPU, DRAM, GPU, image sensors, 2D and 3D image sensor processing.
- National Science Foundation Panel Reviewer for semiconductor/computer chip funding.

C. Legal cases (6 depositions and 3 time testimony at trial**)**

- Bold is the client
  - Amberwave v. **Intel Corporation** 2005-2006
  - Siliconix v. **Alpha Omega Semiconductor** 2007-2008
    - Exert report Jan, 2008 Judicial Arbitration and Mediation Service Ref 1110009946
    - Deposition Feb 6, 2008
    - Testimony at Trial Feb 2008
  - National Semiconductor v. **Alpha Omega Semiconductor** 2008-2009
  - **Intellectual Ventures** v. Canon
    - Expert report and deposition
    - Expert report: Oct 19, 2015 No. 1:11:00792-SLR - filed 9/9/2011
    - Deposition: United State district court for the District of Delaware, Nov 10th 2015 No. 11-792
  - **Round Rock Research, LLC** v. Nintendo Co., LTD and Ricoh Americas Corp
    - Declaration claims construction brief for Markman hearing
    - Declaration 01-21-2016 C. A. No. 1:14-cv-1491-SLR-SRF (D. Del.) - filed 12/17/2014
    - Supplemental Declaration 04-05-2016, C. A. No. 1:15-cv-157-SLR-SRF (D. Del.) - filed 2/13/2015
  - **Labaton Sucarow** /**Motley Rice LLP** v. Advanced Micro Devices, Inc.
    - Amended class action complaint, United States District Court Northern District of California, 05/23/14, No. 3:14-cv-00226-JD - filed 1/15/2014
    - Expert Report (Nov/2016), Rebuttal Report(Jan/2017) and Deposition (March/2017)
  - Godo Kaisha IP Bridge v/ **Xilinx**/**TSMC**
    - 7/2017 - 2018 Industry and expert witness
    - Case No. 2:17-CV-00100-JRG-RSP (E.D. Tex.) - filed 1/31/2017
  - KAIST IP v. **Apple**
    - 2018-2019 Industry and expert witness
    - Feb/2018 File report for Apple to Korea Trade Commission
    - May/2018 Supplemental Report to Korea Trade Commission
    - March /2019 Report to Intellectual Property Trial and Appeals board regarding Korean Patent No. 10-0458288
    - Case in Korea : Intellectual Property Trial and Appeal Board ("IPTAB") regarding Korean Patent No. 10-0458288 (hereinafter, "KR '288 patent").
  - IP Bridge, Inc. v. **NVIDIA** Godo Kaisha
    - NVIDIA Singapore Pte Ltd. as a technical expert in the customs proceeding initiated by petitioner Godo Kaisha IP Bridge 1

- Chinese Academy of Sciences v. **Intel**
  - IPR report Sept / 2018 in case IPR2018-01574 - filed 9/18/2018
  - IPR report Mar / 2019 in case IPR2019-00834 - filed 3/19/2019
  - Beijing Court Testimony IME vs Lenovo 11/21/2021
  - Beijing court Testimony IME vs Intel China 1/12/2022
- IFT v. **TSMC (**ITC case)
  - Case 1:19-cv-00308-UNA (D. Del.) - filed 2/13/2019
  - Inv. No. 337-TA-1149 - initial notice 4/3/2019
- NXP v. **Impinj**
  - 9,495,631, IPR2020-00543 - filed 2/10/2020
  - 9,633,302, IPR2020-00516 - filed 2/5/2020
  - 6,680,523, IPR2020-01630 - filed 9/17/2020
    - Deposition 7/7/2021
  - 7,538,444, IPR2021-00003 - filed 10/5/2020
  - Infringement Report 6/17/2022
    - Deposition Infringement Report 9/6/2022
  - Validity Report 8/16/2022
    - Deposition Validity Report 9/7/2022
- Katana Silicon Technology LLC v. **Global Foundry** 2022
  - IPR2022-01083
- Ericsson v. **Apple** 2022
- Greenthread v. **Intel** 2022
- ITC Daedalus v. **TSMC** 2023

Honors and Awards

- 100 granted US patents, 60 publications and 1 book on semiconductors
- Elected to **IEEE Fellow** in 2006 for Advancing Fabrication of nanoscale MOSFET
- Elected to Intel Fellow in 2003
- Thompson and co-workers were the first to publish at the International Electron Device Meeting (IEDM) in 2002 on a 90nm logic technology which introduced high levels of strain for significant mobility enhancement using SiGe
- 2008 SEMI award North American Recipient
- 2014 TiE 50: Top Startup (SuVolta)
- 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology: SuVolta
- 2011 EuroAsia IC Industry Award for start-up
- 2008 Semi Award North America (for Develop of Strained Silicon Transistors)

D. Publications/Patents

[1] T. A. Weingartner, C. -H. Kuo, A. Thomas, S. E. Thompson and M. E. Law, "Negative Impact of Compressive Biaxial Stress on High Precision Bipolar Devices," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, doi: 10.1109/TCPMT.2021.3095670.
[2] C.-H. Kuo, T. A. Weingartner, M. E. Law, S. E. Thompson, and A. Appaswamy, *Effect of Stress on Bipolar Transistor,* SRC TECHCON 2021

[3] S. E. Thompson et al., "Digital Circuits Having Improved Transistors, and Methods therefor" US Patent 10,250,257, 2019.

[4] S. E. Thompson et al., "Advanced Transistors with Punch Through Suppression", US Patent US10325986B2, 2019.

[5] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent 10,217,668, 2019.

[6] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent 10224244B2, 2019.

[7] S. E. Thompson et al., "Digital Circuits Having Improved Transistors, and Methods therefor" US Patent US20180248548A1, 2018.

[8] S.E. Thompson et.al., "Low Power Semiconductor Transistor Structure and Method of Fabrication Thereof", US9865596B2, 2018.

[9] S.E. Thompson et al. "Integrated Circuit Devices and Methods", US Patent US9966130B2, 2018

[10] S.E. Thompson et al. "Buried Channel Deeply Depleted Channel Transistor, US Patent US9991300B2, 2018.

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[12] S.E. Thompson et al., Transistor With Threshold Voltage Set Notch and Method of Fabrication Thereof" US Patent US9922977B2, 2018.

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Appendix B

Appendix B

List of Materials Cited in Declaration of Dr. Scott E. Thompson, Ph.D. in Support of Petition for Inter Partes *Review of U.S. Patent No. 11,251,281*

Citation	Exhibit
U.S. Patent No. 11,251,281 to Glass et al. ("'281 Patent").	**1001**
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