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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/872,844	06/28/2016	9379233	74735/258	1965

130036 7590 06/08/2016
IIPH2 [54361] c/o Stoel Rives LLP 130036
201 South Main Street, Suite 1100, One Utah Center
Salt Lake City, UT 84111

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Yoshihiro TAKAISHI, Tokyo, JAPAN;
PS4 Luxco S.a.r.l., Luxembourg, LUXEMBOURG;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

130036 7590 03/03/2016
IIPH2 [54361] c/o Stoel Rives LLP 130036
201 South Main Street, Suite 1100, One Utah Center
Salt Lake City, UT 84111

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/872,844	10/01/2015	Yoshihiro TAKAISHI	74735/258	1965

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	06/03/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
COLEMAN, WILLIAM D	2823	257-334000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

PS4 Luxco S.a.r.l.

Luxembourg, LU

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☒ Payment by credit card. ~~Form PTO-2018 is attached~~
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 502375 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Joseph J. Hawkins/

Date June 1, 2016

Typed or printed name Joseph J. Hawkins

Registration No. 63,194

Electronic Patent Application Fee Transmittal

Application Number:	14872844			
Filing Date:	01-Oct-2015			
Title of Invention:	SEMICONDUCTOR DEVICE			
First Named Inventor/Applicant Name:	Yoshihiro TAKAISHI			
Filer:	Joseph Jackson Hawkins/Janet Wilson			
Attorney Docket Number:	74735/258			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	25935194
Application Number:	14872844
International Application Number:	
Confirmation Number:	1965
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro TAKAISHI
Customer Number:	130036
Filer:	Joseph Jackson Hawkins/Janet Wilson
Filer Authorized By:	Joseph Jackson Hawkins
Attorney Docket Number:	74735/258
Receipt Date:	01-JUN-2016
Filing Date:	01-OCT-2015
Time Stamp:	14:19:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	677
Deposit Account	502375
Authorized User	HAWKINS, JOSEPH J.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination process fees)

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2016_06_01_CommentsonReasonsforAllowance.pdf	360548	no	2
			d8e8bc6668206b03a2fd7e8469c6d8393952a44		
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	2016_06_01_PartB.pdf	86694	no	1
			5c998b0178530a89e56e31694ced5d3ef7939316		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30698	no	2
			1015bfff6795a24720dbe3bdebb1a6a7c2bf3657		
Warnings:					
Information:					
Total Files Size (in bytes):			477940		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First named inventor:

Yoshihiro TAKAISHI

Application No. 14/872,844

Filed: October 1, 2015

For: **SEMICONDUCTOR DEVICE**

Group Art Unit: 2823

Examiner: COLEMAN, William D.

Confirmation No. 1965

Docket No. 74735/258

Dated: June 1, 2016

COMMENTS ON REASONS FOR ALLOWANCE

The Applicant appreciates the allowance of the claims of the above-referenced Application, and agrees that the claimed subject matter is patentable. The Applicant takes no position regarding the Reasons for Allowance adopted by the Examiner (if any) other than the positions the Applicant may have previously taken during prosecution of the Application. Therefore, such Reasons for Allowance (if any) should not be attributed to the Applicant as an indication of the basis for the Applicant's belief that the claims are patentable. Furthermore, the Applicant respectfully asserts that there may also be additional reasons for patentability of the claimed subject matter not explicitly stated in this record, and the Applicant does not waive their rights to make such arguments by not further addressing such reasons herein. Moreover, the Applicant respectfully submits that there may be additional, unclaimed subject matter disclosed in the Application and explicitly reserves the right to pursue such subject matter in one or more continuation, divisional, and/or continuation-in-part applications.

The Commissioner is hereby authorized to charge any ***additional*** fees which may be required in connection with filing of this paper, or credit overpayment, to Deposit Account No. 50-2375.

Respectfully submitted,

/Joseph J. Hawkins/
Joseph J. Hawkins
Registration No. 63,194

STOEL RIVES LLP
201 S Main Street, Suite 1100
Salt Lake City, UT 84111-4904
Telephone: (801) 328-3131
Facsimile: (801) 578-6999

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14/872,844
	Filing Date		2012-12-19
	First Named Inventor	Yoshihiro TAKAISHI	
	Art Unit	2523	
	Examiner Name		
	Attorney Docket Number	8040-1178	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/WDC/	1	7945272		2011-05-17	KIM	Corresponds to 2006-081184
/WDC/	2	6813714		2004-11-02	HARDJONO et al.	English language
/WDC/	3	6584566		2003-06-24	HARDJONO	English language
If you wish to add additional U.S. Patent citation information please click the Add button.						Add
U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/WDC/	1	20100011063		2010-01-14	BLAIOTTA et al.	Corresponds to 2008-543137
/WDC/	2	20070071021		2007-03-29	GIRAO	Corresponds to 2007-089156
/WDC/	3	20060063548		2006-03-23	KIM	Corresponds to 2006-081184

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14/872,844
Filing Date	2012-12-19
First Named Inventor	Yoshihiro TAKAISHI
Art Unit	2823
Examiner Name	
Attorney Docket Number	8040-1178

/WDC/	4	20090024848		2009-01-22	TAKASUGI et al.	Corresponds to WO2007/072814
/WDC/	5	20110072121		2011-03-24	TAKASUGI et al.	Corresponds to WO2007/072814
/WDC/	6	20030044020		2003-03-06	ABOBA et al.	English language
/WDC/	7	20030177267		2003-09-18	ORAVA et al.	English language

If you wish to add additional U.S. Published Application citation information please click the Add button. **Add**

FOREIGN PATENT DOCUMENTS

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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² i	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
/WDC/	1	WO2007/072814	WO		2007-06-28		English abstract	☐
/WDC/	2	2006-081184	JP		2006-03-23		English abstract	☐
/WDC/	3	2007-089156	JP		2007-04-05		English abstract	☐
/WDC/	4	2008-257340	JP		2008-10-23		English abstract	☐
/WDC/	5	2008-543137	JP		2008-11-27		English abstract	☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		14/872,844
Filing Date		2012-12-19
First Named Inventor	Yoshihiro TAKAISHI	
Art Unit	2823	
Examiner Name		
Attorney Docket Number	8040-1178	

/WDC/	6	2009-081389	JP		2009-04-16		Cited in the specification, English abstract	☐
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If you wish to add additional Foreign Patent Document citation information please click the Add button **Add**

NON-PATENT LITERATURE DOCUMENTS

Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/William Coleman/	Date Considered	03/14/2016
--------------------	-------------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2012-12-19
First Named Inventor	Yoshihiro TAKAISHI
Art Unit	
Examiner Name	
Attorney Docket Number	8040-1178

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Eric Jensen/	Date (YYYY-MM-DD)	2012-12-19
Name/Print	Eric Jensen	Registration Number	37855

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/872,844	10/01/2015	Yoshihiro TAKAISHI	74735/258	1965

130036 7590 03/17/2016
IIPH2 [54361] c/o Stoel Rives LLP 130036
201 South Main Street, Suite 1100, One Utah Center
Salt Lake City, UT 84111

EXAMINER

COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
----------	--------------

2823

NOTIFICATION DATE	DELIVERY MODE
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03/17/2016

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

joe.hawkins@stoel.com
slcpatent@stoel.com
janet.wilson@stoel.com

**Corrected
Notice of Allowability**

Application No.
14/872,844

Examiner
W DAVID COLEMAN

Applicant(s)
TAKAISHI, YOSHIHIRO

Art Unit
2823

**AIA (First Inventor to File)
Status**
No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-4. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date 10/01/2015
- ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
- ☒ Interview Summary (PTO-413),
Paper No./Mail Date 20161314.
- ☐ Examiner's Amendment/Comment
- ☐ Examiner's Statement of Reasons for Allowance
- ☐ Other _____.

/WILLIAM COLEMAN/
Primary Examiner
Art Unit: 2823

<i>Examiner-Initiated Interview Summary</i>	Application No. 14/872,844	Applicant(s) TAKAISHI, YOSHIHIRO	
	Examiner W DAVID COLEMAN	Art Unit 2823	

All participants (applicant, applicant's representative, PTO personnel):

(1) W DAVID COLEMAN. (3) _____.

(2) Joe Hawkins 63,194. (4) _____.

Date of Interview: 11 March 2016.

Type: ☒ Telephonic ☐ Video Conference
 ☐ Personal [copy given to: ☐ applicant ☒ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
 If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
 (For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1-4.

Identification of prior art discussed: IDS dated 10/01/2015.

Substance of Interview
 (For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant's representative indicated that pursuant to MPEP 609.02, Applicant(s) expected the Examiner to consider all the references submitted in parent application 13/722,125.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/W DAVID COLEMAN/ Primary Examiner, Art Unit 2823	
--	--



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

130036 7590 03/03/2016
IIPH2 [54361] c/o Stoel Rives LLP 130036
201 South Main Street, Suite 1100, One Utah Center
Salt Lake City, UT 84111

EXAMINER

COLEMAN, WILLIAM D

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 03/03/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

14/872,844

10/01/2015

Yoshihiro TAKAISHI

74735/258

1965

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	06/03/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

130036 7590 03/03/2016
IIPH2 [54361] c/o Stoel Rives LLP 130036
201 South Main Street, Suite 1100, One Utah Center
Salt Lake City, UT 84111

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/872,844	10/01/2015	Yoshihiro TAKAISHI	74735/258	1965

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	06/03/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
COLEMAN, WILLIAM D	2823	257-334000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/872,844	10/01/2015	Yoshihiro TAKAISHI	74735/258	1965
130036 7590 03/03/2016 IIPH2 [54361] c/o Stoel Rives LLP 130036 201 South Main Street, Suite 1100, One Utah Center Salt Lake City, UT 84111			EXAMINER COLEMAN, WILLIAM D	
			ART UNIT	PAPER NUMBER
			2823	
DATE MAILED: 03/03/2016				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/872,844	Applicant(s) TAKAISHI, YOSHIHIRO	
	Examiner W DAVID COLEMAN	Art Unit 2823	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to October 1, 2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-4. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some *c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 13/722,125.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____ |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____ | |

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Art Unit: 2823

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed October 1, 2015 has been misplaced by the Office.

Please resubmit.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Allowable Subject Matter

3. Claims 1-4 allowed.
4. The following is an examiner's statement of reasons for allowance: the prior art does not anticipate nor render obviousness with respect to a semiconductor device comprising amongst other limitations: a plurality of semiconductor pillars provided on a semiconductor substrate each having a upper diffusion layer and a lower diffusion layer with a side contact plug connected to the lower diffusion layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to W DAVID COLEMAN whose telephone number is (571)272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W DAVID COLEMAN/
Primary Examiner, Art Unit 2823

CPC Classification - Application Number: 14872844

Examiner: William Coleman **Date Created:** Feb 22, 2016 1:47 PM

Family ID: 48653688

US App. No. (2) & Documents (3): 14/872844 (20160020316 A1), 13/722125 (20130161738 A1, 9178056 B2)

Foreign Documents (1): JP2013153133A

Allocations (6)

No.	CPC	Type			Endorsed By	CPC Version	IPC
1	H01L 29/7802	F			US	2013-01-01	H01L29/78
2	H01L 29/66666	I			EP, US	2013-01-01	H01L29/66
3	H01L 27/088	I			EP, US	2013-01-01	H01L27/088
4	H01L 29/7827	I			EP, US	2013-01-01	H01L29/78
5	H01L 29/7813	I			US	2013-01-01	H01L29/78
6	H01L 21/823487	A			EP, US	2013-01-01	H01L21/8234

Combination Sets (0)

No.	CPC	Type	Set	Rank	Endorsed By	CPC Version	IPC
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	213085	pillar	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:32
S2	1124	silicon adj plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:32
S3	54	S1 and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:32
S4	2519	(438/268).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:32
S5	0	conductive adj padt	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:33
S6	16535	conductive adj pad	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:33
S7	6	S4 and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:33
S8	589912	interconnect	US-PGPUB;	OR	OFF	2014/08/20

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			06:34
S9	238	S4 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:34
S10	36642	multiple adj vias or multiple adj holes or multiple adj openings	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:36
S11	0	S5 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:36
S12	2	conductive adj pad near4 (multiple adj vias or multiple adj holes or multiple adj openings)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:37
S13	405950	fuse or anti adj fuse	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:38
S14	571	S6 and S13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:38
S15	3653087	semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:39
S16	305	S14 and S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2014/08/20 06:39

			IBM_TDB			
S17	6815	vertical adj transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:40
S18	0	S16 and S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:40
S19	0	H01L27/78.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:44
S20	12780	H01L29/78.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:45
S21	10471	elpida adj memory.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:45
S22	65	S20 and S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:45
S23	2016923	laser	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:54
S24	48140	S13 and S23	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:54
S25	226	S6 and S24	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2014/08/20 06:55

			EPO; JPO; DERWENT; IBM_TDB			
S26	4275	via adj array	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:56
S27	54	S6 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/08/20 06:57
S28	10	("20030020163" "20050280149" "20060091566" "20060097406" "20060125118" "7233075" "7291865" "7538434").PN. OR ("8178980").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/08/20 06:59
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APPLICANTS PS4 Luxco S.a.r.l., Luxembourg, LUXEMBOURG; INVENTORS Yoshihiro TAKAISHI, Tokyo, JAPAN; ** CONTINUING DATA ***** This application is a CON of 13/722,125 12/20/2012 PAT 9178056 ** FOREIGN APPLICATIONS ***** JAPAN 2011-285544 12/27/2011 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 10/15/2015						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/W DAVID COLEMAN/</u> Examiner's Signature		☐ Met after Allowance <u>/WDC/</u> Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 10	TOTAL CLAIMS 4	INDEPENDENT CLAIMS 1
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TITLE SEMICONDUCTOR DEVICE						
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H01L		27	/	088	I	2013-01-01
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This is to certify that the annexed is a true copy of the following application as filed with this Office.

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The country code and number
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to be used for filing abroad
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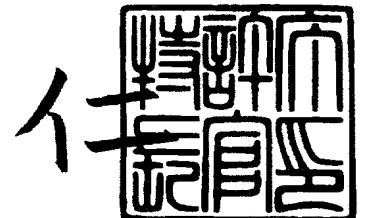
J P 2 0 1 1 - 2 8 5 5 4 4

出 願 人 マイクロンメモリジャパン株式会社
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【書類名】明細書

【発明の名称】半導体装置および半導体装置の製造方法

【技術分野】

【0001】

本発明は、半導体装置および半導体装置の製造方法に関する。

【背景技術】

【0002】

近年、トランジスタの微細化の技術として、縦型トランジスタが提案されている。

【0003】

縦型トランジスタは、半導体基板の主面に対して垂直方向に延びる半導体ピラーをチャネルとして用いるトランジスタである。

【0004】

具体的には、縦型トランジスタは、半導体基板から立ち上がるように半導体ピラー（基柱）が設けられており、半導体ピラーの周囲にはゲート絶縁膜を介してゲート電極が設けられている。半導体ピラーの下部の横側にはドレイン領域およびドレイン電極が設けられ、半導体ピラーの上部にはソース領域及びソース電極が設けられている（特許文献1）。

【0005】

この縦型トランジスタはチャネルを基板平面に平行に配置した従来のトランジスタと比べて、平面上の占有面積が小さく、チャネル長（ゲート長）を長くしてもトランジスタの平面上の占有面積の増加がない。

【0006】

そのため、トランジスタの平面上の占有面積を大きくしなくても短チャネル効果が抑制できる。またチャネルの完全空乏化が可能となり、良好なS値（Subthreshold swing value）および大きなドレイン電流が得られるという利点を有している。

【0007】

また縦型トランジスタは、チャネル部の全周に亘ってゲート電極が形成されており（ゲート電極で覆われており）、ソース・ドレイン以外の外的要因に左右されることなく、チャネルの電位をゲート電極で効果的に制御可能である。

【先行技術文献】

【特許文献】

【0008】

【特許文献1】特開2009-081389号公報

【発明の概要】

【発明が解決しようとする課題】

【0009】

ここで、縦型トランジスタを用いた半導体装置は、トランジスタの特性を維持しつつ、高い電流駆動能力を得るために、半導体ピラーを複数設けて、それら複数の半導体ピラーの上下部に設けた上部拡散層と下部拡散層を夫々並列に接続する場合がある。この際、半導体ピラーの上部拡散層に接続させる上部コンタクトプラグと半導体ピラー間における電気抵抗のばらつきは、上部拡散層が半導体ピラーの上端に設けられるという構造上、上部コンタクトプラグの接続位置が限定されるので、許容程度となっている。しかし、半導体ピラーの下部拡散層に接続させる下部コンタクトプラグと半導体ピラー間における電気抵抗のばらつきは、下部拡散層と下部コンタクトプラグの接続位置によって大きく変動するために、平面視において半導体ピラーと下部コンタクトプラグの最長間隔が最短間隔の2倍以上になると、複数の半導体ピラーに設けられた夫々のトランジスタ特性がばらつく問題があった。

【0010】

本発明は、このような問題に鑑みてなされたもので、その目的は、複数の縦型トランジスタを接続した構造でも、個々の半導体ピラーに設けられたトランジスタの特性を安定化させることが可能な半導体装置を提供することにある。

【課題を解決するための手段】

【0011】

前述した目的を達成するために、本発明の第1の態様は、半導体基板から立ち上がるように設けられ、前記半導体基板側の端部に拡散層を有する複数の縦型トランジスタと、前記半導体基板から立ち上がるように設けられ、複数の前記縦型トランジスタの前記拡散層に接続される導電プラグと、を有し、複数の前記縦型トランジスタは、前記導電プラグの周囲に均等配置され、前記拡散層および前記導電プラグを共有している、半導体装置である。

【0012】

本発明の第2の態様は、(a)半導体基板から立ち上がるように、複数の縦型トランジスタを形成し、複数の前記縦型トランジスタの前記半導体基板側の端部に、拡散層を、複数の縦型トランジスタが共有するように設け、(b)前記半導体基板から複数の前記縦型トランジスタの前記拡散層に接続される導電プラグを立ち上がるように設ける、を有し、前記(a)は、複数の前記縦型トランジスタを、前記導電プラグを設ける部分の周囲に均等配置する、半導体装置の製造方法である。

【発明の効果】

【0013】

本発明によれば、複数の縦型トランジスタを接続した構造でも、個々の半導体ピラーに設けられたトランジスタの特性を安定化させることが可能な半導体装置を提供することができる。

【図面の簡単な説明】

【0014】

【図1】第1の実施形態に係る半導体装置100の構造を示す模式図（平面図）であって、構成要素の配置状況を明確にするため、層間絶縁膜並びにコンタクトプラグ上に位置している配線を透過状態として、その輪郭だけを点線で記載している。

【図2】図1のX1-X1'断面図である。

【図3】図1のY1-Y1'断面図である。

【図4】第2の実施形態に係る半導体装置100aの構造を示す模式図（平面図）である。

【図5】第3の実施形態に係る半導体装置100bの構造を示す模式図（平面図）である。

【図6】第4の実施形態に係る半導体装置100cの構造を示す模式図（平面図）である。

【図7】第5の実施形態に係る半導体装置100dの構造を示す模式図（平面図）である。

【図8】第1の実施形態に係る半導体装置100の製造方法を説明するための図（平面図）である。

【図9】図8のX1-X1'断面図である。

【図10】第1の実施形態に係る半導体装置100の製造方法を説明するための図（平面図）である。

【図11】図10のX1-X1'断面図である。

【図12】図10のY1-Y1'断面図である。

【図13】第1の実施形態に係る半導体装置100の製造方法を説明するための図（平面図）である。

【図14】図13のX1-X1'断面図である。

【図15】図13のY1-Y1'断面図である。

【図16】第1の実施形態に係る半導体装置100の製造方法を説明するための図（断面図）である。

【図17】第1の実施形態に係る半導体装置100の製造方法を説明するための図（断面図）である。

【図18】第1の実施形態に係る半導体装置100の製造方法を説明するための図（平面図）であって、構成要素の配置状況を明確にするため、最上層の下地となった構成要素を破線で記載している。

【図19】図18のX1-X1'断面図である。

【図20】図18のY1-Y1'断面図である。

【発明を実施するための形態】

【0015】

以下、図面に基づいて本発明に好適な実施形態を詳細に説明する。

【0016】

まず、図1を参照して、本発明の第1の実施形態に係る半導体装置100の概略構成を説明する。

【0017】

図1に示すように、第1の実施形態に係る半導体装置100は、半導体基板としてのシリコン基板1から立ち上がるように設けられた縦型トランジスタである第1の単位トランジスタ50A₁、第2の単位トランジスタ50A₂、第3の単位トランジスタ50A₃、第4の単位トランジスタ50A₄、および第5の単位トランジスタ50A₅と、各単位トランジスタのシリコン基板1側の端部に設けられ、各単位トランジスタに共有されるピラ一下部拡散層9と、シリコン基板1から立ち上がるように設けられ、ピラ一下部拡散層9に接続された導電プラグとしてのメタルコンタクトプラグ31を有しており、各々の単位トランジスタは後述するように、メタルコンタクトプラグ31を共有しており、1つの並列トランジスタを構成している。

【0018】

また、各単位トランジスタはメタルコンタクトプラグ31の周囲に均等配置されている。なお、「均等配置」とは、第1の実施形態では、平面視において、メタルコンタクトプラグ31から最も距離が近い単位トランジスタと最も遠い単位トランジスタの距離の差が2倍以内になるような配置を指すものとする。

【0019】

次に、図1を参照して、半導体装置100の構成について、さらに詳細に説明する。

【0020】

図1に示すように、半導体装置100は、STI (Shallow Trench Isolation) 2に囲まれた活性領域となる領域Aを有し、領域A内に、シリコン基板1の表面から立ち上がるように（Z方向に向けて突出するように）設けられた第1のシリコンピラー5A₁、第2のシリコンピラー5A₂、第3のシリコンピラー5A₃、第4のシリコンピラー5A₄、および第5のシリコンピラー5A₅の5つのシリコンピラーが設けられている。各々のシリコンピラーは、X方向の幅およびY方向の幅が同一の矩形となるように構成されている。ここでは幅を50nmとする。なお、各々のシリコンピラーの平面形状は、矩形に限らず、円形であっても良い。円形の場合は直径を50nmとする。

【0021】

各々のシリコンピラーは、単位トランジスタのチャネル部を構成するものである。すなわち、第1のシリコンピラー5A₁、第2のシリコンピラー5A₂、第3のシリコンピラー5A₃、第4のシリコンピラー5A₄、および第5のシリコンピラー5A₅の5つのシリコンピラーは、第1の単位トランジスタ50A₁、第2の単位トランジスタ50A₂、第3の単位トランジスタ50A₃、第4の単位トランジスタ50A₄、および第5の単位トランジスタ50A₅の5つの単位トランジスタに各々対応している。

【0022】

5つの単位トランジスタは、平面視で凹形状となるように配置されている。すなわち、第1の単位トランジスタ50A₁と第2の単位トランジスタ50A₂の2つの単位トランジスタがX方向の同一線上に中心が位置するように一定の間隔で配置される。ここでは、その間隔を30nmとしている。また、第2の単位トランジスタ50A₂、第3の単位トランジスタ50A₃、第4の単位トランジスタ50A₄の3つの単位トランジスタがY方

向の同一線上に中心が位置するように一定の間隔で配置される。ここでは、各々の単位トランジスタの間隔を30nmとしている。さらに、第4の単位トランジスタ50A₄と第5の単位トランジスタ50A₅の2つの単位トランジスタがX方向の同一線上に中心が位置するように一定の間隔で配置される。ここでは、その間隔を30nmとしている。第1の単位トランジスタ50A₁および第2の単位トランジスタ50A₂と、第5の単位トランジスタ50A₅および第4の単位トランジスタ50A₄とは、第3の単位トランジスタ50A₃の中心を通してX方向に延在する線分に対して線対称の位置に配置されている。これにより、5つの単位トランジスタの配置は凹形状となっている。

【0023】

各々の単位トランジスタの直上には、シリコンプラグ19、メタルコンタクトプラグ30及びメタル配線33が配置されている。各々の単位トランジスタと、シリコンプラグ19及びメタルコンタクトプラグ30は、平面視において、同一領域内で互いに重なって配置されている。メタル配線33は、5つの単位トランジスタの配置に沿って凹形状となるようにXY方向へ延在して配置されている。メタル配線33は、メタルコンタクトプラグ30を介して、各々のシリコンピラーの上部に形成され、各々の単位トランジスタを構成するピラー上部拡散層16と接続されており、各々の単位トランジスタへの給電配線となっている。このように、5つの単位トランジスタは、メタル配線33によって並列に接続されており、1つの並列トランジスタを構成している。

【0024】

一方、第3のシリコンピラー5A₃とX方向に隣接するように、平面視矩形形状のゲート吊りシリコンピラー6が一定の間隔で、シリコン基板1から立ち上がるように配置されている。ここでは、その間隔を30nmとしている。ゲート吊りシリコンピラー6の直上には、平面視矩形形状のメタルコンタクトプラグ41が配置されている。メタルコンタクトプラグ41は、平面視において、ゲート吊りシリコンピラー6と部分的に重なる位置に配置されているが、X方向においてゲート吊りシリコンピラー6の外側に若干はみ出した構成となっている。なお、図1では、メタルコンタクトプラグ41がゲート吊りシリコンピラー6に対してX方向にオフセットしているが、これに限るものではなく、各々のシリコンピラーに接触しない範囲の任意の位置でY方向にオフセットされても良い。

【0025】

また、隣接するシリコンピラーの隙間及び第3のシリコンピラー5A₃とゲート吊りシリコンピラー6の隙間を覆って、各々のシリコンピラーとゲート吊りシリコンピラー6の側面全体にゲート電極11（図2、図3参照）が設けられている。上記のメタルコンタクトプラグ41は、上記のはみ出した部分でゲート吊りシリコンピラー6の側面に設けられたゲート電極11と接続されている。ゲート電極11の平面視の厚さ（図2におけるX方向の厚さ）は20nmとしている。

【0026】

ゲート電極の厚さを20nmとしているので、前述のように30nmとした各々のシリコンピラー同士の間隔は、ゲート電極11の厚みの2倍以下とされている。第1のシリコンピラー5A₁～第5のシリコンピラー5A₅の側面に設けられた厚さ20nmのゲート電極11は、各々のシリコンピラー間隔がゲート電極11の膜厚の2倍以下とされた30nmの部分で互いに接触し、1つのゲート電極として機能する。

【0027】

前述のように、第3のシリコンピラー5A₃とゲート吊りシリコンピラー6との間隔も30nmとしているので、ゲート電極11の厚みの2倍以下となっている。第3のシリコンピラー5A₃の側面とゲート吊りシリコンピラー6の側面に設けられた厚さ20nmのゲート電極11は、各々のピラー間隔がゲート電極11の膜厚の2倍以下とされた30nmの部分で互いに接触し、第3のシリコンピラー5A₃とゲート吊りシリコンピラー6に共通のゲート電極となっている。従って、ゲート吊りシリコンピラー6のゲート電極11から供給されたゲート電圧は、第3のシリコンピラー5A₃のゲート電極11を介して、第1のシリコンピラー5A₁と第2のシリコンピラー5A₂と第4のシリコンピラー5A₄と第5のシリコンピラー5A₅に供給される。

4と第5のシリコンピラー5 A₅のゲート電極1 1に供給される。

【0028】

メタルコンタクトプラグ4 1の直上には、ゲート吊り配線4 2が配置されている。ゲート吊り配線4 2は、平面視で直線状に設けられており、メタル配線3 3と交わらないように一方のX方向へ延在して配置されている。ゲート吊り配線4 2の端部は、メタルコンタクトプラグ4 1を介して、各々の単位トランジスタ5 0 Aを構成するゲート電極1 1と接続されている。

【0029】

凹形状に配置された5つの単位トランジスタの内側で、2つの単位トランジスタ（第1の単位トランジスタ5 0 A₁と第5の単位トランジスタ5 0 A₅）で挟まれた領域の中央部には、平面視で円形のメタルコンタクトプラグ3 1が配置されている。即ち、図1ではメタルコンタクトプラグ3 1は、凹形状に配置された5つの単位トランジスタに囲まれるように設けられている。メタルコンタクトプラグ3 1は、図1に示したように、第1の単位トランジスタ5 0 A₁および第5の単位トランジスタ5 0 A₅の中心を結ぶY方向の中心線と、第3の単位トランジスタ5 0 A₃の中心を通るX方向の中心線との交点に中心が位置する円形として形成される。第1の実施形態ではメタルコンタクトプラグ3 1の直径を40 nmとしている。前述のように、各々のシリコンピラーのX方向およびY方向の幅を50 nmとし、各々のシリコンピラーの間隔を30 nmとしている。従って、メタルコンタクトプラグ3 1の外周と、第1のシリコンピラー5 A₁、第3のシリコンピラー5 A₃、および第5のシリコンピラー5 A₅との各々の最近接間隔は35 nmとなり、最短間隔となる。

【0030】

一方、第2のシリコンピラー5 A₂、および第4のシリコンピラー5 A₄は、メタルコンタクトプラグ3 1に対してX方向に45度傾斜した方向に延在することとなる。従って、第2のシリコンピラー5 A₂、および第4のシリコンピラー5 A₄を構成する矩形の角部がメタルコンタクトプラグ3 1の外周に対して最近接の状態となり、この場合、最近接間隔は57 nmとなる。

【0031】

第1の実施形態では、メタルコンタクトプラグ3 1の中心に対して、X方向もしくはY方向に延在する同一中心線上に中心が位置するように設けられた第1のシリコンピラー5 A₁、第3のシリコンピラー5 A₃、第5のシリコンピラー5 A₅と、メタルコンタクトプラグ3 1の外周との間隔はいずれも35 nmで最短間隔を構成する。一方、メタルコンタクトプラグ3 1に対して、X方向の中心線から45度傾斜した方向に延在する第2のシリコンピラー5 A₂、第4のシリコンピラー5 A₄とメタルコンタクトプラグ3 1の外周との間隔はいずれも57 nmで最長間隔を構成する。この場合、最長間隔（57 nm）は、最短間隔（35 nm）の2倍以下となっているので、複数のシリコンピラーを配置するためにメタルコンタクトプラグ3 1と各々のシリコンピラーとの間隔が不均一となり、メタルコンタクトプラグ3 1からシリコンピラーに至る下部拡散層の寄生抵抗が各々のシリコンピラーごとに変化してしまい、半導体装置全体として特性が不安定になる問題を回避することができる。各々のシリコンピラーを直径50 nmの円形で形成した場合、最長間隔は67 nmとなるが、この場合でも最短間隔（35 nm）の2倍以下となっているので、上記の問題を回避することができる。

【0032】

メタルコンタクトプラグ3 1の直上には、メタル配線3 4が配置されている。メタル配線3 4は、メタルコンタクトプラグ3 1を介して、各々の単位トランジスタを構成するピラー下部拡散層9と接続されており、ピラー下部拡散層への給電配線となっている。

【0033】

次に、図2および図3を参照して、個々の単位トランジスタ5 0の構造の詳細について、さらに説明する。図2および図3に示すように、シリコン基板1上には、STI（Shallow Trench Isolation；素子分離溝）2が設けられている。STI 2に囲まれた活性領域

である領域Aには、半導体の基柱（半導体ピラー）である、第1のシリコンピラー5A₁～第5のシリコンピラー5A₅の5つのシリコンピラー5が立設されている。第1のシリコンピラー5A₁および第2のシリコンピラー5A₂はX方向に延在している。第5のシリコンピラー5A₅および第4のシリコンピラー5A₄もX方向に延在している。また、第2のシリコンピラー5A₂、第3のシリコンピラー5A₃、第4のシリコンピラー5A₄はY方向に延在している。そのため、5つのシリコンピラーは、前述のように凹形状に配置されている。

【0034】

各々のシリコンピラーは、対応する各々の単位トランジスタ50のチャネル部を構成する柱状の半導体である。従って、各々の単位トランジスタは縦型トランジスタである。5つのシリコンピラーは、STI2に区画された領域Aに全てが同一の高さとなるように配置されている。

【0035】

なお、各々のシリコンピラーの太さ（シリコン基板1の基板表面に平行な面で切った断面の大きさ）は、完全空乏化が可能な太さにしている。

【0036】

各々の単位トランジスタは、シリコンピラー5の上端部と下端部に、それぞれ不純物拡散層を有している。シリコンピラーの上端部に位置したピラー上部拡散層16はソース／ドレインの一方であり、シリコンピラーの下端部に位置したピラー下部拡散層9はソース／ドレインの他方である。ピラー上部拡散層16とピラー下部拡散層9との間に挟まれたシリコンピラーの中央部は、チャネル部を構成している。

【0037】

5つのシリコンピラーのシリコンピラー群の中心となっている第3のシリコンピラー5A₃に対してX方向に隣接するように、ゲート吊りシリコンピラー6が配置されている。シリコンピラー5とゲート吊りシリコンピラー6は、シリコン基板1の表面をエッチングして設けられている。ゲート吊りシリコンピラー6は、シリコン基板1の表面から突出した柱状の半導体である。ゲート吊りシリコンピラー6は、ゲート電極11の高さを嵩上げてゲート電極11と上部のゲート吊り配線42との距離を小さくするための突起層として機能する。隣接するシリコンピラー5の間隔並びにゲート吊りシリコンピラー6とシリコンピラー5との間隔（シリコンピラー5とゲート吊りシリコンピラー6との隙間の大きさ）は、ゲート電極11の厚みの2倍以下としている。ここでは30nmとしている。なお、ゲート電極の平面視における厚さは20nmとしている。

【0038】

シリコンピラー5とゲート吊りシリコンピラー6の周囲におけるシリコン基板1の上面には、絶縁膜8が設けられている。絶縁膜8は、シリコンピラー5とゲート吊りシリコンピラー6の周囲を覆って、STI2に達している。ピラー下部拡散層9は、絶縁膜8の下方で絶縁膜8と重なるように配置されており、絶縁膜8によってピラー下部拡散層9とゲート電極11とが電氣的に絶縁されている。ピラー下部拡散層9は、5つのシリコンピラー同士を電氣的に接続しており、5つの単位トランジスタである第1の単位トランジスタ50A₁～第5の単位トランジスタ50A₅に共通の拡散層を構成する。なお、STI2は、ピラー下部拡散層9よりも深く設けられており、STI2を挟んで隣接する活性領域同士でピラー下部拡散層9が導通しないようになっている。

【0039】

シリコンピラー5とゲート吊りシリコンピラー6の側面には、ゲート絶縁膜10が配置されている。また、ゲート絶縁膜10を介してシリコンピラー5とゲート吊りシリコンピラー6の側面に厚さ20nmのゲート電極11が配置されている（図2のX方向の厚さ）。ゲート電極11は、ここでは図示していないが、STI2の内壁面と、STI2の上面に積層された絶縁膜3とマスク膜4の内壁面の一部にも設けられている。ゲート絶縁膜10は、シリコンピラー5の外周面を覆って絶縁膜8と接続されている。シリコンピラー5のチャネル部とピラー上部拡散層16と絶縁膜8の下方に配置されたピラー下部拡散層9

は、ゲート絶縁膜10と絶縁膜8によって、ゲート電極11と電氣的に絶縁されている。

【0040】

ゲート電極11は、隣接するシリコンピラー5の隙間及びシリコンピラー5とゲート吊りシリコンピラー6の隙間を覆って、シリコンピラー5とゲート吊りシリコンピラー6の側面全体に設けられている。

【0041】

シリコンピラー同士の間隔（隙間の大きさ）は、ゲート電極11の厚みの2倍以下とされている。第1のシリコンピラー5A₁～第5のシリコンピラー5A₅の側面に設けられた厚さ20nmのゲート電極11は、各々のシリコンピラー間隔がゲート電極11の膜厚の2倍以下とされた30nmの部分で互いに接触し、1つのゲート電極として機能する。第1のシリコンピラー5A₁～第5のシリコンピラー5A₅の隙間には、ゲート電極11がシリコンピラー5の高さ方向全体に隙間なく設けられており、第1の単位トランジスタ50A₁～第5の単位トランジスタA₅に共通のゲート電極として配置される。

【0042】

第3のシリコンピラー5A₃とゲート吊りシリコンピラー6との間隔（隙間の大きさ）は、ゲート電極11の厚みの2倍以下とされている。第3のシリコンピラー5A₃の側面とゲート吊りシリコンピラー6の側面に設けられた厚さ20nmのゲート電極11は、各々のピラー間隔がゲート電極11の膜厚の2倍以下とされた30nmの部分で互いに接触し、1つのゲート電極として機能する。第3のシリコンピラー5A₃とゲート吊りシリコンピラー6との隙間には、ゲート電極11がシリコンピラー5の高さ方向全体に隙間なく設けられており、第3のシリコンピラー5A₃とゲート吊りシリコンピラー6に共通のゲート電極となっている。従って、ゲート吊りシリコンピラー6のゲート電極11から供給されたゲート電圧は、第3のシリコンピラー5A₃のゲート電極11を介して、第1のシリコンピラー5A₁と第2のシリコンピラー5A₂と第4のシリコンピラー5A₄と第5のシリコンピラー5A₅のゲート電極11に供給される。

【0043】

STI2とゲート吊りシリコンピラー6の上面には、絶縁膜3が配置されている。STI2とゲート吊りシリコンピラー6の上面には、絶縁膜3を覆ってマスク膜4が設けられており、さらにゲート電極11と絶縁膜8を覆って第1層間絶縁膜12が設けられている。第1層間絶縁膜12は、STI2と絶縁膜3とマスク膜4の壁面に囲まれた領域に設けられている。マスク膜4と第1層間絶縁膜12の上面には、第2層間絶縁膜20が設けられている。第2層間絶縁膜20を覆ってストッパー膜21が設けられ、さらにストッパー膜21を覆って第3層間絶縁膜24が設けられている。

【0044】

第3層間絶縁膜24の上面には、ゲート吊り配線42が配置されている。ゲート吊り配線42は、第3層間絶縁膜24、ストッパー膜21、第2層間絶縁膜20及び第1層間絶縁膜12を貫通するメタルコンタクトプラグ41（導電プラグ）によってゲート電極11と接続されている。

【0045】

メタルコンタクトプラグ41は、ゲート吊りシリコンピラー6と部分的に重なる位置に設けられている。ゲート吊りシリコンピラー6の上（より詳細には、ゲート吊りシリコンピラー6の上面に位置した絶縁膜3の上）には、マスク膜4が配置されており、メタルコンタクトプラグ41は、マスク膜4の側面に位置したゲート電極11の上端部と接続されている。ゲート吊りシリコンピラー6の上に配置されたマスク膜4は、ゲート吊りシリコンピラー6と共に、ゲート電極11の高さを嵩上げして、ゲート電極11とゲート吊り配線42との距離を小さくするための突起層として機能する。

【0046】

ゲート吊り配線42は、メタルコンタクトプラグ41と少なくとも部分的に重なる位置に配置されている。

【0047】

第3層間絶縁膜24の上面には、メタル配線33、34が配置されている。

【0048】

メタル配線33は、第1層間絶縁膜12とゲート電極11で取り囲まれたシリコンプラグ（導電プラグ）19と、第3層間絶縁膜24、ストッパー膜21及び第2層間絶縁膜20を貫通するメタルコンタクトプラグ（導電プラグ）30とを介して、各々のシリコンピラーのピラー上部拡散層16と接続されている。シリコンプラグ19は、シリコン中にヒ素等の不純物を注入（拡散）したものであり、ピラー上部拡散層16と共に単位トランジスタ50のソース／ドレインの一方を構成している。シリコンプラグ19の側面には、サイドウォール膜18と絶縁膜17が配置されており、サイドウォール膜18と絶縁膜17によって、シリコンプラグ19とゲート電極11とが電氣的に絶縁されている。

【0049】

メタル配線34は、第3層間絶縁膜24、ストッパー膜21、第2層間絶縁膜20、第1層間絶縁膜12及び絶縁膜8を貫通するメタルコンタクトプラグ（導電プラグ）31によって、ピラー下部拡散層9と接続されている。

【0050】

このように、第1の実施形態に係る半導体装置は、1つの活性領域内でピラー下部拡散層9を共有して立設され、第一の方向（X方向）の同一線上に中心が位置するように一定の間隔で配置された第1および第2の単位トランジスタ（50A₁、50A₂）と、第一の方向に垂直な第二の方向（Y方向）の同一線上に中心が位置するように一定の間隔で配置された第2、第3、第4の単位トランジスタ（50A₂、50A₃、50A₄）と、第一の方向の同一線上に中心が位置するように一定の間隔で配置された第4、第5の単位トランジスタ（50A₄、50A₅）と、ピラー下部拡散層に導通するメタルコンタクトプラグ31を有し、メタルコンタクトプラグ31は、第1の単位トランジスタ50A₁および第5の単位トランジスタ50A₅の中心を結ぶ第二の方向の中心線と、第3の単位トランジスタ50A₃の中心を通る第一の方向の中心線との交点に中心が位置する円形として配置される構成となっている。

【0051】

これにより、メタルコンタクトプラグ31の外周と第2の単位トランジスタ50A₂を構成する第2のシリコンピラー5A₂との最近接間隔となる最長間隔を、メタルコンタクトプラグ31の外周と第3の単位トランジスタ50A₃を構成する第3のシリコンピラー5A₃との最近接間隔となる最短間隔の2倍以下の距離とすることができる（均等配置することができる）。

【0052】

従って、従来技術のように、複数のシリコンピラーを配置するためにメタルコンタクトプラグ31と各々のシリコンピラーとの間隔が不均一となり、メタルコンタクトプラグ31からシリコンピラーに至る下部拡散層9の寄生抵抗が各々のシリコンピラーごとに变化してしまい、半導体装置100全体として特性が不安定になる問題を回避することができる。

【0053】

次に、第2の実施形態に係る半導体装置100aについて、図4を参照して説明する。

【0054】

第2の実施形態は、第1の実施形態において、凹形状の両側辺部分の先端に、さらに単位トランジスタを追加配置したものである。

【0055】

なお、第2の実施形態において、第1の実施形態と同様の機能を果たす要素については同一の番号を付し、主に第1の実施形態と異なる部分について説明する。

【0056】

図4に示すように、第2の実施形態に係る半導体装置100aは、第1の実施形態における凹形状の両側辺部分の先端にそれぞれ新たな単位トランジスタである第6の単位トランジスタ50A₆および第7の単位トランジスタ50A₇が配置された構成となっている。

。すなわち、第7の単位トランジスタ50A₇、第1の単位トランジスタ50A₁、第2の単位トランジスタ50A₂の3つの単位トランジスタがX方向の同一線上に中心が位置するように一定の間隔で配置される。また、第2の単位トランジスタ50A₂、第3の単位トランジスタ50A₃、第4の単位トランジスタ50A₄の3つの単位トランジスタがY方向の同一線上に中心が位置するように一定の間隔で配置される。さらに、第4の単位トランジスタ50A₄、第5の単位トランジスタ50A₅、第6の単位トランジスタ50A₆の3つの単位トランジスタがX方向の同一線上に中心が位置するように一定の間隔で配置される。第7、第1および第2の単位トランジスタ（50A₇、50A₁、50A₂）と、第6、第5、第4の単位トランジスタ（50A₆、50A₅、50A₄）とは、第3の単位トランジスタ50A₃の中心を通してX方向に延在する線分に対して線対称の位置に配置されている。これにより、7つの単位トランジスタの配置は凹形状となっている。各々の単位トランジスタは縦型トランジスタで構成されている。また、7つの単位トランジスタは実施形態1と同様に、ピラー下部拡散層を共有すると共にメタル配線33で並列に接続することにより1つの並列トランジスタを構成している。

【0057】

凹形状に配置された7つのシリコンピラー5の内側で、第1のシリコンピラー5A₁と第5のシリコンピラー5A₅で挟まれた領域の中央部には、平面視で円形のメタルコンタクトプラグ31が、7つのシリコンピラーに囲まれるように配置されている。具体的には、メタルコンタクトプラグ31は、図4に示したように、第1の単位トランジスタ50A₁および第5の単位トランジスタ50A₅の中心を結ぶY方向の中心線と、第3の単位トランジスタ50A₃の中心を通るX方向の中心線との交点に中心が位置する円形として配置される。

【0058】

上記の構成により、平面視におけるメタルコンタクトプラグ31と、第2のシリコンピラー5A₂、第4のシリコンピラー5A₄、第6のシリコンピラー5A₆、第7のシリコンピラー5A₇との最近接間隔で示される最長間隔は、最短間隔（第1のシリコンピラー5A₁、第3のシリコンピラー5A₃、第5のシリコンピラー5A₅との最近接間隔）の2倍以下にすることができる（均等配置することができる）。

【0059】

従って、第2の実施形態に係る半導体装置100aは、縦型トランジスタで構成される並列トランジスタの特性の不安定性を回避しつつ、第1の実施形態に比べてより大きな電流に対応することができる。

【0060】

次に、第3の実施形態に係る半導体装置100bについて、図5を参照して説明する。

【0061】

第3の実施形態は、第2の実施形態において、8つのシリコンピラー5を、平面視で複数の凹形状を組み合わせた形状となるように配置したものである。

【0062】

なお、第3の実施形態において、第2の実施形態と同様の機能を果たす要素については同一の番号を付し、主に第2の実施形態と異なる部分について説明する。

【0063】

図5に示すように、第3の実施形態に係る半導体装置100bは、STI2に囲まれた領域Aを有し、領域Aには、平面視で矩形状の8つのシリコンピラー5（5A₁～5A₅及び5A₈～5A₁₀）が設けられている。8つのシリコンピラー5は、平面視で複数の凹形状を組み合わせた形状、ここでは2つの凹形状を組み合わせた「ダブル凹形状」となるように配置されている。さらに詳細に述べると、8つのシリコンピラー5の一部（5A₂～5A₄、5A₈、5A₉）はY方向へ点在するように等間隔で配置されており、さらに第2のシリコンピラー5A₂の左側となるように、第1のシリコンピラー5A₁がX方向へ点在して第2のシリコンピラー5A₂～第4のシリコンピラー5A₄と同じ間隔となるように配置されている。また、第1のシリコンピラー5A₁と同様に、第4のシリコン

ピラー5 A₄の左側となるように、第5のシリコンピラー5 A₅が配置されており、さらに第9のシリコンピラー5 A₉の左側となるように、第10のシリコンピラー5 A₁₀が配置されている。

【0064】

ダブル凹形状に配置された8つのシリコンピラー5の内側で、第1のシリコンピラー5 A₁と第5のシリコンピラー5 A₅並びに第5のシリコンピラー5 A₅と第10のシリコンピラー5 A₁₀で挟まれた夫々の領域の中央部には、平面視で円形状の2つのメタルコンタクトプラグ31（31 A、31 B）が、それぞれ凹形状に配置されたシリコンピラーに囲まれるように配置されている。このような配置にすることで、平面視におけるメタルコンタクトプラグ31（31 A、31 B）とシリコンピラー5との最長間隔（第2のシリコンピラー5 A₂、第4のシリコンピラー5 A₄、第9のシリコンピラー5 A₉との間隔）は、最短間隔（第1のシリコンピラー5 A₁、第3のシリコンピラー5 A₃、第5のシリコンピラー5 A₅、第8のシリコンピラー5 A₈、第10のシリコンピラー5 A₁₀との間隔）の2倍以下にすることができる（均等配置することができる）。

【0065】

従って、第3の実施形態に係る半導体装置100 bによれば、縦型トランジスタで構成される並列トランジスタの特性の不安定性を回避しつつ、第2の実施形態に比べてより大きな電流に対応することができる。

【0066】

次に、第4の実施形態に係る半導体装置100 cについて、図6を参照して説明する。

【0067】

第4の実施形態は、第3の実施形態において、ダブル凹形状の、それぞれの両側辺部分の先端に、さらに単位トランジスタを追加配置したものである。

【0068】

なお、第4の実施形態において、第3の実施形態と同様の機能を果たす要素については同一の番号を付し、主に第3の実施形態と異なる部分について説明する。

【0069】

図6に示すように、第4の実施形態に係る半導体装置100 cは、STI 2に囲まれた領域Aを有し、領域Aには、平面視で矩形状の11個のシリコンピラー5（5 A₁～5 A₁₁）が設けられている。11個のシリコンピラー5は、平面視でダブル凹形状となるように配置されている。さらに詳細に述べると、11個のシリコンピラー5の一部（5 A₂～5 A₄、5 A₈、5 A₉）はY方向へ点在するように等間隔で配置されており、さらに第2のシリコンピラー5 A₂の左側となるように、第1のシリコンピラー5 A₁と第7のシリコンピラー5 A₇がX方向へ点在して第2のシリコンピラー5 A₂～第4のシリコンピラー5 A₄と同じ間隔となるように配置されている。また、第1のシリコンピラー5 A₁、第7のシリコンピラー5 A₇と同様に、第4のシリコンピラー5 A₄の左側となるように、第5のシリコンピラー5 A₅と第6のシリコンピラー5 A₆が配置されており、さらに第9のシリコンピラー5 A₉の左側となるように、第10のシリコンピラー5 A₁₀と第11のシリコンピラー5 A₁₁が配置されている。

【0070】

ダブル凹形状に配置された11個のシリコンピラー5の内側で、第1のシリコンピラー5 A₁と第5のシリコンピラー5 A₅並びに第5のシリコンピラー5 A₅と第10のシリコンピラー5 A₁₀で挟まれた夫々の領域の中央部には、平面視で円形状の2つのメタルコンタクトプラグ31（31 A、31 B）が凹形状に配置されたシリコンピラーに囲まれるように配置されている。このような配置にすることで、平面視におけるメタルコンタクトプラグ31（31 A、31 B）とシリコンピラー5との最長間隔（第2のシリコンピラー5 A₂、第4のシリコンピラー5 A₄、第6のシリコンピラー5 A₆、第7のシリコンピラー5 A₇、第9のシリコンピラー5 A₉、第11のシリコンピラー5 A₁₁との間隔）は、最短間隔（第1のシリコンピラー5 A₁、第3のシリコンピラー5 A₃、第5のシリコンピラー5 A₅、第8のシリコンピラー5 A₈、第10のシリコンピラー5 A₁₀と

の間隔)の2倍以下にすることができる(均等配置することができる)。

【0071】

従って、第4の実施形態に係る半導体装置100cは、縦型トランジスタで構成される並列トランジスタの特性の不安定性を回避しつつ、第3の実施形態に比べてより大きな電流に対応することができる。

【0072】

次に、第5の実施形態に係る半導体装置100dについて、図7を参照して説明する。

【0073】

第5の実施形態は、第1～第4の実施形態とは異なり、シリコンピラーが一行に並んでいる構造において、シリコンピラーがメタルコンタクトプラグ31の周囲に均等に配置されるように構成したものである。

【0074】

なお、第5の実施形態において、第1～第4の実施形態と同様の機能を果たす要素については同一の番号を付し、主に第1の実施形態と異なる部分について説明する。

【0075】

図7に示すように、第5の実施形態に係る半導体装置100dは、Y方向に点在した7つのシリコンピラー5と、均等間隔で3つ配置された、メタルコンタクトプラグ31を有している。

【0076】

より具体的に説明すると、1つの活性領域内でY方向に配置された7つのシリコンピラーの内、中央に位置する第4のシリコンピラー5A₄に対して中心がX方向に延在するように配置されたメタルコンタクトプラグ31Bの他、第2のシリコンピラー5A₂と第6のシリコンピラー5A₆に対して中心がX方向に延在する2つのメタルコンタクトプラグ31A、31Cが配置されており、いずれのシリコンピラー5Aであってもいずれかのメタルコンタクトプラグとの間隔を最短間隔の2倍以下となっている。この場合、3つのメタルコンタクトプラグ31とX方向に対向する各々のシリコンピラーの間隔は最短間隔で配置される。

【0077】

このように、シリコンピラーは必ずしも凹形状にメタルコンタクトプラグを囲んでいる必要はなく、シリコンピラーとメタルコンタクトプラグ31の最短間隔と最長間隔の差が2倍以内となるように均等配置されていればよい。

【0078】

次に、第1の実施形態に係る半導体装置100の製造方法について、図8～図20を参照して詳細に説明する。

【0079】

なお、第2～第5の実施形態に係る半導体装置100a～100dの製造方法は、第1の実施形態に係る半導体装置100の製造方法と同様であるため、説明を省略する。

【0080】

まず図8および図9に示すように、フォトリソグラフィ法およびドライエッチング法を用いて、シリコン基板1に溝(図示せず)を形成する。次に、溝の内壁を含むシリコン基板1の全面に薄いシリコン酸化膜(図示せず)を熱酸化法によって形成した後、溝の内部を埋め込むように、シリコン基板1の全面へシリコン窒化膜をCVD(Chemical Vapor Deposition)法によって堆積させる。その後、シリコン基板1上の不要なシリコン窒化膜をCMP(Chemical Mechanical Polishing)法により除去して、シリコン窒化膜を溝の内部だけに残すことにより、素子分離となるSTI2を形成する。

【0081】

次に図10～図12に示すように、CVD法によって、シリコン基板1上にシリコン酸化膜である絶縁膜3を10nm厚となるように形成してから、シリコン窒化膜であるマスク膜4を120nm厚となるように形成する。次に、フォトリソグラフィ法およびドライエッチング法を用いて、絶縁膜3とマスク膜4をパターンニングする。ここでは、各シリコ

ンピラー（ $5A_1 \sim 5A_5$ ）に対応するマスク膜4をX方向およびY方向の幅が各々50nmとなる矩形で形成した。矩形に限らず、直径50nmの円形であっても良い。また、このときパターンニングした開口部には、シリコン基板1とSTI2が露出している。

【0082】

次に、マスク膜4をマスクとして、露出させたシリコン基板1とSTI2を深さが150nmとなるようにドライエッチングして、単位トランジスタのチャンネルとなる5つのシリコンピラー5（ $5A_1 \sim 5A_5$ ）とゲート電極を上層配線に接続するための1つのゲート吊りシリコンピラー6を、シリコン基板1から立ち上がるような形状に形成する。これにより、各シリコンピラー（ $5A_1 \sim 5A_5$ ）は、X方向およびY方向の幅を50nmとする矩形で形成される。

【0083】

このときのシリコンピラー5とゲート吊りシリコンピラー6のレイアウトは、図10に示した通りである。すなわち、STI2で囲まれた領域Aに、単位トランジスタを形成するためのシリコンピラー5を配置形状が凹形状となるように5つ配置し、それぞれのシリコンピラー5の間隔をこの後形成するゲート電極の膜厚の2倍以下とする。具体的には、図10において、X方向の同一線上に中心が位置するように設けられた第1のシリコンピラー $5A_1$ と第2のシリコンピラー $5A_2$ の間隔は30nmとなっている。同じくX方向の同一線上に中心が位置する第5のシリコンピラー $5A_5$ と第4のシリコンピラー $5A_4$ の間隔も30nmとなっている。また、Y方向の同一線上に中心が位置するように設けられた第2のシリコンピラー $5A_2$ 、第3のシリコンピラー $5A_3$ 、第4のシリコンピラー $5A_4$ の各々の間隔も30nmとなっている。

【0084】

なお、凹形状の内部の中心は、後にメタルコンタクトプラグ31が配置される位置31であり、換言すれば、各シリコンピラーは位置31'の周囲に均等配置されるように形成される（図10では、各シリコンピラーは位置31'を囲むように凹形状に配置されている）。

【0085】

同様に、ゲート電極の膜厚の2倍以下の間隔で、第3のシリコンピラー $5A_3$ とX方向に隣接するように、ゲート吊りシリコンピラー6を1つ配置する。ここでは、第3のシリコンピラー $5A_3$ とゲート吊りシリコンピラー6の間隔も30nmとしている。チャンネル部を形成するシリコンピラー5の太さ（シリコン基板1に平行な面で切った断面の大きさ）は、完全空乏化が可能な太さである。ゲート電極を吊り上げるゲート吊りシリコンピラー6のサイズは任意であり、チャンネル部を形成するシリコンピラー5と同じサイズである必要はない。

【0086】

次に図13～図15に示すように、シリコンピラー5とゲート吊りシリコンピラー6の側面を熱酸化法で5nm厚となるように酸化し（図示せず）、CVD法によるシリコン窒化膜を20nm厚となるように成膜後、全面エッチバックを行って、シリコンピラー5とゲート吊りシリコンピラー6とマスク膜4の側面にサイドウォール膜を形成する。このとき、STI2の側面にもサイドウォール膜が形成される。次に、熱酸化法によってシリコン基板1の酸化を行い、シリコンの露出部分に30nm厚の絶縁膜8を形成する。このとき、シリコンピラー5とゲート吊りシリコンピラー6の側面はサイドウォール膜で覆われており、夫々の上面はマスク膜4で覆われているため、酸化はされない。

【0087】

次に、イオン注入によって、絶縁膜8の下方にピラー下部拡散層9を形成する。ここで、ピラー下部拡散層9は、5つのシリコンピラー5（ $5A_1 \sim 5A_5$ ）で共有される。なお注入する不純物は、例えばN型トランジスタの場合はヒ素を用いることができる。このとき、シリコンピラー5とゲート吊りシリコンピラー6の上面には、マスク膜4が100nm厚で形成されており、マスク膜4はピラー下部拡散層9上の絶縁膜8よりも十分に厚く、シリコンピラー5とゲート吊りシリコンピラー6の上部には不純物が注入されないの

で、拡散層は形成されない。次に、ドライエッチング法あるいはウェットエッチング法によって、シリコンピラー5とゲート吊りシリコンピラー6の側面に形成したサイドウォール膜と熱酸化膜を除去する。

【0088】

次に、熱酸化法によって、シリコンピラー5とゲート吊りシリコンピラー6の側面に3nm厚のシリコン酸化膜であるゲート絶縁膜10を形成する。次に、シリコン基板1の全面にゲート電極となる20nm厚のポリシリコン膜（多結晶シリコン膜）をCVD法により成膜してから、全面エッチバックを行い、シリコンピラー5及びゲート吊りシリコンピラー6の側面のみにゲート電極11を形成する。シリコンピラー5及びゲート吊りシリコンピラー6の側面にゲート電極11を形成した場合、STI2の側面にもゲート電極11（図示せず）が形成される。図14と図15に示すように、シリコンピラー5同士の間隔並びにシリコンピラー5とゲート吊りシリコンピラー6の間隔は、前述のように、ゲート電極11の膜厚の2倍以下（30nm）としているので、各々のシリコンピラー5の間および第3のシリコンピラー5A₃とゲート吊りシリコンピラー6の間はゲート電極11で完全に埋められる。従って、第1のシリコンピラー5A₁～第5のシリコンピラー5A₅の側面におけるゲート電極11は、一体化して接続されており、さらにゲート吊りシリコンピラー6の側面におけるゲート電極11が、第3のシリコンピラー5A₃の側面におけるゲート電極11へ接続されている。

【0089】

次に図16に示すように、シリコンピラー5とゲート吊りシリコンピラー6を埋め込むように、CVD法によって、シリコン酸化膜である第1層間絶縁膜12を形成する。次に、CMP法によって、第1層間絶縁膜12をマスク膜4が露出するように平坦化し、続けてCVD法によって、シリコン酸化膜であるマスク膜13を50nm厚となるように成膜する。

【0090】

次に、フォトリソグラフィ法とエッチング法を用いて、マスク膜13の一部を除去する。除去するマスク膜13のパターン40は、図1に示したように、シリコンピラー5を配置した部分のみである。マスク膜13を除去した開口部14には、シリコンピラー5の上方におけるマスク膜4が露出する。次に、露出したマスク膜4をウェットエッチングによって選択的に除去し、さらに絶縁膜3を除去することで、シリコンピラー5の上方に開口部15を形成する。開口部15の底面には、シリコンピラー5の上面が露出しており、側面にはゲート電極11の一部が露出している。

【0091】

次に図17に示すように、熱酸化法によって、開口部15の内壁へシリコン酸化膜である絶縁膜17を形成する。次に、開口部15からシリコンピラー5の上部に不純物（N型トランジスタとするのであれば、磷やヒ素など）をイオン注入し、ピラー上部拡散層16を形成する。また、CVD法によるシリコン窒化膜を10nm厚程度成膜してから、エッチバックを行うことにより、開口部15の内壁へサイドウォール膜18を形成する。このサイドウォール膜18の形成時に、シリコンピラー5の上面に形成されていた絶縁膜17も除去して、シリコンピラー5の上面を露出させる。このとき絶縁膜17は、サイドウォール膜18の下方と開口部15におけるゲート電極11の露出面に残留する。サイドウォール膜18は、この後形成するシリコンプラグとゲート電極11との間の絶縁を確保する役割を果たす。

【0092】

次に、選択エピタキシャル成長法を用いて、開口部15を塞ぐようにシリコンピラー5の上面へシリコンプラグ19を成長させる。その後、N型トランジスタとする場合には、ヒ素などをイオン注入して、シリコンプラグ19内をn型の導電体として、シリコンピラー5の上部に形成したピラー上部拡散層16と電気的に接触させる。

【0093】

次に図18～図20に示すように、CVD法によって、開口部14を埋め込むようにシ

リコン酸化膜である第2層間絶縁膜20を形成する。次に、CVD法によって、シリコン窒化膜であるストッパー膜21を20nm厚となるように成膜する。次に、CVD法によって、シリコン酸化膜である第3層間絶縁膜24を150nm厚となるように成膜する。

【0094】

次に、フォトリソグラフィ法およびドライエッチング法を用いて、コンタクト孔27～29を形成する。ここで、コンタクト孔29は、図18に示したように、第1のシリコンピラー5A₁および第5のシリコンピラー5A₅の中心を結ぶY方向の中心線と、第3のシリコンピラー5A₃の中心を通るX方向の中心線との交点に中心が位置する円形として形成される。ここではコンタクト孔29の直径を40nmとしている。これにより、コンタクト孔29の外周と、第1のシリコンピラー5A₁、第3のシリコンピラー5A₃、および第5のシリコンピラー5A₅との各々の最近接間隔は35nmとなり、最短間隔となる。コンタクト孔27の形成では、ドライエッチングをストッパー膜21で一旦止めることで、ゲート電極11までの深さを制御しているが、ゲート吊りシリコンピラー6の上面は、残留しているマスク膜4が保護するので、エッチングされない。コンタクト孔27は、ゲート吊りシリコンピラー6の中心からずらした位置に形成しているので、その底部には、ゲート吊りシリコンピラー6の上方に形成したマスク膜4と、ゲート吊りシリコンピラー6の側面に形成したゲート電極11の一部が露出している。またコンタクト孔28の底部には、シリコンプラグ19の少なくとも一部が露出しており、コンタクト孔29の底部には、ピラー下部拡散層9の一部が露出している。これらのコンタクト孔27～29は同時に形成しても良いが、別々に形成しても良い。

【0095】

次に、CVD法によって、第3層間絶縁膜24を覆うようにタングステン(W)と窒化チタン(TiN)とチタン(Ti)で構成された金属膜を成膜して、コンタクト孔27～29の内部を埋め込む。次にCMP法によって、第3層間絶縁膜24上の金属膜を除去して、シリコンプラグ19に対するメタルコンタクトプラグ30、ピラー下部拡散層9に対するメタルコンタクトプラグ31、ゲート電極11に対するメタルコンタクトプラグ41を形成する。

【0096】

前述のように、直径40nmのコンタクト孔29内に形成されたメタルコンタクトプラグ31の直径は40nmとなる。従って、図18に示すように、メタルコンタクトプラグ31の外周と、第1のシリコンピラー5A₁、第3のシリコンピラー5A₃、および第5のシリコンピラー5A₅との各々の最近接間隔は35nmとなり、最短間隔となる。一方、第2のシリコンピラー5A₂、および第4のシリコンピラー5A₄は、メタルコンタクトプラグ31に対してX方向に45度傾斜した方向に延在することとなる。従って、第2のシリコンピラー5A₂、および第4のシリコンピラー5A₄を構成する矩形の角部がメタルコンタクトプラグ31の外周に対して最近接の状態となり、この場合、57nmとなる。ここでは、メタルコンタクトプラグ31に対して、X方向もしくはY方向に延在する同一中心線上に中心が位置するように設けられた第1のシリコンピラー5A₁、第3のシリコンピラー5A₃、第5のシリコンピラー5A₅との間隔はいずれも35nmで最短間隔を構成する。一方、メタルコンタクトプラグ31に対して、X方向の中心線から45度傾斜した方向に延在する第2のシリコンピラー5A₂、第4のシリコンピラー5A₄との間隔はいずれも57nmで最長間隔を構成する。この場合、最長間隔(57nm)は、最短間隔(35nm)の2倍以下となっているので、図7に示した従来技術のように、複数のシリコンピラーを配置するためにメタルコンタクトプラグ31と各々のシリコンピラーとの間隔が不均一となり、下部拡散層の寄生抵抗が各々のシリコンピラーごとに变化して、半導体装置全体として特性が不安定になる問題を回避することができる。各々のシリコンピラーを円形で形成した場合、最長間隔は67nmとなるが、この場合でも最短間隔(35nm)の2倍以下となっているので、上記の問題を回避することができる。

【0097】

次に図1に示したように、スパッタ法によるタングステン(W)と窒化タングステン(

WN) で構成されたメタル配線 3 3、3 4 とゲート吊り配線 4 2 を形成する。このとき、メタルコンタクトプラグ 4 1 は、ゲート吊り配線 4 2 と接続される。また、ピラー下部拡散層 9 に接続している 1 つのメタルコンタクトプラグ 3 1 A は、メタル配線 3 4 と接続している。さらに、5 つのシリコンピラー 5 A に形成されたピラー上部拡散層 1 6 に接続している 5 つのメタルコンタクトプラグ 3 0 は、メタル配線 3 3 に接続している。

【0098】

以上が製造方法の説明である。

【0099】

以上説明した第 1 の実施形態～第 5 の実施形態の半導体装置によれば、平面視において複数のシリコンピラー 5 をメタルコンタクトプラグ 3 1 の周辺に均等配置している。この構成によれば、メタルコンタクトプラグ 3 1 と個々のシリコンピラー 5 の最長間隔は、最短間隔の 2 倍以内となり、メタルコンタクトプラグ 3 1 とシリコンピラー 5 の間の電気抵抗ばらつきを許容値以内にすることができる。さらに、縦型トランジスタの特性劣化を防いで、半導体装置の動作を安定させることができる。

【産業上の利用可能性】

【0100】

以上、本発明を実施形態に基づいて説明したが、本発明は実施形態に限定されるものではない。当業者であれば本発明の範囲内において各種変形例および変更例に想到するのは当然のことであり、これらも本発明の範囲に属するものと了解される。

【符号の説明】

【0101】

- 1 シリコン基板
- 2 S T I
- 3 絶縁膜
- 4 マスク膜
- 5 シリコンピラー
- 5 A₁ 第 1 のシリコンピラー
- 5 A₂ 第 2 のシリコンピラー
- 5 A₃ 第 3 のシリコンピラー
- 5 A₄ 第 4 のシリコンピラー
- 5 A₅ 第 5 のシリコンピラー
- 5 A₆ 第 6 のシリコンピラー
- 5 A₇ 第 7 のシリコンピラー
- 5 A₈ 第 8 のシリコンピラー
- 5 A₉ 第 9 のシリコンピラー
- 5 A₁₀ 第 10 のシリコンピラー
- 5 A₁₁ 第 11 のシリコンピラー
- 6 シリコンピラー
- 8 絶縁膜
- 9 ピラー下部拡散層
- 10 ゲート絶縁膜
- 11 ゲート電極
- 12 第 1 層間絶縁膜
- 13 マスク膜
- 14 開口部
- 15 開口部
- 16 ピラー上部拡散層
- 17 絶縁膜
- 18 サイドウォール膜
- 19 シリコンプラグ

2 0	第 2 層間絶縁膜
2 1	ストッパー膜
2 4	第 3 層間絶縁膜
2 7	コンタクト孔
2 8	コンタクト孔
2 9	コンタクト孔
3 0	メタルコンタクトプラグ
3 1	メタルコンタクトプラグ
3 1 A	メタルコンタクトプラグ
3 1'	位置
3 3	メタル配線
3 4	メタル配線
4 0	パターン
4 1	メタルコンタクトプラグ
4 2	配線
5 0	単位トランジスタ
5 0 A	単位トランジスタ
5 0 A ₁	第 1 の単位トランジスタ
5 0 A ₂	第 2 の単位トランジスタ
5 0 A ₃	第 3 の単位トランジスタ
5 0 A ₄	第 4 の単位トランジスタ
5 0 A ₅	第 5 の単位トランジスタ
5 0 A ₆	第 6 の単位トランジスタ
5 0 A ₇	第 7 の単位トランジスタ
1 0 0	半導体装置
1 0 0 a	半導体装置
1 0 0 b	半導体装置
1 0 0 c	半導体装置
1 0 0 d	半導体装置
A	領域

【書類名】特許請求の範囲

【請求項 1】

半導体基板から立ち上がるように設けられ、前記半導体基板側の端部に拡散層を有する複数の縦型トランジスタと、

前記半導体基板から立ち上がるように設けられ、複数の前記縦型トランジスタの前記拡散層に接続される導電プラグと、

を有し、

複数の前記縦型トランジスタは、前記導電プラグの周囲に均等配置され、前記拡散層および前記導電プラグを共有している、半導体装置。

【請求項 2】

前記縦型トランジスタは、

半導体基板から立ち上がるように設けられ、チャネル部を有する半導体ピラーと、

複数の前記半導体ピラーの側面に設けられたゲート絶縁層およびゲート電極と、

複数の前記半導体ピラーの上端に設けられ、ソースまたはドレインの一方となる上部拡散層と、

複数の前記半導体ピラーの下端に設けられ、ソースまたはドレインの他方となる下部拡散層と、

を有し、

前記導電プラグは、前記下部拡散層に接続される下部拡散層側コンタクトプラグであり

、
複数の前記縦型トランジスタは、前記下部拡散層と前記下部拡散層側コンタクトプラグを共有するように設けられ、かつ各々の前記半導体ピラーが前記下部拡散層側コンタクトプラグの周囲に均等配置されている、請求項 1 記載の半導体装置。

【請求項 3】

前記半導体ピラーは、前記下部拡散層側コンタクトプラグの周囲を囲むように均等配置されている、請求項 2 記載の半導体装置。

【請求項 4】

複数の前記半導体ピラーは、平面視において、前記下部拡散層側コンタクトプラグとの距離が最も近いものと最も遠いものの差が 2 倍以内である、請求項 2 または 3 のいずれか一項に記載の半導体装置。

【請求項 5】

前記半導体ピラーは、前記下部拡散層側コンタクトプラグの周囲を「凹」形状に囲むように均等配置されている、請求項 2～4 のいずれか一項に記載の半導体装置。

【請求項 6】

前記下部拡散層側コンタクトプラグは複数設けられ、

前記半導体ピラーは、「凹」形状を複数組み合わせた配置形状を有し、

前記下部拡散層側コンタクトプラグは個々の前記「凹」形状に囲まれるように配置されている、請求項 5 に記載の半導体装置。

【請求項 7】

前記半導体ピラーは、平面上の配置形状が「凹」形状を 2 つ組み合わせた配置形状であり、

前記下部拡散層側コンタクトプラグは、2 つの前記「凹」形状のそれぞれに囲まれるように設けられている、請求項 6 記載の半導体装置。

【請求項 8】

前記半導体基板から立ち上がるように設けられ、複数の前記縦型トランジスタの前記ゲート電極に接続されるゲート吊りシリコンピラーを有する、請求項 2～7 のいずれか一項に記載の半導体装置。

【請求項 9】

複数の前記上部拡散層は互いに接続され、複数の前記縦型トランジスタが並列接続されている、請求項 2～8 のいずれか一項に記載の半導体装置。

【請求項 1 0】

前記半導体ピラーは、完全空乏化が可能な太さである、請求項 2～9 のいずれか一項に記載の半導体装置。

【請求項 1 1】

(a) 半導体基板から立ち上がるように、複数の縦型トランジスタを形成し、複数の前記縦型トランジスタの前記半導体基板側の端部に、拡散層を、複数の縦型トランジスタが共有するように設け、

(b) 前記半導体基板から複数の前記縦型トランジスタの前記拡散層に接続される導電プラグを立ち上がるように設ける、

を有し、

前記 (a) は、複数の前記縦型トランジスタを、前記導電プラグを設ける部分の周囲に均等配置する、半導体装置の製造方法。

【請求項 1 2】

前記 (a) は、半導体基板から立ち上がるように複数の半導体ピラーを設け、

複数の前記半導体ピラーの側面にゲート絶縁膜およびゲート電極を設け、

複数の前記半導体ピラーの上端にソースまたはドレインの一方となる上部拡散層を設け

、

複数の前記半導体ピラーの下端にソースまたはドレインの他方となる下部拡散層を設け

、

を有し、

前記 (b) は、前記導電プラグを、下部拡散層側コンタクトプラグとして前記下部拡散層に接続し、

さらに、前記 (a) は、複数の前記半導体ピラーを、前記 (b) において前記下部拡散層側コンタクトプラグが設けられる位置の周囲に均等配置する、請求項 1 1 記載の半導体装置の製造方法。

【請求項 1 3】

前記 (a) は、複数の前記半導体ピラーを、前記下部拡散層側コンタクトプラグが設けられる位置の周囲を囲むように均等配置する、請求項 1 2 記載の半導体装置の製造方法。

【請求項 1 4】

前記 (a) は、複数の前記半導体ピラーを、平面視において、前記下部拡散層側コンタクトプラグが設けられる位置との距離が最も近いものと最も遠いものの差が 2 倍以内になるように配置する、請求項 1 2 または 1 3 のいずれか一項に記載の半導体装置の製造方法。

【請求項 1 5】

前記 (a) は、複数の前記半導体ピラーを、前記下部拡散層側コンタクトプラグが設けられる位置の周囲を「凹」形状に囲むように均等配置する、請求項 1 2～1 4 のいずれか一項に記載の半導体装置の製造方法。

【請求項 1 6】

前記 (a) は、前記半導体ピラーを、「凹」形状を複数組み合わせた配置形状となるように設け、

前記 (b) は、前記下部拡散層側コンタクトプラグを複数設け、かつ、個々の前記下部拡散層側コンタクトプラグが個々の前記「凹」形状に囲まれるように配置する、請求項 1 5 記載の半導体装置の製造方法。

【請求項 1 7】

前記 (a) は、前記半導体ピラーを、平面上の配置形状が「凹」形状を 2 つ組み合わせた配置形状となるように設け、

前記 (b) は、前記下部拡散層側コンタクトプラグを、2 つの前記「凹」形状に囲まれるように設ける、請求項 1 5 記載の半導体装置の製造方法。

【請求項 1 8】

(c) 前記半導体基板から立ち上がるように複数の前記縦型トランジスタの前記ゲート

電極に接続されるゲート吊りシリコンピラーを設ける、
を有する、請求項 12～17 のいずれか一項に記載の半導体装置の製造方法。

【請求項 19】

(d) 複数の前記上部拡散層を互いに接続し、複数の前記縦型トランジスタを並列接続する、

を有する請求項 12～18 のいずれか一項に記載の半導体装置の製造方法。

【請求項 20】

前記 (a) は、前記半導体ピラーを、完全空乏化が可能な太さに形成する、請求項 12～19 のいずれか一項に記載の半導体装置の製造方法。

【書類名】 要約書

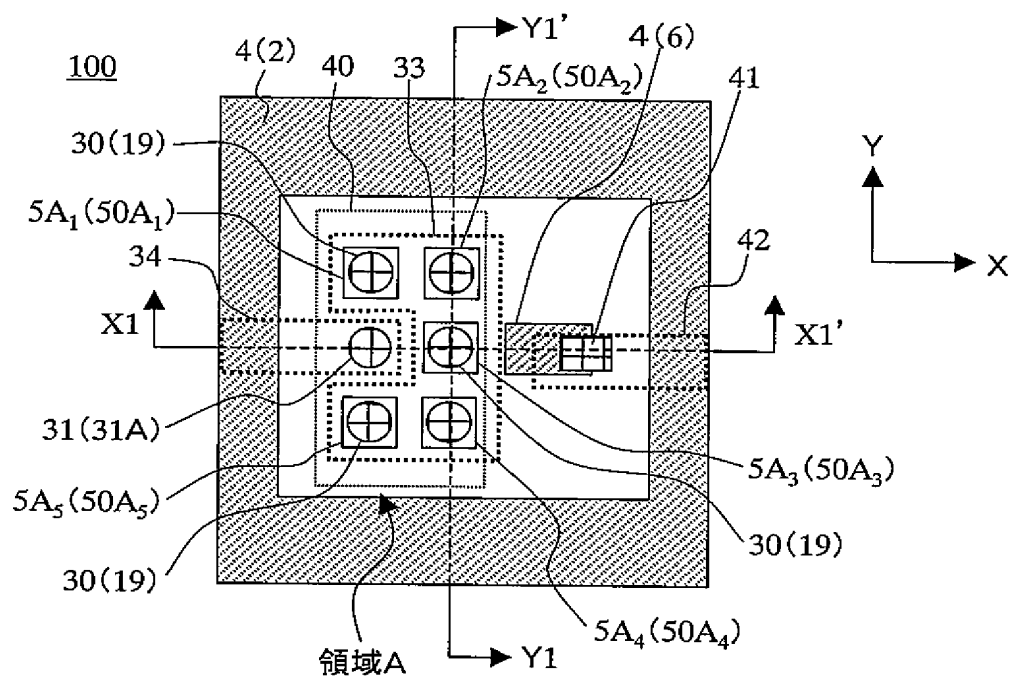
【要約】

【課題】 複数の縦型トランジスタを接続した構造でも、個々のピラーに設けられたトランジスタの特性を安定化させることが可能な半導体装置を提供する。

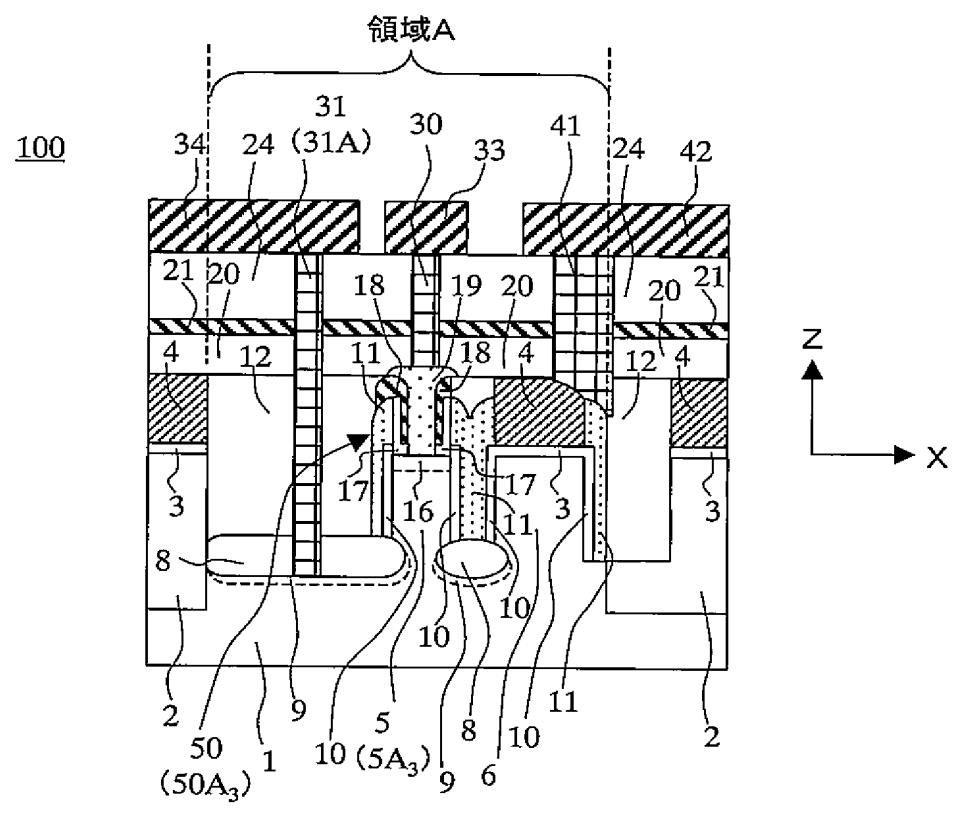
【解決手段】 本発明の半導体装置 100 は、シリコン基板 1 から立ち上がるように設けられ、シリコン基板 1 の端部にピラー下部拡散層 9 を有する複数の縦型トランジスタ 50 と、シリコン基板 1 から立ち上がるように設けられ、複数の縦型トランジスタ 50 のピラー下部拡散層 9 に接続されるメタルコンタクトプラグ 31 を有し、複数の縦型トランジスタ 50 は、メタルコンタクトプラグ 31 の周囲に均等配置され、メタルコンタクトプラグ 31 を共有している。

【選択図】 図 2

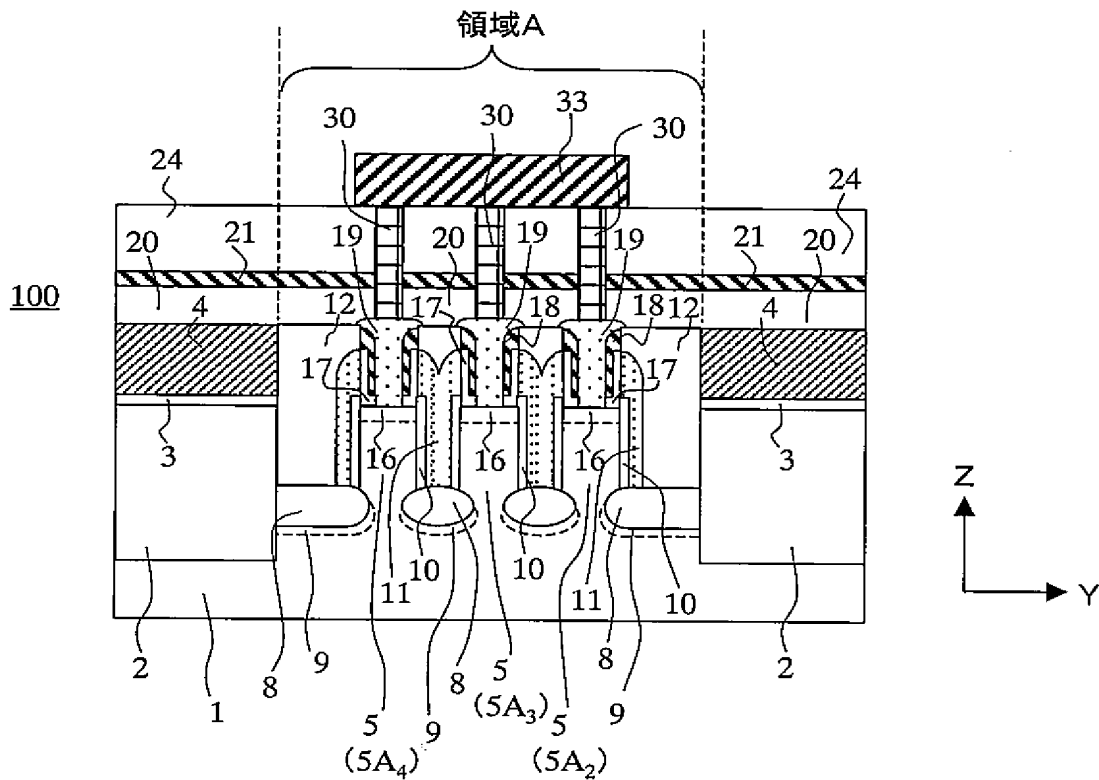
【書類名】 図面
【図 1】



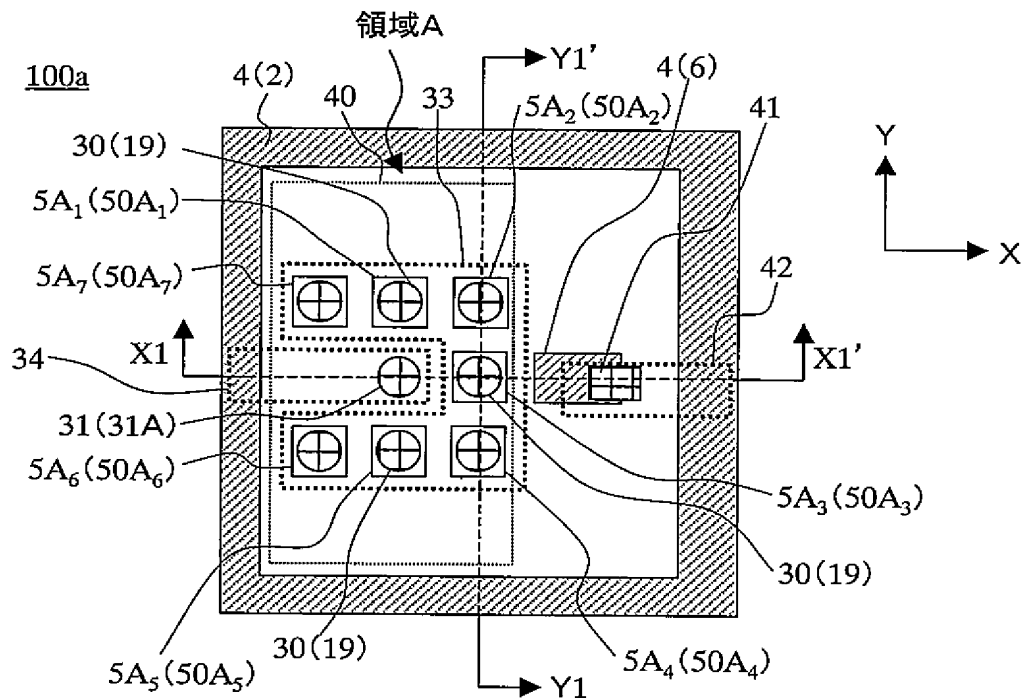
【図 2】



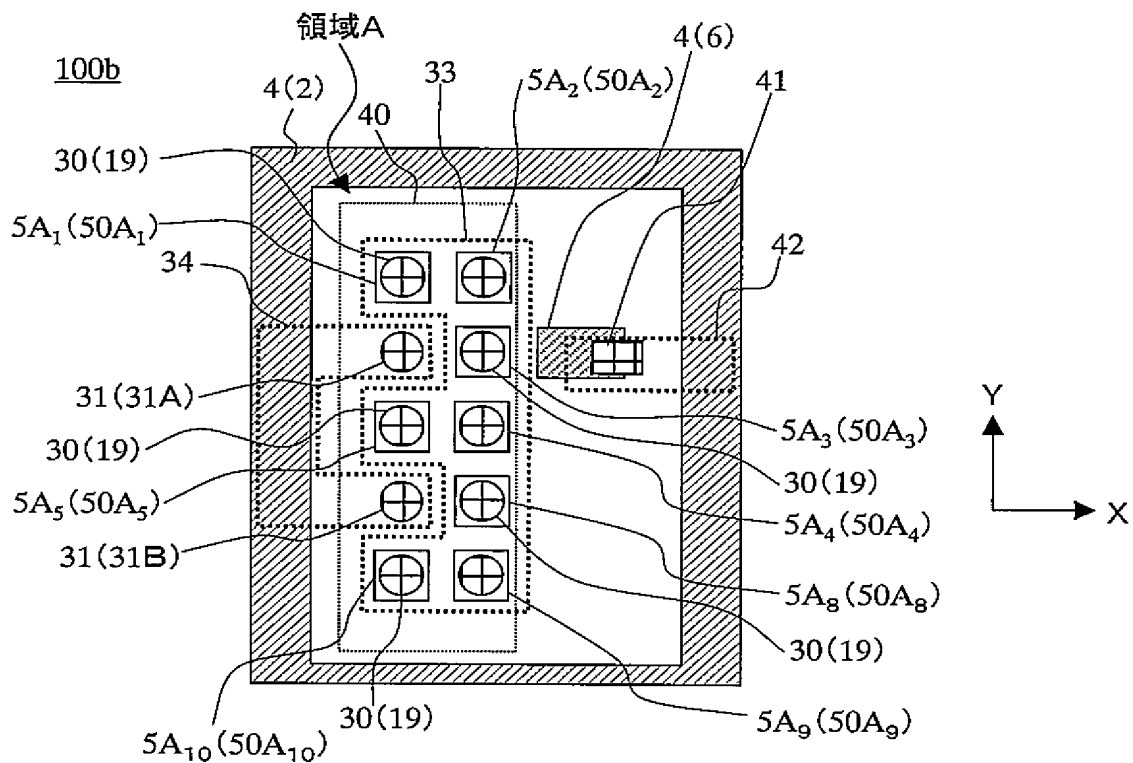
【図 3】



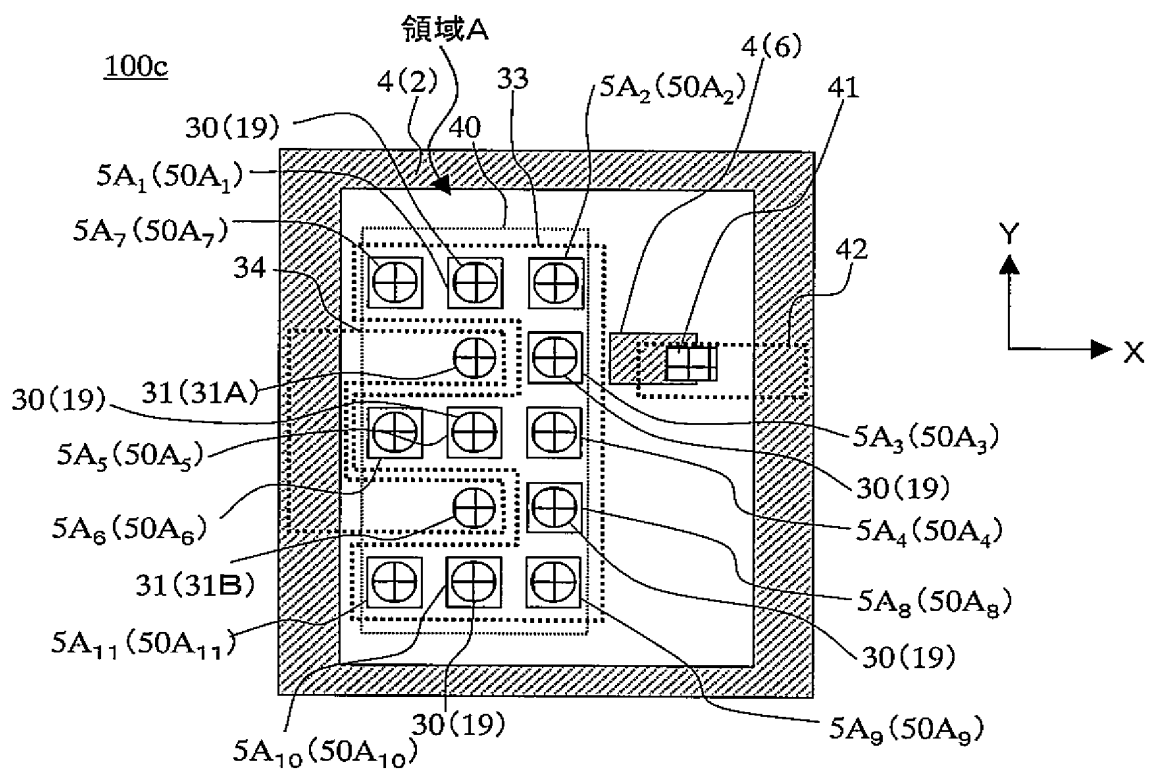
【図 4】



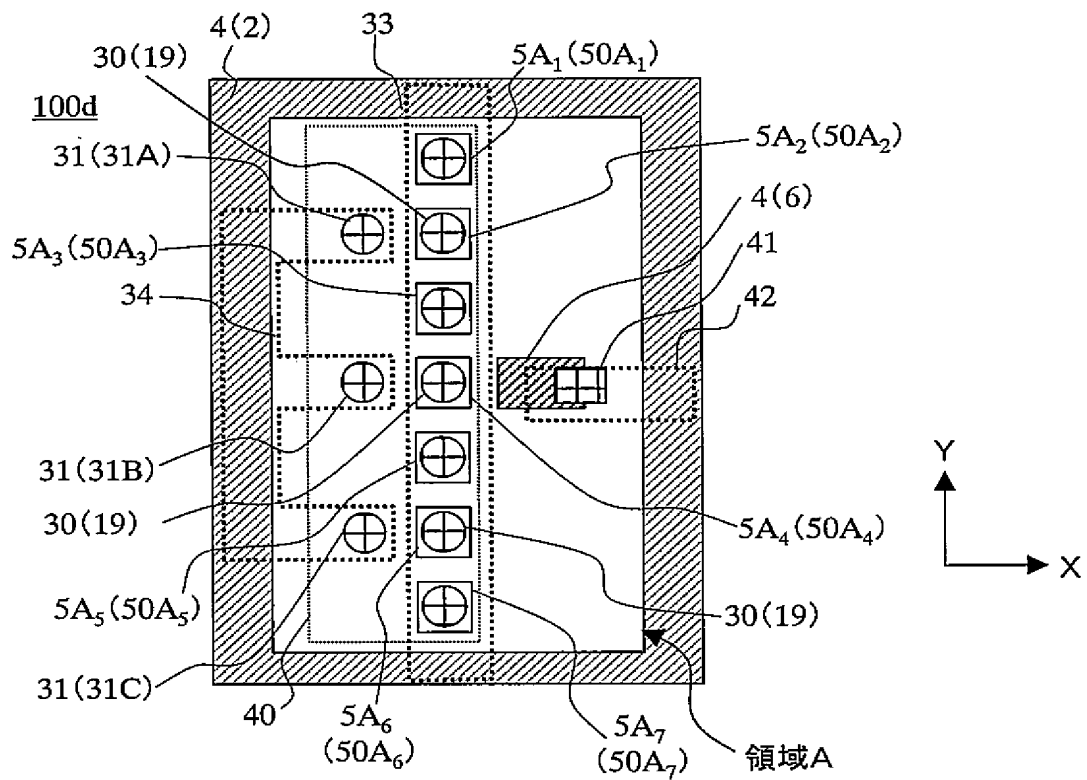
【図 5】



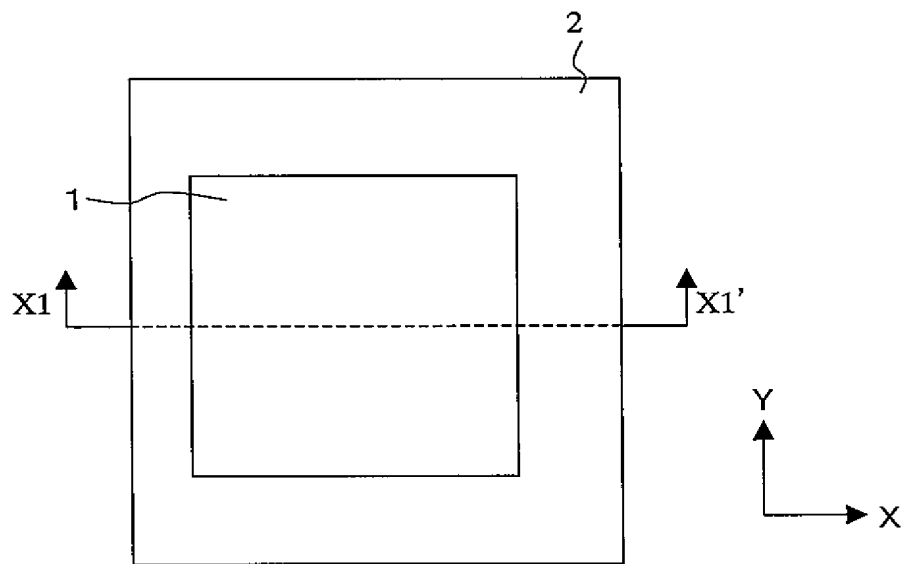
【図 6】



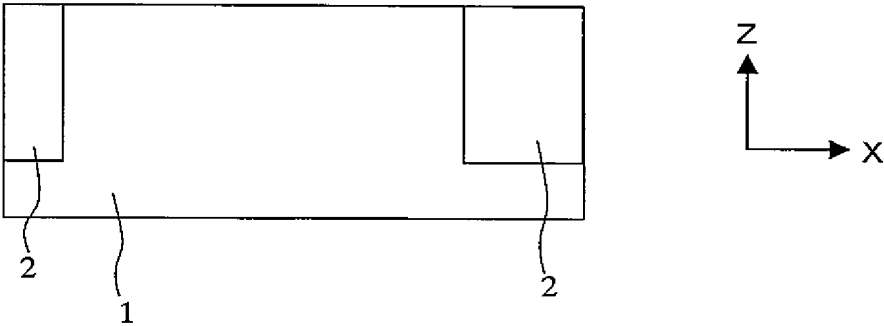
【図 7】



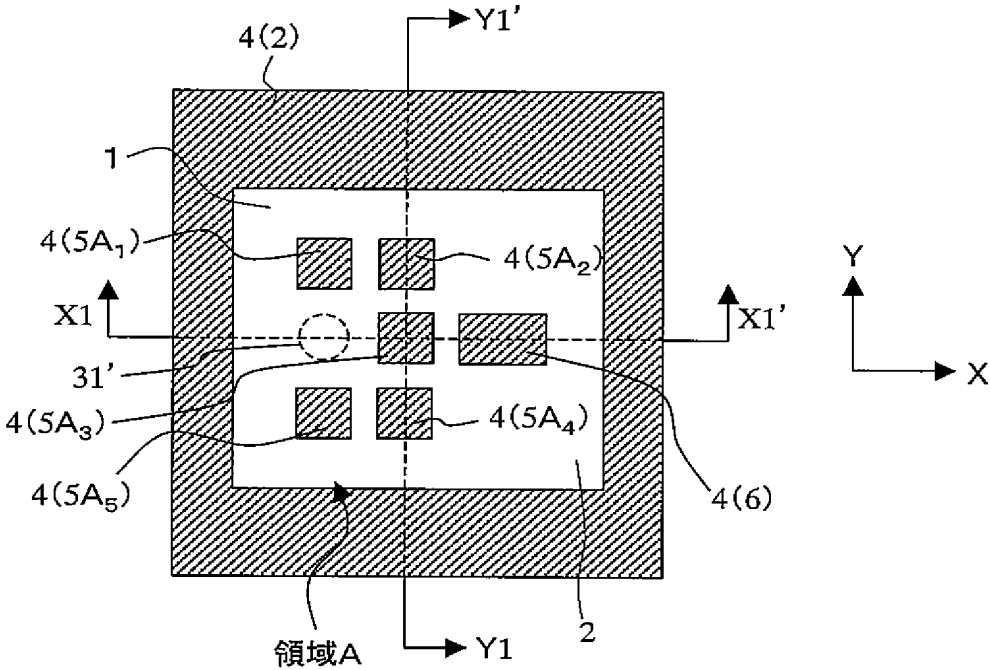
【図 8】



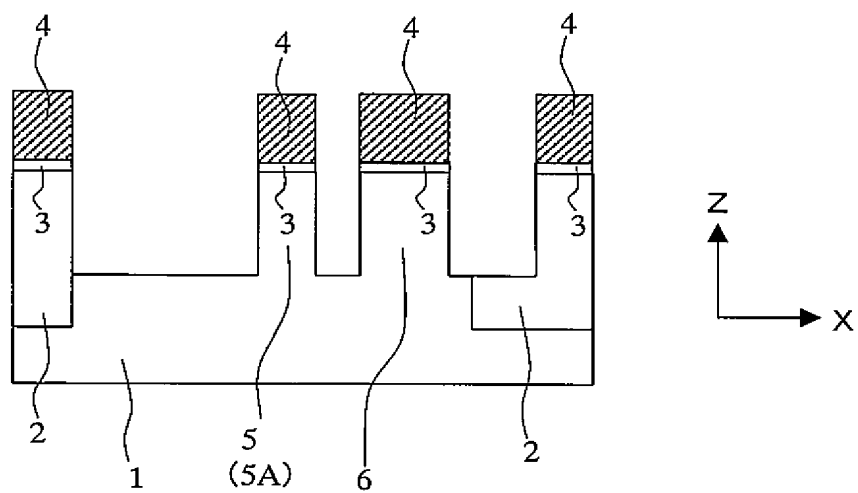
【図 9】



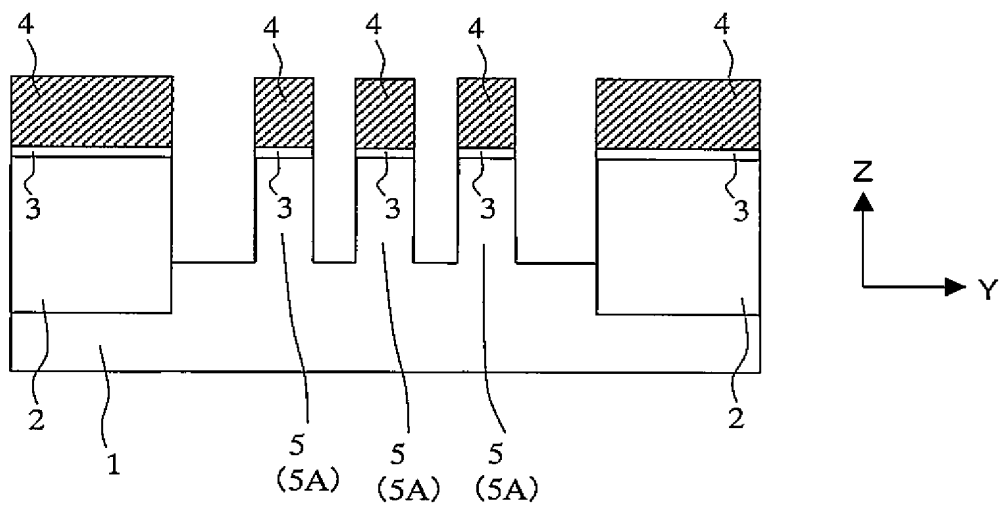
【図 10】



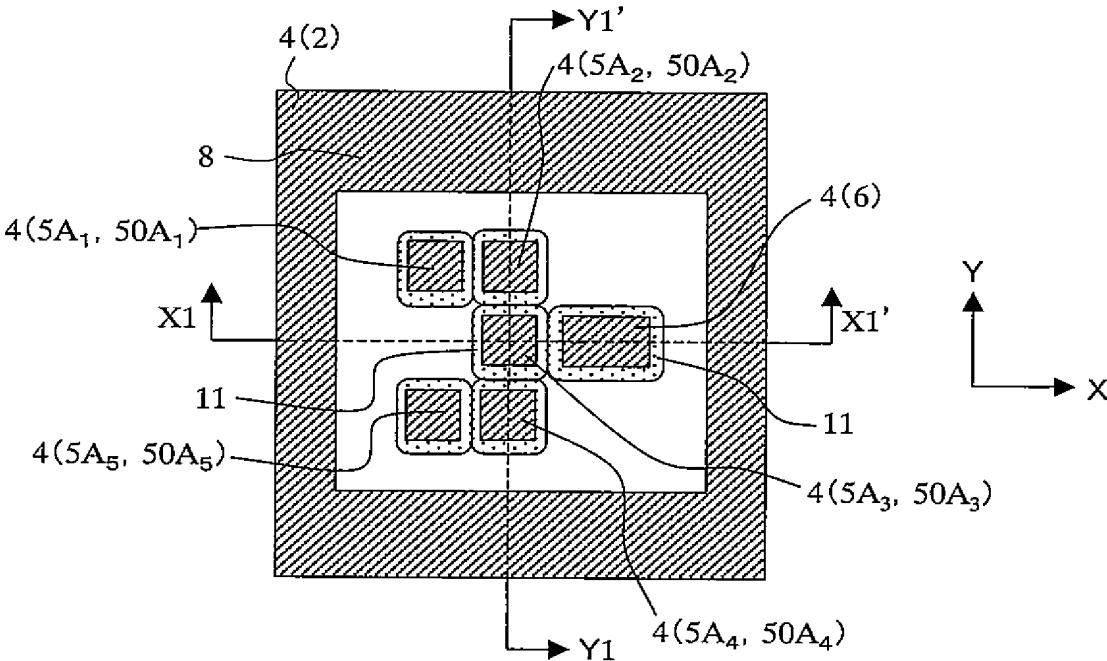
【図 1 1】



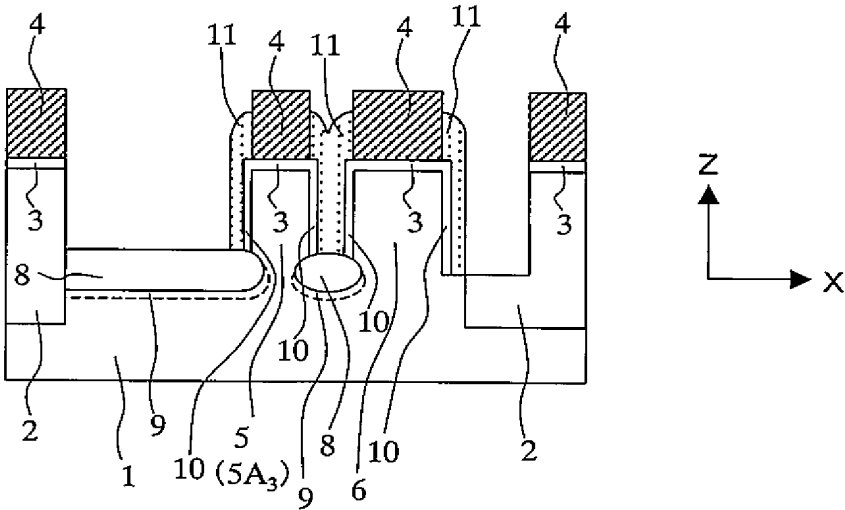
【図 1 2】



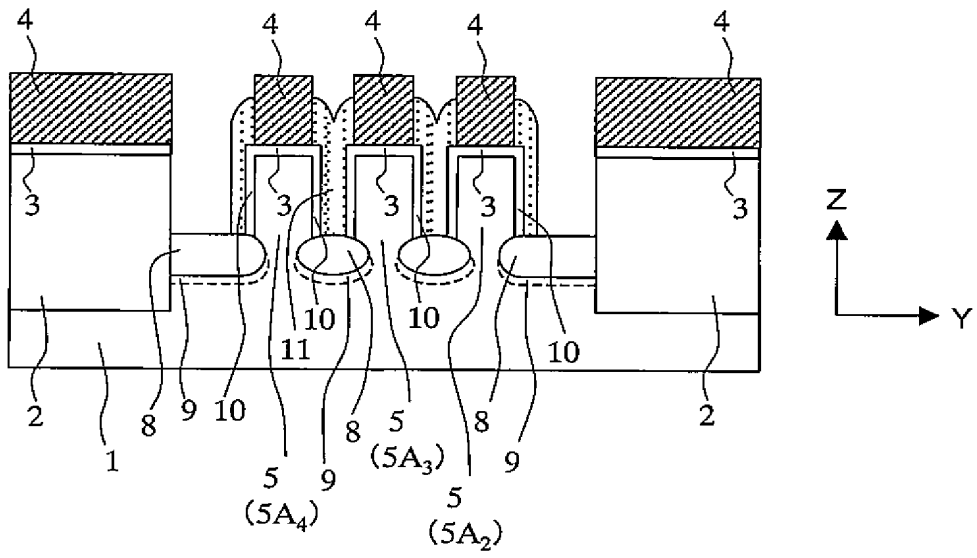
【図 1 3】



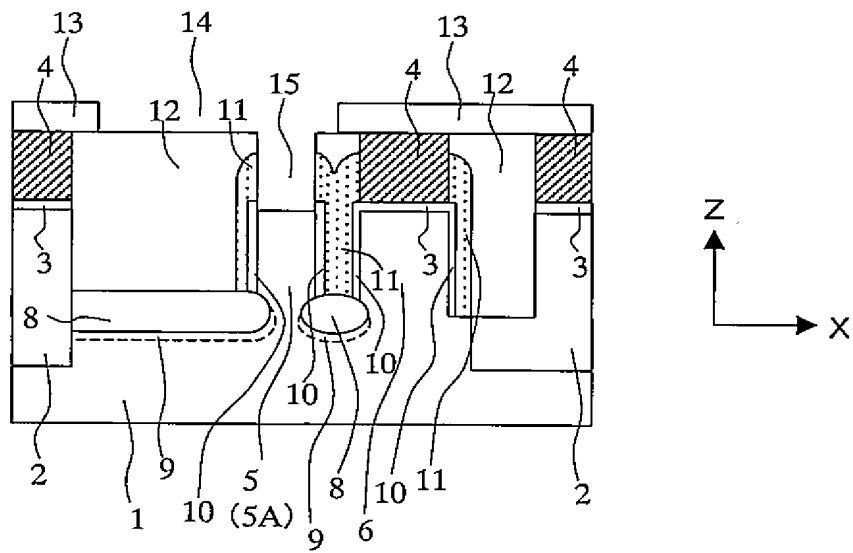
【図 1 4】



【図 15】



【図 16】



出願人履歴

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/872,844	10/01/2015	2811	1600	74735/258	4	1

CONFIRMATION NO. 1965

FILING RECEIPT

130036

IIPH2 [54361] c/o Stoel Rives LLP 130036
201 South Main Street, Suite 1100, One Utah Center
Salt Lake City, UT 84111



Date Mailed: 10/16/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

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Applicant(s)

PS4 Luxco S.a.r.l., Luxembourg, LUXEMBOURG;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/722,125 12/20/2012 PAT 9178056

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)
JAPAN 2011-285544 12/27/2011

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 10/15/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/872,844**

Projected Publication Date: 01/21/2016

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR DEVICE

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/872,844	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(j))	4	minus 20 = *			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s)) If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							0.00
							0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
			TOTAL			TOTAL	1600
* If the difference in column 1 is less than zero, enter "0" in column 2.							
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	x =
	Application Size Fee (37 CFR 1.16(s))					OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR	
			TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	x =
	Application Size Fee (37 CFR 1.16(s))					OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR	
			TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Yoshihiro TAKAISHI
Filed: October 1, 2015
Title: **SEMICONDUCTOR DEVICE**
Examiner: Not yet assigned
Serial No.: Not yet assigned
Art Unit: Not yet assigned
Conf. No.: Not yet assigned
Docket No: 74735/258 (12P00415US1)
Date: October 1, 2015

PRELIMINARY AMENDMENT

TO THE COMMISSIONER FOR PATENTS:

Prior to examination, please amend the above-identified Application as follows:

Amendments to the Specification begin on page 2; and

Remarks begin on page 3.

AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows. No new matter is entered.

Please replace the paragraph at line 4 of page 1 with the following amended paragraph:

This application is a continuation of, and claims priority to, United States Patent Application No. 13/722,125 filed on December 20, 2012, which claims the benefit of priority from Japanese Patent Application No. 2011-285544, filed on December 27, 2011, the disclosure of each of which is incorporated herein in its entirety by reference.

REMARKS

The specification is amended to update the cross-references to related applications section. Specifically, the specification is amended to clarify that this Application, "is a continuation of, and claims priority to, United States Patent Application No. 13/722,125 filed on December 20, 2012, which claims the benefit of priority from Japanese Patent Application No. 2011-285544, filed on December 27, 2011." No new matter is entered.

The Applicant respectfully submits that the Application is in condition for allowance. If the Examiner notes any further matters that may be resolved by a telephone interview or Examiner's amendment, the Examiner is encouraged to contact Joseph Hawkins by telephone at (801) 578-6971 or email at joe.hawkins@stoel.

Respectfully submitted,

By: /Joseph J. Hawkins/

Joseph J. Hawkins
Registration No. 63,194

STOEL RIVES LLP
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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SEMICONDUCTOR DEVICE		
First Named Inventor/Applicant Name:		Yoshihiro Takaishi		
Filer:		Joseph Jackson Hawkins/Janet Wilson		
Attorney Docket Number:		74735/258		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt

EFS ID:	23668489
Application Number:	14872844
International Application Number:	
Confirmation Number:	1965
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro Takaishi
Customer Number:	130036
Filer:	Joseph Jackson Hawkins/Janet Wilson
Filer Authorized By:	Joseph Jackson Hawkins
Attorney Docket Number:	74735/258
Receipt Date:	01-OCT-2015
Filing Date:	
Time Stamp:	17:04:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	3946
Deposit Account	502375
Authorized User	HAWKINS, JOSEPH J.

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Western Digital Exhibit 1002

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2015_10_01_TransmittalLtr.pdf	235376	no	1
			3115e81715c363b3bba7960545d475c59d1ac9e9		
Warnings:					
Information:					
2	Application Data Sheet	2015_10_01_ADS.pdf	1507950	no	6
			09e83cf7ae2b4232b0b71d78d27bbc5d5c499915		
Warnings:					
Information:					
3		2015_10_01_Application.pdf	2199911	yes	33
			d6d423d0a487de3109e3c2c845385a95fa5a7aac		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	30	
	Claims		31	32	
	Abstract		33	33	
Warnings:					
Information:					
4	Drawings-only black and white line drawings	2015_10_01_Drawings.pdf	420310	no	10
			c4a3aaa41207f57fecbeaa9ebabe63fe0d5e14a7		
Warnings:					
Information:					
5	Oath or Declaration filed	2015_10_01_Declaration.pdf	63953	no	1
			93e8bc27fa7ef05f840c977fca1f9cf3cfe60d69		
Warnings:					
Information:					
6	Assignee showing of ownership per 37 CFR 3.73	2015_10_01_Statement.pdf	119613	no	3
			022e6ba60a24ab8774e735e5b93d8e2d3f064810		

Warnings:					
Information:					
7	Information Disclosure Statement (IDS) Form (SB08)	2015_10_01_IDS.pdf	252701 5c71fa134acc48d12d16dc8515b9b7b1695c3d17	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
8	Preliminary Amendment	2015_10_01_PreliminaryAmendment.pdf	251143 2d170648f6f9acf16d4986aece452ef34b98e2bc	no	3
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	35038 0e8583b0f8026fa7694b7b878bbf0193d928046d	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			5085995		
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In re application of:

Yoshihiro TAKAISHI

Application No.

Filed: October 1, 2015

For: **SEMICONDUCTOR DEVICE**

Group Art Unit:

Examiner:

Confirmation No.

Docket No. 74735/258

TRANSMITTAL LETTER

I hereby certify that the following papers are being submitted for the above-referenced application ("Application") to the United States Patent and Trademark Office via EFS-Web electronic filing system on October 1, 2015.

1. An Application Data Sheet;
2. A Continuation Patent Application;
3. Drawings;
4. A Declaration;
5. A Statement Under 37 CFR 3.73(c);
6. An Information Disclosure Statement; and
7. A Preliminary Amendment.

The Commissioner is authorized to charge any additional fees required in connection with the filing of these papers, or credit overpayment, to **Deposit Account No. 502375**.

Signature: **Joseph J. Hawkins/**

Joseph J. Hawkins
joe.hawkins@stoel.com
(801) 578-6971
Registration No. 63,194
Dated October 1, 2015

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	74735/258
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--

Inventor Information:

Inventor 1 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Yoshihiro		TAKAISHI	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Tokyo	Country of Residence i	JP	
Mailing Address of Inventor:				
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Address 2		2-1, Yaesu 2-chome, Chuo-ku		
City	Tokyo	State/Province		
Postal Code		Country i	JP	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	130036		
Email Address	joe.hawkins@stoel.com	Add Email	Remove Email
Email Address	patlaw@stoel.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE		
Attorney Docket Number	74735/258	Small Entity Status Claimed ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	Suggested Figure for Publication (if any)	

Western Digital Exhibit 1002

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	74735/258
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE		

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

<p>Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.</p>			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	130036		

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This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.			
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13722125	2012-12-20
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).			
Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
2011-285544	JP	2011-12-27	
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	74735/258
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE		

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐	This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
--------------------------	--

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☐	Authorization to Permit Access to the Instant Application by the Participating Offices
<p>If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.</p> <p>In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.</p> <p>In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.</p>	

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<p>Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.</p>
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	74735/258
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE		

Applicant 1				Remove	
<p>If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.</p>					
Clear					
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117		☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign.			☐ Person who shows sufficient proprietary interest		
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:					
Name of the Deceased or Legally Incapacitated Inventor : <input type="text"/>					
If the Applicant is an Organization check here. ☒					
Organization Name		PS4 Luxco S.a.r.l.			
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Address 1		208, Val Des Bons Malades			
Address 2					
City		Luxembourg	State/Province		
Country ⁱ	LU	Postal Code		L-2121	
Phone Number			Fax Number		
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Additional Applicant Data may be generated within this form by selecting the Add button. Add					

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	74735/258
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE		

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information:

Address 1			
Address 2			
City		State/Province	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

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Signature:

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Signature	/Joseph J. Hawkins/		Date (YYYY-MM-DD)	2015-10-01
First Name	Joseph	Last Name	Hawkins	Registration Number
			63194	

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SEMICONDUCTOR DEVICE

This application claims the benefit of priority from Japanese Patent
5 Application No. 2011-285544, filed on December 27, 2011, the disclosure of
which is incorporated herein in its entirety by reference.

BACKGROUND OF THE INVENTION:

Field of the Invention

10 This invention relates to a semiconductor device.

Description of Related Art

In recent years, vertical transistors have been proposed as a technique
for transistor miniaturization.

The vertical transistor is a transistor which uses as a channel a
15 semiconductor pillar extending in a direction perpendicular to a main surface of
a semiconductor substrate.

Specifically, as disclosed in, for example, JP-A-2009-081389 (Patent
Document 1), in a vertical transistor, a semiconductor pillar (base pillar) is
provided to stand from a semiconductor substrate and a gate electrode is
20 provided around the semiconductor pillar with a gate insulating film interposed
therebetween. A drain region and a drain electrode are provided on the side of
a lower portion of the semiconductor pillar while a source region and a source
electrode are provided at an upper portion of the semiconductor pillar.

As compared with a conventional transistor in which a channel is
25 disposed parallel to the substrate plane, the area in the plane occupied by the
vertical transistor is smaller and, even if the channel length (gate length) is
increased, there is no increase in transistor occupation area in the plane.

Consequently, it is possible to suppress the short channel effect without

increasing the transistor occupation area in the plane. Further, the vertical transistor has an advantage that since the channel can be fully depleted, it is possible to obtain a satisfactory S value (subthreshold swing value) and a large drain current.

5 In addition, in the vertical transistor, since the gate electrode is formed over the entire periphery of the channel, i.e. the gate electrode covers the entire periphery of the channel, it is possible to effectively control the potential of the channel by a voltage applied to the gate electrode without being affected by external factors other than the source and the drain.

10

SUMMARY:

 Herein, in order to obtain a high current drive capability while maintaining the transistor characteristics, a vertical transistor type semiconductor device may be provided with a plurality of semiconductor pillars, wherein upper diffusion layers provided at upper portions of the semiconductor pillars are connected in parallel to each other and lower diffusion layers provided at lower portions of the semiconductor pillars are connected in parallel to each other. In this event, variation in electrical resistance between upper contact plugs, which are connected to the upper diffusion layers, and the semiconductor pillars is in an allowable range because, in terms of the structure in which the upper diffusion layers are provided at the upper ends of the semiconductor pillars, connecting positions of the upper contact plugs are limited. On the other hand, there has been a problem that electrical resistances between a lower contact plug, which is connected to the lower diffusion layers, and the semiconductor pillars largely differ depending on connecting positions between the lower diffusion layers and the lower contact plug and that if the maximum interval between the semiconductor pillar and the lower contact plug becomes more than twice the minimum interval between the

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semiconductor pillar and the lower contact plug in plan view, there occurs variation in characteristics of transistors provided to the semiconductor pillars.

Therefore, a semiconductor device has been desired which, even in a structure where a plurality of vertical transistors are connected to each other,
5 can stabilize the characteristics of the transistors provided to individual semiconductor pillars.

In one embodiment, there is provided a semiconductor device comprising a plurality of vertical transistors provided to stand from a semiconductor substrate and comprising a diffusion layer at their end portions
10 on the semiconductor substrate side; and a conductive plug provided to stand from the semiconductor substrate and connected to the diffusion layer of the plurality of vertical transistors, wherein the plurality of vertical transistors are uniformly arranged near the conductive plug and share the diffusion layer and the conductive plug.

15 In another embodiment, there is provided a semiconductor device comprising a semiconductor pillar provided to stand from a semiconductor substrate and forming a channel a gate insulating film and a gate electrode provided over a side surface of the semiconductor pillar an upper diffusion layer provided at an upper end of the semiconductor pillar and serving as one of a
20 source and a drain a lower diffusion layer provided at a lower end of the semiconductor pillar and serving as the other of the source and the drain and a lower diffusion layer side contact plug connected to the lower diffusion layer, the plurality of semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug, and the semiconductor pillars are uniformly
25 arranged near the lower diffusion layer side contact plug.

In still another embodiment, there is provided a semiconductor device comprising a semiconductor substrate comprising an active region on its surface, a plurality of vertical transistors provided in the active region so as to

stand from the semiconductor substrate and comprising a lower diffusion layer at their end portions on the semiconductor substrate side and upper diffusion layers at their other end portions; and a conductive plug provided to stand from the semiconductor substrate and connected to the lower diffusion layer of the plurality of vertical transistors, wherein the plurality of vertical transistors are uniformly arranged near the conductive plug and share the upper diffusion layers and the lower diffusion layer so as to be connected in parallel to each other.

(Effect of the Invention)

10 According to this invention, it is possible to provide a semiconductor device which, even in a structure where a plurality of vertical transistors are connected to each other, can stabilize the characteristics of the transistors provided to individual semiconductor pillars.

15 BRIEF DESCRIPTION OF THE DRAWINGS:

The above features and advantages of the present invention will be more apparent from the following description of certain preferred embodiments taken in conjunction with the accompanying drawings, in which:

20 Fig. 1 is an exemplary diagram (plan view) showing the structure of a semiconductor device 100 according to a first embodiment of this invention, wherein, in order to clarify the arrangement of components, interconnections located on an interlayer insulating film and on contact plugs are shown in a see-through state with only their profiles given in dotted lines;

Fig. 2 is a cross-sectional view taken along line X1-X1' of Fig. 1;

25 Fig. 3 is a cross-sectional view taken along line Y1-Y1' of Fig. 1;

Fig. 4 is an exemplary diagram (plan view) showing the structure of a semiconductor device 100a according to a second embodiment of this invention;

Fig. 5 is an exemplary diagram (plan view) showing the structure of a semiconductor device 100b according to a third embodiment of this invention;

Fig. 6 is an exemplary diagram (plan view) showing the structure of a semiconductor device 100c according to a fourth embodiment of this invention;

5 Fig. 7 is an exemplary diagram (plan view) showing the structure of a semiconductor device 100d according to a fifth embodiment of this invention;

Fig. 8 is a diagram (plan view) for explaining a method of manufacturing the semiconductor device 100 according to the first embodiment;

Fig. 9 is a cross-sectional view taken along line X1-X1' of Fig. 8;

10 Fig. 10 is a diagram (plan view) for explaining the method of manufacturing the semiconductor device 100 according to the first embodiment;

Fig. 11 is a cross-sectional view taken along line X1-X1' of Fig. 10;

Fig. 12 is a cross-sectional view taken along line Y1-Y1' of Fig. 10;

15 Fig. 13 is a diagram (plan view) for explaining the method of manufacturing the semiconductor device 100 according to the first embodiment;

Fig. 14 is a cross-sectional view taken along line X1-X1' of Fig. 13;

Fig. 15 is a cross-sectional view taken along line Y1-Y1' of Fig. 13;

Fig. 16 is a diagram (cross-sectional view) for explaining the method of manufacturing the semiconductor device 100 according to the first embodiment;

20 Fig. 17 is a diagram (cross-sectional view) for explaining the method of manufacturing the semiconductor device 100 according to the first embodiment;

Fig. 18 is a diagram (plan view) for explaining the method of manufacturing the semiconductor device 100 according to the first embodiment, wherein, in order to clarify the arrangement of components, those components
25 underlying an uppermost layer are shown in broken lines;

Fig. 19 is a cross-sectional view taken along line X1-X1' of Fig. 18; and

Fig. 20 is a cross-sectional view taken along line Y1-Y1' of Fig. 18.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS:

Hereinbelow, preferred embodiments of this invention will be described in detail with reference to the drawings.

First, referring to Figs. 1, 2, and 3, a schematic structure of a semiconductor device 100 according to a first embodiment of this invention will be described.

As shown in a plan view of Fig. 1, the semiconductor device 100 according to the first embodiment has, on a semiconductor substrate of silicon single crystal or the like, an STI (shallow trench isolation) 2 serving as an element isolation region, and an active region 1A (broken-line region) which is the semiconductor substrate surrounded by the STI 2. In the active region 1A, five vertical transistors, i.e. a first unit transistor 50A₁, a second unit transistor 50A₂, a third unit transistor 50A₃, a fourth unit transistor 50A₄, and a fifth unit transistor 50A₅, are arranged in a $\square$ -shape and protrude from a semiconductor substrate surface. An impurity diffusion layer is provided in a surface portion, located around the unit transistors, of the active region 1A and forms a lower diffusion layer shared by the vertical transistors. A metal contact plug 31 connected to the lower diffusion layer and shared by the vertical transistors is disposed in a central region of the $\square$ -shape. Metal contact plugs 30 are disposed above the vertical transistors and are connected to each other by a metal interconnection 33 disposed in contact with upper surfaces of the metal contact plugs 30. Accordingly, the five vertical transistors share the lower diffusion layer and further share the metal interconnection 33 disposed above them. That is, the semiconductor device 100 forms a single vertical transistor in which the five vertical transistors are connected in parallel to each other. A pillar groove forming region A is arranged as an expanded region defined by moving one side surface of the active region 1A to the STI 2 side. As will be described later, a dummy pillar (gate-lift pillar) 6 for applying a gate voltage to

gate electrodes of the five vertical transistors is disposed at the boundary between the active region 1A and the STI 2 in the pillar groove forming region A. The dummy pillar 6 comprises a first dummy pillar (gate-lift silicon pillar) 6A which is a silicon pillar disposed on the active region 1A side and a second
 5 dummy pillar (gate-lift insulating film pillar) 6B which is an insulating film pillar disposed on the STI 2 side. Facing side surfaces of the first and second dummy pillars 6A and 6B are in contact with each other, thereby forming an integral composite pillar.

Referring to Fig. 1, the structure of the semiconductor device 100 will be
 10 described in further detail.

The unit transistors are uniformly arranged around the metal contact plug 31. In the first embodiment, "uniformly arranged" represents an arrangement in which, in plan view, the distance between the metal contact plug 31 and a closest portion of the unit transistor farthest from the metal contact
 15 plug 31 is twice or less the distance between the metal contact plug 31 and a closest portion of the unit transistor closest to the metal contact plug 31. Each of silicon pillars 5 forming channels of the respective unit transistors has a rectangular shape in plan view in which a width in an X-direction (first direction) and a width in a Y-direction (second direction) perpendicular to the X-direction
 20 are equal to each other. Herein, the width is set to 50nm. The shape of each silicon pillar 5 in plan view is not limited to rectangular and may be circular. In the case of the circular shape, the diameter is set to 50nm.

As described above, the silicon pillars respectively form the channels of the unit transistors. That is, the five silicon pillars, i.e. the first silicon pillar $5A_1$,
 25 the second silicon pillar $5A_2$, the third silicon pillar $5A_3$, the fourth silicon pillar $5A_4$, and the fifth silicon pillar $5A_5$, respectively correspond to the five unit transistors, i.e. the first unit transistor $50A_1$, the second unit transistor $50A_2$, the third unit transistor $50A_3$, the fourth unit transistor $50A_4$, and the fifth unit

transistor 50A₅.

The five unit transistors are arranged in the $\sqcap$ -shape in plan view. That is, the two unit transistors, i.e. the first unit transistor 50A₁ and the second unit transistor 50A₂, are arranged at an interval therebetween so that their
 5 centers are located on the same line in the X-direction. Herein, this interval is set to 30nm. Further, the three unit transistors, i.e. the second unit transistor 50A₂, the third unit transistor 50A₃, and the fourth unit transistor 50A₄, are arranged at an interval therebetween so that their centers are located on the same line in the Y-direction. Herein, this interval is set to 30nm. Further, the
 10 two unit transistors, i.e. the fourth unit transistor 50A₄ and the fifth unit transistor 50A₅, are arranged at an interval therebetween so that their centers are located on the same line in the X-direction. Herein, this interval is set to 30nm. The first and second unit transistors 50A₁ and 50A₂ and the fifth and fourth unit transistors 50A₅ and 50A₄ are arranged at positions which are axisymmetric
 15 with respect to a line extending in the X-direction through the center of the third unit transistor 50A₃. Consequently, the five unit transistors are arranged in the $\sqcap$ -shape.

Right above the unit transistors, silicon plugs 19, the metal contact plugs 30, and the metal interconnection 33 are disposed. Each unit transistor,
 20 the corresponding silicon plug 19, and the corresponding metal contact plug 30 are arranged so as to overlap each other in plan view in the same region. The metal interconnection 33 is arranged so as to extend in the XY-directions to thereby form a $\sqcap$ -shape along the arrangement of the five unit transistors. The metal interconnection 33 is connected, through the silicon plugs 19 and the
 25 metal contact plugs 30, to pillar upper diffusion layers provided at upper portions of the silicon pillars to form the unit transistors and serves as power feed wiring to the unit transistors. In this manner, the five unit transistors are connected in parallel to each other by the metal interconnection 33, thereby forming a single

parallel transistor.

On the other hand, the dummy pillar 6 of a rectangular shape in plan view is adjacently disposed at an interval from the third silicon pillar $5A_3$ in the X-direction and stands from the silicon substrate 1 and the STI 2. Herein, this interval is set to 30nm. The dummy pillar 6 lies over the active region 1A and the STI 2 and comprises the first dummy pillar 6A standing on the active region 1A side formed by the silicon substrate 1 and the second dummy pillar 6B standing on the STI 2 side. One side surface of the first dummy pillar 6A is in contact with one side surface of the second dummy pillar 6B so as to be integrated together. Another side surface of the first dummy pillar 6A faces one side surface, located at a position closest to the first dummy pillar 6A, of the third silicon pillar $5A_3$. A metal contact plug 41 of a rectangular shape in plan view is disposed right above the second dummy pillar 6B. The metal contact plug 41 is arranged at a position partially overlapping the second dummy pillar 6B in plan view and slightly protrudes outward of the second dummy pillar 6B in the X-direction. In Fig. 1, as described above, the metal contact plug 41 is offset in the X-direction with respect to the second dummy pillar 6B, but the configuration is not limited thereto. The metal contact plug 41 may be offset in the Y-direction at an arbitrary position within a range that is free of contact with the silicon pillars.

On side surfaces of each silicon pillar, a gate electrode 11a is provided with a gate insulating film 10 interposed therebetween. The gate electrodes 11a are connected to each other by burying gaps (spaces) between the adjacent silicon pillars, thereby forming a single gate electrode 11a shared by the silicon pillars. On the other hand, a power feed gate electrode 11b is provided on side surfaces of the dummy pillar 6. The power feed gate electrode 11b and the gate electrode 11a are connected to each other by burying a gap (space) between the dummy pillar 6 and the closest silicon pillar

(5A₃ in Fig. 1).

The metal contact plug 41 is connected, at its above-mentioned protruding portion, to the power feed gate electrode 11b provided on the side surface of the second dummy pillar 6B. The thickness in plan view (the
 5 thickness in the X-direction in Fig. 2) of each of the gate electrodes 11a and the power feed gate electrode 11b is set to 20nm. Hereinbelow, the gate electrodes 11a and the power feed gate electrode 11b will be collectively referred to as gate electrodes 11.

Since the thickness of each gate electrode 11 is set to 20nm, the
 10 interval between the silicon pillars and the interval between the silicon pillar and the dummy pillar, each set to 30nm as described above, are each twice or less the thickness of each gate electrode 11. Therefore, the gate electrodes 11 each having the thickness of 20nm, which are provided on the side surfaces of the first to fifth silicon pillars 5A₁ to 5A₅ and the dummy pillar 6, are in contact
 15 with each other in the portions where the interval between the pillars is set to 30nm, i.e. twice or less the thickness of each gate electrode 11, so that the gate electrodes 11 function as a single gate electrode. Consequently, a gate voltage supplied from the power feed gate electrode 11b of the dummy pillar 6 is supplied through the gate electrode 11a of the third silicon pillar 5A₃ to the gate
 20 electrodes 11a of the first silicon pillar 5A₁, the second silicon pillar 5A₂, the fourth silicon pillar 5A₄, and the fifth silicon pillar 5A₅.

In Fig. 1, the metal contact plug 31 is provided so as to be surrounded by the five unit transistors arranged in the $\square$ -shape. As shown in Fig. 1, the metal contact plug 31 has a circular shape in plan view having its center at an
 25 intersection between a center line in the Y-direction passing through the centers of the first and fifth unit transistors 50A₁ and 50A₅ and a center line in the X-direction passing through the center of the third unit transistor 50A₃. In the first embodiment, the diameter of the metal contact plug 31 is set to 40nm. As

described before, the width of each silicon pillar in each of the XY-directions is set to 50nm and the interval between the silicon pillars is set to 30nm.

Therefore, the closest interval between the outer periphery of the metal contact plug 31 and each of the first silicon pillar 5A₁, the third silicon pillar 5A₃, and the fifth silicon pillar 5A₅ is 35nm, which is the minimum interval.

On the other hand, the second silicon pillar 5A₂ and the fourth silicon pillar 5A₄ are each located in a direction inclined by 45 degrees from the X-direction with respect to the metal contact plug 31. Therefore, one corner of the rectangular shape of each of the second silicon pillar 5A₂ and the fourth silicon pillar 5A₄ is closest to the outer periphery of the metal contact plug 31. In this case, the closest interval therebetween is 57nm.

In the first embodiment, the interval between the outer periphery of the metal contact plug 31 and each of the first silicon pillar 5A₁, the third silicon pillar 5A₃, and the fifth silicon pillar 5A₅, the center of which is located on the same center line in the X- or Y-direction as the center of the metal contact plug 31, is 35nm, which is the minimum interval. On the other hand, the interval between the outer periphery of the metal contact plug 31 and each of the second silicon pillar 5A₂ and the fourth silicon pillar 5A₄, each located in the direction inclined by 45 degrees from the center line in the X-direction with respect to the metal contact plug 31, is 57nm, which is the maximum interval. In this case, since the maximum interval (57nm) is twice or less the minimum interval (35nm), it is possible to avoid the prior art problem that the intervals between the metal contact plug 31 and the respective silicon pillars become non-uniform so that parasitic resistances of the lower diffusion layer from the metal contact plug 31 to the respective silicon pillars differ from each other, resulting in unstable characteristics of the entire semiconductor device. If each silicon pillar has a circular shape in plan view having a diameter of 50nm, the maximum interval becomes 67nm. Accordingly, even in this case, the

maximum interval (67nm) is twice or less the minimum interval (35nm) so that it is possible to avoid the above-mentioned problem.

A metal interconnection 34 is disposed on the metal contact plug 31. The metal interconnection 34 is connected to the pillar lower diffusion layer 9, forming the unit transistors, through the metal contact plug 31, thereby serving as power feed wiring to the pillar lower diffusion layer 9.

While a description will be given later with reference to Fig. 16, a pattern 40 shown in Fig. 1 represents a region, which is removed for providing the silicon plugs 19, of a mask film 13 (not illustrated), wherein the inside of the pattern 40 is an opening 14 (not illustrated).

Next, referring to Figs. 2 and 3, details of the structure of the individual unit transistors 50 will be further described. The STI (shallow trench isolation; element isolation region) 2 is provided on the silicon substrate 1. The five silicon pillars 5, i.e. the first to fifth silicon pillars $5A_1$ to $5A_5$, each being a semiconductor base pillar, are provided to stand upright in the active region 1A which is the silicon substrate 1 surrounded by the STI 2.

Each silicon pillar 5 is a columnar semiconductor forming a channel of the corresponding unit transistor 50. Therefore, each unit transistor is a vertical transistor. The five silicon pillars are arranged so as to have the same height in the active region 1A defined by the STI 2. The thickness of each silicon pillar (the size of a cross section taken along a plane parallel to a surface of the silicon substrate 1) is set so as to allow full depletion of the channel.

Each unit transistor has impurity diffusion layers at upper and lower end portions of the silicon pillar 5. The pillar upper diffusion layer 16 located at the upper end portion of the silicon pillar forms one of a source and a drain while the pillar lower diffusion layer 9 located at the lower end portion of the silicon pillar forms the other of the source and the drain. A middle portion, between the pillar upper diffusion layer 16 and the pillar lower diffusion layer 9, of the

silicon pillar forms the channel.

The dummy pillar 6 is disposed adjacent, in the X-direction, to the third silicon pillar $5A_3$ located at the center of the five silicon pillars in the Y-direction. The silicon pillars 5 and the first dummy pillar 6A are formed by etching a surface of the silicon substrate 1 while the second dummy pillar 6B is formed by etching a surface of the STI 2. The first dummy pillar 6A is a columnar semiconductor protruding from the etched surface of the silicon substrate 1 while the second dummy pillar 6B is a columnar semiconductor protruding from the etched surface of the STI 2. The dummy pillar 6 serves as a protruding layer that increases the height of the power feed gate electrode 11b to reduce the distance between the power feed gate electrode 11b and a gate-lift interconnection 42 disposed above the power feed gate electrode 11b. The interval between the adjacent silicon pillars 5 and the interval between the dummy pillar 6 and the silicon pillar $5A_3$ are each set to twice or less the thickness of each gate electrode 11. Herein, this interval is set to 30nm. The thickness of each gate electrode 11 in plan view is set to 20nm.

An insulating film 8 is provided on the etched surface of the active region 1A (silicon substrate 1) located around the silicon pillars 5 and the first dummy pillar 6A. The insulating film 8 covers the etched surface around the silicon pillars 5 and the first dummy pillar 6A and reaches the STI 2. The pillar lower diffusion layer 9 is disposed under the insulating film 8 so as to overlap the insulating film 8 so that the pillar lower diffusion layer 9 is electrically insulated from the gate electrodes 11 by the insulating film 8. The pillar lower diffusion layer 9 electrically connects the five silicon pillars to each other and forms a lower diffusion layer common to the five unit transistors, i.e. the first to fifth unit transistors $50A_1$ to $50A_5$. The STI 2 is provided deeper than the pillar lower diffusion layer 9 so that pillar lower diffusion layers 9 in active regions 1A adjacent to each other across the STI 2 do not conduct each other.

The gate insulating films 10 are disposed on the side surfaces of the silicon pillars 5 and the first dummy pillar 6A. Further, the gate electrodes 11a and the power feed gate electrode 11b each having the thickness (the thickness in the X-direction in Fig. 2) of 20nm are respectively disposed on the side surfaces of the silicon pillars 5 and the first dummy pillar 6A with the gate insulating films 10 interposed therebetween. On the other hand, only the power feed gate electrode 11b is disposed on the side surfaces of the second dummy pillar 6B. Although not illustrated herein, gate electrodes 11 are also provided on portions of inner wall surfaces of the STI 2 and on portions of inner wall surfaces of an insulating film 3 and a mask film 4 stacked on the upper surface of the STI 2. The gate insulating films 10 cover the outer peripheral surfaces of the silicon pillars 5 and are connected to the insulating film 8. The silicon pillars 5 (channels), the pillar upper diffusion layers 16, and the pillar lower diffusion layer 9 disposed under the insulating film 8 are electrically insulated from the gate electrodes 11 by the gate insulating films 10 and the insulating film 8.

As shown in Fig. 2, for example, the unit transistor 50A₃ is formed by the lower diffusion layer 9, the upper diffusion layer 16, the gate insulating film 10, and the gate electrode 11a.

Insulating films 3 are disposed on the upper surfaces of the STI 2 and the dummy pillar 6. Mask films 4 are disposed over the upper surfaces of the STI 2 and the dummy pillar 6 so as to cover the insulating films 3 and, further, a first interlayer insulating film 12 is provided to cover the gate electrodes 11 and the insulating film 8. The first interlayer insulating film 12 is provided by burying a recess in the pillar groove forming region A. That is, the first interlayer insulating film 12 is provided in a region surrounded by the inner wall surfaces of the STI 2, the insulating film 3 stacked thereon, and the mask film 4 stacked thereon. A second interlayer insulating film 20 is provided on upper

surfaces of the mask films 4 and the first interlayer insulating film 12. A stopper film 21 is provided to cover the second interlayer insulating film 20 and, further, a third interlayer insulating film 24 is provided to cover the stopper film 21.

5 The gate-lift interconnection 42 is disposed on an upper surface of the third interlayer insulating film 24. The gate-lift interconnection 42 is connected to the power feed gate electrode 11b through the metal contact plug 41 passing through the third interlayer insulating film 24, the stopper film 21, the second interlayer insulating film 20, and the first interlayer insulating film 12.

10 Jointly with the dummy pillar 6, the mask film 4 disposed over the dummy pillar 6 serves as a protruding layer that increases the height of the power feed gate electrode 11b to reduce the distance between the power feed gate electrode 11b and the gate-lift interconnection 42.

 Metal interconnections 33 and 34 are disposed on the upper surface of
15 the third interlayer insulating film 24.

 The metal interconnection 33 is connected to the pillar upper diffusion layers 16 of the silicon pillars through the metal contact plugs 30 passing through the third interlayer insulating film 24, the stopper film 21, the second interlayer insulating film 20, and the silicon plugs 19 surrounded by the first
20 interlayer insulating film 12 and the gate electrodes 11a. The silicon plugs 19 are formed by injecting (diffusing) impurities such as arsenic into silicon. Jointly with the pillar upper diffusion layer 16, each silicon plug 19 forms one of the source and the drain of the unit transistor 50. A sidewall film 18 and an insulating film 17 are disposed on side surfaces of each silicon plug 19.

25 Consequently, the silicon plugs 19 are each electrically insulated from the gate electrode 11a by the sidewall film 18 and the insulating film 17.

 The metal interconnection 34 is connected to the pillar lower diffusion layer 9 through the metal contact plug (conductive plug) 31 passing through the

third interlayer insulating film 24, the stopper film 21, the second interlayer insulating film 20, the first interlayer insulating film 12, and the insulating film 8.

As described above, the semiconductor device 100 according to the first embodiment has the first and second unit transistors ($50A_1$, $50A_2$) which are arranged at an interval therebetween so that their centers are located on the same line in the first direction (X-direction), the second, third, and fourth unit transistors ($50A_2$, $50A_3$, $50A_4$) which are arranged at an interval therebetween so that their centers are located on the same line in the second direction (Y-direction) perpendicular to the first direction, and the fourth and fifth unit transistor ($50A_4$, $50A_5$) which are arranged at an interval therebetween so that their centers are located on the same line in the first direction, the first to fifth unit transistors standing upright and sharing the pillar lower diffusion layer 9 in the single active region 1A, and further has the metal contact plug 31 electrically connected to the pillar lower diffusion layer 9, wherein the metal contact plug 31 has a circular shape in plan view having its center at the intersection between the center line in the second direction passing through the centers of the first and fifth unit transistors $50A_1$ and $50A_5$ and the center line in the first direction passing through the center of the third unit transistor $50A_3$.

With this configuration, as shown in Fig. 1, in the semiconductor device 100, the closest interval W1 between the outer periphery of the metal contact plug 31 and the second silicon pillar $5A_2$ can be set to twice or less the closest interval W2 between the outer periphery of the metal contact plug 31 and the third silicon pillar $5A_3$, i.e. the uniform arrangement can be achieved. In this case, W1 represents the maximum interval while W2 represents the minimum interval. That is, the maximum interval can be set to twice or less the minimum interval.

Consequently, it is possible to avoid the prior art problem that the intervals between the metal contact plug 31 and the respective silicon pillars

become non-uniform so that parasitic resistances of the lower diffusion layer 9 from the metal contact plug 31 to the respective silicon pillars differ from each other, resulting in unstable characteristics of the entire semiconductor device 100.

5 Next, a semiconductor device 100a according to a second embodiment of this invention will be described with reference to Fig. 4.

In the second embodiment, unit transistors are additionally arranged at open ends of both side portions of the $\sqcap$ -shape in the first embodiment.

10 In the second embodiment, the same reference symbols are assigned to components having the same functions as in the first embodiment, thereby mainly describing those portions which are different from the first embodiment.

As shown in Fig. 4, the semiconductor device 100a according to the second embodiment is configured such that a sixth unit transistor $50A_6$ and a seventh unit transistor $50A_7$, which are new unit transistors, are respectively
15 arranged at open ends of both side portions of the $\sqcap$ -shape in the first embodiment. That is, three unit transistors, i.e. the seventh unit transistor $50A_7$, a first unit transistor $50A_1$, and a second unit transistor $50A_2$, are arranged at an interval therebetween so that their centers are located on the same line in the X-direction. Further, three unit transistors, i.e. the second unit transistor
20 $50A_2$, a third unit transistor $50A_3$, and a fourth unit transistor $50A_4$, are arranged at an interval therebetween so that their centers are located on the same line in the Y-direction. Further, three unit transistors, i.e. the fourth unit transistor $50A_4$, a fifth unit transistor $50A_5$, and the sixth unit transistor $50A_6$, are arranged at an interval therebetween so that their centers are located on the same line in
25 the X-direction. The seventh, first, and second unit transistors ($50A_7$, $50A_1$, $50A_2$) and the sixth, fifth, and fourth unit transistors ($50A_6$, $50A_5$, $50A_4$) are arranged at positions which are axisymmetric with respect to a line extending in the X-direction through the center of the third unit transistor $50A_3$.

Consequently, the seven unit transistors are arranged in a $\sqcap$ -shape. Each unit transistor is a vertical transistor. As in the first embodiment, the seven unit transistors share a pillar lower diffusion layer and are connected in parallel to each other by a metal interconnection 33, thereby forming a single parallel
5 transistor.

As in the first embodiment, a metal contact plug 31 of a circular shape in plan view is disposed so as to be surrounded by seven silicon pillars 5 at a central portion of a region sandwiched between the first silicon pillar 5A₁ and the fifth silicon pillar 5A₅ in the $\sqcap$ -shape.

10 With this configuration, the maximum interval given by the closest interval between the metal contact plug 31 and each of the second silicon pillar 5A₂, the fourth silicon pillar 5A₄, the sixth silicon pillar 5A₆, and the seventh silicon pillar 5A₇ in plan view can be set to twice or less the minimum interval given by the closest interval between the metal contact plug 31 and each of the
15 first silicon pillar 5A₁, the third silicon pillar 5A₃, and the fifth silicon pillar 5A₅ in plan view, i.e. the uniform arrangement can be achieved.

Consequently, the semiconductor device 100a according to the second embodiment can deal with a current greater than that in the first embodiment while avoiding unstable characteristics of the parallel transistor formed by the
20 vertical transistors.

Next, a semiconductor device 100b according to a third embodiment of this invention will be described with reference to Fig. 5.

In the third embodiment, unit transistors are arranged in a shape in which, using the transistor arrangement of the first embodiment as a basic
25 structure, a plurality of basic structures are combined in the Y-direction.

In the third embodiment, the same reference symbols are assigned to components having the same functions as in the first embodiment, thereby mainly describing those portions which are different from the first embodiment.

As shown in Fig. 5, the semiconductor device 100b according to the third embodiment has an active region 1A surrounded by an STI 2, wherein eight silicon pillars 5 (5A₁ to 5A₅ and 5A₈ to 5A₁₀) each having a rectangular shape in plan view are provided in the active region 1A. The eight silicon pillars 5 are arranged in a shape combining a plurality of □-shapes in plan view, herein, in a "double □-shape" combining two □-shapes. More specifically, part (5A₂ to 5A₄, 5A₈, 5A₉) of the eight silicon pillars 5 are arranged at regular intervals in the Y-direction and the first silicon pillar 5A₁ is arranged on the left side of the second silicon pillar 5A₂ at an interval therebetween in the X-direction which is the same as the interval between the adjacent silicon pillars 5 in the Y-direction. Like the first silicon pillar 5A₁, the fifth silicon pillar 5A₅ is arranged on the left side of the fourth silicon pillar 5A₄ and the tenth silicon pillar 5A₁₀ is arranged on the left side of the ninth silicon pillar 5A₉.

In the double □-shape defined by the eight silicon pillars 5, two metal contact plugs 31 (31A, 31B) each having a circular shape in plan view are respectively disposed at central portions of regions respectively sandwiched between the first silicon pillar 5A₁ and the fifth silicon pillar 5A₅ and between the fifth silicon pillar 5A₅ and the tenth silicon pillar 5A₁₀, so as to be respectively surrounded by the silicon pillars 5 arranged in □-shapes. With this configuration, the maximum interval given by the closest interval between the metal contact plug 31 (31A, 31B) and each of the second silicon pillar 5A₂, the fourth silicon pillar 5A₄, and the ninth silicon pillar 5A₉ in plan view can be set to twice or less the minimum interval given by the closest interval between the metal contact plug 31 (31A, 31B) and each of the first silicon pillar 5A₁, the third silicon pillar 5A₃, the fifth silicon pillar 5A₅, the eighth silicon pillar 5A₈, and the tenth silicon pillar 5A₁₀ in plan view, i.e. the uniform arrangement can be achieved.

Consequently, the semiconductor device 100b according to the third

embodiment can deal with a current greater than that in the first embodiment while avoiding unstable characteristics of the parallel transistor formed by the vertical transistors.

Next, a semiconductor device 100c according to a fourth embodiment of
5 this invention will be described with reference to Fig. 6.

In the fourth embodiment, unit transistors are additionally arranged at open ends of side portions of the double $\sqcap$ -shape in the third embodiment.

In the fourth embodiment, the same reference symbols are assigned to components having the same functions as in the third embodiment, thereby
10 mainly describing those portions which are different from the third embodiment.

As shown in Fig. 6, the semiconductor device 100c according to the fourth embodiment has an active region 1A surrounded by an STI 2, wherein eleven silicon pillars 5 ($5A_1$ to $5A_{11}$) each having a rectangular shape in plan view are provided in the active region 1A. The eleven silicon pillars 5 are
15 arranged in a double $\sqcap$ -shape in plan view. More specifically, part ($5A_2$ to $5A_4$, $5A_8$, $5A_9$) of the eleven silicon pillars 5 are arranged at regular intervals in the Y-direction and, further, the first silicon pillar $5A_1$ and the seventh silicon pillar $5A_7$ are arranged so as to be aligned with the second silicon pillar $5A_2$ in the X-direction. Like the first silicon pillar $5A_1$ and the seventh silicon pillar $5A_7$, the
20 fifth silicon pillar $5A_5$ and the sixth silicon pillar $5A_6$ are arranged so as to be aligned with the fourth silicon pillar $5A_4$ in the X-direction. Further, the tenth silicon pillar $5A_{10}$ and the eleventh silicon pillar $5A_{11}$ are arranged so as to be aligned with the ninth silicon pillar $5A_9$ in the X-direction. The interval between the silicon pillars aligned in the X-direction is the same as the interval between
25 the silicon pillars aligned in the Y-direction.

In the double $\sqcap$ -shape defined by the eleven silicon pillars 5, two metal contact plugs 31 (31A, 31B) each having a circular shape in plan view are respectively disposed at central portions of regions respectively sandwiched

between the first silicon pillar $5A_1$ and the fifth silicon pillar $5A_5$ and between the fifth silicon pillar $5A_5$ and the tenth silicon pillar $5A_{10}$. With this configuration, the maximum interval given by the closest interval between the metal contact plug 31 (31A, 31B) and each of the second silicon pillar $5A_2$, the fourth silicon pillar $5A_4$, the sixth silicon pillar $5A_6$, the seventh silicon pillar $5A_7$, the ninth silicon pillar $5A_9$, and the eleventh silicon pillar $5A_{11}$ in plan view can be set to twice or less the minimum interval given by the closest interval between the metal contact plug 31 (31A, 31B) and each of the first silicon pillar $5A_1$, the third silicon pillar $5A_3$, the fifth silicon pillar $5A_5$, the eighth silicon pillar $5A_8$, and the tenth silicon pillar $5A_{10}$ in plan view, i.e. the uniform arrangement can be achieved.

Consequently, the semiconductor device 100c according to the fourth embodiment can deal with a current greater than that in the third embodiment while avoiding unstable characteristics of the parallel transistor formed by the vertical transistors.

Next, a semiconductor device 100d according to a fifth embodiment of this invention will be described with reference to Fig. 7.

The fifth embodiment is configured such that, as different from the first to fourth embodiments, silicon pillars are uniformly arranged near metal contact plugs in a structure in which the silicon pillars are aligned in one row.

In the fifth embodiment, the same reference symbols are assigned to components having the same functions as in the first to fourth embodiments, thereby mainly describing those portions which are different from the first embodiment.

As shown in Fig. 7, the semiconductor device 100d according to the fifth embodiment has seven silicon pillars 5 ($5A_1$ to $5A_7$) arranged at regular intervals in the Y-direction and three metal contact plugs 31 (31A, 31B, 31C) arranged at regular intervals in the Y-direction.

More specifically, the metal contact plug 31B is disposed so that its center is aligned in the X-direction with the center of the fourth silicon pillar 5A₄ located in the middle of the seven silicon pillars 5 arranged in the Y-direction in a single active region 1A, and the metal contact plugs 31A and 31C are further
5 disposed so that their centers are respectively aligned in the X-direction with the centers of the second silicon pillar 5A₂ and the sixth silicon pillar 5A₆. The interval between each silicon pillar 5 and the corresponding metal contact plug 31 is set to twice or less the minimum interval. In this case, the interval between each metal contact plug 31 and the corresponding silicon pillar 5
10 facing it in the X-direction is the minimum interval.

In this manner, the silicon pillars 5 do not necessarily surround the contact plug 31 in a $\square$ -shape and it is satisfactory if the silicon pillars 5 are uniformly arranged with respect to the metal contact plug 31, i.e. the maximum interval between the metal contact plug 31 and the silicon pillar 5 is twice or less
15 the minimum interval between the metal contact plug 31 and the silicon pillar 5.

Next, a method of manufacturing the semiconductor device 100 according to the first embodiment will be described in detail with reference to Figs. 8 to 20.

Since methods of manufacturing the semiconductor devices 100a to
20 100d according to the second to fifth embodiments are the same as the method of manufacturing the semiconductor device 100 according to the first embodiment, explanation thereof is omitted.

First, as shown in Figs. 8 and 9, a trench 2a is formed in a silicon substrate 1 using photolithography and dry etching. The depth of the trench 2a
25 is set to, for example, 250nm. Then, an insulating film 2b in the form of a silicon nitride film or a silicon oxide film is deposited over the entire surface of the silicon substrate 1 by CVD (chemical vapor deposition), thereby burying the trench 2a. Thereafter, the unnecessary insulating film 2b formed on the silicon

substrate 1 is removed by CMP (chemical mechanical polishing) so that the insulating film 2b remains only in the trench 2a, thereby forming an STI 2 which will serve as an element isolation region. In this manner, an active region 1A surrounded by the STI 2 is formed.

5 Then, as shown in Figs. 10 to 12, an insulating film 3 in the form of a silicon oxide film is deposited to a thickness of 2nm on the silicon substrate 1 and the STI 2 by CVD and then a mask film 4 in the form of a silicon nitride film is deposited to a thickness of 120nm on the insulating film 3 by CVD. Then, a non-illustrated photoresist mask having a pattern which will be a pillar groove
10 forming region A defined by moving in parallel the position of one side surface of the active region 1A to the STI 2 side is formed by photolithography. The photoresist mask may be a hard mask such as an amorphous carbon film. In this event, patterns corresponding to the arrangement of five silicon pillars 5A₁ to 5A₅ arranged in a $\sqcap$ -shape and a pattern corresponding to the arrangement
15 of a dummy pillar 6 lying over the boundary between the active region 1A and the STI 2 are simultaneously formed. Each of the patterns corresponding to the silicon pillars 5A₁ to 5A₅ is formed to have a rectangular shape having a width of 50nm in each of the XY-directions. Each pattern is not limited to the rectangular shape and may have a circular shape with a diameter of 50nm.
20 Further, the interval between the silicon pillars 5 is set to twice or less the thickness of each of gate electrodes which will be formed later. Specifically, in Fig. 10, the interval between the first silicon pillar 5A₁ and the second silicon pillar 5A₂ which are arranged so that their centers are located on the same line in the X-direction is set to 30nm. Likewise, the interval between the fifth silicon
25 pillar 5A₅ and the fourth silicon pillar 5A₄ which are arranged so that their centers are located on the same line in the X-direction is also set to 30nm. Further, the intervals between the second silicon pillar 5A₂ and the third silicon pillar 5A₃ and between the third silicon pillar 5A₃ and the fourth silicon pillar 5A₄,

whose centers are located on the same line in the Y-direction, are also each set to 30nm.

The center of the inside of the $\square$ -shape is a position 31' where a metal contact plug 31 will be disposed later and, in other words, the silicon pillars 5 are uniformly arranged around the position 31' (in Fig. 10, the silicon pillars 5 are arranged in the $\square$ -shape so as to surround the position 31').

Likewise, the dummy pillar 6 is arranged adjacent to the third silicon pillar 5A₃ in the X-direction at an interval twice or less the thickness of each gate electrode. Herein, the interval between the third silicon pillar 5A₃ and the dummy pillar 6 is also set to 30nm. The thickness of each silicon pillar 5 (the size of a cross section taken along a plane parallel to the silicon substrate 1), which forms a channel, is set so as to allow full depletion of the channel. The width, in the Y-direction, of the dummy pillar 6 for lifting the gate electrode is set equal to the width of the silicon pillar 5 in the Y-direction while the width of the dummy pillar 6 in the X-direction may be different from that of the silicon pillar 5.

Then, by anisotropic dry etching using the photoresist mask, the patterns are transferred to the mask film 4 and the insulating film 3. As a result, an upper surface of the silicon substrate 1 and an upper surface of the STI 2 are exposed in a patterned opening portion (pillar groove forming region A). Thereafter, the photoresist mask is removed.

Then, using the patterned mask films 4 as a mask, the exposed silicon substrate 1 and STI 2 are dug down to a depth of 150nm by anisotropic dry etching, thereby forming the five silicon pillars 5 (5A₁ to 5A₅), which will serve as channels of unit transistors, and the dummy pillar 6 for connecting the power feed gate electrode to an upper interconnection. The pillars are formed so as to protrude upward from the dug-down upper surfaces of the silicon substrate 1 and the STI 2. The silicon pillars 5 are each formed into the rectangular shape having the width of 50nm in each of the XY-directions. As shown in Fig. 11, the

dummy pillar 6 is formed as a composite pillar in which one side surface of a first dummy pillar 6A standing on the active region 1A side and one side surface of a second dummy pillar 6B standing on the STI 2 side are in contact with each other so as to be integrated together.

5 Then, as shown in Figs. 13 to 15, side surfaces of the silicon pillars 5 and the dummy pillar 6 are oxidized to a thickness of 5nm by thermal oxidation (not illustrated) and, then, after depositing a silicon nitride film to a thickness of 20nm by CVD, the entire surface is etched back to form sidewall films on the side surfaces of the silicon pillars 5, the dummy pillar 6, the insulating films 3,
10 and the mask films 4. Then, an insulating film 8 is formed to a thickness of 30nm by thermal oxidation at a portion, around the pillars, of the active region 1A, where the dug-down upper surface of the silicon substrate 1 is exposed. In this event, the side surfaces of the silicon pillars 5 and the dummy pillar 6 are not oxidized because the silicon nitride films are coated thereon.

15 Then, a pillar lower diffusion layer 9 is formed under the insulating film 8 by ion implantation. Herein, the pillar lower diffusion layer 9 is shared by the five silicon pillars 5 (5A₁ to 5A₅). As impurities for the ion implantation, it is possible to use, for example, arsenic in the case of an n-type transistor. Then, the sidewall films and the thermal oxide films formed on the side surfaces of the
20 silicon pillars 5 and the dummy pillar 6 are removed by dry etching or wet etching.

 Then, gate insulating films 10 each in the form of a silicon oxide film having a thickness of 3nm are formed on the side surfaces of the silicon pillars 5 and the first dummy pillar 6A by thermal oxidation. Then, a polysilicon film
25 (polycrystalline silicon film) having a thickness of 20nm, which will be gate electrodes, is deposited over the entire surface by CVD and then the entire surface is etched back, thereby forming gate electrodes 11a on the side surfaces of the silicon pillars 5 and a power feed gate electrode 11b on the side

surfaces of the dummy pillar 6. When the gate electrodes 11 are formed on the side surfaces of the silicon pillars 5 and the dummy pillar 6, gate electrodes 11 (not illustrated) are also formed on the side surfaces of the STI 2. As shown in Figs. 14 and 15, since, as described before, the interval between the adjacent silicon pillars 5 and the interval between the third silicon pillar 5A₃ and the dummy pillar 6 are each set to 30nm, i.e. twice or less the thickness of each gate electrode 11, gaps between the adjacent silicon pillars 5 and a gap between the third silicon pillar 5A₃ and the dummy pillar 6 are completely buried by the gate electrodes 11a and the power feed gate electrode 11b.

Consequently, the gate electrodes 11a on the side surfaces of the first to fifth silicon pillars 5A₁ to 5A₅ are integrally connected to each other and, further, the power feed gate electrode 11b on the side surfaces of the dummy pillar 6 is integrally connected to the gate electrode 11a on the side surfaces of the third silicon pillar 5A₃.

Then, as shown in Fig. 16, a first interlayer insulating film 12 in the form of a silicon oxide film is deposited by CVD so as to bury the silicon pillars 5 and the dummy pillar 6. Then, the first interlayer insulating film 12 is flattened by CMP so as to expose the mask films 4. Subsequently, a mask film 13 in the form of a silicon oxide film is deposited to a thickness of 50nm by CVD.

Then, the mask film 13 is partially removed by photolithography and etching. A pattern 40, to be removed, of the mask film 13 is, as shown in Fig. 1, only a region where the silicon pillars 5 are arranged. At an opening 14 with the mask film 13 removed, the mask films 4 above the silicon pillars 5 are exposed. Then, the exposed mask films 4 are selectively removed by wet etching and further the insulating films 3 are removed, thereby forming openings 15 above the silicon pillars 5. Upper surfaces of the silicon pillars 5 are exposed at the bottom of the openings 15 and the gate electrodes 11a are partially exposed at side surfaces of the openings 15.

Then, as shown in Fig. 17, an insulating film 17 in the form of a silicon oxide film is formed on inner walls of each opening 15 by thermal oxidation. Then, impurities (e.g. phosphorus or arsenic in the case of an n-type transistor) are implanted into upper end portions of the silicon pillars 5 through the openings 15, thereby forming pillar upper diffusion layers 16. Then, a silicon nitride film is deposited to a thickness of about 10nm by CVD and then etching back is carried out, thereby forming sidewall films 18 over the inner walls of the openings 15. In the formation of the sidewall films 18, the insulating films 17 formed on the upper surfaces of the silicon pillars 5 are removed to expose the upper surfaces of the silicon pillars. In this event, the insulating films 17 remain under the sidewall films 18 and on the exposed surfaces of the gate electrodes 11a in the openings 15. The sidewall films 18 serve to ensure insulation between the gate electrodes 11a and silicon plugs which will be formed subsequently.

Then, using a selective epitaxial growth method, silicon plugs 19 are grown on the upper surfaces of the silicon pillars 5 so as to fill the openings 15. Thereafter, in the case of an n-type transistor, impurities such as arsenic are implanted to make the silicon plugs 19 serve as an n-type conductor, thereby allowing the silicon plugs 19 to electrically contact the pillar upper diffusion layers 16 formed at the upper end portions of the silicon pillars 5.

Then, as shown in Figs. 18 to 20, a second interlayer insulating film 20 in the form of a silicon oxide film is deposited by CVD so as to bury the opening 14. Then, a stopper film 21 in the form of a silicon nitride film is deposited to a thickness of 20nm by CVD. Then, a third interlayer insulating film 24 in the form of a silicon oxide film is deposited to a thickness of 150nm by CVD.

Then, contact holes 27, 28, and 29 are formed by photolithography and dry etching. As shown in Fig. 18, the contact hole 29 has a circular shape in plan view having its center at an intersection between a center line in the

Y-direction passing through the centers of the first and fifth silicon pillars $5A_1$ and $5A_5$ and a center line in the X-direction passing through the center of the third silicon pillar $5A_3$. Herein, the diameter of the contact hole 29 is set to 40nm. Therefore, the closest interval between the outer periphery of the contact hole 29 and each of the first silicon pillar $5A_1$, the third silicon pillar $5A_3$, and the fifth silicon pillar $5A_5$ is 35nm, which is the minimum interval. In the formation of the contact hole 27, dry etching is once stopped by the stopper film 21 to thereby control the depth to the gate electrode 11 while an upper surface of the dummy pillar 6 is not etched because it is protected by the remaining mask film 4. Since the contact hole 27 is formed at a position offset from the center of the second dummy pillar 6B, the mask film 4 formed above the second dummy pillar 6B and the power feed gate electrode 11b formed on the side surfaces of the second dummy pillar 6B are partially exposed at the bottom of the contact hole 27. The silicon plug 19 is exposed at least partially at the bottom of each contact hole 28 while the pillar lower diffusion layer 9 is partially exposed at the bottom of the contact hole 29. These contact holes 27 to 29 may be formed simultaneously or separately.

Then, a metal film made of tungsten (W), titanium nitride (TiN), and titanium (Ti) is deposited by CVD to cover the third interlayer insulating film 24, thereby burying the contact holes 27 to 29. Then, the metal film on the third interlayer insulating film 24 is removed by CMP, thereby forming metal contact plugs 30 for the silicon plugs 19, a metal contact plug 31 for the pillar lower diffusion layer 9, and a metal contact plug 41 for the power feed gate electrode 11b.

As described before, the diameter of the metal contact plug 31 formed in the contact hole 29 having the diameter of 40nm becomes 40nm. Therefore, as shown in Fig. 18, the closest interval between the outer periphery of the metal contact plug 31 and each of the first silicon pillar $5A_1$, the third silicon

pillar 5A₃, and the fifth silicon pillar 5A₅ is 35nm, which is the minimum interval. On the other hand, the second silicon pillar 5A₂ and the fourth silicon pillar 5A₄ are each located in a direction inclined by 45 degrees from the X-direction with respect to the metal contact plug 31. Therefore, one corner of the rectangular

5 shape of each of the second silicon pillar 5A₂ and the fourth silicon pillar 5A₄ is closest to the outer periphery of the metal contact plug 31. In this case, the closest interval therebetween is 57nm. Herein, the interval between the outer periphery of the metal contact plug 31 and each of the first silicon pillar 5A₁, the third silicon pillar 5A₃, and the fifth silicon pillar 5A₅, the center of which is

10 located on the same center line in the X- or Y-direction as the center of the metal contact plug 31, is 35nm, which is the minimum interval. On the other hand, the interval between the outer periphery of the metal contact plug 31 and each of the second silicon pillar 5A₂ and the fourth silicon pillar 5A₄, each located in the direction inclined by 45 degrees from the center line in the

15 X-direction with respect to the metal contact plug 31, is 57nm, which is the maximum interval. In this case, since the maximum interval (57nm) is twice or less the minimum interval (35nm), it is possible to avoid the prior art problem that the intervals between the metal contact plug 31 and the respective silicon pillars become non-uniform so that parasitic resistances of the lower diffusion

20 layer 9 from the metal contact plug 31 to the respective silicon pillars differ from each other, resulting in unstable characteristics of the entire semiconductor device. If each silicon pillar has a circular shape in plan view having a diameter of 50nm, the maximum interval becomes 67nm. Accordingly, even in this case, the maximum interval (67nm) is twice or less the minimum interval

25 (35nm) so that it is possible to avoid the above-mentioned problem.

Then, as shown in Fig. 1, metal interconnections 33 and 34 and a gate-lift interconnection 42 made of tungsten (W) and tungsten nitride (WN) are formed by sputtering. In this event, the metal contact plug 41 is connected to

the gate-lift interconnection 42. Further, the single metal contact plug 31A connected to the pillar lower diffusion layer 9 is connected to the metal interconnection 34. Further, the five metal contact plugs 30 connected to the pillar upper diffusion layers 16 formed in the five silicon pillars 5 are connected
5 to the metal interconnection 33.

The above is the description of the semiconductor device manufacturing method.

According to the semiconductor devices of the first to fifth embodiments described above, the silicon pillars 5 are uniformly arranged around or near the
10 metal contact plug 31 in plan view. With this configuration, the maximum interval between the metal contact plug 31 and the silicon pillar 5 is twice or less the minimum interval between the metal contact plug 31 and the silicon pillar 5 so that variation in electrical resistance between the metal contact plug 31 and the respective silicon pillars 5 can be set within an allowable value range.
15 Further, it is possible to prevent degradation of characteristics of the vertical transistors and thus to stabilize the operation of the semiconductor device.

Although the inventions has been described above in connection with several preferred embodiments thereof, it will be appreciated by those skilled in the art that those embodiments are provided solely for illustrating the invention,
20 and should not be relied upon to construe the appended claims in a limiting sense.

CLAIMS

1. A semiconductor device comprising:

a plurality of semiconductor pillars provided to stand from a semiconductor

5 substrate,

each of the semiconductor pillars comprising a channel region;

a gate insulating film and a gate electrode provided over a side surface of each

of the

semiconductor pillars;

10 an upper diffusion layer provided at an upper end of each of the semiconductor

pillars to

serve as one of a source and a drain;

a lower diffusion layer operatively coupled to a lower end of each of the

semiconductor

15 pillars to serve as the other of the source and the drain; and

a lower diffusion layer side contact plug connected to the lower diffusion layer,

wherein

the semiconductor pillars share the lower diffusion layer and the lower diffusion
layer side contact plug, and

20 the semiconductor pillars are uniformly arranged near the lower diffusion layer

side contact plug.

2. The semiconductor device according to claim 1, wherein the gate insulating

film and

25 the gate electrode are provided to surround the side surface of each of the

semiconductor pillars.

3. The semiconductor device according to claim 1, wherein the semiconductor

pillars are

30 uniformly arranged on at least two opposite sides of the lower diffusion layer side

contact plug.

4. The semiconductor device according to claim 1, wherein the semiconductor
pillars are uniformly arranged so as to surround the lower diffusion layer side contact
35 plug.

ABSTRACT

A semiconductor device 100 includes a plurality of vertical transistors 50 provided to stand from a silicon substrate 1 and having a pillar lower diffusion layer 9 at their end portions on the silicon substrate 1 side, a metal contact plug 31 provided to stand from the silicon substrate 1 and connected to the pillar lower diffusion layer 9 of the plurality of vertical transistors 50, the plurality of vertical transistors 50 are uniformly arranged around the metal contact plug 31 and share the pillar lower diffusion layer 9 and the metal contact plug 31.

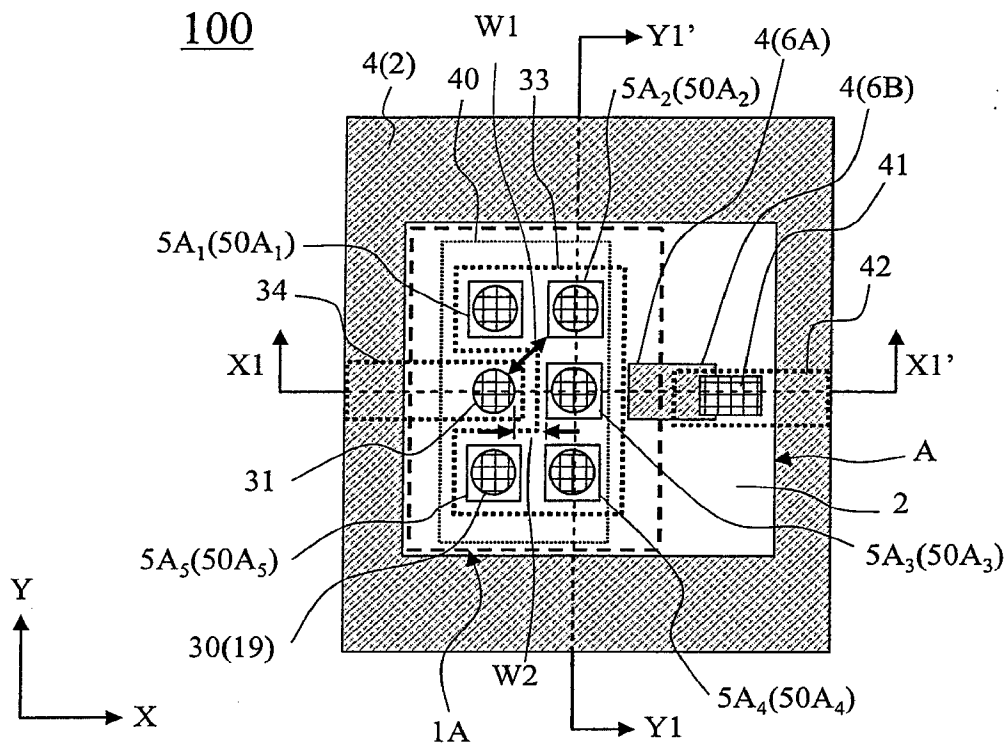


FIG. 1

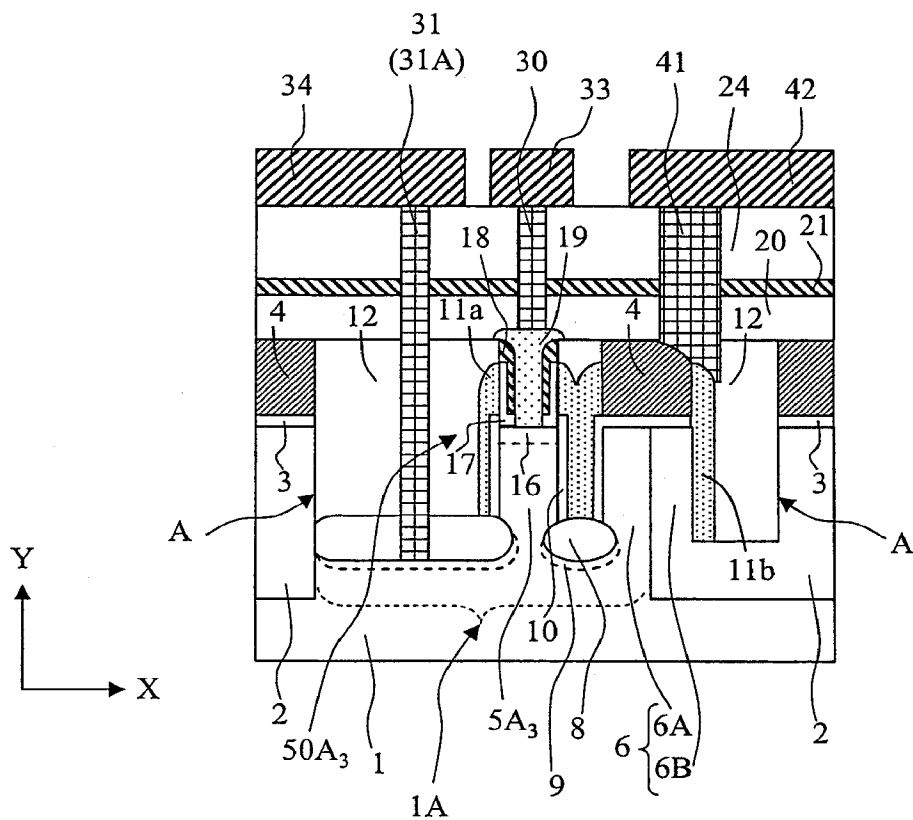


FIG. 2

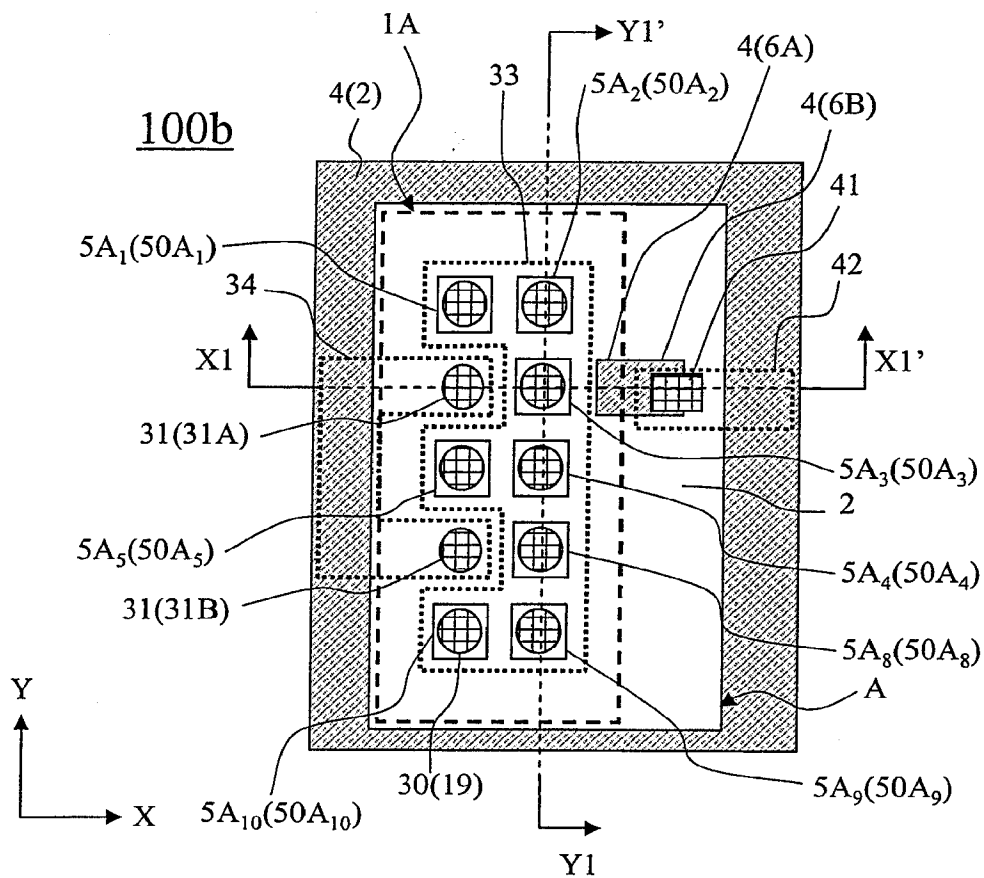


FIG. 5

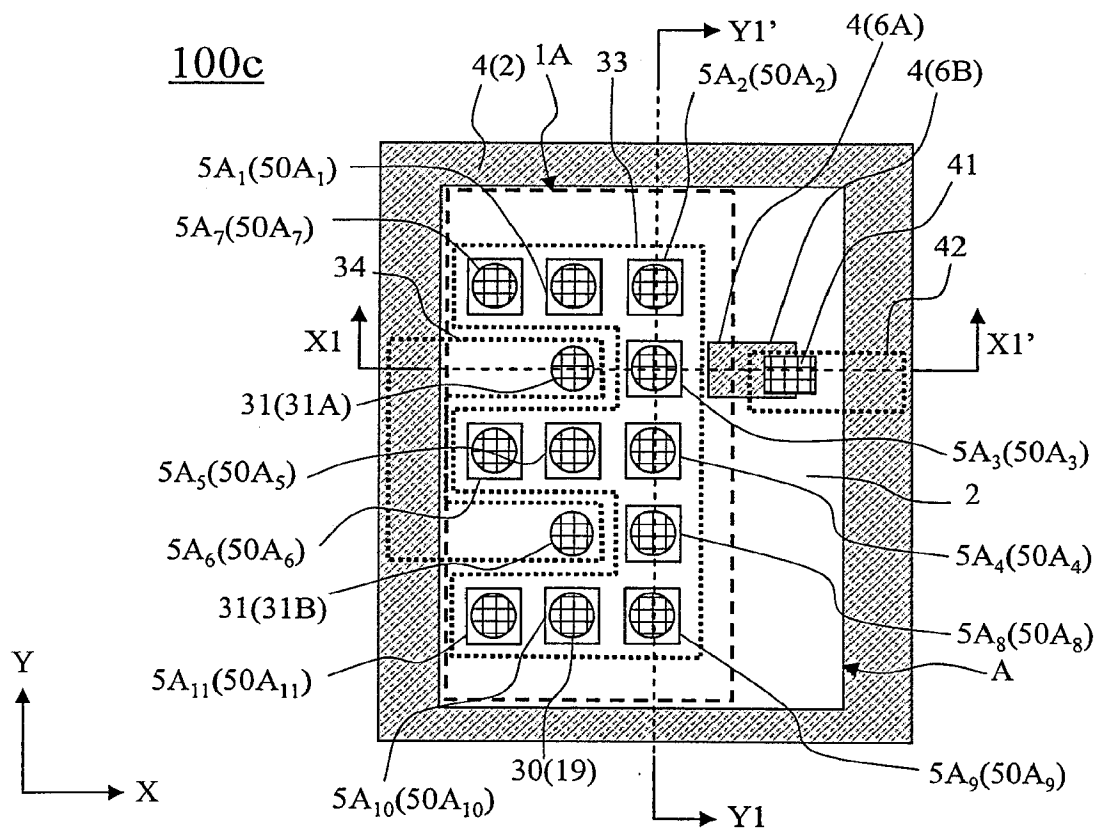


FIG. 6

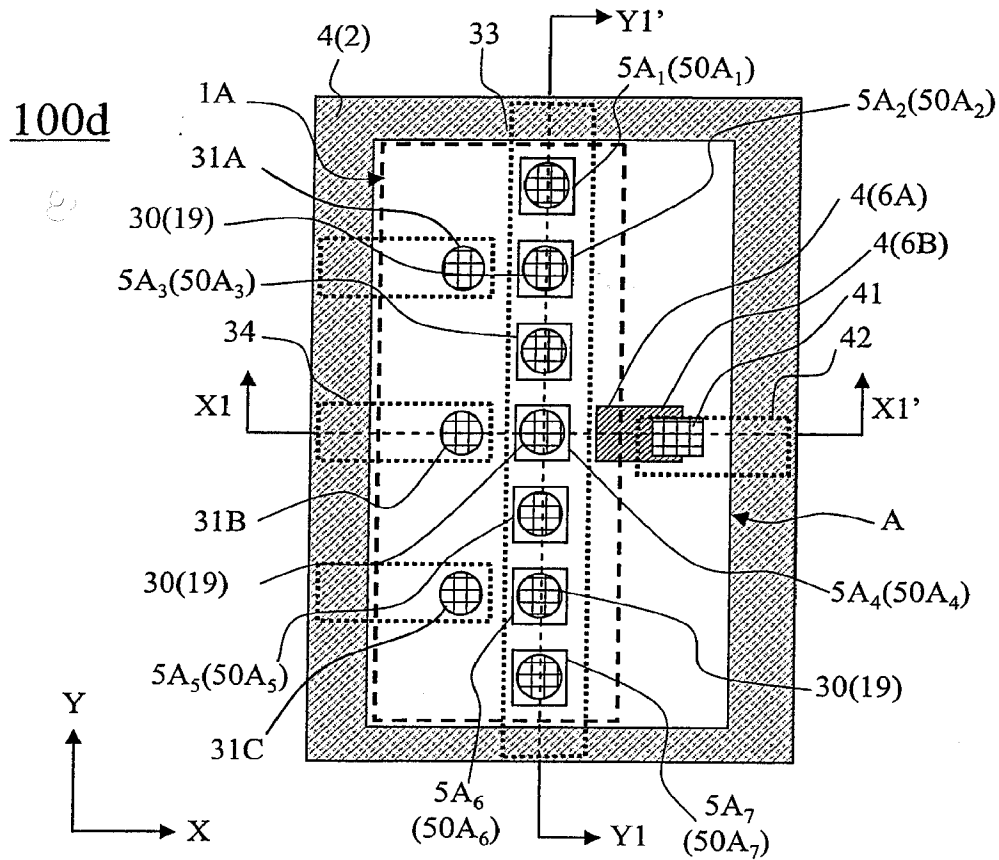


FIG. 7

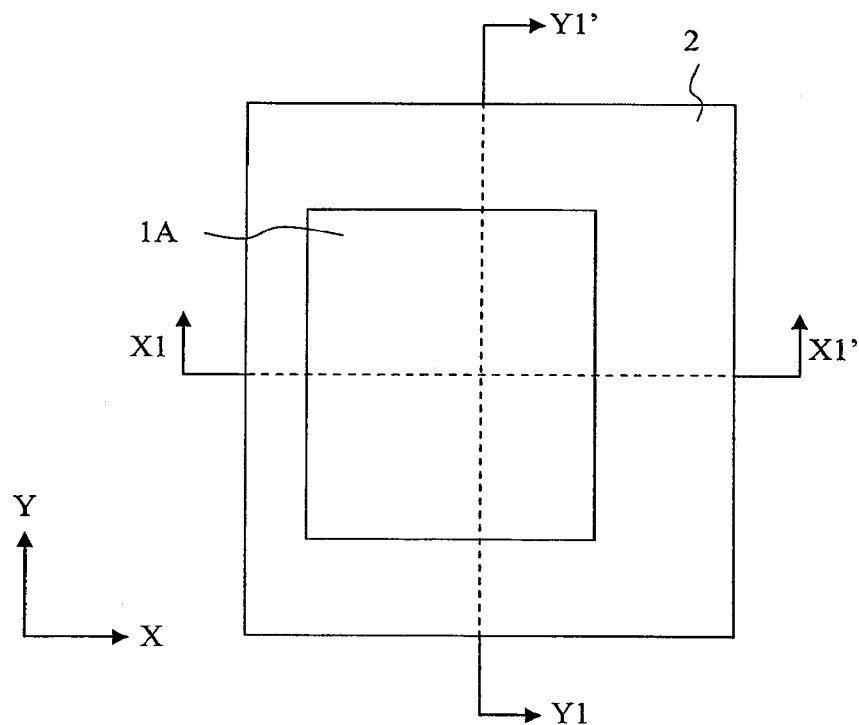


FIG. 8

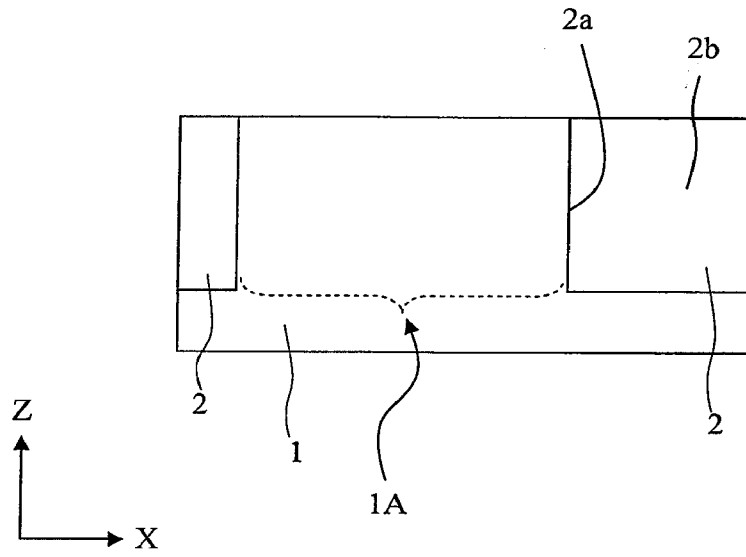


FIG. 9

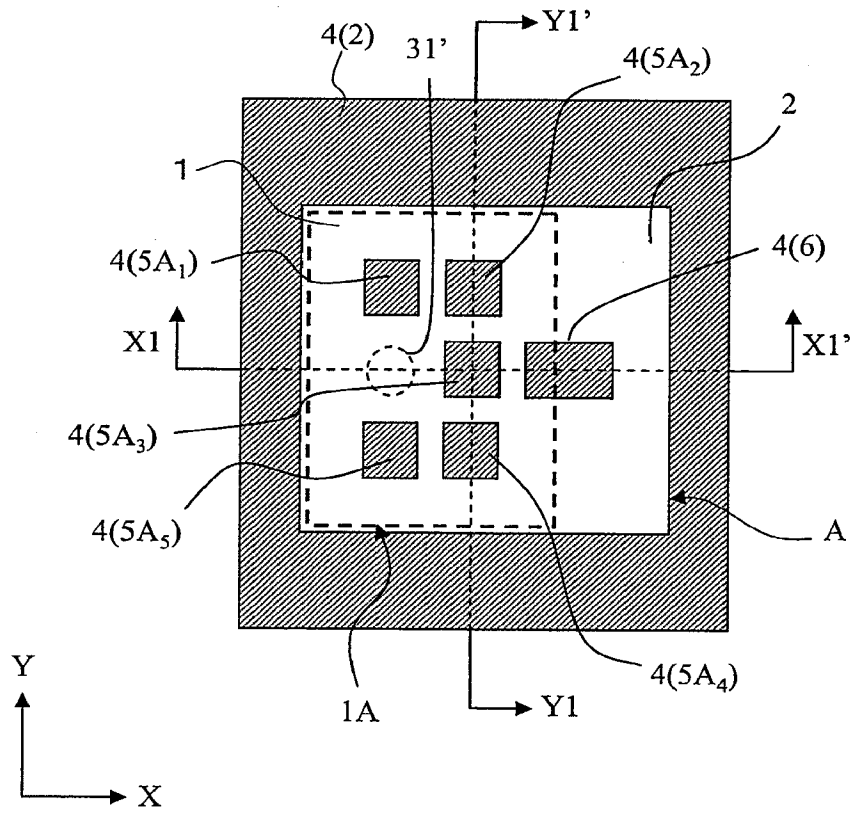


FIG. 10

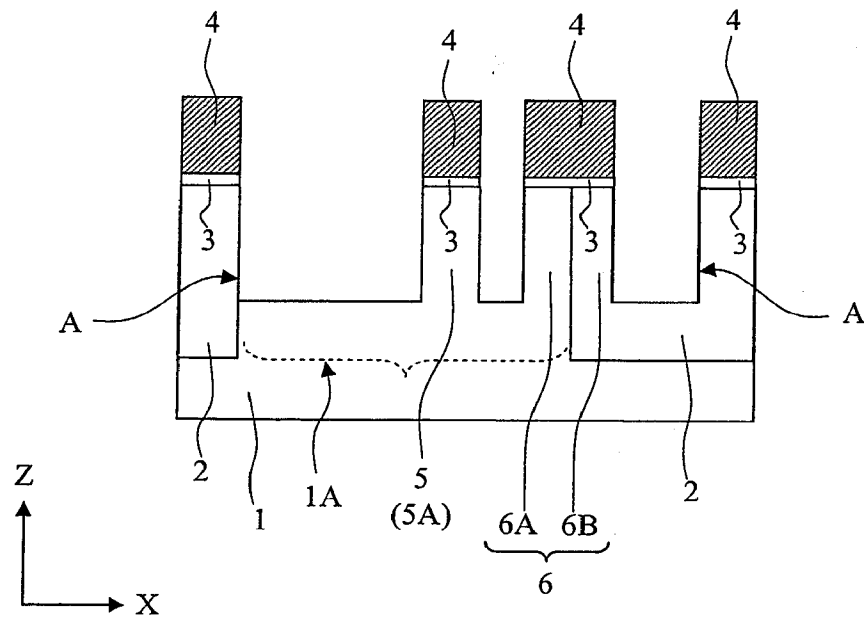


FIG. 11

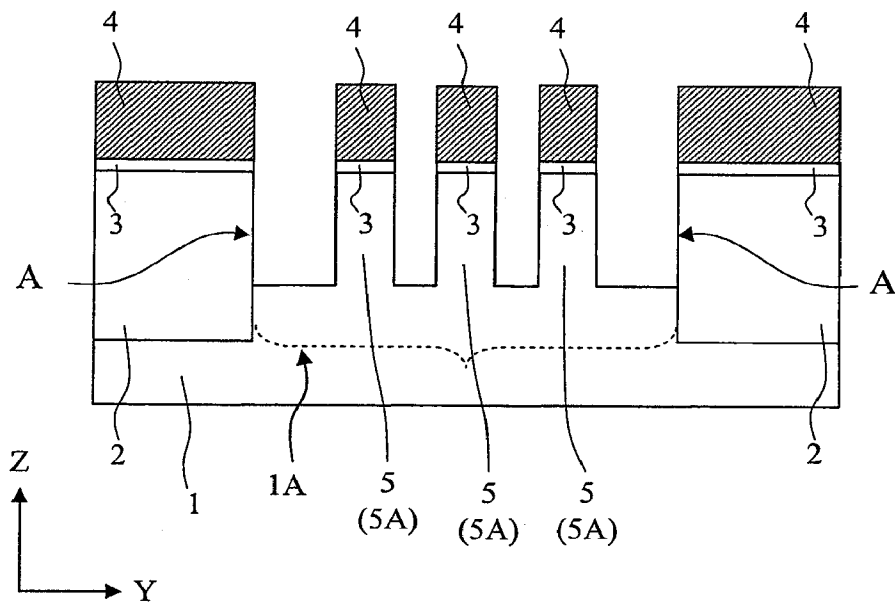


FIG. 12



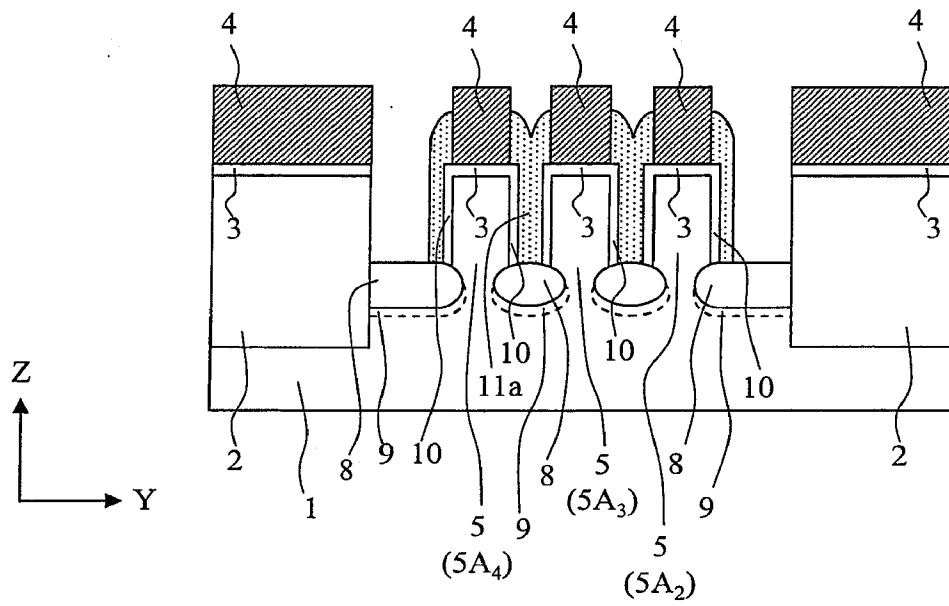


FIG. 15

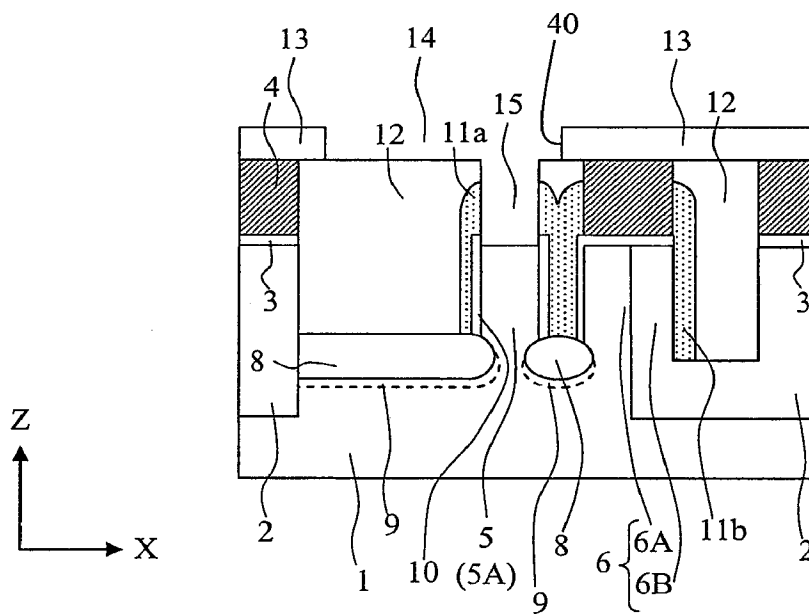


FIG. 16

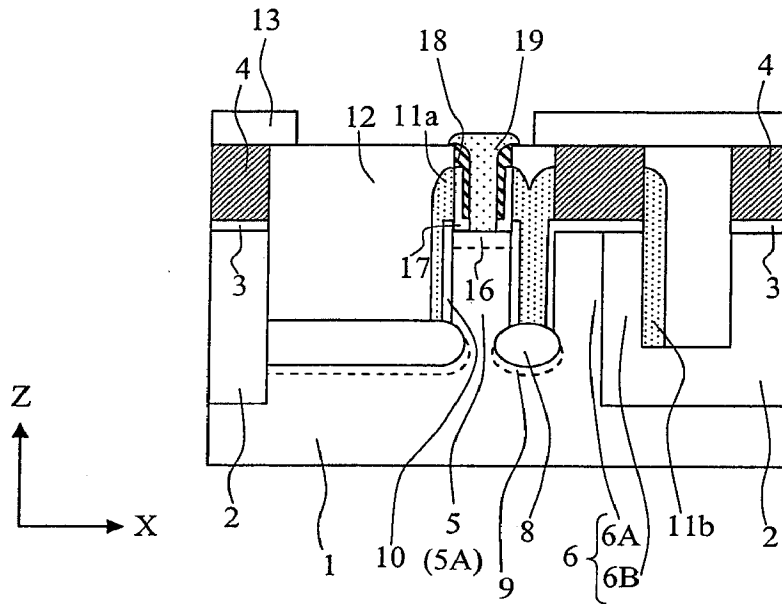


FIG. 17

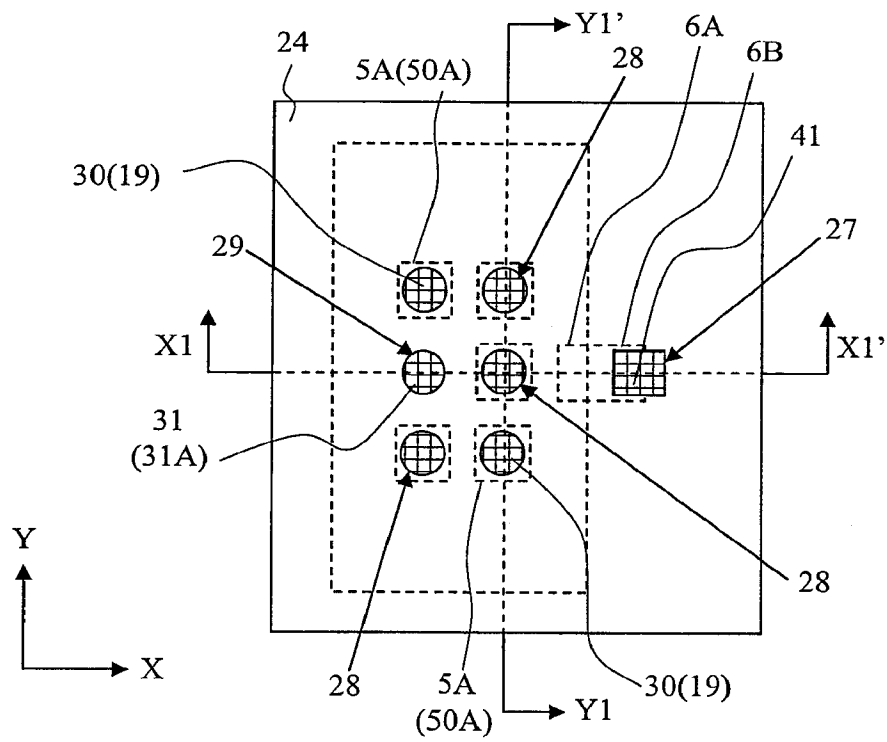


FIG. 18

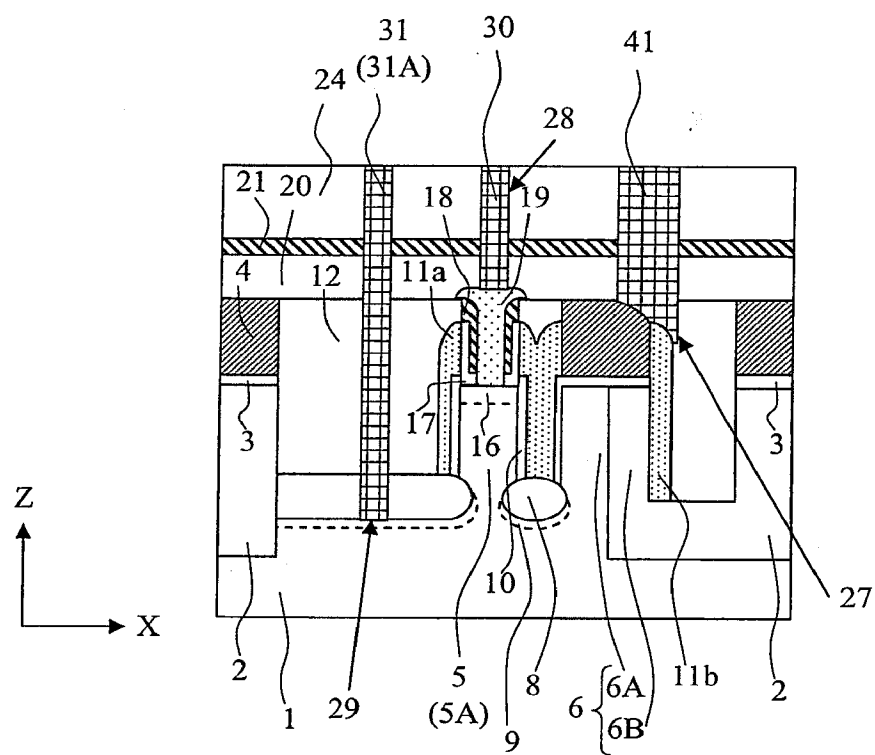


FIG. 19

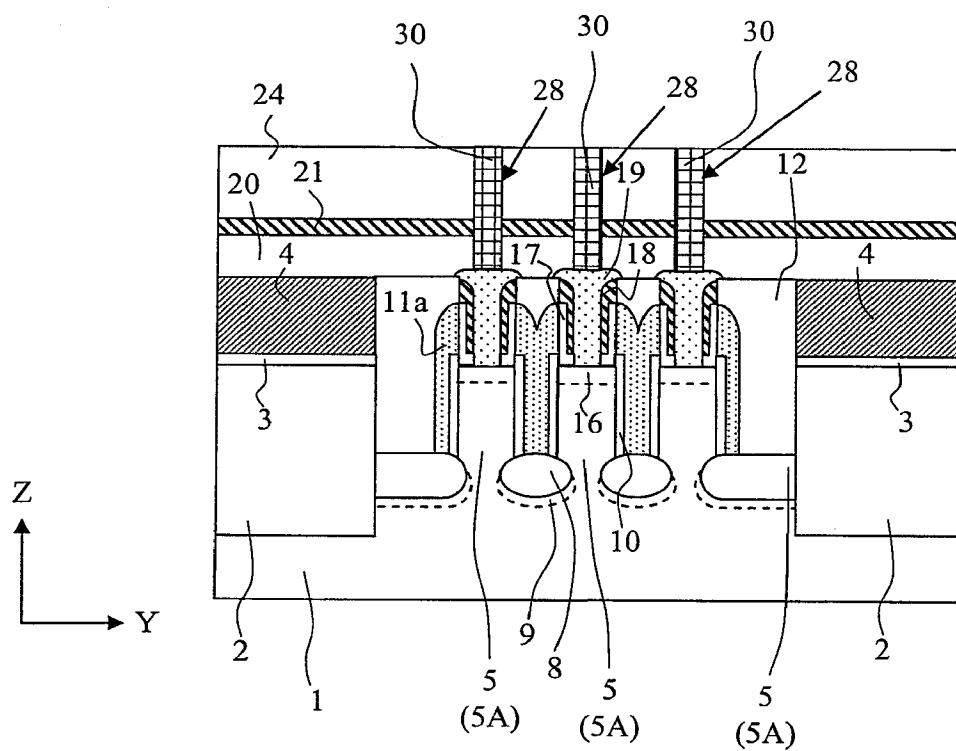


FIG. 20

ASSIGNMENT AND INVENTOR'S DECLARATION

WHEREAS I/we, the undersigned inventor(s), hereafter also referred to as "assignor(s)", have invented certain new and useful improvements described in the application identified below; and

WHEREAS, Elpida Memory, Inc., hereinafter referred to as "assignee(s)", whose address is 2-1, Yaesu 2-chome, Chuo-ku, Tokyo, Japan, is desirous of acquiring the entire right, title and interest in and to the application and invention, and to any United States patents to be obtained therefor;

NOW, THEREFORE, for valuable consideration, the receipt and sufficiency of which is hereby acknowledged, I/we, the above-named assignor(s), hereby sell, assign and transfer to the above named assignee(s), its successors and assigns, the entire right, title and interest in the application and the invention disclosed therein for the United States of America, including all divisions, and continuations thereof, and all Letters Patent of the United States that may be granted thereon, and all reissues thereof, including any right to bring or maintain an action for infringement under the provisional rights granted pursuant to Title 35, Section 154 of the United States Code or any other cause of action for acts which would constitute infringement occurring prior to this assignment, and including the right to claim priority under the International Convention of Paris (1883), as amended, of or in any corresponding foreign patent application, and I/we request the Director of the U.S. Patent and Trademark Office to issue any Letters Patent granted upon the invention set forth in the application to the assignee(s), its successors and assigns.

As a below named inventor, I hereby declare that:

This assignment and declaration ☒ The attached application, or
is directed to:

☐ United States Application or PCT International Application Number _____
filed on _____ (Confirmation No. _____).

The application is entitled: SEMICONDUCTOR DEVICE

The above-identified application was made or was authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this assignment with declaration is punishable under 18 USC 1001 by fine or imprisonment of not more than five (5) years, or both.

Given Name(s)	Yoshihiro	Family Name/Surname	TAKAISHI
Inventor's signature	<i>Yoshihiro Takaishi</i>		Date December 10, 2012
Given Name(s)	Family Name/Surname		
Inventor's signature			Date
Given Name(s)	Family Name/Surname		
Inventor's signature			Date
Given Name(s)	Family Name/Surname		
Inventor's signature			Date

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: PS4 Luxco S.a.r.l.Application No./Patent No.: _____ Filed/Issue Date: October 1, 2015Titled: SEMICONDUCTOR DEVICEPS4 Luxco S.a.r.l., a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Yoshihiro TAKAISHI To: Elpida Memory, Inc.The document was recorded in the United States Patent and Trademark Office at
Reel 029515, Frame 0618, or for which a copy thereof is attached.2. From: Elpida Memory, Inc. To: PS4 Luxco S.a.r.l.The document was recorded in the United States Patent and Trademark Office at
Reel 032901, Frame 0196, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Western Digital Exhibit 1002

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
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6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Joseph J. Hawkins/

Signature

Joseph J. Hawkins

Printed or Typed Name

October 1, 2015

Date

63,194

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

In re application of:

Yoshihiro TAKAISHI

Application No.

Filed: October 1, 2015

For: **SEMICONDUCTOR DEVICE**

Group Art Unit:

Examiner:

Confirmation No.

Docket No. 74735/258

TRANSMITTAL LETTER

I hereby certify that the following papers are being submitted for the above-referenced application ("Application") to the United States Patent and Trademark Office via EFS-Web electronic filing system on October 1, 2015.

1. An Application Data Sheet;
2. A Continuation Patent Application;
3. Drawings;
4. A Declaration;
5. A Statement Under 37 CFR 3.73(c);
6. An Information Disclosure Statement; and
7. A Preliminary Amendment.

The Commissioner is authorized to charge any additional fees required in connection with the filing of these papers, or credit overpayment, to **Deposit Account No. 502375**.

Signature: **Joseph J. Hawkins/**

Joseph J. Hawkins
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(801) 578-6971
Registration No. 63,194
Dated October 1, 2015

STOEL RIVES LLP
201 S Main Street, Suite 1100
Salt Lake City, UT 84111-4904
Telephone: (801) 328-3131
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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: October 1, 2015

Electronic Signature for Joseph J. Hawkins: /Joseph J. Hawkins/

Docket No.: 74735/258
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Yoshihiro TAKAISHI

Application No.:

Confirmation No.:

Filed: October 1, 2015

Art Unit:

Title: SEMICONDUCTOR DEVICE

Examiner:

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

Pursuant to MPEP 609.02, Applicant(s) expect the Examiner to consider all the references submitted, cited, or otherwise considered during the prosecution of all the ancestor applications listed on the application data sheet of the present application. The Applicant(s) do not plan to resubmit a listing of those references unless the Examiner explicitly requests.

Dated: October 1, 2015

Respectfully submitted,

Electronic signature: /Joseph J. Hawkins/

Joseph J. Hawkins

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/872,844	Filing Date 10/01/2015	☒ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	10/01/2015	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 4	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
						TOTAL ADD'L FEE

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SLIE
/NICHELE PETERSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.