

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,

Petitioner

v.

LONGITUDE LICENSING LTD.,

Patent Owner

U.S. Patent No. 9,379,233

DECLARATION OF JACK C. LEE, PH.D.
UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PETITION
FOR INTER PARTES REVIEW

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	QUALIFICATIONS	2
III.	LEVEL OF ORDINARY SKILL IN THE ART	5
IV.	RELEVANT LEGAL STANDARDS	6
	A. Anticipation	7
	B. Obviousness	7
V.	THE '233 PATENT	8
	A. Summary of the '233 patent	8
	B. Prosecution History	11
	1. Prosecution History of '125 App	11
	2. Prosecution History of '844 App	14
VI.	CLAIM CONSTRUCTION	17
VII.	FOUNDATIONS	17
	A. Ground 1: Claims 1-3 are unpatentable under §103(a) over Endoh in view of Hwang	17
	1. Summary of Endoh	17
	2. Summary of Hwang	21
	3. Reasons to Combine Endoh and Hwang.....	25
	4. Claim 1	31
	5. Claim 2	57
	6. Claim 3	61
	B. Ground 2: Claims 1-4 are Rendered Obvious under 35 U.S.C. § 103(a) over Takaishi.	64
	1. Summary of Takaishi	64
	2. Claim 1	69
	3. Claim 2	96
	4. Claim 3	102

5. Claim 4.....	104
VIII. DECLARATION.....	107

I. INTRODUCTION

1. I, Jack C. Lee, have been retained by counsel for Western Digital Technologies, Inc., (“Western Digital” or “Petitioner”) as a technical expert in connection with the proceeding identified above. I submit this declaration in support of Western Digital’s Petition for *Inter Partes* Review of U.S. Patent No. 9,379,233 (“the ’233 patent”).

2. Compensation for my work in this matter is based on an hourly rate. In addition, reasonable and customary expenses associated with my work and testimony in this matter are reimbursed. This compensation is not contingent on the outcome of this matter, nor is it contingent on the specifics of my testimony. I have no personal or financial stake, nor any interest in the outcome of the present proceeding.

3. In the preparation of this declaration, I have studied:

- (1) The ’233 patent, EX1001;
- (2) The prosecution file history of the ’233 patent (’844 App),
EX1002;
- (3) The ’056 patent (parent of the ’233 patent), EX1005;
- (4) The prosecution file history of the ’056 patent (’125 App),
EX1006;
- (5) US App. Pub. No. 2009/0,085,102 to Takaishi (“Takaishi”),

EX1007;

(6) Japanese App. Pub. No. 1992079369 to Endoh, English translation, translation certification, and Japanese publication (“Endoh”), EX1008;

(7) US Patent No 8,492,797 to Hwang, et al. (“Hwang”), EX1009.

4. In forming the opinions expressed below, I have considered:

(1) The documents listed above;

(2) Any additional documents discussed below; and

(3) My own knowledge and experience based upon my work in the fields of semiconductor technology as described below.

II. QUALIFICATIONS

5. My qualifications for forming the opinions set forth in this Declaration are summarized here and explained in more detail in my curriculum vitae, which is attached as EX1004.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on

bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised over 40 students who received their doctoral degrees under my guidance. I am currently the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering at UT Austin.

10. My current research and teaching interests include semiconductor devices, fabrication processes, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, semiconductor memory applications, and alternative channel materials. My research has been partially supported by grants from the

National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

11. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., best paper awards.

12. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

13. I have served in various technology consulting and business advisor roles. For example, I have been teaching short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. LEVEL OF ORDINARY SKILL IN THE ART

14. I understand that the level of ordinary skill may be reflected by the prior art of record, and that a Person of Ordinary Skill in The Art (“POSITA”) to which the claimed subject matter pertains would have the capability of understanding the scientific and engineering principles applicable to the pertinent art. I understand that a POSITA has ordinary creativity, and is not an automaton.

15. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including (1) the levels of education and experience of persons working in the field at the time of the invention; (2) the sophistication of the technology; (3) the types of problems encountered in the field; and (4) the prior art solutions to those problems.

16. I have been informed by counsel that the earliest claimed priority date for the ’233 patent is December 27, 2011, although any given claim of the ’233 patent may or may not be entitled to the earliest claimed priority date. I am familiar with the semiconductor technology pertinent to the ’233 patent. I am also aware of the state of the art at the time of the earliest claimed priority date.

17. Based on the technologies disclosed in the ’233 patent, I believe that a POSITA would include someone who had, as of the claimed priority date of the ’233 patent, a bachelor’s or the equivalent degree in electrical engineering or a related field and 2-3 years of professional experience relating to semiconductor

device design and fabrication. In addition, I recognize that someone with less formal education but more experience, or more formal education but less experience could have also met the relevant standard for a POSITA. I believe that I am at least a POSITA and, furthermore, I have supervised students and engineers who were also POSITAs. Accordingly, I believe that I am qualified to opine from the perspective of a POSITA regarding the '233 patent.

18. For purposes of this Declaration, unless otherwise noted, my opinions and statements, such as those regarding the understanding of a POSITA (and specifically related to the references I consulted herein), reflect the knowledge that existed in the art before the earliest claimed priority date of the '233 patent.

IV. RELEVANT LEGAL STANDARDS

19. I have been asked to provide my opinions regarding whether claims 1-4 (the "Challenged Claims") of the '233 patent would have been obvious to a POSITA at the time of the alleged invention in light of the prior art.

20. I am not an attorney. In preparing and expressing my opinions and considering the subject matter of the '233 patent, I am relying on certain legal principles explained to me by counsel.

21. I understand that a claim is unpatentable if it is anticipated under 35 U.S.C. § 102 or obvious under 35 U.S.C. § 103.

A. Anticipation

22. I have been informed by counsel that a patent claim is unpatentable as anticipated if each element of that claim is present either explicitly or inherently in a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

B. Obviousness

23. I have been informed and I understand that a claimed invention is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a POSITA at the time the invention was made. I understand that the appropriate analysis for determining obviousness of a claimed invention takes into account factual inquiries, including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the claimed subject matter as a whole.

24. I have been informed and I understand that the United States Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include the following: (a) combining prior art elements according to known

methods to yield predictable results; (b) simple substitution of one known element for another to obtain predictable results; (c) use of a known technique to improve a similar device (method, or product) in the same way; (d) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (f) some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. I have also been informed and I understand that a demonstration of obviousness does not require a physical combination or bodily incorporation, but rather may be found based on consideration of what the combined teachings would have suggested to a POSITA at the time of the alleged invention.

V. THE '233 PATENT

A. Summary of the '233 patent

25. The '233 patent is directed to “a semiconductor device” that “includes a plurality of vertical transistors.” EX1001, '233 patent, Abstract.

26. In the Background section, the '233 patent acknowledges that vertical transistors were well-known in the art. Specifically, the '233 patent acknowledges that “vertical transistors have been proposed as a technique for transistor

miniaturization,” where the vertical transistor is “a transistor which uses as a channel a semiconductor pillar extending in a direction perpendicular to a main surface of a semiconductor substrate.” EX1001, ’233 patent, 1:15-19. The ’233 patent further acknowledges various known benefits of a vertical transistor compared to a conventional transistor having a channel parallel to the substrate plane, including “the area in the plane occupied by the vertical transistor is smaller,” and such transistor occupation area in the plane is not increased “even if the channel length (gate length) is increased.” EX1001, ’233 patent, 1:29-34.

27. According to the ’233 patent, the “effect of the invention” is that “it is possible to provide a semiconductor device which, even in a structure where a plurality of vertical transistors are connected to each other, can stabilize the characteristics of the transistors provided to individual semiconductor pillars.” EX1001, ’233 patent, 2:50-56.

28. The ’233 patent further describes that the “unit transistors are uniformly arranged around the metal contact 31,” and that “[i]n the first embodiment, ‘uniformly arranged’ represents an arrangement in which, in plan view, the distance between the metal contact plug 31 and a closest portion of the unit transistor farthest from the metal contact plug 31 is twice or less the distance between the metal contact plug 31 and a closest portion of the unit transistor closest to the metal contact plug 31.” EX1001, ’233 patent, 4:35-42.

29. Referring to embodiment of FIG. 1 below, the '233 patent states, "[i]n this case, since the maximum interval (57 nm) [e.g., between the metal contact plug 31 and the silicon pillar 5A₂] is twice or less the minimum interval (35 nm) [e.g., between the metal contact plug 31 and the silicon pillar 5A₃], it is possible to avoid the prior art problem that the intervals between the metal contact plug 31 and the respective silicon pillars become non-uniform so that parasitic resistances of the lower diffusion layer from the metal contact plug 31 to the respective silicon pillars different from each other, resulting in unstable characteristics of the entire semiconductor device." EX1001, '233 patent, 6:57-65.

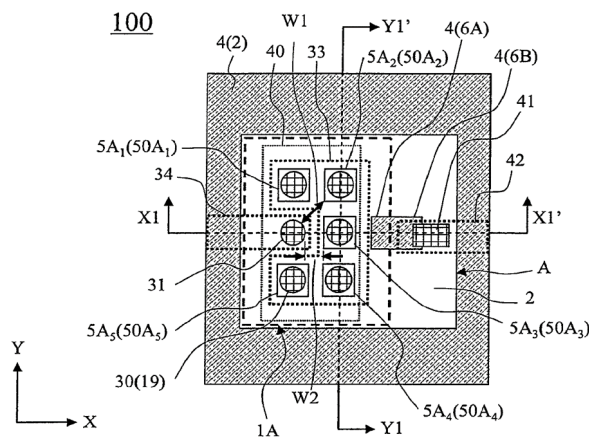


FIG. 1

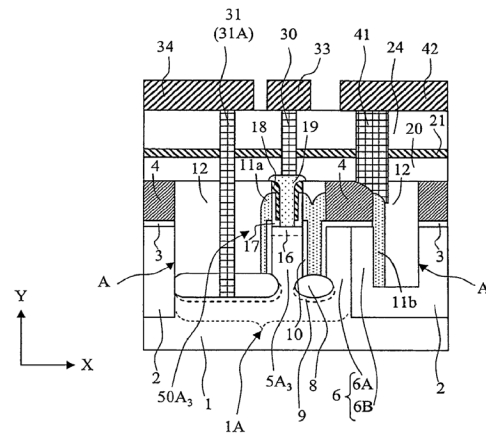


FIG. 2

'233 patent, FIGS. 1 and 2

30. Representative independent claim 1 of the '233 patent is reproduced below:

1. A semiconductor device comprising:

a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region;
a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars;
an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain;
a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain; and
a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein
the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug, and
the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.

EX1001, '233 patent, 17:6-18:6.

31. As I discuss below in more detail, the semiconductor device presented in the '233 patent was well known to persons of ordinary skill in the art before the earliest claimed priority date of the '233 patent.

B. Prosecution History

1. Prosecution History of '125 App

32. On December 20, 2012, Applicant filed U.S. Patent App. No. 13/722,125 ("125 App"), claiming the benefit of priority from Japanese Patent App. No. 2011-285544, filed on Dec. 27, 2011. EX1006, '125 App, 305.

33. On November 21, 2013, Examiner issued a non-final rejection, rejecting claims 1-20 under nonstatutory double patenting over copending Application No. 13/683,191, rejecting claims 5-7 under 112, and rejecting claims 1-20 under 103(a) over Cheng (U.S. Patent No. 7,528,035) in view of Matsuoka

(U.S. Patent No. 6,560,135) and/or Nojima (U.S. Patent No. 8,174,068).

Examiner explained that it would have been obvious to combine these references because it is “necessary to open a contact with passing through a portion between the writing word lines without electrically shorting with the writing word lines so as to connect plugs.” EX1006, ’125 App, 178-188.

34. On February 21, 2014, Applicant filed a response amending claims 9, 10, 15, and 18 to overcome the rejections.

35. On August 26, 2014, Examiner issued a non-final office action, objecting claims 9-17 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Examiner rejected claims 1-8 and 13-20 under 102(b) over U.S. Patent Application Publication 2009/0085102 (EX1007, “Takaishi”), acknowledging that Takaishi corresponded to “Japanese Patent Abstract 2009-081389.” EX1006, ’125 App, 133-142. Specifically, Examiner stated that Takashi teaches all limitations of claims 1-8 and 13-20, including for example,

- “wherein the plurality of vertical transistors are uniformly arranged near the conductive plug and share the diffusion layer and the conductive plug” of claim 1;
- “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug” of claim 2,

- “the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug” of claim 3,
- “in plan view, a distance between the lower diffusion layer side contact plug and the semiconductor pillar farthest from the lower diffusion layer side contact plug is twice or less a distance between the lower diffusion layer side contact plug and the semiconductor pillar closest to the lower diffusion layer side contact plug” of claim 4.

36. On November 25, 2014, Applicant filed a response to the Office Action, amending independent claims 1 and 18 with the subject matter of claim 9 indicated by Examiner as allowable: “a dummy pillar provided to stand from the semiconductor substrate and comprising, over a side surface of the dummy pillar, a power feed gate electrode connected to the gate electrodes of the plurality of vertical transistors.” EX1006, ’125 app, 119-124.

37. In the response, Applicant did **not** dispute that Takaishi teaches claims 1-8 and 13-20 before amendment. Instead, Applicant only relied on the feature of the dummy pillar to distinguish from Takaishi, stating that Takaishi “does not anticipate, or even suggest, a semiconductor device as recited by claims 1 and 18 as amended to include this feature [of a dummy pillar].” EX1006, ’125 app, 127-128.

38. On January 29, 2015, Examiner issued a final rejection, indicating that

claims 1-9, 10-14, and 18-20 were allowed, and claims 15-17 were rejected on the ground of nonstatutory double patenting over claims 1 and 2 of copending Application No. 12/212,364. EX1006, '125 app, 109-114.

39. On June 12, 2015, Applicant filed a response after final, including an examiner interview summary stating that Examiner indicated that the provisional rejections based on nonstatutory double patenting are moot because the Application No. 12/212,364 is abandoned. EX1006, '125 app, 35.

40. On July 2, 2015, Notice of Allowance was issued. Examiner indicated that because copending Application was abandoned, terminal disclaimer is not required.

41. On November 3, 2015, the '125 App issued as U.S. Patent No. 9,178,056 ("'056 parent patent", EX1005). As shown in Exhibit 1010, the allowed claims of the '056 parent patent are substantially similar to the claim limitations of the '233 patent, but the claims of the '233 patent do not include the "dummy pillar" feature of the '056 parent patent that Applicant used to overcome Takaishi. Exhibit 1010, Comparison of '233 Patent Claims and Parent Claims Rejected Over Takaishi.

2. Prosecution History of '844 App

42. On October 1, 2015, the Applicant filed U.S. Patent Application No. 14/872,844 ("the '844 App"), which ultimately issued as the '233 patent. The '844

App is a continuation of U.S. Patent App. No. 13/722,125 filed on Dec. 20, 2012, which claims the benefit of priority from Japanese Patent App. No. 2011-285544, filed on Dec. 27, 2011.

43. Examiner issued a notice of allowance March 3, 2016, without any office action. EX1002, '844 App, 17-23. Examiner first indicated that “[t]he information disclosure statement filed October 1, 2015 has been misplaced by the Office. Please resubmit.” EX1002, '844 App, 22. In the notice of allowance, Examiner indicated that claims 1-4 were allowed, and provided a statement of reasons for allowance stating that “the prior art does not anticipate nor render obviousness with respect to a semiconductor device comprising amongst other limitations: a plurality of semiconductor pillars provided on a semiconductor substrate each having a[n] upper diffusion layer and a lower diffusion layer with a side contact plug connected to the lower diffusion layer.” EX1002, '844 App, 23.

44. Examiner’s statement of reasons for allowance contradicts the prosecution history of the parent application, where Examiner relied on Takaishi to disclose the limitations of the '056 parent patent including “each vertical transistor [of a plurality of vertical transistors] comprises: a semiconductor pillar provided to stand from the semiconductor substrate and forming a channel; ... an upper an upper diffusion layer provided at an upper end of the semiconductor pillar and serving as one of a source and a drain; and a lower diffusion layer provided at a

lower end of the semiconductor pillar and serving as the other of the source and the drain, the conductive plug is a lower diffusion layer side contact plug connected to the lower diffusion layer.” EX1006, ’125 App, 133-142; EX1005, ’056 parent patent, claims 1 and 2; EX1010. Such contradiction with the prosecution history of the parent is an error by the Examiner that is material to the patentability of the ’233 claims.

45. On March 17, 2016, a corrected notice of allowability was issued, together with an IDS with a filing date of “2012-12-19,” considered by Examiner Coleman on March 14, 2016, and an interview summary indicating that prior art in IDS dated 10/01/2015 was discussed, and “Applicant’s representative indicated that pursuant to MPEP 609.02, Applicant(s) expected the Examiner to consider all the references submitted in parent application 13/722,125.” EX1002, ’844 App, 16.

46. The ’233 patent issued on June 28, 2016. As shown in Exhibit 1010, the allowed claims of the ’233 patent are substantially similar to the claims of the parent rejected by Examiner over Takaishi, and the claims of the ’233 patent do not include the “dummy pillar” feature of the ’056 parent patent that Applicant used to overcome Takaishi. Exhibit 1010, Comparison of ’233 Patent Claims and Parent Claims Rejected Over Takaishi.

VI. CLAIM CONSTRUCTION

47. It is my understanding that in order to properly evaluate the '233 patent, the terms of the claims must first be interpreted. It is my understanding that for the purposes of this inter partes review, the claims are to be construed under the so-called Phillips standard, under which claim terms are given their ordinary and customary meaning as would have been understood by one of ordinary skill in the art in light of the specification and prosecution history, unless the inventor has set forth a special meaning for a term. I have also been informed that claim terms only need to be construed to the extent necessary to resolve the obviousness inquiry.

48. I have reviewed the entirety of the '233 patent, as well as its prosecution history. It is my opinion that for purposes of applying the prior art presented herein to evaluate the patentability of the claims no term requires express construction. Accordingly, I have analyzed the claims consistent with their ordinary and customary meaning as would have been understood by a POSITA.

VII. GROUNDS

A. Ground 1: Claims 1-3 are unpatentable under §103(a) over Endoh in view of Hwang

49. In my opinion, Endoh in view of Hwang renders claims 1-3 obvious.

1. Summary of Endoh

50. Endoh is titled “Non-volatile Semiconductor Memory,” and its field of invention is about “non-volatile electrically erasable semiconductor memory

using memory transistor with charge accumulation layer and control gate

(EEPROM).” EX1008, Endoh, Title; Field of the Invention.

51. Specifically, Endoh identifies the problems to be solved is that “it is impossible to ensure an enough capacitance between floating gate and control gate while reducing the occupied area of memory cell,” and it “aims to provide an EEPROM of resolving this kind of problem, with large capacitance and high efficiency of writing and erasure.” EX1008, Endoh, 3 (Problems to be Solved by the Invention).

52. Endoh solves the identified problems by providing “a memory transistor formed by the side wall of **multiple pillar-shaped semiconductor layers in matrix arrangement**, separating by the plaid-shaped groove on the semiconductor substrate. That is to say, the memory transistor is composed of **drain diffused layer formed on the various pillar-shaped semiconductor layer, common source diffused layer formed at the bottom of the aforementioned groove** and charge accumulation layer and control gate surrounding at least a part of various pillar-shaped semiconductor layer around, for the multiple pillar-shaped semiconductor layer in the same direction, continuously setting control gate lines formed from gate electrodes, respectively. In addition, it also sets the bit line connecting to the drain diffused layer of multiple memory transistors in the cross direction with control gate line.” EX1008, Endoh, 3 (Means for Solving

Problems).

53. Endoh teaches multiple embodiments of semiconductor devices, including for example:

- Embodiment of FIGS. 1, 2(a), 2(b), and 3 (referred to as “Embodiment 1”);
- Embodiment of FIGS. 6, 7(a), 7(b), 8, and 9 (referred to as “Embodiment 2”).
- Embodiment of FIG. 4 (referred to as “Embodiment 3”);
- Embodiment of FIG. 5 (referred to as “Embodiment 4”);
- Embodiment of FIG. 10 (referred to as “Embodiment 5”);
- Embodiment of FIG. 11 (referred to as “Embodiment 6”);
- Embodiment of FIG. 12, 13(a), 13(b), 14, 15 (referred to as “Embodiment 7”).

54. While the analysis below primarily uses Embodiments 1 and 2 of Endoh as examples, the analysis applies to each of the Embodiments 1-7 of Endoh with similar features, unless noted otherwise. *See e.g.*, EX1008, Endoh, 5 (“In these figures, when using the same symbols with the corresponding part in the previous embodiments, the detailed description is omitted.”).

55. Regarding Embodiment 1 of Endoh, as shown in FIGS. 1, 2(a), and 2(b) of Endoh below, Endoh teaches a EEPROM memory cell, which includes a P-

type silicon substrate and pillar-shaped P-type silicon layer 2, where the “common source diffused layer 9 of memory cell is formed at the bottom of groove 3” of the P-type silicon substrate, and “drain diffusion layer 10 of various memory cells is formed on various pillar-shaped silicon layer 2.” EX1008, Endoh, 3.

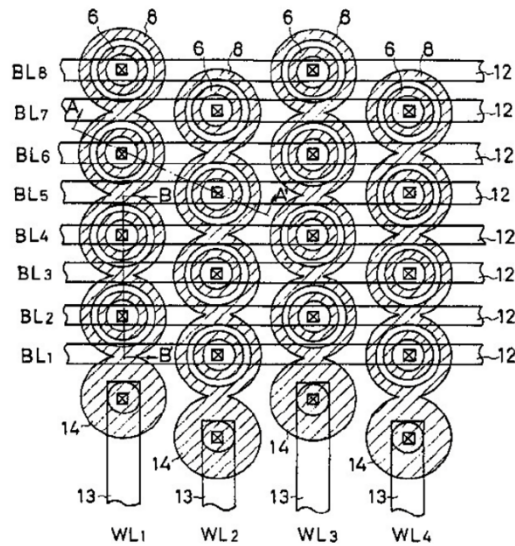


Fig. 1

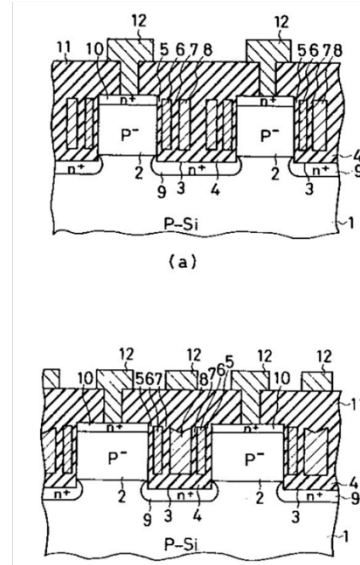


Fig. 2

EX1008, Endoh, FIGS. 1, 2(a), and 2(b) (Embodiment 1)

56. Regarding Embodiment 2 of Endoh, as shown in FIGS. 6, 7(a), and 7(b) of Endoh below, Endoh teaches that besides memory transistor as taught in Embodiment 1 of Endoh, a gate transistor is used to prevent the condition where “the unit electric current also will flow even if not selected which is not appropriate.” EX1008, Endoh, 5. “The same with the previous embodiments [including Embodiment 1],” Embodiment 2 of Endoh also teaches a memory device formed by arranging to “form pillar-shaped silicon layer 2, form the drain

diffused layer 10 above each pillar-shaped silicon layer 2 and form the common source diffused layer 9 in the bottom of groove 3” of the silicon substrate.

EX1008, Endoh, 5.

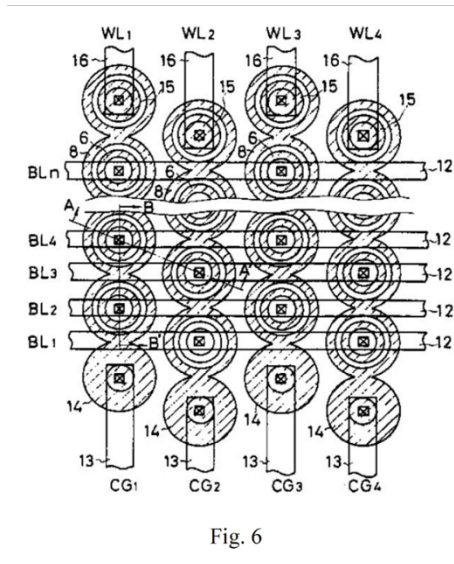


Fig. 6

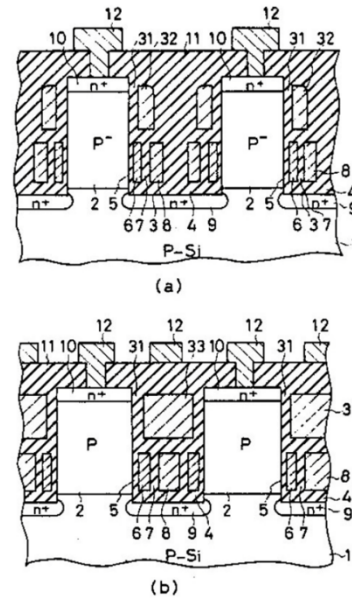


Fig. 7

EX1008, Endoh, FIGS. 6, 7(a), and 6(b) (Embodiment 2)

2. Summary of Hwang

57. Hwang is titled “Vertical Structure Semiconductor Memory Devices and Methods of Manufacturing the Same.” EX1009, Hwang, Title. Hwang’s “[e]xample embodiments of inventive concepts relate to semiconductor devices, for example, semiconductor memory devices in which memory cells are arranged vertically.” EX1009, Hwang, 1:15-18, Field.

58. Hwang acknowledges “[e]lectronic appliances are becoming increasingly smaller in size, while data throughput requirements increase,” as such

“semiconductor memory devices for electronic appliances generally require higher integration densities.” EX1009, Hwang, 1:20-23. To achieve high integration densities, embodiments of Hwang “provide vertical structure semiconductor memory devices capable of increasing the dielectric breakdown voltage between an electrode coupled to an impurity region and transistors disposed on one another in a vertical direction.” EX1009, Hwang, 1:27-31. Hwang also provides that its embodiments also “reduce a parasitic capacitance” and “operate with improved reliability relative to conventional semiconductor devices.” EX1009, Hwang, 1:31-32, 10:35-46.

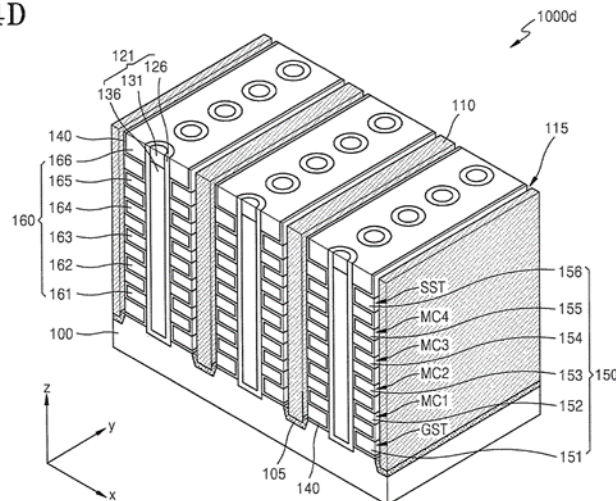
59. A POSITA would have understood that in Hwang, reference numerals denote like elements in different embodiments, and as such, descriptions of elements in one embodiment (e.g., substrate contact electrode 110 of FIG. 3) applies in like elements in another embodiment (e.g., substrate contact electrode 110 of FIG. 4D). *See* EX1009, Hwang, 10:55-58 (“In FIG. 4A to FIG. 4D, reference numerals like those used in FIG.3 denote like elements. Thus, in order to avoid redundancy, detailed descriptions of those elements are not provided.”).

60. Hwang teaches that to achieve memory devices with high integration densities and improved performance, vertical structure semiconductor memory devices include a vertical contact plug connected to a lower diffusion layer (e.g., a bottom source region), and vertical channels share the vertical contact plug and are

uniformly arranged near the vertical contact plug.

61. For example, as shown in FIG. 4D of Hwang below, Hwang teaches a semiconductor device 1000d, where “cylindrical semiconductor regions 121 extend from the upper surface of the substrate 100 in the z-axis direction, and are arranged in a matrix array.” EX1009, Hwang, 11:62-66. Furthermore, Hwang teaches that the cylindrical semiconductor regions 121 (vertical channels), share the impurity regions 105 (lower diffusion layer) and the substrate contact electrodes 110 (vertical contact plug) connected to the impurity regions 105 (lower diffusion layer), and the cylindrical semiconductor regions 121 (vertical channels) are uniformly arranged near the substrate contact electrodes 110 (vertical contact plug).

FIG. 4D



EX1009, Hwang, FIG. 4D

62. Specifically, Hwang describes “a plurality of substrate contact

electrodes 110 extending in the z-axis direction are disposed in ohmic contact with the respective ones of the impurity regions 105.” EX1009, Hwang, 10:6-9. “The substrate contact electrodes 110 also extend in the y-axis direction along respective ones of the impurity regions 105.” EX1009, Hwang, 10:9-11. Hwang describes that “[e]ach substrate contact electrode 110 includes at least one metal line composed of a metal selected from the group including tungsten (W), aluminum (Al), copper (Cu) and the like.” EX1009, Hwang, 10:13-16. “[I]f the impurity regions 105 have a conductivity type opposite to that of the substrate 100, the substrate contact electrodes 110 may be coupled to the common source line CSL (as shown, e.g., in FIG. 1).” EX1009, Hwang, 10:20-24. “In the example embodiment illustrated in FIG. 4D, a memory cell string extends along each semiconductor region 121 in the Z-axis direction.” EX1009, Hwang, 12:13-15.

63. Hwang explains that in addition to achieving high integration densities by using vertical structures including cylindrical semiconductor regions 121 and substrate contact electrodes 110, various performance improvements are achieved by various features related to the vertical structures. For example, using air gap to insulate the substrate contact electrodes 110 from gate electrodes 150 reduces the parasitic capacitance between the substrate contact electrode 110 and the gate electrodes 150, increases the dielectric breakdown voltage between the substrate contact electrodes 110 and the gate electrodes 150, such that the

semiconductor memory device 1000 may operate with improved reliability relative to conventional semiconductor devices. *See, e.g.*, EX1009, Hwang, 12:8-13 (“As in the semiconductor memory device 1000 of FIG. 3, the substrate contact electrodes 110 in the semiconductor memory device 1000d of FIG. 4D are separated and insulated from the memory cell strings by insulating regions 115, which are in the form of air gaps.”); EX1009, Hwang, 10:35-46 (“The substrate contact electrodes 110 are insulated from the gate electrodes 150 by the insulating regions 115. In the example embodiment shown in FIG.3, the insulating regions 115 are air gaps. Because the dielectric constant of air is less than the dielectric constant of other insulating materials, the parasitic capacitance between the substrate contact electrode 110 and the gate electrodes 150 may be reduced. In addition, the dielectric breakdown voltage between the substrate contact electrodes 110 and the gate electrodes 150 may increase. Thus, the semiconductor memory device 1000 may operate with improved reliability relative to conventional semiconductor devices.”). A POSITA would have understood these benefits of the configurations described with reference to FIG. 3 similarly applies to the semiconductor device 1000d of FIG. 4D.

3. Reasons to Combine Endoh and Hwang

64. A POSITA would have been motivated to apply Hwang’s teaching of arrangement of vertical structures (including providing a vertical contact plug for

connecting the bottom source region to a common source line and vertical channels sharing the vertical contact plug and uniformly arranged near the vertical contact plug) in embodiments of Endoh to produce the obvious, beneficial, and predictable results of high integration density and performance (e.g., reduced parasitic capacitance, and improved reliability relative to conventional semiconductor devices), as taught by Hwang.

65. First, like the '233 patent, Endoh and Hwang are analogous prior art to the '233 patent, and are in the same field of endeavor pertaining to semiconductor devices. *See, e.g.*, EX1001, '233 patent, Abstract (providing “a semiconductor device” that “includes a plurality of vertical transistors.”); EX1008, Endoh, Title (“Non-volatile Semiconductor Memory”); 2, Field of Invention (“about a non-volatile electrically erasable semiconductor memory using memory transistor with charge accumulation layer and control gate (EEPROM);” *see also e.g.*, EX1008, Endoh, FIGS. 1, 2(a), 2(b), 6, 7(a), 7(b) (disclosing various embodiments of semiconductor memory devices including vertical structures); EX1009, Hwang, Title (“Vertical Structure Semiconductor Memory Devices and Methods of Manufacturing the Same”); EX1009, Hwang, 1:15-18 (“[e]xample embodiments of inventive concepts relate to semiconductor devices, for example, semiconductor memory devices in which memory cells are arranged vertically.”).

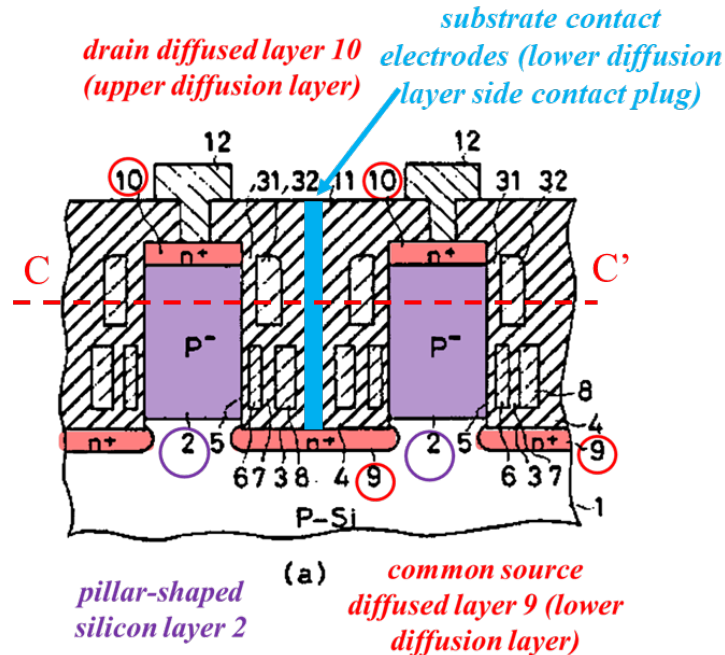
66. Second, Endoh itself provides motivations to use Hwang’s teachings

in the semiconductor devices of Endoh, including the needs to connect a bottom common source region to a common source line and to achieve high memory cell density and improved performance. For example, Endoh has a need to connect its bottom common source region to a common source S. *See, e.g.*, EX1008, Endoh, FIG. 9 (illustrating a common source S connected to the common source diffused layer 9), 6. For further example, Endoh describes one of its goals is “achieving the purpose of reducing the area of memory cell and enlarging the capacitance of EEPROM.” EX1008, Endoh, 2; *see also* EX1008, Endoh, 3 (“[the invention] can reduce the area of isolation region of elements, so as to make the size of memory cell smaller.”).

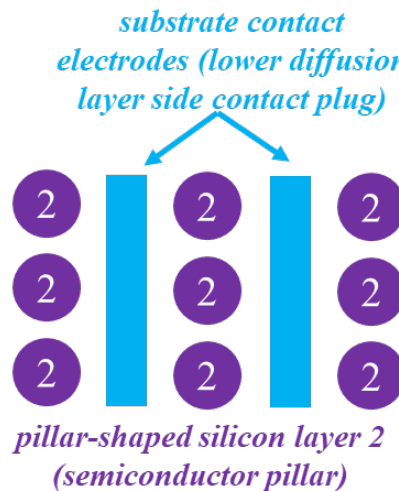
67. A POSITA with Endoh would have looked to Hwang and been motivated to apply Hwang’s teachings of the vertical structure arrangement of the vertical contact plug and the vertical channels in the semiconductor devices of Endoh, because Hwang’s teachings (1) provide the connection between the bottom source region to a common source line as needed by Endoh, and (2) provide the obvious, beneficial, and predictable results of high integration density and improved performance (e.g., reduced parasitic capacitance, improved reliability, more uniform electronic characteristics) with the vertical channel and contact arrangement and features. *See, e.g.*, EX1009, Hwang, 1:20-23 (providing techniques to address the need that “[e]lectronic appliances are becoming

increasingly smaller in size, while data throughput requirements increase,” as such “semiconductor memory devices for electronic appliances generally require higher integration densities”); EX1009, Hwang, 1:27-31 (describing “provid[ing] vertical structure semiconductor memory devices capable of increasing the dielectric breakdown voltage between an electrode coupled to an impurity region and transistors disposed on one another in a vertical direction”); EX1009, Hwang, 1:31-32, 10:35-46, 12:8-13 (describing embodiments that “reduce a parasitic capacitance” and “operate with improved reliability relative to conventional semiconductor devices”).

68. Simplified figures of an example (Example 1) of the combination of Endoh and Hwang are provided below, including a cross-section of Example 1 (based on FIG. 7(a) of Endoh) and a top view of Example 1 along C-C’ of the cross-section of Example 1.



**Cross-section of Example 1 of Endoh Combined with Hwang
(Annotated Based on EX1008, Endoh, FIG. 7(a))**



**Top-view Along C-C' of Cross-section of Example 1 of
Endoh Combined with Hwang**

69. Finally, applying Hwang's teachings in embodiments of Endoh would

have been no more than the combination of known elements according to known methods (e.g., incorporating the arrangement of the vertical channels and vertical

contact plugs according to the known processing steps) obvious to a POSITA.

Techniques (e.g., using photolithography to form the contact trench/hole and using chemical vapor deposition (CVD) to form conductive materials in the contact trench/hole) for forming vertical contact plugs and arranging the vertical channels uniformly near the contact plug were well-known. *See, e.g.*, EX1009, Hwang, 21:6-14, FIG. 8I (describing forming the vertical contact plug 110 with conductive materials, e.g., tungsten (W)); *see also* EX1007, Takaishi, [0058], FIG. 18 (disclosing forming vertical contact plug 25 with conductive materials, e.g., W/TiN/Ti). Furthermore, techniques for using different metal levels to form different connections (e.g., the connection of the vertical contact plug to a common source line and other connections like bit lines and word lines) in order to avoid metal wire shorting were well-known. *See, e.g.*, EX1009, Hwang, 8A-8L (illustrating forming bit line 193 at a higher layer than conductive layer 130); FIGS. 9A-9H (illustrating forming bit line 293 at a higher layer than conductive layer 230).

70. As such, the combination of Hwang's teachings of the vertical structure arrangement (e.g., a vertical contact plug connecting a lower diffusion layer to a common source line and vertical channels sharing and uniformed arranged near the vertical contact plug) with the embodiments of semiconductor devices of Endoh is nothing more than the combination of known elements

applying known methods, and would have been obvious to a POSITA.

4. Claim 1

[1.0] *A semiconductor device comprising:*

71. To the extent that this preamble is deemed limiting, Endoh discloses or renders obvious a semiconductor device.

72. Specifically, Endoh is titled “Non-volatile Semiconductor Memory,” and is “about a non-volatile electrically erasable semiconductor memory using memory transistor with charge accumulation layer and control gate (EEPROM).” EX1008, Endoh, 1 (Title of Invention); Endoh 2 (“Field of the Invention”); *see also e.g.*, Endoh, FIGS. 1, 2(a), 2(b), 6, 7(a), 7(b) (disclosing various embodiments of semiconductor memory devices).

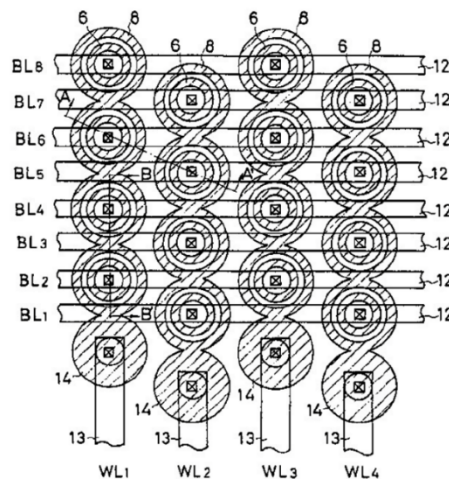


Fig. 1

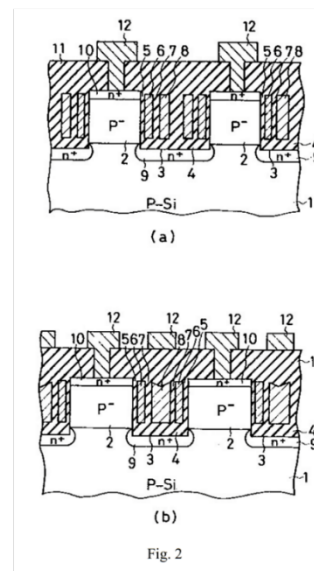


Fig. 2

EX1008, Endoh, FIGS. 1, 2(a), and 2(b) (Embodiment 1)

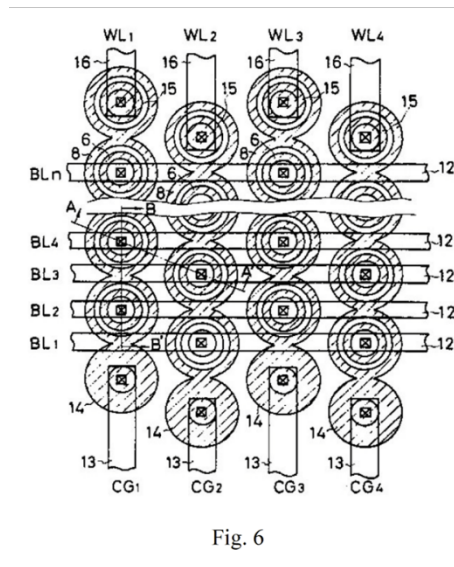


Fig. 6

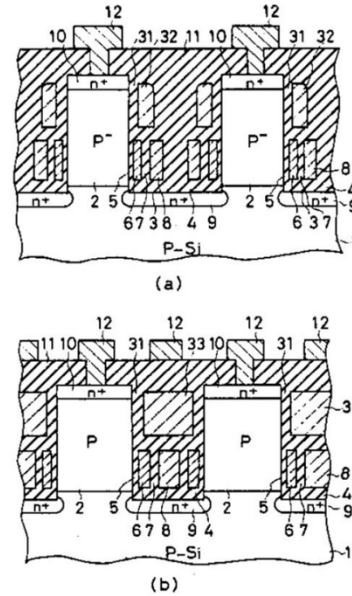


Fig. 7

EX1008, Endoh, FIGS. 6, 7(a), and 6(b) (Embodiment 2)

73. Therefore, Endoh discloses a semiconductor memory device, which teaches “a semiconductor device,” as recited in the claim.

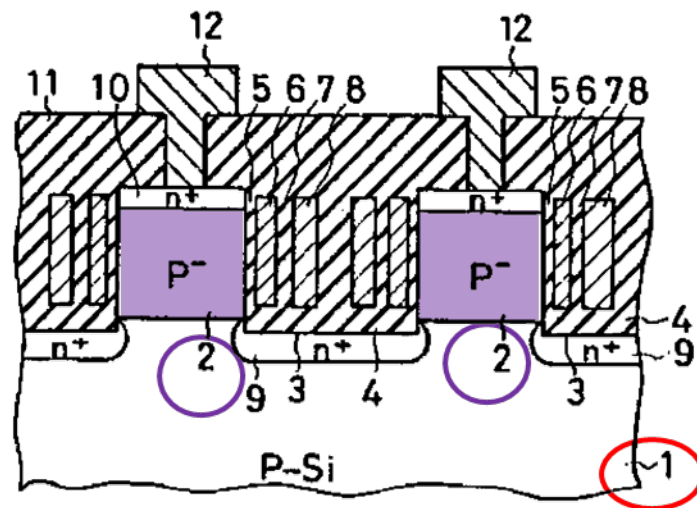
[1.1] a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region;

74. Endoh discloses or renders obvious a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region.

75. **First**, Endoh teaches, e.g., in each of Embodiments 1 and 2, a semiconductor memory device including a plurality of pillar-shaped silicon layer 2 (semiconductor pillars) provided to stand from a P-type silicon substrate 1, each of

the pillar-shaped silicon layers comprising a channel region.

76. Regarding Embodiment 1, as shown in annotated FIG. 2(a) (section diagram of A-A' in Fig. 1), Endoh teaches that the semiconductor memory device includes a plurality of pillar-shaped silicon layer 2 (semiconductor pillars) provided to stand from a P-type silicon substrate 1.



(a)

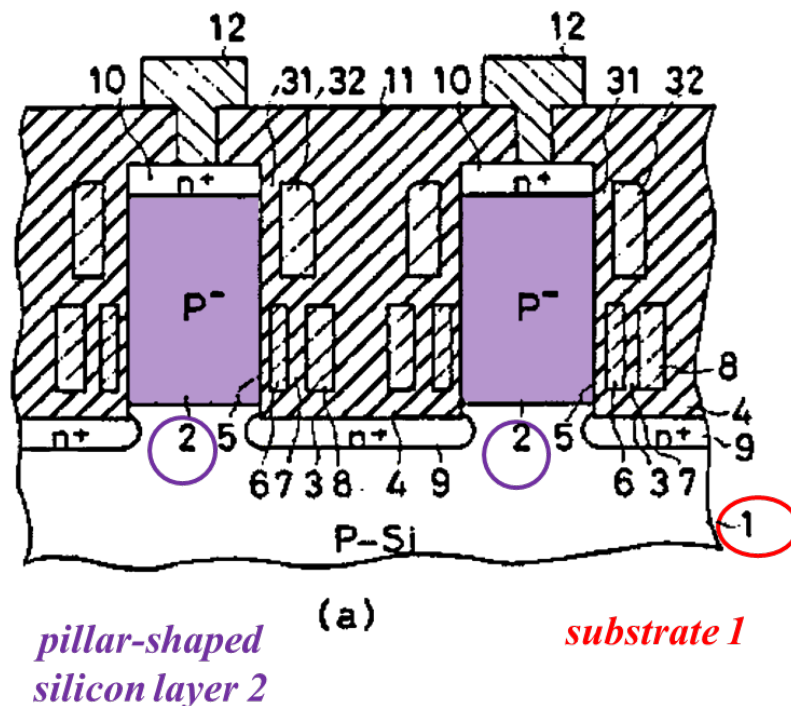
*pillar-shaped
silicon layer 2*

substrate 1

EX1008, Endoh, FIG. 2(a), annotated

77. Specifically, Endoh describes that “[i]n this embodiment [FIGS. 1, 2(a), and 2(b)], it uses **P-type silicon substrate**, it is separated by the plaid-shaped groove 3 on the top of it, presenting **multiple pillar-shaped P-type silicon layers** in matrix arrangement, the pillar-shaped silicon layer 2 is changed to be the domain of memory cell, respectively.” EX1008, Endoh, 3.

78. Similarly, regarding Embodiment 2, as shown in annotated FIG. 7(a) (section diagram of A-A' in Fig. 6), Endoh teaches that the semiconductor memory device includes a plurality of a plurality of pillar-shaped silicon layer 2 (semiconductor pillars) provided to stand from a P-type silicon substrate 1. EX1008, Endoh, 5 (“In these figures [of FIGS. 6, 7(a), and 7(b)], when using the same symbols with the corresponding part in the previous embodiments, the detailed description is omitted.”); EX1008, Endoh, 5 (“The same with the previous embodiments [including Embodiment 1], depending on groove 3, to separate and arrange to form pillar-shaped silicon layer 2” on substrate 1).



EX1008, Endoh, FIG. 7(a), annotated

79. As such, pillar-shaped silicon layer 2 of the semiconductor memory

device) of the semiconductor memory device teach “*a plurality of semiconductor pillars*” as claimed.

80. Second, Endoh teaches that the pillar-shaped silicon layer 2 comprises a channel region. Specifically, as shown in annotated FIGS. 2(a) and 7(a) above, Endoh describes that the semiconductor memory device includes common source diffused layer 9 formed at the bottom of pillar-shaped silicon layer 2, and drain diffused layer 10 is formed at the top of pillar-shaped silicon layer 2. EX1008, Endoh, 3, 5 (describing common source diffused layer 9 and drain diffused layer 10).

81. As such, a POSITA would have understood that the pillar-shaped silicon layer 2 includes a channel region. The channel region is located between the common source diffused layer 9 and the common source diffused layer 9, where the electric current flows in the channel between the common source diffused layer 9 and the common source diffused layer 9. EX1008, Endoh, 4 (“By supplying the positive potential to the selection word line and selection bit line to **flow the channel current on the selected memory cell**, so as to inject the hot electron formed nearby drain electrode into the floating gate. In this way, the threshold value of this memory cell moves in the positive direction. This is so-called data writing.”). EX1008, Endoh, 4; *see also* EX1007, Takaishi, [0026] (providing the well-known knowledge that “[e]ach silicon pillar 5 is a

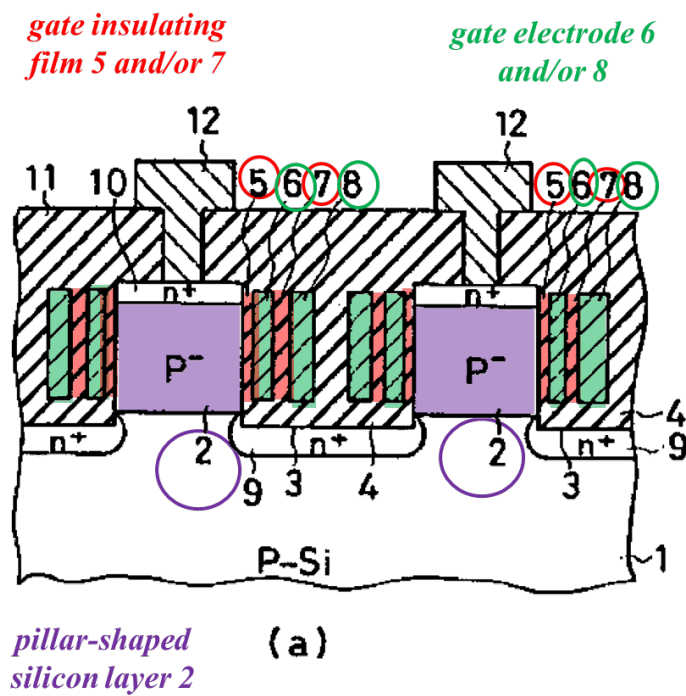
semiconductor layer having a pillar shape **which forms a channel** and parts of a source section and a drain section of each unit transistor 50.”)

82. Therefore, Endoh discloses or renders obvious that “a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region,” as recited in the claim.

[1.2] *a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars;*

83. Endoh discloses or renders obvious that the semiconductor device includes a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars.

84. For example, as shown in annotated FIGS. 1 and 2(a), the semiconductor device of Embodiment 1 includes tunnel oxidation film 5 (gate insulating film) for floating gate 6 (gate electrode) and layer dielectric film 7 (gate insulating film) for control gate 8 (gate electrode) provided over a side surface of each of the pillar-shaped silicon layer 2. EX1008, Endoh, 3 (“the floating gate 6 is formed on the side wall by relying on **tunnel oxidation film 5** by surrounding the pillar-shaped silicon layer 2, in addition, control gate 8 is formed in the outside of it through **layer dielectric film 7**.”).



EX1008, Endoh, FIG. 2(a), annotated

gate electrode 6, 8

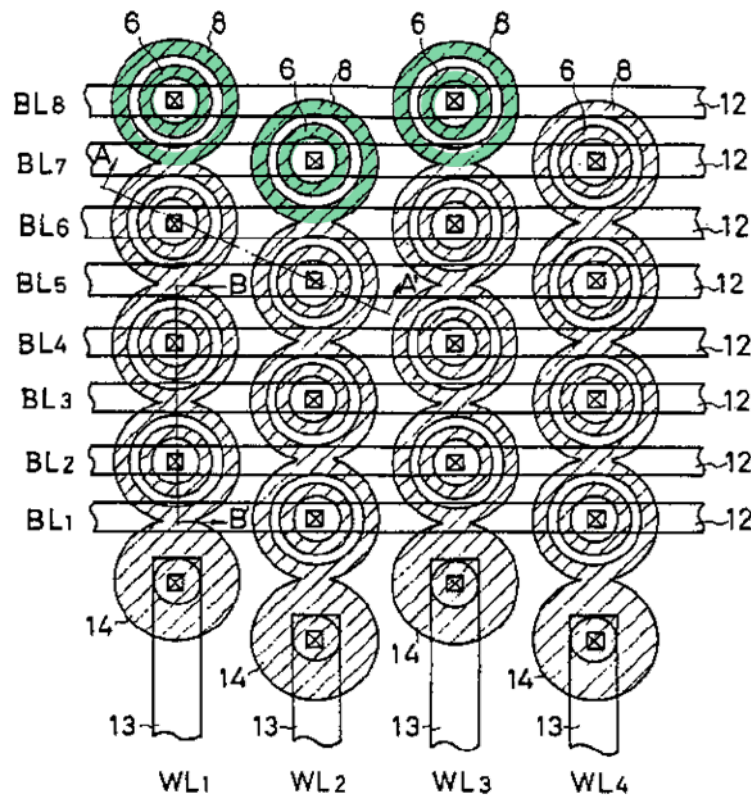


Fig. 1

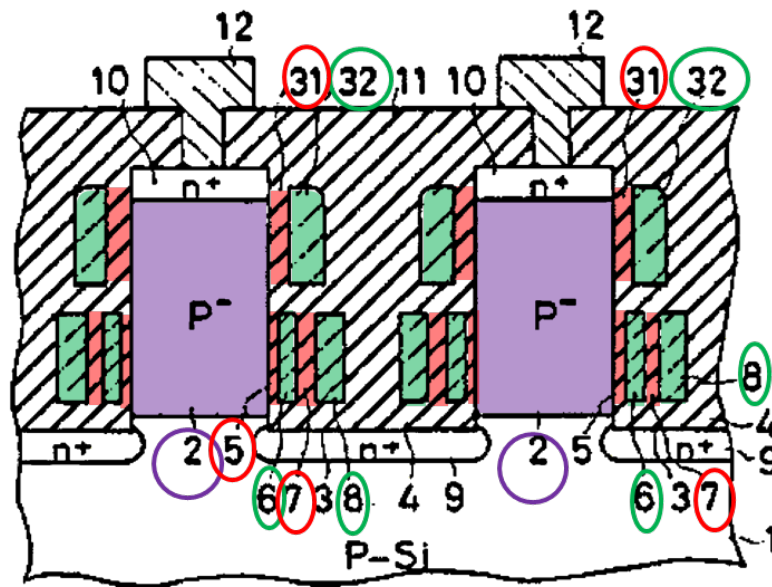
EX1008, Endoh, FIG. 1, annotated

85. Similarly, as shown in annotated FIGS. 6 and 7(a) of Endoh below, the semiconductor device of Embodiment 2 includes tunnel oxidation film 5 (gate insulating film) for floating gate 6 (gate electrode) and layer dielectric film 7 (gate insulating film) for control gate 8 (gate electrode) provided over a side surface of each of the pillar-shaped silicon layer 2. EX1008, Endoh, 5 (“The memory cell is in the bottom of such pillar-shaped silicon layer 2; the same with the method of the previous embodiments, the floating gate 6 is formed through tunnel oxide film 5;

then the control gate 8 is formed by layer dielectric film 7, thereby constituting memory transistor.”).

*gate insulating film
5, 7, and/or 31*

*gate electrode 6,
8, and/or 32*



(a)

*pillar-shaped
silicon layer 2*

EX1008, Endoh, FIG. 7(a), annotated

gate electrode
6, 8

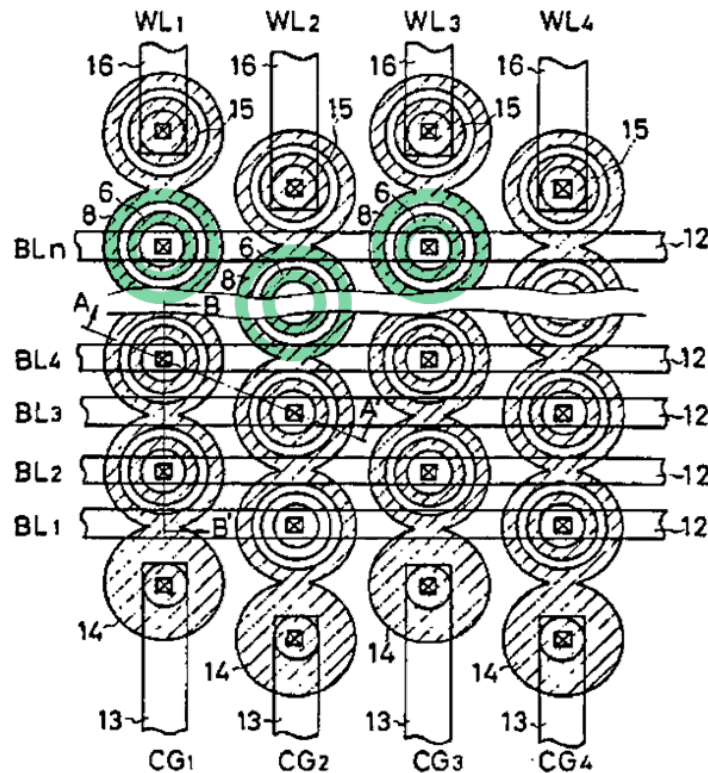


Fig. 6

EX1008, Endoh, FIG. 6, annotated

86. Furthermore, the semiconductor device of Embodiment 2 includes gate oxide film 31 (gate insulating film) for gate electrode 32 (gate electrode) provided over a side surface of each of the pillar-shaped silicon layer 2. EX1008, Endoh, 5 (“And, in the upside of pillar-shaped silicon layer 2, the same with memory transistor, the gate electrode 32 is set through gate oxide film 31 surrounding it, constituting selection gate transistor. The same with control gate 8 of memory cell, gate electrode 32 of this transistor is continuously set in the same

direction with control gate line to form selection gate line. Through this method, in the internal groove, memory transistor and selection gate transistor are implanted and formed under the state of stack.”). Endoh also teaches that in some embodiments, as shown in FIGS. 13(a) and (b), “the control gate 8 of memory transistor and gate electrode 32 of selection gate transistor are continuously formed.” EX1008, Endoh, 7, FIGS. 13(a) and (b).

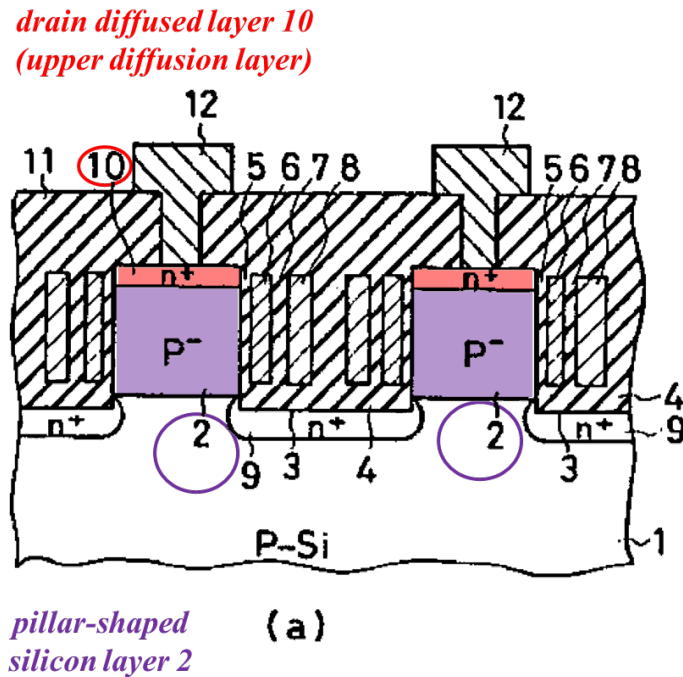
87. Therefore, Endoh (e.g., each of gate insulating films 5, 7, and 31 for corresponding gate electrodes 6, 8, and 32 respectively) discloses or at least renders obvious “*a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars,*” as recited in the claim.

[1.3] *an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain;*

88. Endoh discloses or renders obvious that the semiconductor device includes an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain.

89. For example, as shown in annotated FIG. 2(a) and FIG. 3 of Endoh below, Endoh describes that “**drain diffused layer 10** of various memory cells is formed on various pillar-shaped silicon layer 2,” which teaches an upper diffusion layer provided at an upper end of the pillar-shaped silicon layer 2 to serve as a drain (one of a source and a drain). EX1008, Endoh, 3. Referring to FIG. 3(b),

Endoh describes the process forming the drain diffused layer 10 by “implant[ing] n-type impurity into the ion, it respectively forms **drain diffused layer 10 on the top of** various pillar-shaped silicon layer 2.” EX1008, Endoh, 4.



EX1008, Endoh, FIG. 2(a), annotated

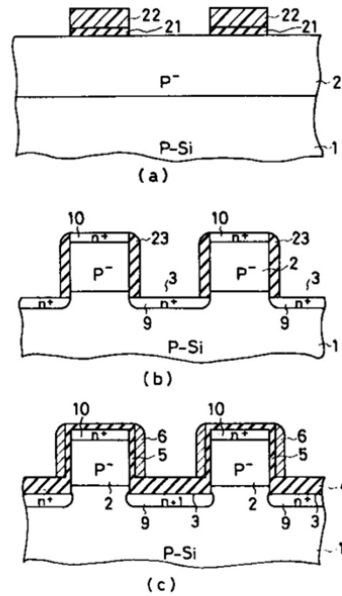
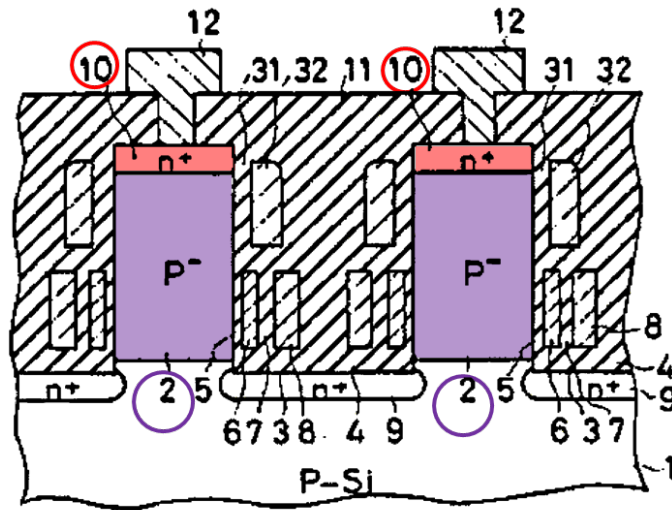


Fig. 3

EX1008, Endoh, FIG. 3

90. For further example, as shown in annotated FIG. 7(a) and FIG. 8 of Endoh below, Endoh describes “**form[ing] the drain diffused layer 10 above each pillar-shaped silicon layer 2**”. EX1008, Endoh, 5. Referring to FIG. 8(b), Endoh describes that “drain diffused layer 10 is formed above each silicon layer 2.” EX1008, Endoh, 5.

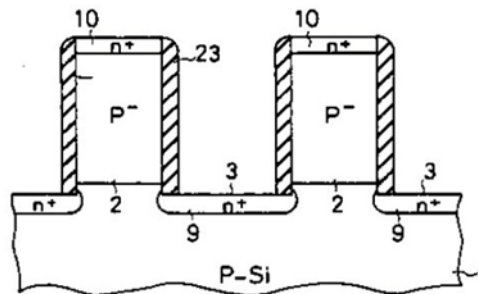
*drain diffused layer 10
(upper diffusion layer)*



(a)

*pillar-shaped
silicon layer 2*

EX1008, Endoh, FIG. 7(a), annotated



(b)

Fig. 8

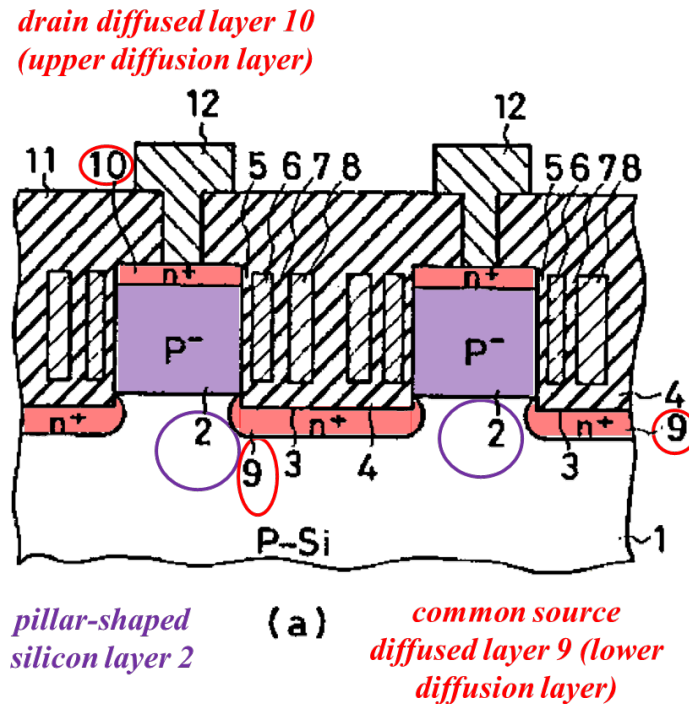
EX1008, Endoh, FIG. 8

91. Therefore, Endoh discloses or renders obvious that “an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain,” as recited in the claim.

[1.4] *a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain; and*

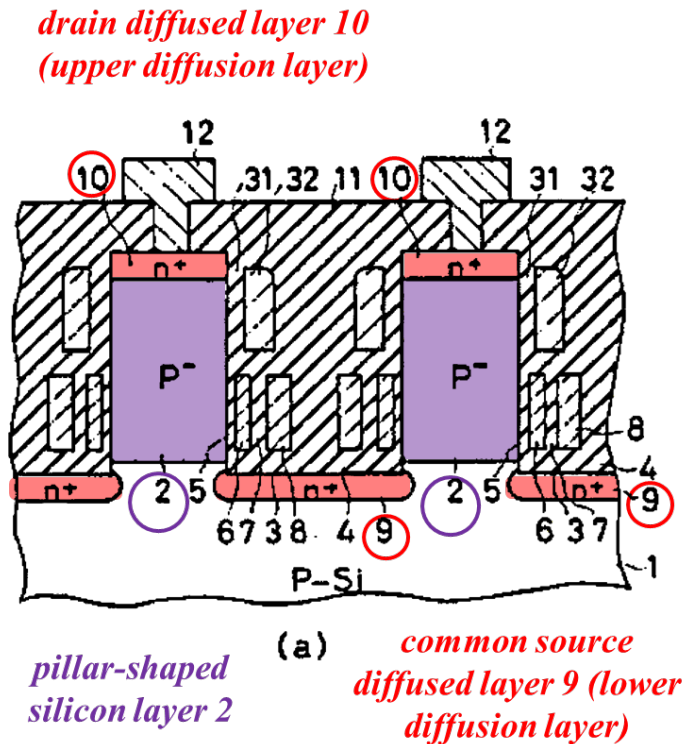
92. Endoh discloses or renders obvious that the semiconductor device includes a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain.

93. For example, as shown in annotated FIG. 2(a) of Endoh below, Endoh describes that “[t]he **common source diffused layer 9 of memory cell is formed at the bottom of groove 3**” of the substrate 1, which teaches a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars 2 to serve as to serve as a source (the other of the source and the drain). EX1008, Endoh, 3. Referring to FIG. 3(b), Endoh describes the process forming semiconductor devices includes that by “implant[ing] n-type impurity into the ion, it respectively forms drain diffused layer 10 on the top of various pillar-shaped silicon layer 2; it forms **common source diffused layer 9 at the bottom of groove.**” EX1008, Endoh, 4.



EX1008, Endoh, FIG. 2(a), annotated

94. For further example, as shown in annotated FIG. 7(a) of Endoh below, Endoh describes “form[ing] **common source diffused layer 9 in the bottom of groove 3**” of the substrate 1, which teaches a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars 2 to serve as to serve as a source (the other of the source and the drain). EX1008, Endoh, 5. Referring to FIG. 8(a), (b), Endoh describes that “the common source diffused layer 9 is formed in the bottom of groove.” EX1008, Endoh, 6.



EX1008, Endoh, FIG. 7(a), annotated

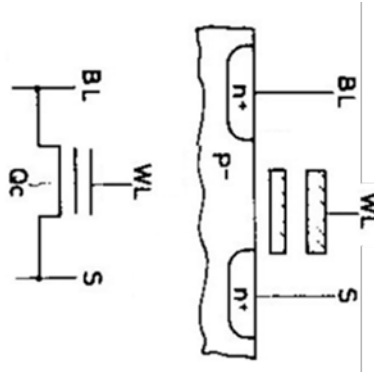
95. Therefore, Endoh discloses or renders obvious “a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain,” as recited in the claim.

[1.5] a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug, and;

96. Endoh in view of Hwang renders obvious a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug.

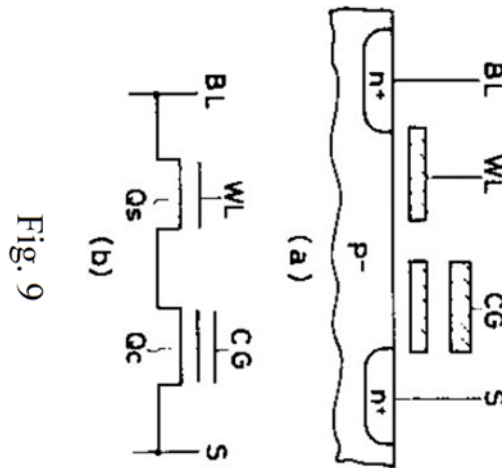
97. First, as discussed at Ground 1:[1.5], Endoh teaches that multiple pillar-shaped silicon layer 2 (semiconductor pillars) share the common source diffused layer 9 (the lower diffusion layer). As illustrated in the example equivalent circuit diagrams of Embodiments 1 and 2, a POSITA would have understood that in the semiconductor devices of Endoh, the n-type common source diffused layer 9 is connected to a common source line (CSL) (indicated as “S” in the equivalent circuit diagrams below). As such, Endoh has the need to provide a connection between the n-type common source diffused layer 9 (at the bottom of the semiconductor pillars) and the common source line (CSL) (above the top of the semiconductor pillars).

98. Specifically, for Embodiment 1, I have drawn the Equivalent Circuit Diagram below (with “S” at the bottom to be aligned with the vertical structures of the semiconductor device) to illustrate the actions of the semiconductor device. Specifically, the BL (bit line 12) is connected to the drain diffused layer 10 (upper diffusion layer serving as a drain), the common source S is connected to the common source diffused layer 9 (lower diffusion layer serving as a source shared by multiple pillar-shaped silicon layer 2), and the channel current is flowed in the channel region of the pillar-shaped silicon layer 2 (semiconductor pillars) between the source and the drain.



Equivalent Circuit Diagram of Embodiment 1

99. For Embodiment 2, as shown in FIG. 9 below (rotated 90 degrees to the right to be aligned with the vertical structure of the semiconductor device), the BL (bit line 12) is connected to the drain diffused layer 10 (upper diffusion layer serving as a drain), the common source S is connected to the common source diffused layer 9 (lower diffusion layer serving as a source shared by multiple pillar-shaped silicon layer 2), and the channel current is flowed in the channel region of the pillar-shaped silicon layer 2 (semiconductor pillars) between the source and the drain. EX1008, Endoh, 6. The difference from Embodiment 1 is that Embodiment 2 includes a selection gate transistor Qs. EX1008, Endoh, 6.

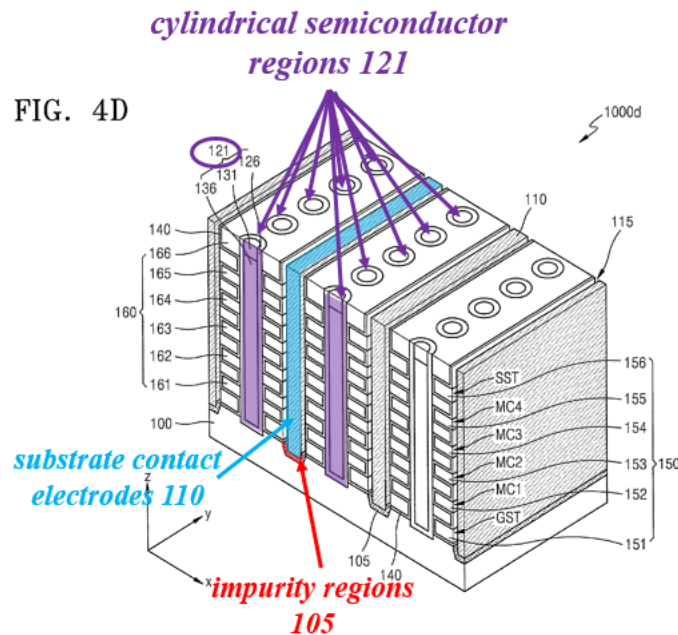


Endoh, FIG. 9 (Rotated 90 Degrees to the Right)

100. Second, with Endoh's need to provide a connection between the n-type common source diffused layer 9 (at the bottom of the semiconductor pillars) and the common source line (CSL) (above the top of the semiconductor pillars), a POSITA would have looked to Hwang and applied Hwang's teachings of providing a vertical contact plug to connect the bottom source region to a common source line, in Endoh.

101. Specifically, as shown in FIG. 4 of Hwang below, Hwang teaches using vertical substrate contact electrodes 110 (vertical contact plug) to connect the bottom source region (impurity regions 105) to a common source line. Hwang's substrate contact electrodes 110 teaches the "*lower diffusion layer side contact plug*" because it is a vertical contact plug connected to the lower diffusion layer side (impurity regions 105) of the channel regions 121. Specifically, Hwang describes "a plurality of substrate contact electrodes 110 extending in the z-axis

direction are disposed in ohmic contact with the respective ones of the impurity regions 105.” EX1009, Hwang, 10:6-9. “The substrate contact electrodes 110 also extend in the y-axis direction along respective ones of the impurity regions 105.” EX1009, Hwang, 10:9-11. “[I]f the impurity regions 105 have a conductivity type opposite to that of the substrate 100, **the substrate contact electrodes 110 may be coupled to the common source line CSL** (as shown, e.g., in FIG. 1).” EX1009, Hwang, 10:20-24; *see also* EX1009, Hwang, 12:13-15; FIG. 1.



EX1009, Hwang, FIG. 4D, annotated

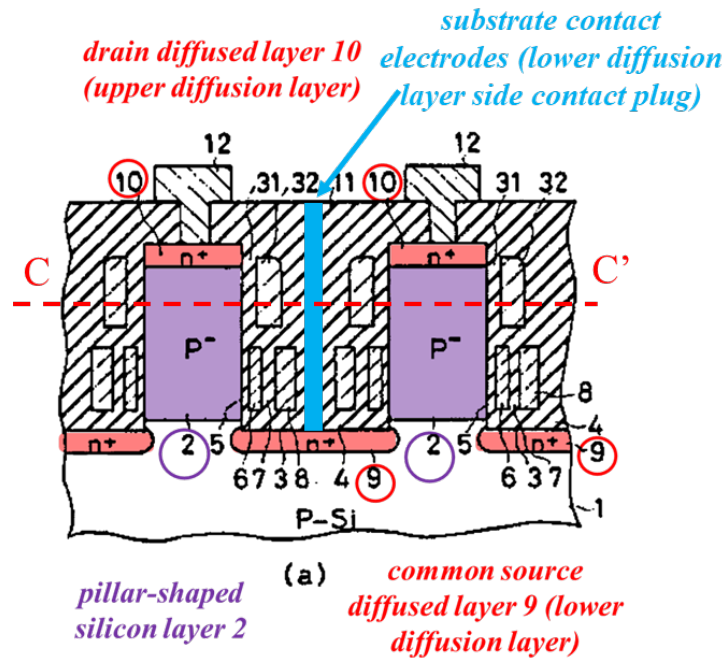
102. A POSITA would have understood that Hwang’s cylindrical semiconductor regions 121 provide channel regions, similar to Endoh’s pillar-shaped semiconductor layer 2. Hwang’s impurity regions 105 provide one of a source and a drain, similar to Endoh’s common source diffused layer 10. Hwang’s

substrate contact electrodes 110 provides connection of the source region at the bottom of the cylindrical semiconductor regions 121 to a common source line.

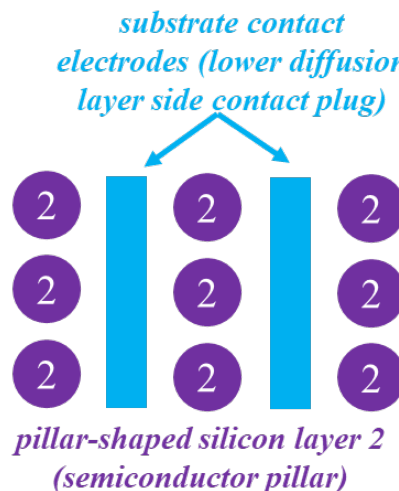
103. Accordingly, a POSITA would have been motivated to apply Hwang's teachings of the vertical structure arrangement including the vertical contact plug (substrate contact electrodes 110) providing connection between the bottom source region (impurity regions 105) to a common source line (CSL) in the semiconductor devices of Endoh, because Hwang's teachings provide the connection between the bottom source region to a common source as needed by Endoh, while providing the obvious, beneficial, and predictable results of high integration density and improved performance (e.g., reduced parasitic capacitance, and improved reliability) with Hwang's vertical channel and contact arrangement and features. *See, e.g.*, EX1009, Hwang, 1:27-32; 12:8-13; 10:35-46; Ground 1: Reasons to Combine Endoh and Hwang.

104. As shown in the simplified figures of Example 1 of the combination of Endoh and Hwang below, in the combination of Endoh and Hwang, a vertical contact plug (lower diffusion layer side contact plug) is connected to the common source diffused layer 9 (the lower diffusion layer), and the plurality of pillar-shaped silicon layer 2 (semiconductor pillars) share the common source diffused layer 9 (the lower diffusion layer) and the vertical contact plug (lower diffusion layer side contact plug), because the lower end of the multiple pillar-shaped silicon

layer 2 is connected to a common source line through the common source diffused layer 9 and the vertical contact plug. Similar to the '233 patent, the pillar-shaped silicon layer (2) is electrically connected to the common source diffused layer (9) when the transistors are turned on.



**Cross-section of Example 1 of Endoh Combined with Hwang
(Annotated Based on EX1008, Endoh, FIG. 7(a))**



**Top-view Along C-C' of Cross-section of Example 1 of
Endoh Combined with Hwang**

105. Therefore, Endoh in view of Hwang renders obvious “a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug,” as recited in the claim.

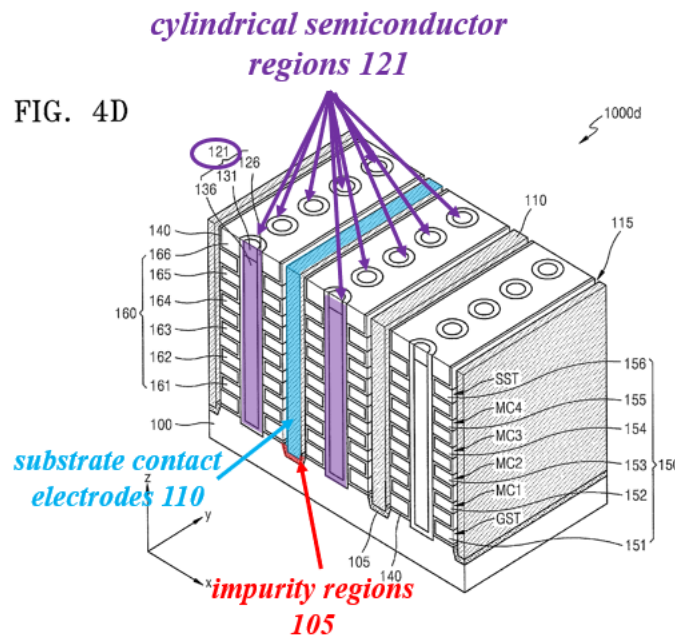
[1.6] *the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.*

106. Endoh in view of Hwang renders obvious that the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.

107. First, as discussed above at [1.5], a POSITA would have been motivated to apply Hwang’s teachings of the arrangement of the vertical structures including the vertical contact plug in the semiconductor devices of Endoh, such that Endoh in view of Hwang renders obvious a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug.

108. Second, Hwang discloses arrangement of vertical structures, including vertical channels sharing the vertical contact plug and uniformly arranged near the vertical contact plug, for high integration density and improved performance (e.g., reduced parasitic capacitance, and improved reliability relative to conventional semiconductor devices, more uniform electronic characteristics).

As shown in FIG. 4D of Hwang below, Hwang discloses that to achieve high integration density and improved performance, the vertical channels (cylindrical semiconductor regions 121) are uniformly arranged near the vertical contact plug (substrate contact electrodes 110). As shown in FIG. 4D of Hwang, the vertical channel regions 121 have substantially the same distance to the vertical contact plug 110.



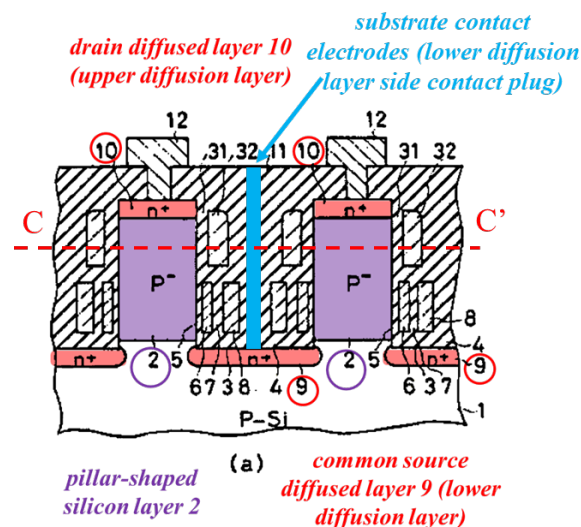
EX1009, Hwang, FIG. 4D, annotated

109. A POSITA would have understood that Hwang's cylindrical semiconductor regions 121 provide channel regions, similar to Endoh's pillar-shaped semiconductor layer 2, and Hwang's impurity regions 105 provide one of a source and a drain, similar to Endoh's common source diffused layer 10.

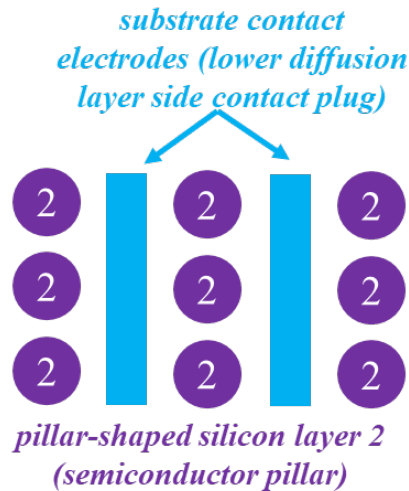
110. Accordingly, a POSITA would have been motivated to apply

Hwang's teachings of the vertical structure arrangement including vertical channels (cylindrical semiconductor regions 121) sharing the vertical contact plug (substrate contact electrodes 110) and uniformly arranged near the vertical contact plug (substrate contact electrodes 110), in the semiconductor device of Endoh, for high integration density and improved performance (e.g., reduced parasitic capacitance, improved reliability, more uniform electronic characteristics). *See also* Ground 1: Reasons to Combine Endoh and Hwang.

111. As shown in the simplified figures of Example 1 of the combination of Endoh and Hwang below, in the combination of Endoh and Hwang, Endoh's pillar-shaped semiconductor layer 2 are uniformly arranged near the vertical contact plug (lower diffusion layer side contact plug), which connects the common source diffused layer 10 (the lower diffusion layer) to the common source line, as taught by Hwang.



**Cross-section of Example 1 of Endoh Combined with Hwang
(Annotated Based on EX1008, Endoh, FIG. 7(a))**



**Top-view Along C-C' of Cross-section of Example 1 of
Endoh Combined with Hwang**

112. Therefore, Endoh in view of Hwang renders obvious that “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug,” as recited in the claim.

5. Claim 2

[2.1] *The semiconductor device according to claim 1, wherein the gate insulating film and the gate electrode are provided to surround the side surface of each of the semiconductor pillars.*

113. Endoh discloses or renders obvious that the gate insulating film and the gate electrode are provided to surround the side surface of each of the semiconductor pillars.

114. **First**, as discussed above at Ground 1:[1.2], Endoh teaches a semiconductor device including tunnel oxidation film 5 (gate insulating film) for

floating gate 6 (gate electrode) and layer dielectric film 7 (gate insulating film) for control gate 8 (gate electrode) provided over a side surface of each of the pillar-shaped silicon layer 2, and/or as shown in Embodiment 2, gate oxide film 31 (gate insulating film) for gate electrode 32 (gate electrode) provided over a side surface of each of the pillar-shaped silicon layer 2.

115. Second, as shown in annotated FIGS. 1 and 6 of Endoh below, Endoh teaches that the gate insulating film and the gate electrode are provided to surround the side surface of each of the semiconductor pillars. For example, Endoh describes that “the floating gate 6 is formed on the side wall by relying on **tunnel oxidation film 5** by surrounding the pillar-shaped silicon layer 2, in addition, control gate 8 is formed in the outside of it through **layer dielectric film 7**.” EX1008, Endoh, 3; *see also* EX1008, Endoh, 5 (in Embodiment 2, “in the upside of pillar-shaped silicon layer 2, the same with memory transistor, **the gate electrode 32 is set through gate oxide film 31 surrounding it**, constituting selection gate transistor.”).

gate electrode 6, 8

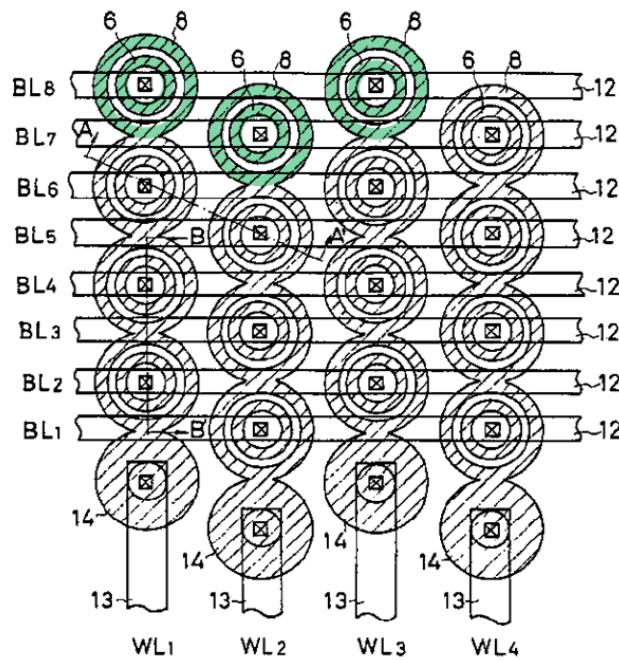


Fig. 1

EX1008, Endoh, FIG. 1, annotated

gate electrode
6, 8

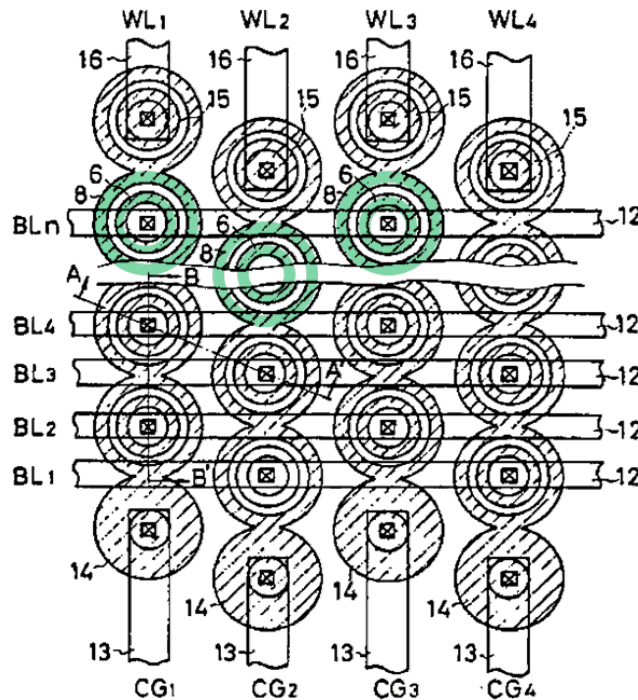


Fig. 6

EX1008, Endoh, FIG. 6, annotated

116. Therefore, Endoh (e.g., each of gate insulating films 5, 7, and 31 for corresponding gate electrodes 6, 8, and 32 respectively) discloses or at least renders obvious that “*the gate insulating film and the gate electrode are provided to surround the side surface of each of the semiconductor pillars,*” as recited in the claim.

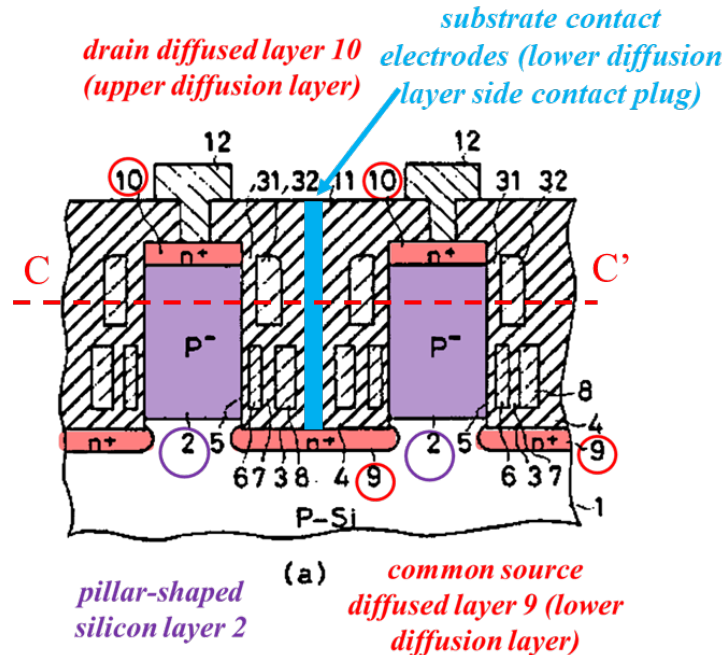
6. Claim 3

[3.1] *The semiconductor device according to claim 1, wherein the semiconductor pillars are uniformly arranged on at least two opposite sides of the lower diffusion layer side contact plug.*

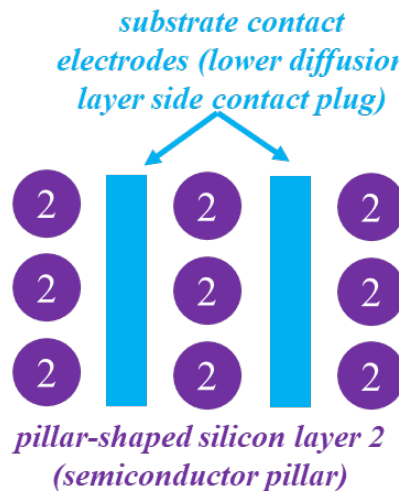
117. Endoh in view of Hwang renders obvious that the semiconductor pillars are uniformly arranged on at least two opposite sides of the lower diffusion layer side contact plug.

118. First, as discussed at Ground 1:[1.6], a POSITA would have been motivated to apply Hwang's teachings of the arrangement of the vertical structures (e.g., vertical channels (cylindrical semiconductor regions 121) sharing and uniformly arranged near the vertical contact plug (substrate contact electrodes 110)) in the semiconductor devices of Endoh, such that Endoh in view of Hwang renders obvious that the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.

119. Second, as shown in FIG. 4D of Hwang below, Hwang teaches that the cylindrical semiconductor regions 121 (vertical channel regions) are uniformly arranged on at least two opposite sides of the substrate contact electrodes 110 (vertical contact plug).



**Cross-section of Example 1 of Endoh Combined with Hwang
(Annotated Based on EX1008, Endoh, FIG. 7(a))**



**Top-view Along C-C' of Cross-section of Example 1 of
Endoh Combined with Hwang**

122. Therefore, Endoh in view of Hwang renders obvious that “the semiconductor pillars are uniformly arranged on at least two opposite sides of the lower diffusion layer side contact plug,” as recited in the claim.

B. Ground 2: Claims 1-4 are Rendered Obvious under 35 U.S.C. § 103(a) over Takaishi.

123. In my opinion, Takaishi renders claims 1–4 of the '233 patent obvious. To the extent that the Patent Owner argues that a single embodiment of Takaishi does not disclose all the limitations of any of claims 1–4, a POSITA would have found claims 1-4 obvious, in view of the POSITA's own knowledge and/or the disclosures provided by Takaishi's other embodiments as explained herein.

124. It is noted that while the discussion below mainly focuses on the two left semiconductor pillars 5 of FIG. 2 of Takaishi, the analysis similarly applies to each silicon pillar 5.

125. Furthermore, while the cross-section view of FIG. 1 of Takaishi shows only the bottom two semiconductor pillars 5 of FIG. 2 of Takaishi, the description related to FIG. 1 applies to each of the semiconductor pillars 5 of FIG. 2, unless specified otherwise below.

1. Summary of Takaishi

126. U.S. App. Pub. No. 2009/0,085,102 to Takaishi ("Takaishi") is directed to a "semiconductor device having vertical surrounding gate transistor structure." EX1007, Takaishi, Title. Takaishi describes "[a] semiconductor device is provided which includes: semiconductor pillars which include impurity diffused layers, each semiconductor pillar having a width which allows full depletion of a

semiconductor forming each semiconductor pillar, the impurity diffused layers being electrically connected to each other; and a common gate section which covers side faces of the pillars.” EX1007, Takaishi, Abstract.

127. Takaishi acknowledges that “transistors having a three-dimensional structure have been investigated as a measure of refining transistors.” EX1007, Takaishi, [0005]. Takaishi recognizes various issues related to transistors having a three-dimensional structure. For example, Takaishi provides that “[w]hen the gate length of a transistor is extremely small, the influence of the short channel effect increases and it becomes difficult to control the threshold voltage of the transistor.” EX1007, Takaishi, [0008]. For further example, Takaishi provides that “[t]he drain current of transistors employing a silicon pillar is proportional to the diameter of the silicon pillar which forms the channel. The drain current can be increased by increasing the diameter of the silicon pillar. However, if the diameter of the silicon pillar is increased, the transistors are unable to be fully depleted, so that the characteristics of the transistors are deteriorated drastically. Thus, the drain current of fully depleted transistors employing a silicon pillar is limited. When a large drain current is required, the threshold voltage is increased instead of increasing the diameter of the silicon pillar so as to prevent the S value from being deteriorated. In addition, since the influence of the short channel effect becomes significant, it is necessary to, for example, change the profile of the diffused layers

129. Takaishi provides that with such a semiconductor device including semiconductor pillars having a common gate section and impurity diffused layers electrically connected to each other, “characteristics equal to those of a structure in which a plurality of unit transistors are arranged in parallel can be obtained.” EX1007, Takaishi, [0013]. Specifically, “even if each semiconductor pillar is thinned to a width which allows full depletion of the semiconductor forming each semiconductor pillar, it is possible to increase the drain current of the transistor without increasing the threshold voltage so as to prevent the S value from being deteriorated and without changing the profile of diffused-layers of the source and the drain taking the influence of the short channel effect into consideration.” EX1007, Takaishi, [0013]. Takaishi provides that with this structure, “it becomes possible to avoid influences due to an increase in width of each pillar (e.g., a drastic deterioration in the S value as a result of the semiconductor forming the pillars being not fully depleted, an influence of the short channel effect as a result of the influence of the source and the drain becoming remarkable, etc.) as well as influences by changing the profile of the diffused layers (e.g., a reduction in drain current due to an increase in resistance of the diffused-layers of the source and the drain). Thus, even in semiconductor devices which operate at a low voltage, a satisfactory (small) S value and a large drain current can be obtained while maintaining the characteristics of fully depleted transistors. Therefore, it is possible

to **realize miniaturized, quickly responsive, and low power consumption semiconductor devices.**” EX1007, Takaishi, [0015].

130. As detailed below, Takaishi teaches each element of Challenged Claims of the '233 patent, e.g., by the first embodiment of Takaishi (as described with reference to FIGS. 1 and 2). The description below refers to Takaishi's first embodiment (including but not limited to the example of FIGS. 1 and 2) unless provided otherwise. A POSITA would have understood that the first embodiment of Takaishi is not limited to the examples illustrated in its figures. *See, e.g.,* Takaishi, [0040] (“It is noted that FIG. 2 shows **an example** in which four silicon pillars 5, each having a rectangular cross section in the XY plane, are arranged in a matrix with two rows in the X direction and two columns in the Y direction. However, the shape, the number, and the arrangement of the silicon pillars 5 are **not limited to those of this example.**”). To the extent that Patent Owner argues that the first embodiment of Takaishi does not explicitly disclose certain limitations, as discussed in detail below, a POSITA would have understood that the limitations are at least rendered obvious by Takaishi in view of a POSITA's knowledge and/or other embodiments of Takaishi.

131. Furthermore, FIG. 1 of Takaishi “is a cross-sectional view of a part of a semiconductor device in accordance with a first embodiment of the present invention taken along a line X-X shown in FIG. 2.” EX1007, Takaishi, [0019]. As

such, FIG. 1 of Takaishi does not show all four silicon pillars of FIG. 2, and instead only shows the bottom two silicon pillars of FIG. 2. A POSITA would have understood that the discussion below referring to FIG. 1 (showing only two silicon pillars 5) applies to each of the semiconductor pillars (e.g., all four semiconductor pillars 5 of the example of FIG. 2) of the first embodiment of Takaishi.

2. Claim 1

[1.0] *A semiconductor device comprising:*

132. To the extent that this preamble is deemed limiting, Takaishi discloses or renders obvious a semiconductor device.

133. Specifically, Takaishi teaches a “**semiconductor device** having vertical surrounding gate transistor structure.” EX1007, Takaishi, Title. Takaishi describes that “[a] **semiconductor device** is provided which includes: semiconductor pillars which include impurity diffused layers, each semiconductor pillar having a width which allows full depletion of a semiconductor forming each semiconductor pillar, the impurity diffused layers being electrically connected to each other; and a common gate section which covers side faces of the pillars.” EX1007, Takaishi, Abstract; EX1007, Takaishi, FIGS. 1 and 2 (providing a cross-sectional view and a plan view of a part of a semiconductor device respectively); Takaishi, claims 1-19 (claiming a semiconductor device including semiconductor

pillars).

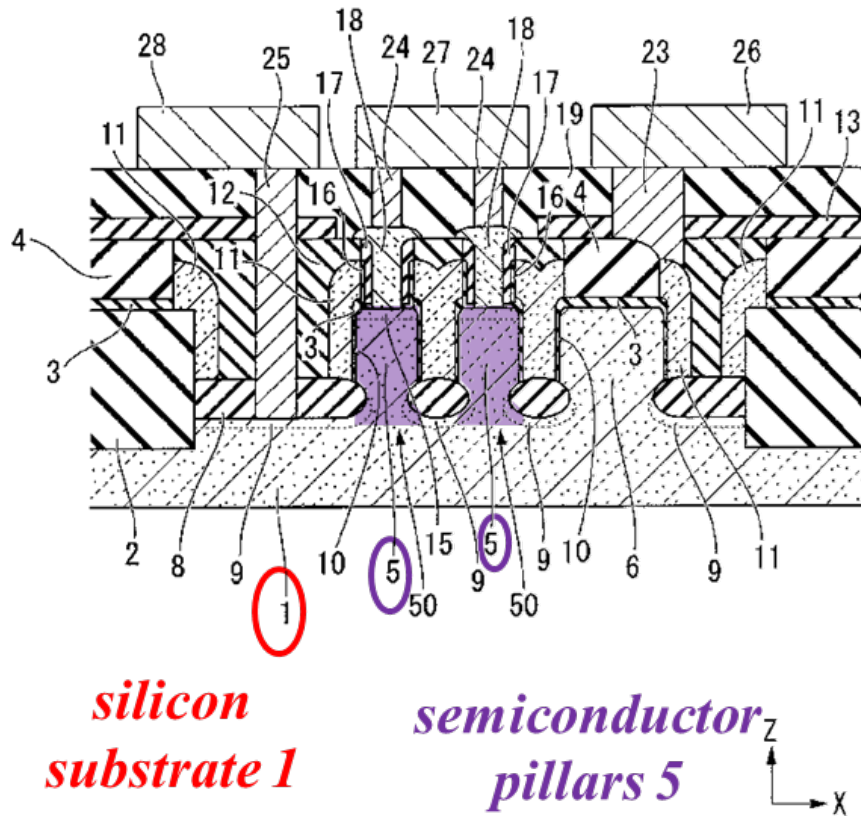
134. Therefore, Takaishi discloses or renders obvious a semiconductor device including semiconductor pillars with a common gate section, which teaches “*a semiconductor device*,” as recited in the claim.

[1.1] *a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region;*

135. Takaishi discloses or renders obvious that the semiconductor device includes a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region.

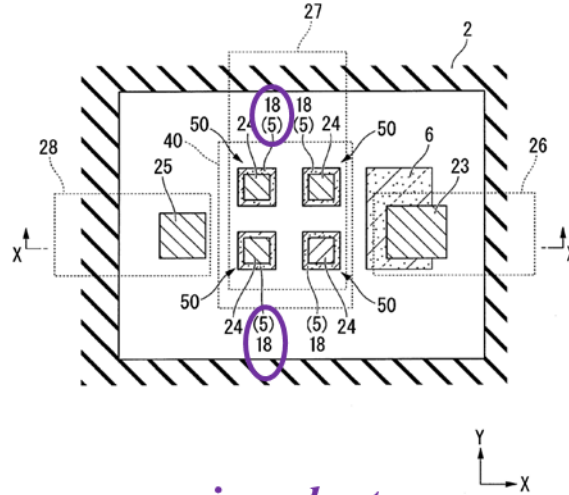
136. Specifically, as shown in annotated FIGS. 1 and 2 below, Takaishi describes that the semiconductor device includes a plurality of semiconductor pillars (semiconductor pillars 5) provided to stand from a semiconductor substrate (semiconductor substrate 1), each of the semiconductor pillars (semiconductor pillars 5) comprises a channel region. While the cross-section view of FIG. 1 of Takaishi shows the only the bottom two semiconductor pillars 5 of FIG. 2 of Takaishi, the description related to FIG. 1 applies to each of the semiconductor pillars 5 of FIG. 2.

FIG. 1



EX1007, Takaishi, FIG. 1, annotated

FIG. 2



*semiconductor
pillars 5*

EX1007, Takaishi, FIG. 2, annotated

137. First, Takaishi teaches that the semiconductor device includes a plurality of semiconductor pillars (semiconductor pillars 5) provided to stand from a semiconductor substrate (semiconductor substrate 1). Referring to FIG. 1, Takaishi describes that “FIG. 1 is a schematic view showing the cross section of the structure of a semiconductor device in accordance with a first embodiment of the present invention.” EX1007, Takaishi, [0026]. Takaishi describes that “shallow ranch isolation (STI) 2, which functions as a trench for separating semiconductor devices, is provided in a **silicon substrate 1 (a semiconductor substrate).**” EX1007, Takaishi, [0026]. A semiconductor device in silicon substrate 1 is provided, which includes “[a] **plurality of silicon pillars (semiconductor pillars) 5** [] provided **in a standing manner** around the center of

an area surrounded by the STI 2” in silicon substrate 1. EX1007, Takaishi, [0026];
see also EX1007, Takaishi, claim 1 (“A semiconductor device comprising:
semiconductor pillars which include impurity diffused layers...”).

138. It is noted that while FIGS. 1 and 2 illustrate an example of the first embodiment of Takaishi, the first embodiment of Takaishi is not limited to the example of FIG. 2, which “shows an example in which four silicon pillars 5, each having a rectangular cross section in the XY plane, are arranged in a matrix with two rows in the X direction and two columns in the Y direction.” EX1007, Takaishi, [0040]. As explained by Takaishi, “**the shape, the number, and the arrangement of the silicon pillars 5 are not limited to those of this example.** For instance, the shape of the cross section of the silicon pillars 5 in the XY plane may be a circle, or a polygon other than a rectangle. Moreover, when forming a large number of silicon pillars 5, these silicon pillars 5 may be arranged in a honeycomb-shape to form a closed packing structure, thereby making it possible to realize **miniaturized and highly integrated semiconductor devices.**” EX1007, Takaishi, [0040].

139. Additionally, while the discussion and annotation mainly focus on the two left silicon pillars 5 in FIG. 2, the analysis similarly applies to each silicon pillar 5.

140. Second, Takaishi teaches that each of the semiconductor pillars

comprise a channel region. Specifically, Takaishi describes that “[e]ach silicon pillar 5 is a semiconductor layer having a pillar shape **which forms a channel** and parts of a source section and a drain section of each unit transistor 50.” EX1007, Takaishi, [0026]. As shown in the example of FIG. 1 of Takaishi, “[t]he silicon pillars 5 have the same height and are arranged in parallel with each other,” and “[e]ach silicon pillar 5 has a width (i.e., the size of the cross-section thereof in a plane parallel to the silicon substrate 1) which allows full depletion of a semiconductor which forms each silicon pillar 5 (i.e., **the channel of each unit transistor 50**).” EX1007, Takaishi, [0026]. Takaishi describes that “[a]n intermediate portion of each silicon pillar 5 which is interposed between each upper diffused layer 15 and the lower diffused layer 9 is **the channel of each unit transistor 50**.” EX1007, Takaishi, [0027]; *see also* EX1007, Takaishi, claim 13 (“The semiconductor device as recited in claim 9, wherein the semiconductor device is a single transistor which includes unit transistors, and the **pillars include channels of the unit transistors**.”); EX1007, Takaishi, claim 14 (“wherein the **channels are intermediate portions of the pillars** which are interposed between the first impurity diffused layer and the second impurity diffused layers”).

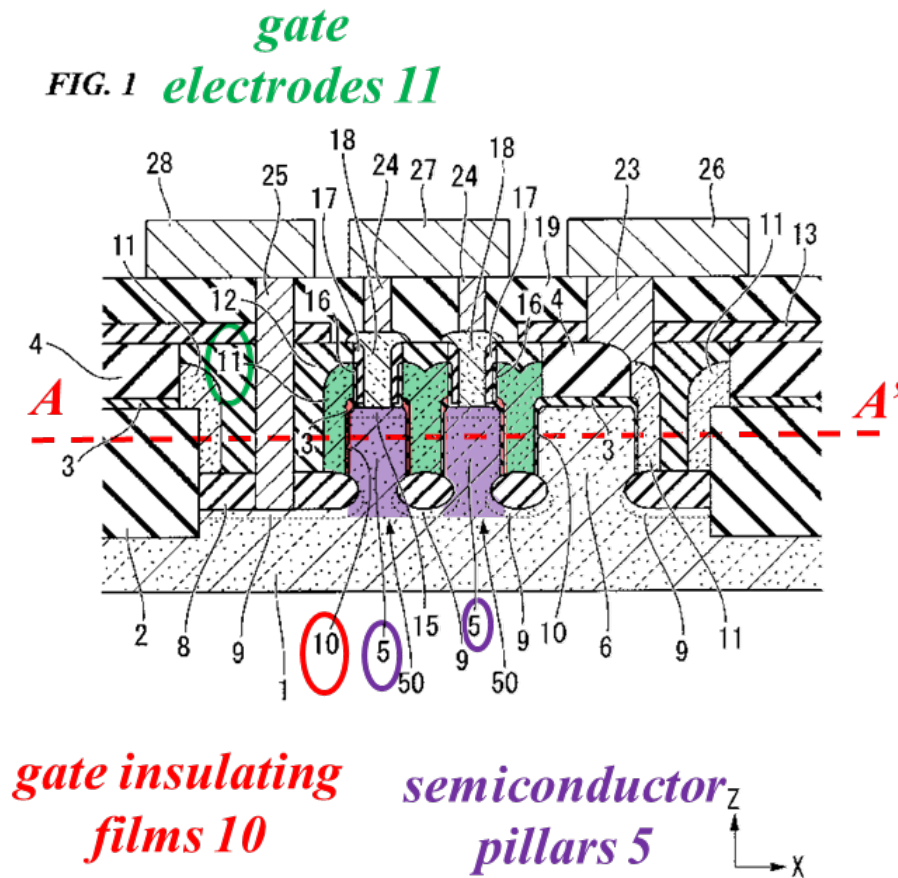
141. Therefore, Takaishi teaches that a semiconductor device includes a plurality of semiconductor pillars (semiconductor pillars 5) provided to stand from a semiconductor substrate (semiconductor substrate 1), each of the semiconductor

pillars (semiconductor pillars 5) comprises a channel region (between upper diffused layer 15 and lower diffused layer 9), which discloses or renders obvious “*a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region,*” as recited in the claim.

[1.2] *a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars;*

142. Takaishi discloses or renders obvious that the semiconductor device includes a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars.

143. Specifically, as shown in annotated FIG. 1 below, Takaishi describes that the semiconductor device includes a gate insulating film (gate insulating film 10) and a gate electrode (gate electrode 11) provided over a side surface of each of the semiconductor pillars (semiconductor pillars 5).



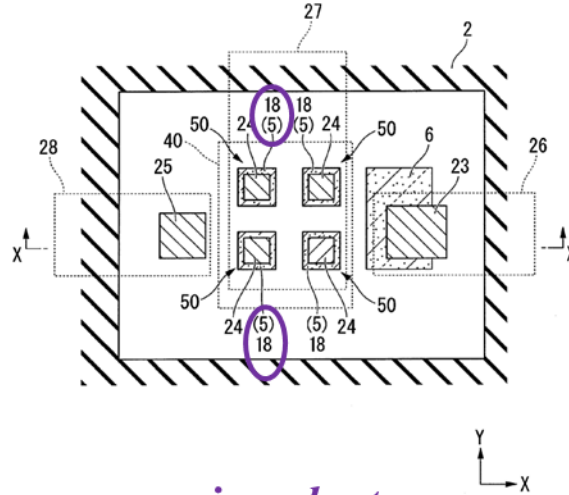
EX1007, Takaishi, FIG. 1, annotated

144. Referring to FIG. 1, Takaishi describes that “[g]ate insulating films 10 are formed on side faces of the silicon pillars 5 and the gate-lifting silicon pillar 6,” and that “[t]he gate electrodes 11 are formed over the surfaces of the silicon pillars 5 and the gate-lifting silicon pillar 6 with the gate insulating films 10 interposed therebetween.” EX1007, Takaishi, [0030]. Takaishi further provides, “[t]he gate insulating films 10 cover the outer periphery surfaces of the silicon pillars 5 and the gate-lifting silicon pillar 6, and are connected to the oxide film 8.” EX1007, Takaishi, [0030]. As such, “the channels of the silicon pillars 5, the

upper diffused layers 15, and the lower diffused layer 9 are electrically insulated from the gate electrodes 11 by means of the gate insulating films 10 and the oxide film 8.” EX1007, Takaishi, [0030]; *see also* EX1007, Takaishi, claim 2 (“The semiconductor device as recited in claim 1, wherein the gate section includes **gate electrodes which are formed over the side faces** of the pillars and contact each other.”); Takaishi, claim 16 (“The semiconductor device as recited in claim 1, further comprising **gate insulating films which are formed on the side faces of the pillars**, wherein the gate section covers the gate insulating films and fills a gap between the pillars.”)

145. Furthermore, FIG. 1 of Takaishi “is a cross-sectional view of a part of a semiconductor device in accordance with a first embodiment of the present invention taken along a line X-X shown in FIG. 2.” EX1007, Takaishi, [0019]. While FIG. 1 of Takaishi does not show all four silicon pillars of FIG. 2, and instead only shows the bottom two silicon pillars of FIG. 2, a POSITA would have understood that in Takaishi, a gate insulating film and a gate electrode are provided over a side surface of each of the semiconductor pillars of the semiconductor device, including those semiconductor pillars not shown in FIG. 1.

FIG. 2



*semiconductor
pillars 5*

EX1007, Takaishi, FIG. 2, annotated

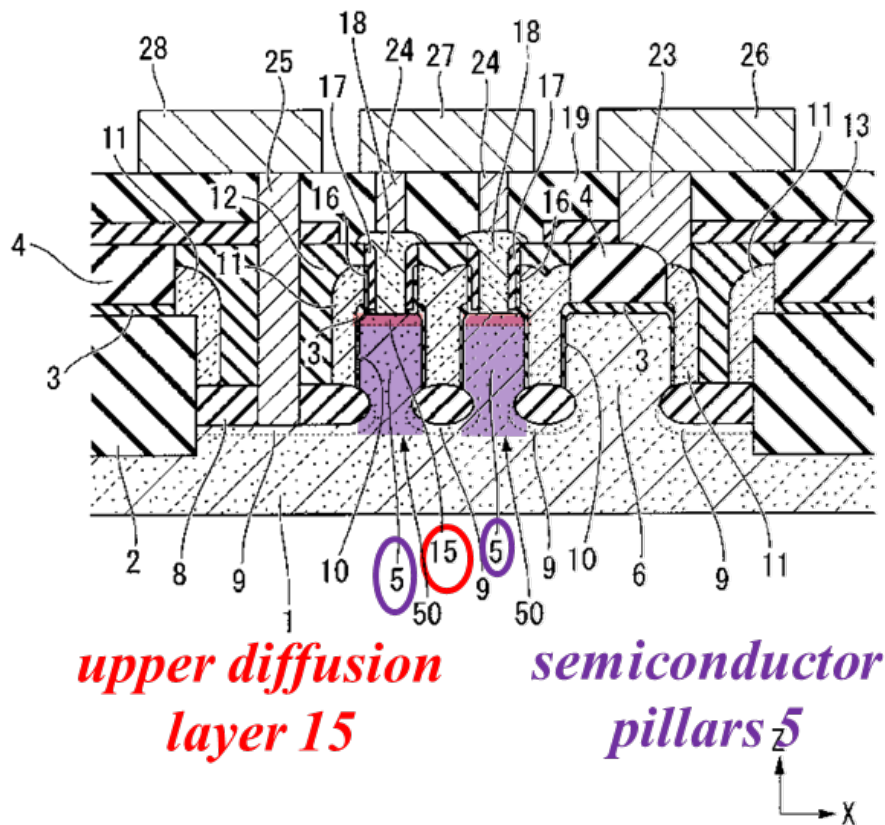
146. Therefore, Takaishi teaches that the semiconductor device includes a gate insulating film (gate insulating film 10) and a gate electrode (gate electrode 11) provided over a side surface of each of the semiconductor pillars (semiconductor pillars 5), which discloses or renders obvious “a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars,” as recited in the claim.

[1.3] *an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain;*

147. Takaishi discloses or renders obvious that the semiconductor device includes an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain.

148. Specifically, as shown in annotated FIG. 1 of Takaishi below, Takaishi describes that the semiconductor device includes an upper diffused layer 15 (upper diffusion layer) provided at an upper end of each of the semiconductor pillars 5 to serve as a source (one of a source and a drain).

FIG. 1



EX1007, Takaishi, FIG. 1, annotated

149. First, Takaishi teaches an upper diffusion layer provided at an upper end of each of the semiconductor pillars. Referring to FIG. 1, Takaishi describes “[p]illar upper diffused layers (hereinafter referred to as “**upper diffused layers**”)) **15**, which are second impurity diffused layers, are formed **at the upper end**

portions (second end portions) of the silicon pillars 5.” EX1007, Takaishi, [0027].

150. Second, Takaishi teaches that the upper diffusion layer serves as a source (one of a source and a drain). Referring to FIG. 1, Takaishi describes that “[s]ilicon plugs 18, which are third impurity diffused layers, are formed on the upper diffused layers 15,” and that “[t]he upper diffused layers 15 and the silicon plugs 18 are **source diffused-layers.**” EX1007, Takaishi, [0027]. Similarly, Takaishi describes that “[i]n conjunction with the upper diffused layers 15, the silicon plugs 18 form **source sections** of the unit transistors 50.” EX1007, Takaishi, [0034]. “Each silicon pillar 5 forms the channel and **parts of the source section** and the drain section of each unit transistor 50.” EX1007, Takaishi, [0036]; *see also* EX1007, Takaishi, claim 9 (“The semiconductor device as recited in claim 1, wherein the impurity diffused layers include: ... second impurity diffused layers which are provided at second end portions of the pillars...the second impurity diffused layers and the third impurity diffused layers **form source sections.**”).

151. While FIG. 1 of Takaishi does not show all four silicon pillars of FIG. 2, and instead only shows the bottom two silicon pillars of FIG. 2, a POSITA would have understood that in Takaishi, an upper diffusion layer is provided at an upper end of each of the semiconductor pillars of the semiconductor device to serve as a source, including those semiconductor pillars not shown in FIG. 1 (e.g.,

the top two silicon pillars of FIG. 2).

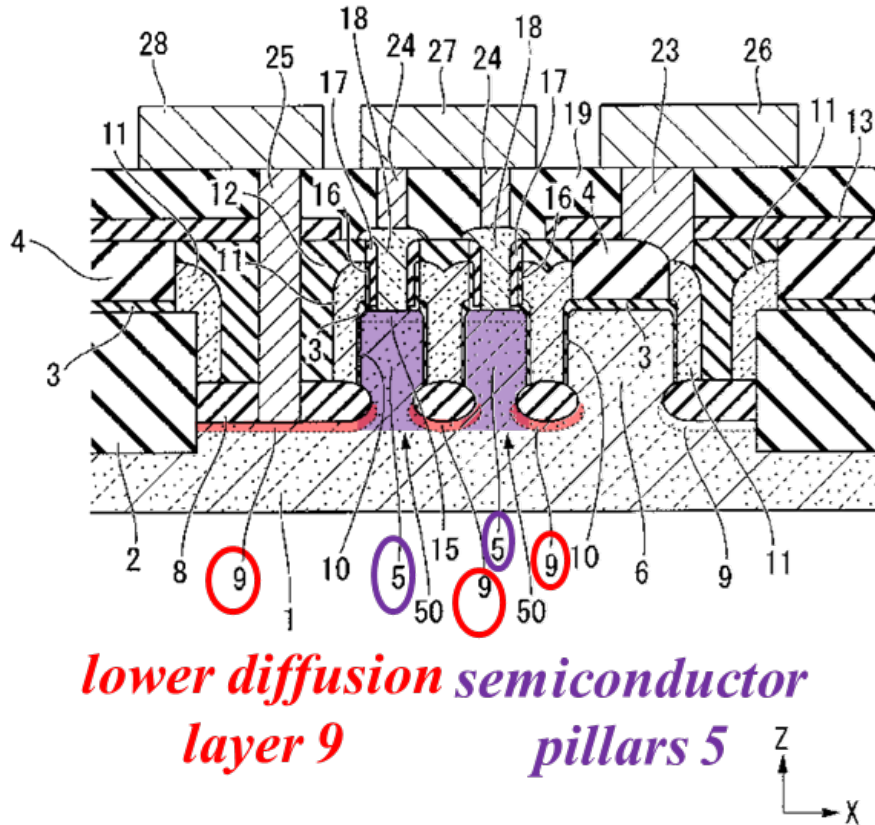
152. Therefore, Takaishi teaches that the semiconductor device includes an upper diffused layer 15 provided at an upper end of each of the semiconductor pillars 5 to serve as a source, which discloses or renders obvious “*an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain,*” as recited in the claim.

[1.4] *a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain; and*

153. Takaishi discloses or renders obvious that the semiconductor device includes a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain.

154. Specifically, as shown in annotated FIG. 1 of Takaishi below, Takaishi describes that the semiconductor device includes a lower diffused layer 9 (lower diffusion layer) operatively coupled to a lower end of each of the semiconductor pillars 5 to serve as a drain (the other of the source and the drain).

FIG. 1



EX1007, Takaishi, FIG. 1, annotated

155. First, Takaishi teaches a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars, because its lower diffused layer 9 is electronically connected to the lower end portions of the semiconductor pillars 5. Referring to FIG. 1, Takaishi describes that “[a] pillar lower diffused layer (hereinafter referred to as “lower diffused layer”) 9, which is a first impurity diffused layer, is formed at the lower end portions (first end portions) of the silicon pillars 5 and formed around the silicon pillars 5.” EX1007, Takaishi, [0027]. “The lower diffused layer 9 of each silicon pillar 5 extends over an area between the

silicon pillars 5, and connects to the lower diffused layer 9 of adjacent silicon pillars 5,” and as such, “the lower diffused layers 9 formed at the lower end portions of the silicon pillars 5 are electrically connected to each other.” EX1007, Takaishi, [0027].

156. Second, Takaishi teaches that a lower diffusion layer serves as the drain (the other of the source and the drain). Specifically, Takaishi describes that “[t]he lower diffused layer 9 formed at the lower end portions of the silicon pillars 5 and formed around the silicon pillars 5 are **drain** diffused-layers.” EX1007, Takaishi, [0027]; *see also*, EX1007, Takaishi, [0036] (“each silicon pillar 5 forms the channel and parts of the source section and **the drain section** of each unit transistor 50;” claim 9 (“The semiconductor device as recited in claim 1, wherein the impurity diffused layers include: **a first impurity diffused layer which is provided at first end portions of the pillars**; ... the first impurity diffused layer extends over an area between the pillars, and connects to the first impurity diffused layer of an adjacent silicon pillar to **form a common drain section**, and the second impurity diffused layers and the third impurity diffused layers form source sections.”).

157. While FIG. 1 of Takaishi does not show all four silicon pillars of FIG. 2, and instead only shows the bottom two silicon pillars of FIG. 2, a POSITA would have understood that in Takaishi, an upper diffusion layer is provided at an

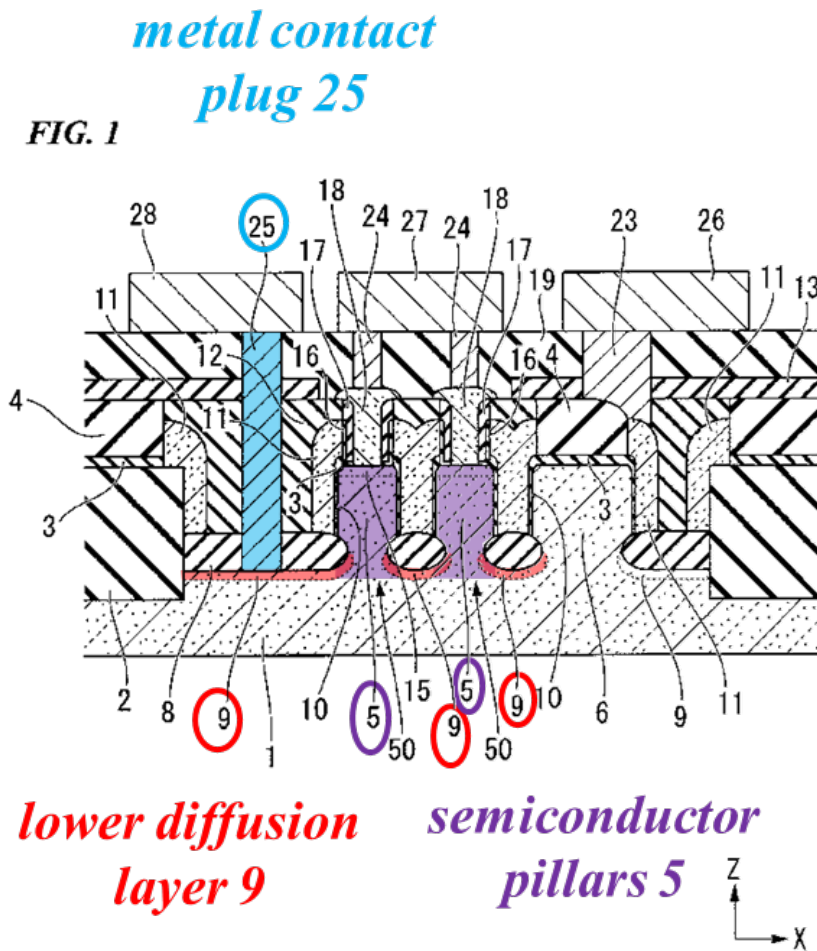
upper end of each of the semiconductor pillars of the semiconductor device to serve as a drain, including those semiconductor pillars not shown in FIG. 1 (e.g., the top two silicon pillars of FIG. 2).

158. Therefore, Takaishi teaches that the semiconductor device includes a lower diffused layer 9 operatively coupled to a lower end of each of the semiconductor pillars 5 to serve as a drain, which discloses or renders obvious “*a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain,*” as recited in the claim.

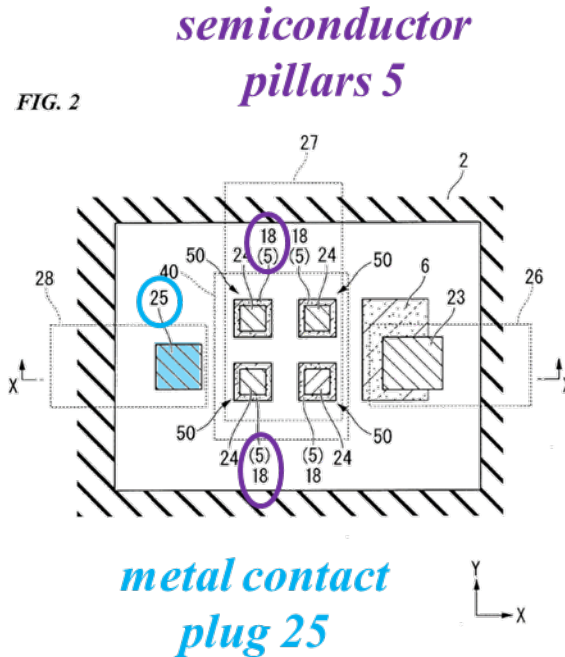
[1.5] *a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug, and;*

159. Takaishi discloses or renders obvious a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug.

160. Specifically, as shown in annotated FIGS. 1 and 2 of Takaishi below, Takaishi describes that the semiconductor device includes a metal contact plug 25 (lower diffusion layer side contact plug) connected to the lower diffused layer 9 (lower diffusion layer), wherein the semiconductor pillars 5 share the lower diffused layer 9 and the metal contact plug 25.



EX1007, Takaishi, FIG. 1, annotated



EX1007, Takaishi, FIG. 2, annotated

161. Referring to FIG. 1, Takaishi describes that “[t]he metal wire (a drain wire) 28 is connected to the lower diffused layer 9 through a **metal contact plug 25** (a third conductive plug),” and the metal contact plug 25 “penetrates the second interlayer insulating film 19, the mask oxide film 13, the first interlayer insulating film 12, and the oxide film 8” to connect to the lower diffused layer 9. EX1007, Takaishi, [0035]. In the example of FIG. 1, “[t]he metal contact plug 25 is formed at an intermediate area between the silicon pillars 5 and the STI 2 where no gate electrodes 11 are formed.” EX1007, Takaishi, [0035].

162. Referring to FIG. 2, which is a plan view of the semiconductor device of FIG. 1, Takaishi describes that the metal contact plug 25 is “formed on the

left...of the silicon pillar group.” EX1007, Takaishi, [0039]. Takaishi describes that “[t]he metal wire 28 is formed directly on the metal contact plug 25. The metal wire 28 is **connected to the lower diffused layers through the metal contact plug 25, and functions as a common drain wire of the unit transistors 50.**” EX1007, Takaishi, [0039]. As such, the metal wire 28 functions as a common drain wire through the metal contact plug 25 connected to the lower diffused layer 9, where the semiconductor pillars 5 share the lower diffused layer 9 and the metal contact plug 25. *See also* EX1007, Takaishi, claim 15 (“The semiconductor device as recited in claim 9, further comprising: **a third conductive plug which is connected to the drain section**; and a drain wire which is connected to the third conductive plug.”).

163. While FIG. 1 of Takaishi does not show all four silicon pillars of FIG. 2, and instead only shows the bottom two silicon pillars of FIG. 2, a POSITA would have understood that in Takaishi, all semiconductor pillars 5 of the semiconductor device share the lower diffused layer 9 and the metal contact plug 25, including those semiconductor pillars not shown in FIG. 1 (e.g., the top two silicon pillars of FIG. 2).

164. Therefore, Takaishi teaches a metal contact plug 25 (lower diffusion layer side contact plug) connected to the lower diffused layer 9 (lower diffusion layer), wherein the semiconductor pillars 5 share the lower diffused layer 9 and the

metal contact plug 25, which discloses or renders obvious “*a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug,*” as recited in the claim.

[1.6] *the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.*

165. Takaishi discloses or renders obvious that the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug. While the discussion and annotation mainly focus on the two left silicon pillars 5 in FIG. 2, the analysis similarly applies to each silicon pillar 5.

166. First, as shown in annotated FIG. 2 below, Takaishi describes that the semiconductor device includes semiconductor pillars 5 “arranged in a matrix” near the metal contact plug 25, and as such, teaches semiconductor pillars uniformly arranged near the metal contact plug 25 (lower diffusion layer side contact plug).

167. Referring to FIG. 2, Takaishi describes that “[t]he silicon pillars 5 having a rectangular cross section in the XY plane are provided around the center of an area surrounded by the STI 2. **The silicon pillars 5 are arranged in a matrix along the X direction and the Y direction.**” EX1007, Takaishi, [0036]. A POSITA would have understood that a matrix arrangement in circuit layout is a uniform arrangement, and as such, in the example of FIGS. 1 and 2 of the first



168. Second, to the extent that Patent Owner argues that “*uniformly arranged*” requires the distance configuration of the first embodiment of the ’233 patent (EX1001, ’233 patent, FIG. 1, 4:35-42), the first embodiment of Takaishi (including e.g. example of FIGS. 1 and 2 and examples A, B and C provided below) teaches this limitation as well.

Western Digital Exhibit 1003

provided by the '233 patent. Specifically, the '233 patent provides:

The unit transistors are uniformly arranged around the metal contact plug. 31. In the first embodiment, “uniformly arranged” represents an arrangement in which, in plan view, the distance between the metal contact plug 31 and a closest portion of the unit transistor farthest from the metal contact plug 31 is twice or less the distance between the metal contact plug 31 and a closest portion of the unit transistor closest to the metal contact plug 31.

EX1001, '233 patent, 4:35-42.

170. Referring to FIG. 1 of '233 patent as annotated below, the '233 patent describes:

With this configuration, as shown in FIG. 1, in the semiconductor device 100, the closest interval W1 between the outer periphery of the metal contact plug 31 and the second silicon pillar 5A can be set to twice or less the closest interval W2 between the outer periphery of the metal contact plug. 31 and the third silicon pillar 5A, i.e. the uniform arrangement can be achieved. In this case. W1 represents the maximum interval while W2 represents the minimum interval. That is, the maximum interval can be set to twice or less the minimum interval.

EX1001, '233 patent, 9:35-44.

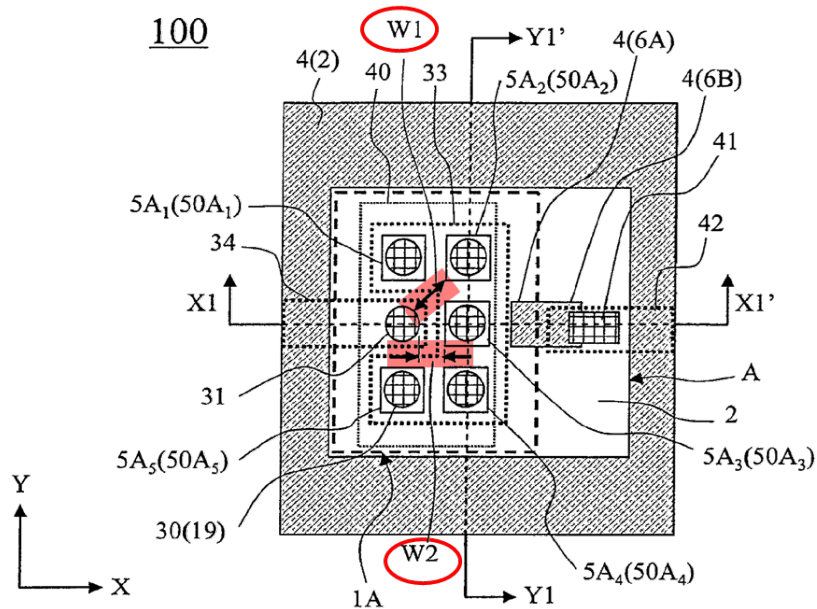
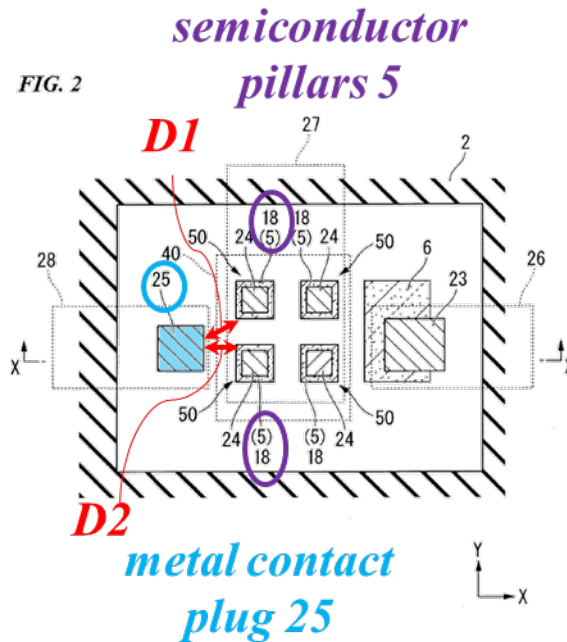


FIG. 1

EX1001, '233 patent, FIG. 1, annotated

171. Similar to the '233 patent, Takaishi teaches that a plurality of semiconductor pillars 5 have a uniform arrangement near the metal contact plug 25 (the lower diffusion layer side contact plug) similar to the example distance arrangement provided in the '233 patent.



EX1007, Takaishi, FIG. 2, annotated

172. For example, as shown in annotated FIG. 2 of Takaishi above, which is a plan view of the semiconductor device, the distance (D1) between the metal contact plug 25 and the top left semiconductor pillar 5 is twice or less the distance (D2) between the metal contact plug 25 and the bottom left semiconductor pillar 5. *See also* EX1007, Takaishi, [0036] (“[t]he silicon pillars 5 having a rectangular cross section in the XY plane are provided around the center of an area surrounded by the STI 2. The silicon pillars 5 are arranged in a matrix along the X direction and the Y direction.”). Further, it would have been obvious to a POSITA use such arrangements for all the semiconductor pillars for the benefit of “miniaturized and highly integrated semiconductor devices” with improved performance by providing similar electronics characteristics related to each semiconductor pillar.

EX1007, Takaishi, [0040].

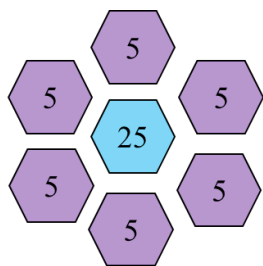
173. My analysis is not relied upon whether FIG. 2 of Takaishi is drawn to scale, and does not depend on actual dimensions of FIG. 2. Even if not drawn to scale and without any specific measurements regarding dimensions, a POSITA would have understood that FIG. 2 of Takaishi, together with Takaishi's description, reasonably depicts the important features of the device and the relative positions of the elements in the device, including the relative positions of the silicon pillars 5 and the vertical contact plug 25 and the relative distances D1 and D2 as discussed above.

174. Furthermore, as shown in plan views of examples A-C of the first embodiment of Takaishi, Takaishi teaches that semiconductor pillars 5 may have various arrangements for different design needs.

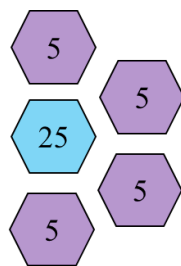
175. Specifically, Takaishi explicitly provides that "FIG. 2 shows an example in which four silicon pillars 5, each having a rectangular cross section in the XY plane, are arranged in a matrix with two rows in the X direction and two columns in the Y direction. **However, the shape, the number, and the arrangement of the silicon pillars 5 are not limited to those of this example [of FIG. 2].** For instance, the shape of the cross section of the silicon pillars 5 in the XY plane may be a circle, or a polygon other than a rectangle. Moreover, when forming a large number of silicon pillars 5, these silicon pillars 5 may be arranged

in a honeycomb-shape to form a closed packing structure, thereby making it possible to realize **miniaturized and highly integrated semiconductor devices.**”
EX1007, Takaishi, [0040].

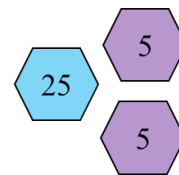
176. As shown in drawings below, I have included plan views of examples A-C of arrangement disclosed or rendered obvious by the first embodiment of Takaishi to realize miniaturized and highly integrated semiconductor devices. Each of the examples A-C teaches that a plurality of semiconductor pillars 5 of a semiconductor device as taught by the first embodiment of Takaishi are uniformly arranged near the metal contact plug 25 (the lower diffusion layer side contact plug) as claimed, at least because they have distance configurations similar to those of the first embodiment of the '233 patent (EX1001, '233 patent, FIG. 1, 4:35-42). A POSITA would have been motivated to use suitable pillar numbers and arrangements based on a particular design need (e.g., an arrangement with a larger number of semiconductor pillars for a higher current/power requirement).



**Example A of First
Embodiment of
Takaishi**



**Example B of First
Embodiment of
Takaishi**



**Example C of First
Embodiment of
Takaishi**

177. Example C is very similar to Fig. 2 of Takaishi except that only the

left two silicon pillars 5 are included, and the right two silicon pillars are eliminated. Example A is also similar to Fig. 2 of Takaishi except a honeycomb-shape as discussed in Takaishi is incorporated in Example A. As discussed in Takaishi, a honeycomb-shape arrangement would lead to formation of a closed packing structure, thereby making it possible to realize miniaturized and highly integrated semiconductor devices. For Example A, it would have been obvious to a POSITA to form metal line contacts to the contact plug 25 and to the silicon pillars 5 using two metal levels (a well-known multi-level metallization technology) in order to avoid metal wire shorting. Example B is similar to Example A except half of the honeycomb-shape arrangement is utilized. A POSITA would have been motivated to use suitable pillar numbers and arrangements based on a particular design need (e.g., an arrangement with a larger number of semiconductor pillars for a higher current/power requirement).

178. Furthermore, the prosecution history supports that Takaishi teaches this limitation. As discussed above in Prosecution History at V.B, during the prosecution of the parent of the '233 patent, Examiner relied on Takaishi to teach:

- “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug” as recited in claim 2 of the parent '125 App;
- “in plan view, a distance between the lower diffusion layer side

contact plug and the semiconductor pillar farthest from the lower diffusion layer side contact plug is twice or less a distance between the lower diffusion layer side contact plug and the semiconductor pillar closest to the lower diffusion layer side contact plug” of claim 4 of the parent ’125 App.

EX1006, ’125 App, 133-142; EX1010. Patent Owner did not dispute Takaishi’s teachings as relied by the Examiner. EX1006, ’125 App, 119-124.

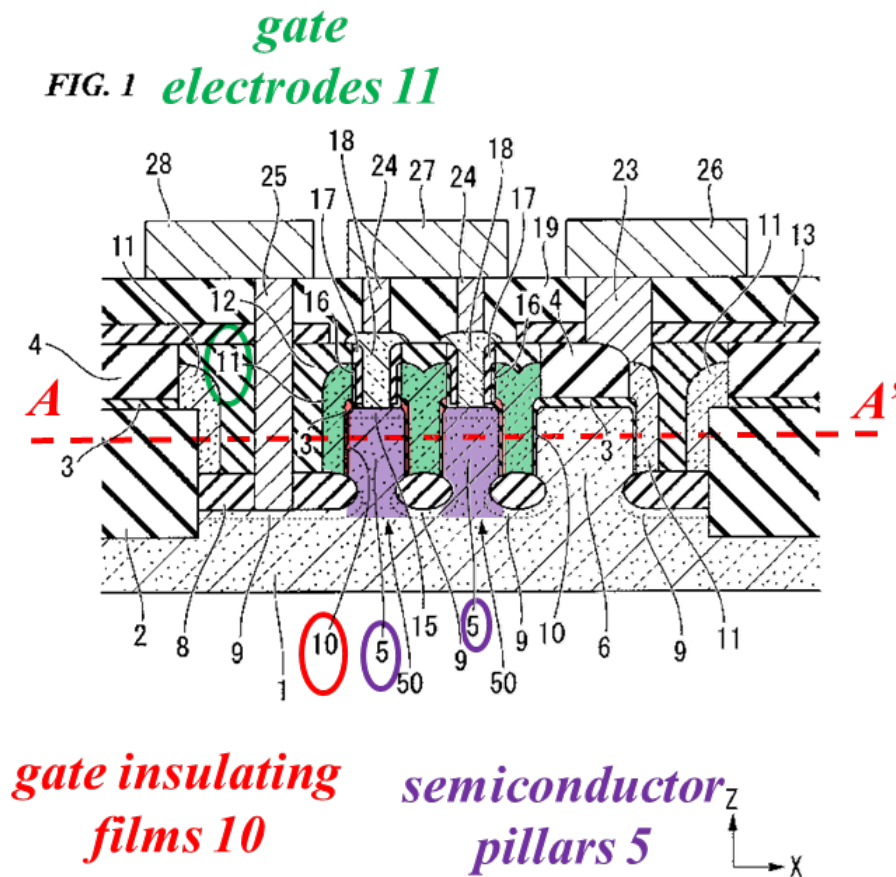
179. Therefore, Takaishi discloses or renders obvious that “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug,” as recited in the claim.

3. Claim 2

[2.1] *The semiconductor device according to claim 1, wherein the gate insulating film and the gate electrode are provided to surround the side surface of each of the semiconductor pillars.*

180. Takaishi discloses or renders obvious that the gate insulating film and the gate electrode are provided to surround the side surface of each of the semiconductor pillars.

181. As shown in annotated FIG. 1, Takaishi teaches that in the semiconductor device of FIG. 1, the gate insulating film 10 and the gate electrode 11 are provided to surround the side surface of each of the semiconductor pillars 5.

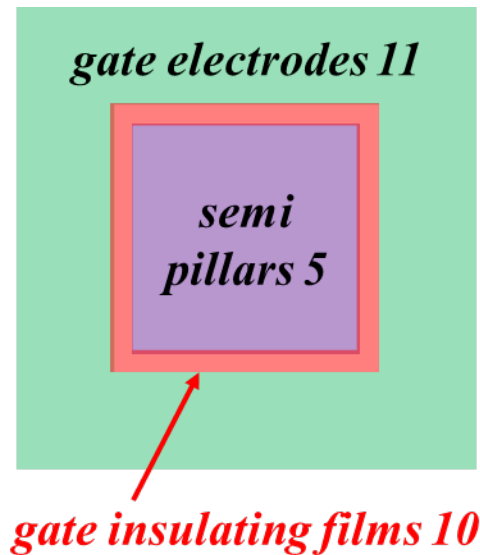


EX1007, Takaishi, FIG. 1, annotated

182. Specifically, Takaishi describes that “[g]ate insulating films 10 are formed on side faces of the silicon pillars 5 and the gate-lifting silicon pillar 6. The gate electrodes 11 are formed over the surfaces of the silicon pillars 5 and the gate-lifting silicon pillar 6 with the gate insulating films 10 interposed therebetween.” EX1007, Takaishi, [0030]. Takaishi further describes that “[t]he gate electrodes 11 are also formed on a part of the inner wall of the STI 2, the inner wall of an oxide film 3 which is stacked on the top face of the STI 2, and a part of

the inner wall of the mask nitride film 4 which is stacked on the top face of this oxide film 3. The gate insulating films 10 **cover the outer periphery surfaces of the silicon pillars 5** and the gate-lifting silicon pillar 6, and are connected to the oxide film 8. **The channels of the silicon pillars 5, the upper diffused layers 15, and the lower diffused layer 9 are electrically insulated from the gate electrodes 11 by means of the gate insulating films 10 and the oxide film 8.**”
EX1007, Takaishi, [0030].

183. A POSITA would have understood that Takaishi discloses or at least renders obvious that the gate insulating film and the gate electrode are provided to surround the side surface of each of the semiconductor pillars 5, and as a result, the semiconductor pillars 5 are electrically insulated from the gate electrodes 11 by the gate insulating films 10. Below I provide a drawing of a partial top view of each semiconductor pillar 5 of the semiconductor device of FIG. 1 along A-A' of FIG. 1, which illustrates a POSITA's understanding of the structure of the semiconductor device, where the gate insulating film 10 and the gate electrode 11 are provided to surround the side surface of each of the semiconductor pillars 5.

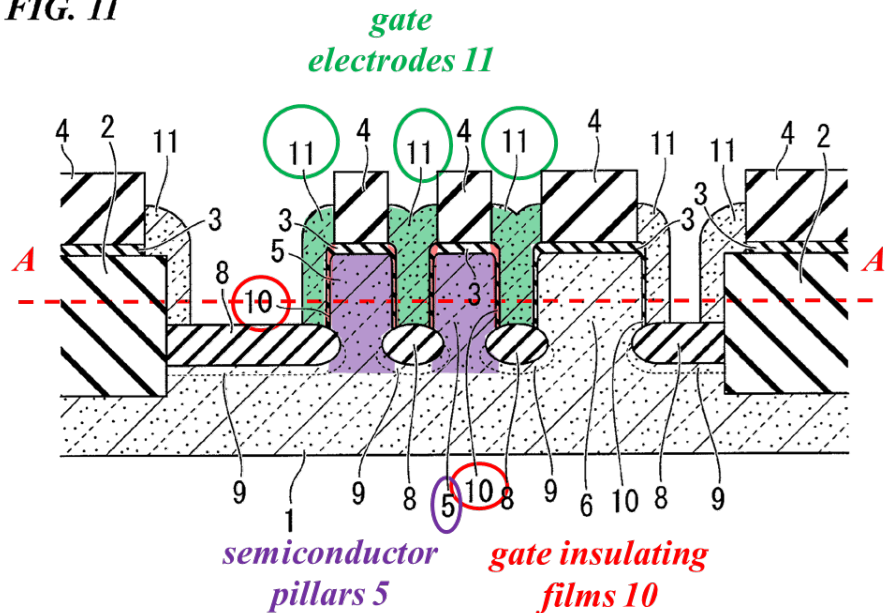


Partial Top View of Each Semiconductor Pillar 5

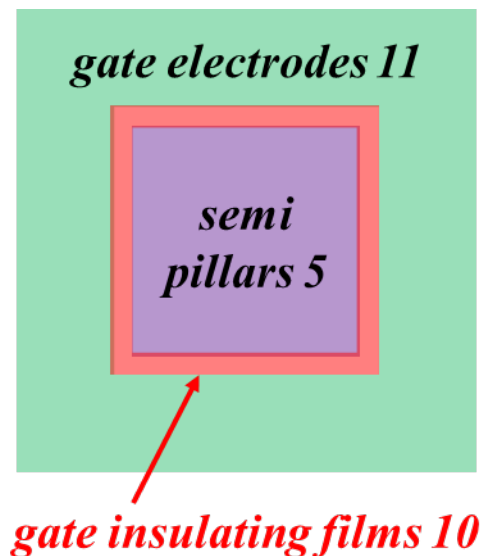
Along A-A' of EX1007, Takaishi, FIG. 1

184. Furthermore, as shown in annotated FIG. 11 of Takaishi below, during the process for manufacturing the semiconductor device shown in FIG. 1, Takaishi discloses or at least renders obvious that the gate insulating films 10 and gate electrodes 11 are provided to surround the side surface of each of the semiconductor pillars. For example, Takaishi describes that “as shown in FIG. 11, **gate insulating films 10 are formed** on the side faces of the silicon pillars 5 and the gate-lifting silicon pillar 6. When silicon oxide films are used as the gate insulating films 10, the thickness thereof is approximately 3 nm. Next, polysilicon of 20 nm in thickness is deposited over the entire surface, and the entire surface is etched back to **form the gate electrodes 11** over the side faces of the silicon pillars 5 and the gate-lifting silicon pillar 6.” EX1007, Takaishi, [0051].

FIG. 11



EX1007, Takaishi, FIG. 11, annotated



Partial Top View of Each Semiconductor Pillar 5

Along A-A' of EX1007, Takaishi, FIG. 11

185. As shown in the partial top view of each semiconductor pillar 5 along A-A' of FIG. 11 of Takaishi, a POSITA would have understood that the process of

forming the gate insulating films 10 that cover the outer periphery surfaces of the silicon pillars 5 as described in Takaishi teaches that gate insulating films 10 is provided to surround the silicon pillars 5. Furthermore, a POSITA would have understood that the process of etching the entire surface back to form the gate electrodes 11 over the side faces of the silicon pillars 5 as described in Takaishi teaches that the gate electrodes 11 is provided to surround the side surface of each of the semiconductor pillars, with the gate insulating films 10 interposing between the silicon pillars 5 and the gate electrodes 11.

186. Such processes for providing the gate insulating film and the gate electrode are provided to surround the side surface of each of the semiconductor pillars are consistent with the well-known knowledge of a POSITA. *See, e.g.*, EX1008, Endoh, FIGS. 1, 2(a), 2(b), 6, 7(a), 7(b), 3 (“the floating gate 6 [gate electrode] is formed on the side wall by relying on tunnel oxidation film 5 [gate insulating film] **by surrounding the pillar-shaped silicon layer 2**, in addition, control gate 8 is formed in the outside of it through layer dielectric film 7”).

187. Therefore, Takaishi discloses or renders obvious that “the gate insulating film and the gate electrode are provided to surround the side surface of each of the semiconductor pillars,” as recited in the claim.

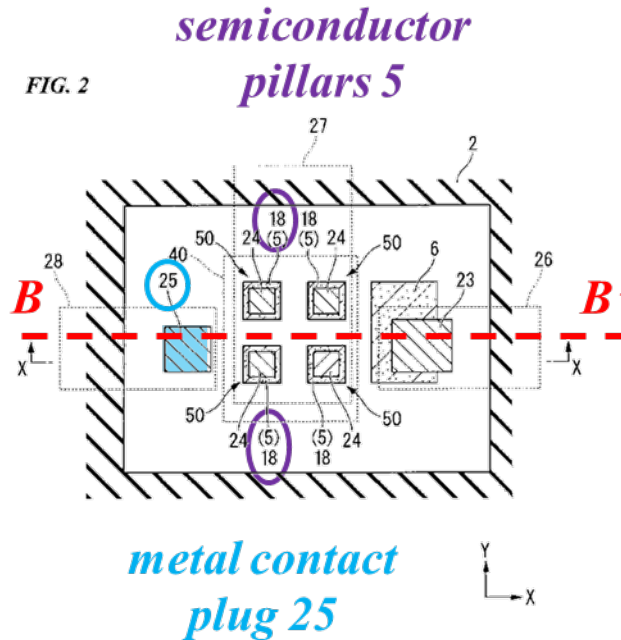
4. Claim 3

[3.1] *The semiconductor device according to claim 1, wherein the semiconductor pillars are uniformly arranged on at least two opposite sides of the lower diffusion layer side contact plug.*

188. Takaishi discloses or renders obvious that wherein the semiconductor pillars are uniformly arranged on at least two opposite sides of the lower diffusion layer side contact plug.

189. First, as shown in annotated FIG. 2 of Takaishi below, the semiconductor pillars are uniformly arranged on at least two opposite sides of the metal contact plug 25 (lower diffusion layer side contact plug), namely, the top side above line B-B' and the bottom side below line B-B'. EX1007, Takaishi, [0036] ("FIG. 2 is a plan view showing the structure of the semiconductor device shown in FIG.1. The silicon pillars 5 having a rectangular cross section in the XY plane are provided around the center of an area surrounded by the STI 2. **The silicon pillars 5 are arranged in a matrix along the X direction and the Y direction.**").

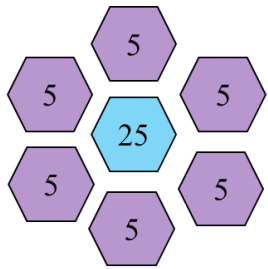
190. To the extent that Patent Owner argues that "*uniformly arranged*" requires the distance configuration of the first embodiment of the '233 patent ('233 patent, FIG. 1, 4:35-42), the two left silicon pillars 5 teach the "*plurality of semiconductor pillars*" as claimed, and are uniformly arranged on the two opposite sides of metal contact 5 (top and bottom sides of line B-B' of FIG. 2).



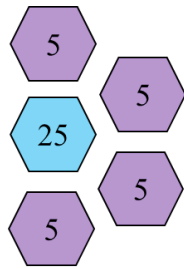
EX1007, Takaishi, FIG. 2, annotated

191. **Second**, the first embodiment of Takaishi, in addition to the example of FIGS. 1 and 2, teaches this limitation. Takaishi provides that “FIG. 2 shows an example in which four silicon pillars 5,” “[h]owever, the shape, the number, and the arrangement of the silicon pillars 5 are not limited to those of this example.” EX1007, Takaishi, [0040]. Takaishi describes examples of the first embodiment where “the shape of the cross section of the silicon pillars 5 in the XY plane may be a circle, or a polygon other than a rectangle,” and “when forming a large number of silicon pillars 5, these silicon pillars 5 may be arranged in a honeycomb-shape to form a closed packing structure, thereby making it possible to realize miniaturized and highly integrated semiconductor devices.” EX1007, Takaishi, [0040].

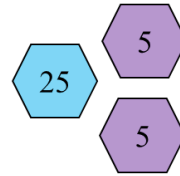
192. Furthermore, as discussed above at Ground 2: [1.6], as shown in the drawings below, a POSITO would have understood that the first embodiment of Takaishi discloses or at least renders obvious various arrangements to realize miniaturized and highly integrated semiconductor devices, including examples A-C below. Each of the examples A-C as taught by the first embodiment of Takaishi teaches that semiconductor pillars are uniformly arranged on at least two opposite sides (top and bottom sides) of the metal contact plug 25.



**Example A of First
Embodiment of
Takaishi**



**Example B of First
Embodiment of
Takaishi**



**Example C of First
Embodiment of
Takaishi**

193. Therefore, Takaishi discloses or renders obvious that “the semiconductor pillars are uniformly arranged on at least two opposite sides of the lower diffusion layer side contact plug,” as recited in the claim.

5. Claim 4

[4.1] *The semiconductor device according to claim 1, wherein the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug.*

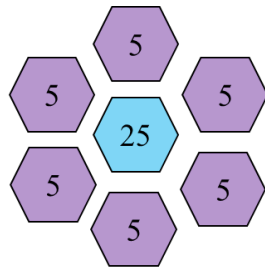
194. Takaishi discloses or renders obvious that the semiconductor pillars

are uniformly arranged so as to surround the lower diffusion layer side contact plug.

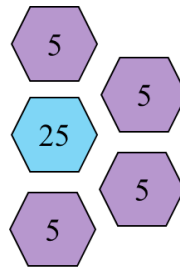
195. As discussed above at Ground 2:[1.6], the first embodiment of Takaishi, teaches this limitation. Takaishi provides that “FIG. 2 shows an example in which four silicon pillars 5,” “[h]owever, the shape, the number, and the arrangement of the silicon pillars 5 are not limited to those of this example.” EX1007, Takaishi, [0040]. Takaishi describes examples of the first embodiment where “the shape of the cross section of the silicon pillars 5 in the XY plane may be a circle, or a polygon other than a rectangle,” and “when forming a large number of silicon pillars 5, these silicon pillars 5 **may be arranged in a honeycomb-shape to form a closed packing structure**, thereby making it possible to realize **miniaturized and highly integrated semiconductor devices**.” EX1007, Takaishi, [0040].

196. As shown in drawings below, a POSITO would have understood that the first embodiment of Takaishi discloses or at least renders obvious various arrangements to realize miniaturized and highly integrated semiconductor devices, including example B below. Each of Examples A and B as taught by the first embodiment of Takaishi teaches that semiconductor pillars are uniformly arranged so as to surround the metal contact plug 25. *See also* EX1007, '233 patent, FIG. 1; EX1001, '233 patent, 6:21-23 (“In FIG. 1, the metal contact plug 31 is provided so

as to be **surrounded** by the five unit transistors arranged in the $\sqcap$ -shape.”).



**Example A of First
Embodiment of
Takaishi**



**Example B of First
Embodiment of
Takaishi**

197. Furthermore, the prosecution history supports that Takaishi teaches this limitation. As discussed above in Prosecution History at V.B, during the prosecution of the parent '125 App of the '233 patent, Examiner relied on Takaishi to teach:

- “the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug” of claim 3 of the parent '125 App.

EX1006, '125 App, 133-142; EX1010. Patent Owner did not dispute Takaishi's teachings as relied by the Examiner. EX1006, '125 App, 119-124.

198. Therefore, Takaishi discloses or renders obvious that “the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug,” as recited in the claim.

VIII. DECLARATION

199. I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: June 21, 2023



Jack C. Lee