

US9,379,233 Claims	App. No. 13/722,125 (Parent of '233 Patent) Pending Claims Rejected Over Takaishi (EX1006, '125 App, 136-160)	Issued Claims of App. No. 13/722,125 (US9,178,056)
1. A semiconductor device comprising: a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region; a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars; an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain; a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain; and a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug, and	1. (original) A semiconductor device comprising: a plurality of vertical transistors provided to stand from a semiconductor substrate and comprising a diffusion layer at their end portions on the semiconductor substrate side; and a conductive plug provided to stand from the semiconductor substrate and connected to the diffusion layer of the plurality of vertical transistors, wherein the plurality of vertical transistors are uniformly arranged near the conductive plug and share the diffusion layer and the conductive plug.	1. A semiconductor device comprising: a plurality of vertical transistors provided to stand from a semiconductor substrate and comprising a diffusion layer at their end portions on the semiconductor substrate side; a conductive plug provided to stand from the semiconductor substrate and connected to the diffusion layer of the plurality of vertical transistors, the plurality of vertical transistors being uniformly arranged near the conductive plug and sharing the diffusion layer and the conductive plug; and <u>a dummy pillar provided to stand from the semiconductor substrate and comprising, over a side surface of the dummy pillar, a power feed gate electrode connected to the gate electrodes of the plurality of vertical transistors.</u> [EX1006, 118

the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.	2. (original) The semiconductor device according to claim 1, wherein each vertical transistor comprises: a semiconductor pillar provided to stand from the semiconductor substrate and forming a channel; a gate insulating film and a gate electrode provided over a side surface of the semiconductor pillar; an upper diffusion layer provided at an upper end of the semiconductor pillar and serving as one of a source and a drain; and a lower diffusion layer provided at a lower end of the semiconductor pillar and serving as the other of the source and the drain, the conductive plug is a lower diffusion layer side contact plug connected to the lower diffusion layer, the plurality of vertical transistors share the lower diffusion layer and the lower diffusion layer side contact plug, and	(Amendment to overcome 102 rejection over US 2009/0085102 to Takaishi (EX1007)) 2. The semiconductor device according to claim 1, wherein each vertical transistor comprises: a semiconductor pillar provided to stand from the semiconductor substrate and forming a channel; a gate insulating film and a gate electrode provided over a side surface of the semiconductor pillar; an upper diffusion layer provided at an upper end of the semiconductor pillar and serving as one of a source and a drain; and a lower diffusion layer provided at a lower end of the semiconductor pillar and serving as the other of the source and the drain, the conductive plug is a lower diffusion layer side contact plug connected to the lower diffusion layer, the plurality of vertical transistors share the lower diffusion layer and the lower diffusion layer side contact plug, and
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	the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.	the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.
2. The semiconductor device according to claim 1, wherein the gate insulating film and the gate electrode are provided to surround the side surface of each of the semiconductor pillars.		
3. The semiconductor device according to claim 1, wherein the semiconductor pillars are uniformly arranged on at least two opposite sides of the lower diffusion layer side contact plug.	3. (original) The semiconductor device according to claim 2, wherein the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug. 5. (original) The semiconductor device according to claim 2, wherein the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug in a Π-shape in plan view.	4. The semiconductor device according to claim 2, wherein the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug. 6. The semiconductor device according to claim 2, wherein the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug in a Π shape in plan view.
4. The semiconductor device according to claim 1, wherein the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug.	3. (original) The semiconductor device according to claim 2, wherein the semiconductor pillars are uniformly arranged so as to surround	4. The semiconductor device according to claim 2, wherein the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug.

	the lower diffusion layer side contact plug. 4. (original) The semiconductor device according to claim 2, wherein, in plan view, a distance between the lower diffusion layer side contact plug and the semiconductor pillar farthest from the lower diffusion layer side contact plug is twice or less a distance between the lower diffusion layer side contact plug and the semiconductor pillar closest to the lower diffusion layer side contact plug. 5. (original) The semiconductor device according to claim 2, wherein the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug in a Π-shape in plan view.	5. The semiconductor device according to claim 2, wherein, in plan view, a distance between the lower diffusion layer side contact plug and the semiconductor pillar farthest from the lower diffusion layer side contact plug is twice or less a distance between the lower diffusion layer side contact plug and the semiconductor pillar closest to the lower diffusion layer side contact plug. 6. The semiconductor device according to claim 2, wherein the semiconductor pillars are uniformly arranged so as to surround the lower diffusion layer side contact plug in a Π shape in plan view.
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