

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

Case IPR2023-01123
Patent 9,379,233

PATENT OWNER'S PRELIMINARY RESPONSE

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Rules

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I. Introduction

Neither of the Petition's two grounds demonstrates a reasonable likelihood of prevailing on demonstrating invalidity of any claim of the '233 Patent.

The Petition's first ground is based on the unsupported premise that the primary reference Endoh has a "need" to connect a structure near the bottom of its semiconductor device to a "common source line (CSL)" that is allegedly "above the top of the semiconductor pillars)." Pet. at 46. Based on that supposed "need," the Petition asserts that a POSITA would have been motivated to combine Endoh with secondary reference Hwang. *See* Pet. at 46. Despite the Petition's Ground 1 motivation resting on that specific "need," however, the Petition identifies *no* evidence or analysis supporting the conclusion that Endoh teaches (or renders obvious) a common source line above the top of the semiconductor pillars. Because the Petition fails to set forth evidence supporting its purported motivation to combine, the Petition's first ground fails to set forth a prima facie case of obviousness.

The Petition's second ground also fails, because the Petition cannot show that what it identifies as the "semiconductor pillars" of the claim are "uniformly arranged near the... contact plug" as recited by limitation [1.6]. The Petition attempts to cure this deficiency with various "examples" (which are figures designed by Petitioner and/or its expert) of how a POSITA allegedly could have modified Takaishi to arrive

at the “uniformly arranged” limitation, but the Petition does not identify any purported *motivation* to implement those modifications that would have been recognized by a POSITA before the invention of the ’233 Patent. Even worse, the Petition’s proposed modifications to Takaishi violate the design principles articulated in Takaishi itself, such that a POSITA would have avoided implementing the “examples” that Petitioner was able to devise with the benefit of hindsight.

Accordingly, institution should be denied.

II. Background

A. Western Digital’s Petition

Petitioner Western Digital Technologies, Inc. (“Petitioner” or “Western Digital”) challenges claims 1-4 of U.S. Patent No. 9,379,233 (the “’233 Patent”). Petitioner structures its two asserted grounds for unpatentability as follows:

- Ground 1: Obviousness of claims 1-3 over Endoh in view of Hwang.
- Ground 2: Obviousness of claims 1-4 over Takaishi.

Because all challenged dependent claims across both grounds depend from claim 1, this Preliminary Response need only address the Petition’s arguments concerning claim 1. If the Petition does not show a reasonable likelihood of prevailing on claim 1, then it cannot prevail on any other challenged claim.

B. Overview of the '233 Patent

At a high level, the '233 Patent is directed generally to novel semiconductor devices with vertical transistors, which solve the problem of “variation in characteristics of transistors” by ensuring that the “vertical transistors are uniformly arranged” near an electrically conductive contact plug. *See generally* Ex. 1001 at 1:50-2:48.

The '233 Patent states: “in order to obtain a high current drive capability while maintaining the transistor characteristics, a vertical transistor type semiconductor device may be provided with a plurality of semiconductor pillars.” The '233 Patent recognizes a problem that may arise in such a configuration, however: “electrical resistances between a lower contact plug, which is connected to the lower diffusion layers, and the semiconductor pillars largely differ depending on connecting positions between the lower diffusion layers and the lower contact plug.” *Id.* at 1:63-2:1. The '233 Patent states that this “variation in characteristics of transistors provided to the semiconductor pillars” arises when “the *maximum* interval between the semiconductor pillar and lower contact plug becomes more than twice the

minimum interval between the semiconductor pillar and the lower contact plug in plan view.” *Id.* at 1:63-2:6.¹

In order to “stabilize the characteristics of the transistors” and thus solve this problem of electrical variation between transistors, the ’233 Patent describes a number of arrangements wherein the transistors/semiconductor pillars “are uniformly arranged near” the conductive/contact plug. *Id.* at 2:7-48. The ’233 Patent makes clear that in order to be “uniformly arranged” near the contact plug and overcome the problems identified in prior art solutions, the “maximum interval between the metal contact plug” and the pillars “is twice or less the minimum interval between the metal contact plug” and the pillars. *Id.* at 12:40-46 (“[I]t is satisfactory if the silicon pillars 5 are uniformly arranged with respect to the metal contact plug 31, i.e. the maximum interval between the metal contact plug 31 and the silicon pillar 5 is twice or less the minimum interval between the metal contact plug 31 and the silicon pillar 5.”); *see also id.* at 6:57-65 (“In this case, since the maximum interval (57 nm) is twice or less the minimum interval (35 nm), it is possible to avoid the prior art problem....”); *id.* at 9:35-44 (“[T]he uniform arrangement can be achieved” when “the maximum interval [is] set to twice or less

¹ All emphases herein are added unless otherwise specified.

the minimum interval. Consequently, it is possible to avoid the prior art problem that the intervals... become non-uniform so that parasitic resistances... differ from each other....”).

This solution to the prior art problem of a lack of uniformity in vertical transistor design is reflected, for example, in claim 1 of the '233 Patent, which recites:

1. A semiconductor device comprising:
 - a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region;
 - a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars;
 - an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain;
 - a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain; and
 - a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein
- the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug, and
- the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.*

Ex. 1001 at claim 1. All other challenged claims 2-4 depend from claim 1.

III. Level of Ordinary Skill in the Art

The Petition proposes that a person of ordinary skill in the art in the field of the '233 Patent “would have a bachelor’s or the equivalent degree in electrical engineering or a related field and 2-3 years of professional experience relating to semiconductor device design and fabrication.” Pet. at 9. For purposes of this preliminary response, Patent Owner does not challenge that definition.

IV. Claim Construction

Patent Owner proposes construction of a single claim term—“the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug”—because the '233 Patent specification expressly defines what it means for semiconductor pillars to be “uniformly arranged” with respect to a contact plug.

Specifically, the '233 Patent defines pillars being uniformly arranged with respect to a contact plug as meaning that “the maximum interval between the metal contact plug 31 and the silicon pillar[s] 5 is twice or less the minimum interval between the metal contact plug and the silicon pillar[s] 5.” See Ex. 1001 at 12:40-46 (“[I]t is satisfactory if the silicon pillars are *uniformly arranged* with respect to the metal contact plug 31, *i.e. the maximum interval* between the metal contact plug 31 and the silicon pillar 5 *is twice or less the minimum interval* between the metal contact plug 31 and the silicon pillar 5.”); see also *id.* at 4:35-42 (“The unit

transistors are uniformly arranged around the metal contact plug 31. In the first embodiment, ‘uniformly arranged’ represents an arrangement in which, in plan view, the distance between the metal contact plug 31 and a closest portion of the unit transistor farthest from the metal contact plug 31 is twice or less the distance between the metal contact plug 31 and a closest portion of the unit transistor closest to the metal contact plug 31.”).

The definition of “uniformly arranged” in the specification (using “i.e.,” as a definitional indicator) is precisely the type of definitional language that creates lexicography under Federal Circuit precedent. *See, e.g., SkinMedica, Inc. v. Histogen Inc.*, 727 F.3d 1187, 1200 (Fed. Cir. 2013) (“In a specification, a patentee's “use of ‘i.e.’ signals an intent to define the word to which it refers.”) (quoting *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1334 (Fed. Cir. 2009)); *Caritas Techs., Inc. v. Comcast Corp.*, No. 2:05-CV-339-DF, 2006 WL 6112191, at *16 (E.D. Tex. Oct. 18, 2006) (“The use of ‘i.e’ means that the patentee has ‘chosen to be his own lexicographer....’”) (applying the reasoning of *Abbott Labs. v. Novopharm Ltd.*, 323 F.3d 1324, 1327, 1330 (Fed. Cir. 2003), which held that the use of “i.e.” “explicitly defined” the claim term in question).

Notably, this definition is not limited to any particular embodiment; it is presented in general terms and is consistent with all five embodiments set forth in the '233 Patent. Ex. 1001 at 16:54-65 (“***According to the semiconductor devices of***

the first to fifth embodiments described above, the silicon pillars are uniformly arranged around or near the metal contact plug 31 in plan view. With this configuration, the maximum interval between the metal contact plug 31 and the silicon pillar 5 is twice or less the minimum interval between the metal contact plug 31 and the silicon pillar 5....”). Thus, the claim term “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug” should be construed to mean that “the maximum interval between the contact plug and the semiconductor pillars is twice or less the minimum interval between the contact plug and the semiconductor pillars.”

Furthermore, the above definition is consistent with the purpose of the invention discussed above in Section II.B, which is to avoid the prior art’s “problem that electrical resistances between a lower contact plug . . . and the semiconductor pillars largely differ depending on connecting positions,” and that “if the maximum interval between the semiconductor pillar and the lower contact plug becomes more than twice the minimum interval between the semiconductor pillar and the lower contact plug becomes more than twice the minimum interval between the semiconductor pillar and the lower contact plug in plan view, there occurs variation in characteristics of transistors provided to the semiconductor pillars.” *Id.* at 1:63-2:7. The ’233 Patent proposes a solution where the pillars are “uniformly arranged near the” contact plug in order to avoid the problems that occur when the maximum

distance between the pillars and the contact plug exceeds the minimum distance between the pillars and the contact plug by more than a factor of two, thereby “stabiliz[ing] the characteristics of the transistors.” Ex. 1001 at 1:63-2:6, 2:7-10, 2:18-21, 2:34-35, 2:45-48; *see also, e.g., id.* a 6:57-65 (“[S]ince the maximum interval... is twice or less the minimum interval..., it is possible to avoid the prior art problem....”); *id.* at 16:28-36 (same); *id.* at 16:54.

Despite offering no theory regarding the correct construction of “uniformly arranged” or any other claim term (Pet. at 10), the Petition implies at one point that any matrix configuration of pillars would meet the requirement that “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.” *See* Pet. at 78-79 (implying this limitation is met by any “matrix arrangement in circuit layout”). But that understanding is incorrect for two reasons. First, it is directly contrary to the definition set forth in the ’233 Patent at 12:40-46 (which definition the Petition does not even mention, much less rebut). Second, a construction where any matrix configuration meets the claim requirements would improperly read out the requirement that the “pillars are uniformly arranged *near* the” contact plug, because that construction does not specify any distance that would be “near” the contact plug. In contrast, the ’233 Patent’s definition specifies what distances satisfy the “near” requirement (*i.e.*, the maximum distance between pillar

and contact plug must be no more than twice the minimum distance between pillar and contact plug).

V. The Petition’s Ground 1 fails.

The Petition provides a motivation to combine that rests on two critical assumptions: first, that Endoh includes a common source line (CSL) that is “above” the semiconductor pillars; and second, that because Endoh’s lower diffusion layer 9 is connected to a common source, that layer “needs” a connection to the CSL alleged to be above the semiconductor pillars. Neither of these assumptions, however, is supported by any evidence or analysis accompanying the Petition.

A. Overview of the Petition’s Motivation to Combine

The logical structure of the Petition’s argument regarding the obviousness of limitation [1.5] based on the combination of Endoh with Hwang is as follows. *First*, the Petition contends that “Endoh has the need to provide a connection between the n-type common source diffused layer 9 (at the bottom of the semiconductor pillars) and the common source line (CSL) (above the top of the semiconductor pillars).” Pet. at 44.

Second, based on the premise that the above contention is correct, the Petition argues that a POSITA would have been motivated to combine Endoh with Hwang:

Second, *with Endoh’s need to provide a connection between the n-type common source diffused layer 9 (at the bottom of the semiconductor pillars) and the common source line (CSL) (above the*

top of the semiconductor pillars), a POSITA would have looked to Hwang and applied Hwang’s teachings of providing a vertical contact plug to connect the bottom source region to a common source line, in Endoh.

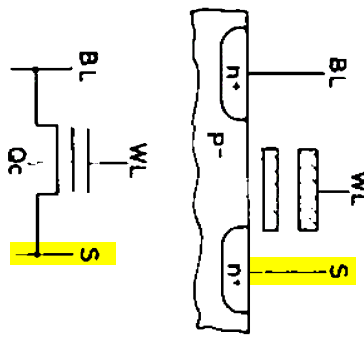
Pet. 46. Thus, the purported motivation to combine Endoh with Huang rests upon the premise that Endoh has a “need to provide a connection between the n-type common source diffused layer 9 (at the bottom of the semiconductor pillars) and the common source line (CSL) (above the top of the semiconductor pillars).” *Id.* As explained below, the Petition has not set forth any evidence that Endoh does, in fact, have such a need, and thus cannot establish a motivation to combine Endoh with Hwang in the proposed manner.

B. The Petition’s motivation to combine is based upon the false premise that Endoh includes a common source layer near the top of the semiconductor device.

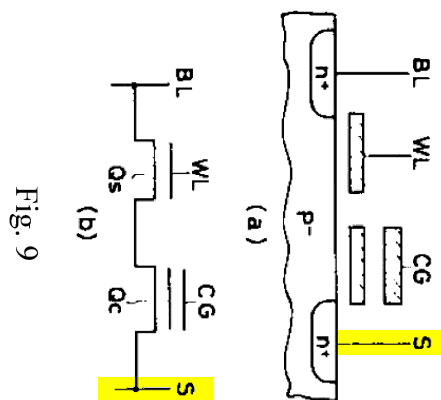
As a basic preliminary matter, in order for the Petition to support its premise of a “need” in Endoh to connect layer 9 to a CSL “above the top of the semiconductor pillars,” the Petition must provide evidence that Endoh discloses a CSL above the top of the semiconductor pillars.

The Petition, however, sets forth no evidence or analysis supporting such a conclusion. For example, the Petition provides no citation to Endoh that describes a CSL at the top of any semiconductor pillars. *See generally* Pet. at 43-46. Indeed, the only references the Petition provides to Endoh on this point are an “Equivalent

Circuit Diagram of Embodiment 1” provided by Petitioner (*see* Pet. 44-45), and Endoh’s Figure 9 rotated 90 degrees to the right “to be aligned with the vertical structure of the semiconductor device,” (Pet. at 45-46). Both of these diagrams are reproduced below, annotated to emphasize the location of the “common source S” in the orientation of the semiconductor device.



Petitioner’s “Equivalent Circuit Diagram of Embodiment 1”

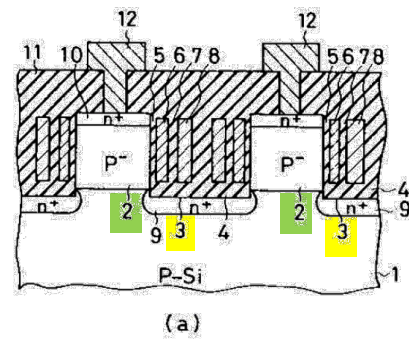


Endoh’s Figure 9 (rotated 90 degrees to the right)

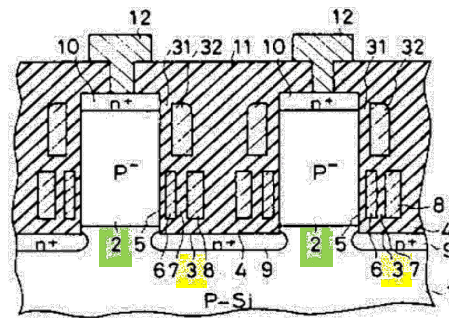
It is immediately clear that even the Petitioner’s depictions of Endoh show a common source “S” *only* toward the *bottom* of the semiconductor device, and *not* “located above the top of the semiconductor pillars” as the Petition claims.

Furthermore, Endoh's description is consistent with these diagrams, in that to the extent any location is disclosed as corresponding to a "source," it is always toward the bottom of the semiconductor configuration, and not "above the top of the semiconductor pillars." For instance, Endoh from the very beginning teaches a "common source diffused layer formed in the bottom of the aforementioned [plaid-shaped] groove." Ex. 1008 at -343-.² Endoh further makes clear that the "plaid-shaped groove" is depicted as element 3. *See* Ex. 1008 at -345- ("the plaid-shaped groove 3"); *id.* at -346- (discussing the method of "form[ing] the plaid-shaped groove 3 reaching the depth of substrate 1"); *id.* at -350- ("3: plaid-shaped groove"). And as shown, *e.g.*, by Figures the Petition relies on (*e.g.*, Figures 2 and 7 reproduced below, but also Figures 3, 4, 7, 8, 10, 13 and 14), the plaid-shaped groove extends **below** semiconductor pillars 2, such that a common source formed "in the bottom of" the plaid-shaped groove would be formed below the bottom of the semiconductor pillars, not "above the top of the semiconductor pillars" as alleged by the Petition.

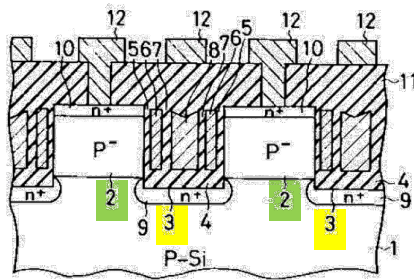
² Although the use of "plaid-shaped" is not entirely clear in this context, it may be an imprecise reference to the fact that in the diagrams, groove 3 is depicted using diagonal lines.



(a)

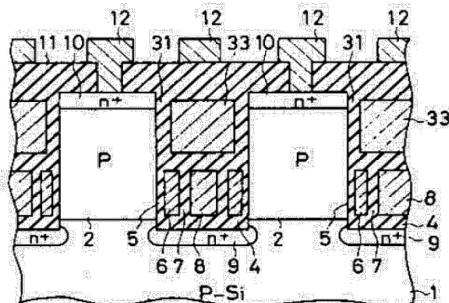


(a)



(b)

Fig. 2



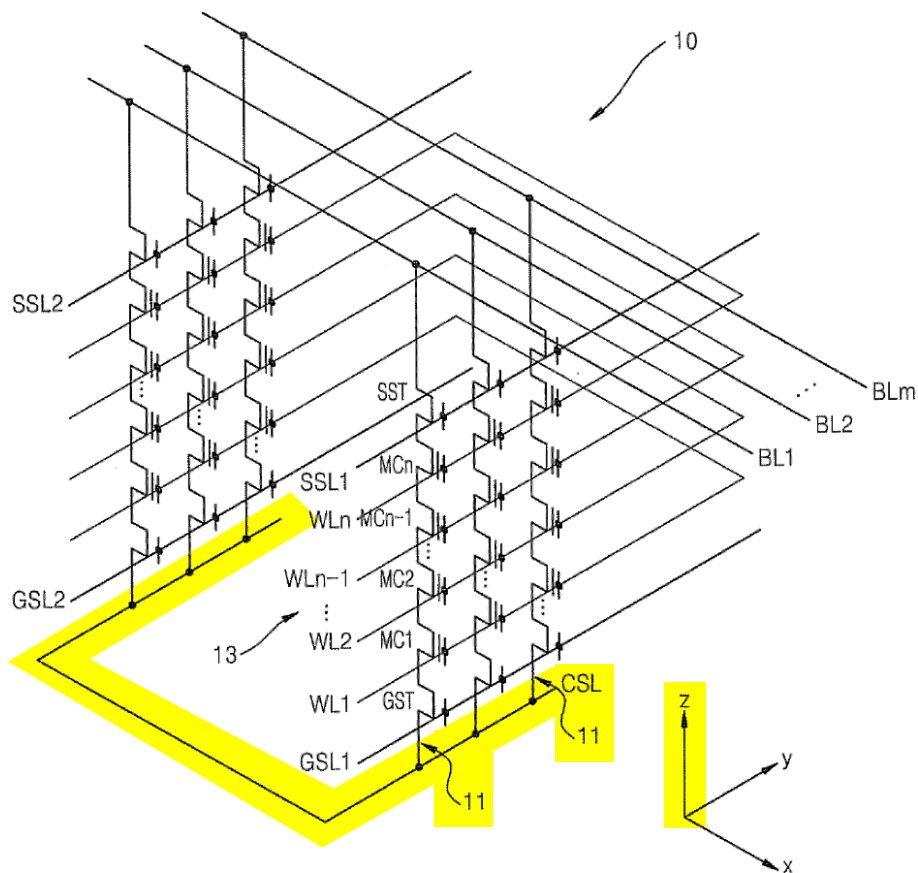
(b)

Fig. 7

Ex. 1008 at Figs. 2, 7 (annotated to show pillars 2 and groove 3); *see also, e.g., id.* at -345- (“common source diffused layer formed at the bottom of the aforementioned groove”); *id.* (“The common source diffused layer 9 of memory cell is formed at the bottom of groove 3....”); *id.* at -346- (referencing “common source diffused layer 9 at the bottom of groove”); *id.* at -347- (referencing “the common source diffused layer 9 in the bottom of groove 3”); *id.* at -348- (“until drain diffused layer 10 is formed above each silicon layer 2, and the common source diffused layer 9 is formed in the bottom of the groove; the method is the same as in the previous embodiments”).

Additionally, although Patent Owner does not understand the Petition to set forth any inherency argument, it is certainly not inherent that a CSL must be located above the top of the semiconductor pillars. Indeed, even *Hwang* (which the Petition proposes would fill the supposed “need” to connect “common source diffused layer 9 (at the bottom of the semiconductor pillars) and the common source line (CSL) (above the top of the semiconductor pillars)”) teaches that a CSL may exist (as it does in Endoh) entirely toward the bottom of the semiconductor device, and need not be located “above the top of the semiconductor pillars” as the Petition implies must be the case in Endoh. In particular, Hwang’s Figure 1 (reproduced below) teaches a “common source line CSL” *only* at the *bottom* of the circuit, as shown by the fact that it is located only at the lower range of the Z axis of Hwang’s device.

FIG. 1



Ex. 1009 at Fig. 1 (annotated to emphasize CSL depicted only at the bottom of the substrate); *id.* at 6:28-34 (“As shown in FIG. 1, an end of each of the memory cell strings 11 (e.g., a drain side of side of the string selection transistors SST) is coupled to a corresponding one of the plurality of bit lines BL1-BLm extending in the x-axis direction. ***The other end*** of each of the memory cell strings 11 (e.g., a source side of the ground selection transistors GST) ***is coupled to a common source line CSL.***”).

In sum, Endoh does not teach (either expressly or inherently) any common source ***above the top*** of any semiconductor pillars, and to the contrary consistently teaches that its common source is positioned ***below the bottom*** of the semiconductor pillars. The Petition simply identifies no evidence or analysis to the contrary, even considering the corresponding expert declaration. *See generally* Pet. at 43-46 (providing no explanation of ***why*** a POSITA would allegedly have viewed Endoh as having a CSL above the top of the semiconductor pillars, when Endoh clearly does not explicitly teach as much); Ex. 1003 at ¶¶97-99 (expert declaration reciting, nearly verbatim, the Petition’s conclusory allegations on this point); *see also* 37 CFR § 42.65 (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Thus, the Petition fails to establish that Endoh teaches a “common source line (CSL) (above the top of the semiconductor pillars).” *See* Pet. 44, 46. And because there is no evidence that Endoh includes a CSL above the top of the semiconductor pillars, there is certainly no evidence that, as the Petition alleges, Endoh has a “need to provide a connection between the n-type common source diffused layer 9 (at the bottom of the semiconductor pillars) and the common source line (CSL) (above the top of the semiconductor pillars).” *See* Pet. at 44, 46.

In light of the absence of the “need” alleged by the Petition, the Petition provides no motivation to combine Endoh with Hwang to arrive at limitation [1.5]

of the '233 Patent. Specifically, for limitation [1.5], the Petition's motivation to combine Endoh with Hwang in the suggested manner is to satisfy Endoh's alleged "need to provide a connection" to "the common source line (CSL) (above the top of the semiconductor pillars)." *See* Pet. at 46 ("Second, with Endoh's need to provide a connection between the n-type common source diffused layer 9 (at the bottom of the semiconductor pillars) and the common source line (CSL) (above the top of the semiconductor pillars), a POSITA would have looked to Hwang and applied Hwang's teachings of providing a vertical contact plug to connect the bottom source region to a common source line, in Endoh."). The Petition additionally argues more generally that a motivation to "provide [a] connection between the bottom source region to a common source line as needed by Endoh"—without specifying *where* the common source line is located—would incentivize a POSITA to use Hwang's "vertical structure arrangement of the vertical contact plug." Pet. at 25; *see also id.* at 48 ("Hwang's teachings of the vertical structure arrangement including the vertical contact plug . . . provide the connection between the bottom source region to a common source as needed by Endoh."). But, of course, a "vertical structure arrangement of the vertical contact plug" would only be needed if the CSL were located *above* Endoh's bottom source region (such that a *vertical* connection would be necessary), which the Petition has not shown.

Finally, the Petition states that “Hwang’s teachings of the vertical structure arrangement of the vertical contact plug” would “provide the obvious, beneficial, and predictable results of high integration density and improved performance.” Pet. 25. But the Petition does not explain how this proposed combination would have increased integration density or improved performance over Endoh’s already functional system (which already makes use of a vertical transistor arrangement), much less how such unexplained improvement in density or performance would have been “obvious” or “predictable.” *See id.* at 25, 43-50; *see also* 37 CFR § 42.65 (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

VI. The Petition’s Ground 2 fails because Takaishi does not disclose or render obvious limitation [1.6].

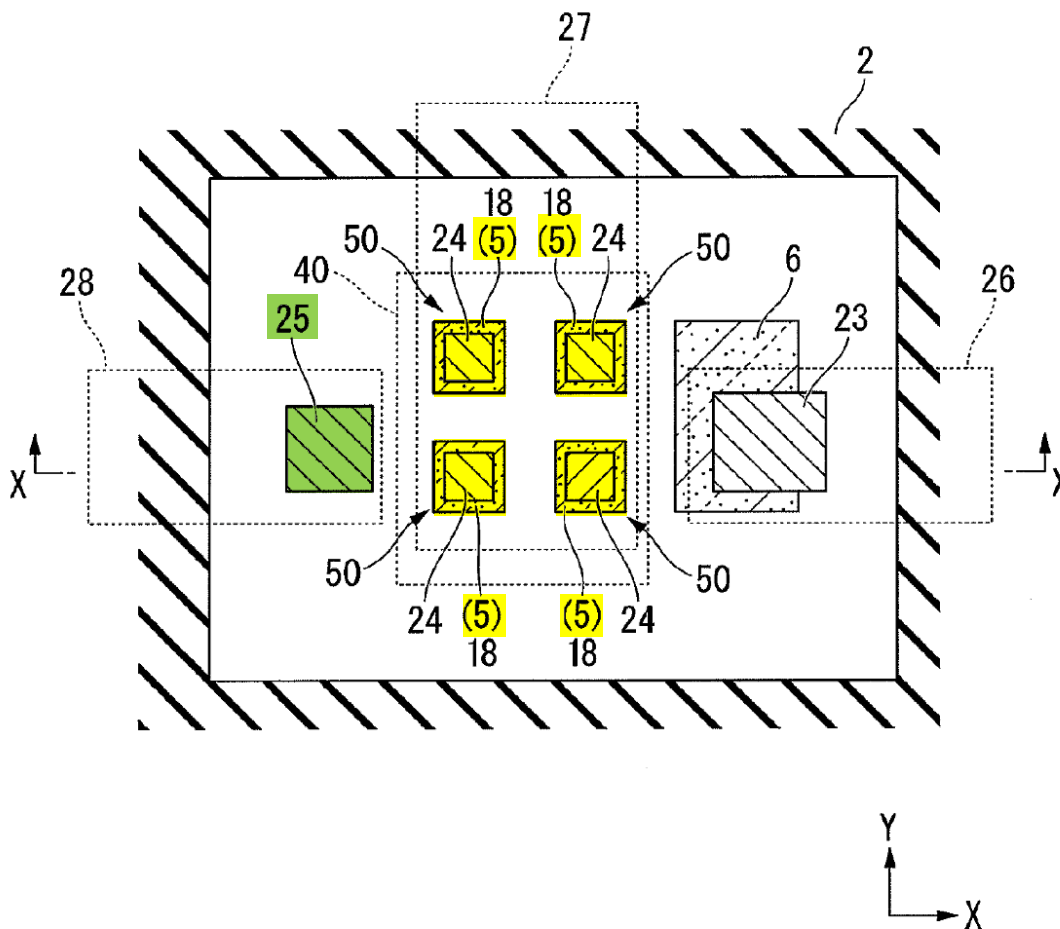
Claim 1 recites, a semiconductor device comprising “a plurality of semiconductor pillars” (limitation [1.1]), wherein “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug” (limitation [1.6]). Because “a plurality of semiconductor pillars” of limitation [1.1] provides antecedent basis for “the semiconductor pillars” of limitation [1.6], the plurality of semiconductor pillars identified for limitation 1.1 must be “uniformly arranged near the lower diffusion layer side contact plug.”

As described below, the Petition does not provide evidence that Takaishi discloses or renders obvious that “the plurality of semiconductor pillars” is “uniformly arranged near the lower diffusion layer side contact plug.”

A. Takaishi does not disclose that “the [plurality of] semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.”

The Petition relies on the embodiment of Takaishi’s Figures 1 and 2 as supposedly disclosing this limitation. In that embodiment, Takaishi discloses four distinct semiconductor pillars 5 arranged in a grid formation, arranged outwardly to the right (positive x direction) from the contact plug 25 in the plan view of Takaishi’s Figure 2.

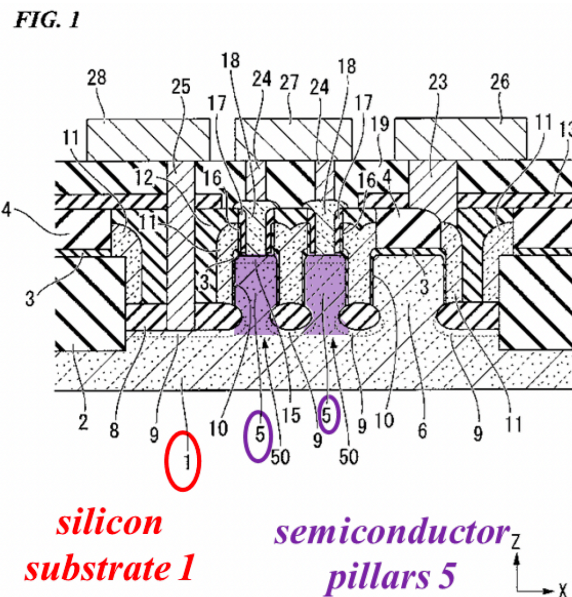
FIG. 2



Ex. 1007, FIG. 2 (pillars 5 annotated with yellow, metal plug 25 annotated with green).

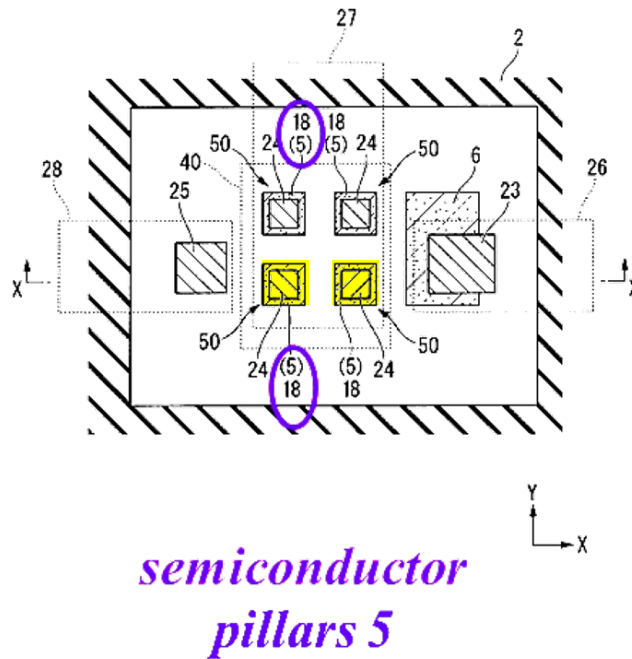
The Petition is explicit that for limitation [1.1], it is identifying *each* of the four pillars 5 in Takaishi's Figure 2 as being the claimed "plurality of semiconductor pillars." See Pet. at 66 ("While the discussion and annotation mainly focuses on the two left silicon pillars 5 in FIG. 2, the analysis similarly applies to *each* silicon pillar 5.").

Indeed, while the Petition highlights only the two left-most semiconductor pillars in its annotation of Figure 2, the Petition highlights the two bottom-most semiconductor pillars in its annotation of Figure 1, because those two pillars extend outwardly to the right from metal plug 25. The Petition’s annotations of Takaishi’s Figures 1 and 2 are reproduced below, with Figure 2 additionally annotated to show in yellow the two pillars the Petition annotated for Figure 1, confirming that the Petition is *not* limiting the “semiconductor pillars 5” to only the two left-most pillars.



Pet. at 65 (Petition’s annotations of Takaishi’s Figure 1).

FIG. 2



Pet. at 65 (Petition’s annotations of Takaishi’s Figure 2, additionally annotated by Patent Owner to highlight in yellow the two semiconductor pillars that the Petition’s annotated Figure 1 identified as being part of the “plurality of semiconductor pillars”).

Because the Petition has mapped each of these four semiconductor pillars to the claimed “plurality of semiconductor pillars” in limitation [1.1], the Petition must show that these same four semiconductor pillars “are uniformly arranged near the lower diffusion layer side contact plug.” *See* Section VI, *supra*; *see also* Pet. 78 (alleging that the Petition’s limitation [1.6] analysis “applies to each silicon pillar 5”).

The Petition sets forth two theories as to how the pillars are supposedly “uniformly arranged near the lower diffusion layer side contact plug.” **First**, the Petition alleges that because these pillars are “‘arranged in a matrix’ near the metal contact plug 25,” they are necessarily “uniformly arranged near the metal contact plug 25.” Pet. at 78. While this may be a uniform arrangement of sorts, outside of the context of the ’233 Patent, the Petition does not explain why the two right-most semiconductor pillars 5 are “uniformly arranged *near* the [contact plug]” as that term would be understood by a POSITA in the context of the ’233 Patent. As explained above in Section IV, the ’233 Patent expressly defines “*pillars 5 [being] uniformly arranged with respect to the metal contact plug*” as a configuration where “*the maximum interval between the [contact plug] and the silicon pillar[s] is twice or less the minimum interval between the [contact plug] and the silicon pillar[s].*” Ex. 1001 at 12:40-46. As explained below, the Petition does not show that Takaishi discloses such an arrangement.

Second, the Petition addresses “the distance configuration” that the ’233 Patent defines as constituting pillars being “uniformly arranged” with respect to the

contact plug,³ to allege that “the first embodiment of Takaishi . . . teaches this limitation.”

As an initial matter, Takaishi does *not* actually disclose limitation [1.6] under the correct claim construction, as the Petition appears to acknowledge. In particular, the Petition does not allege that the “plurality of semiconductor pillars” (i.e., all four of the semiconductor pillars shown in Figure 2) are “uniformly arranged near” the

³ The Petition incorrectly implies that the ’233 Patent’s definition of “uniformly arranged” with respect to the contact plug can only be derived from a “configuration of the first embodiment of the ’233 Patent.” Pet. 79. This is incorrect; as explained above in Section IV, the ’233 Patent expressly defines what it means for pillars to be “uniformly arranged” with respect to a contact plug, and that definition is stated as a general matter, even outside the context of the first embodiment of Figures 1 and 2. *See* Ex. 1001 at 12:22-46 (generalized definition, while discussing “the fifth embodiment”); *id.* at 16:54-65 (explaining that the definition is applicable “to the semiconductor devices of the first to fifth embodiments”). Notably, the Petition does not even mention (much less rebut) the express definition of “uniformly arranged with respect to the metal contact plug” as set forth at 12:40-46 of the ’233 Patent.

contact plug. Instead, the Petition alleges only that *two* of the four pillars are “uniformly arranged near” the contact plug. *See* Pet. 81 (“[A]s shown in annotated FIG. 2 . . . the distance (D1) between the metal contact plug 25 and the *top left* semiconductor pillar 5 is twice or less the distance (D2) between the metal contact plug and the *bottom left* semiconductor pillar 5.”). And the Petition relies only on obviousness to have the distance requirement apply to *all* of the plurality of the semiconductor pillars. *See id.* at 81-82 (“Further, it would have been obvious to a POSITA to use such arrangements for *all* the semiconductor pillars....”). Thus, the Petition concedes (as it must) that all four semiconductor pillars of Takaishi’s Figure 2 (i.e., the alleged “plurality of semiconductor pillars”) do *not* meet the “uniformly arranged near...” limitation of challenged claim 1.

As discussed below, the Petition does not provide any motivation to arrive at a configuration where each of the plurality of semiconductor pillars is “uniformly arranged near the [contact plug].”

B. The Petition does not establish a motivation for the plurality of semiconductor pillars to be “uniformly arranged near” the contact plug.

As shown in the previous section, Takaishi does not disclose that the alleged plurality of semiconductor pillars is uniformly arranged near the contact plug, as required by limitation [1.6]. The Petition’s sole alleged motivation for a POSITA to apply the claimed uniform arrangement to “all of the semiconductor pillars” is “for

the benefit of ‘miniaturized and highly integrated semiconductor devices’ with improved performance by providing similar electronics characteristics related to each semiconductor pillar.” Pet. at 81-82 (citing Ex. 1007, [0040]). But the cited portion of Takaishi teaches that the benefit of “miniaturized and highly integrated semiconductor devices” comes from arranging “silicon pillars 5” in “a *honeycomb shape*,” and says *nothing* of ensuring that the maximum distance between the contact plug and the pillars is no more than twice the minimum distance between the contact plug and the pillars. *See* Ex. 1007, [0040] (“Moreover, when forming a large number of silicon pillars 5, these *silicon pillars 5 may be arranged in a honeycomb-shape* to form a close packing structure, *thereby making it possible to realize miniaturized and highly integrated semiconductor devices*.”). Furthermore, Takaishi says nothing of “providing similar electronics characteristics related to each semiconductor pillar.” *See generally* Takaishi, [0040] (no discussion of keeping the semiconductor pillars arranged such that the pillars are of similar distance to the contact plug, and also no discussion of the importance of ensuring that the semiconductor pillars have similar electronics characteristics). Of course, a honeycomb shape can be implemented in a variety of different arrangements, and as discussed in further detail later in this section, does not necessitate or even imply that the “uniformly arranged near...” requirement of limitation [1.6] would be satisfied.

The failure of Takaishi to disclose the importance of reducing variation in electrical characteristics of the pillars is in direct contrast to the teachings of the '233 Patent on this point, which recognize that the claimed uniform arrangement near the contact plug is a solution to “variations in characteristics of transistors” that results “if the maximum interval between the semiconductor pillar and the lower contact plug becomes more than twice the minimum interval between the semiconductor pillar and the lower contact plug in plan view.” Ex. 1001 at 1:63-2:6 (discussing the problem of variation in electrical characteristics), 2:7-48 (explaining that embodiments where the pillars are “uniformly arranged near” the contact plug is a solution that “can stabilize the characteristics of the transistors provided to individual semiconductor pillars”).

Unlike the '233 Patent, Takaishi does not provide *any* teaching that the uniform arrangement near the contact plug recited in limitation [1.6] is desirable, and the Petition does not allege that a POSITA would have been motivated to implement such an arrangement in Takaishi (as opposed to an arrangement where the distances between pillars and contact plug have significant variations, as disclosed by Takaishi).

Because the Petition does not rely on any teachings from Takaishi itself that provide any motivation to modify Takaishi's Figure 2 embodiment to arrive at the “uniformly arranged near...” limitation, the Petition must identify something in a

“POSITA’s own knowledge” that would have provided a motivation to modify Takaishi in the proposed manner. *See* Pet. 61 (alleging that regarding Ground 2, “a POSITA would have found claims 1-4 obvious, in view of the POSITA’s own knowledge and/or the disclosures provided by Takaishi[]”). The Petition fails to make such a showing.

Specifically, the only motivation for a uniform arrangement of pillars near the contact plug (as opposed to merely the use of a honeycomb shape for pillars as taught by Takaishi) is “providing similar electronics characteristics related to each semiconductor pillar.” Pet. at 81-82. But the Petition provides no evidence that a POSITA, as of the priority date of the ’233 Patent, would have recognized a motivation to provide similar electronic characteristics for each semiconductor pillar, or recognized that the claimed uniform arrangement near the contact plug would have been a means of accomplishing that motivation. *See* Pet. 81-82 (citing only Takaishi at [0040], which provides no such motivation, and Ex. 1003 at ¶ 172, which other than non-substantive differences in citation formatting, is a *verbatim* parroting of the Petition’s conclusory analysis); *see also* 37 CFR § 42.65 (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”). Neither Petitioner nor its expert provides any competent evidence that a POSITA would have recognized a problem in Takaishi’s Figure 2 of dissimilar electronic characteristics of the semiconductor

pillars, or that the uniform arrangement near the contact plug taught by the '233 Patent would have been a solution to that unidentified problem.

Indeed, it appears that the *only* reference cited by the Petition that recognizes a desire to reduce electrical variations between the semiconductor pillars, or that recognizes uniform arrangement near the metal plug as the means to accomplish that objective, is the '233 Patent itself. *See, e.g.*, Ex. 1001 at 1:63-2:48 (identifying the problem and claimed solution). Such reliance on the *inventor's* insights at the time of the invention, rather than reliance on motivations and rationales that would have been apparent to a POSITA in view of the *prior art*, is precisely the type of hindsight bias the Supreme Court and Federal Circuit have cautioned against. *See Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) (“[W]hile we understand that ‘the obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation,’ we also recognize that we cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention.”) (cleaned up, quoting *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 419 (2007)); *Ortho-McNeil Pharm., Inc. v. Mylan Labs., Inc.*, 520 F.3d 1358, 1364 (Fed. Cir. 2008) (“[Hindsight] reasoning is always inappropriate for an obviousness test [A]t the time of the invention, the inventor’s insights, willingness to confront and overcome obstacles, and yes, even serendipity, cannot be discounted.”); *Mitsubishi Chem. Corp. v. Barr Lab’ys, Inc.*,

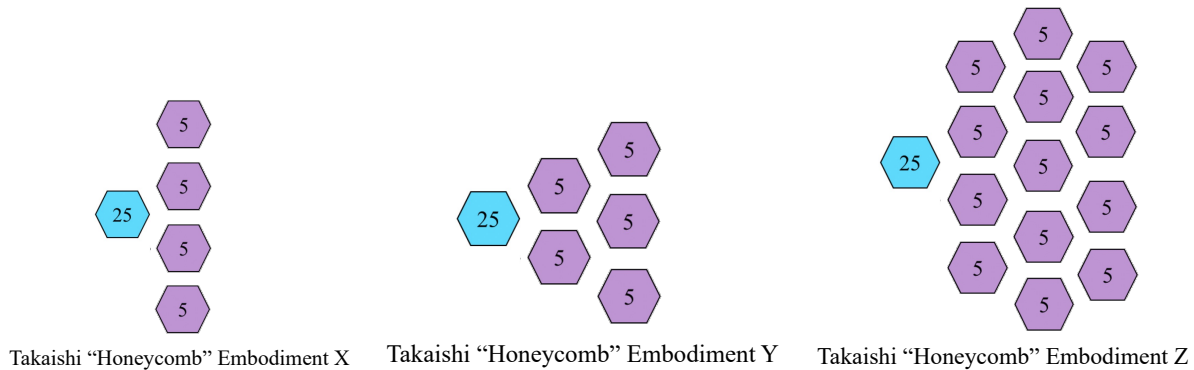
718 F. Supp. 2d 382, 426 (S.D.N.Y. 2010), *aff'd*, 435 F. App'x 927 (Fed. Cir. 2011) (“A proper obviousness analysis thus requires the recognition that *the prior art, not hindsight knowledge of a patentee's success, must motivate a person skilled in the art to do what the patentee has done.*”).

The Petition’s hindsight analysis is exemplified by its reliance on purported “examples A-C of the first embodiment of Takaishi” (*see* Pet. 82-84), which are not actually *examples* of Takaishi’s first embodiment, but are rather *modifications* to Takaishi’s first embodiment that Petitioner’s expert constructed with the benefit of hindsight in order to arrive at the challenged claims. *See* Pet. at 82 (referencing “examples A-C of the first embodiment of Takaishi *as provided by Dr. Lee*”).

These “examples,” far from being what Takaishi actually discloses or renders obvious, merely appear to be what Petitioner’s expert contends are *possible* ways to implement Takaishi’s first embodiment. As explained in further detail below, these are not possible ways to implement Takaishi’s first embodiment, because they are directly inconsistent with Takaishi’s descriptions of its first embodiment. But even if these examples *were* possibilities, that does not mean that a POSITA would have been *motivated* to modify Takaishi’s first embodiment to arrive at any of these examples, which is what the Petition must establish. *See Personal Web Tech. v. Apple*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) (“Obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the

combinations or modifications of prior art to arrive at the claimed invention.”) (emphasis original; internal citations and quotations omitted); *Apple, Inc. v. Realtime Data LLC*, IPR 2016-01737, Paper 57 at 59 (March 13, 2018) (granting motion to amend in full, in part because petitioner did not adequately “articulate a *reason why* a person of ordinary skill in the art would combine the prior art references”) (citing and quoting *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention”)) (emphases in original); *Sisvel Int’l S.A. c. Sierra Wireless, Inc.*, Appeal No, 2022-1493, Dkt. No. 68 at 13-14 (Fed. Cir. October 6, 2023) (affirming Board’s decision finding lack of motivation to combine references where “reasons to combine were merely assertions that the references were analogous art, which, without more, is an insufficient articulation for motivation to combine” or “were too conclusory, lacked clarity, or suffered from both problems”).

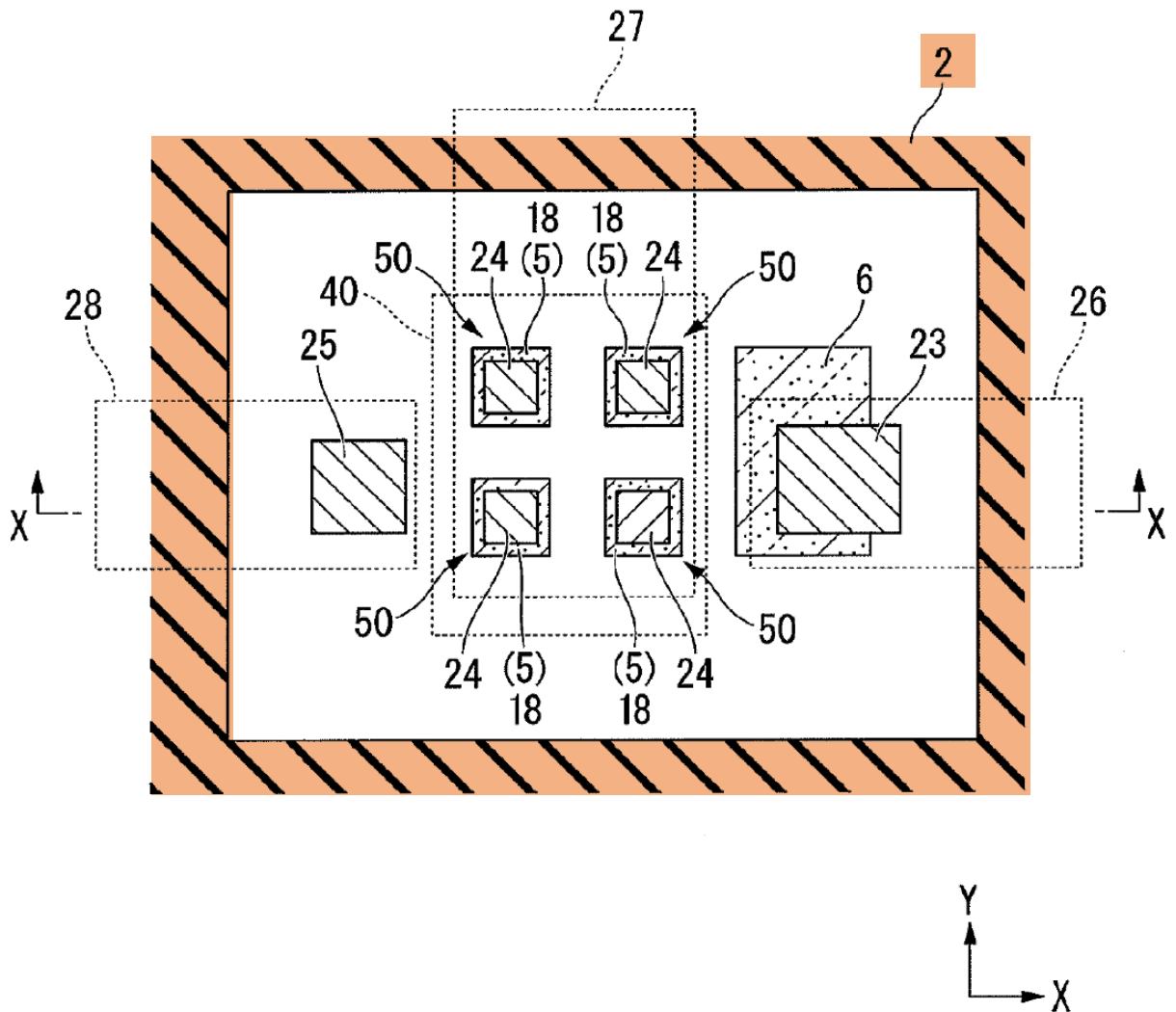
The fact that the Petition *at most* addresses what modifications a POSITA *could have made* is shown by the fact that a POSITA could have implemented Takaishi’s “honeycomb” teaching in a variety of ways, including the exemplary ways X, Y, and Z provided below, to implement Takaishi’s first embodiment using “honeycomb” shapes in a manner that would be far more consistent with Takaishi’s discussion of that embodiment:



As shown by potential implementations X, Y, and Z depicted above, the Petition’s “examples A-C” are at most evidence that a POSITA *could* implement Takaishi’s first embodiment in the claimed manner, not that a POSITA *would* have done so, given that there are numerous ways to implement Takaishi’s “honeycomb” shape that do not satisfy the “uniformly arranged near...” limitation of claim 1.

And in any event, a POSITA could *not* have implemented any of the Petition’s examples A-C consistently with Takaishi’s description of its first embodiment, because each of those examples conflicts with Takaishi’s description in at least one respect. For example, Takaishi clearly teaches that its first embodiment includes a “shallow trench isolation (STI) 2, which functions as a trench for separating semiconductor devices.” Ex. 1007 at [0026]. The STI 2 region is shown in Takaishi’s Figure 2, reproduced and annotated below.

FIG. 2



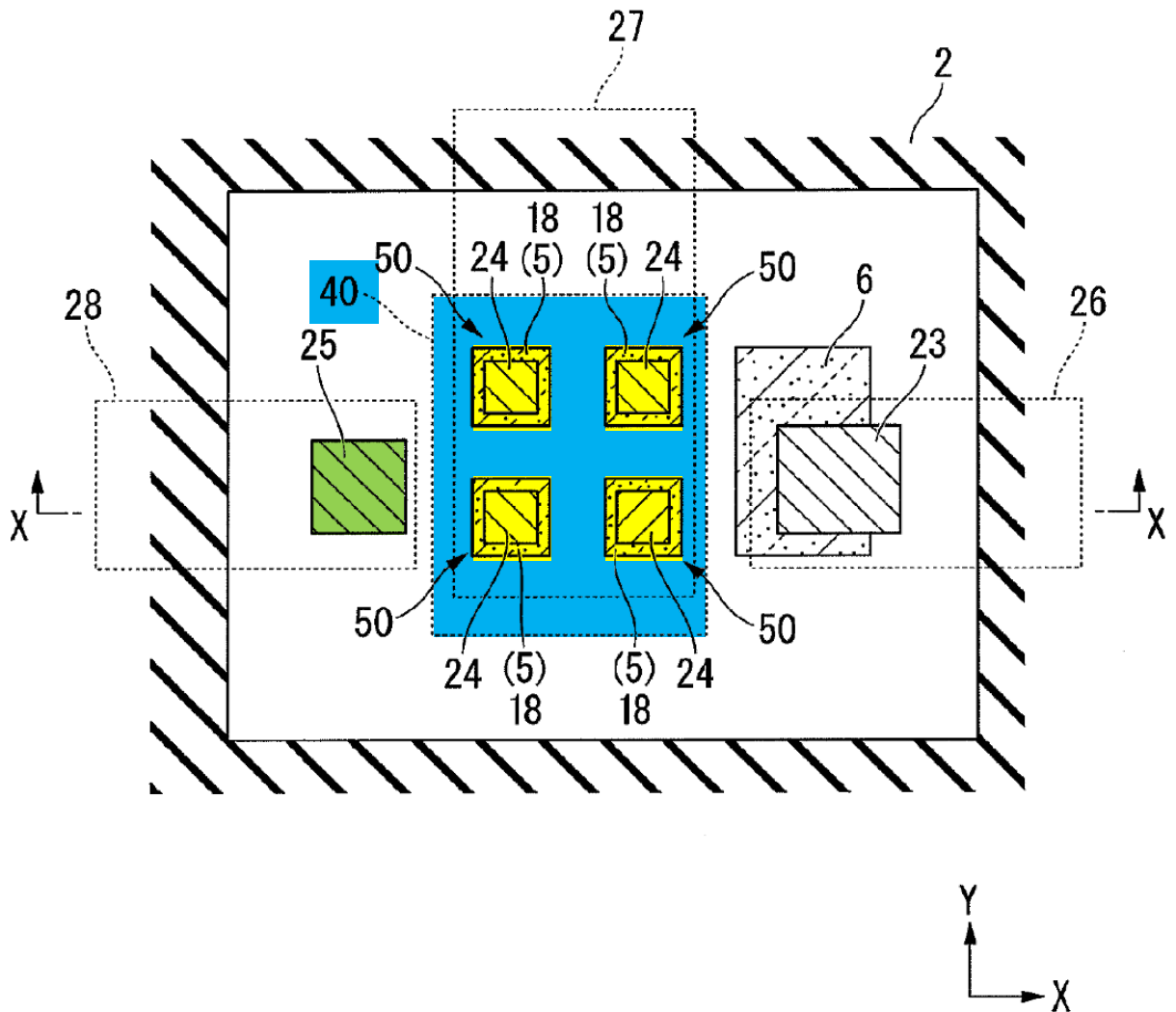
Ex. 1007, Fig. 2 (annotated to show shallow trench isolation (STI) region 2).

Takaishi further teaches that its “*plurality of silicon pillars* (semiconductor pillars) 5 *are provided* in a standing manner *around the center of an area surrounded by the STI 2,*” and that “[t]he metal contact plug 25 is formed at an intermediate area between the silicon pillars 5 and the STI 2.” *Id.* at [0026], [0035].

In other words, Takaishi teaches that the pillars 5 should be located toward the *center* of the area surrounded by STI 2, and that the “metal contact plug 25” should be located “at an intermediate area *between* the silicon pillars 5 and the STI 2.” *Id.* This arrangement is clearly depicted in Takaishi’s Figure 2, in which all of the semiconductor pillars 5 are located to the right of metal plug 25, such that metal plug 25 is “at an intermediate area between the silicon pillars 5 and the STI 2.” Takaishi at FIG. 2, [0035].

A POSITA would recognize that this arrangement is important because during the manufacturing process, “*a pattern layout 40* used for removing the part of the mask oxide film 13 has a pattern *only around an area where the silicon pillars 5 are arranged.*” *Id.* at [0053]. This is visually depicted in Takaishi’s Figure 2 (annotated version reproduced below), which shows pattern layout 40 (blue) *only* overlying the silicon pillars (yellow), and not overlying the contact plug 25 (green).

FIG. 2



Ex. 1007 at FIG. 2 (annotated).

In contrast to Takaishi's teachings on this point, both of the Petition's "examples" A and B locate the semiconductor pillars 5 more toward the left (away from the center of the area surrounded by STI 2), such that the contact plug 25 is *not* situated in an "intermediate region" between pillars 5 and STI 2. A POSITA would

recognize that this would make placing pattern layout 40 to only cover silicon pillars 5 much more difficult, increasing the difficulty and expense of the manufacturing process. Petitioner and its expert are entirely silent on these inconsistencies between Takaishi's teachings and the made-up "examples" A and B.

The Petition's "example" C is also inconsistent with Takaishi's teachings. In particular, Takaishi teaches that "*when forming a large number of silicon pillars 5, these silicon pillars 5 may be arranged in a honeycomb-shape.*" Ex. 1007, [0040]. However, the Petition's "example" C only uses two silicon pillars 5, and thus is not a scenario that Takaishi teaches is applicable to the honeycomb shape. Indeed, although Takaishi teaches that "the shape, the number, and the arrangement of the silicon pillars 5 are not limited to those" depicted in Figure 2, nothing in Takaishi (or any other reference relied on by the Petition) teaches that the "plurality of semiconductor pillars" would be limited to only *two* semiconductor pillars, and the Petition does not even *allege* any motivation to modify Takaishi to reduce the number of pillars from four to two. Accordingly, Takaishi does not teach the Petition's "example" C, and the Petition has not set forth even a *prima facie* case that such a configuration would have been obvious.

Finally, the Petition vaguely alleges that "the prosecution history supports that Takaishi teaches this limitation." Pet. at 83. Precisely the opposite. The examiner clearly *allowed* claim 1 over Takaishi. And the Petition cites no authority for its

implication that if an examiner rejects a claim and an applicant does not expressly dispute the basis for that rejection, *different* claims alleged to be “similar” to the rejected claim should be presumed invalid. As discussed in detail above, Takaishi clearly does *not* disclose limitation [1.6] (or render that limitation obvious), such that the Examiner did not err in allowing claim 1 over Takaishi.

VII. Conclusion

For the reasons set forth above, Patent Owner respectfully requests that the Board deny institution of the Petition. Regarding Ground 1, the Petition’s purported motivation to combine rests on an assumption that Endoh has a “need” that is not taught or suggested by any art of record. And regarding Ground 2, the Petition resorts to hindsight “examples” of potential ways a POSITA allegedly *could* have modified Takaishi’s first embodiment, without establishing that a POSITA *would have been motivated* to implement those “examples.” And each of those examples is inconsistent with Takaishi’s teachings, such that a POSITA would not have found it obvious to implement them.

Date: October 10, 2023

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CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 7,223 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on October 10, 2023, by filing this document through the Patent Trial and Appeal Board Cast Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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