

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

IPR2023-01123
Patent 9,379,233 B2

Before RICHARD M. LEBOVITZ, DAVID C. McKONE, and
KEVIN C. TROCK, *Administrative Patent Judges*.

McKONE, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Western Digital Technologies, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–4 of U.S. Patent No. 9,379,233 B2 (Ex. 1001, “the ’233 patent”). Paper 2 (“Pet.”). Longitude Licensing LTD (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 6 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2016); 37 C.F.R. § 42.4(a) (2019). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons explained below, we decline to institute an *inter partes* review of the ’233 patent.

B. *Related Matters*

The parties identify several proceedings that may affect, or be affected by, this proceeding, including *Longitude Licensing Limited v. Amazon.com, Inc.*, 8-23-cv-00039 (C.D. Cal.), in which Petitioner has filed a motion to intervene. Pet. 2–3; Paper 4, 2.

C. *The ’233 Patent*

The ’233 patent describes vertical transistor type semiconductor devices. Ex. 1001, 1:50–53. Figure 2, reproduced below, illustrates an example.

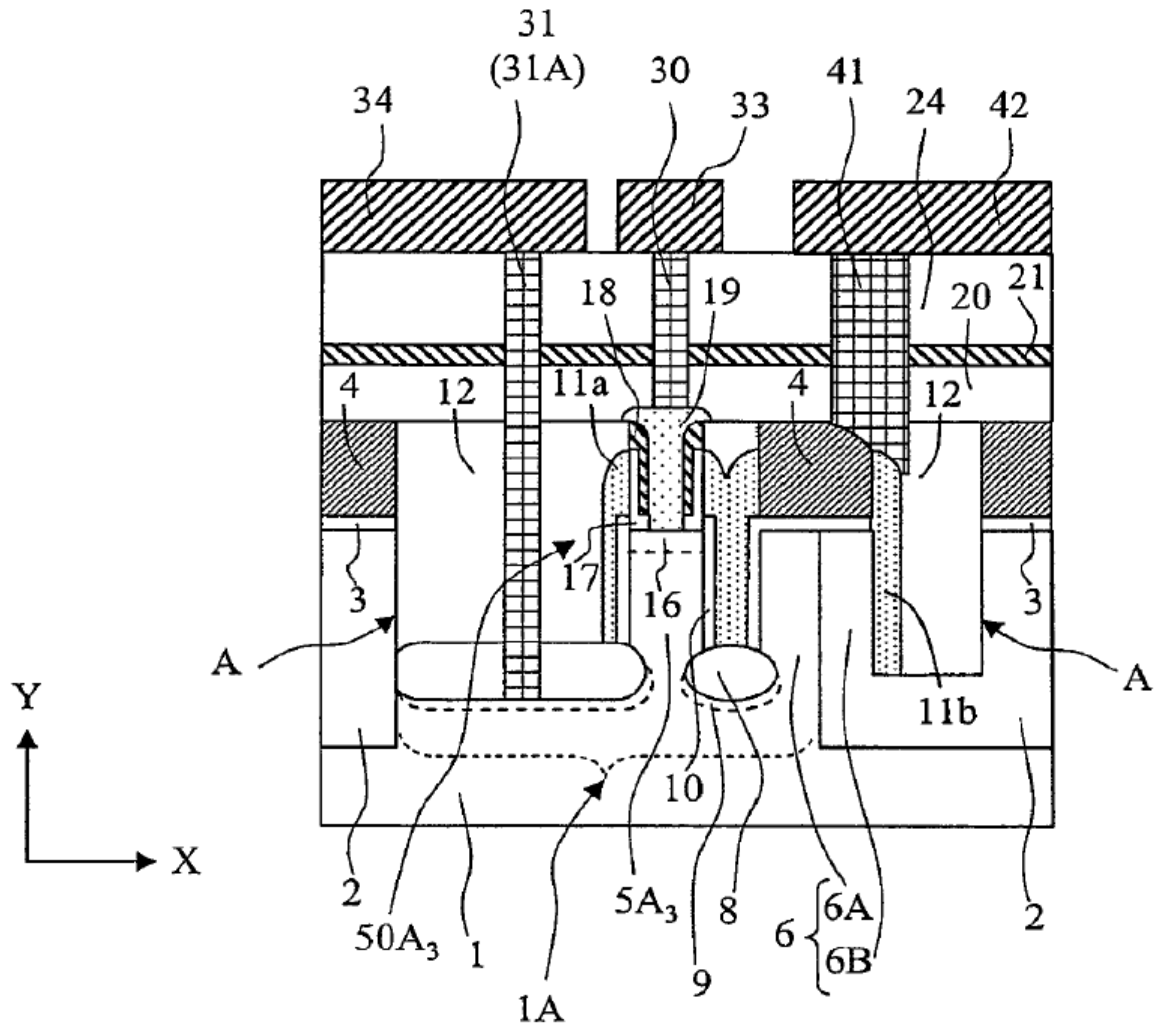


FIG. 2

Figure 2 is a cross-sectional view of a semiconductor device taken along line X1—X1' of Figure 1 (discussed below). *Id.* at 2:64–3:4.

Shallow trench isolation (STI) region 2 is provided on silicon substrate 1. *Id.* at 7:16–17. Pillars 5 (e.g., pillar 5A₃) stand upright in active region 1A, the region of silicon substrate 1 surrounded by STI 2. *Id.* at 7:17–21. Pillar 5 is a columnar semiconductor forming a channel of the corresponding unit transistor 50, which is a vertical transistor. *Id.* at 7:22–24. Pillar upper diffusion layer 16 is located at the upper end portion of pillar 5 and forms one of a source and a drain while pillar lower diffusion

layer 9 located at the lower end portion of pillar 5 forms the other of the source and the drain. *Id.* at 7:31–35. A middle portion of pillar 5, between pillar upper diffusion layer 16 and pillar lower diffusion layer 9, forms the channel. *Id.* at 7:35–38. Insulating film 8 covers the etched surface around silicon pillar 5 and reaches STI 2. *Id.* at 7:60–62. Pillar lower diffusion layer 9 is disposed under insulating film 8 such that pillar lower diffusion layer 9 is electrically insulated from gate electrode 11 by insulating film 8. *Id.* at 7:62–66. Metal interconnection 34 is connected to pillar lower diffusion layer 9 through metal contact plug (conductive plug) 31. *Id.* at 9:8–10.

Figure 1, reproduced below, shows an arrangement of multiple pillars.

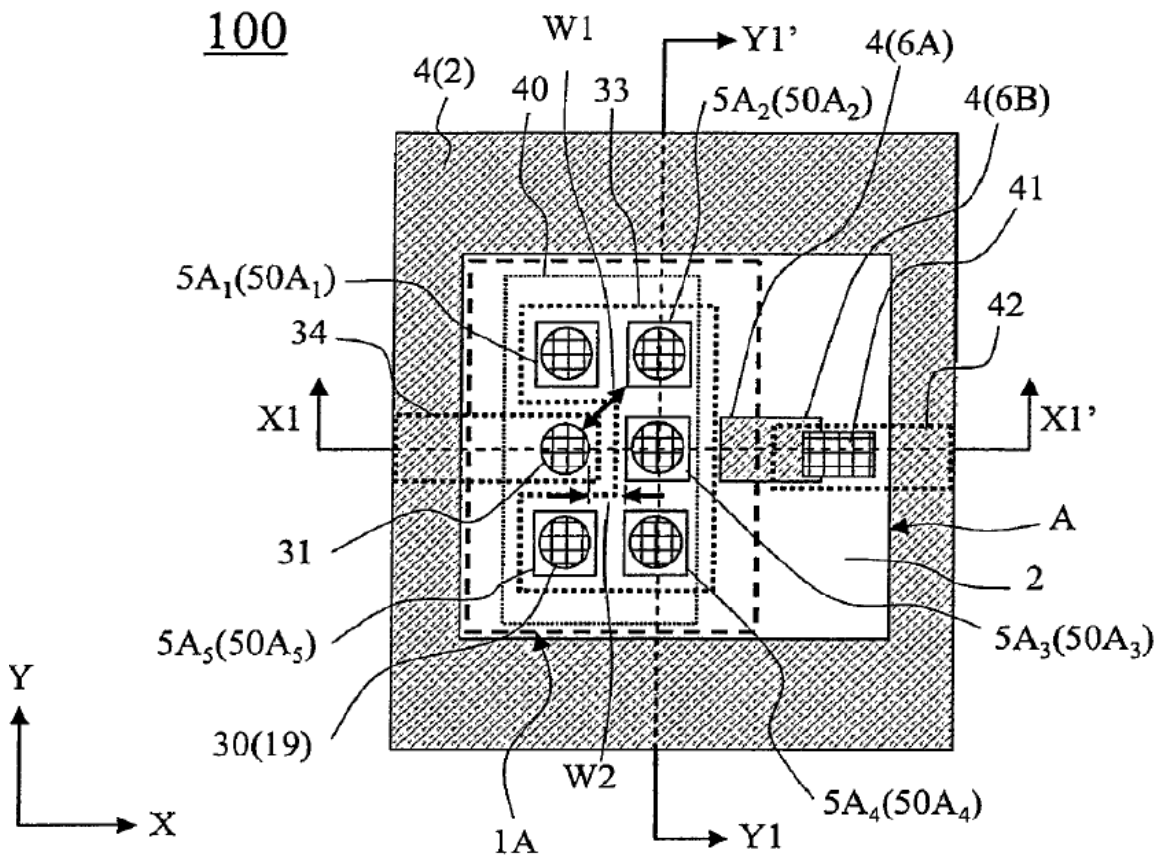


FIG. 1

Figure 1 is a plan view showing the structure of the semiconductor device shown in Figure 2. *Id.* at 2:64–3:4. Five silicon pillars, 5A₁–5A₅, corresponding to five unit transistors 50A₁–50A₅, are arranged in a ' shape in plan view. *Id.* at 4:52–60.

That is, the two unit transistors, i.e. the first unit transistor 50A₁ and the second unit transistor 50A₂, are arranged at an interval therebetween so that their centers are located on the same line in the X-direction. Herein, this interval is set to 30 nm. Further, the three unit transistors, i.e. the second unit transistor 50A₂, the third unit transistor 50A₃, and the fourth unit transistor 50A₄, are arranged at an interval therebetween so that their centers are located on the same line in the Y-direction. Herein, this interval is set to 30 nm. Further, the two unit transistors, i.e. the fourth unit transistor 50A₄ and the fifth unit transistor 50A₅, are arranged at an interval therebetween so that their centers are located on the same line in the X-direction. Herein, this interval is set to 30 nm.

Id. at 4:60–5:5. Metal contact plug 31 is surrounded by the five unit transistors. *Id.* at 6:21–22.

According to the '233 patent, in a preferred embodiment, the interval between the outer periphery of the metal contact plug 31 and each of the first silicon pillar 5A₁, the third silicon pillar 5A₃, and the fifth silicon pillar 5A₅, the center of which is located on the same center line in the X- or Y-direction as the center of the metal contact plug 31, is 35 nm, which is the minimum interval. On the other hand, the interval between the outer periphery of the metal contact plug 31 and each of the second silicon pillar 5A₂ and the fourth silicon pillar 5A₄, each located in the direction inclined by 45 degrees from the center line in the X-direction with respect to the metal contact plug 31, is 57 nm, which is the maximum interval. In this case, since the maximum interval (57 nm) is twice or less the minimum interval (35 nm), it is possible to avoid the prior art problem that the intervals between the metal contact plug 31 and the respective silicon pillars become non-uniform so that parasitic resistances of the lower diffusion layer from the metal contact

plug 31 to the respective silicon pillars differ from each other, resulting in unstable characteristics of the entire semiconductor device.

Id. at 6:46–65.

Claim 1, reproduced below,¹ is illustrative of the invention:

1. A semiconductor device comprising:

- [1.1] a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region;
- [1.2] a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars;
- [1.3] an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain;
- [1.4] a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain; and
- [1.5] a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein
the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug, and
- [1.6] the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.

¹ We use the bracketed numbering added by Petitioner to differentiate among the claim limitations.

D. Evidence

Petitioner relies on the references listed below.

Reference		Date	Exhibit No.
Takaishi	US 2009/0085102 A1	Apr. 2, 2009	1007
Endoh	H4-79369 ²	Mar. 12, 1992	1008
Hwang	US 8,492,797 B2	July 23, 2013	1009

Petitioner also relies on the Declaration of Jack C. Lee, Ph.D.
(Ex. 1003).

E. The Asserted Grounds of Unpatentability

Petitioner contends that claims 1–4 are unpatentable under the following grounds. Pet. 10.

Claims Challenged	35 U.S.C. §	References
1–3	103(a) ³	Endoh, Hwang
1–4	103(a)	Takaishi

II. ANALYSIS

A. Level of Skill in the Art

Petitioner argues that a person of ordinary skill in the art “would have a bachelor’s or the equivalent degree in electrical engineering or a related field and 2–3 years of professional experience relating to semiconductor

² We rely on Petitioner’s certified English translation of the Japanese publication.

³ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Because the ’233 patent claims a filing date before March 16, 2013, the effective date of the relevant amendment, the pre-AIA version of § 103 applies.

device design and fabrication,” and that “a person with less formal education but more experience, or more formal education but less experience, could have also met the relevant standard for” a person of ordinary skill. Pet. 9 (citing Ex. 1003 ¶ 17). Patent Owner does not challenge Petitioner’s proposal. Prelim. Resp. 6.

For purposes of this Decision, we adopt Petitioner’s proposal, which we find consistent with the level of skill reflected by the prior art, and which is supported by expert testimony. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art may reflect an appropriate level of skill in the art).

B. Claim Construction

We construe a claim

using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b) (2019); *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc).

Petitioner contends that “no claim term requires express construction,” and that “this Petition analyzes the claims consistent with ordinary and customary meaning as would be understood by [person of ordinary skill in the art] in light of the specification.” Pet. 10.

Patent Owner proposes that we construe “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug,” as recited in claim limitation 1.6, to mean “the maximum interval between the

contact plug and the semiconductor pillars is twice or less the minimum interval between the contact plug and the semiconductor pillars.” Prelim. Resp. 6–10. Patent Owner argues that the ’233 patent provides an express definition of this language and, thus, the patentee has acted as his own lexicographer. *Id.* at 6–7.

Specifically, the Specification of the ’233 patent states:

In this manner, the silicon pillars 5 do not necessarily surround the contact plug 31 in ‘-shape and it is satisfactory if the silicon pillars 5 are uniformly arranged with respect to the metal contact plug 31, *i.e. the maximum interval between the metal contact plug 31 and the silicon pillar 5 is twice or less the minimum interval between the metal contact plug 31 and the silicon pillar 5.*

Ex. 1001, 12:40–46 (emphasis added). Patent Owner argues that the use of “i.e.” is definitional language that creates lexicography. Prelim. Resp. 7. According to the Federal Circuit, “[i]n a specification, a patentee’s ‘use of ‘i.e.’ signals an intent to define the word to which it refers.” *SkinMedica, Inc. v. Histogen Inc.*, 727 F.3d 1187, 1200 (Fed. Cir. 2013) (quoting *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1334 (Fed. Cir. 2009)).

Patent Owner also argues that its proposed construction is consistent with all other embodiments described in the ’233 patent. Prelim. Resp. 7–8. The Specification states:

According to the semiconductor devices of the first to fifth embodiments described above, the silicon pillars 5 are uniformly arranged around or near the metal contact plug 31 in plan view. With this configuration, the maximum interval between the metal contact plug 31 and the silicon pillar 5 is twice or less the minimum interval between the metal contact plug 31 and the silicon pillar 5 so that variation in electrical

resistance between the metal contact plug 31 and the respective silicon pillars 5 can be set within an allowable value range.

Ex. 1001, 16:54–63. Here, the Specification refers to each of the embodiments having the silicon pillars uniformly arranged around or near the metal contact plug and describes these embodiments as having the same maximum and minimum intervals as provided in the Specification’s definition. *See also id.* at 4:35–42 (“The unit transistors are uniformly arranged around the metal contact plug 31. In the first embodiment, ‘uniformly arranged’ represents an arrangement in which, in plan view, the distance between the metal contact plug 31 and a closest portion of the unit transistor farthest from the metal contact plug 31 is twice or less the distance between the metal contact plug 31 and a closest portion of the unit transistor closest to the metal contact plug 31.”), 9:40–44 (“i.e. the uniform arrangement can be achieved. In this case, W1 represents the maximum interval while W2 represents the minimum interval. That is, the maximum interval can be set to twice or less the minimum interval.”), 10:23–36, 11:10–19, 11:60–12:4.

Patent Owner further argues that its proposed construction is consistent with the purpose of the invention. Prelim. Resp. 8–9. According to the ’233 patent,

there has been a problem that electrical resistances between a lower contact plug, which is connected to the lower diffusion layers, and the semiconductor pillars largely differ depending on connecting positions between the lower diffusion layers and the lower contact plug and that if the maximum interval between the semiconductor pillar and the lower contact plug becomes more than twice the minimum interval between the semiconductor pillar and the lower contact plug in plan view, there occurs variation in characteristics of transistors provided to the semiconductor pillars.

Ex. 1001, 1:64–2:6. In the first embodiment, for example,

since the maximum interval (57 nm) is twice or less the minimum interval (35 nm), it is possible to avoid the prior art problem that the intervals between the metal contact plug 31 and the respective silicon pillars become non-uniform so that parasitic resistances of the lower diffusion layer from the metal contact plug 31 to the respective silicon pillars differ from each other, resulting in unstable characteristics of the entire semiconductor device.

Id. at 6:57–65. Thus, the Specification describes the uniform arrangement of pillars near the contact plug as solving a problem recognized in the prior art.

Petitioner anticipates that Patent Owner might raise this claim construction issue, and presents an obviousness theory “to the extent that Patent Owner argues that ‘uniformly arranged’ requires the distance configuration of the first embodiment of the ’233 patent (EX1001, FIG. 1, 4:35–42).” Pet. 79; *see also id.* at 80 (“[A person of ordinary skill in the art] would have understood that the claim term ‘uniformly arranged’ at least includes an example arrangement as explicitly provided by the ’233 patent, e.g., an arrangement that ‘the distance between the metal contact plug 31 and a closest portion of the unit transistor farthest from the metal contact plug 31 is twice or less the distance between the metal contact plug 31 and a closest portion of the unit transistor closest to the metal contact plug 31.’” (quoting Ex. 1001, 4:35–42)). Nevertheless, Petitioner does not propose a construction of “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.”

In any case, on the current record, we agree with Patent Owner that the ’233 patent, through its use of “*i.e.*” (Ex. 1001, 12:40–46), defines “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug” as “the maximum interval between the contact plug and

the semiconductor pillars is twice or less the minimum interval between the contact plug and the semiconductor pillars.” Ex. 1001, 12:40–46; *SkinMedica*, 727 F.3d at 1200. All embodiments described in the ’233 patent are consistent with this definition. Ex. 1001, 4:35–42, 9:40–44, 10:23–36, 11:10–19, 11:60–12:4, 16:54–63. Moreover, the ’233 patent describes such a uniform arrangement as solving a known problem of the prior art. Ex. 1001, 1:64–2:6, 6:57–65. This description reinforces the definition and makes clear that the use of “*i.e.*” is more than “a qualifier, meaning ‘that is to say’ or ‘in other words,’” or “as merely clarifying” the description. *SkinMedica*, 727 F.3d at 1214 (Rader, J., dissenting).

Based on the record before us, we do not find it necessary to provide express claim constructions for any other claim terms. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

C. Obviousness over Endoh and Hwang

Petitioner contends that claims 1–3 would have been obvious over Endoh and Hwang. Pet. 10. For the reasons explained below, Petitioner has not shown that it is reasonably likely to prevail on this ground.

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are “such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” We resolve the question of obviousness on the basis of

underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.⁴ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. Overview of Endoh

Endoh describes a memory transistor formed by the side wall of of multiple pillar-shaped semiconductor layers in a matrix arrangement. Ex. 1008, 3.⁵ Figure 2(a), reproduced below, illustrates an example.

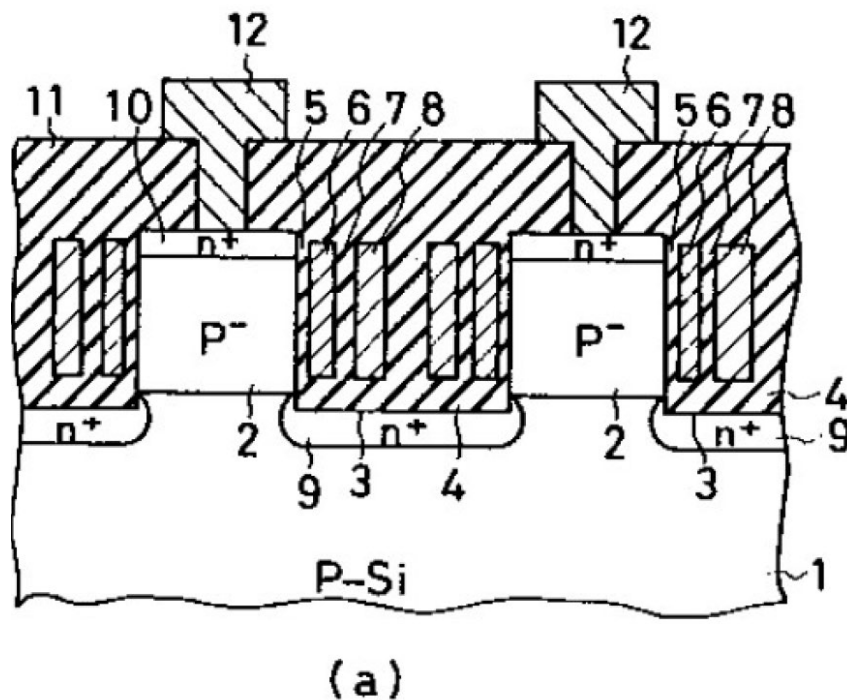


Figure 2(a) is a section diagram of an electrically readable programmable read-only memory (EEPROM) cell. *Id.* at 3, 8. P-type silicon substrate 1 is

⁴ The record does not include allegations or evidence of objective indicia of nonobviousness.

⁵ We use the pagination in the upper-right corners of the English translation.

separated by plaid-shaped groove 3, presenting multiple pillar-shaped P-type silicon layers in a matrix arrangement (shown in Figure 1 below). *Id.* at 3. Tunnel oxidation film 5 and floating gate 6 are formed on a side wall of groove 3 by surrounding pillar-shaped silicon layer 2. *Id.* Layer dielectric film 7 and control gate 8 are formed outside of floating gate 6. *Id.* Common source diffused layer 9 is formed at the bottom of groove 3 and drain diffused layer 10 of multiple memory cells is formed on multiple instances of pillar-shaped silicon layer 2. *Id.*

Figure 7(a) of Endoh is reproduced below:

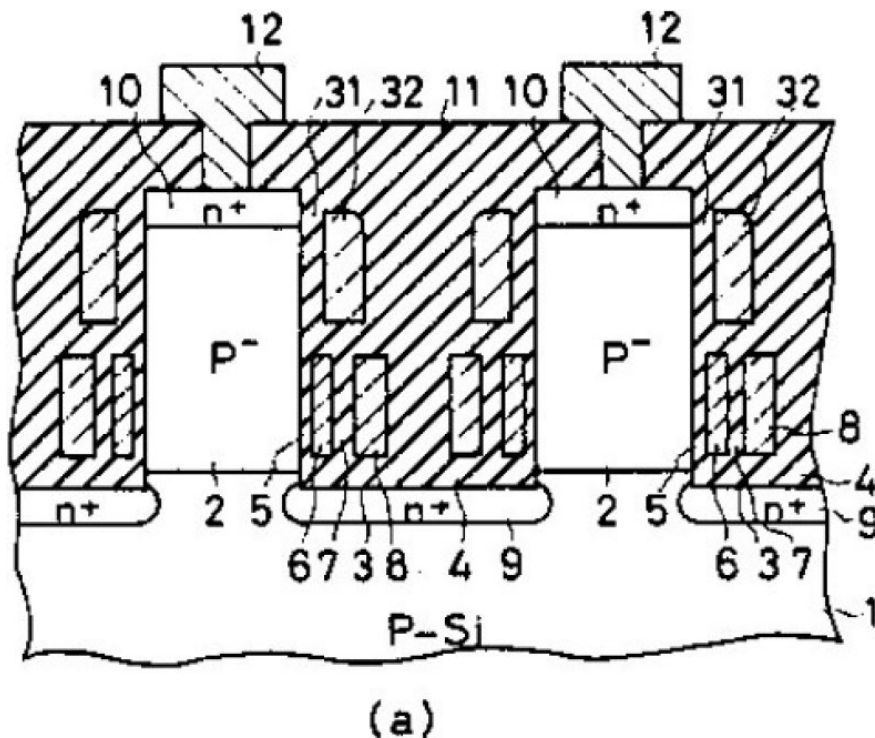


Figure 7(a) is a section diagram of an EEPROM cell. *Id.* at 5, 8. Endoh's description of Figure 7(a) is similar to that of Figure 2(a). *Id.* at 5–6. Petitioner cites a similar disclosure in Endoh for this second embodiment of a memory cell. Pet. 19 (citing Ex. 1008, 5).

Figure 1 of Endoh is reproduced below.

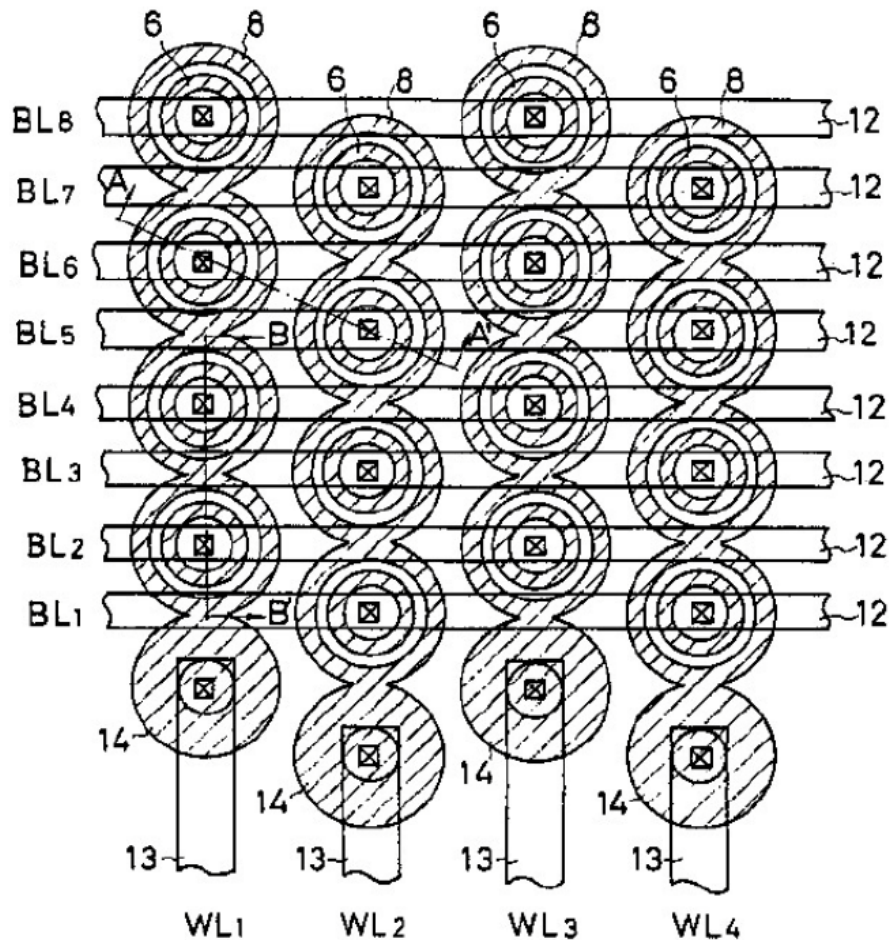


Fig. 1

Figure 1 is a plane diagram of the EEPROM cell shown in Figure 2(a); specifically, Figure 2(a) is a section of Figure 1 along line A—A'. Ex. 1008, 3, 8. Figure 1 shows a matrix arrangement of multiple pillar-shaped silicon layers. *Id.* at 3. Bit lines (BL1-BL8) of drain diffused layer 10 and word lines (WL1-WL4) 13 form AL wiring 12. *Id.*

2. Overview of Hwang

Hwang describes semiconductor memory devices with memory cells arranged vertically. Ex. 1009, 1:16–18. Figure 4D of Hwang, reproduced below, illustrates an example:

FIG. 4D

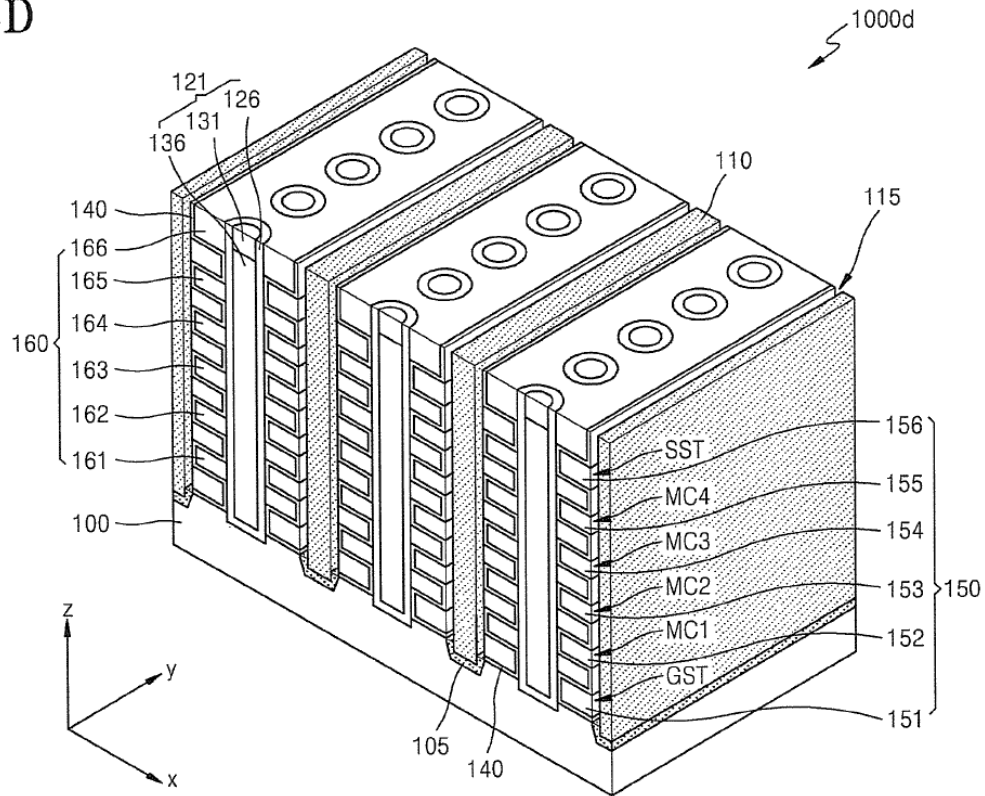


Figure 4D is a three-dimensional perspective view of a semiconductor memory device. *Id.* at 4:42–44.

Gate electrodes 150 are separated by interlayer insulating layers 160. *Id.* at 9:28–31. Gate dielectric layers 140 are disposed between semiconductor regions 120 and gate electrodes 150, and are disposed to cover upper and lower surfaces of gate electrodes 150 and a side of interlayer insulating layers 160 opposite to semiconductor regions 120. *Id.* at 9:39–44. Gate dielectric layers 140 also are disposed between gate electrodes 151 of the ground selection transistors GST and substrate 100. *Id.* at 9:44–46. When the ground selection transistors GST are turned on,

channels are created in the regions of substrate 100 underlying gate electrodes 151 so that semiconductor regions 120 and impurity regions 105 are electrically connected. *Id.* at 9:46–50.

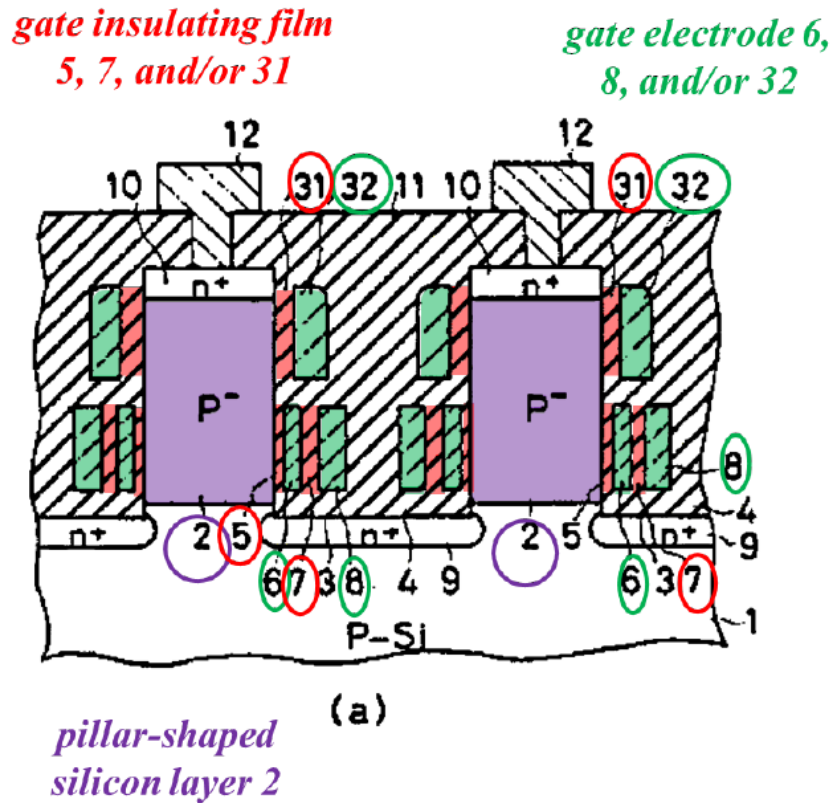
A plurality of substrate contact electrodes 110 are disposed in ohmic contact with respective ones of impurity regions 105. *Id.* at 10:6–11. If impurity regions 105 have a conductivity type opposite to that of substrate 100, substrate contact electrodes 110 may be coupled to a common source line CSL. *Id.* at 10:20–23. Substrate contact electrodes 110 are insulated from gate electrodes 150 by insulating regions 115 (e.g., air gaps). *Id.* at 10:35–38.

3. *Analysis of Claims 1–3*

As to claim 1, Petitioner contends that Endoh teaches limitations 1.1–1.4. Pet. 29–43. As to claim limitations 1.5–1.6, Petitioner cites the combination of Endoh and Hwang. *Id.* at 43–54.

With reference to Figures 2(a) and 7(a) of Endoh (both reproduced above), Petitioner contends that pillar-shaped silicon layers 2 provided on silicon substrate 1 are “a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region,” as recited in claim limitation 1.1. Pet. 29–33 (citing Ex. 1008, 3–5; Ex. 1003 ¶¶ 74–82).

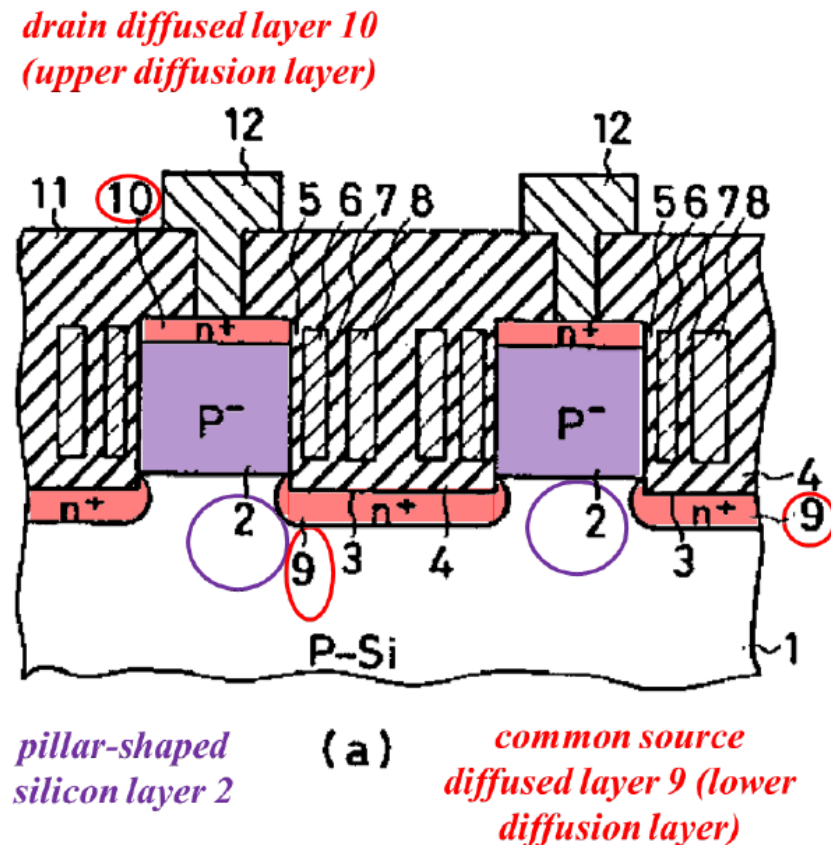
Petitioner further contends that tunnel oxidation film 5, floating gate 6, layer dielectric film 7, and control gate 8 teach “a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars,” as recited in claim limitation 1.2. *Id.* at 33–38 (citing Ex. 1008, 3, 5, 7; Ex. 1003 ¶¶ 83–87). Petitioner illustrates these aspects in its annotation of Endoh’s Figure 7(a), reproduced below:



EX1008, Endoh, FIG. 7(a), annotated

The figure above is a section diagram of an EEPROM cell annotated to add purple coloring and labeling for pillar-shaped silicon layer 2; red coloring and labeling for gate insulating film 5, 7, 31; and green coloring and labeling for gate electrode 6, 8, 32. Pet. 36.

As to claim limitation 1.3, “an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain,” and claim limitation 1.4, “a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain,” Petitioner points to drain diffused layer 10 and common source diffused layer 9, respectively. *Id.* at 38–43 (citing Ex. 1008, 4–6; Ex. 1003 ¶¶ 88–95). Petitioner illustrates these aspects in its annotation of Endoh’s Figure 2(a), reproduced below:



EX1008, Endoh, FIG. 2(a), annotated

The figure above is a section diagram of an EEPROM cell annotated to add purple coloring and labeling for pillar-shaped silicon layer 2 and red coloring and labeling for drain diffused layer 10 and common source diffused layer 9. Pet. 41–42.

Patent Owner does not dispute these aspects of claim 1. The parties dispute whether Endoh and Hwang teach claim limitation 1.5.

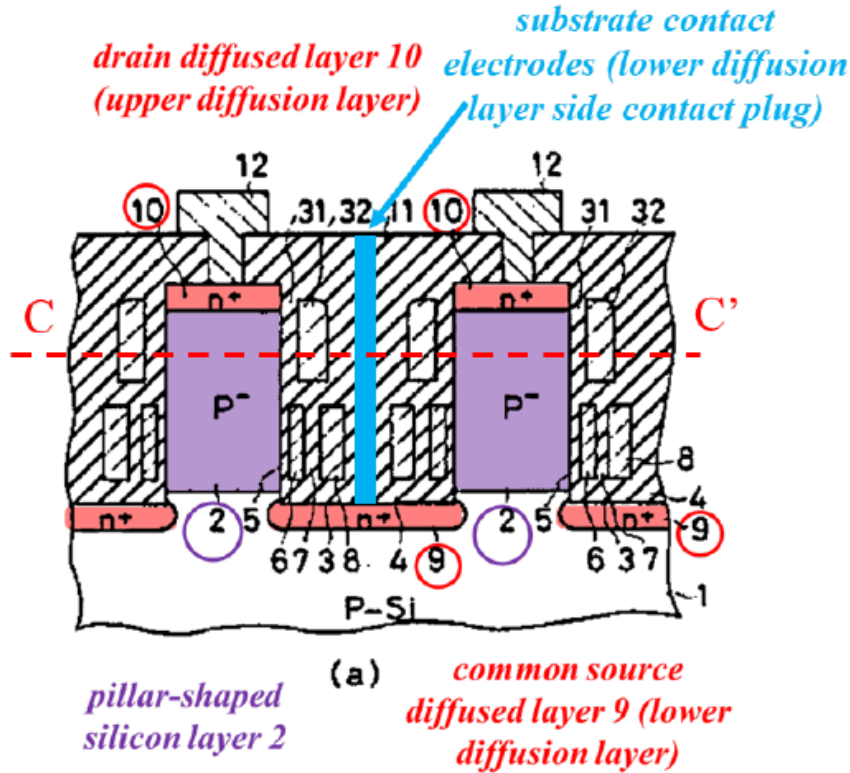
As to claim limitation 1.5, “a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug,” Petitioner does not contend that Endoh describes a contact plug connected to common source diffused layer 9. However, Petitioner argues

that a skilled artisan would have combined Endoh's teachings with Hwang's teachings of substrate contact electrodes 110 (alleged contact plugs) connecting impurity regions 105 (an alleged lower diffusion layer) to a common source line CSL. Pet. 46–48 (citing Ex. 1009, 10:6–11, 10:20–24, 12:13–15, Fig. 4D; Ex. 1003 ¶¶ 101–102). According to Petitioner,

a [person of ordinary skill in the art] would have been motivated to apply Hwang's teachings of the vertical structure arrangement including the vertical contact plug (substrate contact electrodes 110) providing connection between the bottom source region (impurity regions 105) to a common source line (CSL) in the semiconductor devices of Endoh, because Hwang's teachings provide the connection between the bottom source region to a common source as needed by Endoh, while providing the obvious, beneficial, and predictable results of high integration density and improved performance (e.g., reduced parasitic capacitance, improved reliability, more uniform electronic characteristics).

Id. at 48 (citing Ex. 1009, 1:27–32, 10:35–46, 12:8–13; Ex. 1003 ¶ 103).

Petitioner provides the following annotation of Endoh's Figure 7(a) to add in Hwang's substrate contact electrode:



**Cross-section of Example 1 of Endoh Combined with Hwang
(Annotated Based on EX1008, Endoh, FIG. 7(a))**

The figure above is a section diagram of an EEPROM cell annotated to add purple coloring and labeling for pillar-shaped silicon layer 2; red coloring and labeling for drain diffused layer 10 and common source diffused layer 9; and a blue bar and labeling for a substrate contact electrode provided from Hwang. *Id.* at 26.

Petitioner argues that Endoh itself provides a motivation to use Hwang’s teachings. *Id.* at 24. Specifically, Petitioner argues that Endoh expresses a “need to provide a connection between the n-type common source diffused layer 9 (at the bottom of the semiconductor pillars) and the common source line (CSL) (above the top of the semiconductor pillars).” *Id.* at 46 (citing Ex. 1003 ¶ 100); *see also id.* at 44 (“Endoh has the need to

provide a connection between the n-type common source diffused layer 9 (at the bottom of the semiconductor pillars) and the common source line (CSL) (above the top of the semiconductor pillars)” (citing Ex. 1003 ¶ 97)).

Petitioner argues that Endoh’s Figures 9a and 9b, reproduced below (rotated 90°), illustrate a common source S connected to a common source diffused layer.

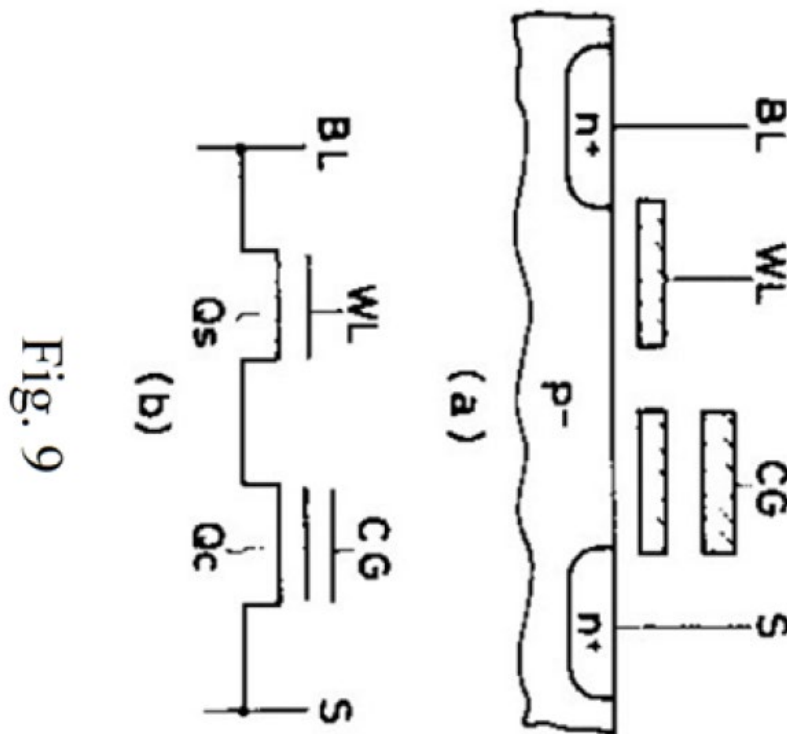


Figure 9a is a planer structure of an EEPROM cell and Figure 9b is a circuit diagram of the EEPROM cell of Figure 9a. Ex. 1008, 6, 8. Both figures are rotated 90°, as Petitioner does in reproducing these figures in the Petition. Pet. 46.

In response, Patent Owner argues that, even in Petitioner’s depictions of Endoh’s memory cells, a common source “S” is shown only toward the bottom of the device, and not above the top of the semiconductor pillars. Prelim. Resp. 12. Patent Owner further points out, correctly in our view, that Endoh’s remaining figures and description show a source only toward

the bottom of the device. *Id.* at 13–14 (citing Ex. 1008, 1, 3–4, 8, Figs. 2–4, 7, 8, 10, 13, 14). For example, in Figures 2(a) and 7(a), both reproduced above, common source diffused layer 9 is depicted below pillar-shaped silicon region 2, near the bottom of the drawings. We note that Endoh’s description of Figures 9a and 9b, relied upon by Petitioner, does not describe a location for common source “S” or describe any common source lines. Ex. 1008, 6–7. Patent Owner further argues that Hwang depicts an embodiment in which the common source line CSL is toward the bottom of the semiconductor device, which would undermine any inherency argument had Petitioner made such an argument. Prelim Resp. 15–16 (citing Ex. 1009, 6:28–34, Fig. 1).

Patent Owner argues that, because Petitioner’s reason to combine Endoh and Hwang rests on Endoh’s expression of a need to connect common source diffused layer 9 to a common source line above the top of the semiconductor pillars, and because Petitioner has presented no such evidence of a need in Endoh, Petitioner provides no reason to combine Endoh and Hwang to arrive at claim limitation 1.5. *Id.* at 17–18. We agree with Patent Owner. Endoh does not appear to teach a position of a common source line CSL and, thus, does not express a need for a means, such as a vertical contact plug, to connect common source diffused layer 9 to a common source line CSL above the top of pillar-shaped silicon layer 2. Dr. Lee’s testimony largely repeats the arguments in the Petition and, thus, does not provide any additional persuasive evidence from which we might conclude that Endoh’s device has a common source line CSL above pillar-shaped silicon layer 2, or any evidence that placement of a common source line CSL above pillar-shaped silicon layer 2 would have been obvious. *See* Ex. 1003 ¶¶ 66–68, 97–100, 103–105. Thus, we are not persuaded that

Endoh expresses a need to connect its common source diffused layer 9 to a common source line CSL above pillar-shaped silicon layer 2.

Petitioner also argues that Endoh provides “the needs to connect a bottom common source region to a common source line and to achieve high memory cell density and improved performance.” Pet. 24 (citing Ex. 1003 ¶ 66). Petitioner points to the “large barrier” described in Endoh to “achieving the purpose of reducing the area of memory cell and enlarging the capacitance of EEPROM,” and that the placement of drain diffused layer 10 “can reduce the area of isolation region of elements, so as to make the size of memory cell smaller.” *Id.* at 25 (quoting Ex. 1008, 2, 3). However, Petitioner does not point to any teaching in Endoh suggesting that connecting a bottom source region, the common source diffused layer 9, to a common source line, wherever it might be located, has an impact on memory cell density, size, capacitance, or performance. Dr. Lee’s testimony merely repeats the argument in the Petition, without adding to it materially, and, thus, is unhelpful. *See* Ex. 1003 ¶ 66. In sum, Petitioner’s evidence does not support a finding that Endoh provides a need for Hwang’s teachings.

As to Hwang, Petitioner argues:

A [person of ordinary skill in the art] with Endoh would have looked to Hwang and been motivated to apply Hwang’s teachings of the vertical structure arrangement of the vertical contact plug and the vertical channels in the semiconductor devices of Endoh, because Hwang’s teachings (1) provide the connection between the bottom source region to a common source line as needed by Endoh, and (2) provide the obvious, beneficial, and predictable results of high integration density and improved performance (e.g., reduced parasitic capacitance, improved reliability, more uniform electronic characteristics) with the vertical channel and contact arrangement and features.

Pet. 25 (citing Ex. 1009, 1:27–32, 10:35–46, 12:8–13; Ex. 1003 ¶ 67).

Patent Owner argues that Petitioner does not explain how Hwang’s teachings would have increased integration density of Endoh’s system or improved its performance. Prelim. Resp. 19. We agree. None of Petitioner’s citations to Hwang support the premise that the feature Petitioner seeks to incorporate from Hwang, a vertical contact plug, contributes to high integration density and improved performance. Ex. 1009, 1:27–32, 10:35–46, 12:8–13. Dr. Lee’s testimony merely repeats the argument in the Petition, without adding to it materially, and, thus, is unhelpful. *See* Ex. 1003 ¶ 67. Petitioner’s evidence does not show that Hwang provides a reason to combine the teachings of Endoh and Hwang.

Petitioner further argues that “applying Hwang’s teachings in embodiments of Endoh would have been no more than the combination of known elements according to known methods (e.g., incorporating the arrangement of the vertical channels and vertical contact plugs according to the known processing steps) obvious to a [person of ordinary skill in the art].” Pet. 26–27. “The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). However, “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does,” “because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *Id.* at 418–19. Here, Petitioner does not provide a reason, with rational underpinning, to combine the known elements of Endoh and Hwang. Thus, Petitioner has not demonstrated a

reasonable likelihood that it would prevail with respect to claims 1–3 as obvious over Endoh and Hwang.

D. Obviousness over Takaishi

Petitioner contends that claims 1–4 would have been obvious over Takaishi. Pet. 10. For the reasons explained below, Petitioner has not shown that it is reasonably likely to prevail on this ground.

1. Overview of Takaishi

Takaishi is directed to semiconductor devices having a vertical surrounding gate transistor (SGT) structure. Ex. 1007 ¶ 2. Figure 1, reproduced below, illustrates an example.

FIG. 1

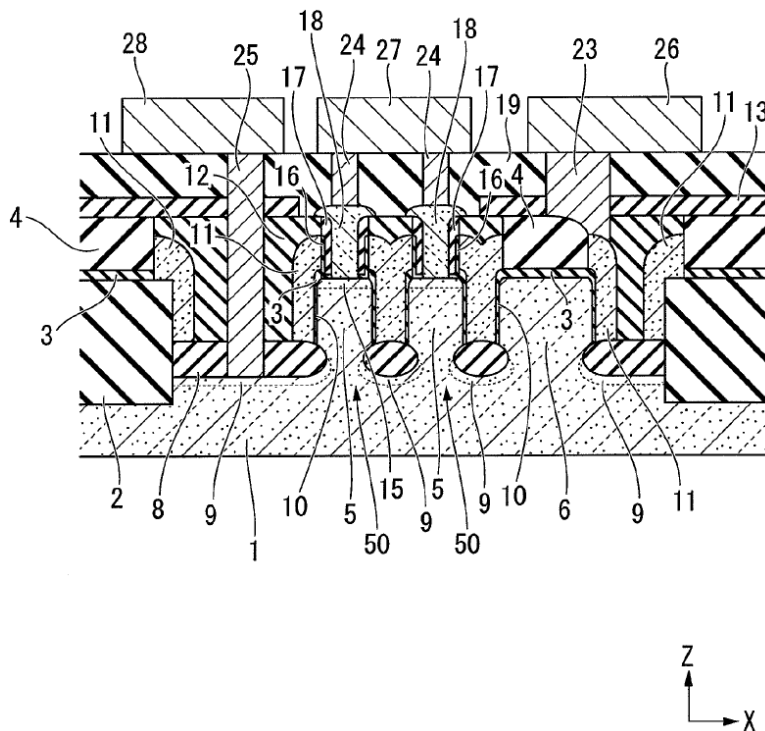


Figure 1 is a schematic view showing the cross section of the structure of a semiconductor device. *Id.* ¶¶ 19, 26.

Shallow trench isolation (STI) 2, which separates semiconductor devices, is provided in silicon substrate 1. *Id.* ¶ 26. Silicon pillars 5 stand around the center of an area surrounded by STI 2. *Id.* Each silicon pillar 5 forms a channel and parts of a source section and a drain section of each unit transistor 50. *Id.* Lower diffused layers 9 are formed at the lower end portions of silicon pillars 5 and are connected to each other. *Id.* ¶ 27. They serve as source diffused layers. *Id.* Upper diffused layers 15 are formed at the upper end portions of silicon pillars 5. *Id.* They serve as drain diffused layers. *Id.* Gate insulating films 10 are formed on side faces of silicon pillars 5 and gate electrodes 11 are formed over the surfaces of silicon pillars 5 with gate insulating films 10 interposed therebetween. *Id.* ¶ 30. Metal drain wire 28 is formed on metal contact plug 25, is connected to lower diffused layer 9 through metal contact plug 25, and functions as a common drain wire of unit transistors 50. *Id.* ¶¶ 35, 39.

Figure 2 of Takaishi is reproduced below:

FIG. 2

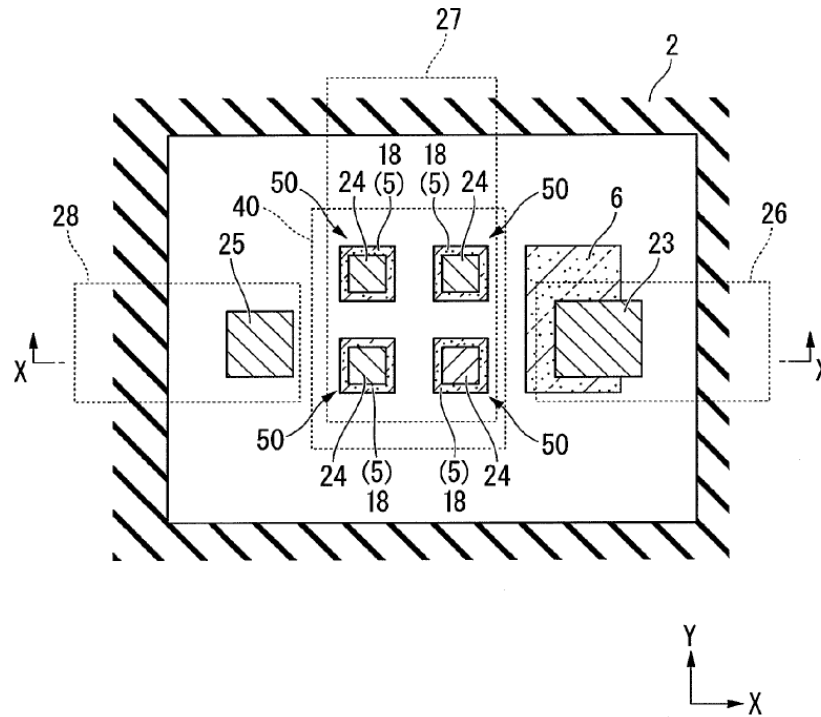


Figure 2 is a plan view showing the structure of the semiconductor device of Figure 1. *Id.* ¶¶ 20, 36. Silicon pillars 5 are arranged in a matrix along the X direction and the Y direction. *Id.* ¶ 36. Metal contact plug 25 is formed on the left of the group of silicon pillars 5, on the side opposing gate-lifting pillar 6. *Id.* ¶ 39.

2. Analysis of Claims 1–4

As to claim 1, Petitioner contends that Takaishi’s silicon pillars 5 are “a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region,” as recited in claim limitation 1.1. Pet. 64–67 (citing Ex. 1007 ¶¶ 26–27; Ex. 1003 ¶¶ 135–141).

As to claim limitation 1.2, Petitioner contends that gate insulating film and gate electrode 11 teach “a gate insulating film and a gate electrode

provided over a side surface of each of the semiconductor pillars.” *Id.* at 67–70 (citing Ex. 1007 ¶¶ 19, 30; Ex. 1003 ¶¶ 142–146).

As to claim limitation 1.3, Petitioner contends that upper diffused layer 15 is “an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain,” in this case, a source. *Id.* at 70–72 (citing Ex. 1007 ¶¶ 27, 34, 36; Ex. 1003 ¶¶ 147–152).

As to claim limitation 1.4, Petitioner contends that lower diffused layer 9 is “a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain,” in this case, a drain. *Id.* at 73–75 (citing Ex. 1007 ¶¶ 27, 36; Ex. 1003 ¶¶ 153–158).

As to claim limitation 1.5, Petitioner contends that metal contact plug 25 is “lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug.” *Id.* at 75–78 (citing Ex. 1007 ¶¶ 35, 39; Ex. 1003 ¶¶ 159–164).

Patent Owner does not challenge these aspects of claim 1. The parties dispute whether Takaishi teaches claim limitation 1.6, “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug.”

Petitioner first contends that Takaishi’s description of its silicon pillars 5 as “**arranged in a matrix along the X direction and the Y direction,**” as depicted in Takaishi’s Figure 2, reproduced above, shows that the pillars are uniformly arranged near metal contact plug 25. Pet. 78–79 (quoting Ex. 1007 ¶ 36; citing Ex. 1003 ¶¶ 166–167). As explained above, we construe “the semiconductor pillars are uniformly arranged near the lower diffusion layer side contact plug” to mean “the maximum interval

between the contact plug and the semiconductor pillars is twice or less the minimum interval between the contact plug and the semiconductor pillars.” Although we do not presume that Takaishi’s Figure 2 is drawn to scale, *see Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (“figures in a patent are not drawn to scale unless otherwise indicated”), Petitioner does not argue, or present evidence, that the interval between contact plug 25 and the top-right pillar 5 is twice or less the interval between contact plug 25 and the lower-left pillar 5. We see nothing in Figure 2 or Takaishi’s description to suggest that it is (Figure 2 appears to suggest the opposite). Thus, Petitioner’s first argument is not persuasive.

Second, Petitioner argues that Takaishi teaches claim limitation 1.6 even if “‘*uniformly arranged*’ requires the distance configuration of the first embodiment of the ’233 patent (EX1001, FIG. 1, 4:35–42).” Pet. 79–80.

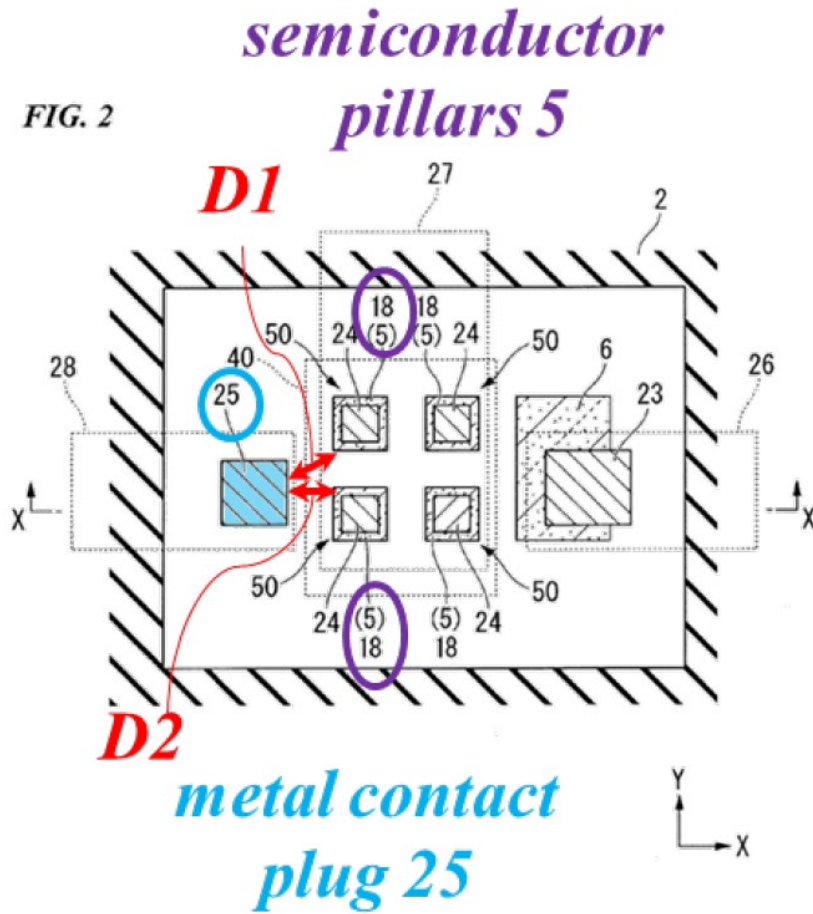
Petitioner argues that

a [person of ordinary skill in the art] would have understood that the claim term “*uniformly arranged*” at least includes an example arrangement as explicitly provided by the ’233 patent, e.g., an arrangement that “the distance between the metal contact plug 31 and a closest portion of the unit transistor farthest from the metal contact plug 31 is twice or less the distance between the metal contact plug 31 and a closest portion of the unit transistor closest to the metal contact plug 31.”

Id. at 80 (quoting Ex. 1001, 4:35–42). Here, we understand Petitioner to argue that Takaishi teaches claim limitation 1.6 under our construction.

Referring to its annotated version of Takaishi’s Figure 2, reproduced below, Petitioner argues that “the distance (D1) between the metal contact plug 25 and the top left semiconductor pillar 5 is twice or less the distance (D2) between the metal contact plug 25 and the bottom left semiconductor pillar 5.” *Id.* at 81 (citing Ex. 1007 ¶ 36).

FIG. 2



EX1007, Takaishi, FIG. 2, annotated

The above figure is a plan view of a semiconductor device, annotated by Petitioner to add purple coloring and labeling for silicon pillars 5; blue coloring and labeling for metal contact plug 25; and red arrows and labeling for distances D1 and D2. *Id.* at 81. Petitioner argues that “it would have been obvious to a [person of ordinary skill in the art] [to] use such arrangements for all the semiconductor pillars for the benefit of ‘miniaturized and highly integrated semiconductor devices’ with improved performance by providing similar electronics characteristics related to each semiconductor pillar.” *Id.* at 81–82 (quoting Ex. 1007 ¶ 40; citing Ex. 1003 ¶ 172). We agree with Patent Owner (Prelim. Resp. 26–27), however, that

the portion of Takaishi cited by Petitioner does not connect the benefits of miniaturized and highly integrated semiconductor devices to the distances between the pillars and the contact plug or identify a need for similar electronics characteristics related to each pillar. Ex. 1007 ¶ 40.

Petitioner acknowledges that we should not presume Figure 2 is drawn to scale, but argues that this figure, “together with Takaishi’s description, reasonably depicts the important features of the device and the relative positions of the elements in the device, including the relative positions of the silicon pillars 5 and the vertical contact plug 25 and the relative distances D1 and D2 as discussed above.” *Id.* at 82 (citing Ex. 1003 ¶ 173). Here, it is unclear whether Petitioner argues that all four pillars 5 would satisfy claim limitation 1.6, or whether it argues that it is only necessary to show that the two left pillars 5 are uniformly arranged near metal contact plug 25. However, as Patent Owner observes (Prelim. Resp. 21), Petitioner, earlier in the Petition, makes clear that “[w]hile the discussion and annotation mainly focus on the two left silicon pillars 5 in FIG. 2, the analysis similarly applies to each silicon pillar 5.” Pet. 66. And, as Patent Owner further observes (Prelim. Resp. 22–23), Petitioner repeatedly refers to the bottom two pillars 5 in its annotations to Takaishi’s Figure 1. Pet. 65, 68, 71, 73, 76. Thus, Petitioner appears to argue that all four pillars 5 depicted in Takaishi’s Figure 2 would have been uniformly arranged near metal contact plug 25.

Once again, however, Petitioner does not point to persuasive evidence that pillars 5 shown in Figure 2 are arranged, relative to contact plug 25, such that “the maximum interval between the contact plug and the semiconductor pillars is twice or less the minimum interval between the contact plug and the semiconductor pillars.” Figure 2 itself does not appear

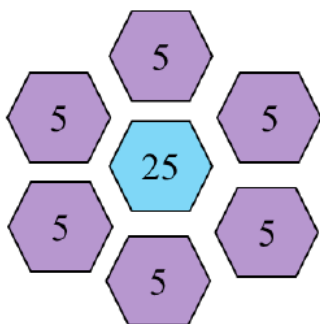
to depict such a relationship and Takaishi's description does not describe it. Ex. 1007 ¶¶ 36–39. Dr. Lee's testimony largely repeats the arguments in the Petition, without adding to them materially. *See* Ex. 1003 ¶¶ 168–173. Such conclusory and unsupported testimony adds little to the Petitioner's arguments and is entitled to little weight. *See Xerox Corp. v. ByteMark, Inc.*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential); 37 C.F.R. § 42.65(a).

Petitioner (Pet. 82–83) further cites to paragraph 40 of Takaishi, which provides, in reference to Figure 2:

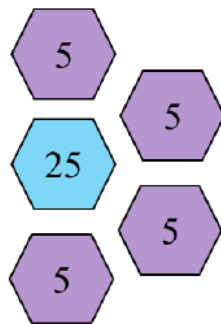
The shape, the number, and the arrangement of the silicon pillars 5 are not limited to those of this example. For instance, the shape of the cross section of the silicon pillars 5 in the XY plane may be a circle, or a polygon other than a rectangle. Moreover, when forming a large number of silicon pillars 5, these silicon pillars 5 may be arranged in a honeycomb-shape to form a closed packing structure, thereby making it possible to realize miniaturized and highly integrated semiconductor devices.

Ex. 1007 ¶ 40. Dr. Lee provides three examples of honeycomb-shaped structures that he contends would have rendered obvious claim limitation

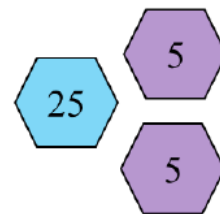
1.6. Ex. 1003 ¶ 176. These examples are reproduced below:



**Example A of First
Embodiment of
Takaishi**



**Example B of First
Embodiment of
Takaishi**



**Example C of First
Embodiment of
Takaishi**

The three figures above, Examples A, B, and C, are arrangements of pillars 5 (shown in purple) relative to metal contact 25 (shown in blue). Petitioner argues that a skilled artisan “would have been motivated to use suitable pillar numbers and arrangements based on a particular design need (e.g., an arrangement with a larger number of semiconductor pillars for a higher current/power requirement).” Pet. 83. Dr. Lee repeats this argument in his testimony, without providing a basis for that testimony. Ex. 1003 ¶ 176.

Dr. Lee testifies that “[f]or Example A, it would have been obvious to a [person of ordinary skill in the art] to form metal line contacts to the contact plug 25 and to the silicon pillars 5 using two metal levels (a well-known multi-level metallization technology) in order to avoid metal wire shorting.” Ex. 1003 ¶ 177. As to Example B, Dr. Lee testifies that a skilled artisan “would have been motivated to use suitable pillar numbers and arrangements based on a particular design need (e.g., an arrangement with a larger number of semiconductor pillars for a higher current/power requirement).” *Id.* As to Example C, he testifies that it is “very similar to Fig. 2 of Takaishi except that only the left two silicon pillars 5 are included, and the right two silicon pillars are eliminated.” *Id.* As to each of these examples, Dr. Lee’s testimony is conclusory, does not explain why he chose the particular arrangement, and is without a stated basis. As such, this testimony is entitled to little weight. *See Xerox*, Paper 9 at 15; 37 C.F.R. § 42.65(a).

Moreover, to the extent Petitioner’s argument, and Dr. Lee’s testimony, is based on paragraph 40 of Takaishi, this paragraph says nothing about the positional relationship between pillars 5 and metal contact plug 25. Ex. 1007 ¶ 40; Prelim. Resp. 27. We agree with Patent Owner that “Takaishi does not provide *any* teaching that the uniform arrangement near

the contact plug recited in limitation [1.6] is desirable.” Prelim. Resp. 28. If anything, Takaishi’s description of locating silicon pillars 5 “in the XY plane . . . around the center of an area surrounded by the STI 2” and metal contact plug 25 “at an intermediate area between the silicon pillars 5 and the STI 2 where no gate electrodes 11 are formed,” Ex. 1007 ¶¶ 35–36, suggests that a skilled artisan would not have located pillars 5 surrounding metal contact plug 25, as in Dr. Lee’s examples. Prelim. Resp. 33–37. Thus, even if Dr. Lee’s honeycomb arrangements of pillars are contemplated by Takaishi, there appears to be nothing other than hindsight supporting Dr. Lee’s proposed locations of the metal contact plug within those arrangements, rather than in an intermediate area apart from the arrangements. Prelim. Resp. 30–31; *KSR*, 550 U.S. at 421 (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning.”).

Finally, Petitioner argues that the prosecution history of the ’233 patent supports its argument that Takaishi teaches claim limitation 1.6 because the Examiner relied on Takashi to teach limitations of then-pending claims 2 and 4, which Petitioner argues are similar to limitation 1.6, and Patent Owner did not dispute such findings. Pet. 83 (citing Ex. 1006, 119–24, 133–42; Ex. 1003 ¶ 178). Patent Owner argues that the prosecution history supports the opposite conclusion, as the Examiner allowed claim 1 over Takaishi. Prelim. Resp. 37–38. We agree with Patent Owner. The Examiner initiated an interview with the patent applicant and suggested amendments to overcome the rejection, which the applicant accepted. Ex. 1006, 109–11, 117–26, 133–34. Thus, it appears that expressly contesting the Examiner’s findings as to then-pending claims 2 and 4 would have been unnecessary, leading us to draw no conclusion as to the

applicant's alleged failure to contest the Examiner's findings. Petitioner has not shown persuasively that the prosecution history of the '233 patent supports its position.

In sum, Petitioner's evidence does not support a finding that Takaishi teaches claim limitation 1.6, or that a skilled artisan would have modified Takaishi to arrive at claim limitation 1.6. Thus, Petitioner has not demonstrated a reasonable likelihood that it would prevail with respect to claims 1–4 as obvious over Takaishi.

III. CONCLUSION

For the foregoing reasons, we decline to institute an *inter partes* review of the '233 patent.

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is denied as to claims 1–4 of the '233 patent.

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