

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMA SOLAR TECHNOLOGY AMERICA, LLC,
Petitioner,
v.

TIGO ENERGY, INC.,
Patent Owner.

Patent 10,333,405
Filing Date: May 2, 2018
Issue Date: June 25, 2019
Title: SYSTEMS AND METHODS FOR ENHANCED EFFICIENCY
AUXILIARY POWER SUPPLY MODULE

Inter Partes Review No.: IPR2023-0113
Declaration of Douglas Holberg

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I. INTRODUCTION

- 1) I have been engaged by SMA Solar Technology America, LLC to opine on the patentability or otherwise of U.S. Patent No. 10,333,405 (—the `405 Patent), entitled —SYSTEMS AND METHODS FOR ENHANCED EFFICIENCY AUXILIARY POWER SUPPLY MODULE. My opinions are set forth herein. I submit this Declaration on behalf of SMA Solar Technology America, LLC in connection with its request for *inter partes* review of the `405 Patent.

A. Education and Relevant Experience

- 2) My education includes a B.S. in Electrical Engineering from Texas A&M University in 1977, followed by a M.S. in Electrical Engineering from the University of Texas at Austin in 1989. I earned a Ph.D. in Electrical Engineering from the University of Texas at Austin in 1992.
- 3) I have over 40 years of experience in the electronics field. During that time, I have worked for several different electronics companies including: Mostek, Texas Micro Engineering (acquired by Crystal Semiconductor), Crystal Semiconductor, Cirrus Logic, Cygnal Integrated Products, and Silicon Laboratories. I joined Silicon Laboratories when they acquired Cygnal, which I co-founded in 1999.
- 4) I am a named inventor on 43 U.S. granted patents. I have held a variety of engineering positions throughout my career, from circuit designer, design manager, Director of Engineering, Chief Technology Officer (CTO), Vice President (V.P.)

of Engineering, and V.P. of Technology. In addition to my engineering experience, I also have served as an adjunct faculty member at the University of Texas, where I taught CMOS analog and mixed-signal design for six years.

- 5) I am the co-author of the textbook —CMOS Analog Circuit Design, the first edition of which published 1987. As explained in the Preface of the second edition, published in 2002, the objective of the textbook is to teach the fundamentals and background that are necessary to understand how a —circuit works. It is now available in third edition and published in English and Chinese (first and second edition). This textbook is widely used throughout the world by new and experienced engineers in industry and by students in the classroom.
- 6) Upon graduating from Texas A&M University, I went to work for Mostek Corporation designing integrated circuits for telecommunications applications. I designed an integrated dual tone multi frequency (DTMF) generator. I received my first patent for this integrated DTMF generator. After leaving Mostek, I joined a startup company, Texas Micro Engineering, as the second employee. At Texas Micro Engineering, I designed, among other things, a dual-channel (atrium-ventricle) pacemaker sense amplifier/filter using discrete-time switched-capacitor technology.
- 7) While enrolled in the Masters/Ph.D. program at the University of Texas at Austin, I worked on the application of bipolar technology to dynamic random access

memory (DRAM) sense-amplifier architectures and circuit-simulation algorithms.

While at The University of Texas at Austin, I also designed and laid out the mask set (The Holberg Mask Set) still in use by the fabrication class/lab.

- 8) Upon graduating with a Ph.D. in Electrical Engineering, I went to work for Crystal Semiconductor/Cirrus Logic, where I designed high frequency synthesizers for hard-disk read-channel applications. I managed a group designing charge-coupled device (CCD) interface circuits for digital camera applications, as well as television encoder chips and CMOS imagers.
- 9) Upon leaving Cirrus, I started a company called Cygnal Integrated Products that developed mixed-signal microcontrollers. At Cygnal, I was the founder, CTO), V.P. of Engineering, and an individual contributor. While at Cygnal, I designed analog-to-digital converters (ADCs), V_{be} temperature sensors, input/output (I/O) cells/pads (both design and layout), as well as many additional miscellaneous circuits. My company was later purchased by Silicon Labs, where I remained employed as a manager of the microcontroller group, followed by the position of V.P. of Technology.
- 10) I have significant experience with the technology described in the '405 patent, including resistors, capacitors, diodes, inductors, transistors, transformers, oscillators, operational amplifiers, comparators, general integrated-circuit technology, analog/digital mixed-signal circuits, device analysis and modeling,

floor-planning, and layout of integrated circuits, and the tools used to design, and verify integrated circuits (CAD tools). In addition, I have experience with device modeling and characterization, which has been applied throughout my career.

- 11) My analyses set forth in this declaration are informed by my experience in the field of electrical engineering, including analog circuitry, ADCs, and digital circuits.

Based on my above-described experience, I believe that I am considered to be an expert in the field.

- 12) The `405 Patent is entitled —Systems and Methods for Enhanced Efficiency Auxiliary Power Supply Module. Prior to reviewing the `405 Patent, I was well familiar with the subject matter described and claimed therein. I am well familiar with circuits generally, such as disclosed in the `405 Patent.

B. Materials Considered

- 13) The analysis that I provide in this Declaration is based on my education and experience as an engineer, and upon my knowledge of CMOS integrated circuit design, as well as the documents I have considered, including the `405 Patent (Ex.1001). I have reviewed the prosecution history for the `405 Patent (Ex.1006).
- 14) I have reviewed various publications from the prior art at the time of the alleged invention of the `405 Patent. These publications, along with other materials I have reviewed, include those listed below:

- 15) Certified English Translation of German Publication DE3725476 (Mieth) (Ex. 1002).
- 16) U.S. Patent No. 6,246,592 (Balogh) (Ex. 1003).
- 17) U.S. Patent No. 6,798,177 (Liu) (Ex. 1005).
- 18) File wrapper of U.S. Patent No. 10,333,405 (Ex. 1006).
- 19) Allen, Philip E., and Douglas R. Holberg. "CMOS Analog Circuit Design" (2002) ("CMOS") (Ex. 1009).
- 20) Solibro GmbH CIGS THIN FILM SOLAR MODULE SL2 ("Solibro") (Ex. 1010).
- 21) MITSUBISHI ELECTRIC PHOTOVOLTAIC MODULE ("ME") (Ex. 1011).
- 22) US Patent application No. 2007/0001653 (Xu) (Ex. 1012).
- 23) U.S. Patent Publication No. 2006/0207192 (Durham) (Ex. 1013).
- 24) Arias et al., "A Modular PV Regulator Based on Microcontroller with Maximum Power Point Tracking," IEEE, IAS 2004. (Ex. 1014).
- 25) U.S. Patent No. 4,617,529 (Suzuki) (Ex. 1015).

II. LEGAL PRINCIPLES USED IN MY ANALYSIS

- 26) I understand that in writing this Declaration I am obliged to follow existing applicable law. I have therefore been asked to apply the following legal principles to my analysis, and I have done so.

A. Person Having Ordinary Skill in the Art

- 27) I understand that my assessment of the claims of the `405 Patent must be undertaken from the perspective of what would have been known or understood by a person having ordinary skill in the art, reading the `405 Patent on its relevant filing date and in light of the specification and file history of that patent. I often refer to such a person as a —PHOSITA in this Declaration.
- 28) I am informed and understand that various factors can be considered in determining a person having ordinary skill in the art (PHOSITA). I am informed and understand that those factors include: (1) the educational level of the inventor(s);
- 29) (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) the rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the field.
- 30) I understand that SMA Solar Technology America, LLC proposed in the Petition that a person having ordinary skill in the art (—PHOSITA) in the field of the `405 Patent in 2009 would have a bachelor's degree in electrical engineering, or a similar discipline and at least two years of experience designing circuits.
- 31) I agree with this level of ordinary skill for the `405 Patent. Based on my experience, I understand and know of the capabilities of a person of this skill level as of the time the `405 Provisional Patent was filed. (i.e., the priority application to which the `405 Patent claims its earliest priority) in 2009. I am familiar with how

a PHOSITA would have understood and used the terminology found in the `405 Patent at the time of its filing, and with the state of the art at that time.

32) My analysis and opinions regarding the claims of the `405 Patent have been based on the perspective of a PHOSITA as defined above as of September 2, 2009, the filing date of the provisional application to which the application which later issued as the `405 Patent claimed priority. As described above and as shown in my CV, I have extensive experience in the field of electronics in the relevant timeframe.

B. The Prior Art

33) I understand that applicable patent law provides categories of information that constitute prior art that may be used to anticipate patent claims or to render them obvious. I understand that for a reference to qualify as prior art to a particular patent claim under the relevant law, that reference must have been made, known, used, published, or patented, or must have been the subject of a patent application by another person, before the priority date of the patent, and in this matter, must satisfy one of the standards of pre-AIA 35 U.S.C. § 102.

C. Claim Construction Standard

34) In making this Declaration, I have been asked to review the terms in the `405 Patent claims to determine what a PHOSITA would have understood those terms to have meant at the time of the alleged invention. In addition, I have been informed that, in an *inter partes* review proceeding, the claim terms under

consideration are to be construed using the same claim construction standard used in a civil action under 35 U.S.C. § 282(b), which is articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. I further understand that under the *Phillips* standard, the claim terms are given their ordinary and customary meaning, as would be understood by a PHOSITA at the time of the invention, consistent with the specification and the prosecution history. My opinions regarding the meaning of claim terms of the `405 Patent are based on the construction of the claim terms using the *Phillips* standard in view of the specification and the prosecution history of the `405 Patent.

D. Anticipation

- 35) I understand that to be valid, a patent claim must be —novel, and that a claim is invalid if it is —anticipated by a single prior art reference. I further understand that a reference anticipates if it discloses each and every element of the claim and enables a PHOSITA to make and use the claimed invention without undue experimentation.

E. Obviousness

- 36) I also understand that even if a claim of a patent is not anticipated, that claim is still invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious to a PHOSITA at the time the invention was made.

37) I understand further that the condition “at the time the invention was made” in an obviousness determination is imposed to rule out impermissible hindsight.

Accordingly, permissible reasoning takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned from the applicant’s disclosure in the patent under analysis. I also understand that an opining expert is required to analyze prior art from the perspective of a PHOSITA and may not simply provide his or her own personal conclusions.

38) I also understand that an obviousness determination includes several factual inquiries, including: (1) determining the scope and content of the prior art;

39) (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any secondary indicia (objective evidence) of non-obviousness.

40) I also understand that such objective evidence of non-obviousness may include: (1) a long felt but unsolved need that was satisfied by the claimed invention; (2) commercial success attributable to the claimed invention; (3) unexpected results achieved by the claimed invention; (4) praise by experts of the claimed invention with factual support; (5) taking of licenses under the patent by others for reasons related to the alleged non-obviousness of the claimed invention;

41) (6) the failure of others; (7) the teaching away of others; (8) skepticism by experts; and (9) evidence that competitors in the marketplace have copied the invention instead of using the prior art. I also understand that, in order to establish non-obviousness, there must be a demonstrated relationship, or nexus, between any such secondary indicia and the claimed invention, i.e., there must be objective evidence of non-obviousness attributable to the claimed invention.

42) I further understand that near simultaneous invention by two or more equally talented inventors working independently may or may not be an indication of obviousness when considered in light of all the circumstances.

43) I understand that a conclusion of obviousness can be based on a combination of multiple prior art references. I understand that rationales that may support a conclusion of obviousness include:

(A) Combining prior art elements according to known methods to yield predictable results;

(B) Simply substituting one known element for another to obtain predictable results;

(C) Using known techniques to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) Using an —obvious to try solution, i.e., choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Applying known work in one field of endeavor to yield variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

(G) Applying some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference disclosures to arrive at the claimed invention.

- 44) I further understand that an analysis of obviousness should recognize that market demand, rather than scientific literature, often drives design trends.
- 45) I also understand that if a technique has been used to improve one device, and if a PHOSITA would recognize the technique would improve similar devices in the same way, then using that technique would be obvious to a PHOSITA unless actual application of that technique is beyond his or her skill.
- 46) I also understand that practical and common-sense considerations should guide an analysis of obviousness, because familiar items may have obvious uses beyond their primary purposes. I further understand that applying common sense does not require a —specific hint or suggestion in a particular reference. Rather, applying common sense requires a reasoned explanation that avoids conclusory generalizations and false deductions.

- 47) I also understand that, when addressing a problem, a PHOSITA will often be able to fit together the disclosures of multiple publications. In this regard, I understand that an analysis of obviousness may consider inferences and creative steps that a PHOSITA would normally employ.
- 48) I also understand that a particular combination of prior art may be proven obvious merely by showing that it was obvious for a PHOSITA to try that combination. For example, when there is a design need or a market pressure to solve a problem, and/or there exists a finite number of identified, predictable solutions with a reasonable expectation of success, a PHOSITA has good reason to pursue the known options within his or her technical grasp. I understand that if this leads to anticipated success, it is likely that the result is not of innovation but of ordinary skill and common sense.
- 49) I also understand that a combination of familiar elements according to known methods is presumed to be obvious when that combination does no more than yield predictable results. Work known in one field of endeavor may prompt variations of that work for use in either the same field or a different field, based on design incentives and other market forces. If a technique has been used to improve some device, and a PHOSITA can implement a predictable variation of that technique, then that variation is likely unpatentable.

- 50) I further understand that to be proper for use in an analysis of obviousness, a reference must teach art that is analogous to the claimed invention. I also understand that under a correct analysis, any need or problem known in the field of endeavor at the time of the invention and addressed by the claimed invention can provide a reason for combining the elements in the manner claimed.
- 51) I understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in that single reference can be supplied by the common sense or technical knowledge of a PHOSITA. For example, combining two embodiments disclosed adjacent to each other in a prior art patent likely does not require a leap of inventiveness.
- 52) I also understand that a claimed invention may be obvious if it merely involves simple substitution of one known element for another to obtain predictable results.
- 53) I understand further that, in an analysis of obviousness, two items of prior art need not be like two puzzle pieces that must fit together perfectly. For example, a claimed invention may be found obvious if a PHOSITA would view rearrangement as an obvious matter of design choice.
- 54) I also understand that an analysis of obviousness requires a comparison between the properly construed claim language and the prior art on a limitation-by-limitation basis.

III. BACKGROUND OF THE TECHNOLOGY

- 55) Comparators are a widely used component that detects and indicates the relationship between its two inputs. A symbol for a comparator is shown in Fig. 1 below, but can be illustrated in other ways as well.

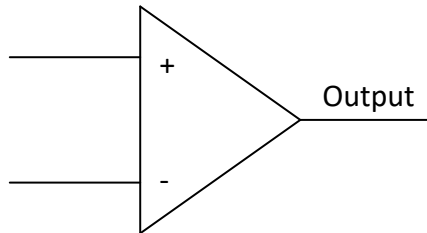


Fig. 1

- 56) The inputs are characterized as the positive input and the negative input. Sometimes also referred to as the non-inverting and inverting inputs, respectively. A comparator generally has, but is not limited to, a single output that indicates the relationship between the input signals at the positive and negative inputs. If the positive input is greater than the negative input, then the output of the comparator will be high. Alternatively, if the positive input is less than the negative input, then the output of the comparator is low. Theoretically for an ideal comparator, if the inputs are equal, the output is indeterminate. The ideal transfer curve for a comparator is shown in Fig. 2 below. (Ex. 1009, Fig 8.1-4).

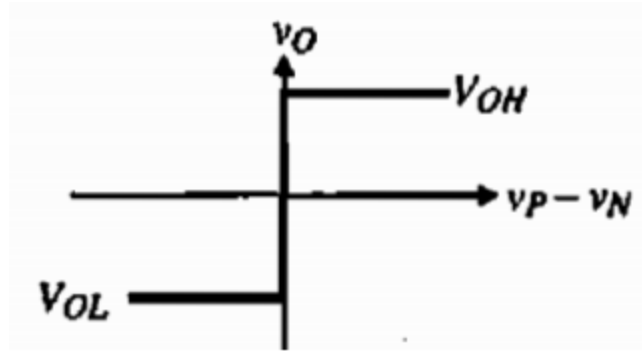


Fig. 2

57) Comparators, like all electronic devices, are subject to noise—both internal and external noise. When comparators are intrinsically noisy, or are placed in a noisy environment they can “chatter” when the input is close to the switching threshold (comparator threshold) (Ex. 1009, 462). This is illustrated in Fig. 3 below. (Ex. 1009, Fig 8.4-6a).

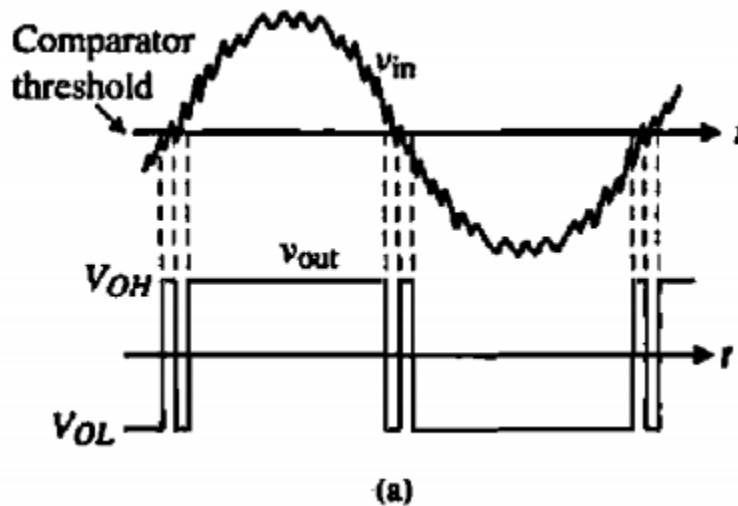


Fig. 3

58) As seen in Fig. 3, due to the noise on v_{in} (the positive input terminal of the comparator), at the comparator threshold, the noise of the signal bounces above and below the threshold, causing the signal at the output (v_{out}) to switch quickly or “chatter” between V_{OH} and V_{OL} , in some instances, multiple times depending upon the frequency of the noise on the input signal. One of the methods to avoid this “chatter” on a comparator output is to add hysteresis to the transfer function curve of the comparator. To add hysteresis, the trip threshold of the comparator is varied based on the state of the comparator. This can be understood as follows. When the input signal to the comparator is rising, the state of the comparator does not change until the input signal reaches a positive trip point threshold (V_{TRP}^+ as shown in Fig. 4 below). Once the state has changed due to the input signal exceeding the threshold, the trip-point threshold is reduced to a negative trip point so that the state of the comparator output does not change until the input signal falls below the negative trip point (V_{TRP}^- as shown in Fig. 4 below). This is illustrated in Fig. 4 below (Ex. 1009, Fig. 8.4-5).

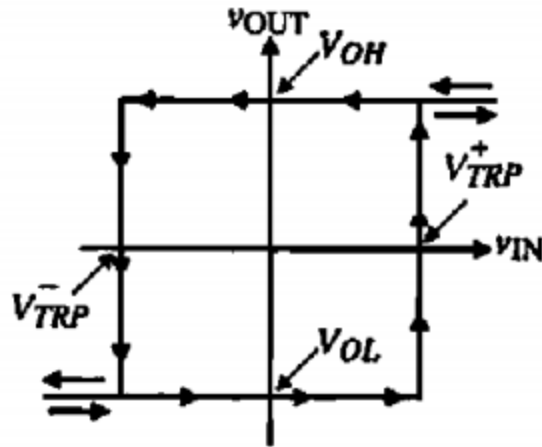


Fig. 4

- 59) As shown, the input signal, v_{IN} , starting from the left is low causing v_{OUT} to be low (V_{OL} or the “first state”). As v_{IN} increases to the right, a positive trip point is reached, V_{TRP}^+ . At that point v_{OUT} goes high (V_{OH} or the “second state”). v_{IN} can continue increasing with no change in state. As v_{IN} starts decreasing, the output, v_{OUT} , remains high (second state) until it reaches a negative trip point threshold V_{TRP}^- (which is lower than the initial positive trip point V_{TRP}^+) causing the comparator output, v_{OUT} , to go low (first state).
- 60) Once hysteresis is introduced to the comparator, the “chatter” effect is removed as long as the noise amplitude on the signal is less than the difference of the positive and negative trip voltages (i.e., keeping the noise less than the hysteresis “window”). This is illustrated in Fig. 5 below (Ex. 1009, Fig. 8.4-6b) where the “chatter” on the output signal of the comparator no longer exists.

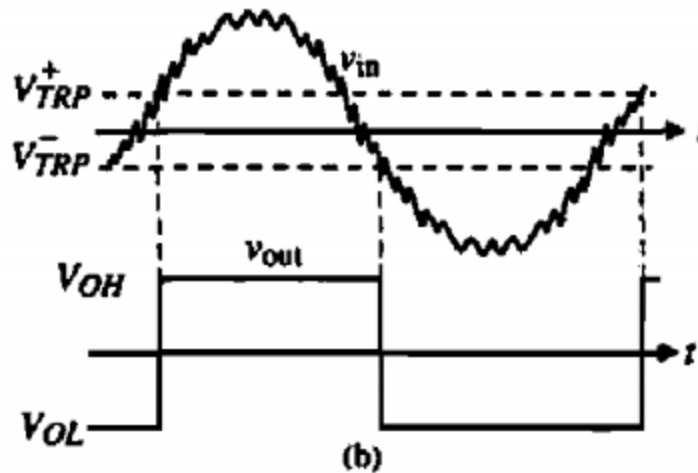


Fig. 5

- 61) When the signals at the positive and negative inputs cross (e.g., when the positive input becomes greater than the negative input), the state of the comparator output changes (e.g., goes from a low state to a high state in this case). This transition does not happen instantaneously—there is some intrinsic delay. This delay is generally referred to as propagation delay as illustrated in Fig. 6 below (Ex. 1009, Fig. 8.1-9). In fact, nothing in real-world circuitry happens instantaneously, i.e., without delay.

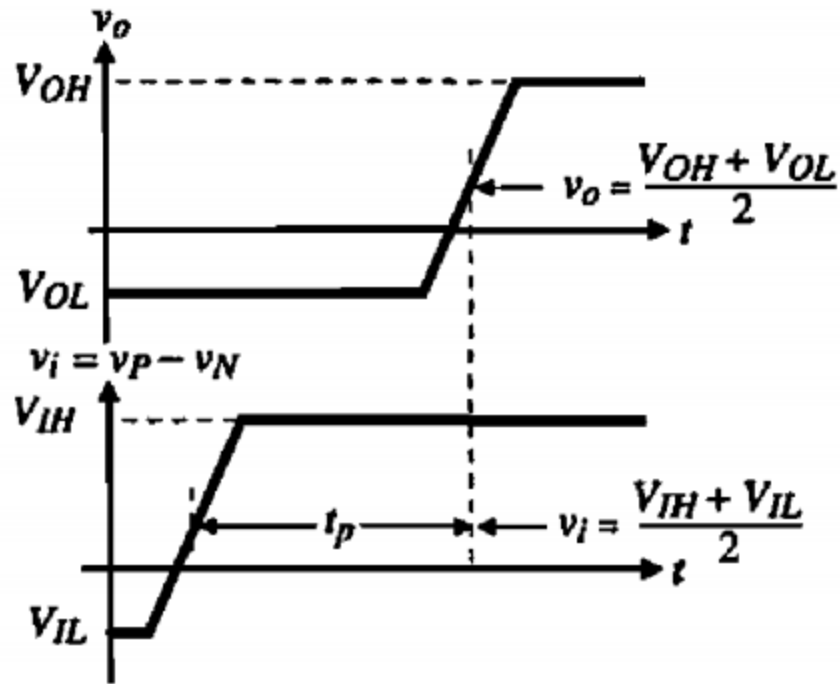


Fig. 6

62) As can be seen in the figure, if the midpoint of the transition is taken as the reference point between the low state and high state of both the input signal and the output signal, respectively, it is clear that a delay of t_p represents the time delay between the transition at the comparator input and the corresponding signal transition at the comparator output. This delay, t_p , represents a delay associated with the various internal circuitry of the comparator to effectuate the corresponding signal transition at the output in response to the transition at the comparator input.

IV. OVERVIEW OF THE '405 PATENT

A. Brief Description

63) The '405 patent is directed to a power supply for use in a solar electric production system. Ex.1001, 1:50-51, Figure 4 (my Fig. 7). In Fig. 7 below, a power supply is shown having a first stage 401 and a second stage 402, where the first stage 401 receives an input voltage from a photovoltaic ("PV") panel and outputs a first voltage at a first output. The second stage 402 is connected to the first stage 401 and in one example comprises a second power converter. Ex.1001,1:51-56. The second stage 402 operates in two states: (1) a first, deactivated state, and (2) a second, enabled state. In the second state the second stage 402 generates a second voltage at a second output using the first voltage to supply a micro-controller with a voltage. Ex.1001,8:41-48.

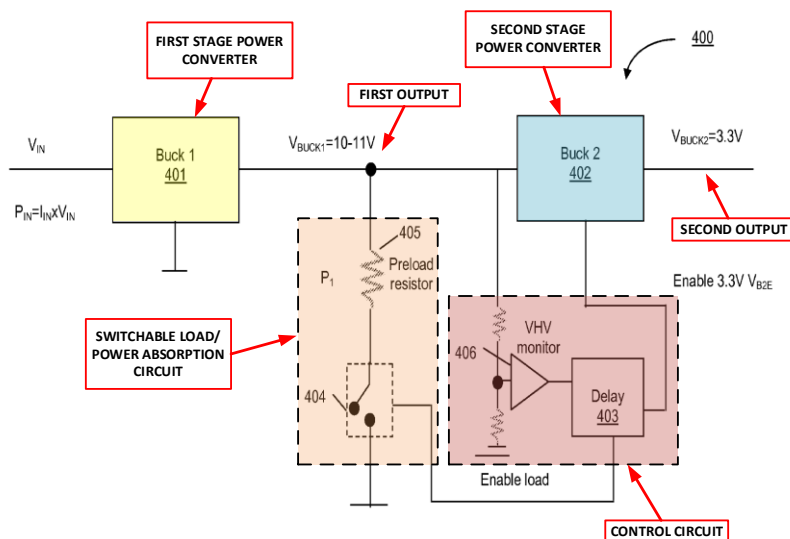


Figure 4

Fig. 7

- 64) The power supply includes a control circuit (406, 403) to prevent false start problems when the solar panel is providing insufficient power. Ex.1001,8:19-22. The control circuit, in the first state, connects a preload resistor 405 to the first output by closing a switch 404 via a first control signal to emulate the load of the second stage 402 on the first stage output prior to activating the second stage 402 via a second control signal. Ex.1001, 8:22-23,8:35-37. If the first stage output voltage exceeds a threshold, the control circuit, in the second state, disconnects the preload resistor 405 by opening the switch 404 via the first control signal. Ex.1001, 8:41-45. The control circuit employs a delay 403 to delay the second control signal with respect to the first control signal to ensure the second stage operation remains disabled until after the switch 404 is opened, thus providing a “break before make condition,” wherein the switch 404 opens before the second stage 402 is enabled. Ex.1001, 8:40-48.
- 65) In another embodiment shown in Fig. 8 (Figure 3 of Ex.1001), a capacitor 326 is connected to the input of the second stage 311/402. Ex.1001, 9:32-34.

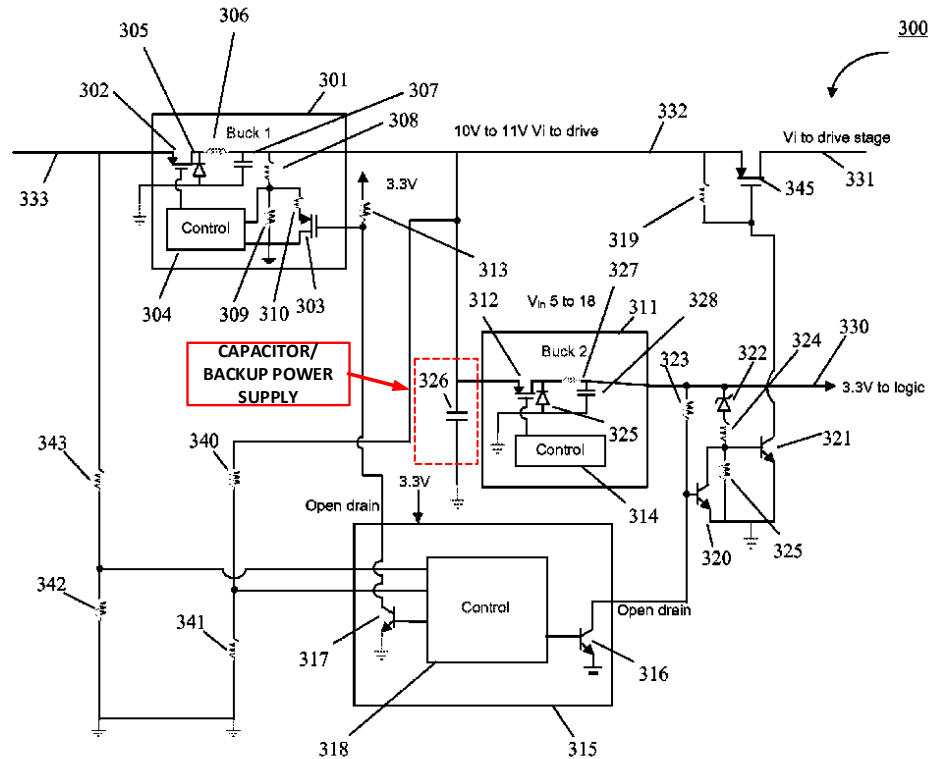


Fig. 8

66) Capacitor 326 is employed as a backup power supply to keep the second stage 311/402 running longer than the first stage 401. Thus, in the first state, the capacitor 326 is charged and absorbs power, and when the first stage 401 is inoperative/unstable, the capacitor provides charge to keep the second stage 402 working to provide the second voltage at the second output. Ex.1001, 4:60-66.

B. Earliest Priority Date for the Claims

67) The '405 patent was filed as App. No. 15/969,607 ('607 application) on May 2, 2018, as a continuation of App. No. 15/392,960 (issued as Patent No. 8,966,848), filed on December 28, 2016, as a continuation of App. No. 14/822,227 (issued as Patent No. 9,584,021), filed on August 10, 2015, as a continuation of App. No.

12/787,205 (issued as Patent No. 9,143,036), filed on May 25, 2010, claiming priority to U.S. App. No. 61/275,734, filed on September 2, 2009, and U.S. App. No. 61/336,743, filed on January 26, 2010. Ex.1001, P.1;Ex.1006,88-90,101-108). At least 61/275,734, and arguably 61/336,743, does not provide support under 35 U.S.C. §112, first paragraph, for the claimed subject matter. While I do not rely on prior art published in the time period between the priority dates and the non-provisional filing date of May 25, 2010 of the great-grandparent application, I reserve the right to challenge the priority date of the claimed subject matter of the '405 Patent.

- 68) A first substantive Office Action was issued in the '607 application on October 18, 2018. In the non-final Office Action, claims 1-3 and 10-12 were rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent Publication No. 2007/0001653 (Xu) in view of U.S. Patent No. 5,565,761 (Hwang). Claim 4 was rejected under 35 U.S.C. § 103(a) as being obvious over Xu in view of Hwang and U.S. Patent Publication No. 2007/0278861 (Lou), and claims 19-20 were rejected under 35 U.S.C. § 103(a) as being obvious over Xu in view of Hwang and U.S. Patent Publication No. 2008/0179949 (Besser). Claims 5-9 and 13-18 were held to contain allowable subject matter, but were objected to for depending upon a rejected independent claim. (Ex.1006, 70-79).

- 69) A response to the non-final Office Action was filed by the applicant on January 3, 2019. In the response, allowable claims 5 and 13 were amended into independent form, claims 1, 3-4, 10-11 and 19-20 were cancelled, and the other rejected depending claims were amended to depend upon amended independent claims 5 and 13, respectively. (Ex.1006, 43-48). The allowable subject matter of claim 5 deemed to distinguish over the cited art of record was: “wherein the control circuit is configured to signal the switchable load to be in a first state of consuming the first output during the time period and to be in a second state of not consuming the first output after the time period.” The allowable subject matter of claim 13 deemed to distinguish the claim over the cited art of record was: “consuming, by a switchable load in a power absorption circuit, a portion of the first output from the first stage power converter during the time period.” (Ex.1006).
- 70) A Notice of Allowance was issued on February 19, 2019, wherein pending claims 2, 5-9 and 12-18 were deemed allowed. (Ex. 1006,10-18). The ‘405 patent issued on June 25, 2019, wherein independent claims 5 and 13 were renumbered as independent claims 1 and 7, respectively. (Ex.1006,2).
- 71) The earliest alleged priority date for the ’405 patent claims is the filing date of the U.S. provisional application—the earlier one filed September 2, 2009. Each reference discussed herein in the grounds for unpatentability predates this date and constitutes available prior art under 35 U.S.C. § 311(b)

V. OVERVIEW OF PRIOR ART

A. DE3725476 (Mieth) (Ex.1002)

- 72) Mieth discloses a circuit and associated method that supplies power to an electrical load such as a micro-controller from a solar generator. See Fig. 9 below. Ex.1002, 8:8-9, Fig. 1.
- 73) For electrical energy sources that exhibit variability in performance, such as a solar converter (due to the time of day or weather conditions), depending on the power provided by the energy source, the circuit arrangement operates in two different states. Ex.1002, 1:23-28; 5:22-27. In a first state, at lower source voltages, a preliminary load is switched “in” to the circuit, while a downstream auxiliary power supply circuit is disabled. In a second state, at higher source voltages, the preliminary load is switched “out” of the circuit arrangement, and the power from the solar generator is fed to the auxiliary power supply circuit (*e.g.*, power supply apparatus 19). *Id.* 1:28-34; claim 1, 2:10-34.
- 74) As given below, Fig. 9 shows the solar generator 1 that provides a direct current to a first stage capacitor 2 that provides a first voltage at a first output in response to a direct current input.

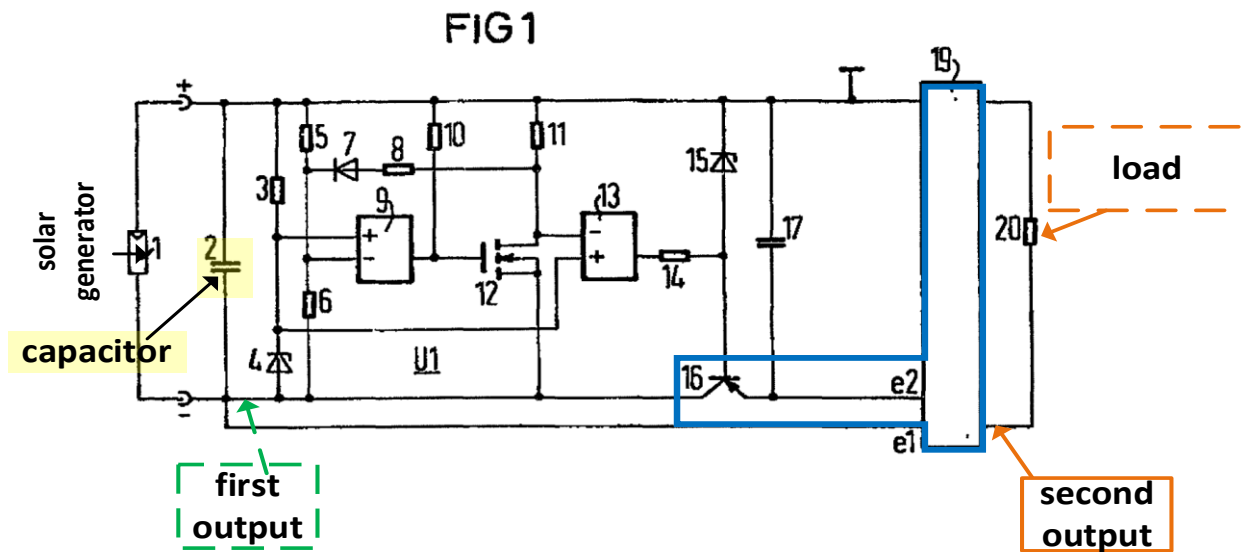


Fig. 9

- 75) The circuit arrangement includes two comparators, a first comparator 9, and a second comparator 13, that operate in one of two states. In the first state, with a low voltage at the first output, the first comparator 9 switches “in” the preliminary load, while the state of the second comparator 13 results in the power supply apparatus 19 being disabled. Id. 6:14-23; 9: 15-32.
- 76) Fig. 10 highlights the first state at low input voltages, where first comparator 9 is “high” and preliminary switchable load 11 (i.e., resistor 11), is switched “in” due to transistor 12 being “on” (i.e., conducting).

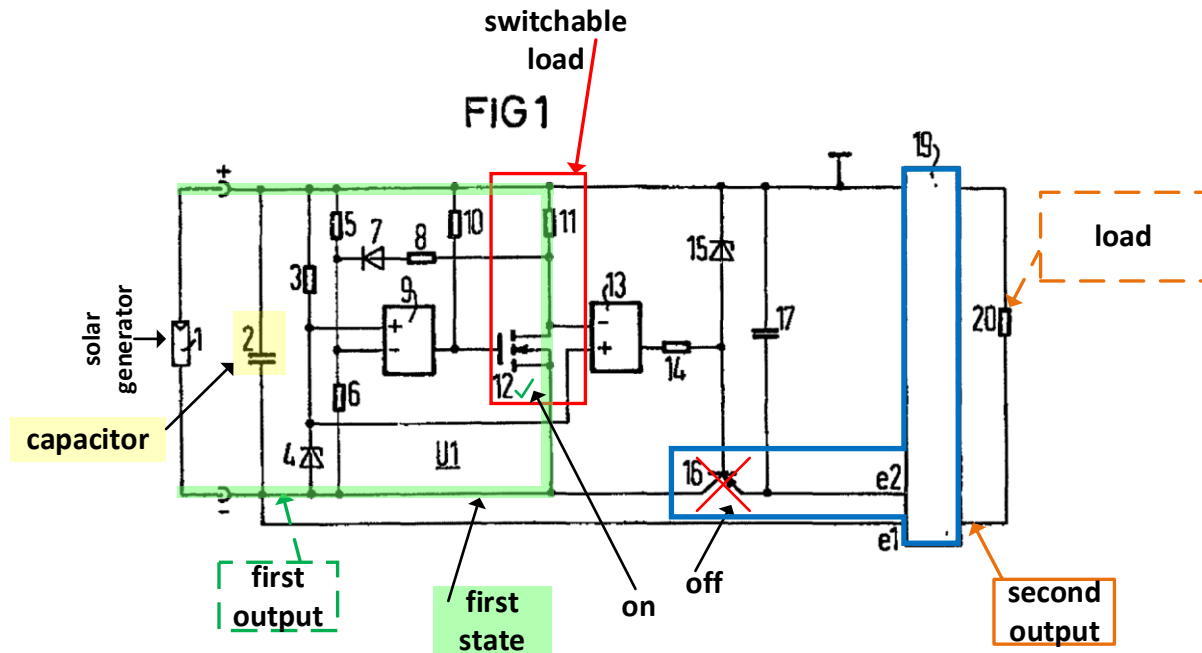


Fig. 10

- 77) Further, in the first state, second comparator 13 output is “high”, causing the pnp bipolar transistor 16 to be “off” (i.e., non-conducting), and power supply apparatus 19 to be disabled. *Id.* 12:12-19.
- 78) Fig. 11 illustrates the second state when power provided by solar generator 1 is high (the magnitude of the voltage across capacitor 2 is high), thus the magnitude of the first voltage at the first output is high. With higher magnitude input voltages, the voltage at the negative input of first comparator 9 exceeds the reference voltage at the positive input terminal, causing the first comparator output to transition “low” and turning off transistor 12 (i.e., “switching out” switchable load, resistor 11).

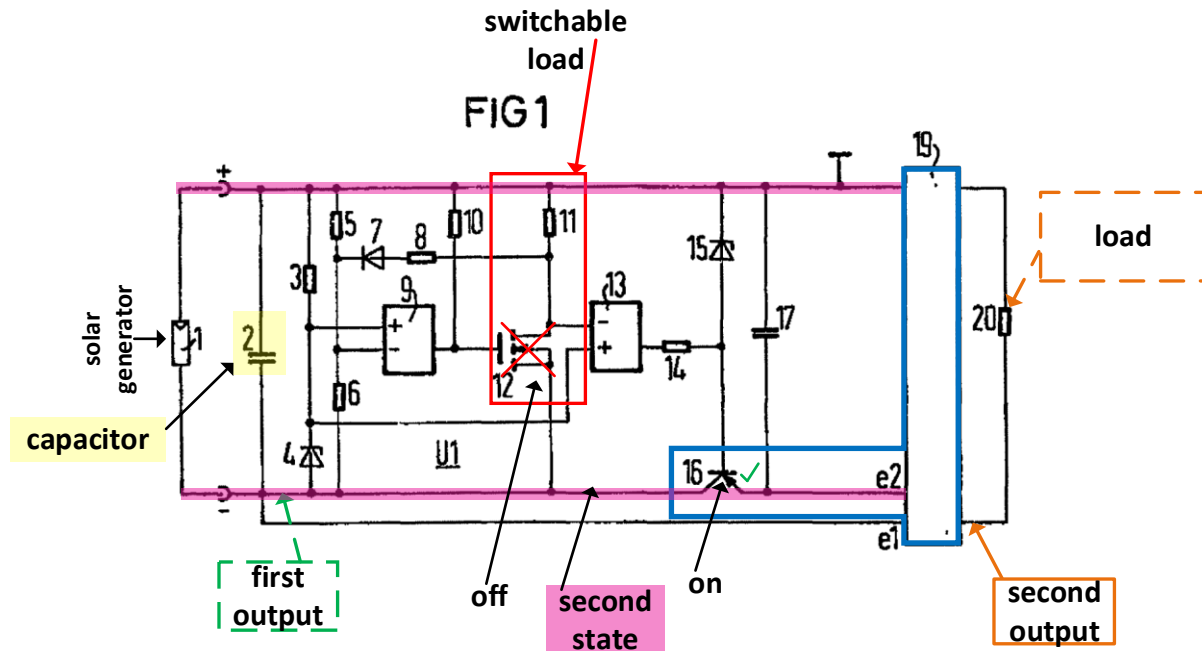


Fig. 11

79) With transistor 12 off, the negative input of second comparator 13 gets pulled high, causing second comparator 13 output to go “low,” turning on transistor 16 (pnp bipolar transistor). *Id.* 12:21-30. With transistor 16 conducting, the first output is passed to the e2 input of auxiliary power converter 19, enabling such circuitry, which provides the second output to load 20. *Id.* 9:15-32. Auxiliary power converter 19 is also connected to solar generator 1 via supply voltage input e1. *Ex.1002* 8:29-35. Mieth does not discuss the function of supply voltage input e1, a PHOSITA would understand that supply voltage input e1 may provide additional functionality to the circuit of Mieth, perhaps, for a product or particular implementation that is extraneous to the detailed description.

80) In addition, Mieth discloses a “break before make” operation between the first and second states, wherein an exit from the first state (preliminary load 11 is “switched in”) is concluded before the second state (where auxiliary power converter 19 is enabled) is initiated. This “break before make” operability is facilitated by the cascaded first and second comparators 9 and 13. When the first voltage at the first output goes low (relative to the positive terminal of the PV), first comparator 9 output changes state to turn off the transistor 12. Only after transistor 12 stops conducting does second comparator 13 output transition from “high” to “low” in order to activate the transistor 16. Thus when transistor 12 shuts off, the voltage at the negative input terminal of second comparator 13 rises and exceeds the reference voltage at the positive input terminal, causing output of the second comparator 13 to transition low. Transistor 16 is a pnp-type transistor, and is activated or turned “on” when the voltage at its base terminal that connects to the output of the second comparator 13 is low. Because comparator 9 must change state before the output of transistor 12 (the negative input of comparator 13) changes state and comparator 13 changes state only after the negative input changes state, there is an intrinsic delay built into the cascaded comparator arrangement to ensure that the first control signal that disables preliminary load 11 always occurs before the second control signal that enables power supply apparatus 19. Thus, Mieth teaches a delay between first and second control signals.

81) Mieth includes a hysteresis circuit comprising comparator 9, voltage divider resistors 5, 6, 8, 11, and diode 7. *Id.* 12:21-30. The hysteresis function is provided by the positive feedback via resistor 8 and diode 7. *Id.* Using the nomenclature shown in the Fig. 12 below, Mieth's hysteresis will be analyzed.

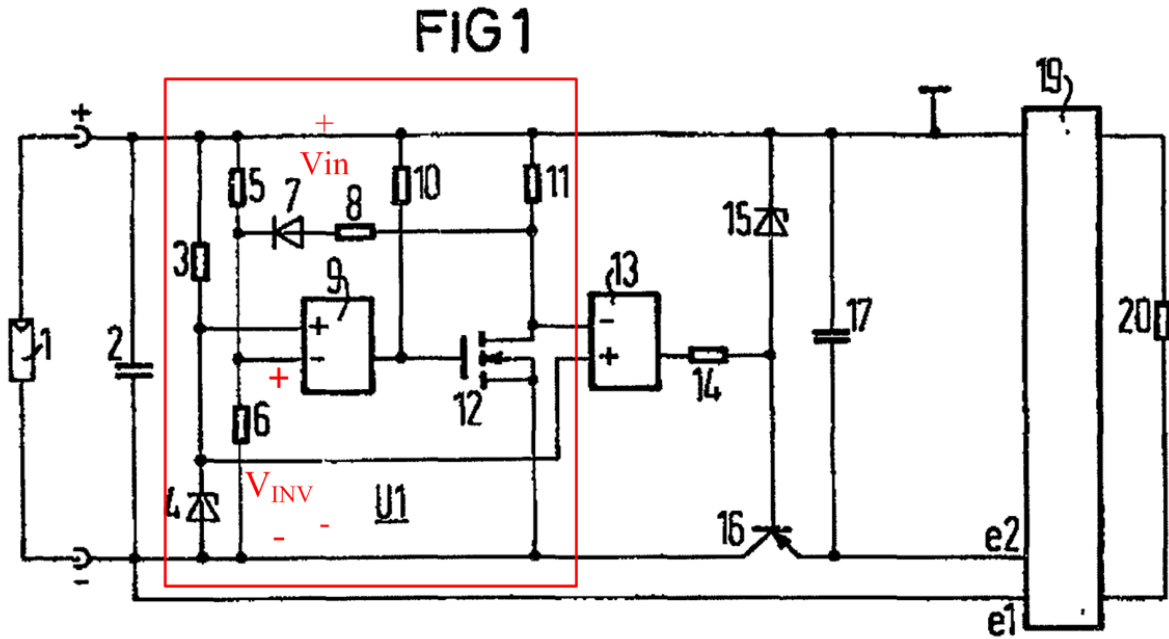


Fig. 12

82) Mieth incorporates a diode 7 in the hysteresis circuit so that the hysteresis feedback is applied in only one state (when the output of comparator 9 is low causing drain of transistor 12 to be high). Thus, in the first state where

$$V_{in} \frac{R6}{R5 + R6} < V_{ZENER}, \text{ the drain of transistor 12 is low, so diode 7 does not conduct.}$$

When V_{in} increases so that when $V_{in} \frac{R6}{R5 + R6} > V_{ZENER}$, the output of the comparator

goes low and the drain of transistor 12 goes high so that diode 7 is conducting and as a result changes the voltage at the inverting input of comparator 9 to:

$$\frac{V_{in}\left(\frac{R6}{R5} + \frac{R6}{R8 + R11}\right) - V_{DIODE} \frac{R6}{R8 + R11}}{1 + \frac{R6}{R5} + \frac{R6}{R8 + R11}} = V_{INV}$$

83) Ignoring the forward voltage of the diode (setting $V_{DIODE} = 0$) this expression simplifies to:

$$V_{in} \frac{R6}{R_{EQ} + R6} = V_{INV}$$

where:

$$R_{EQ} = \frac{R5(R8 + R11)}{R5 + R8 + R11}$$

84) Thus there are two thresholds. The upper threshold is given by:

$$V_{in} = \frac{R5 + R6}{R6} V_{ZENER}$$

85) and the lower threshold given by:

$$V_{in} = \frac{R_{EQ} + R6}{R6} V_{ZENER}$$

86) The hysteresis curve resulting from this circuit arrangement is shown in Fig. 13 below.

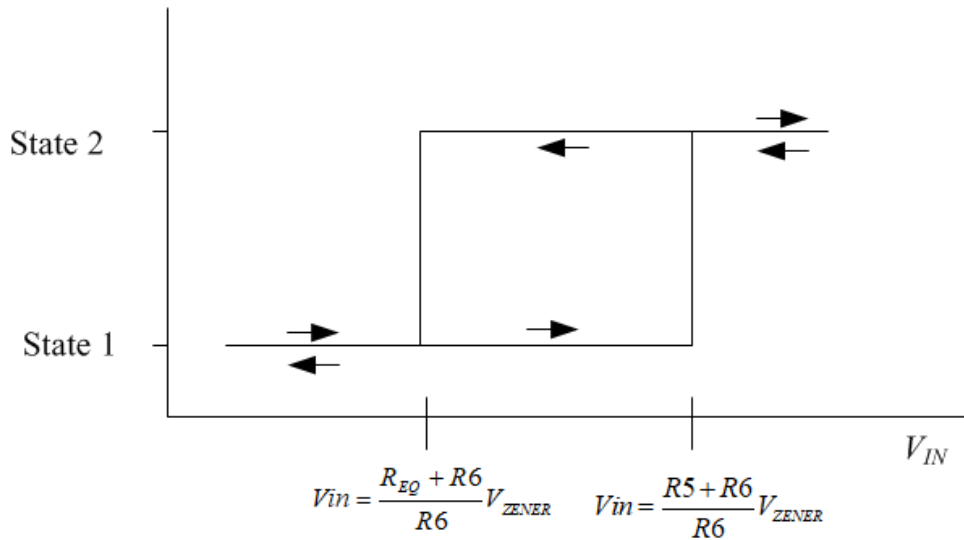


Fig. 13

B. U.S. Patent No. 6,246,592 (Balogh) (Ex.1003)

87) Balogh is a United States patent that issued on June 12, 2001. Balogh discloses that cascaded power converter arrangements that include two or more power converters are well known. Ex.1003, 1:21-22. Balogh further discloses that cascaded converters are commonly used to provide large input to output voltage conversion ratios (step-up or step-down). *Id.* 1:25-28. Solar power applications often employ individual modules with voltages as high as 75-80V under some operation conditions, and as low as 10V in other instances, while still providing enough power to operate a load such as a microcontroller. Ex. 1010; Ex. 1011. Consequently, solar power applications including cascaded power converter systems having large input to output voltage conversion ratios can be advantageous.

- 88) It is well known in the art that improved efficiency can be achieved by cascading buck converters when there is a large ratio of input to output voltage as described in Patent application: US 2007/0001653 (hereafter “Xu”). Ex. 1012. Xu states: “The present invention provides a two-stage power delivery system that employs cascaded buck stages. For high input-to-output voltage ratios, each cascaded buck stage has a more suitable (i.e., larger) duty cycle that results in a much lower total power loss than in a single-stage buck.” Ex. 1012, ¶6. Xu teaches using cascaded buck converters where the input is in the range from 6 to 24 volts and an output voltage on the order of 1 volt. *Id.* ¶18. Thus, as will be discussed in greater detail *infra*, Xu provides a teaching that a PHOSITA would readily consider a cascaded converter arrangement in various solar applications, such as the application taught in Mieth.
- 89) Balogh discloses multiple cascaded buck converter arrangements in prior art Figs.1B-1D, respectively. One example of a conventional, cascaded converter arrangement provided in Fig. 1D thereof is illustrated in Fig. 14 below.

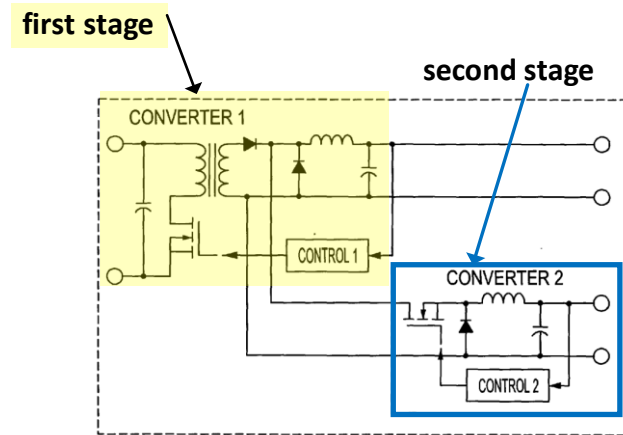


FIG. 1D
PRIOR ART

Fig. 14

- 90) In Fig. 14, an isolated DC-DC converter (converter 1) feeds a post regulator circuit (converter 2) to form first and second step-down (buck) converter stages, respectively. In one example, the first converter is a transformer-coupled input power converter that steps down the input voltage to an intermediate voltage. Ex.1003, 1:61-66; 3:8-13. The second converter is a buck power converter. *Id.*, 1:62-63.

C. U.S. Patent No. 6,798,177 (Liu) (Ex.1005)

- 91) Liu is a United States patent that published on September 28, 2004. Liu discloses a multi-stage converter circuit that employs a storage capacitor in between, and in parallel with, two cascaded converter stages. As shown in Fig. 15 below (which corresponds to Fig. 5 of Liu), the multi-stage converter circuit includes an input stage 50, a storage or reservoir capacitor 58, and output stage 60. Output stage 60 connects to a power amplifier (“PA”) 68 as a load. Ex.1005, Fig.5, 4:25-28.

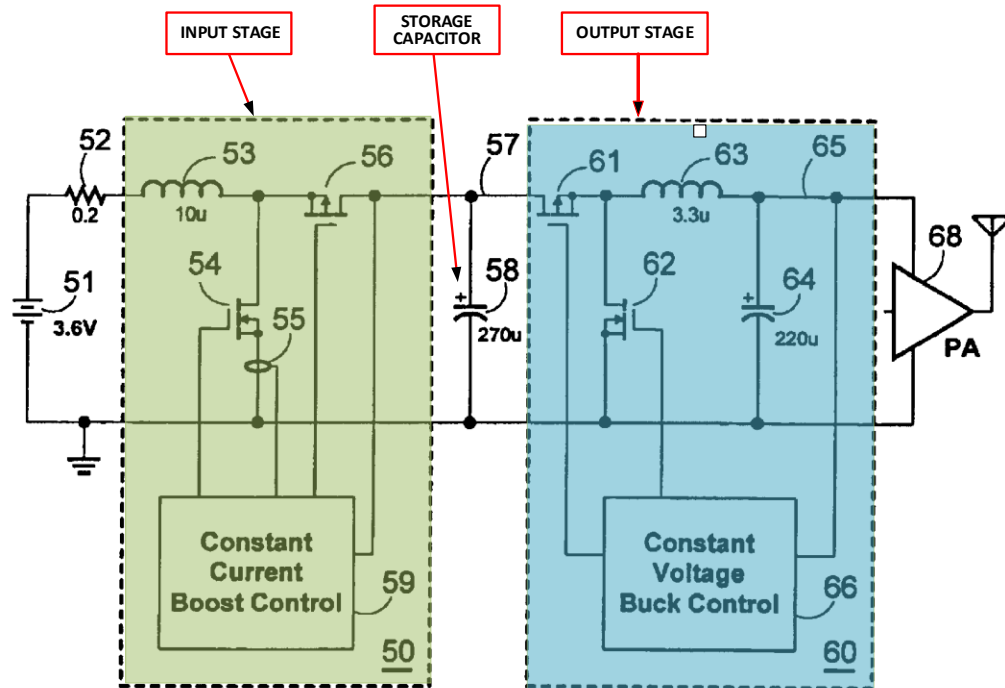


FIG. 5

Fig. 15

92) The input stage 50 operates to charge the storage capacitor 58 and thus increase the voltage across the capacitor. The output stage 60 operates to down-convert the voltage on the reservoir capacitor 58 to an output voltage, for example, 3.4V, needed by the PA 68, which the output stage 60 regulates. *Id.*, 4:36-50. During operation the storage or reservoir capacitor 58 supplies energy to the PA 68, such that if the input stage 50 ceases operating, the output stage continues powering the PA 68 for some further period of time. *Id.*

VI. SUMMARY OF ARGUMENT

- 93) The '405 patent claims an apparatus and method for supplying power. The prior art herein is replete with auxiliary power supply circuitry that teaches the features of the apparatus and the steps of the method. Mieth teaches all the elements of the '405 patent's independent claims and most dependent claims. For independent and dependent claim elements arguably not taught by Mieth, Balogh teaches first stage power converter features and cascaded first and second stage power converters such as step-down power converters, and Liu discloses a capacitor as an auxiliary power supply between cascaded power converters. Adding these features to Mieth's auxiliary power supply system would have been obvious, and yields the alleged invention claimed in the '405 patent.
- 94) In sum, as demonstrated by a preponderance of the evidence, including this prior art, the '405 patent claims are unpatentable as being anticipated and/or obvious in view of the cited prior art.

VII. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Ground A: Anticipation of claims 1-2, 4-9 and 11-13 over Mieth

1. Independent Claim 1

95) With reference to the claim listing appendix, Mieth discloses elements [1A] – [1H].

i. [1A]: “An apparatus, comprising:”

96) Mieth (Ex.1002) discloses a circuit that supplies power to an electrical load from a solar generator. Ex.1002 (Mieth), 8:8-9. A PHOSITA understands that a “circuit” is a species of the genus term “apparatus.” Thus, Mieth teaches [1A].

ii. [1B]: “a micro-controller;”

97) Mieth discloses a circuit as shown below in Fig. 16. Mieth discloses a capacitor 2 (yellow) in parallel with the solar generator 1, and a power supply apparatus 19 connected to a bipolar transistor 16 (blue). Ex.1002, 9:5-9, 11:14-16. The capacitor 2 receives direct current from the solar generator 1, and provides a first output.

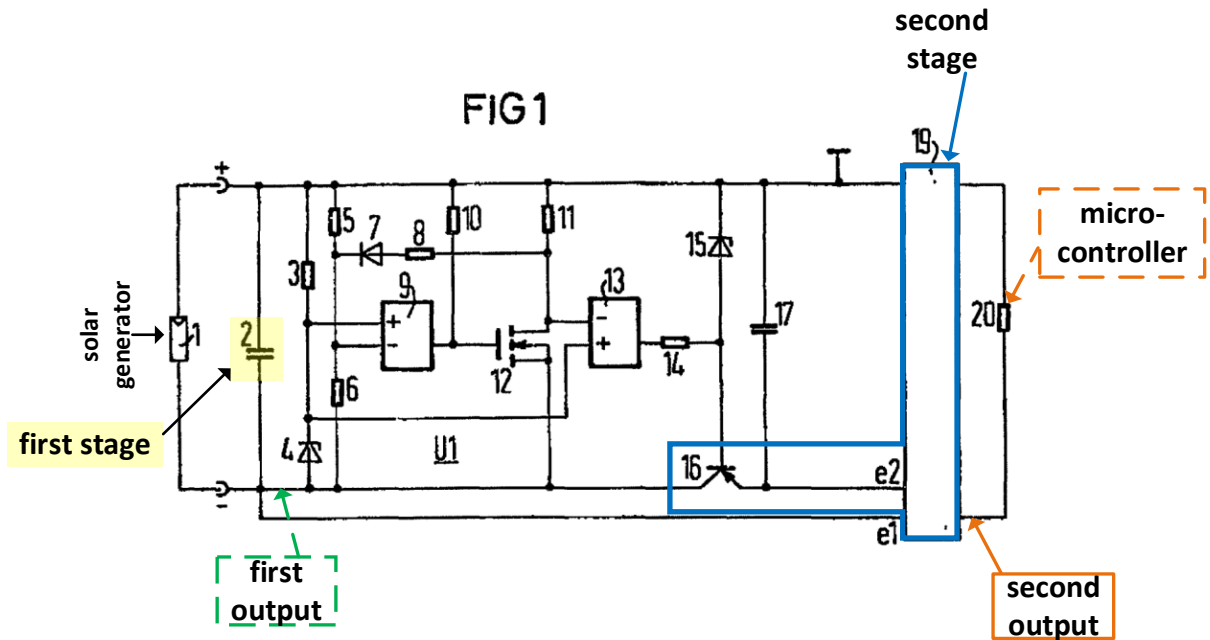


Fig. 16

98) The power supply apparatus 19 of Mieth is a DC-DC voltage converter or a charging converter and outputs a voltage and current to power a load 20 as shown in Fig. 16 (Fig.1, annotated-1B). A PHOSITA understands that the load 20 is a generic term, and can be or include a micro-controller. Ex.1014, 1180, Fig.5. As such, the load 20 is analogous to the claimed *micro-controller* (dashed-orange).

99) Thus, Mieth teaches [1B].

iii. [1C]: “a first stage power converter to generate a first output from a direct current input;”

100) There is no explicit definition of “power converter” in the ‘405 patent specification, thus a PHOSITA, would construe “a first stage power converter” to be one or more circuit elements that perform the recited function set forth in this

claim. As such, the solar generator 1 of Mieth supplies a ***direct current input*** (dashed-red) to the capacitor 2. The supplied current charges the capacitor resulting in a voltage across its terminals. As specified in the claim, the first stage power converter merely generates a first output from a direct current input. The capacitor 2 performs that recited function and thus constitutes “a first stage power converter” as shown in Fig. 17 below. The “first stage power converter” of Mieth is a parallel capacitor 2 which converts the direct current input into a ***first output*** (dashed-green) as shown.

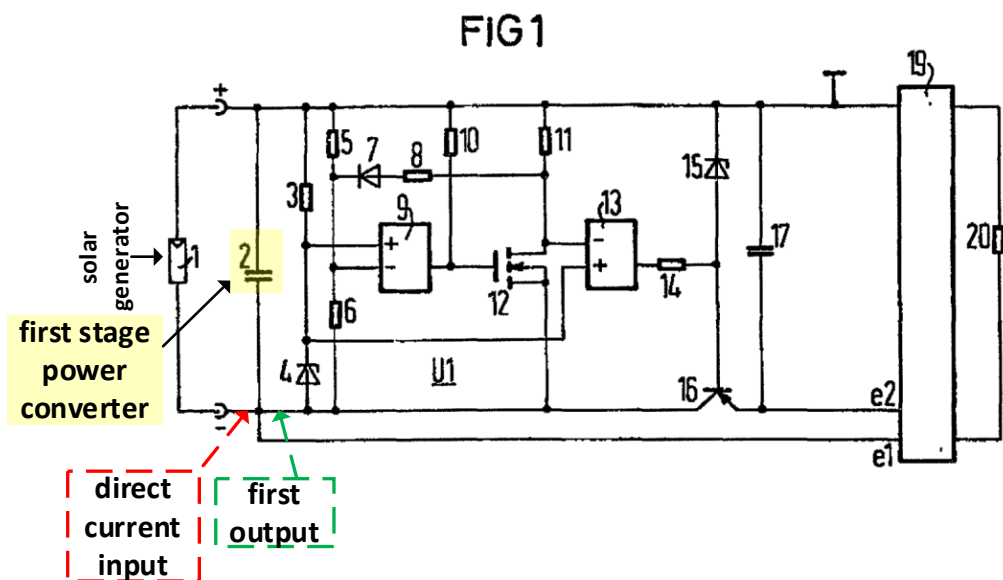


Fig. 17

101) Thus, Mieth discloses [1C].

iv. [1D]: “a switchable load powered by the first output;”

102) Mieth discloses that the first output (**dashed-green**) of capacitor 2 is connected to field-effect transistor 12 in series with resistor 11 (a preliminary load) as shown in Fig. 18 below. Ex.1002, 10:5-14.

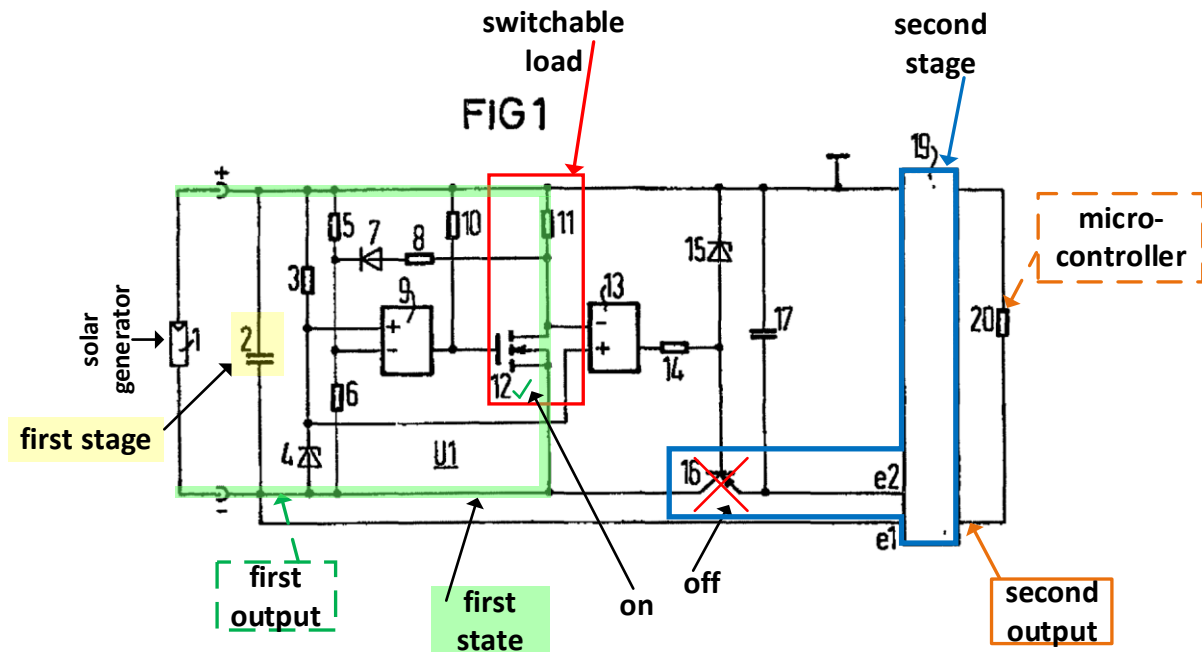


Fig. 18

103) The field-effect transistor 12, which operates as a switch, and the preliminary load 11 in combination are analogous to the claimed **switchable load** (red). Mieth discloses that when voltages at the first output are below a predefined minimum value (in magnitude) for reliable operation of the power supply apparatus 19, the field-effect transistor 12 is “on”, and operates as a closed switch where the preliminary, switchable load 11 is connected to the solar generator 1 by the first

output. Ex.1002, 9:15-23. As shown in Fig. 18, a first state (highlighted-green) illustrates that the switchable load is powered by the first output from the capacitor 2 (i.e., field-effect transistor 12 is “on” or in a conducting state). As such, Mieth is analogous to *a switchable load powered by the first output*.

104) Thus, Mieth teaches [1D].

v. [1E]: “a control circuit powered by the first output; and”

105) Mieth discloses a first comparator 9 that turns the transistor 12 “on” or “off” as shown in Fig. 19 below. Ex.1002, 9:34-10-14.

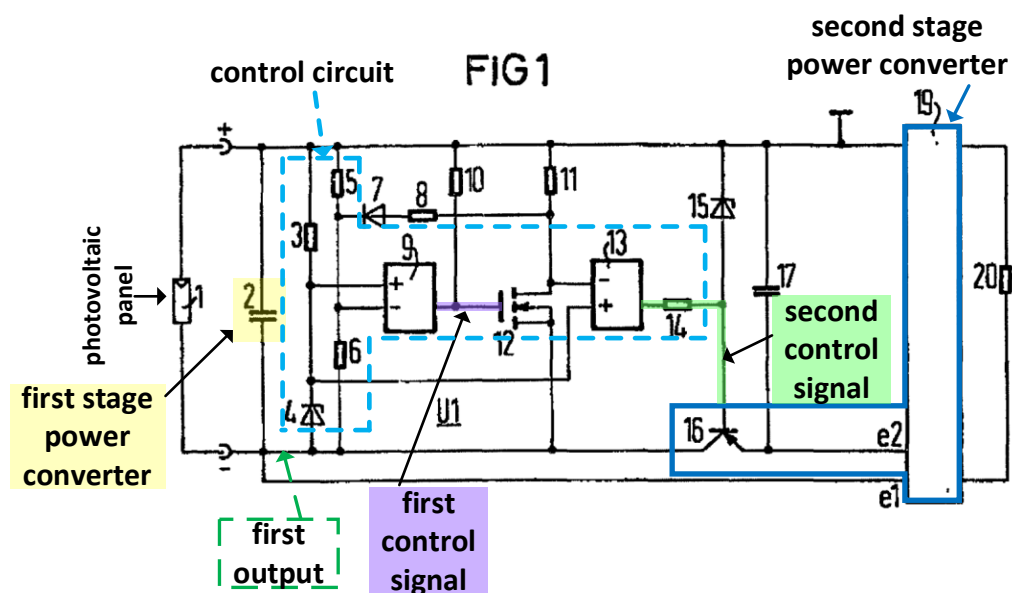


Fig. 19

106) First comparator 9 compares a reference voltage from a reference voltage generator to a voltage from a voltage divider. Ex.1002, 9:34-0:3. The reference voltage generator is defined by the Zener diode 4. Id. The voltage divider is defined by the voltage divider resistors 5 and 6 and the monitored voltage is

representative of the first output (dashed-green) of capacitor 2 (first stage power converter-yellow). Id. First comparator 9 compares the voltage from a voltage divider to the reference voltage from the reference voltage generator to determine if the monitored voltage exceeds a voltage threshold (in magnitude) (See ¶84)), and outputs a first control signal (highlighted-purple) to transistor 12 based on the comparison. Ex.1002, 12:12-26.

107) A PHOSITA understands that the circuitry (dashed-blue) that controls transistor 12, which includes first comparator 9, voltage divider 5, 6 and reference voltage generator 3,4 constitutes a control circuit. Further, such circuitry are powered by the first output from the capacitor 2, and therefore the circuitry is analogous to the claimed ***a control circuit powered by the first output***. Ex.1002,9:34-10:3.

108) Thus, Mieth teaches [1E].

vi. [1F]: “a second stage power converter connected to the first stage power converter and configured to convert the first output to a second output;”

109) In Mieth, a power supply apparatus 19 connected to a bipolar transistor 16 (second stage-blue) together constitutes ***a second stage power converter connected*** (green) coupled to capacitor 2 that forms the first output (dashed-green), as illustrated below in Fig. 20. As stated above in ¶100), the capacitor 2 is a first stage power converter according to the claim language. The first stage power converter is connected (green) to the second stage power converter (blue), as shown in Fig. 20.

110) Still referring to the figure below, the power supply apparatus 19 **is powered** by way of auxiliary voltage input e2 which is coupled to the first output when the bipolar transistor 16 is conducting. Ex.1002, 8:29-35. According to Mieth, the power supply apparatus 19 is a DC-DC voltage converter or a charging converter and outputs a voltage and current to power a load 20. Id. Thus the power supply apparatus 19 is a power converter, and as a power converter, power supply apparatus 19 receives the first output and **converts the first output to a second output** (orange) as shown below in Fig. 20. As shown, the second output is provided by the second stage power converter 16/19 to the load 20, and a PHOSITA understands that a load in a circuit can be or include a micro-controller (dashed-orange). Ex.1014, 1180, Fig.5.

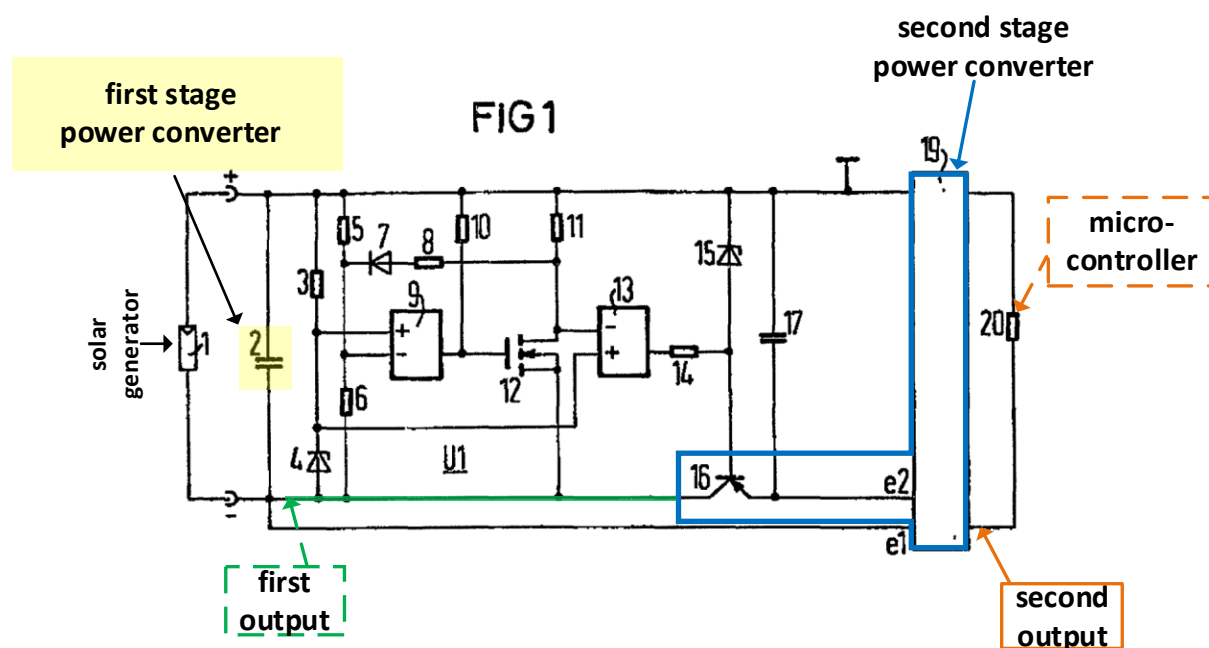


Fig. 20

111) Therefore the combination of bipolar transistor 16 and power supply apparatus 19 is analogous to a second stage power converter connected to the first stage power converter and configured to convert the first output to a second output.

112) Thus, Mieth teaches [1F].

- vii. [1G]: “wherein the control circuit is configured to block the second stage power converter from powering the micro-controller using the second output in a time period that is after the control circuit is powered by the first output and before a predefined condition is met in the control circuit; and”

113) According to element [1G], the control circuit functions to block the second stage power converter from powering the micro-controller using the second output in a time period. Further, element [1G] requires the time period in which such control occurs to be bounded by two constraints: (1) after the control circuit is powered by the first output, and (2) before a predefined condition is met in the control circuit. As will be appreciated below, Mieth discloses such a control circuit.

114) As discussed briefly in ¶¶75), 77), 78), the control circuit of Mieth is configured to place the power supply circuitry into two different states: (1) a first state associated with “low” first output voltages, where the switchable load is connected and the second output is not powered, and (2) a second state associated with “high” first output voltages, where the switchable load is disconnected, and power from the first output connects to the second power converter which, in response, powers the micro-controller via the second output. See above, ¶¶ 75 and 77-78.

115) For the first state, bipolar transistor 16 is non-conducting, and the power supply apparatus 19 (i.e., second stage-blue) is disabled, or “blocked” from supplying the load 20 (i.e., micro-controller-dashed-orange) with the second output (orange), see

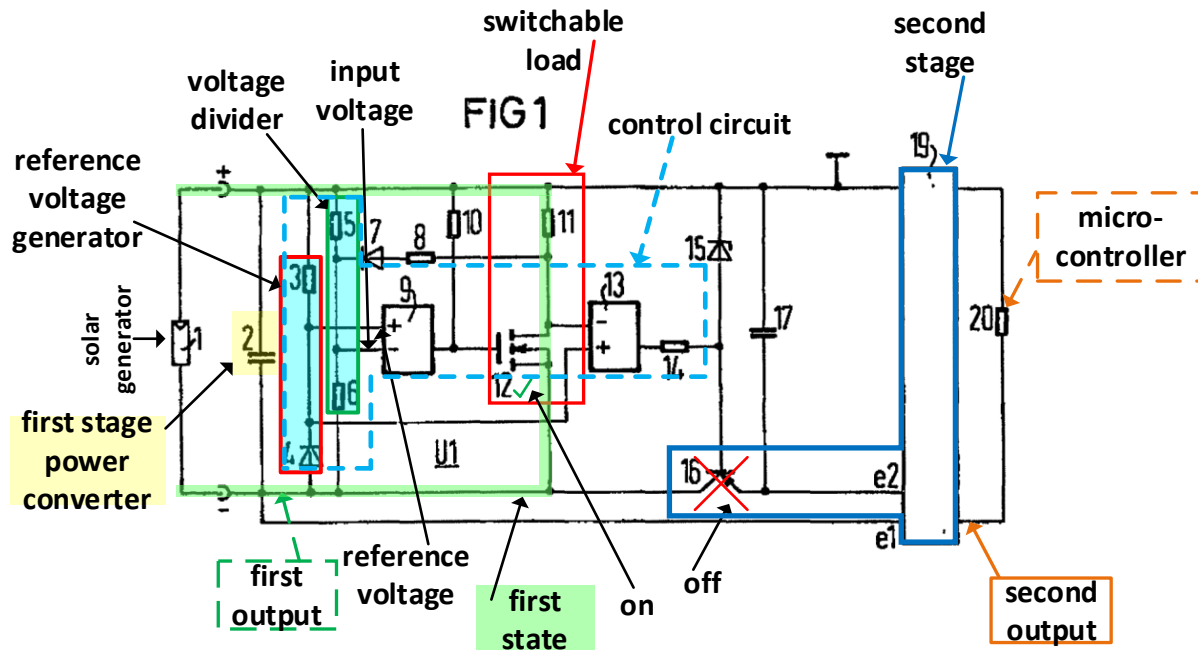


Fig. 21

116) While in the first state, transistor 12 is turned “on” by the first comparator 9 thereby loading the first output with the preliminary load 11 (controlled through the field-effect transistor 12 when conducting, i.e., the first state – analogous to the switchable load-red). Ex.1002, 9:15-32, 10:5-14. In the first state, the first comparator 9 compares a voltage from the reference voltage generator (highlighted-teal-outlined-red) connected to a positive terminal of the first comparator 9 to a voltage from a voltage divider (highlighted-teal-outlined-green)

connected to a negative terminal of the first comparator 9. Ex.1002,9:34-10:3.

The reference voltage generator is defined by the Zener diode 4. *Id.* The voltage divider is defined by resistors 5 and 6 and the monitored voltage is representative of the first output. *Id.* The first comparator 9 compares the monitored voltage to a threshold voltage defined by the voltage divider 5, 6 and the reference voltage to determine if the monitored voltage exceeds the threshold voltage. See ¶84)

Ex.1002, 12:12-26.

117) In the first state, the monitored voltage is less than the threshold voltage in magnitude (i.e., a “low” voltage condition at the first output), and the control circuit of Mieth powers the preliminary load 11 and field-effect transistor 12 by the first output. Ex.1002, 12:12-19. The first state of Mieth concurrently disables the second output of the power supply apparatus 19 to the load 20 (i.e., the micro-controller) by turning the bipolar transistor 16 “off,” which is the same as the claimed ***the control circuit is configured to block the second stage power amplifier from powering the micro-controller using the second output.*** *Id.* More particularly, when transistor 12 is conducting and powering the switchable load 11 in the first state, the negative input node to the second comparator 13 is pulled low, below that of the reference voltage supplied to the positive input node of the second comparator 13, causing the second comparator output to go “high,” which ensures that the pnp bipolar transistor 16 is turned “off,” as shown. With transistor

16 “off,” the second stage power converter 19 is blocked from powering the micro-controller 20.

118) The time period the circuit of Mieth is in the first state is the same as the claimed time period and the predefined minimum value of Mieth (i.e., the threshold created by the zener diode 4) is the same as the claimed ***predefined condition***. Ex.1002, 9:15-26. The circuit of Mieth is in the first state for the time period after the control circuit is being powered by the first output (i.e., the first output is providing power to the first comparator 9 and the second comparator 13, as well as the voltage monitoring circuit 5/6, and the reference voltage generator circuit 3/4). The time period in question is also before the predefined condition is met, because once the first output exceeds the predefined minimum threshold value in magnitude (See ¶84), the output of the first comparator 9 goes low, causing the field-effect transistor 12 to shut “off,” which ends the first state. Thus, the ***control circuit blocks the second stage power converter 19 from powering the micro-controller using the second output in a time period after the control circuit is powered by the first output and before the predefined condition is met.***

119) As such, Mieth teaches [1G].

viii. [1H]: “wherein the control circuit is configured to signal the switchable load to be in a first state of consuming the first output during the time period and to be in a second state of not consuming the first output after the time period.”

120) As discussed above in accordance with paragraphs 109-119 (element [1F] and element [1G]), in the first state associated with relatively low voltages at the first output, the preliminary load 11 and the field-effect transistor 12 (i.e., switchable load-red) are powered by the first output of capacitor 2 (i.e., first stage power converter-highlighted-yellow), *resulting in current conducting through the preliminary/switchable load 11 and thus consuming the first output.* (See Fig. 21). Thus, in the first state, the control circuit is analogous to the first portion of claim feature [1H] *wherein the control circuit is configured to signal the switchable load to be in a first state of consuming the first output during the time period.* (Ex.1001, claim 1).

121) Mieth further discloses that when voltage from the solar generator 1 is above a predefined minimum value (as represented at the input terminals of first comparator 9), the control circuit transitions the circuit to the second state, wherein in the second state the auxiliary voltage input e2 of the power supply apparatus 19 is connected to the first output of the solar generator 1. Ex.1002, 9:23-26. As shown below in Fig. 22, when the predefined minimum value is satisfied, the circuit of Mieth operates in the second state (highlighted-pink) where the bipolar transistor 16 is “on” or conducting, causing the first output (dashed-green) of

capacitor 2 to be connected to e2 thereby powering the power supply apparatus 19.

Ex.1002, 10:16-29.

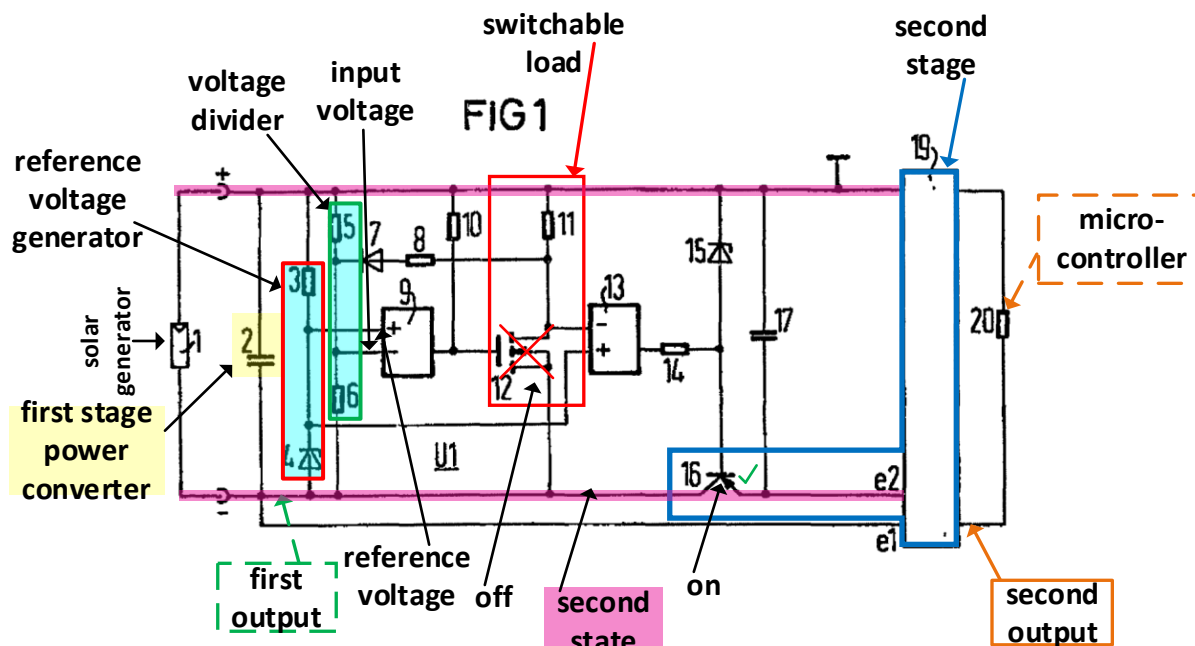


Fig. 22

122) Furthermore, in the second state, the field-effect transistor 12 is “off” or non-conducting, thereby disconnecting the preliminary load 11 from the first output.

Id. As discussed above in paragraphs 113-119, the first comparator 9 compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) to a voltage from a voltage divider (highlighted-teal-outlined-green) to determine if the monitored voltage exceeds the threshold defined by the reference voltage. See ¶84) Ex.1002, 12:12-26. While in the first state, when the first output of capacitor 2 rises in magnitude and the monitored voltage across voltage divider 5, 6 is above the threshold, see ¶84), (i.e., “predefined minimum value” as

quoted by Mieth), the “time period” of the first state ends, and the control circuit disconnects the preliminary load 11 from the first output by configuring the field-effect transistor 12 to an “off” state, which results in the preliminary load 11 (i.e., the switchable load) not consuming the first output in the second state. Thus, the control circuit of Mieth teaches the second portion of claim element [1H] ***and to be in a second state of not consuming the first output after the time period. Id.***

(Ex.1001, claim 1).

123) Thus, Mieth discloses element [1H].

124) As Mieth discloses each and every element [1A]-[1H], Mieth anticipates claim 1.

2. Dependent Claim 2

125) Claim 1 is disclosed by Mieth. See paragraphs 95-124. Claim 2 depends from claim 1 and requires, “wherein the predefined condition includes a voltage of the first output reaching a threshold.” Ex.1001, claim 2.

126) As discussed in detail in paragraphs 113-119, and as shown below in Fig. 23, Mieth discloses that the predefined condition that is monitored to determine an end of the first state, and an initiation of the second state is a threshold dictated by the zener diode 4.

127) For the first state, bipolar transistor 16 is non-conducting, and the power supply apparatus 19 (i.e., second stage-blue) is disabled, or “blocked” from supplying the load 20 (i.e., micro-controller-dashed-orange) with the second output (orange), see

Fig. 23.

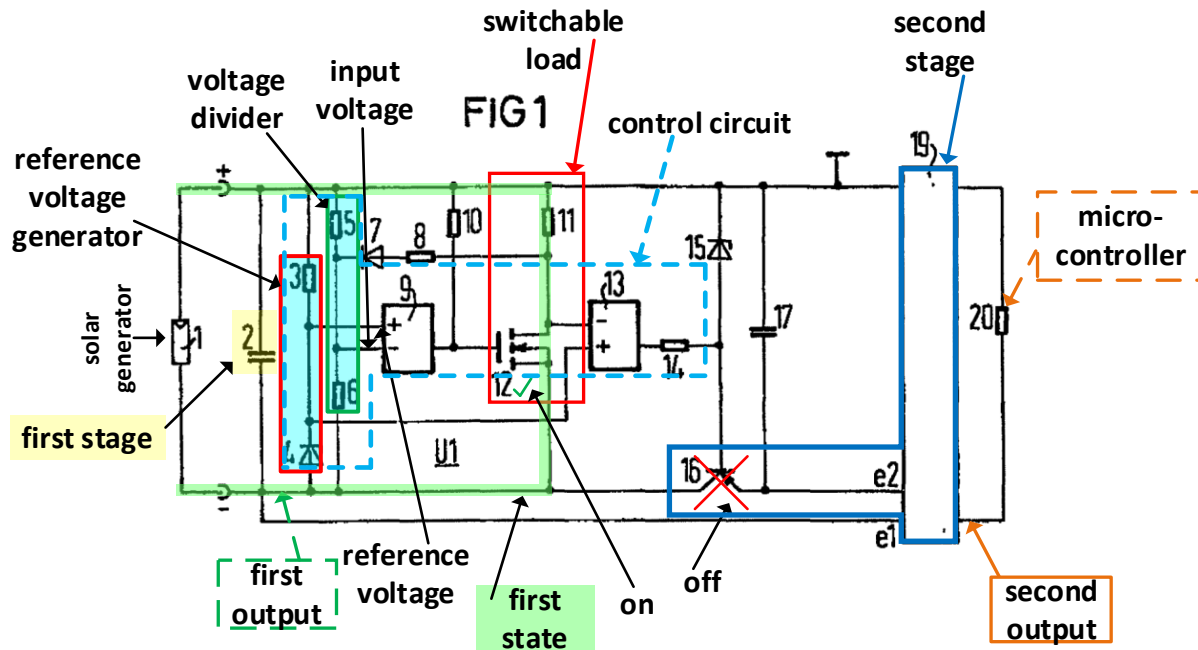


Fig. 23

128) While in the first state, transistor 12 is turned “on” by the first comparator 9 thereby loading the first output with the preliminary load 11 (controlled through the field-effect transistor 12 when conducting, *i.e.*, the first state – analogous to the switchable load-**red**). Ex.1002, 9:15-32, 10:5-14. In the first state, the first comparator 9 compares a reference voltage from a reference voltage generator (**highlighted-teal-outlined-red**) connected to a positive terminal of the first comparator 9 to a voltage from the voltage divider (**highlighted-teal-outlined-green**) connected to a negative terminal of the first comparator 9. Ex.1002, 9:34-10:3. The reference voltage generator that generates the reference is defined by the Zener diode 4. *Id.* The voltage divider is defined by resistors 5 and 6 and the

monitored voltage is representative of the first output. *Id.* The first comparator 9 compares the voltage provided by the voltage divider 5, 6 to the reference voltage threshold to determine if the monitored voltage exceeds ***the threshold*** defined by the reference voltage. See ¶84). Ex.1002, 12:12-26.

129) In the first state, the monitored voltage is less than the threshold voltage (see ¶84) in magnitude (i.e., a “low” voltage condition at the first output), and the circuit of Mieth powers the preliminary load 11 and field-effect transistor 12 by the first output. Ex.1002, 12:12-19. Thus, the control circuit that involves the first comparator 9 operation with the voltage divider 5, 6 and the reference voltage generator 3,4 is analogous to the claim feature ***wherein the predefined condition includes a voltage of the first output reaching a threshold.***

130) Thus, Mieth discloses claim 2.

3. Dependent Claim 4

131) Claim 1 is disclosed by Mieth. See paragraphs 95-124. Claim 4 depends from claim 1 and requires [4A], “wherein the switchable load comprises: a resistive device.” Ex.1001, claim 4. As shown below in Fig. 24 of Mieth, preliminary load 11 (highlighted-orange) can be a resistor. Ex.1002, 12:14-20 (“preliminary load formed by the resistor 11”). Since the preliminary load 11 can be a resistor, and a resistor is a resistive device, preliminary load 11 of Mieth is analogous to element [4A] ***the switchable load comprises: a resistive device.***

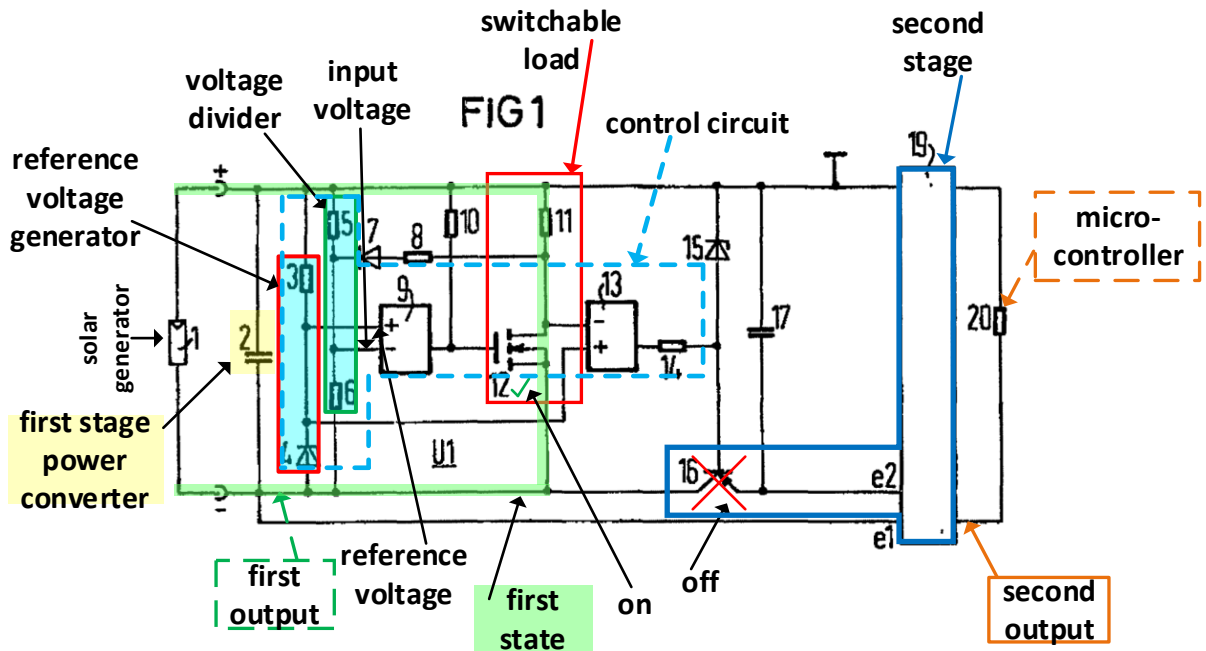


Fig. 24

132) Claim 4 further requires [4B], *inter alia*, “a switching device connected to the resistive device.” Ex.1001, claim 4. As shown in Fig. 24, the field-effect transistor 12 (highlighted-teal) is connected to the preliminary load 11. Mieth describes the field-effect transistor 12 as a first electronic switch, and thus a PHOSITA would understand that the field-effect transistor 12 is a switching device. Ex.1002, 10:5-14. As such, the field-effect transistor 12 connected to resistor 11 is analogous to a first portion of element [4B], the ***switching device connected to the resistive device***.

133) Feature [4B] further recites, “wherein the switching device is turned on in the first state to connect the resistive device to the first output and turned off in the second state to disconnect the resistive device from the first output.” As discussed above

in ¶¶ 72-80 and 113-119, the control circuit of Mieth is configured to operate in two different states: (1) a first state associated with “low” first output voltages, where the switchable load is connected to and consumes the first output, and the second output is not powered, and (2) a second state associated with “high” first output voltages, where the switchable load is disconnected, and power from the first output connects to the second power converter which, in response, powers the micro-controller via the second output.

134) As stated above in ¶¶ 113-119, element[1G], in the first state, for “low” first output voltages, transistor 12 is turned “on” by the first comparator 9, loading the first output with the preliminary load 11 analogous to the switchable load-red).

Ex.1002, 9:15-32, 10:5-14. In the first state, the first comparator 9 compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) connected to a positive terminal of the first comparator 9 to a voltage from a voltage divider (highlighted-teal-outlined-green) connected to a negative terminal of the first comparator 9. Ex.1002, 9:34-10:3.

135) In the first state, the monitored voltage is less than the threshold voltage (see ¶84) in magnitude (i.e., a “low” voltage condition at the first output), and the circuit of Mieth powers the preliminary load 11 and field-effect transistor 12 by the first output. Ex.1002, 12:12-19. Thus, Mieth’s operation of the control circuit with respect to the switchable load is analogous to the claim recitation **wherein the**

switching device is turned on in the first state to connect the resistive device to the first output, which is a further portion of feature [4B].

136) Mieth further discloses that when voltages from the solar generator 1 are above a predefined minimum threshold value (see ¶84) (*i.e.*, relatively “high” first output voltages), the control circuit transitions the circuit to the second state, wherein in the second state the auxiliary voltage input e2 of the power supply apparatus 19 is connected to the first output of the solar generator 1. Ex.1002, 9:23-26. As shown in Fig. 25 below, when the predefined minimum value is exceeded, the circuit of Mieth operates in the second state (highlighted-pink) where the first output (dashed-green) is connected to e2 to power the power supply apparatus 19. Ex.1002, 10:16-29.

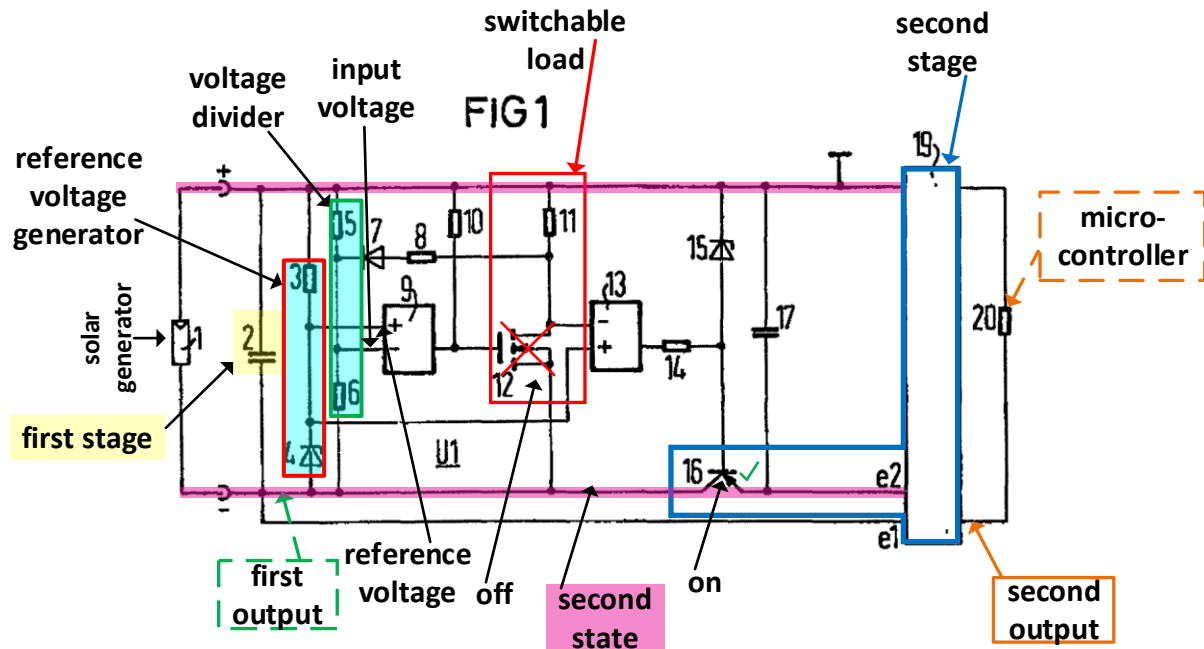


Fig. 25

137) Furthermore, in the second state, the field-effect transistor 12 is “off” or non-conducting, thereby disconnecting the preliminary load 11 from the first output.

Id. As discussed in ¶¶ 120-124, the first comparator 9 compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) to a voltage from a voltage divider (highlighted-teal-outlined-green) to determine if the monitored voltage exceeds a threshold defined by the reference voltage (see ¶84).

Ex.1002,12:12-26, While in the first state, when the first output rises in magnitude and the monitored voltage exceeds the threshold, see ¶84), (i.e., “predefined minimum value” as quoted by Mieth), the “time period” of the first state ends, and the control circuit disconnects the preliminary load 11 from the first output by

configuring the field-effect transistor 12 to an “off” state, which results in the preliminary load 11 (i.e., the switchable load) not consuming the first output in the second state. Thus, the control circuit of Mieth teaches the remaining claim feature of element [4B] *wherein the switching device is... turned off in the second state to disconnect the resistive device from the first output. Id.*

138) Thus, Mieth discloses every feature of claim 4.

4. Dependent Claim 5

139) Claim 1 is disclosed by Mieth. See ¶¶ 95-124. Claim 5 depends from claim 1 and requires “wherein the control circuit delays a first signal instructing the switching device to change from the first state to the second state to generate a second delayed signal that instructs the second stage power converter to change from not powering the micro-controller to powering the micro-controller.”

140) In the first state, the output of the first comparator 9 (e.g., the claimed first signal, **highlighted-purple**) which controls the field-effect transistor 12 (switching device, **highlighted-teal**) is “high,” turning transistor 12 “on.” Ex.1002, 12:21-30; Ex.1002, Fig. 26.

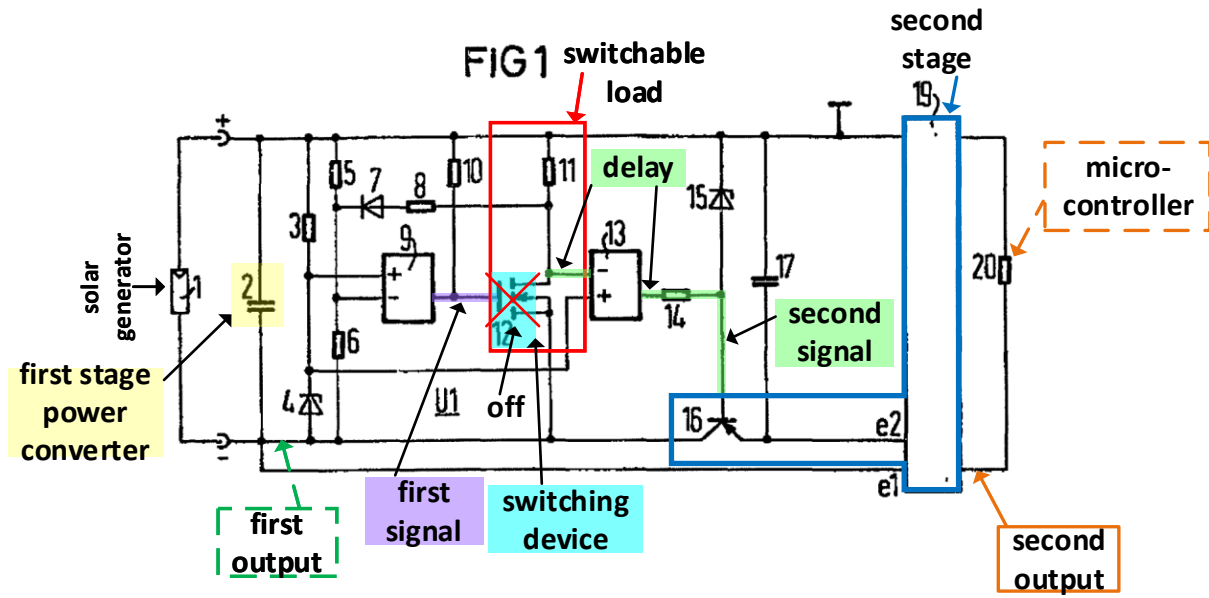


Fig. 26

141) When the first output reaches a high voltage, the output of the first comparator 9 turns the transistor 12 “off” (i.e., when the output voltage at the first output reaches the desired threshold voltage, see ¶84)). Ex.1002, 10:16-29,12:21-30 The circuit of Mieth that generates **the first signal** (i.e., the output of the first comparator 9 that feeds the gate of the transistor 12) is *analogous to the first signal portion of claim 5.*

142) Mieth discloses delaying the first signal from the first comparator 9 to generate a second signal at the output of the second comparator 13 to enable the second stage power converter to power the load 20. Mieth discloses that the field-effect transistor 12 and comparator 13 (hereinafter the second comparator 13) **delays the first signal from the first comparator 9 to generate a second signal** (highlighted-green) that turns on the bipolar transistor 16. More particularly, the second

comparator 13 outputs the second signal based on an output from the field-effect transistor 12, where the output from the field-effect transistor 12 (i.e., the drain terminal thereof) is itself based on the first signal. *Id.* As such, the state of the second signal is dictated by the state of the first signal, and the transition of the second signal to activate bipolar transistor 16 is delayed with respect to the transition of the first signal by the propagation delays of the transistor 12 and the second comparator 13 which is analogous to the claimed ***delaying the first signal.***

The second comparator 13 generates the second signal based on the first signal which is analogous to the claimed ***to generate a second signal,*** and the second signal controls the bipolar transistor 16 which operates as a switch to selectively pass the first output to the second stage power converter 19 at the e2 terminal.

Ex.1002, Fig. 26. Upon the second stage power converter 19 being powered by the first output via bipolar transistor 16 at e2, the second stage power converter 19 provides the second output that powers the load 20, which is the micro-controller.

This circuit functionality is analogous to the last part of claim 5, wherein the ***control circuit is configured to generate the second delayed signal that instructs the second stage power converter to change from not powering the micro-controller to powering the micro-controller.***

143) Furthermore, while not required by the claim language nor described as necessary in the detailed description of the '405 Patent, if it is contended that the *delaying the*

first signal should be defined by a specific delay circuitry rather than the intrinsic switching and delay characteristics of comparator 13 and switch 12. For example, a PHOSITA would have known to interpose one or more buffer circuits or delay elements could be interposed between the second comparator output and the base of bipolar transistor 16. Further, or in the alternative, a PHOSITA would have known to add a capacitor (optionally with a series resistor) parallel to resistor 11 according to customary practices in the art at the time of filing to define a larger delay period as is well known and customary in the general knowledge of a PHOSITA. Ex.1015, 3:53-63, Fig.3.

144) Thus, Mieth teaches all the features of claim 5.

5. Dependent Claim 6

145) Claim 6 depends upon claim 5, and feature [6A] recites hysteresis, namely,

“wherein the control circuit comprises: a hysteresis amplifier coupled to the first output to generate the first signal....” A PHOSITA understands hysteresis is a positive feedback loop between the output of a device and an input of a device, such as an amplifier or comparator, to mitigate instability in switched signals. See above ¶¶ 57-60 and 81-86; Ex. 1009. A PHOSITA would further understand that an amplifier can be configured as a comparator, and thus the first comparator 9 can be an amplifier. Id.

146) As shown in Fig. 27 below, Mieth discloses a capacitor 2 (highlighted-yellow) that outputs a first output (dashed-green) analogous to the claimed first output, and the first comparator 9 (dashed-blue) that is analogous to the claimed hysteresis amplifier that outputs a first signal (highlighted-purple) analogous to the claimed first signal that teach [6A] as discussed further below.

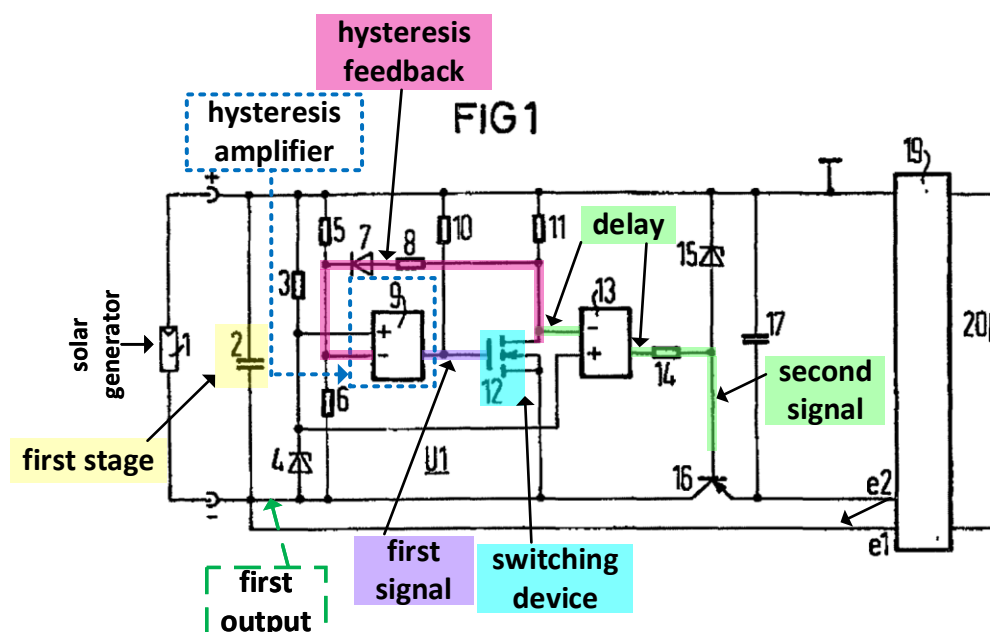


Fig. 27

147) The first comparator 9 is configured with hysteresis where the hysteresis feedback path (highlighted-pink) from the output of the switching device (field-effect transistor 12) is connected to the negative input node of the first comparator 9 through resistor 8 and diode 7. Ex.1002, 9:34-38. Furthermore, Mieth recites that “hysteresis is achieved by means of the resistor 8.” Ex.1002, 12:26-27. Specifically, when the switch 12 is off, the series circuit comprising resistors, 8, 11 and diode 7 are in parallel with resistor 5 forming a voltage divider with resistor 6.

When the switch 12 is on, diode 7 is non-conducting and no current flows through resistor 8 leaving only resistors 5 and 6 to form the voltage divider. In this way the first comparator 9 and associated circuitry exhibit hysteretic behavior. Since the first comparator 9 can be an amplifier with a positive feedback loop, the first comparator 9 is the same as the claimed ***hysteresis amplifier***. The first output of the capacitor 2 is represented at the negative input node of the first comparator 9 through a voltage divider defined by resistors 5 and 6 in addition to resistors 8 and 11 and diode 7 when comparator 9 output is low, and the first comparator 9 outputs the first signal, which is analogous to the claimed ***hysteresis amplifier coupled to the the first output to generate the first signal***. Ex.1002,9:34-38.

148) Thus, Mieth teaches [6A].

149) Claim 6 further requires [6B], “a delay circuit coupled to the first signal to generate the second delayed signal.” Fig. 27 further illustrates the field-effect transistor 12 (switching device, highlighted-teal) and the second comparator 13 that delays the first signal (highlighted-purple) from first comparator 9 to generate a second signal (highlighted-green). Ex.1002, Fig.1,11:4-12.

150) The delay circuit operates when the first signal goes low, causing transistor 12 to turn “off,” and pulling the drain terminal thereof high due to no current conducting through resistor 11. With the drain terminal connected to the negative input terminal of the second comparator 13, the drain terminal going high causes the

output of the second comparator 13 to go low (i.e., the second signal), which activates the bipolar transistor 16. The propagation delays from the first signal through the transistor 12 and the second comparator 13 constitute a delay circuit that delays the second signal with respect to the first signal. That is, when the first signal goes low, the second signal goes low thereafter by a delay time period dictated by the transistor 12 and the second comparator 13.

151) Since, the field-effect transistor 12 and the second comparator 13 are coupled together and delay the first signal to generate the second signal at the output of the second comparator 13, the field-effect transistor 12 and the second comparator 13 are analogous to the claimed ***delay circuit coupled to the first signal to generate the second delayed signal***. However, if it is argued that the *delay* circuit should be defined by further specific circuitry rather than the intrinsic switching characteristics of second comparator 13 and switch 12, delay elements discussed in accordance with claim 5 in ¶143 can be implemented.

152) Thus, Mieth teaches [6B].

6. Independent Claim 7

153) Claim 7 is an independent claim, and is directed toward a method of supplying power. With reference to the claim listing appendix, Mieth discloses elements [7A]-[7H] as provided below

i. [7A]: “A method to supply power, the method comprising:”

154) Mieth (Ex.1002) discloses a circuit that supplies power to an electrical load from a solar generator. Ex.1002 (Mieth), 8:8-9. A PHOSITA would understand that when the circuit of Mieth supplies power to the electrical load, the circuit is performing a method to supply power to the electrical load. Thus, Mieth teaches [7A].

ii. [7B]: “generating, by a first stage power converter, a first output from a direct current input;”

155) PHOSITA understands that solar generators generate a direct current. Ex.1013, ¶ 21. As such, the solar generator 1 of Mieth supplies a ***direct current input*** (dashed-red) to the capacitor 2 that is analogous to a first stage power converter as shown in Fig. 29 below. The ‘405 Patent does not define what is a first stage power converter, but instead merely recites its function in claim 7; namely to generate a first output from a direct current input. The first stage power converter of Mieth is a parallel capacitor 2 that performs the recited method function in that it converts power associated with the direct current input into a ***first output*** (dashed-green) as shown.

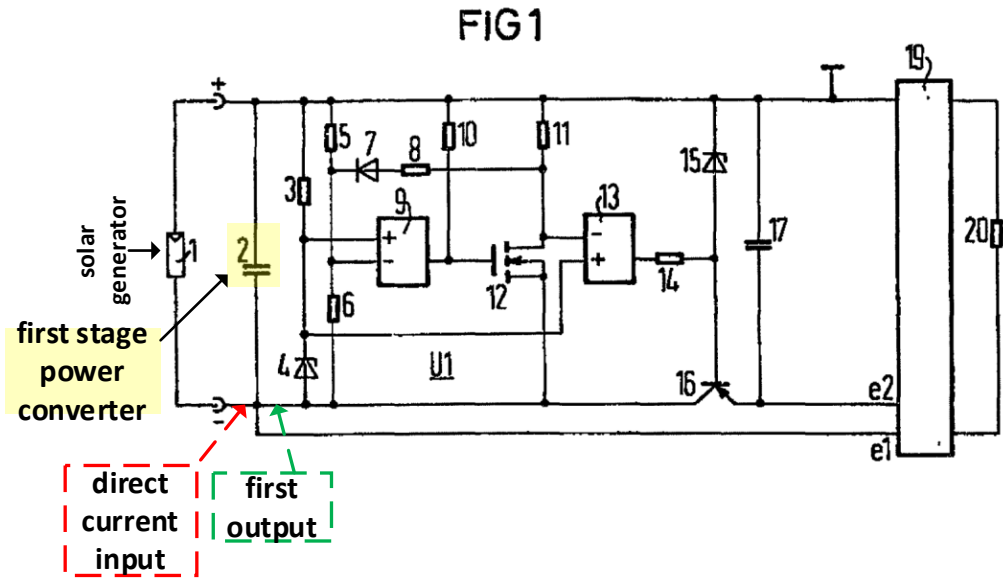


Fig. 28

156) Thus, Mieth discloses [7B].

iii.[7C]: “powering a control circuit using the first output;”

157) Mieth discloses, *inter alia*, a first comparator 9 that turns the transistor 12 “on” or “off” as shown in Fig. 29. Ex.1002, 9:34-10-14.

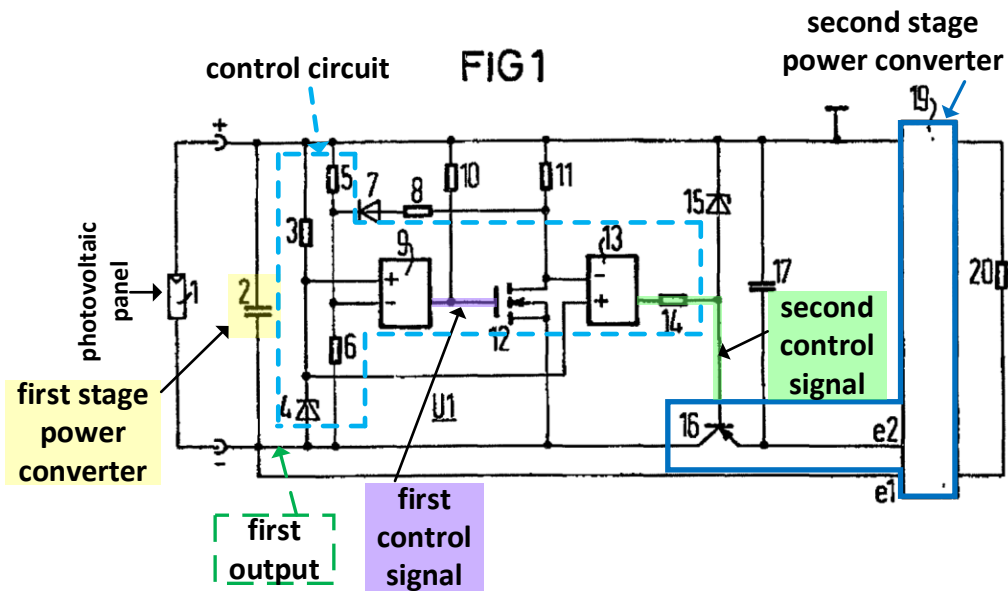


Fig. 29

158) First comparator 9 compares the reference voltage from the reference voltage generator 3,4 to a representative voltage from the voltage divider 5,6.

Ex.1002,9:34-10:3. First comparator 9 compares the monitored voltage to the threshold voltage (See ¶84) to determine if the monitored voltage exceeds a threshold (in magnitude) defined by the reference voltage, and outputs a first control signal (highlighted-purple) to transistor 12 based on the comparison.

Ex.1002, 12:12-26.

159) A PHOSITA understands that the circuitry (dashed-blue) that controls transistor 12, which includes first comparator 9, voltage divider 5,6 and reference input generator 4 are coupled electrically to the first output, and thus are powered by the first output from the capacitor 2, is analogous to the claimed *powering a control circuit using the first output*. Ex.1002,9:34-10:3.

160) Thus, Mieth disclose [7C].

iv. [7D]: “generating, by a second stage power converter connected to the first stage power converter, a second output from the first output from the first stage power converter;”

161) In Mieth, a power supply apparatus 19 connected to a bipolar transistor 16 (second stage-blue) together constitutes a *second stage power converter connected* (green) to a capacitor 2 that forms the first stage power converter and generates the first output (dashed-green), as illustrated below in Fig. 30. Thus, *Mieth discloses a first*

stage power converter connected (green) to a second stage power converter, as shown in Fig. 30.

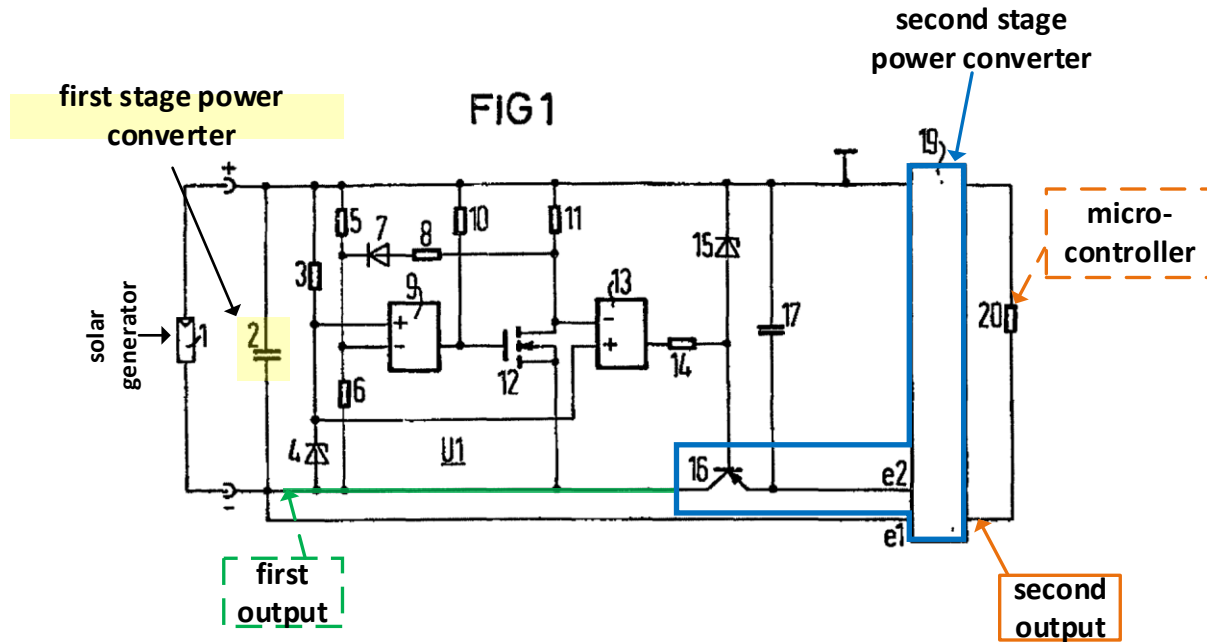


Fig. 30

162) Still referring to the figure above, the power supply apparatus 19 **is powered** by way of auxiliary voltage input e2 which is associated with the first output when the bipolar transistor 16 is conducting (green), Fig. 30. Ex.1002, 8:29-35. According to Mieth, the power supply apparatus 19 is a DC-DC voltage converter or a charging converter and outputs a voltage and current to power the micro-controller load 20. *Id.* As a power converter, power supply apparatus 19 receives the first output and **converts the first output to a second output** (orange) as shown in Fig. 30. As shown, the second output is provided by the second stage power converter 16/19 to the load/microcontroller (dashed-orange). Ex.1014, 1180, Fig.5.

163) Thus, Mieth teaches [7D].

- v. [7E]: “**blocking, by the control circuit during a time period that is after the control circuit is powered by the first output and before a predefined condition is met in the control circuit, the second output from the second stage power converter from powering a micro-controller;**”

164) According to element [7E], the control circuit functions to block the second stage power converter from powering the micro-controller using the second output in a time period. Further, element [7E] requires the time period in which such control occurs to be bounded by two constraints: (1) after the control circuit is powered by the first output, and (2) before a predefined condition is met in the control circuit. Mieth discloses such functionality in the control circuit for at least the reasons set forth above in ¶¶ 113-119.

165) Therefore the function of the control circuit is analogous to ***blocking, by the control circuit during a time period that is after the control circuit is powered by the first output and before a predefined condition is met in the control circuit, the second output from the second stage power converter from powering a micro-controller.***

166) Thus, Mieth teaches [7E].

- vi. [7F]: “**consuming, by a switchable load in a power absorption circuit, a portion of the first output from the first stage power converter during the time period;**”

167) As discussed above in accordance with ¶¶ 109-119 in discussing elements [1F] and element [1G] (that define and disclose the “time period”), in the first state associated with relatively low voltages at the first output, the preliminary, switchable load 11 and the field-effect transistor 12 (i.e., switchable load-**red**) are powered by the first output of capacitor 2 (i.e., first stage power converter-**highlighted-yellow**). See Fig. 31 below. In this condition, with the transistor 12 conducting, the switchable load 11 operates as part of a power absorption circuit to consume at least a part of the first output. Ex.1002,18:19-19:3;19:9-14.

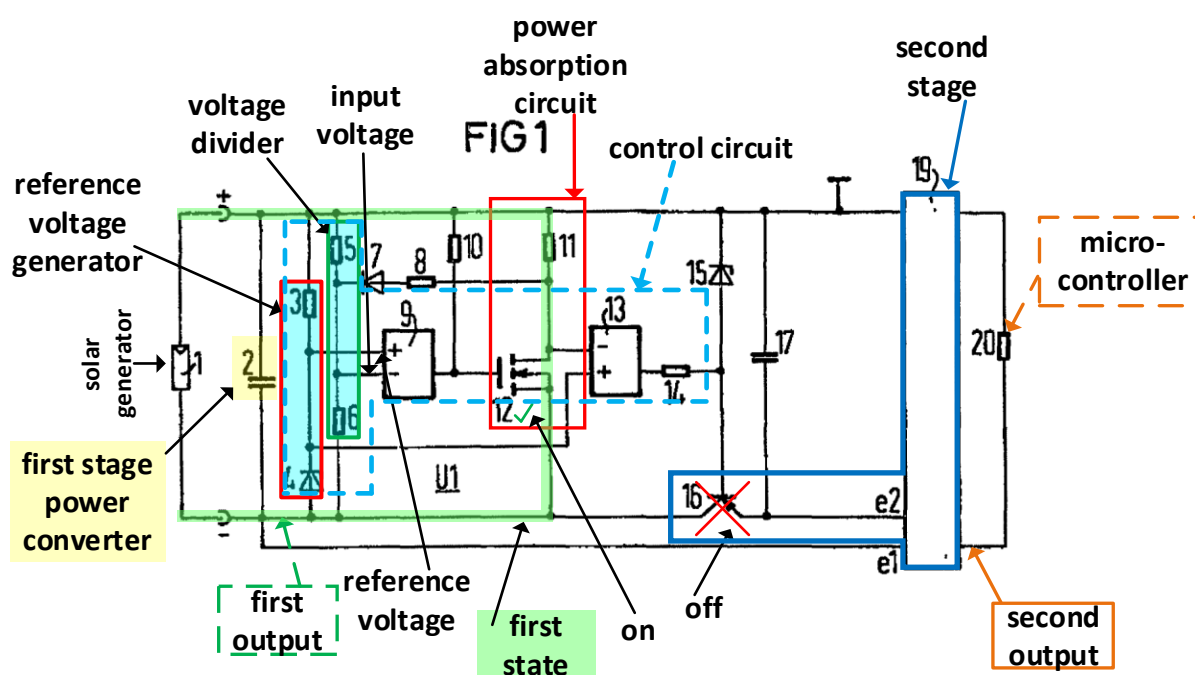


Fig. 31

168) Thus, in the first state, the control circuit function is analogous to the claim feature *consuming, by a switchable load in a power absorption circuit, a portion of the*

first output from the first stage power converter during the time period.

(Ex.1001, claim 1).

169) Thus, Mieth teaches feature [7F].

vii. [7G]: “powering the micro-controller using the second output from the second stage power converter after the time period; and”

170) Mieth further discloses that when voltages from the solar generator 1 reflected at the first output (as represented at the negative terminal of first comparator 9) are above a predefined minimum value (as represented at the positive terminal of first comparator 9)(i.e., the “predefined condition” is met at relatively “high” first output voltages) the control circuit transitions the circuit to the second state. In the second state the auxiliary voltage input e2 of the power supply apparatus 19 is connected to the first output of the first stage power converter 2. Ex.1002, 9:23-26. As shown in Fig. 32 below, when the predefined condition is satisfied, the circuit of Mieth operates in the second state (highlighted-pink) where transistor 12 is shut off. As the output of the first comparator goes low, the second comparator 13 trips, resulting in the second comparator 13 output going low. With the output of the second comparator 13 (the second signal) going low, the bipolar transistor 16 turns “on,” causing the first output (dashed-green) of capacitor 2 to be connected to e2, thereby powering the power supply apparatus 19. Ex.1002, 10:16-29. With the power supply apparatus 19 powered during the second state

(which is after the time period), the second stage power converter is operational and provides the second output to power the load 20, which may be a micro-controller. Ex.1002,17:19-18:3; Ex.1014,1180,FIG.5.

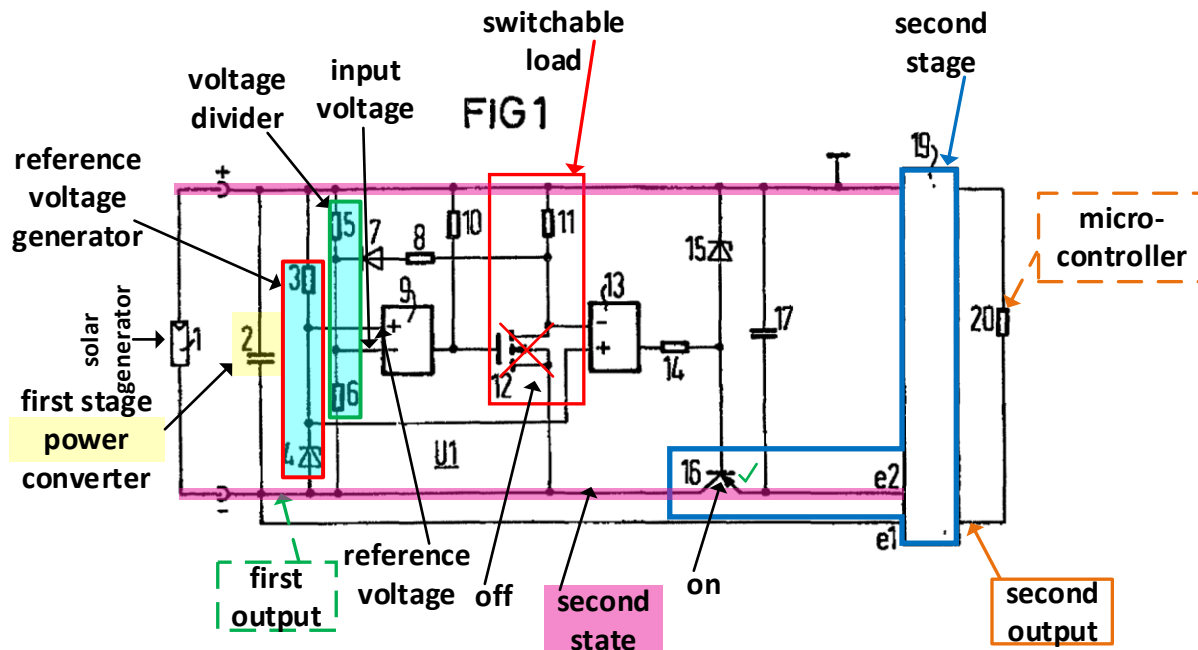


Fig. 32

171) Therefore the function of the control circuit in the second state is analogous to ***powering the micro-controller using the second output from the second stage power converter after the time period.***

viii. [7H]: “stopping, by the control circuit and after the time period, the switchable load from consuming the first output from the first stage power converter.”

172) In the first state, the first comparator 9 outputs a high value, resulting in transistor 12 being “on”, and the switchable load 11 consuming the first output. Ex.1002, 12:12-26. While in the first state, when the first output of capacitor 2 rises in

magnitude and the monitored voltage across voltage divider 5, 6 rises above the threshold, see ¶84), (i.e., “predefined minimum value” as quoted by Mieth), the “time period” of the first state ends, and the control circuit disconnects the preliminary load 11 from the first output due to the output of the first comparator 9 going low, thus configuring the field-effect transistor 12 to an “off” state, which results in the preliminary load 11 (i.e., the switchable load) not consuming the first output in the second state. In this way, the control circuit function in the second state is analogous to ***stopping, by the control circuit and after the time period, the switchable load from consuming the first output from the first stage power converter.***

173) Thus, Mieth teaches claim element [7H]. As Mieth teaches all elements [7A]-[7H] of claim 7, Mieth anticipates the claim.

7. Dependent Claim 8

174) Claim 7 is taught by Mieth. See above ¶¶ 153-173. Claim 8 depends from claim 7 and requires, “wherein the predefined condition includes a voltage of the first output reaching a threshold.” Ex.1001, claim 8.

175) The feature of claim 8 is the same as claim 2. As discussed in detail above in ¶¶ 125-130, Mieth discloses this feature.

176) Thus, Mieth discloses the method feature of claim 8 for at least the same reasons.

8. Dependent Claim 9

177) Claim 7 is taught by Mieth. See above ¶¶ 153-173. Claim 9 depends from claim 7 and element [9A] requires, “signaling, by the control circuit, the switchable load to be in a first state of consuming the portion of the first output during the time period,” and element [9B] requires, “signaling, by the control circuit, the switchable load to be in a second state of not consuming the first output from the first stage power converter after the time period.” Ex.1001, claim [9A]-[9B]. As set forth above in ¶¶ 120-123, for element [1H]. Mieth discloses each of features [9A]-[9B] for at least the same reasons.

178) Thus, Mieth discloses features [9A] and [9B].

9. Dependent Claim 11

179) Claim 9 is taught by Mieth. See above ¶¶ 177-178. Claim 11 depends from claim 9 and element [11A] requires, “wherein the switchable load includes a resistive device, and a switching device connected to the resistive device,” element [11B] requires “turning on the switching device to place the switchable load in the first state in which the resistive device is connected to the first output,” and element [11C] requires “turn[ing] off the switching device to place the switchable load in the second state in which the resistive device is disconnected from the first output.” Ex.1001, claim [11A]-[11C]. As set forth above in ¶¶ 131-138, for elements [4A]-[4B], Mieth discloses each of features [11A]-[11C] for at least the same reasons.

180) Thus, Mieth discloses features [11A], [11B] and [11C].

10. Dependent Claim 12

181) Claim 9 is taught by Mieth. See above ¶¶ 177-178. Claim 12 depends from claim 9 and element [12A] requires, “delaying, by the control circuit, a first signal instructing the switching device to change from the first state to the second state,” and element [12B] recites, “generating, via the delaying, a second delayed signal that instructs the second stage power converter to change from not powering the micro-controller to powering the micro-controller.” Ex.1001, claim [12A]. As set forth above in ¶¶ 139-144, for elements [5A]-[5C], Mieth discloses each of features [12A]-[12B] for at least the same reasons.

182) Thus, Mieth discloses features [12A] and [12B].

11. Dependent Claim 13

183) Claim 12 is taught by Mieth. See above ¶¶ 181-182. Claim 13 depends from claim 12 and requires, “generating the first signal using a hysteresis amplifier coupled to the first output.” Ex.1001, claim 13. As set forth above in ¶¶ 145-152, for element [6A], Mieth discloses the feature of claim 13 for at least the same reasons.

184) Thus, Mieth discloses claim 13.

B. Ground B: Obviousness of claims 1-2, 4-9 and 11-13 over Mieth in view of Balogh

1. Independent Claim 1

185) With reference to the claim listing appendix, Mieth is believed to disclose all the elements of claims 1-2, 4-9 and 11-13. To the extent it is argued that Mieth does not teach the first stage power converter (e.g., elements [1C] and [7B]), Balogh discloses a first stage power converter as set forth in elements [1C] and [7B]. Further, as explained below, a PHOSITA would have been motivated to combine together Mieth and Balogh to arrive at the alleged invention of claims 1-2, 4-9 and 11-13.

i. [1C]: “a first stage power converter to generate a first output from a direct current input;”

186) A PHOSITA understands that solar generators generate a direct current. Ex.1013,

¶21. As such, the solar generator 1 of Mieth supplies a ***direct current input*** (dashed-red) to the capacitor 2 as shown in **Error! Reference source not found.**

below, and generates a first output.

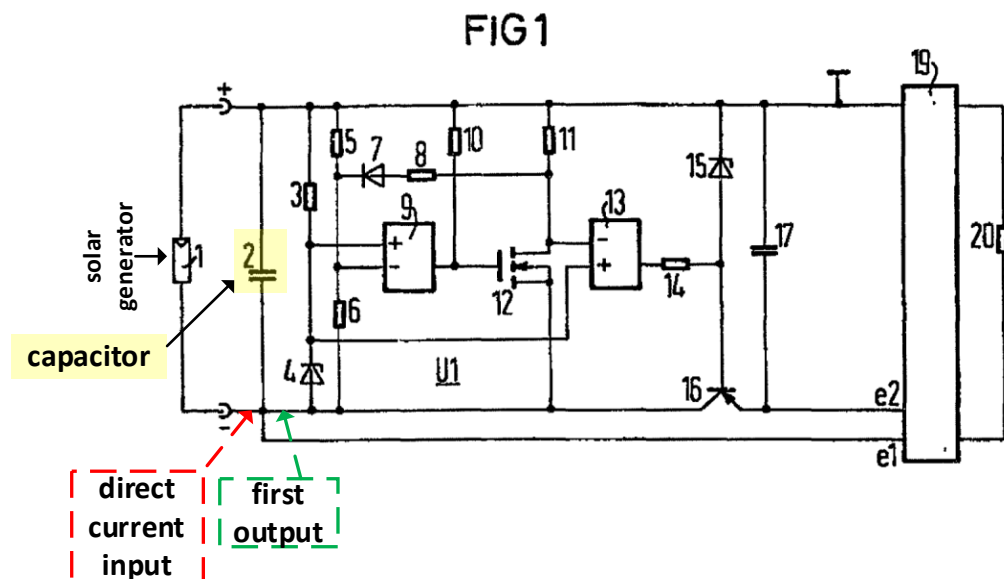


Fig. 33

187) Balogh discloses cascaded converter arrangements (e.g., Ex.1003(Balogh), Figs.1B-1D), and states that cascaded arrangements using first and second buck converters are employed in circuit applications that require large input/output conversion ratios. Ex.1003, 1:21-27. It is known to a PHOSITA that photovoltaic panels or modules can realize high input voltages, and such high input voltages need large input/output conversion ratios to step down the input voltage. Ex.1003, 1:21-27. Even a single photovoltaic module can see a voltage as high as 80V, which may necessitate a large input/output conversion ratio. Ex.1010; Ex.1011. Balogh teaches in Fig 1D a cascaded converter arrangement using **a first stage transformer-coupled input power converter that steps down an input voltage to an intermediate voltage**, followed by a second stage buck output power converter

that further steps down the intermediate voltage to a final voltage. Ex.1003,1:62-66. Thus, Balogh clearly discloses **a first stage power converter**, as recited in element [1C] and shown in Fig. 34 below.

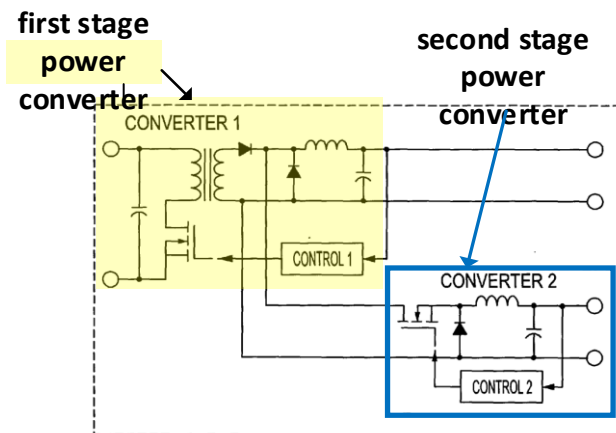


FIG. 1D

PRIOR ART

Fig. 34

188) Mieth states that applications having photovoltaic energy sources or wind energy sources often provide varying levels of input voltage that can create difficulties when serving as an input to a power converter. Ex.1002, 5:22-38. Mieth further teaches the use of a switchable load in situations where an input voltage to a power converter varies, such as the voltage from a photovoltaic system that will vary depending upon the time of day, or weather conditions. Ex.1002, 5:22-38.

189) A PHOSITA is motivated to combine the cascaded power converter architecture of Balogh with Mieth. Balogh discloses the first stage power converter to replace the capacitor 2 of Mieth and generate two, cascaded power converters with the

switchable load feature of Mieth for DC applications with high input voltages.

Mieth is directed towards solar generators that generate up to 36 volts. Ex.1002,

12:21-26. Balogh discloses higher DC voltages relative to Mieth, for example,

48V with large step-down ratios, for example, 48V to 1.5V. Ex.1003, 10:45-52.

In other prior art examples, solar panel modules can have 80V output voltages

requiring large step-down ratios. Ex.1010;Ex.1011; As such, a PHOSITA would

have known and been motivated to combine the cascaded power converter

architecture of Balogh with Mieth for high DC applications (e.g., 48V or 80V solar

panel modules) to realize an appropriate intermediate voltage for the second stage

power converter 16/19 of Mieth.

190) The combination of Mieth-Balogh involves combining known prior art elements

(Mieth's switchable load and step-down converter and Balogh's cascaded step

down converter architecture) according to known methods to yield predictable

results, i.e., a cascaded step-down power converter having a switchable load at the

second power converter input that is selectively employed based on the output

voltage of the first stage step-down power converter. A PHOSITA would have had

the skills, knowledge, and motivation to carry out the combination. A PHOSITA

would have reasonably expected success in combining Mieth and Balogh as no

significant modifications are required to implement. *Id.* A PHOSITA would have

appreciated the benefit of adapting the high DC voltage stepped down to an

intermediate voltage of Balogh to situations with a variable input voltage to a power converter as shown in Mieth. As understood by a PHOSITA, there are no undue technical hurdles to applying Mieth with Balogh or vice-versa, as such a combination would have been a simple modification to Mieth's system, readily accomplished by a PHOSITA. Accordingly, Mieth in combination with Balogh is proper and teaches element [1C]. *Id.*

191) Specifically, while the capacitor 2 discussed above in ¶¶ 97-104 (see Fig. 18 above) provides the recited function of the first stage power converter as recited in the claims, and the bipolar transistor 16/power supply apparatus 19 is analogous to the claimed second stage power converter, Balogh discloses a cascaded converter arrangement having an isolated DC-DC converter in its first stage that is explicitly set forth as a first stage power converter that also receives a direct current input and provides a first output. Ex.1003, 10:45-52.

192) Balogh's isolated DC-DC converter (analogous to the first stage power converter-yellow) and post regulator circuit are cascaded step-down converters and are shown in Fig. 34. Ex.1003, 2:61-64. The DC-DC converter includes a transformer with an input winding that receives a direct current input, and a secondary, output winding that generates a first output based on the turns ratio of the transformer.

193) Based on Balogh, a PHOSITA would understand that cascaded converters are commonly used to provide input to output power conversion that is not optimally implemented in a single converter. Ex.1003, 1:25-28. Thus, the purpose of the first stage power converter and the second stage power converter was previously described by Balogh, that is, to provide input-to-output power conversion that is not optimally implemented in a single converter, for example, in high DC voltage applications. Ex.1003, 10:45-52. The claimed first stage power converter of Balogh can replace the capacitor 2 of Mieth to provide a first output to be consumed by the switchable load or to power the second stage power converter, and the claimed second stage power converter uses the first output from the first stage to power the micro-controller, which is not optimally implemented by a single converter (e.g. the first stage power converter or the second stage power converter alone). As such, a PHOSITA, at the time of filing, would know that the capacitor 2 of Mieth could be replaced by the first stage power converter of Balogh, and combined with the power supply apparatus 19 of Mieth to form a cascaded converter architecture as disclosed by Balogh.

194) In addition, it is well known in the art that improved efficiency can be achieved by cascading buck power converters when there is a large ratio of input to output voltage as described in Patent application: US 2007/0001653 (hereafter “Xu”). Ex. 1012. Xu states: “The present invention provides a two-stage power delivery

system that employs cascaded buck stages. For high input-to-output voltage ratios, each cascaded buck stage has a more suitable (i.e., larger) duty cycle that results in a much lower total power loss than in a single-stage buck.” Ex. 1012, ¶6.

195) In addition, Xu reflects further general knowledge of a PHOSITA that cascaded converters advantageously improve circuit efficiency. Ex. 1012. Xu states that in some applications where there is a lower input-to-output voltage ratio, for example, like in Mieth, the first stage power converter can be configured with a duty cycle of one so that it operates as a well-known L-C filter for the subsequent second stage, thereby being substantially similar to Mieth’s capacitor 2 input stage. For at least these reasons, it would have been obvious for a PHOSITA to combine Balogh with Mieth in view of the general knowledge of a PHOSITA, as shown by the teaching of Xu, where large output/input ratios are more efficient when implemented with cascaded buck converters.

196) Thus, Xu provides a teaching that a PHOSITA would readily consider a cascaded converter arrangement in various solar applications, such as the application taught in Mieth. As such, a PHOSITA, at the time of filing, would know that the capacitor 2 of Mieth could be replaced readily by the first stage power converter of Balogh, and combined with the power supply apparatus 19 of Mieth to form a cascaded converter architecture as disclosed by Balogh.

197) Thus, Balogh discloses [1C], and in combination with Mieth, Mieth-Balogh teaches all the elements [1A]-[1H] of claim 1, as well as claims 2, and 4-6.

198) For at least the same reasons set forth above in ¶¶ 186-197, Balogh discloses element [7B], and in combination with Mieth, Mieth-Balogh discloses all the elements [7A]-[7H] of claim 7, as well as claims 8-9 and 11-13.

C. Ground C: Obviousness of claims 3 and 10 in view of Mieth and Liu, or over Mieth-Balogh and further in view of Liu

1. Dependent Claim 3

199) Claim 1 is taught by Mieth alone, or by a combination of Mieth-Balogh. See ¶¶ 95-124 and 185-198. Claim 3 depends from claim 1 and requires, “wherein, when the switchable load is in the second state, the voltage above the threshold is sufficient to power the second stage power converter to operate the micro-controller for at least a predetermined period of time during which the direct current input to the first stage power converter has diminishing power.” Fig. 35 below illustrates Mieth in the second state. As taught in Mieth, when voltages from the solar generator 1 (as represented at the negative terminal of first comparator 9) are above a predefined minimum value (as represented at the positive terminal of first comparator 9)(i.e., relatively “high” first output voltages), the control circuit transitions the circuit to the second state, wherein the auxiliary voltage input e2 of the power supply apparatus 19 is connected to the first output of the solar generator 1. Ex.1002, 9:23-26. As shown in Fig. 35 below, when the

predefined minimum value is satisfied (i.e., the voltage associated with the first output exceeds the claimed threshold), the circuit of Mieth operates in the second state (highlighted-pink) where the field-effect transistor 12 is “off” or non-conducting, thereby disconnecting the preliminary load 11 from the first output. Id.

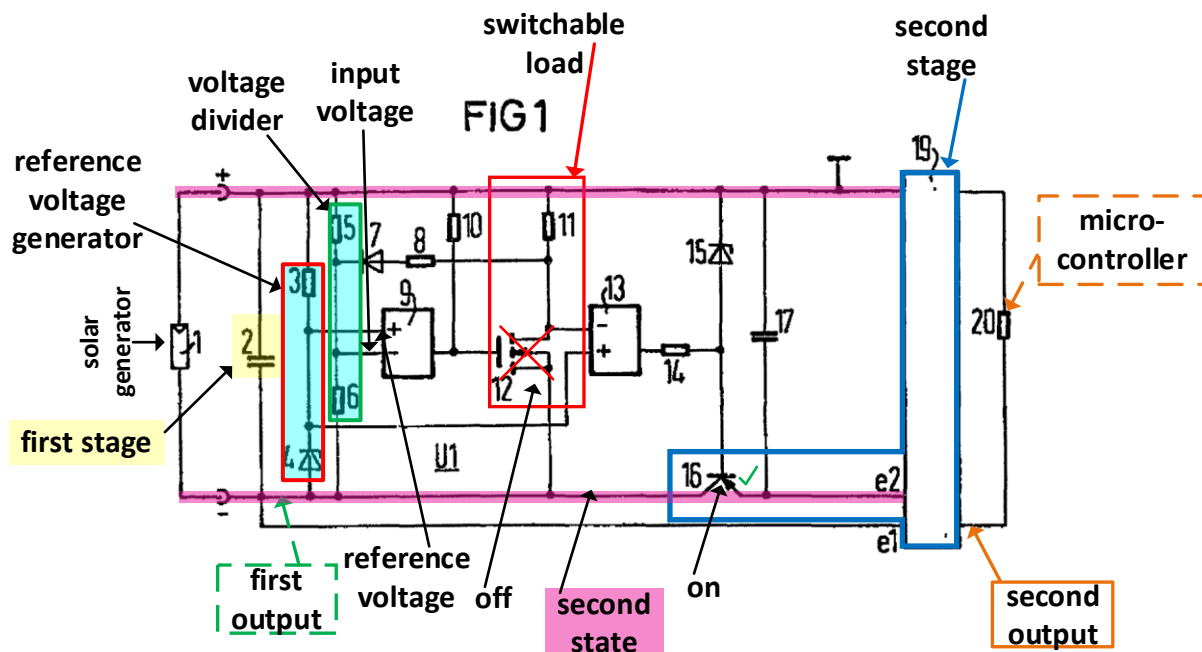


Fig. 35

200) As discussed above in ¶¶ 113-119, the first comparator 9 compares the reference voltage from the reference voltage generator (highlighted-teal-outlined-red) to the representative voltage from the voltage divider (highlighted-teal-outlined-green) to determine if the representative voltage exceeds a threshold defined by the reference voltage. Thus, according to Mieth, *the design of the reference voltage generator*

dictates the magnitude of the threshold that triggers the exit from the first state and entry into the second state. Ex.1002, 12:12-26.

- 201) As shown above, upon the control circuit of Mieth causing the circuitry to exit the first state and enter the second state, the first output is large enough that the threshold defined by the reference voltage generator is exceeded, and the first output is passed to the e2 terminal of the second stage power converter 19.
- 202) More particularly, when the voltage representative of the first output exceeds the threshold, the transistor 12 is shut “off,” pulling its output node (connected to the negative input terminal of the second comparator 13) high due to the resistor 11. This causes the output of the second comparator 13 to go low, thus turning bipolar transistor 16 “on,” and passing the first output to the e2 terminal to power the second stage power converter 19, which, in turns provides the second output to the micro-controller 20.
- 203) Claim 3 requires that when the direct current input to the first stage power converter has diminishing power, the threshold is sufficient for the second stage power converter to operate the micro-controller for at least a predetermined period of time. Ex.1001, claim 3. The ‘405 patent does not define or provide any context for what constitutes the predetermined period of time for the claim feature. In the second state, when the direct current input to the first stage power converter has diminishing power, the first output will begin to decrease. As the second stage

power converter 19 has a range of input voltages at which it may operate effectively to provide the second output to the micro-controller 20, Mieth's control circuit is operable to allow the second stage power converter 19 to operate the micro-controller 20 for a predetermined period of time despite a decreasing first output voltage, as no minimum time period is set forth by the claim, nor provided as an example in the detailed description of the '405 patent. Thus, Mieth discloses this feature.

204) If Mieth standing alone is not deemed to provide adequate support for the feature of claim 3, Liu discloses use of a reservoir capacitor 58 between first and second stage power converters, so that if the first stage power converter is inoperable or otherwise deficient, the capacitor provides auxiliary power to the second stage power converter to power the micro-controller for the predetermined period of time. Ex.1005, 4:25-50.

205) Mieth discloses transistor 12 connected to preliminary load/resistor 11 to form a power absorption circuit coupled to the first output, as, during the first state, power from the first output is at least partially consumed by the preliminary load/resistor 11. Ex.1002, 9:15-32, 10:5-14. Mieth does not disclose that preliminary load/resistor 11 includes a capacitor. However, Liu (Ex.1005) discloses a capacitor as a power absorption circuit coupled to the first output and feeding a

second stage power converter and a PHOSITA is motivated to combine Mieth and Liu for at least the following reasons.

206) As shown in Fig. 36, Liu discloses cascaded DC voltage converters with an input stage (or first stage power converter) 50 separated from an output stage (or a second stage power converter) 60 by a reservoir capacitor 58. Ex.1005, 4:25-35.

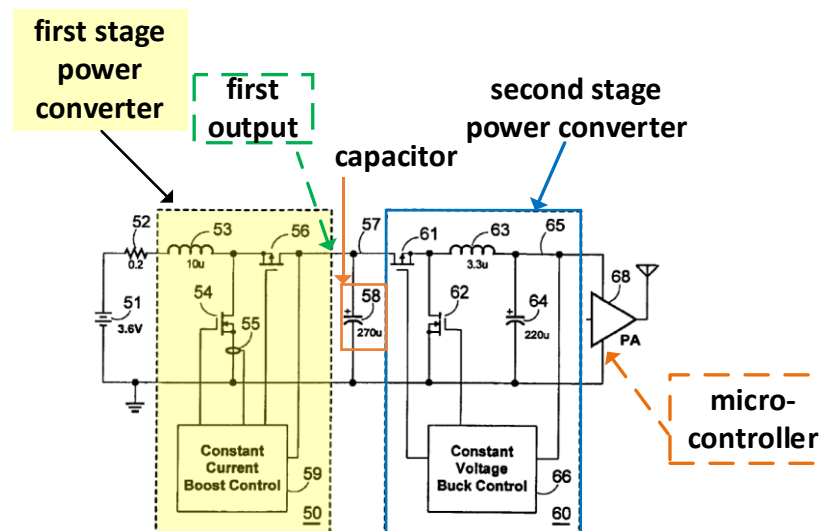


Fig. 36

207) The first stage power converter 50 converts the voltage from battery 51 to charge reservoir capacitor 58, and second stage power converter 60 down converts the voltage of reservoir capacitor 58 to power a power amplifier (“PA”) 68. Ex.1005, 4:36-43. Since first stage power converter 50 (highlighted-yellow) converts an input voltage to an output voltage, input stage 50 is analogous to the claimed first stage power converter of claim 1, and the output (dashed-green) of first stage power converter 50 is analogous to the claimed *first output* of claim 3. Since the reservoir capacitor 58 (orange) is charged from the first output of the first stage

power converter 50, reservoir capacitor 58 absorbs the first output of the first stage power converter 50, and as the capacitor 58 charges, in combination with Mieth, the voltage at the voltage divider eventually exceeds the “predefined condition” which causes the control circuit of Mieth to transition from the first state (lower first output voltages) to the second state (higher first output voltages).

208) Claim 3 further requires “the voltage above the threshold is sufficient to power the second stage power converter to operate the micro-controller for a predetermined period of time during which the direct current input to the first stage power converter has diminishing power.”

209) Liu teaches that reservoir capacitor 58 provides most of the energy to PA 68 through output stage 60 for a period of time when battery 51 cannot supply power to the PA 68. Ex.1005, 1:8-12,4:43-51. A PHOSITA understands that capacitor 58 provides power to the PA 68 for a predetermined period of time by sizing the capacitor appropriately. Furthermore, while Liu shows PA 68 powered by reservoir capacitor 58 through the second stage power converter 60, a PHOSITA understands that reservoir capacitor 58 and output stage 60 could power another load (as opposed to the PA 68) such as the claimed *micro-controller*. *Id.* Thus, capacitor 58 that can provide power to the PA 68 for a period of time is analogous to the claimed *voltage above the threshold is sufficient to power the second stage power converter to operate the micro-controller for at least a predetermined*

period of time during which the direct current input to the first stage power converter has diminishing power.

210) Liu discloses cascaded power converters with a capacitor that provides power to a load through a second power converter for a period of time without incoming power from a first power converter. Ex.1005, 4:36-43. Mieth teaches use of a power absorption circuit when an input voltage to a power converter varies, such as the voltage from a photovoltaic system that varies depending upon time of day, or weather conditions. Ex.1002, 5:22-38. Mieth in view of Balogh disconnects the switchable load between first stage and second stage power converters when the input voltage to the first stage power converter meets a stable criterion according to a voltage threshold. *Id.* A PHOSITA is motivated to combine the capacitor of Liu with the power absorption circuit (i.e., the switchable load 11/12) of Mieth, as the capacitor provides a more stable power source to Mieth's load (i.e., the micro-controller) for a predetermined time period when the power absorption circuit is disconnected from the circuit or voltage from the photovoltaic system is varying due to dynamic conditions. *Id.*

211) A PHOSITA is motivated to employ known means in the art, as taught in Liu, to modify the circuit of Mieth (e.g., Fig. 35 such that when Mieth is in the second state and the monitored voltage connected to first comparator 9 falls below the predefined minimum value (i.e., the "predefined threshold") according to the first

output, the capacitor of Liu powers load 20 (i.e., micro-controller) through power supply apparatus 19 (i.e., the second stage power converter) for a predetermined period of time, ***which is analogous to claim 3***. Therefore, both Mieth and Liu provide an express motivation to combine together to improve a cascaded power converter system by including a capacitor in the power absorption circuit. *Id.*

212) The combination of Mieth-Liu involves combining known prior art elements (replacing/combining Mieth's resistive load between converters with Liu's capacitive load between converters) according to known methods to yield predictable results, a cascaded power converter having a capacitive load at the second power converter input. A PHOSITA has the skills, knowledge, and motivation to carry out the combination. A PHOSITA would reasonably expect success in combining Mieth and Liu, and there is no undue technical hurdles in combining Mieth with Liu, as the combination is a simple modification to Mieth's system. *Id.*

213) If it is argued that Mieth does not teach a first stage power converter, Mieth may be combined with Balogh to provide such feature, as set forth in ¶¶ 185-198. Further, Liu may be combined with a combination of Mieth-Balogh for at least the reasons above in ¶¶ 199-212.

214) Thus, Mieth-Liu, or alternatively Mieth-Balogh-Liu disclose claim 3.

2. Dependent Claim 10

215) Claim 9 is taught by Mieth alone, or by a combination of Mieth and Balogh.

Claim 10 depends from claim 9 and requires, “wherein, when the switchable load is in the second state, the voltage above the threshold is sufficient to power the second stage power converter to operate the micro-controller for at least a predetermined period of time during which the direct current input to the first stage power converter has diminishing power.” This claim language is identical to the claim language of claim 3. It is submitted that claim 10 is taught by a combination of Mieth and Liu, or alternatively by a combination of Mieth, Balogh and Liu for at least the same reasons articulated above for claim 3.

216) Thus, Mieth-Liu, or alternatively Mieth-Balogh-Liu disclose claim 10.

VIII. CONCLUDING STATEMENT

Under penalty of perjury, all statements made herein of my own knowledge are true, and I believe that all statements made herein on information and belief to be true. I have been warned and I am aware that willful false statements are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code. In signing this Declaration, I understand that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may

be subject to cross-examination in the case and that cross-examination will take place in the United States. If cross examination is required of me, I undertake to appear within the United States during the time allotted for cross-examination, and within the limits of my ability so to do. I declare under penalty of perjury that the foregoing is true and correct.

Executed on 23 June 2023.

A handwritten signature in black ink, reading "Douglas Holberg", written over a horizontal line.

Douglas Holberg

IX. CLAIM LISTING APPENDIX

U.S. Patent No. 10,333,405 - Avrutsky	
Claim Element Designation	Claim Element
Claim 1	
[1A]	An apparatus, comprising;
[1B]	a micro-controller;
[1C]	a first stage power converter to generate a first output from a direct current input;
[1D]	a switchable load powered by the first output;
[1E]	a control circuit powered by the first output; and
[1F]	a second stage power converter connected to the first stage power converter and configured to convert the first output to a second output;
[1G]	wherein the control circuit is configured to block the second stage power converter from powering the micro-controller using the second output in a time period that is after the control circuit is powered by the first output and before a predefined condition is met in the control circuit; and
[1H]	wherein the control circuit is configured to signal the switchable load to be in a first state of consuming the first output during the time period and to be in a second state of not consuming the first output after the time period.
Claim 2: wherein the predefined condition includes a voltage of the first output reaching a threshold.	
Claim 4: wherein the switchable load comprises: a resistive device.	
Claim 5: wherein the control circuit delays a first signal instructing the switching device to change from the first state to the second state to generate a second delayed signal that instructs the second stage power converter to change from not powering the micro-controller to powering the micro-controller.	
Claim 6:	
[6A]	wherein the control circuit comprises: a hysteresis amplifier coupled to the first output to generate the first signal
[6B]	a delay circuit coupled to the first signal to generate the second delayed signal.
Claim 7: The method of claim 6, wherein when the switch device is turned on,	

the switchable load and an input of the second stage are connected in parallel to the first output of the first stage.	
[7A]	A method to supply power, the method comprising:
[7B]	generating, by a first stage power converter, a first output from a direct current input;
[7C]	powering a control circuit using the first output;
[7D]	generating, by a second stage power converter connected to the first stage power converter, a second output from the first output from the first stage power converter;
[7E]	blocking, by the control circuit during a time period that is after the control circuit is powered by the first output and before a predefined condition is met in the control circuit, the second output from the second stage power converter from powering a micro-controller;
[7F]	consuming, by a switchable load in a power absorption circuit, a portion of the first output from the first stage power converter during the time period;
[7G]	powering the micro-controller using the second output from the second stage power converter after the time period; and
[7H]	stopping, by the control circuit and after the time period, the switchable load from consuming the first output from the first stage power converter.
Claim 8: wherein the predefined condition includes a voltage of the first output reaching a threshold.	
Claim 9	
[9A]	signaling, by the control circuit, the switchable load to be in a first state of consuming the portion of the first output during the time period; and
[9B]	signaling, by the control circuit, the switchable load to be in a second state of not consuming the first output from the first stage power converter after the time period.
Claim 11	
[11A]	wherein the switchable load includes a resistive device, and a switching device connected to the resistive device;
[11B]	turning on the switching device to place the switchable load in the first state in which the resistive device is connected to the first output.
Claim 12	
[12A]	delaying, by the control circuit, a first signal instructing the

	switching device to change from the first state to the second state.
[12B]	generating, via the delaying, a second delayed signal that instructs the second stage power converter to change from not powering the micro-controller to powering the micro-controller.
Claim 13: generating the first signal using a hysteresis amplifier coupled to the first output.	