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APPLICATION ELEMENTS:

(X) Specification in seven (7) pages.

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RANK BUFFERED DUAL INLINE MEMORY MODULE

Background of the Invention

Field of the Invention

[0001] The present invention relates to memory modules for use in computers, and more specifically, relates to configurations of memory devices and other components of a memory module.

Description of the Related Art

[0002] Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

Brief Description of the Drawings

[0003] Figure 1 schematically illustrates a block diagram of a rank-buffered dual inline memory module (DIMM) memory subsystem in accordance with embodiments described herein.

Summary of the Invention

[0004] In certain embodiments, a memory module comprises a dual inline memory module (DIMM) comprising two or more ranks of memory devices and a logical translation element. The logical translation element is electrically connectable to a memory controller of a computer system and is electrically connected to the ranks of memory devices. In certain embodiments, the logic translation element comprises address decoding logic which translates between a system memory density domain of the computer system to a physical memory density domain of the DIMM.

[0005] In certain embodiments, the memory devices of the DIMM are configured in two or more ranks of memory devices. A pair of memory devices, one from each of two ranks, are configured to simulate a memory device having twice the memory capacity of an individual memory device. The DIMM of certain embodiments utilizes a transition bit to select which rank of memory devices is enabled for a read or write transfer operation. In

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certain embodiments, the logic translation element further comprises a data path multiplexer/demultiplexer which logically isolates the ranks of memory devices from one another. In certain embodiments, the logic translation element further comprises a serial-presence-detect (SPD) element which reports the CAS latency (CL) to the memory controller. The SPD element of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array.

Detailed Description

[0006] In certain embodiments, a memory module comprises a logical translation element which advantageously increases the addressable ranks per dual inline memory module (DIMM). The memory module of certain embodiments comprises a DDR2 SDRAM memory array, while other embodiments comprise other types of memory arrays.

[0007] Figure 1 schematically illustrates a block diagram of a dual inline memory module (DIMM) memory subsystem in accordance with embodiments described herein. The DIMM of Figure 1 comprises a logic translation element, labeled as "Rank Buffer DIMM Logic (RBDL)." In certain embodiments, the logic translation element is electrically connected to the memory controller of the computer system and is electrically connected to the ranks of memory devices (or chips) of the DIMM. In certain embodiments, the logic translation element comprises address decoding logic which transparently translates from a system memory density domain of the computer system to a physical memory density domain of the DIMM.

[0008] In certain embodiments, the logic translation element comprises a data path multiplexer/demultiplexer which logically isolates the ranks of memory devices from one another. The data path multiplexer/demultiplexer of certain embodiments advantageously diminishes the effects of jitter and other sources of noise, and simplifies various other aspects of operation of the memory module, including, but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

[0009] In certain embodiments, the logic translation element comprises a serial-presence detect (SPD) element which reports the CAS latency (CL) to the memory controller. The SPD element of certain embodiments reports a CL which has one more cycle than does

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the actual operational CL of the memory array. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices from the memory controller. The buffer of certain embodiments comprises combinatorial logic, registers, and logical pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer.

[0010] In certain embodiments, the logic translation element increases the size of the memory array supported by the memory controller of the computer system. This larger memory array has an increased number of ranks of memory devices of the DIMM, with a corresponding increased number of memory devices and chip selects. The SPD element of the memory module of certain embodiments informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices resident on the memory module. For example, for computer systems which are normally limited to using DIMMs which have a single rank of 128M-by-4bit memory devices, certain embodiments described herein enable the computer system to utilize DIMMs which have double the memory, e.g., two ranks of 128M-by-4bit memory devices. In certain such embodiments, the logic translation element provides the address decoding logic to double the number of chip selects, and the SPD element of the memory module reports a memory device density of 256M-by-4bit to the computer system.

[0011] In certain embodiments, the logic translation element provides substantially all of the translation logic used for the address decoding. In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module.

[0012] In certain embodiments, the doubling of the memory device density implies an additional row, column, or bank bit. This additional bit is defined, in certain embodiments, as the transition bit, which selects which rank of memory devices is enabled

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for a read or write transfer operation. Table 1 shows the associated transition bit for various embodiments of memory device density transitions.

Table 1:

Density Transition	Transition Bit
256-Mb to 512-Mb	A13
512-Mb to 1-Gb	BA2
1-Gb to 2-Gb	A14

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 2-Gb memory devices to simulated 4-Gb memory devices.

[0013] In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD element to the memory controller), the memory devices advantageously support the "open row" feature.

Example 1

[0014] In an exemplary embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by the logic translation element to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the logic translation element activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A13.

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Example 2

[0015] In another exemplary embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA2 (bank 2) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA2 bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

Example 3

[0016] In another exemplary embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two 1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the logic translation element activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A14.

[0017] In certain embodiments, the multiplexer/demultiplexer advantageously provides DQ/DQS paths for each rank of memory devices which are separate from one another, and which are separate from the memory controller of the computer system. In certain such embodiments, data transfers between the memory controller and the DIMM are registered for one additional clock cycle by the logic translation element. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. Thus, for example, a DDR2 400-MHz memory system in accordance

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with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three.

[0018] Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

[0019] Certain embodiments described herein advantageously use memory devices (e.g., dynamic-random-access memory, or DRAM, devices) to achieve a desired memory density of the DIMM. In certain such embodiments, the overall cost of the DIMM is reduced. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the DIMM by a factor of up to approximately five.

[0020] Certain embodiments described herein do not require system level changes to hardware (e.g., the motherboard) or to software (e.g., the BIOS).

[0021] Certain embodiments described herein utilize a single rank interface, which decreases the loading on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

[0022] Certain embodiments described herein provide a rank-buffered DIMM technology which is highly scalable over various DRAM technologies, DRAM densities, and frequencies. Certain embodiments described herein are applicable to DRAM technologies which include, but are not limited to, SDR, DDR1, DDR2, and DDR3. Certain embodiments described herein are applicable to memory densities including, but not limited to, 256-Mb, 512-Mb, 1-Gb, 2-Gb, 4-Gb, and above. Certain embodiments described herein are applicable to various frequencies including, but not limited to, 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above.

[0023] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative and are not intended to be limiting. Various

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modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

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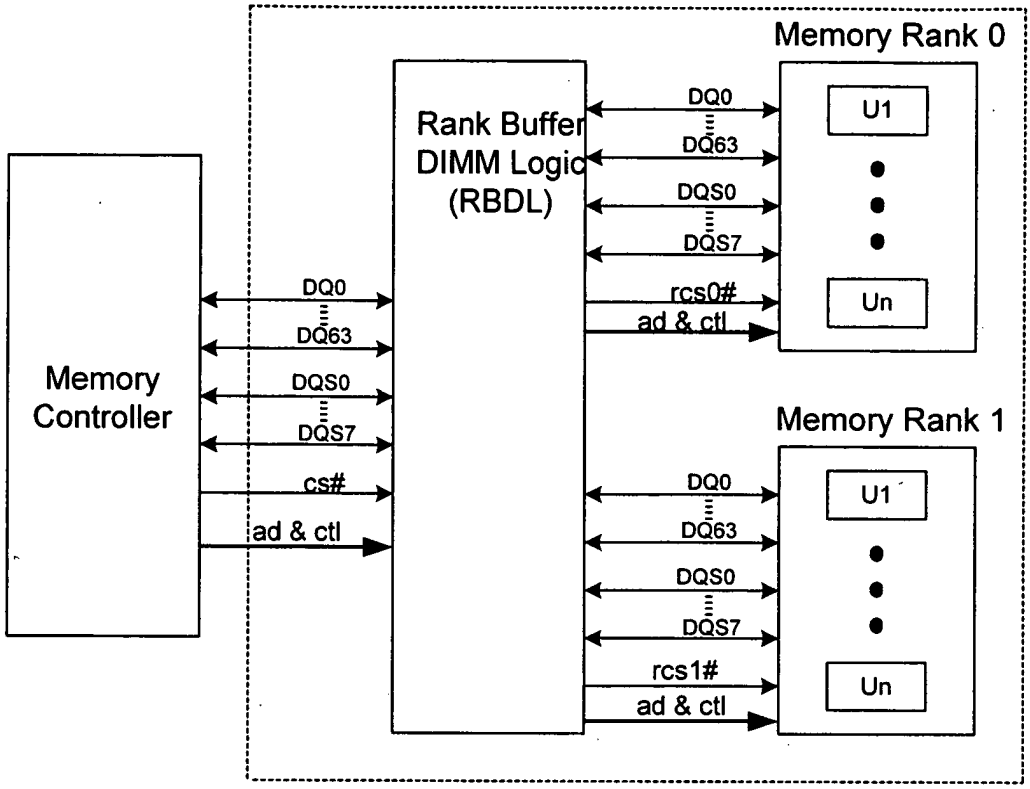
FIGURE 1:



Block Diagram: Rank Buffered DIMM Memory Sub-system

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