

**PROVISIONAL APPLICATION FOR PATENT
COVER SHEET**

Case No. NETL.025PR

Date: May 28, 2004

Page 1

22264 U.S. PTO
60/575595

**Commissioner for Patents
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Sir:

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR § 1.53(c).

For: **METHOD OF FORMING A MEMORY MODULE HAVING x8 ORGANIZATION
USING DRAM DEVICES HAVING x4 ORGANIZATION**

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Enclosed are:

- (X) Specification in forty-seven (47) pages, including Appendix 1 which includes Appendix A, Appendix B, Appendix C, and Appendix D.
- (X) A check in the amount of \$160 to cover the filing fee is enclosed.
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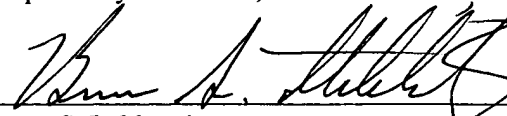
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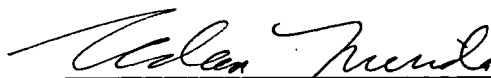
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Attorney Docket No. : NETL.025PR
Applicants : William M. Gervasi et al.
For : METHOD OF FORMING A MEMORY
MODULE HAVING x8 ORGANIZATION
USING DRAM DEVICES HAVING x4
ORGANIZATION
Attorney : Bruce S. Itchkawitz
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**METHOD OF FORMING A MEMORY MODULE HAVING x8 ORGANIZATION
USING DRAM DEVICES HAVING x4 ORGANIZATION**

Detailed Description

[0001] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0002] For example, a 512-Megabyte memory module (termed a “512-MB” memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a “512-Mb” DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such memory devices with 64M 8-bit-wide memory locations (actually with 2^{27} or 134,217,728 one-bit memory cells) are identified as having a “64M x 8-bit” configuration. Thus, a commercially-available 512-MB memory module is termed to have a “64M x 8-byte” configuration or a “64M x 64-bit” configuration.

[0003] Similarly, a 1-Gigabyte memory module (identified as a “1-GB” memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a “1-Gb” DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and each memory location having a width of 8 bits. Such memory devices with 128M 8-bit-wide memory locations (actually with 2^{27} or 134,217,728 memory locations) are identified as having a “128M x 8-bit” configuration. Thus, a commercially-available 1-GB memory module is identified as having a “128M x 8-byte” configuration or a “128M x 64-bit” configuration.

[0004] The commercially-available 512-MB (64M x 8-byte) memory modules and the 1-GB (128M x 8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such “x 8” organizations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with “x 4” organizations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available “x 4” memory modules include, but are not limited to, 512-MB (128M x 4-byte) memory modules comprising eight 512-Mb (128M x 4-bit) memory devices.

[0005] However, rather than fabricating a 1-GB (128M x 8-byte) memory module using eight 1-Gb (128M x 8-bit) DRAM devices, it may be desirable to fabricate a 1-GB (128M x 8-byte) memory module using sixteen 512-Mb (128M x 4-bit) DRAM devices. Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM). In other words, the price per bit ratio of the higher-density DRAM device is greater than that of the lower-density DRAM device. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM device, until volume production factors reduce the costs of the newer higher-density DRAM device. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

[0006] Table 1 provides the numbers of rows and columns for various memory devices as specified by JEDEC standard JESD79D, “Double Data Rate (DDR) SDRAM Specification,” published February 2004, and incorporated in its entirety by reference herein.

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for “x 4” organization	11	11	12	12
Number of column address bits for “x 8” organization	10	10	11	11
Number of column address bits for “x 16” organization	9	9	10	10

As described by Table 1, 512-Mb (128M x 4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128M x 8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128M x 8-byte) memory module using sixteen 512-Mb (128M x 4-bit) DRAM devices.

[0007] Certain embodiments described herein provide an apparatus and method for utilizing two lower-density (e.g., 512-Mb) memory devices to simulate one higher-density (e.g., 1-Gb) memory device without utilizing complex address translation procedures or structures. In certain embodiments, the apparatus and method described herein are useful for memory modules comprising a plurality of memory devices mounted (e.g., soldered) on a printed circuit board (PCB).

[0008] Such memory modules generally include serial-presence-detect (SPD) data stored in an SPD device, such as a serial electrically-erasable, programmable, read-only memory (EEPROM) device, mounted on the PCB. This SPD data contains pertinent information on the memory module, such as the number of row addresses, the number of column addresses, and the data width of each device. From the SPD data, the total memory capacity of the memory module can be calculated. Upon booting a computer comprising the memory module, the SPD device provides the SPD data to the basic input/output system (BIOS). The BIOS then uses the SPD data to configure the computer memory properly for maximum reliability and performance.

[0009] For a commercially-available 512-MB (64M x 8-byte) memory module utilizing eight 512-Mb memory devices each with a 64M x 8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

- Byte 3: Defines the number of row address bits in the DRAM component in the memory module [13 for the 512-Mb memory device].
- Byte 4: Defines the number of column address bits in the DRAM component in the memory module [11 for the 512-Mb memory device].
- Byte 13: Defines the width of the primary DRAM component used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory device].

Byte 14: Defines the width of the error checking DRAM component used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM component used in the memory module [4 for the 512-Mb memory device].

[0010] Similarly, for a commercially-available 1-GB (128M x 8-byte) memory module utilizing eight 1-Gb memory devices each with a 128M x 8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM component in the memory module [14 for the 1-Gb memory device].

Byte 4: Defines the number of column address bits in the DRAM component in the memory module [11 for the 1-Gb memory device].

Byte 13: Defines the width of the primary DRAM component used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory device].

Byte 14: Defines the width of the error checking DRAM component used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM component used in the memory module [4 for the 1-Gb memory device].

[0011] In certain embodiments disclosed herein, two lower-density memory devices are used to simulate one higher-density memory device. In such embodiments, the SPD device of the memory module is programmed to describe the combined pair of lower-density memory devices as one pseudo-higher-density memory device.

[0012] In an exemplary embodiment, two 512-Mb memory devices, each with a 128M x 4-bit configuration, are used to simulate one 1-Gb memory device having a 128M x 8-bit configuration. The SPD device of the memory module is programmed to describe the pair of 512-Mb memory devices as one pseudo-1-Gb memory device.

[0013] For example, to fabricate a 1-GB (128M x 8-byte) memory module, sixteen 512-Mb (128M x 4-bit) memory devices can be used. The sixteen 512-Mb (128M x 4-bit) memory devices are combined in eight pairs, with each pair serving as a pseudo-1-Gb (128M x 8-bit) memory device. In such embodiments, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.
Byte 4: 12 column address bits.
Byte 13: 8 bits wide for the primary DRAM component of the pseudo-1-Gb (128M x 8-bit) memory device.
Byte 14: 8 bits wide for the error checking DRAM component of the pseudo-1-Gb (128M x 8-bit) memory device.
Byte 17: 4 banks.

[0014] In this exemplary embodiment, bytes 3, 4, and 17 are programmed to have the same values as they would have for a 512-MB (128M x 4-byte) memory module utilizing 512-Mb (128M x 4-bit) memory devices. However, bytes 13 and 14 of the SPD data are programmed to be equal to 8, corresponding to the bit width of the pseudo-higher-density 1-Gb (128M x 8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[0015] Appendix 1 describes a configuration in which two output signal pins of two lower-density memory components are connected together to form the pseudo-higher-density memory component. For example, a data strobe pin (DQS) of a first lower-density memory component can be connected to the DQS pin of another lower-density memory component utilizing current-limiting resistors.

[0016] Thus, by allowing two lower-density memory components to be used rather than one higher-density memory component, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory components to build “next-generation” higher-density memory modules.

[0017] Certain embodiments described herein also do not require hardware changes, since the configuration of the memory module is stored in software. In addition, certain embodiments described herein avoid the need for complicated row and column steering logic circuits that would otherwise add cost and lower performance.

[0018] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting.

Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

Summary of the Invention

[0019] In certain embodiments, a memory module has a memory configuration and comprises a printed circuit board (PCB), a plurality of dynamic random-access memory (DRAM) devices mounted on the PCB, and a serial-presence-detect (SPD) device mounted on the PCB. Each DRAM device of the plurality of DRAM device has a first data width, a first number of rows, and a first number of columns. The SPD device comprises data that characterizes the memory configuration of the memory module as having a second data width equal to twice the first data width, a second number of rows equal to the first number of rows, and a second number of columns equal to the first number of columns.

APPENDIX 1:

UNBUFFERED MEMORY MODULE USING SHARED DQS PINS

Summary of the Invention

[0001] In certain embodiments, an unbuffered memory module uses two lower-density DDR DRAM integrated circuits with shared DQS pins to simulate one higher-density DDR SDRAM integrated circuit.

[0002] In certain embodiments, a 1-GB unbuffered memory module is formed by connecting together at least one pair of 256-Mb memory components with 64Mb x 4 organization so as to function as one 512-Mb device with 64Mb x 8 organization.

[0003] In certain embodiments, an unbuffered memory module comprises a plurality of pairs of lower-density memory components, each pair connected together with shared DQS pins to simulate a higher-density memory component.

Brief Description of the Appendices

[0004] Appendix A: Data sheets of an exemplary 1-GB unbuffered double data rate (DDR) dual in-line memory module (DIMM) in accordance with embodiments described herein.

[0005] Appendix B: Schematic drawing of an exemplary 1-GB unbuffered DDR DIMM in accordance with embodiments described herein.

[0006] Appendix C: Printed circuit board layer diagrams including signal traces of an exemplary 1-GB unbuffered DDR DIMM in accordance with embodiments described herein.

[0007] Appendix D: Schematic circuit diagrams of an exemplary 1-GB unbuffered DDR DIMM in accordance with embodiments described herein.

Brief Description of the Drawings

[0008] Figure 1 schematically illustrates a configuration in which a DQS pin of a first device is connected to a DQS pin of a second device.

[0009] Figure 2 is a timing diagram of the voltages supplied from the two DQS pins due to non-simultaneous switching.

[0010] Figure 3 schematically illustrates an exemplary embodiment in which current-limiting resistors are used to reduce the current flow between the DQS pins.

[0011] Figure 4 is a circuit diagram of exemplary current-limiting resistors in conjunction with the impedances of the DRAM devices and provides an exemplary calculation of the resultant power dissipation.

Detailed Description of the Preferred Embodiment

[0012] Most high-density unbuffered memory modules are currently built with 512-Megabit ("512-Mb") memory components with 64Mb x 8 organization. For example, a 1-Gigabyte ("1-GB") memory module can be fabricated using eighteen such 512-Mb memory components. Alternatively, it is advantageous to be able to fabricate the 1-GB memory module using lower-density memory components. For example, by fabricating the 1-GB memory module using thirty-six 256-Mb memory components with 64Mb x 4 organization, the cost of the resulting 1-GB memory module can be reduced since the cost of the 512-Mb memory components is typically much higher than the 256-Mb memory components. The cost savings is significant, even though twice as many 256-Mb memory components are used than 512-Mb memory components.

[0013] For proper operation, the computer system advantageously recognizes the 1-GB memory module comprising 256-Mb memory components with 64Mb x 4 organization as having 512-Mb memory components with 64Mb x 8 organization of the same depth. This advantageous result would desirably be achieved by connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory components. However, it is a general guideline of memory module design to not connect two output signal pins together in this way.

[0014] Figures 1 and 2 schematically illustrate the problem arising from tying together two signal pins. Figure 1 schematically illustrates a configuration in which a DQS pin 12 of a first device 10 is connected to a DQS pin 22 of a second device 20. The two DQS pins 12, 22 are both connected to a controller 30. Figure 2 is a timing diagram of the voltages supplied from the two DQS pins 12, 22 due to non-simultaneous switching.

[0015] The DQS or data strobe is a bi-directional signal which is used during both read cycles and write cycles to validate or latch data. At time t_1 , both DQS pin 12 and DQS

pin 22 are high, so no current flows between them. Similarly, at time t_4 , both DQS pin 12 and DQS pin 22 are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3 , DQS pin 12 is low while DQS pin 22 is high. Under such conditions, a current will flow between the two DQS pins 12, 22. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the DRAM read cycle. During such conditions, the current flowing between the two DQS pins 12, 22 can be substantial, resulting in heating of the devices 10, 20, and contributing to the degradation of reliability and eventual failure of these devices.

[0016] Figure 3 schematically illustrates an exemplary embodiment in which current-limiting resistors are used to reduce the current flow between the DQS pins. Such embodiments result in two x 4 DRAM memory devices of lower bit densities behaving as one x 8 device of higher bit density. The resistance values of the current-limiting resistors (e.g., 22 ohms in Figure 3) is selected to reduce the current flowing between the two DQS pins while allowing signals to propagate between the controller and the DQS pin.

[0017] Figure 4 schematically illustrates exemplary current-limiting resistors in conjunction with the impedances of the DRAM devices and provides an exemplary calculation of the resultant power dissipation. Without the 22 ohm current-limiting resistors, only the 17 ohm impedances of the two devices would limit the current flow between the two devices. In embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, the resistances of the current-limiting resistors is advantageously selected to account for such overshoot/undershoot of voltages. In certain embodiments, there is a potential increase of 12.5% overload on protection diodes if the system overshoot/undershoot are at maximum value (e.g., 1.2 Volts at 4 nanoseconds).

[0018] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

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Figure 1:

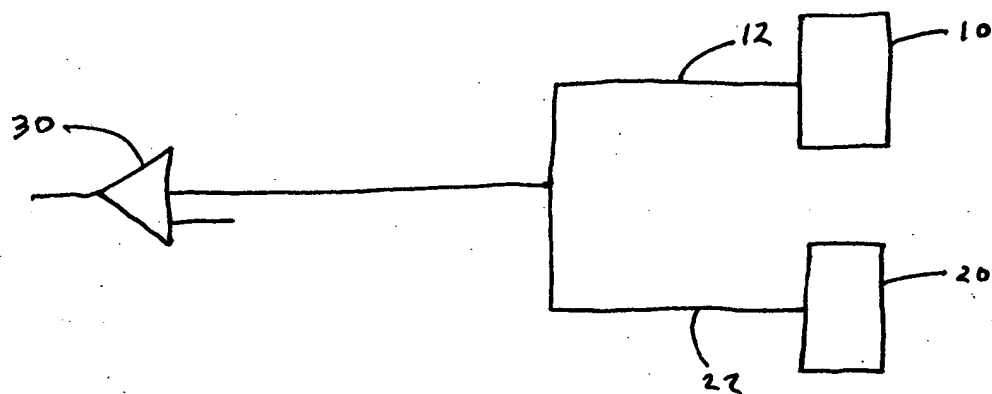


Figure 2:

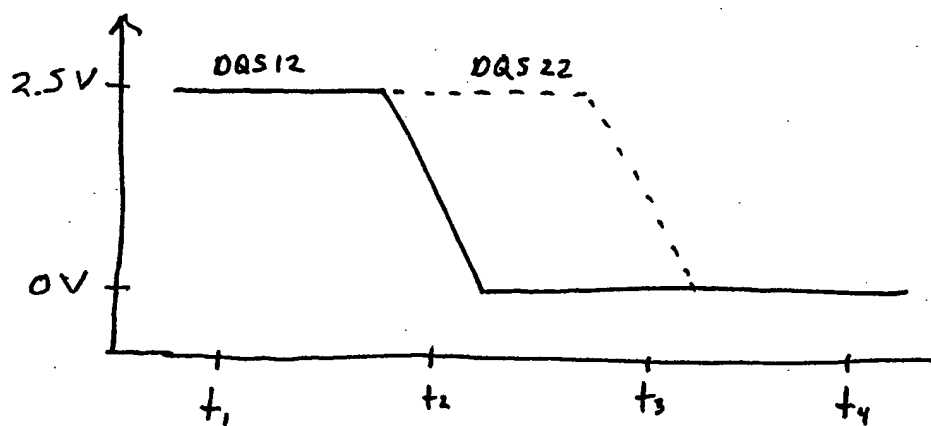


Figure 3:

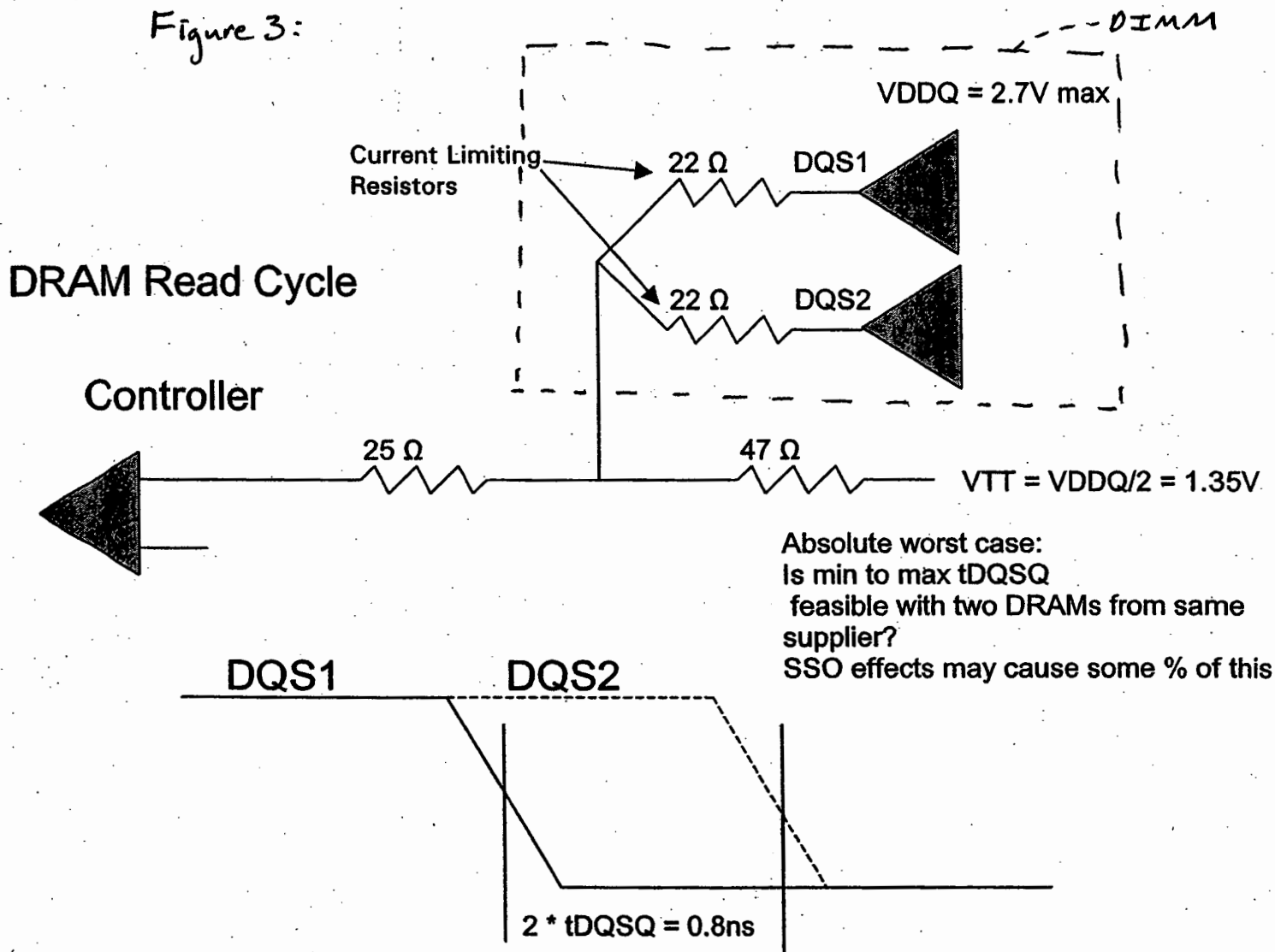
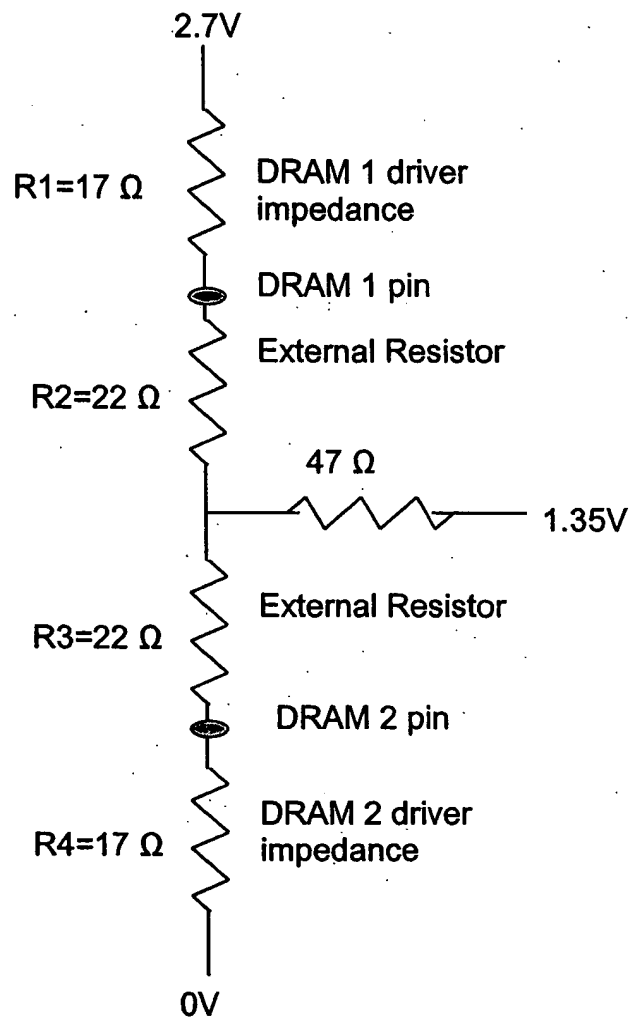


Figure 4:



Assertions:

Data Read operation so controller is in hi-Z

DRAM 1 driving high, DRAM 2 driving low

Upper network = lower network so mid-voltage = VTT voltage
therefore RTT is not considered

Concern is power burn in the drivers

Voltage at DRAM 2 pin = $R4 / (R1 + R2 + R3 + R4) * 2.7V = 0.59V$

Current in DRAM2 driver = $0.59V / R4 = 34 \text{ mA}$

Power dissipation in DRAM 2 driver = $34\text{mA} * 0.59V = 20 \text{ mW}$

22Ω resistors, R1 and R2 are current limiters

Duration of overdrive = 0.8ns max

Total surge = $0.59V * 1.2\text{ns} = 0.3 \text{ V-ns}$

JEDEC spec for overshoot/undershoot = 2.4 V-ns

GENERAL DESCRIPTION

The Netlist NL9127LD64032-Dxxx is a 128M bit x 72 Double Data Rate Synchronous Dynamic RAM high-density memory module. The Netlist module consists of thirty-six 64M x 4 bit, DDR-I SDRAM in FBGA packages, one PLL clock driver and one 2K EEPROM for Serial Presence Detect. All components are mounted on a 184-pin glass-epoxy substrate. The decoupling capacitors are mounted on the printed circuit board in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM.

Synchronous design allows precise control of data transfer between module and the system controller. Data transfer on both edges of DQS signal at various operating frequencies and programmable latencies. Therefore, these modules are suitable for a variety of high performance system applications.

FEATURES

- Double Data Rate design; two data transfers per clock cycle
- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- SSTL_2 compatible inputs and outputs
- Single VDD/VDDQ power supply
- Latency (Access from column address)
- Burst length (2, 4, 8)
- Data scramble (Sequential & Interleave)
- Serial presence detect with EEPROM
- PCB Height: 1.200"

Part No.	Max Clock Freq. (CL)Speed
NL9127LD64032-D27Jxy	166MHz (CL2.5), PC2700
NL9127LD64032-D32Kxy	200MHz (CL3), PC3200
x = DRAM Vendor	y = DRAM Die
S= Samsung, I= Infineon M= Micron	A=A die, B=B die, C=C die etc..

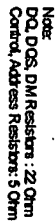
PIN CONFIGURATIONS

Front Side						Back Side					
1	VREF	32	A5	63	WE*	93	VSS	124	VSS	155	DQ45
2	DQ0	33	DQ24	64	DQ41	94	DQ4	125	A6	156	VDDQ
3	VSS	34	VSS	65	CAS*	95	DQ5	126	DQ28	157	S0*
4	DQ1	35	DQ25	66	VSS	96	VDDQ	127	DQ29	158	S1*
5	DQS0	36	DQS3	67	DQS5	97	DM0	128	VDDQ	159	DM5
6	DQ2	37	A4	68	DQ42	98	DQ6	129	DM3	160	VSS
7	VDD	38	VDD	69	DQ43	99	DQ7	130	A3	161	DQ46
8	DQ3	39	DQ26	70	VDD	100	VSS	131	DQ30	162	DQ47
9	NC	40	DQ27	71	NC	101	NC	132	VSS	163	NC
10	NC	41	A2	72	DQ48	102	NC	133	DQ31	164	VDDQ
11	VSS	42	VSS	73	DQ49	103	NC	134	CB4	165	DQ52
12	DQ8	43	A1	74	VSS	104	VDDQ	135	CB5	166	DQ53
13	DQ9	44	CB0	75	CK2*	105	DQ12	136	VDDQ	167	NC
14	DQS1	45	CB1	76	CK2	106	DQ13	137	CK0	168	VDD
15	VDDQ	46	VDD	77	VDDQ	107	DM1	138	CK0*	169	DM6
16	CK1	47	DQS8	78	DQS6	108	VDD	139	VSS	170	DQ54
17	CK1*	48	A0	79	DQ50	109	DQ14	140	DM8	171	DQ55
18	VSS	49	CB2	80	DQ51	110	DQ15	141	A10	172	VDDQ
19	DQ10	50	VSS	81	VSS	111	CKE1	142	CB6	173	NC
20	DQ11	51	CB3	82	VDDID	112	VDDQ	143	VDDQ	174	DQ60
21	CKE0	52	BA1	83	DQ56	113	NC	144	CB7	175	DQ61
22	VDDQ	53	DQ32	84	DQ57	114	DQ20	145	VSS	176	VSS
23	DQ16	54	VDDQ	85	VDD	115	A12	146	DQ36	177	DM7
24	DQ17	55	DQ33	86	DQS7	116	VSS	147	DQ37	178	DQ62
25	DQS2	56	DQS4	87	DQ58	117	DQ21	148	VDD	179	DQ63
26	VSS	57	DQ34	88	DQ59	118	A11	149	DM4	180	VDDQ
27	A9	58	VSS	89	VSS	119	DM2	150	DQ38	181	SA0
28	DQ18	59	BA0	90	DU	120	VDD	151	DQ39	182	SA1
29	A7	60	DQ35	91	SDA	121	DQ22	152	VSS	183	SA2
30	VDDQ	61	DQ40	92	SCL	122	A8	153	DQ44	184	VDDSPD
31	DQ19	62	VDDQ			123	DQ23	154	RAS*		

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK0-2 ~ CLK0*-2*	System clock	Differential clock, active on both edges for DDR sampling of all inputs.
S0* ~ S1*	Chip select, Active low	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE0 ~ 1	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address: RA0 ~ RA12, Column address: CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
RAS*	Row address strobe, Active low	Latches row addresses on the positive going edge of the CLK with RAS* low. Enables row access & precharge.
CAS*	Column address strobe, Active low	Latches column addresses on the positive going edge of the CLK with CAS* low. Enables column access.
WE*	Write enable, Active low	Enables write operation and row precharge. Latches data in starting from CAS*, WE* active.
DM0 ~ 8	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQS0 ~ 8	Data input/output strobe	Data Input/Output strobe.
DQ0 ~ 63	Data input/output	Data Inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Error check bits	
VDD/VDDQ/VSS/VREF	Power/ground	Power and ground for the input buffers and the core logic.
SDA	Serial data I/O	Data inputs/outputs line for serial EEPROM multiplexed on the same pins
SCL	Serial clock	Clock for serial EEPROM
SA0 ~ 2	Address in EEPROM	Address inputs for serial EEPROM

Petitioners
Ex. 1008, p. 18



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD and VDDQ supply relative to Vss	VDD, VDDQ	-1.0 ~ 3.6	V
Storage temperature	TSTG	-55 ~ +150	°C
Operating temperature	TSTO	0 ~ 60	
Power dissipation	PD	54	W
Short circuit current	IOS	50	mA

Note:

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK* inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK* inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note

1. VID is the magnitude of the difference between the input level on CK and the input on CK*.

2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and track variations in the DC level of the same.

3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
The AC and DC input specifications are reference to a Vref envelope that has been bandwidth limited 20MHz.

Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12, BA0 ~ BA1, RAS*, CAS*, WE*)	CIN1	60	96	pF
Input capacitance (CKE0, CKE1)	CIN2	33	51	pF
Input capacitance (S0*, S1*)	CIN3	33	51	pF
Input capacitance (CLK0, CLK0*)	CIN4	15	20	pF
Input capacitance (DM0 ~ DM8)	CIN5	12	14	pF
Data input/output capacitance (DQS0 ~ DQS8)	COUT1	20	24	pF
Data input/output capacitance (DQ0 ~ DQ63)	COUT2	12	14	pF
Data input/output capacitance (CB0 ~ CB7)	COUT3	12	14	pF

DC OPERATING CONDITIONS AND CHARACTERISTICS

Parameter	Symbol	Min		Max		Unit	Note
		D27J	D32K	D27J	D32K		
Supply Voltage	VDD	2.3	2.5	2.7	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.5	2.7	2.7	V	
I/O Reference Voltage	VREF	0.49*VDD		0.51*VDD		V	1
I/O Termination voltage(system)	VTT	VREF-0.04		VREF+0.04		V	2
Input high voltage	VIH	VREF + 0.15		VDDQ + 0.3		V	
Input low voltage	VIL	-0.3		VREF - 0.15		V	
Input Voltage level, CK and CK* inputs	VIN	-0.3		VDDQ + 0.3		V	
Input Differential Voltage, CK and CK* inputs	VID	0.36		VDDQ + 0.6		V	3
Input leakage current	ILI	-2		2		uA	
Output leakage current	IOZ	-5		5		uA	
Output High Current (Normal strength driver) V OUT = V TT + 0.84V	IOH	-16.8				mA	
Output High Current (Normal strength driver) V OUT = V TT - 0.84V	IOL	16.8				mA	
Output High Current (Half strength driver) V OUT = V TT + 0.45V	IOH	-9				mA	
Output High Current (Half strength driver) V OUT = V TT - 0.45V	IOL	9				mA	

Recommended operating conditions (Voltage referenced to VSS = 0V, TA = 0 to 70 C)

Notes:

- 1.VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on VREF may not exceed +/-2% of the dc value.
2. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. VID is the magnitude of the difference between the input level on CK and the input level on CK*.

DDR SDRAM SPEC Items and Test Conditions

Recommended operating conditions Unless Otherwise Noted, TA=0 to 70°C)

Conditions	Symbol
Operating current - One bank Active Precharge; tRC=tRCmin; tCK=6ns for DDR333, 5ns for DDR400; DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	IDD0
Operating current - One bank operation ; One bank open, BL=4, Reads - Refer to the following page for detailed test condition	IDD1
Percharge power-down standby current; All banks idle; power - down mode; CKE = <VIL(max); tCK=6ns for DDR333, 5ns for DDR400; Vin = Vref for DQ,DQS and DM	IDD2P
Precharge Floating standby current; CS# >= VIH(min);All banks idle; CKE >= VIH(min tCK=6ns for DDR333, 4ns for DDR400; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ,DQS and DM	IDD2F
Precharge Quiet standby current; CS# >= VIH(min); All banks idle; CKE >= VIH(min); tCK=6ns for DDR333, 5ns for DDR400; Address and other control inputs stable with keeping >= VIH(min) or <=VIL(max); Vin = Vref for DQ ,DQS and DM	IDD2Q
Active power - down standby current ; One bank active; power-down mode; CKE=< VIL (max); tCK=6ns for DDR333, 4ns for DDR400; Vin = Vref for DQ,DQS and DM	IDD3P
Active standby current; CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; tCK=6ns for DDR333, 5ns for DDR400; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N
Operating current - burst read; Burst length = 2; reads; continuous burst; One bank active; address and control inputs changing once per clock cycle; CL=2.5 at tCK = 6ns for DDR333, CL=3 at tCK = 5ns for DDR400; 50% of data changing at every burst; Iout = 0 m A	IDD4R
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL=2 at CL=2.5 at tCK = 6ns for DDR333, CL=3 at tCK = 5ns for DDR400; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	IDD4W
Auto refresh current; tRC = tRFC(min) - 12*tCK for DDR333 at 166Mhz, 14*tCK for DDR400at 200Mhz; distributed refresh	IDD5
Self refresh current; CKE =< 0.2V; External clock should be on; tCK = 166Mhz for DDR333, 200Mhz for DDR400	IDD6
Operating current - Four bank operation ; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	IDD7A

DDR SDRAM module IDD spec table

Symbol	Typical D27J	Typical D32K	Unit	Notes
IDD0	2990	3620	mA	
IDD1	3350	4070	mA	
IDD2P	488	524	mA	
IDD2F	1280	1460	mA	
IDD2Q	1100	1280	mA	
IDD3P	1640	2360	mA	
IDD3N	2360	3080	mA	
IDD4R	3890	5060	mA	
IDD4W	4250	5150	mA	
IDD5	4430	4970	mA	
IDD6	Normal	488	mA	
	Low Power	434	mA	Optional
IDD7A	6050	7310	mA	

* Module IDD was calculated on the basis of component IDD, and assuming one row of the module is in Active standby mode.

AC Timing Parameters & Specifications

		D27J (DDR333)		D32K(DDR400A)			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
Row cycle time	tRC	60		55		ns	
Refresh row cycle time	tRFC	72		70		ns	
Row active time	tRAS	42	70K	40	70K	ns	
RAS to CAS delay	tRCD	18		15		ns	
Row precharge time	tRP	18		15		ns	
Row active to Row active delay	tRRD	12		10		ns	
Write recovery time	tWR	15		15		ns	
Internal write to Read command	tWTR	1		2		tCk	
Clock cycle time	CL=3.0	tCK	-	5	10	ns	
	CL=2.5		6.0	12	6	12	ns
	CL=2		7.5	12	-	-	
Clock high level width	tCH	0.45	0.55	0.45	0.55	tCK	
Clock low level width	tCL	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/CK*	tDQSK	-0.60	+0.60	-0.55	+0.55	ns	
Output data access time from CK/CK*	tAC	-0.70	+0.70	-0.65	+0.65	ns	
Data strobe edge to output data edge	tDQSQ	-	+0.45	-	+0.40	ns	12
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read Postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in	tDQSS	0.75	1.25	0.72	1.28	tCK	
DQS-In setup time	tWPRES	0		0		ns	
DQS-In hold time	tWPREH	0.25		0.25		tCK	3
DQS falling edge to CK rising-setup time	tDSS	0.2		0.2		tCK	
DQS falling edge from CK rising-hold time	tDSH	0.2		0.2		tCK	
DQS-In high level width	tDQSH	0.35		0.35		tCK	
DQS-In low level width	tDQSL	0.35		0.35		tCK	
DQS-In cycle time	tDSC	0.9	1.1	-	-	tCK	
Address and Control Input setup time (fast)	tIS	0.75		0.6		ns	57
Address and Control Input hold time (fast)	tIH	0.75		0.6		ns	5,7
Address and Control Input setup time (slow)	tIS	0.8		-		ns	
Address and Control Input hold time (slow)	tIH	0.8		-		ns	
Data-out high impedance time from CK/CK*	tHZ	-0.70	+0.70	-	tAC max	ps	1
Data-out low impedance time from CK/CK*	tLZ	-0.70	+0.70	tAC min	tAC max	ps	1
Input Slew Rate(for input only pins)	tSL(I)	0.5		-	-	V/ns	
Input Slew Rate(for I/O pins)	tSL(IO)	0.5		-	-	V/ns	
Output Slew Rate(x4)	tSL(O)	1.0	4.5	-	-	V/ns	
Output Slew Rate Matching Ratio(rise to fall)	tSLMR	0.67	1.5	-	-		

AC Timing Parameters & Specifications(Continued)

		D27J (DDR333)		D32K(DDR400A)			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
Mode register set cycle time	tMRD	12		2		tCK	
DQ & DM setup time to DQS	tDS	0.45		0.4	-	ns	J,k
DQ & DM hold time to DQS	tDH	0.45		0.4	-	ns	J,k
Control & Address input pulse width	tIPW	2.2		2.2	-	ns	8
DQ & DM input pulse width	tDIPW	1.75		1.75		ns	8
Exit self refresh to Non read command	tXSNR	75		75		ns	
Exit self refresh to read command	tXSRD	200		200		tCK	
Refresh interval time	tREFI		7.8		7.8	us	4
Output DQS valid window	tQH	tHPmin -tQHS	-	tHP -tQHS	-	ns	11
Clock half period	tHP	tCLmin or tCHmin	-	min tCH/tCL		ns	10,11
Data hold skew factor	tQHS		0.55		0.5	ns	11
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	tCK	2
Active to Read with Auto precharge command	tRAP	18		-	-		
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) +(tRP/tCK)		-	-	tCK	13

Component Notes

1. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. these parameters are not referenced to a specific voltage level but specify when the device output in no longer driving (HZ), or begins driving (LZ).
2. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
3. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previously in progress on the bus, DQS will be transitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
4. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
5. For command/address input slew rate tY 1.0 V/ns
6. For command/address input slew rate tY 0.5 V/ns and < 1.0 V/ns
7. For CK & CK slew rate tY 1.0 V/ns
8. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
9. Slew Rate is measured between VOH(ac) and VOL(ac).
10. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
11. tQH = tHP - tQHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
12. tDQSQ
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
13. tDAL = (tWR/tCK) + (tRP/tCK)
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR266B at CL=2.5 and tCK=7.5ns tDAL = (15 ns / 7.5 ns) + (20 ns / 7.5ns) = (2) + (3)
tDAL = 5 clocks

Serial Presence Detect

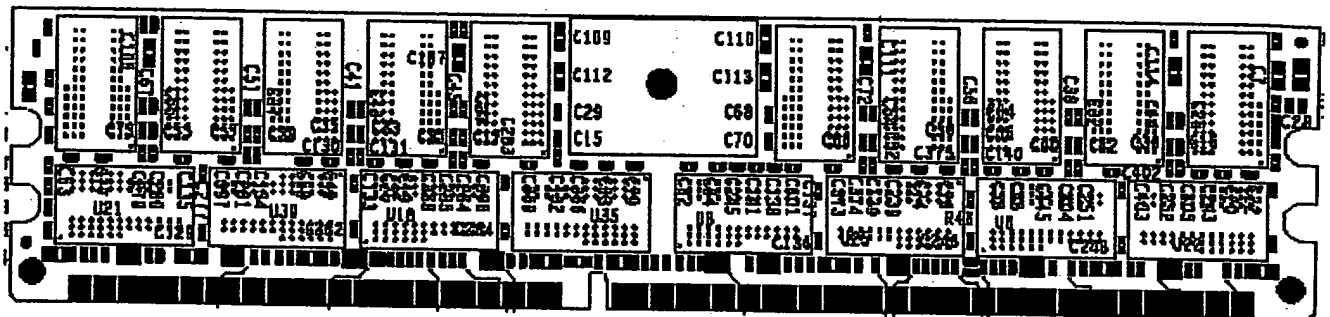
Byte	Description	Hex Value		Function	
		D27J	D32K	D27J	D32K
0	Number of bytes used	80h	80h	128Byte	
1	Total SPD memory size	08h	08h	256Byte	
2	Memory type	07h	07h	SDRAM DDR	
3	Number of row address bits	0Dh	0Dh	13	
4	Number of column address bits	08h	08h	11	
5	Number of banks (module rows)	02h	02h	2 Rows	
6	Module data width (LSB)	48h	48h	72bits	
7	Module data width (MSB)	00h	00h		
8	Module interface signal levels	04h	04h	SSTL 2.5V	
9	DDR SDRAM cycle time for highest CL	60h	50h	6ns	5ns
10	DDR SDRAM access time from clock for highest CL	70h	65h	0.7ns +/-	0.65ns +/-
11	Module configuration type	02h	02h	ECC	
12	Refresh rate/type	82h	82h	7.8us & Self refresh	
13	Primary SDRAM width	08h	08h	X8	
14	Error checking SDRAM width	08h	08h	X8	
15	DDR SDRAM device attributes, min clock delay for back to back random column addresses (Tccd)	01h	01h	tCCD=1tCK	
16	SDRAM device attributes, burst lengths supported	0Eh	0Eh	2,4,8	
17	SDRAM device attributes, number of banks on SDRAM device	04h	04h	4 banks	
18	SDRAM device attributes, CAS latency	0Ch	18h	2, 2.5	2.5,3
19	SDRAM device attributes, CS latency	01h	01h	0 tCK	
20	SDRAM device attributes, WE latency	02h	02h	1 tCK	
21	SDRAM device attributes	24h	24h	Reg Add,CTR,DLL, PLL	
22	SDRAM device attributes, general	C0h	C0h	Fast/Concurrent AP	
23	SDRAM cycle time for second highest CL	75h	60h	7.5ns	6ns
24	SDRAM access time from clock for second highest CL	70h	70h	0.7ns +/-	
25	SDRAM cycle time for third highest CL	00h	00h		
26	SDRAM access time from clock for third highest CL	00h	00h		
27	Minimum row precharge time (Trp)	48h	3Ch	18ns	15ns
28	Minimum row active to row active delay (Trrd)	30h	28h	12ns	10ns
29	Minimum CAS to RAS delay (Trcd)	48h	3Ch	18 ns	15ns
30	Minimum RAS pulse width (Tras)	2Ah	28h	42ns	40ns
31	Module bank density	80h	80h	512MB	
32	Command & Address signal input set up time	80h	60h	0.8ns	0.6ns
33	Command & Address signal input hold time	80h	60h	0.8ns	0.6ns
34	Data signal input set up time	45h	40h	0.44ns	0.4ns
35	Data signal input hold time	45h	40h	0.45ns	0.4ns
36	Reserved	00h	00h		
37	Reserved	00h	00h		
38	Reserved	00h	00h		
39	Reserved	00h	00h		
40	Reserved	00h	00h		
41	Row cycle time (Trc)	3Ch	37h	60ns	55ns
42	Auto Refresh cycle time (Trfc)	48h	46h	72ns	70ns
43	Maximum SDRAM device cycle time (Tckmax)	30h	28h	12ns	10ns
44	DQS-DQ skew (Tdqsq)	2Dh	28h	0.45	0.4ns
45	SDRAM device data hold skew factor (Tqhs)	55h	50h	0.55	0.5ns
46	Reserved	00h	00h		

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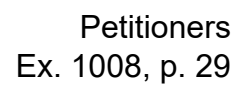
47	Reserved	00h	00h	
48	Reserved	00h	00h	
49	Reserved	00h	00h	
50	Reserved	00h	00h	
51	Reserved	00h	00h	
52	Reserved	00h	00h	
53	Reserved	00h	00h	
54	Reserved	00h	00h	
55	Reserved	00h	00h	
56	Reserved	00h	00h	
57	Reserved	00h	00h	
58	Reserved	00h	00h	
59	Reserved	00h	00h	
60	Reserved	00h	00h	
61	Reserved	00h	00h	
62	SPD revision	10h	10h	Revision 1.0
63	Check sum for byte 0 - 62	7Eh	D5h	7Eh D5h
64	Manufacturer's JEDEC ID code	7Fh	7Fh	Netlist Inc
65	Manufacturer's JEDEC ID code	7Fh	7Fh	Netlist Inc
66	Manufacturer's JEDEC ID code	7Fh	7Fh	Netlist Inc
67	Manufacturer's JEDEC ID code	16h	16h	Netlist Inc
68	Manufacturer's JEDEC ID code	00h	00h	
69	Manufacturer's JEDEC ID code	00h	00h	
70	Manufacturer's JEDEC ID code	00h	00h	
71	Manufacturer's JEDEC ID code	00h	00h	
72	Manufacturing location	00h	00h	
73	Manufacturer part number	4Eh	4Eh	N
74	Manufacturer part number	4Ch	4Ch	L
75	Manufacturer part number	39h	39h	9
76	Manufacturer part number	31h	31h	1
77	Manufacturer part number	32h	32h	2
78	Manufacturer part number	37h	37h	7
79	Manufacturer part number	4Ch	4Ch	L
80	Manufacturer part number	44h	44h	D
81	Manufacturer part number	36h	36h	6
82	Manufacturer part number	34h	34h	4
83	Manufacturer part number	30h	30h	0
84	Manufacturer part number	33h	33h	3
85	Manufacturer part number	32h	32h	2
86	Manufacturer part number	2Dh	2Dh	-
87	Manufacturer part number	44h	44h	D
88	Manufacturer part number	32h	33h	2 3
89	Manufacturer part number	37h	32h	7 2
90	Manufacturer part number	4Ah	4Bh	J K
91	Revision code	00h	00h	
92	Revision code	00h	00h	
93	Manufacturing date	00h	00h	
94	Manufacturing date	00h	00h	
95	Assembly serial number	00h	00h	
96	Assembly serial number	00h	00h	
97	Assembly serial number	00h	00h	
98	Assembly serial number	00h	00h	

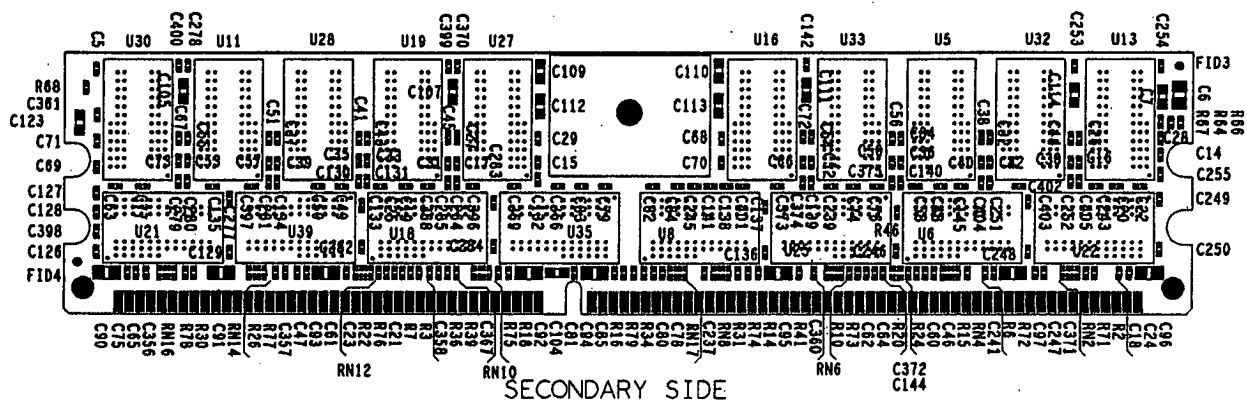
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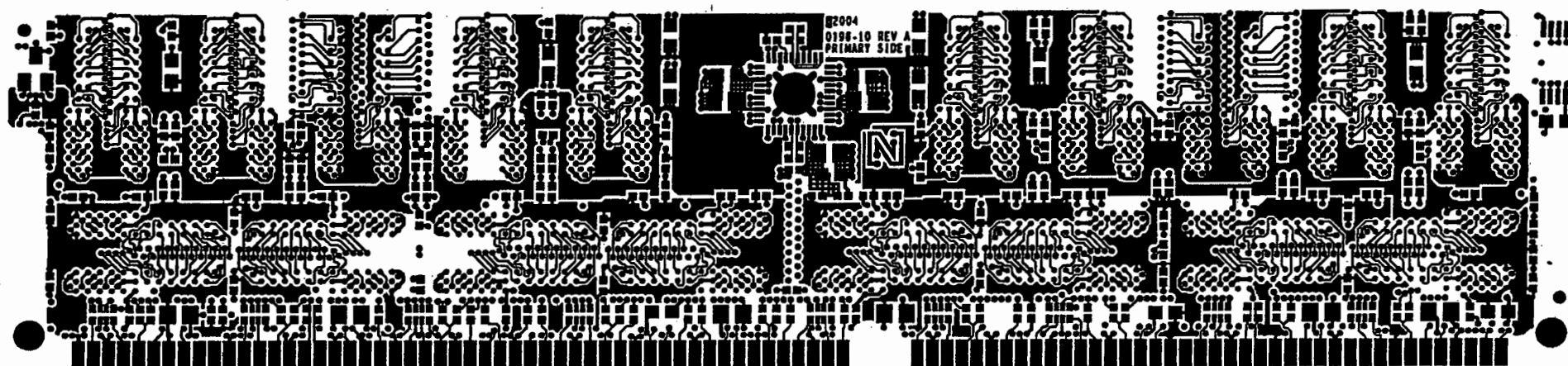
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125	Manufacturer specific data	00h	00h	
126	Specification for frequency	00h	00h	
127	Details	00h	00h	



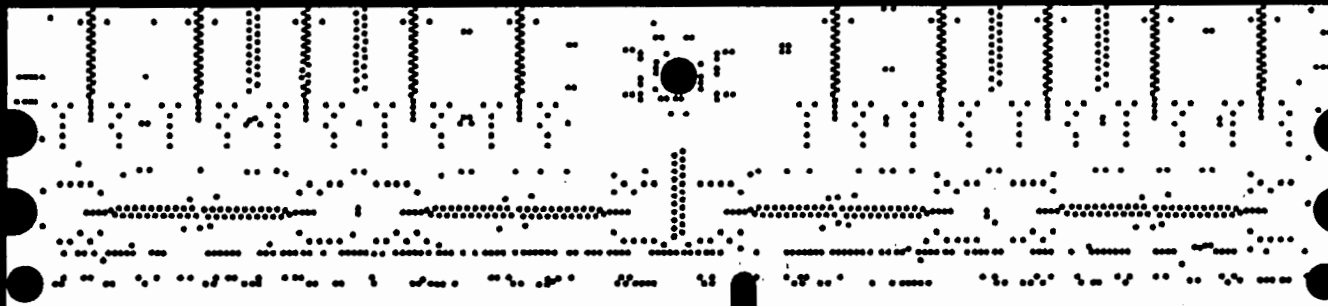




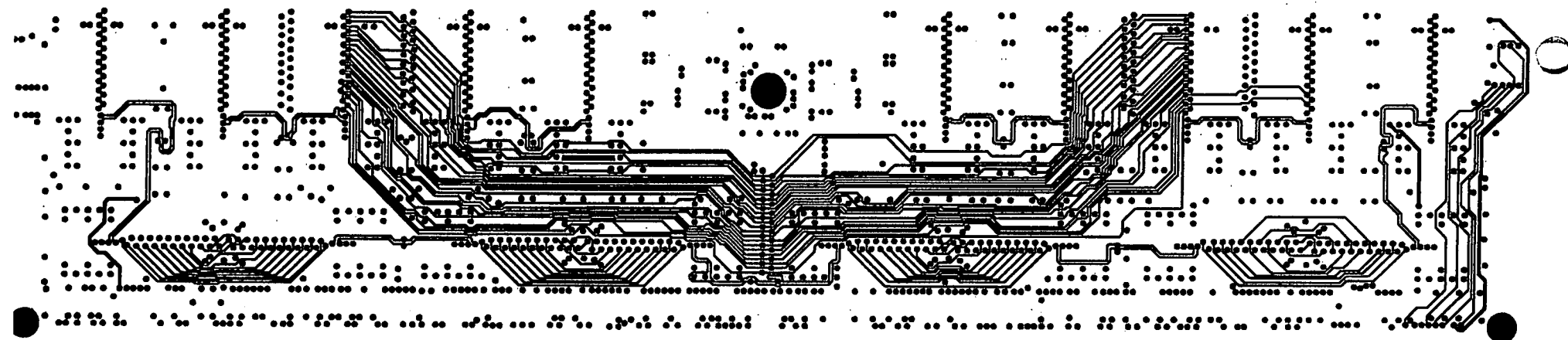




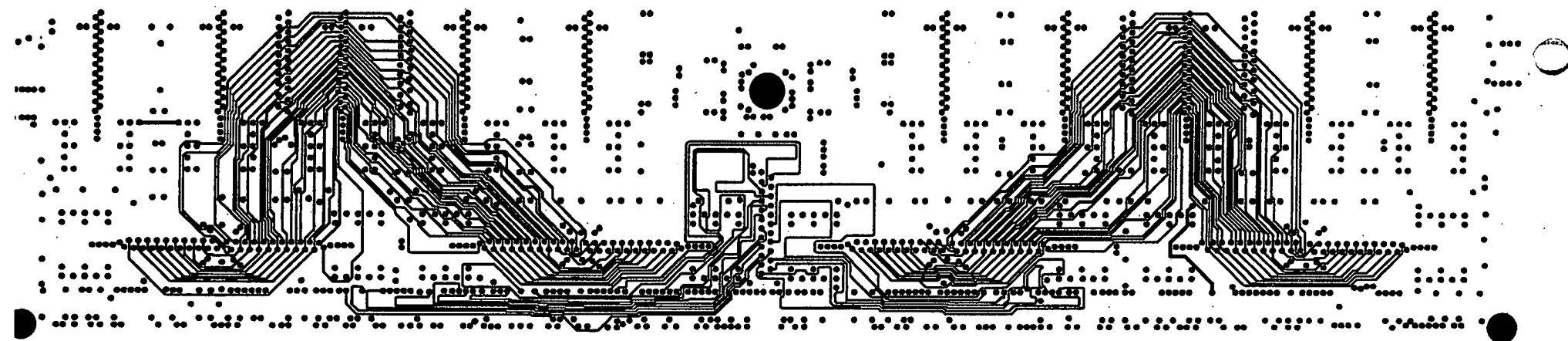
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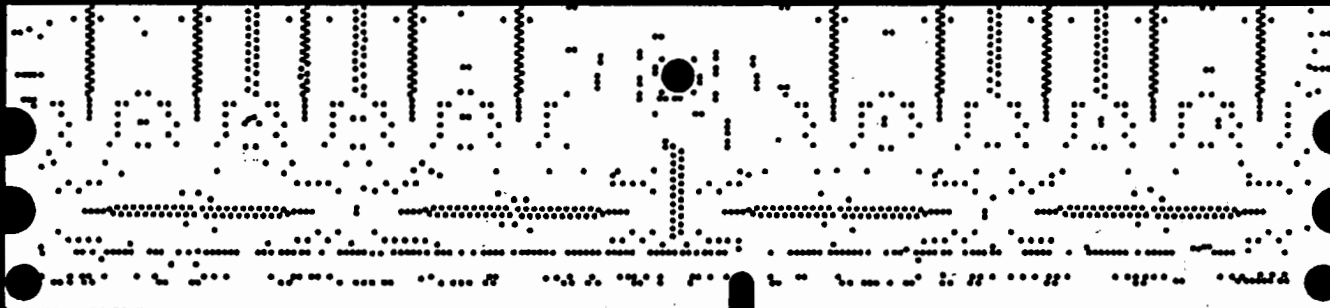
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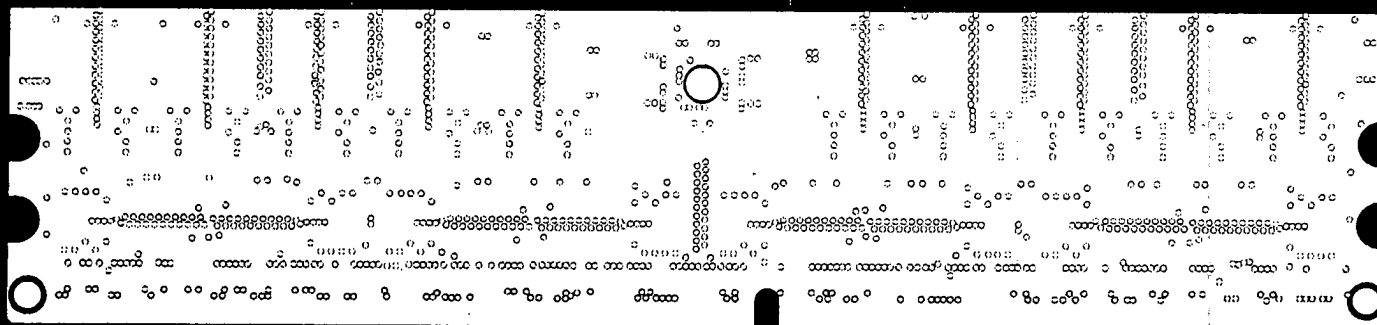
LAYER 8 MID 4



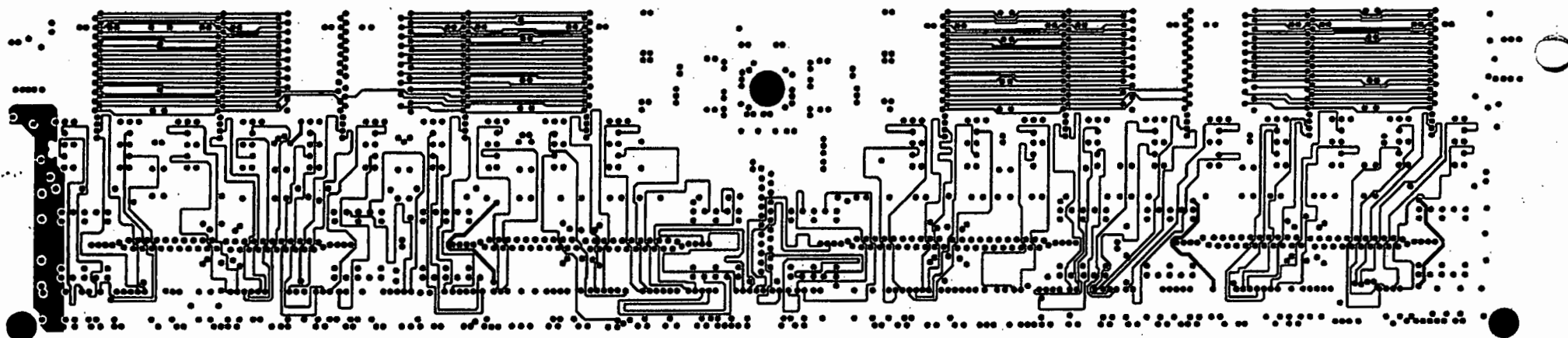
LAYER 7 MID 3



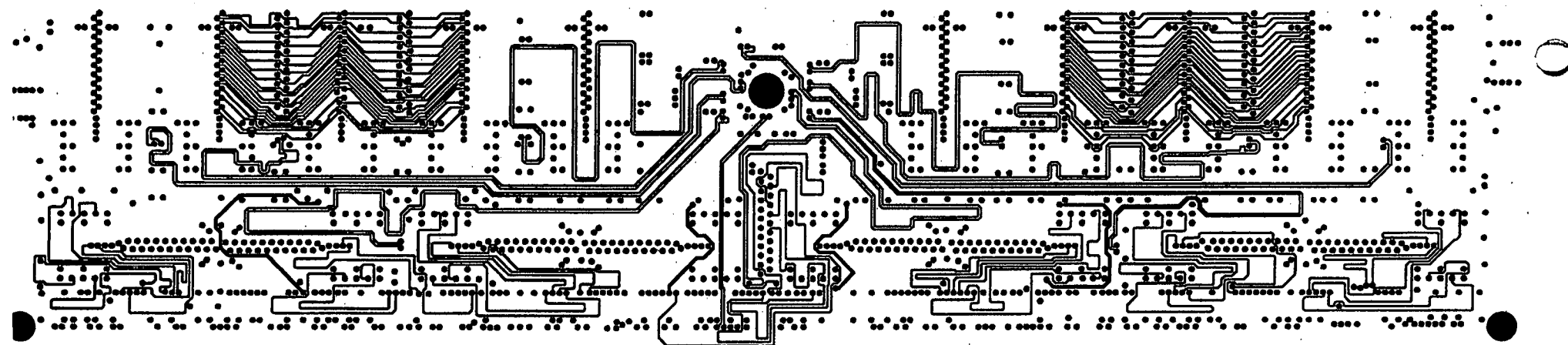
LAYER 6 VCC



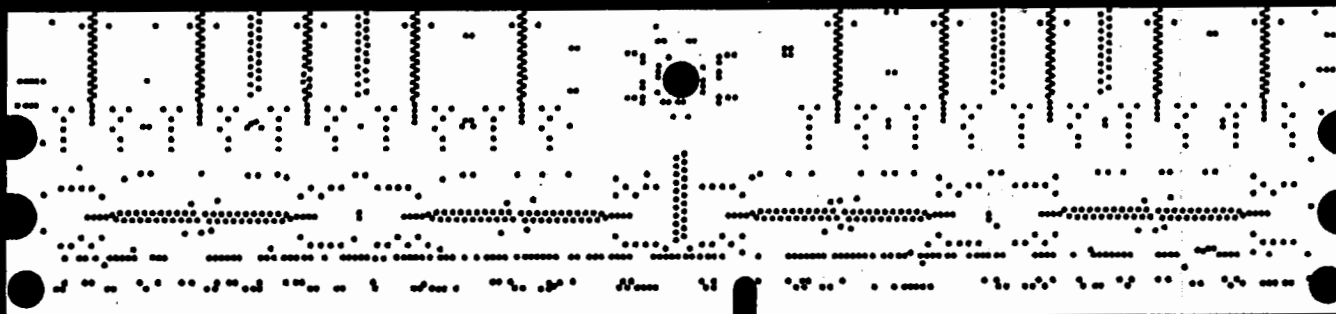
LAYER 5 GND



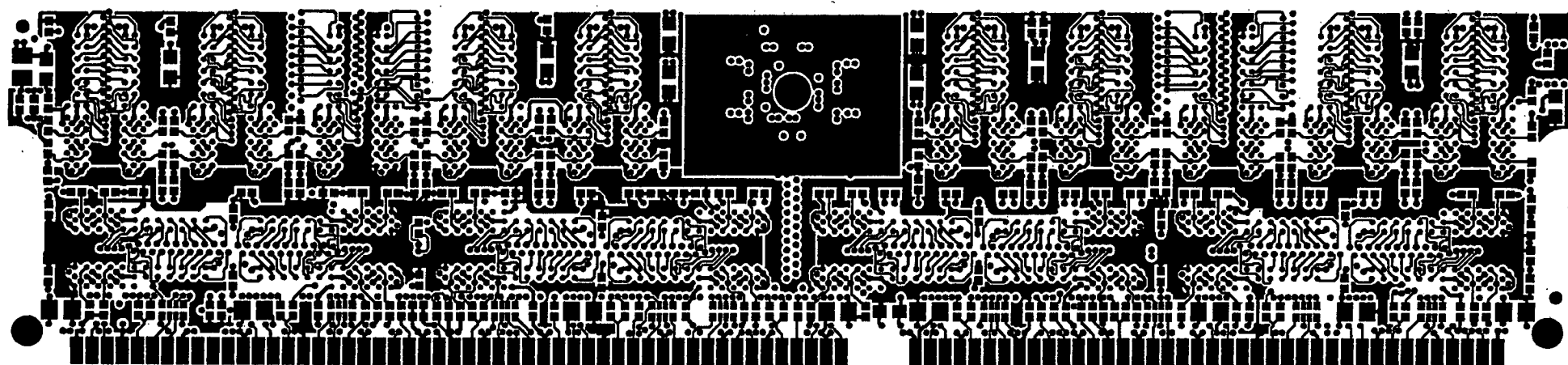
LAYER 4 MID 2



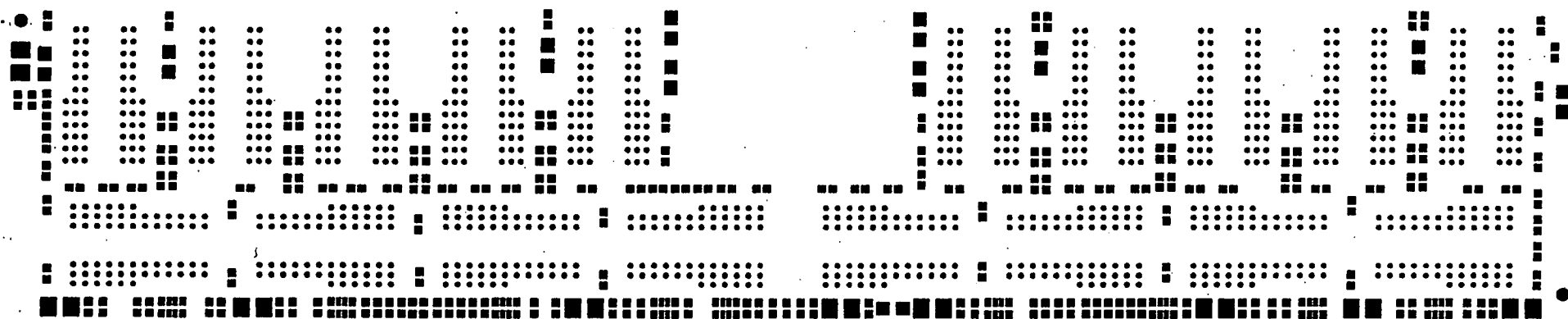
LAYER 3 MID 1



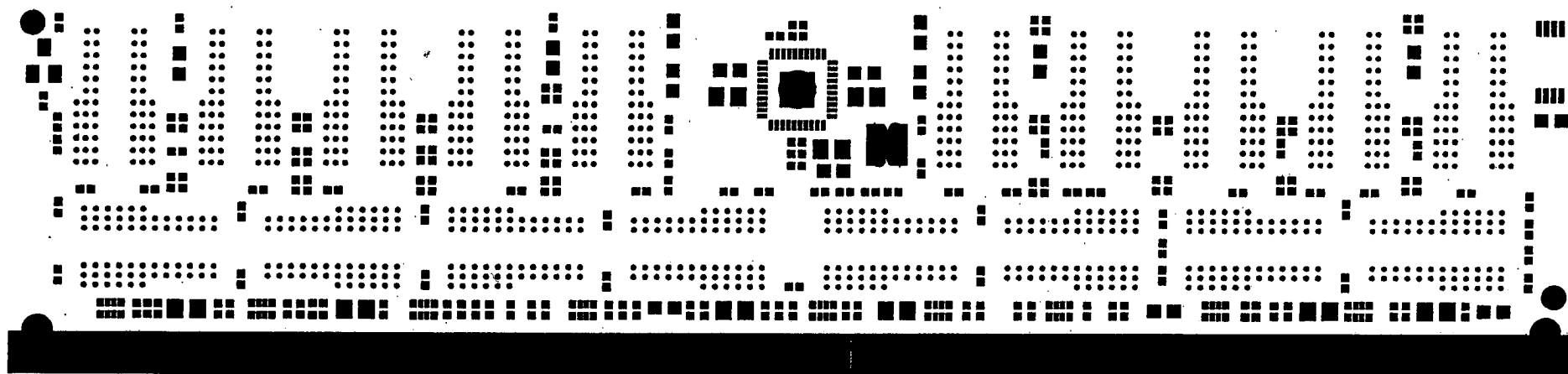
LAYER 2 VSS1



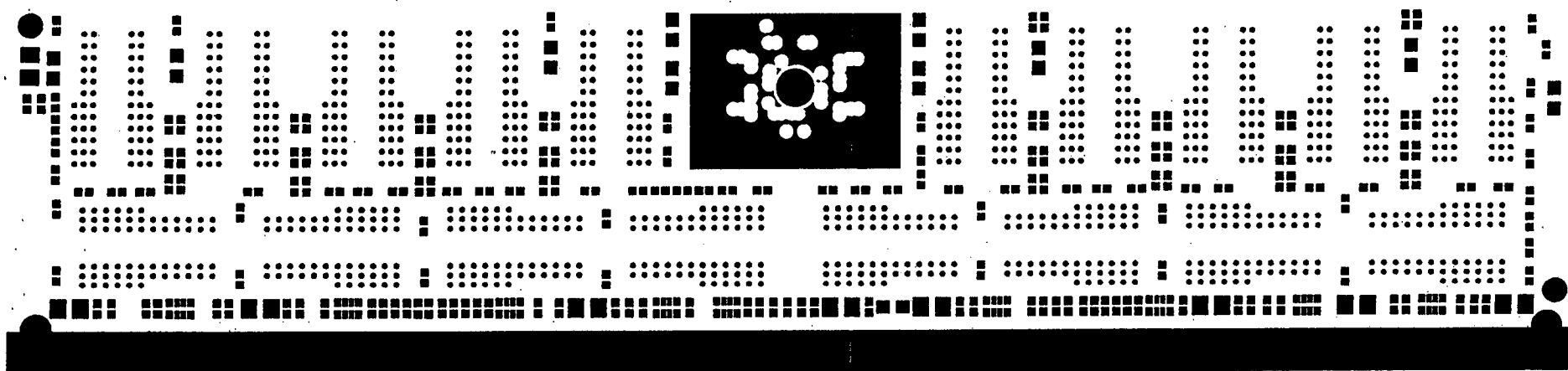
LAYER 10 - SECONDARY SIDE



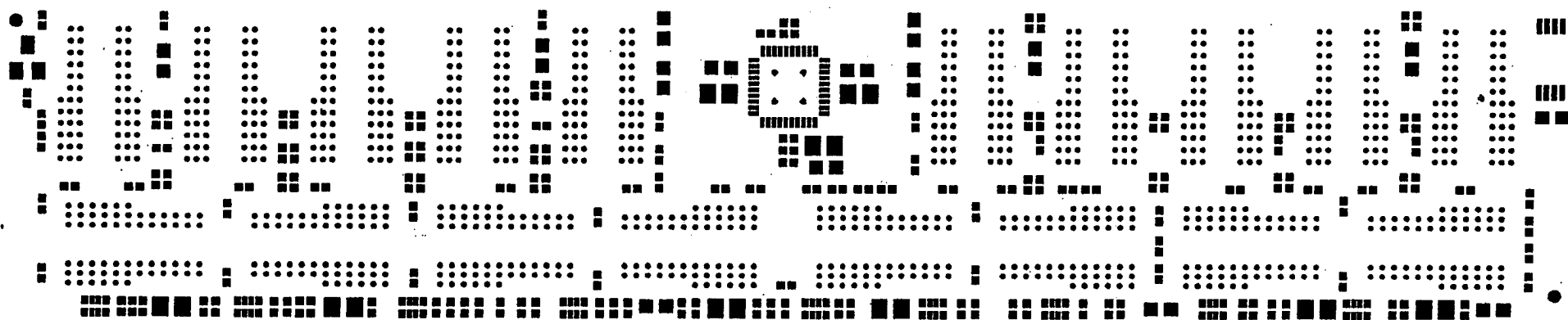
LAYER 14 SOLDERPASTE BOTTOM



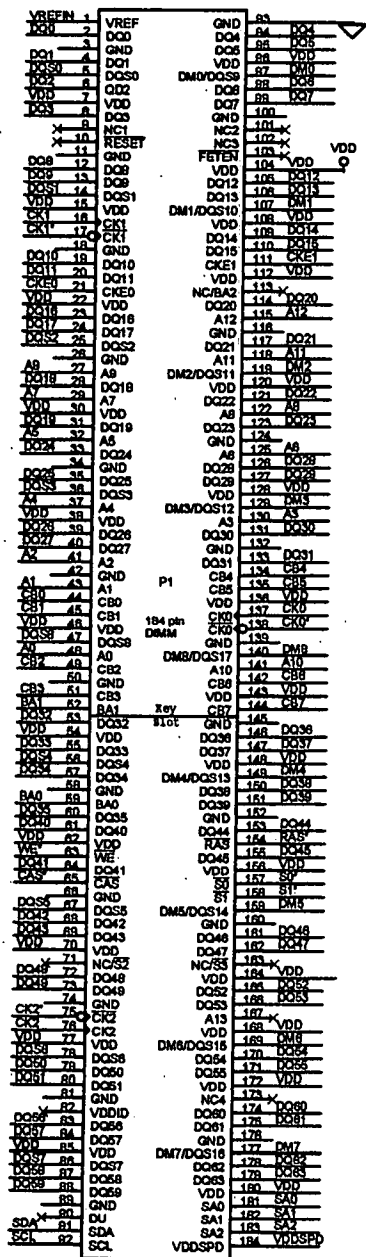
LAYER 11 SOLDERMASK TOP

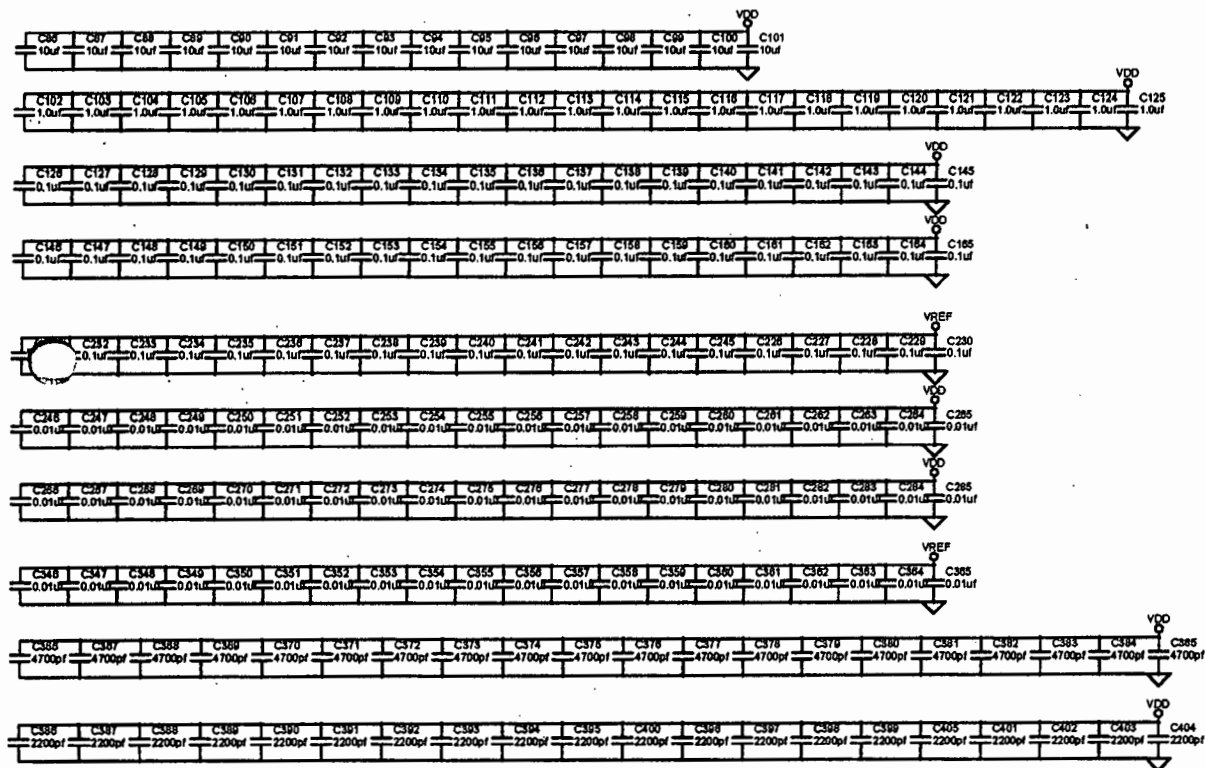


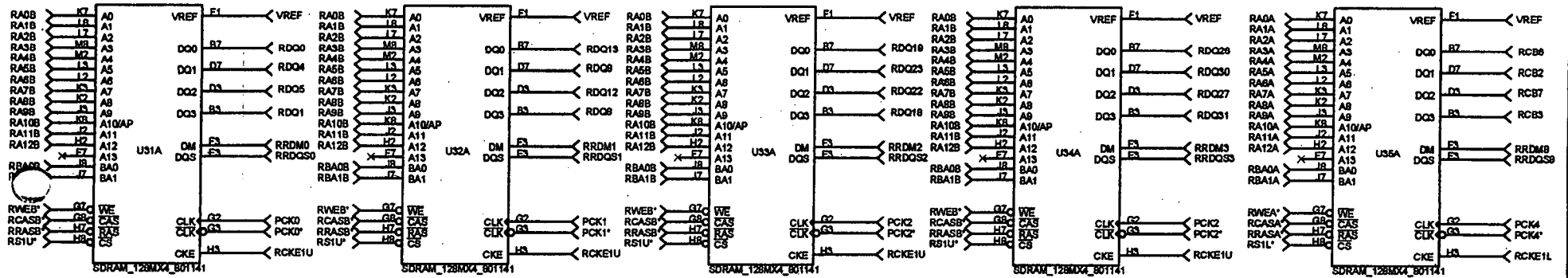
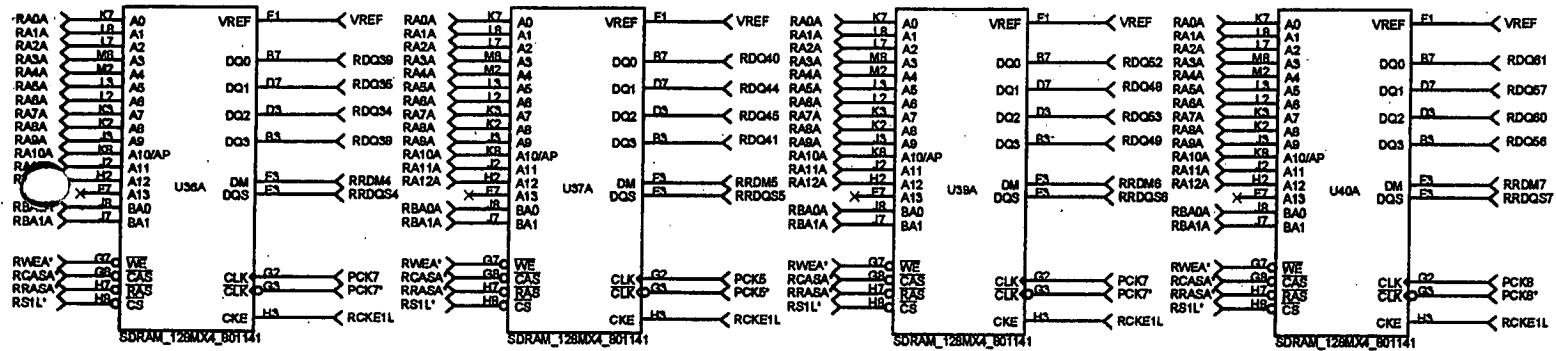
LAYER 12 SOLDERMASK BOTTOM



LAYER 13 SOLDERPASTE TOP

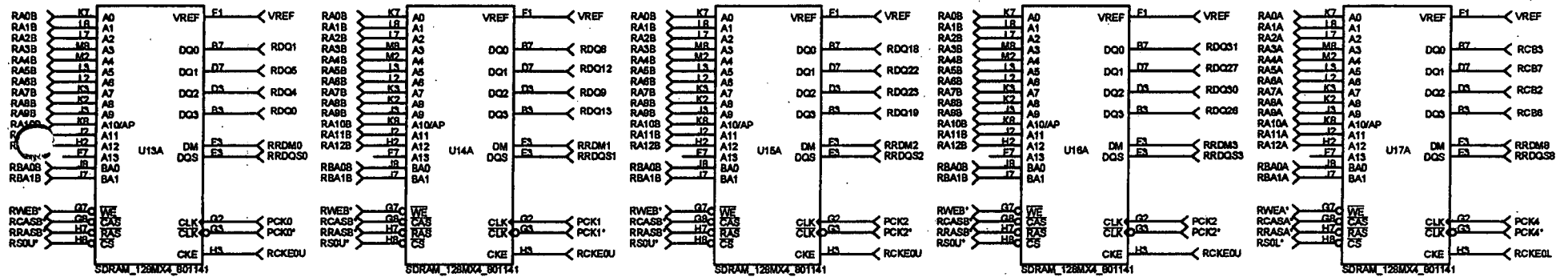
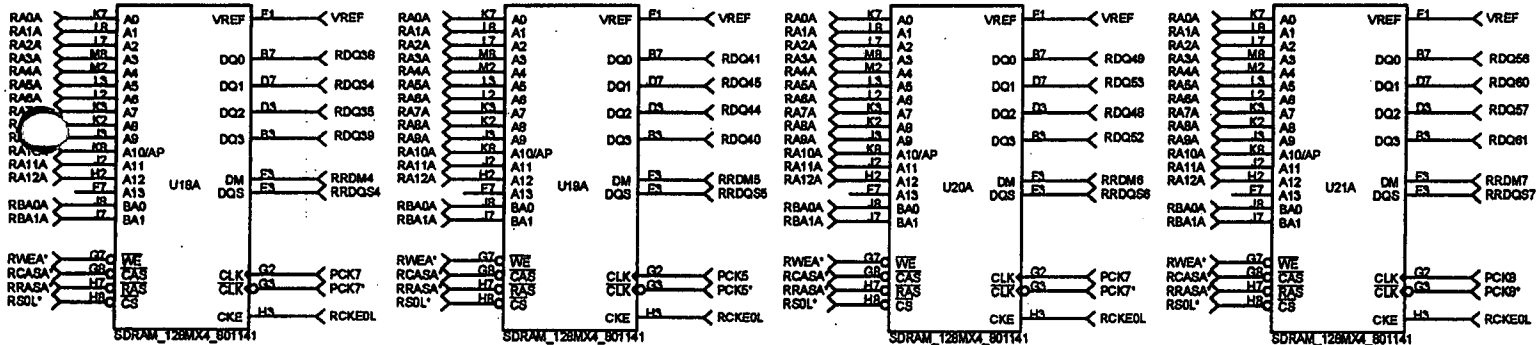






<Core Design> Place one 0.01uF and two 0.1uF caps per SDRAM.

VREF → VREF



<Cons Design>

VREF → VREF

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

06/03/2004 FFANAI2 00000034 60575595

01 FC:1005

160.00 DP

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