16367 U.S. PTO
072104

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

Case No. **NETL.028PR**
Date: July 21, 2004

13441 U.S. PTO
60/590038
072104

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Sir:

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR § 1.53(c).

For: **MEMORY MODULE WITH TIED DQS PINS**

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Enclosed are:

(X) Specification in six (6) pages.

(X) A check in the amount of $160 to cover the filing fee.

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The Commissioner is hereby authorized to charge any additional fees which may be required, now or in the future, or credit any overpayment to Account No. 11-1410.

Was this invention made by an agency of the United States Government or under a contract with an agency of the United States Government?

(X) No.

( ) Yes. The name of the U.S. Government agency and the Government contract number are:

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Attorney Docket No.	:	NETL.028PR
Applicants	:	William M. Gervasi et al.
For	:	MEMORY MODULE WITH TIED DQS PINS
Attorney	:	Bruce S. Itchkawitz
"Express Mail" Mailing Label No.	:	EV 307990886 US
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MEMORY MODULE WITH TIED DQS PINS

Summary of the Invention

[0001] In certain embodiments, a memory module uses two lower-density DDR2 synchronous dynamic random access memory ("SDRAM") integrated circuits with shared data strobe signal ("DQS") pins to simulate one higher-density DDR2 SDRAM integrated circuit.

[0002] In certain embodiments, a memory module comprises a plurality of pairs of lower-density memory components, each pair connected together with shared DQS pins to simulate a higher-density memory component. Each pair of memory components comprises a first memory component and a second memory component. The internal termination resistors of the second memory component are disabled by tying the On-Die Termination ("ODT") pin of the second memory component to ground. In certain such embodiments, the termination resistors for DQ pins of the second memory component are provided off-chip using discrete components. In certain other such embodiments, the termination resistors for DQ pins of the second memory component are provided off-chip using integrated circuit components.

Brief Description of the Drawings

[0003] Figure 1 schematically illustrates a configuration in which a DQS pin of a first memory component is connected to a DQS pin of a second memory component.

[0004] Figure 2 schematically illustrates a configuration in which a DQS pin of a first memory component is connected to a DQS pin of a second memory component with the ODT of the DQS pin of the second memory component tied to ground.

Detailed Description of the Preferred Embodiment

[0005] Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory components wherein each component has a 64Mb x 8 organization. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory components. Alternatively, it can be economically advantageous to be able to fabricate the 1-GB memory module using lower-density memory components and doubling the number of components required to produce the

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desired word width. For example, by fabricating the 1-GB memory module using thirty-six 256-Mb memory components with 64Mb x 4 organization, the cost of the resulting 1-GB memory module can be reduced since the unit cost of 256-Mb memory components is typically lower than one-half the unit cost of 512-Mb memory components. The cost savings can be significant, even though twice as many 256-Mb memory components are used in place of the 512-Mb memory components.

[0006] For proper operation, the computer system advantagously recognizes the 1-GB memory module comprising 256-Mb memory components with 64Mb x 4 organization as having 512-Mb memory components with 64Mb x 8 organization of the same depth. This advantagous result would desirably be achieved by connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory components. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. However, a general guideline of memory module design warns against connecting two output signal pins together in this way.

[0007] Figure 1 schematically illustrates the problem arising from tying together two DQS signal pins of two memory components. Figure 1 schematically illustrates a configuration in which a DQS pin 12 of a first memory component 10 is connected to a DQS pin 14 of a second memory component 20. The two DQS pins 12, 14 are both connected to a controller (not shown). The DQ (data input/output) pin 22 of the first memory component 10 and the corresponding DQ pin 24 of the second memory component 20 are each connected to the memory controller by the DQ bus (not shown). Typically, each memory component will have a plurality of DQ pins (e.g., eight DQ pins per memory component), but for simplicity, Figure 1 only shows one DQ pin for each memory component.

[0008] Figure 1 also schematically illustrates an on-die termination or "ODT" configuration which utilizes termination resistors internal to the memory components to provide signal termination. Each memory component 10, 20 has a corresponding ODT pin 62, 64 which is connected to the memory controller. The ODT pin 62 of the first memory component 10 provides a signal which can disable the internal termination resistors 52, 56 of the first memory component 10. The ODT pin 64 of the second memory component 20 provides a signal which can disable the internal termination resistors 54, 58 of the second

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memory component 20. Certain memory components, including but not limited to DDR2 memory components, are configured to selectively disable the ODT of the memory component in this way. For example, the termination resistors of a memory component can be enabled when the ODT pin of the memory component is pulled high (schematically shown as a closed switch by a dash-dot line in Figure 1) and can be disabled when the ODT pin of the memory component is grounded (schematically shown as an open switch by a solid line in Figure 1). By selectively disabling the termination resistors of an active memory component, while leaving the termination resistors of inactive memory components enabled, such configurations advantageously preserve signal strength on the active memory component while continuing to eliminate signal reflections at the bus-die interface of the inactive memory components.

[0009] In certain embodiments, the DQS pins 12, 14 of each memory component 10, 20 are selectively connected to ground through a corresponding termination resistor 52, 54 internal to the corresponding memory component 10, 20. Similarly, in other embodiments, the DQ pins 22, 24 are selectively connected to ground through a corresponding termination resistor 56, 58 internal to the corresponding memory component 10, 20. In certain embodiments, rather than being connected to ground, the DQ pins 12, 14 or the DQS pins 22, 24 are selectively connected to VTT through the corresponding termination resistors 52, 54, 56, 58. The resistances of the internal termination resistors 52, 54, 56, 58 are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the embodiment schematically illustrated by Figure 1, each internal termination resistor 52, 54, 56, 58 has a resistance of approximately 75 ohms.

[0010] When connecting the first memory component 10 and the second memory component 20 together to form a double word width, both the first memory component 10 and the second memory component 20 are active at the same time. Connecting the first memory component 10 and the second memory component 20 as shown in Figure 1 results in an effective termination resistance for the DQS pins 12, 14 of one-half the desired ODT resistance to reduce signal reflections since the internal termination resistors 52, 54 of the two memory components 10, 20 are connected in parallel. For 75-ohm internal termination resistors, the effective termination resistance for DQS pins 12, 14 is then 37.5 ohms. This

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reduction in the termination resistance can result in signal reflections causing the memory component to malfunction.

[0011] Figure 2 schematically illustrates an embodiment which avoids connecting the internal termination resistances of the DQS pins 12, 14 in parallel. As described above in relation to Figure 1, Figure 2 only shows one DQ pin for each memory component for simplicity. The ODT pin 64 of the second memory component 20 is tied (e.g., directly hard-wired) to ground, thereby disabling the internal termination resistors 54, 58 on the DQS pin 14 and DQ pin 24, respectively, of the second memory component 20 (schematically shown as open switches in Figure 2). The termination resistance for both DQS pin 12 and DQS pin 14 is provided by the termination resistor 52 internal to the first memory component 10. In addition, the ODT pin 62 provides a signal which selectively disables the termination resistance for both the first memory component 10 and the second memory component 20 when these memory components are active.

[0012] The termination resistor 56 of the DQ pin 22 of the first memory component 10 is enabled or disabled by signals to the ODT pin 62 of the first memory component 10. The termination resistance of the DQ pin 24 of the second memory component 20 is enabled or disabled by signals to an ODT circuit 70 which is external to the second memory component 20. In certain embodiments, the termination resistance and the ODT circuit 70 for the second memory component 20 are provided by discrete components. In certain other embodiments, the termination resistance and the ODT circuit 70 for the second memory component 20 are provided by integrated circuit components.

[0013] Certain embodiments advantageously allow the use of lower cost readily available 512-Mb DDR2 SDRAM components to replace more expensive 1-Gb DDR2 SDRAM components. Certain embodiments advantageously reduce the total cost of the resultant memory module.

[0014] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

FIGURE 1:

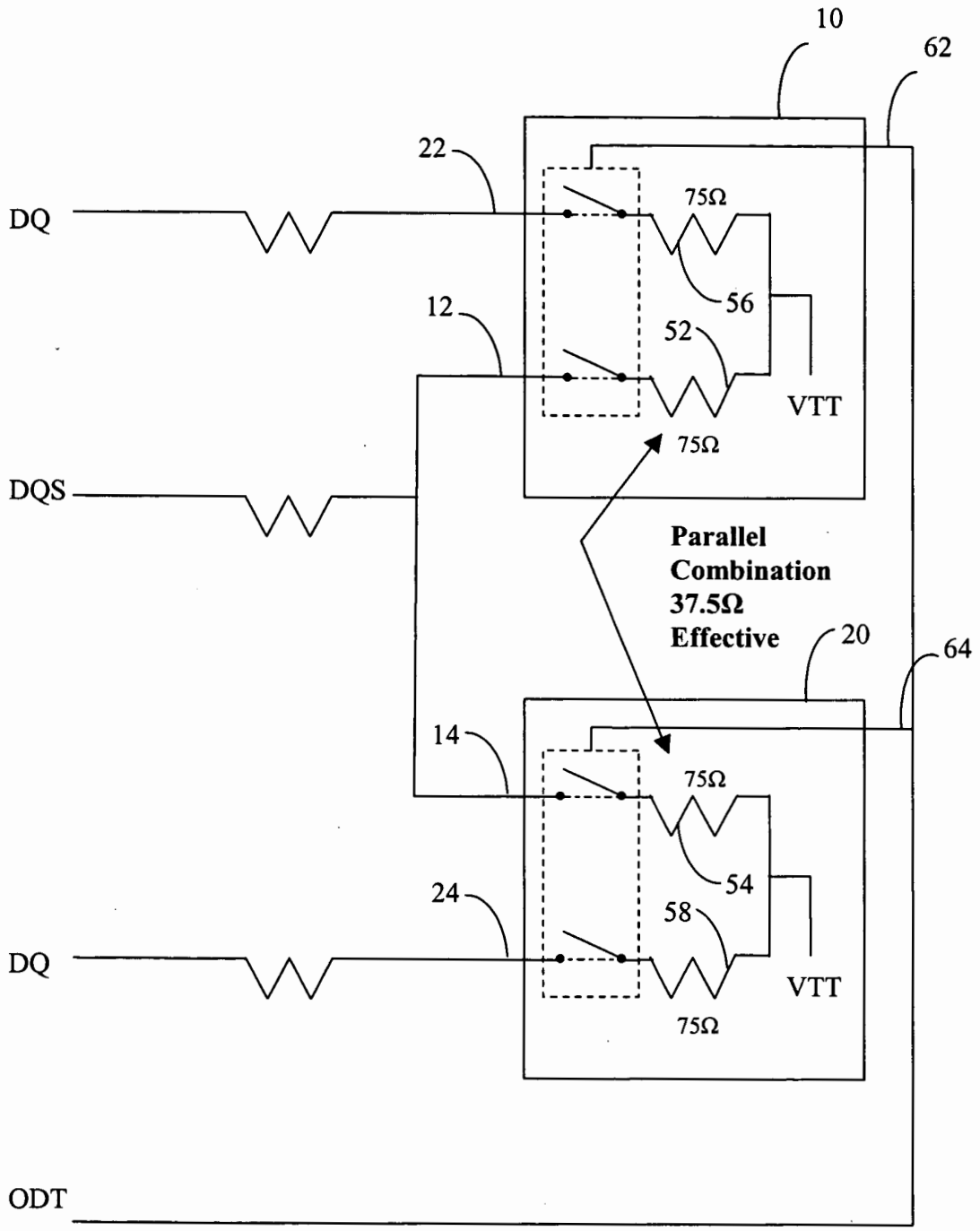

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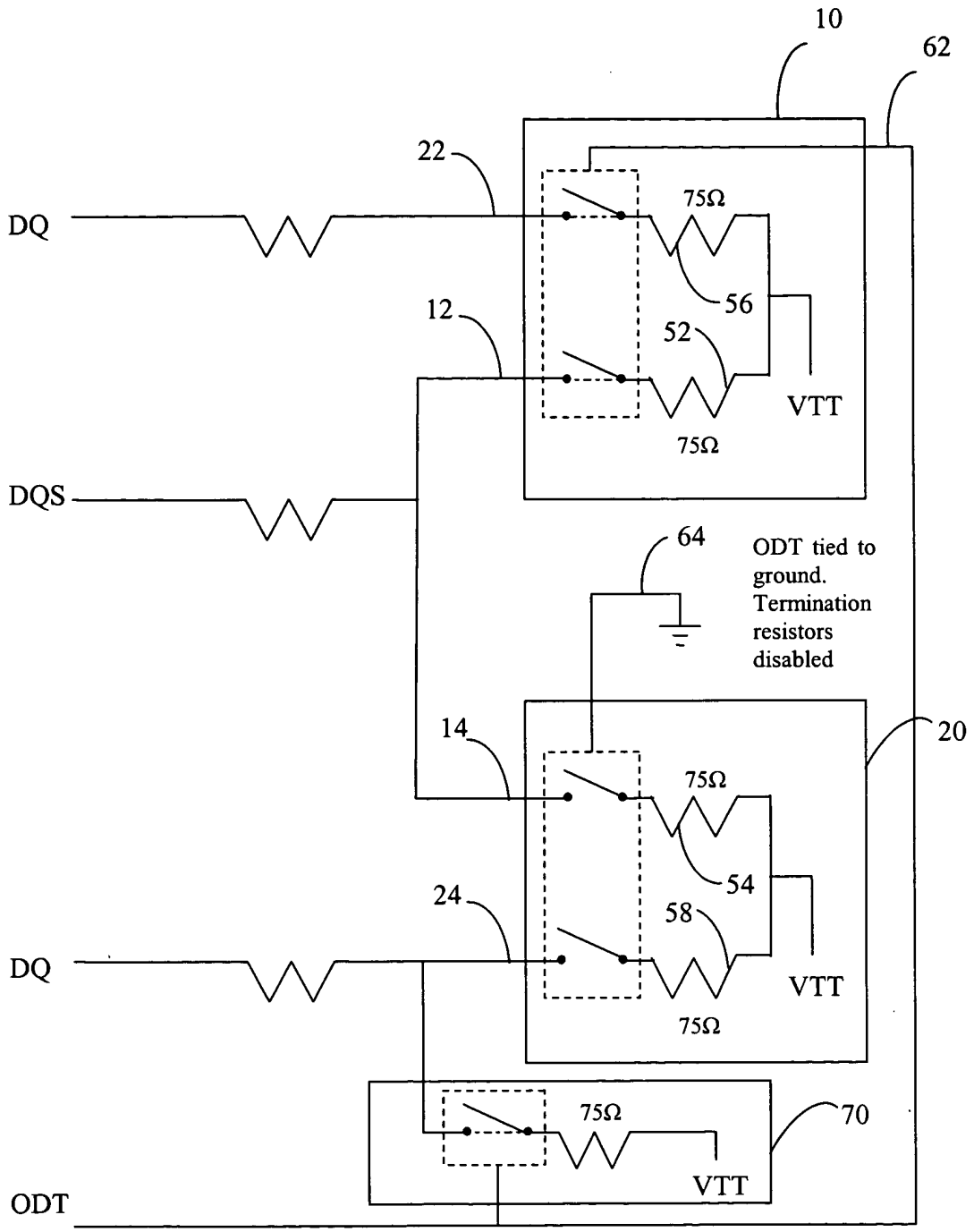
FIGURE 2:



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PATENT APPLICATION SERIAL NO. _____

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PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033