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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,579	10/21/2010	7619912	19473-0099RX1	3547

25224 7590 06/06/2016
MORRISON & FOERSTER, LLP
707 Wilshire Boulevard
LOS ANGELES, CA 90017

EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

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06/06/2016	PAPER

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/001,339	06/08/2010	7619912	043326-000-0021	5035

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

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PEIKARI, BEHZAD

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES (WWH), INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

Appeal 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/001,579
Patent 7,619,912 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and JEREMY J. CURCURI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION ON APPEAL

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STATEMENT OF THE CASE

Requesters 1–3 made three separate requests for *inter partes* reexamination of U.S. Patent No. 7,619,912 B2 ("the '912 patent") issued to Jayesh R. Bhakta and Jeffrey C. Solomon, entitled *Memory Module Decoder*. The '912 patent issued November 17, 2009 and is assigned to Patent Owner, Netlist Inc. Requestor 1 requested reexamination of claims 1–51 of the '912 patent, which was assigned Control No. 95/001,339; Requester 2 requested reexamination of claims 1, 3, 4, 6–11, 15, 18–22, 24, 25, 27–29, 31–34, 36–39, 41–45, and 50 of the '912 patent, which was assigned Control No. 95/000,578; Requester 3 also requested reexamination of the same claims of the '912 patent as Requester 2, which was assigned Control No. 95/000,579. R1 Request 6; R2 Request 1; R3 Request 1.[1] On February 28, 2011, Control Nos. 95/001,339, 95/000,578 and 95/000,579 were merged into a single proceeding. Dec. *Sua Sponte* to Merge Reexamination Proc. 6.

Although indicating claims 1–136[2] are subject to reexamination in the RAN, the Examiner further states claims 44, 51, 55, 59, 64–66, 72–74, 76, 94–108, and

[1] Throughout this opinion, we refer to (1) the Appeal Briefs filed by Requester 1, Requester 2, Requester 3, and Owner as R1 App. Br., R2 App. Br., R3 App. Br., and PO App. Br. respectively; (2) the Respondent Briefs filed by Owner (for Requesters 1–3), Requester 1, Requester 2, and Requester 3 as PO-R1 Resp. Br., PO-R2 Resp. Br., PO-R3 Resp. Br., R1 Resp. Br., R2 Resp. Br., and R3 Resp. Br. respectively ; (3) the Rebuttal Briefs by Requester 1, Requester 2, Requester 3, and Owner as R1 Reb. Br., R2 Reb. Br., R3 Reb. Br., and PO Reb. Br.; (4) the Examiner's Answer (Ans.) mailed January 14, 2015; (5) the Examiner's Right of Appeal (RAN) mailed June 18, 2014, (6) the Action Closing Prosecution (ACP) mailed March 21, 2014, and (7) Requests for Reexaminations by Requester 1, Requester 2, and Requester 3 as R1 Request, R2 Request, and R3 Request respectively.

[2] Claims 52-136 were added during the course of reexamination. *See* RAN 4.

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112–118 have been canceled. RAN 1. Accordingly, claims 1–43, 45–50, 52–54, 56–58, 60–63, 67–71, 75, 77–93, 109–111, and 119–136 remain pending. Of those claims, claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57, and 119 have been rejected and claims 1, 3, 4, 6, 8, 10–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 are indicated as patentable. *Id.*

Requesters 1–3 appeal from the decision in the RAN not to adopt various rejections. R1 App. Br.; R2 App. Br.; R3 App. Br. Patent Owner filed respondent briefs. PO-R1 Resp. Br.; PO-R2 Resp. Br.; PO-R3 Resp. Br. Each Requester filed a rebuttal brief to their respective appeals. R1 Reb. Br.; R2 Reb. Br.; R3 Reb. Br.

Owner cross appeals from the decision in the RAN, rejecting claims 2, 5, 7, 21, 23, 26, 30, 33, and 119 of the '912 patent. PO App. Br. 2. Owner states that rejected claims 9 and 57 are not being appealed. PO App. Br. 47. Requesters 1–3 filed respondent briefs, and Owner filed a rebuttal brief. *See generally* R1 Resp. Br., R2 Resp. Br., R3 Resp. Br., and PO Reb. Br; *see also* Ans. 2.

The Examiner's Answer relies on the RAN, incorporating it by reference. *See* Ans. 1.

An oral hearing was conducted on November 24, 2015. A transcript has been made of record.

We have been informed that the '912 patent relates to (1) U.S. Patent Nos. 7,289,386, 7,532,537, 7,636,274, and 7,864,627 (the '386, '537, '274, and '627 patents, respectively), (2) merged reexamination Control Nos. 95/000,546 and 95/000,577 for the '386 patent, which was appealed to the Board as Appeal No. 2014-007777, and where the rejection of pending claims was affirmed on February

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25, 2015,[3] (3) reexamination Control No. 95/001,381 for the '537 patent, which was appealed to the Board as Appeal No. 2013-009066 and where the Examiner's decision to confirm the patentability of the claims was affirmed on January 16, 2014,[4] (4) reexamination Control No. 95/001,337 for the '274 patent, which has been reopened based on the Board decision dated January 16, 2014 (Appeal No. 2013-009044),[5] (5) reexamination Control No. 95/001,758 for the '627 patent, which was appealed to the Board as Appeal No. 2015-007761 and was heard on December 11, 2015, (6) various AIA proceedings, including IPR2014-00882, IPR2014-00883, and IPR 2014-01011,[6] and (7) several court proceedings.[7] R1 App. Br. 1; R2 App. Br. 2, 18; R3 App. Br. 1, 65; PO App. Br. 1.

We have jurisdiction under 35 U.S.C. §§ 134(b) and 315 (2002).

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[3] Subsequent to the decision, Patent Owner and Requester 3, Google Inc., filed notices of appeal to the Federal Circuit on October 26, 2015 and October 30, 2015, respectively. On February 15, 2016, the appeal was dismissed. *Netlist, Inc. v. Google Inc.*, Nos. 16-1270 and 16-1271, slip op. at 1 (Fed. Cir. January 28, 2016).
[4] Subsequently, Requester appealed the Board decision to the Federal Circuit, which affirmed the Board's decision on November 13, 2015. *Inphi Corp. v. Netlist, Inc.*, 805 F.3d 1350 (Fed. Cir. 2015).
[5] On January 16, 2014, the Board affirmed-in-part and presented new grounds of rejection for various claims. The proceeding has been remanded to the Central Reexamination Unit.
[6] *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00882, Paper No. 33 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 7,881,150 B2), *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00883, Paper No 33 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 8,081,536 B1), and *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-01011, Paper No. 34 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 7,881,150 B2).
[7] *Netlist, Inc. v. Inphi Corp.,* Case No. 2:09-cv-6900 (C.D. Cal.), *Netlist, Inc. v. Google, Inc.,* Case No. 4:09-cv-05718 (N.D. Cal.), and *Google, Inc. v. Netlist, Inc.*, Case No. 4:08-cv-04144 (N.D. Cal.), all stayed due to the reexamination proceedings of the '912, '537, and '274 patents.

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We affirm-in-part the Examiner's decision to reject or not to reject claims 1–43, 45–50, 52–54, 56–58, 60–63, 67–71, 75, 77–93, 109–111, and 119–136.

Illustrative claims 7 and 21 read as follows with emphasis added:

7. [The memory module of claim l] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals,
and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register, *wherein the bank address signals of the set of input control signals are received by both the logic element and the register*.

Copied from 95000579 on 02/08/2017

Petitioners
Ex. 1016, p. 8

21. [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register, *wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.*

PO App. Br. 51–54, Claims App'x.[8]

[8] Underlining in claims indicates added language present in originally issued independent claims 1 and 15 respectively.

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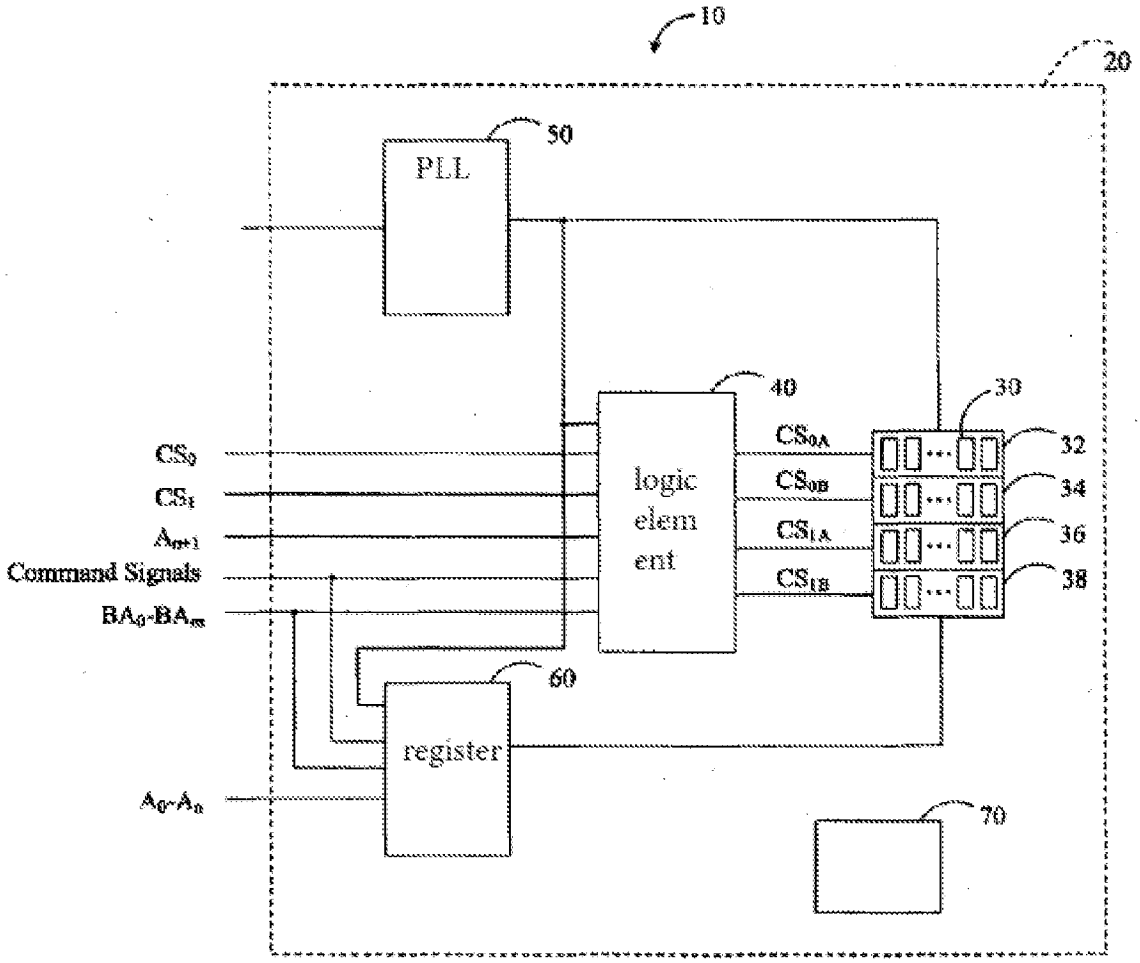
Petitioners
Ex. 1016, p. 9

The Invention

The '912 patent illustrates an exemplary memory module 10 in Figure 1A below:



Annotated Memory Module illustrated in Figure 1A

The '912 patent 3:32–34, 5:6–8; Fig. 1. Memory module 10 contains printed circuit board 20. Memory devices 30, phase lock loop (PLL) 50, logic element 40, and register 60 are coupled to printed circuit board 20. The '912 patent 5:13–14, 22–27; Fig. 1A.

Memory devices 30 are a first number of memory devices (e.g., 4 DDR devices). The '912 patent 5:11–12, 6:12–16; Fig. 1A. The logic element 40

Copied from 95000579 on 02/08/2017

receives input control signals that correspond to a second number of memory devices smaller than the first number of memory devices (e.g., 2). The '912 patent 2:37–39, 5:14–20; Fig. 1A. Input control signals includes address signals, such as bank address signals (e.g., BA_0-BA_m), row address signals, column address signals, gated column address strobe signal, and rank or chip-select signals (e.g., CS_0 and CS_1), and command signals (e.g., refresh and precharge). The '912 patent 2:37–39, 6:56–61; Fig. 1A. Logic element 40 generates output control signals (e.g., CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}) in response to the input control signals, the output control signals corresponding to the first number of memory devices (e.g., 4). The '912 patent 5:18–21; Fig. 1A.

Additionally, in certain embodiments, the output control signals correspond to a first number of ranks (e.g., 4) in which the memory devices 30 are arranged. The '912 patent 6:55–67, 7:36–38. On the other hand, the input control signals correspond to a second number of ranks (e.g., 2) per memory module, for which the computer system is configured. The '912 patent 6:67–7:9, 7:20–29, 38–39; Fig. 1A. The second number of ranks is smaller than the first number of ranks. *See id*. In such a scenario, memory module 10 simulates a virtual memory module, and this may occur when the number of memory devices 30 of memory module 10 is larger than the number of memory devices 30 per memory module the computer system is configured to use. The '912 patent 7:9–19. This arrangement can improve memory module performance, capacity, or both. The '912 patent 1:21–24.

As shown above in Figure 1A, the bank address signals, $BA_0 - BA_m$, are received by both register 60 and logic element 40.

Copied from 95000579 on 02/08/2017

In addition, Figure 2B shows that logic element 40 can save or latch an input control signal (e.g., A_{13}) during a row access procedure (e.g., column access strobe (CAS) high) at program logic device (PLD) 42 and can transmit this signal as an output control signal during a subsequent column access procedure (e.g., CAS low). The '912 patent 21:54–66; Fig. 2A. Figure 2B illustrates this below:

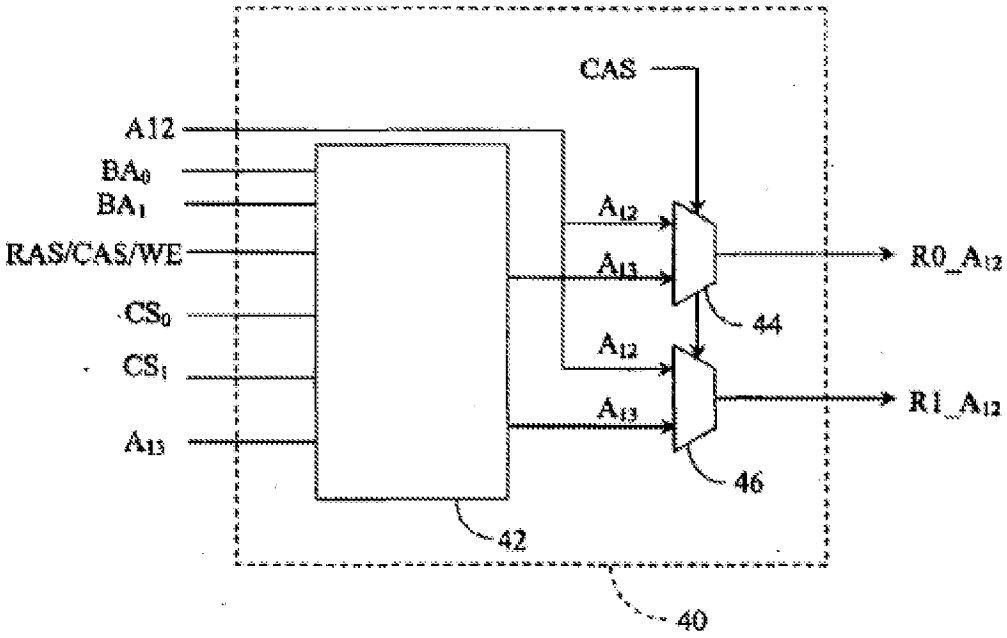


Figure 2B showing Logic Element 40 with PLD 42 Storing Signals

The '912 patent 3:44–45; Fig. 2B. In this exemplary logic element, ranks 32 and 34 (shown in Figure 2A) interpret the previously-saved row address (e.g., A_{13}) as a current column address (e.g., A_{12}), and logic element 40 translates the extra row address into an extra column address. The '912 patent 21:66–22:4; Fig. 2A–B.

Cited Prior Art

The Examiner relies on the following as evidence of unpatentability:

Connolly	US 5,745,914	Apr. 28, 1998
Dell (Dell 1)	US 5,926,827	July 20, 1999
Dell (Dell 2)	US 6,209,074	Mar. 27, 2001

Copied from 95000579 on 02/08/2017

Olarig	US 6,260,127 B1	July 10, 2001
Wong	US 6,414,868 B1	July 2, 2002
Dell (Dell 184)	US 6,446,184 B2	Sept. 3, 2002
Amidi	US 2006/0117152	June 1, 2006 (filed Jan. 5, 2004)

Miles J. Murdocca and Vincent P. Heuring, Principles of Computer Architecture (Chapter 7) 243–252 (2000) (Murdocca)

Micron, *DDR SDRAM RDIMM, MT36VDDF12872 - 1GB, MT36VDDF25672 - 2GB* 1–20 (2002) (Micron)

JEDEC Standard No. 21-C, *PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Rev. 1.3* pages 4.20.4-1–4.20.4-82 (Jan. 2002) (JEDEC 21-C)

JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification JESD79C (Rev. of JESD79B) 1–75 (Mar. 2003) (JEDEC 79C)

JEDEC STANDARD, Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications, JESD82-4B (Rev. of JESD82-4A) 1–12 (May 2003) (JEDEC 82-4B)[9]

HP Printer Memory Explained 1–7 (Jan. 21, 2004), *available at* http://warshaft.com/hpmem.htm (Memory Explained)

The following Declarations are presented in this merged proceeding:

Declaration of Dr. Carl Sechen dated July 5, 2011 (Sechen Decl.),

Declaration of Dr. Carl Sechen dated January 13, 2013 (2d Sechen Decl.),

Declaration of Dr. David Wang dated August 29, 2011 (Wang Decl.),

Declaration of Dr. David Wang dated February 13, 2012 (2d Wang Decl.),

Declaration of Dr. David Wang dated February 13, 2013 (3d Wang Decl.),

[9] Notably, JEDEC 21-C, JEDEC 79C, and JEDEC 82-4B are often referred to collectively as JEDEC or JEDEC standards in the presented rejections, the briefs, and declarations. *See, e.g.*, Sechen Decl. ¶ 8.

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Petitioners
Ex. 1016, p. 13

Declaration of Dr. Nader Bagherzadeh dated August 25, 2011 (Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 10, 2012 (2d Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 13, 2013 (3d Bagherzadeh Decl.),

Declaration of Dr. Christoforos Kozyrakis dated October 21, 2010 (Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated August 28, 2011 (2d Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated February 23, 2012 (3d Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated February 13, 2013 (4th Kozyrakis Decl.), and

Declaration of Dr. Bruce Jacob dated October 19, 2010.

Adopted Rejections

Patent Owner appeals the following rejections adopted by the Examiner:

Reference(s)	Basis	Claims	RAN
Amidi (Ground 3[10])	§ 102	2, 5, 7, 9, 21, 23, 30, 33, and 119	11, 22–26

[10] Throughout the documents in this proceeding, the Examiner, Patent Owner and Requesters 1–3 refer to the various rejections by ground number. *See, e.g.*, RAN 11. We include the ground number here and in the Opinion.

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Amidi (Ground 4)	§ 103(a)	2, 5, 7, 9, 21, 23, 30, 33, 57, and 119	12, 28
Amidi and Dell 2 (Ground 5)	§ 103(a)	2, 5, 7, 9, 21, 23, 26, 30, and 33	12, 30
Amidi and JEDEC (Ground 6)	§ 103(a)	7, 9, 21, 33, 57, and 119	12, 32–33
Dell 1 and JEDEC (Ground 9)	§ 103(a)	9 and 21	RAN 13, 36–39
Wong and JEDEC (Ground 11)	§ 103(a)	9 and 21	RAN 13, 41–43
Micron and Connolly (Ground 12)	§ 103(a)	7, 9, 21, 26, and 33	RAN 13, 44–47
Micron and Amidi (Ground 13)	§ 103(a)	7, 9, 21, 26, 33, and 57	RAN 14, 49–52
Micron, Amidi, and Dell 2 (Ground 19)	§ 103(a)	21	RAN 14, 55

PO App. Br. 11.

ISSUES ON APPEAL

We review the appealed rejections for error based upon the issues identified by Owner in its appeal brief, and in light of the arguments and evidence produced thereon. *Cf. Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential) (citing *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992)). "Any arguments or authorities not included in the brief[s] permitted under this section or [37 C.F.R.] §§ 41.68 and 41.71 will be refused consideration by the Board, unless good cause is shown." 37 C.F.R. § 41.67(c)(1)(vii).

Based on the arguments and evidence presented by Owner, the main issues on appeal are whether the Examiner erred in determining:

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(I) Amidi alone or in combination with at least one other reference (Grounds 3–6) disclose or teach:

(A) "the bank address signals of the set of input control signals are received by both the logic element and the register" recited in claim 7 and similarly recited in claims 26 and 33 (bank address limitation)?

(B) "wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure" recited in claim 21 and similarly recited in claims 2, 5, 23, and 30 (storing limitation)?

(II) Micron and Amidi (Ground 13) teach

(A) the bank address limitation recited in claim 7 and similarly recited in claims 26 and 33?

(B) the storing limitation recited in claim 21?

(III) the proposed rejections of certain claims should not be adopted?

ANALYSIS

Patent Owner's Appeal

Preliminary Matters

Patent Owner states it "is not appealing the rejections of claims 9 and 57." PO App. Br. 47; R3 Resp. Br. 1. These claims have been rejected under Grounds 3–6, 9, and 11–13. RAN 11–14. Because no arguments have been presented for these claims, we summarily sustain the rejections of these claims. *See Hyatt v. Dudas*, 551 F.3d 1307, 1314 (Fed. Cir. 2008) (explaining that when appellant fails to contest a ground of rejection, the Board may affirm the rejection without considering its substantive merits).

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Claim Construction

During examination of a patent application, a claim is given its broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations and internal quotation marks omitted). We presume that claim terms have their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) ("The ordinary and customary meaning 'is the meaning that the term would have to a person of ordinary skill in the art in question.'") (internal citations omitted). However, patentees may rebut this presumption by acting as their own lexicographer, providing a definition of the term in the specification with "reasonable clarity, deliberateness, and precision." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Claims 2, 5, 7, 21, 23, 26, 30, and 33 recite a circuit comprising "a logic element." The '912 patent states that logic element 40 in certain embodiments can be a PLD, an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, or a complex PLD (CPLD). The '912 patent 6:39–43. The '912 patent also describes the logic element in certain embodiments as "a custom device," "compris[ing] various discrete electrical elements," or being "one or more integrated circuits" in certain embodiments. The '912 patent 6:43–44, 48–52. As such, the '912 patent describes "a logic element" in expansive terms, but none of the above passages define or limit the meaning of "logic element" with sufficient precision.

Copied from 95000579 on 02/08/2017

The Examiner similarly determines the '912 patent has not defined "a logic element" and further finds this phrase is not a term of art. RAN 69. The Examiner thus construes the phrase "logic element" to have its plain meaning to include "an element that performs some kind of logic function or an element that comprises a logic circuit." *Id.* Requester 1 proposes that one skilled in the art would have understood a logic element "to mean any circuit that implements one or more logic functions using combinational or sequential logic functions. [*See* Declaration of David Wang, Ph.D., filed Aug. 29, 2011 ("1st Wang Decl.", attached as Exhibit B-1) at ¶¶ 7, 30]." R1 Resp. Br. 5. Requester 2 also proposes an interpretation of "logic element," urging that is "at least as broad" as Patent Owner proposed in litigation. R2 Request 22 (citing R2 Request, Evid. App., Ex. OTH-C 7). In that context, Patent Owner urged "a logic element" to mean a "hardware circuit that performs a predefined function on input signals and presents the resulting signal as its output." *Id.*

Given the record and that the '912 disclosure fails to define the term, we accept the Examiner's understanding of "a logic element" as reasonable, which includes "an element that performs some kind of logic function or an element that comprises a logic circuit." RAN 69. This understanding is consistent with the expansive discussion in the '912 patent that includes a "custom device" or a generic device comprising "various discrete electrical elements." The '912 patent 6:43–44, 48–50.

The Examiner also states "there is nothing in the claims or the specification that precludes the logic element from comprising a storage device such as a register." RAN 69. Notably, each of claims 2, 5, 7, 21, 23, 26, 30, and 33 recites "a register" separate from "a logic element." This distinction in claim language

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presumably supports that the recited "logic element" is something different from a register. Both the Examiner and Dr. Sechen also note they "are separate elements in the claims." RAN 69, 74; Sechen Decl. ¶ 20. Dr. Sechen further argues that one skilled in the art "would understand that the term 'logic element' implies something inherently different than the term 'register.'" Sechen Decl. ¶ 19.

We agree that the recited "logic element" is distinct element from the recited "register." RAN 69, 74. However, the expansive examples in the '912 patent of a logic element cover custom devices or a device of various discrete electrical components, which includes at least some types of registers. Requester 1 also provides the testimony of Dr. Wang, supporting that a register performs logical operations and is a logical element. R1 Resp. Br. 5 (citing Wang Decl. ¶ 7). That is, Dr. Wang testifies that "[r]egisters are logic elements," because they implement one or more logic functions (e.g., AND, NAND, OR, NOR, etc.). Wang Decl. ¶ 7. Also, even Dr. Sechen, Patent Owner's own expert, admits that a register includes "a small amount of control logic" (Sechen Decl. ¶ 19), indicating that registers perform some type of logic function or comprise a logic circuit.

Accordingly, we determine that a reasonably broad interpretation of "a logic element," in light of the '912 patent's disclosure and the testimony of what one of ordinary skill in the art would have understood, includes custom devices and devices with various discrete electrical components that implement logic operations, including registers. We further determine the recited "logic element" is also not limited to a single component, given that the disclosure states the logic element can comprise various discrete electrical components.

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I. Amidi

Patent Owner argues the Examiner erred in adopting the proposed rejections based on Amidi, separately arguing the claims in two groups — (1) claims with the bank address limitation (i.e., claims 7, 26, and 33) and (2) claims with the storing limitation (i.e., claims 2, 5, 21, 23, and 30). PO App. Br. 11. We in turn will address each group separately.

A. Claims 7, 26, and 33 (Claims with the Bank Address Limitation)

Patent Owner argues claims 7, 26, and 33 as a group. PO App. Br. 12–25. As addressed below, claim 26 is only rejected under 35 U.S.C. § 103 based on Amidi and Dell 2 (Ground 5) and we only address claim 26 for that rejection. To the extent these claims are argued together, we select claim 7 as representative. 37 C.F.R. § 41.67(c)(1)(vii).

Claim 7 recites, in pertinent part, that a "memory module comprising . . . a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising . . . bank address signals, . . . the bank address signals of the set of input control signals are received by both the logic element and the register."

1. Anticipation Rejection – Ground 3

The Examiner indicates that both Requester 1 and Requester 2 present a rejection under 35 U.S.C. § 102 based on Amidi for claims 7 and 33. RAN 11, 22, 24, 25; *see also* R1 February 13, 2012 Comments 6–12 and R2 Request 39, 943–961, 965–969, 1025–1026 (referring to Ex. CC–G). The Examiner adopted the proposed rejection of Requesters 1 and 2 for claims 7 and 33. RAN 11, 22–26.

Copied from 95000579 on 02/08/2017

Specifically, the Examiner maps register 418 in Amidi's Figure 4B to the recited "register" and CPLD 410 and register 408 in Amidi's Figure 4A to the recited "logic element." RAN 23[11]; R1 February 13, 2012 Comments 2–12, 27–28 (referring to R1 Request). Based on our construction of "logic element" discussed above, we do not find error in the mapping of register 418 in Amidi to the recited "register" and register 408 to the separately recited "logic element" (RAN 23) given that a register performs some amount of logic (Sechen Decl. ¶ 19). Contrary to Patent Owner's contentions (PO App. Br. 17–18), we also do not find the Examiner erred in further mapping CPLD 410 in combination with register 408 to the separately recited "logic element." By its very name (i.e., Complex Programmable Logic Device), CPLD 410 discloses that it performs logical operations. Moreover, as discussed above, a "logic element" can comprise various discrete electrical components.

As to whether "Figure 6" of Amidi discloses that both registers (e.g., 408, 418) receive bank address signals, Amidi shows bank address signals are received by register 608 (e.g., BA[1:0]) in Figure 6A. *See* RAN 24 (stating "registers 408 and 418, shown as 608 in Figure 6, receive BA signals."). Patent Owner argues that Amidi fails to teach bank address signals are received by both a register and a logic element, arguing Amidi teaches receiving the bank address signals only at a single register for passing to the DDR memory devices. PO App. Br. 14–15; PO Reb. Br. 4; *see* 2d Sechen Decl. ¶ 18.

Patent Owner's position is grounded in what Patent Owner contends one skilled in the art would have understood given Amidi's disclosure. That is, during

[11] Although this portion of the RAN discusses claim 5, claim 7 includes the same limitation of a "circuit comprising a logic element and a register." *Compare* PO App. Br. 50, Claims App'x., *with* PO App. Br. 51, Claims App'x.

Copied from 95000579 on 02/08/2017

examination of a patent application, a claim is given its broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad.*, 367 F.3d at 1364 (citations and internal quotation marks omitted). Patent Owner argues that one skilled in the art would have interpreted Amidi's figures (e.g., Figs. 6A–B) based on industry standards, namely JEDEC. PO App. Br. 13–15, 18–21 (citing JEDEC 79C 6–7 and 11–12; JEDEC 21-C 4.20.4–16, 4.20.4–18, and 4.20.4-33; 2d Sechen Decl. ¶¶ 18–23, 34–36, 40, 42–46; 2d Bagherzadeh Decl. ¶ 31; and 3d Bagherzadeh Decl. ¶¶ 8, 42, 43); PO Reb. Br. 6–8 (citing JEDEC 21-C; 2d Sechen Decl. ¶¶ 34–54; Wang Decl. ¶ 9; 2d Bagherzadeh ¶ 31; 3d Bagherzadeh Decl. ¶¶ 8, 42, 43; Jacob Decl. ¶ 19; and 4th Kozyrakis Decl. ¶ 19).

Specifically, Patent Owner contends that "[s]tandards set the default position in an industry" (PO Reb. Br. 9) and "a POSITA's [person of ordinary skill in the art's] default position would be to understand Amidi's registers in light of [the] JEDEC specification, including JEDEC 21-C." PO Reb. Br. 10. Where Amidi is silent concerning its memory module design, in Patent Owner's view, an ordinarily skilled artisan "would begin with JEDEC reference designs to achieve a JEDEC-compliant memory module." PO Reb. Br. 9.

Patent Owner contends that JEDEC 21-C shows only one register (e.g., Register 2) receiving the bank address signal. PO App. Br. 14 (citing JEDEC 21-C 4.20.4-18). Requester 1 disagrees, arguing that both register 408 and register 418 receive bank address signals.[12] R1 Resp. Br. 6–7. Requester 1 asserts that Amidi

[12] Patent Owner asserts that the anticipation rejection was not opposed by Requester 1, because Requester 1 focuses on the obviousness rejection based on Amidi. PO Reb. Br. 14; R1 Resp. Br. 9. However, Requester 1's discussion

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is not strictly JEDEC-compliant. R1 Resp. Br. 7–8, 10 (citing 3d Wang Decl. ¶ 17). Requester 2 notes that the Examiner correctly found that Amidi discloses both a register and a logic element receiving bank address signals. R2 Resp. Br. 5–6 (citing RAN 26).[13] Specifically, Requester 2 asserts that both registers 408 and 418 in Amidi receive bank address signals. R2 Resp. Br. 6 (citing Amidi, Fig. 6A). Requester 3 does not specifically address the anticipation rejection of Amidi. R3 Resp. Br. 4.

Amidi shows bank address signals are received by register 608 (e.g., BA[1:0]) in Figure 6A. Amidi, Fig. 6A. Unlike the address signals (A0-A11) that Amidi explicitly states are received by both registers 408 and 418 (Amidi ¶ 49), the accompanying disclosure in Amidi does not discuss whether the bank address signals are also received by both registers 408 and 418 shown in Figures 4A and B. *See* Amidi ¶¶ 49–52. Rather, one must infer from Amidi's Figures 6A and 6B that both registers 408 and 418 receive bank address signals. Amidi also fails to describe or show in Figures 4A–B and 6A–B a bank address signal entering CPLD 410 or 604. *See* Amidi, Figs. 4A–B, 6A–B.

As stated,

> If the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if that element is "inherent" in its disclosure. . . . "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient."

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addresses what Amidi discloses. *See, e.g.,* R1 Resp. Br. 6–7, 8–10. In essence, Requester 1 has argued that Amidi anticipates various recited features of the claims. *Id.* Moreover, Requester 2 echoes Requester 1's position. R2 Resp. Br. 5–6.

[13] Requester 2 failed to include page numbers in the respondent brief. We refer to the page numbers sequentially as submitted.

Copied from 95000579 on 02/08/2017

In re Robertson, 169 F.3d 743, 745 (Fed. Cir. 1999) (internal citations omitted). We thus turn to other evidence in the record, such as the JEDEC standards and expert testimony, to determine whether receiving bank address signals at both registers 408 and 418 would have been an inherent feature that would necessarily flow from the teachings in Amidi.

Amidi refers to JEDEC standard only when discussing "defined height limits" (Amidi ¶ 7) and does not discuss any other JEDEC design specifications. Dr. Wang states Amidi's devices and modules "are not restricted to JEDEC specifications-compliant devices and modules" and that the '912 patent, like Amidi, deviates from JEDEC standards by using, for example, twice as many DRAM devices in its arrangement. 3d Wang Decl. ¶¶ 17–18. That is, Amidi also discusses creating a transparent four rank memory module that fits into a memory socket having two chip select signals. Amidi ¶¶ 11–12. On the other hand, Dr. Bagherzadeh states "Amidi discloses JEDEC compliant DIMMs [dual in-line memory module]." 3d Bagherzadeh ¶ 43. But, Dr. Bagherzadeh also states that an ordinary artisan would understand Amidi's DIMMs "conform to standards authored by JEDEC" without indicating to which "standards" Amidi conforms. *See* 2d Bagherzadeh ¶ 31. Weighing the evidence, we agree with Requester 1 that Amidi is not compliant with all of the design specifications set forth for memory module design of JEDEC 21-C.

Even so, Amidi fails to discuss whether both registers 408 and 418 necessarily receive bank address signals. We thus turn to the JEDEC 21-C specification and the testimony of record for any insight as to whether both registers receiving bank address signals is an inherent feature of Amidi.

Copied from 95000579 on 02/08/2017

Petitioners
Ex. 1016, p. 24

Dr. Sechen indicates that JEDEC 21-C is a design specification for DDR SDRAM (synchronous dynamic random access memory) registered DIMMs, including 72-bit registered DIMMs using 36 stacked memory devices arranged in four ranks. 2d Sechen Decl. ¶¶ 18–19 (citing JEDEC 21-C, 4.20.4-16, 4.20.4-18). Amidi in Figure 4A and B also describes a 72-bit registered DDR module, but the record does not indicate clearly whether the cited portions of JEDEC 21-C are directed to a 72-bit embodiment. *Compare* Amidi ¶¶ 37, 42, Figs. 4A–B (describing "Transparent 72-bit Registered DDR Module") *with* JEDEC 21-C, 4.20.4-16 (discussing two physical banks of x4 DDR SDRAMs (synchronous dynamic random access memory)). Even so, the JEDEC 21-C embodiments, including 72-bit embodiments, repeatedly show a single register box receiving the bank address signals (e.g., BA0-BA1). JEDEC 21-C, 4.20.4-10–4.20.4-16. Moreover, concerning the register functional assignments, all the raw card versions in the JEDEC specification show two registers (e.g., Register 1 and Register 2) but only one register (e.g., Register 2) receiving the input bank address signals (e.g., BA0 and BA1). JEDEC 21-C, 4.20.4-18, *reproduced at* 2d Sechen Decl. ¶ 19.

Given the above discussion of JEDEC 21-C, Dr. Sechen asserts that the register function, like that in register 608 in Figure 6A, is shown as a single box but that the register box is implemented using one or two registers. 2d Sechen Decl. ¶ 19. In the two register case, Dr. Sechen testifies that the JEDEC 21-C design specification uses only one of the two registers to receive the input bank address signals. *Id.* ¶¶ 19–21 (citing JEDEC 21-C, 4.20.4-18 and 4.20.4-22). We agree. Similarly and because Amidi does not discuss explicitly whether bank address signals are received by both registers 408 and 418, the record reflects the possibility that Amidi's two registers (e.g., registers 408, 418) may function as a

Copied from 95000579 on 02/08/2017

single register box, such as that shown in JEDEC 21-C. We thus determine that Amidi does not anticipate the bank address recitation of claim 7.

Regarding Amidi's CPLD, Patent Owner further contends that the bank address signals in Amidi are not passed to the CPLD of Amidi. PO App. Br. 16. Patent Owner states that address signals (e.g., Add(n) in Fig. 6A) are received by CPLD (e.g., 604), but these signals are not *bank* address signals (e.g., BA[1:0]). PO App. Br. 17; *See* PO Reb. Br. 5. Rather, they are, in Patent Owner's view, row/column address signals, which are separately recited in claim 7 and which are separately described and shown in Amidi. *See* Amidi ¶¶ 49–51, Fig. 6A. We agree. Accordingly, the Examiner has not demonstrated that Amidi necessarily discloses a register (e.g., 418) and a logic element (e.g., register 408 alone or register 408 and CPLD 410 collectively) receiving bank address signals as recited in claim 7.

On the other hand, Requester 2 points out that claim 33 differs in scope from claim 7. *See* R2 Resp. Br. 6. We agree. Namely, claim 33 does not require both a logic element and a register to receive the input bank address signals, rather *only* "the register receives the bank address signals." *Id.* As discussed above, Amidi discloses a register receiving the bank address signals (*see* R1 Request 148 (citing Amidi ¶ 50, Fig. 6A))— a finding undisputed by Patent Owner. *See* PO App. Br. 15.

For the above reasons, under 35 U.S.C. § 102, we determine that the Examiner erred in rejecting claim 7 and but did not err in rejecting claim 33 based on Amidi.

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2. *Obviousness Rejection Based on Amidi Alone or Amidi and JEDEC – Grounds 4 and 6*

We next consider whether Amidi renders obvious to one of ordinary skill in the art that (1) both registers 408 and 418 receive bank address signals or (2) one of register 408 or 418 and CPLD 410 receive bank address signals. The Examiner states that claims 7 and 33 are rejected under 35 U.S.C. § 103, "[b]ecause these claims are anticipated by Amidi." RAN 28. As previously stated, we agree claim 33 is anticipated by Amidi. Thus, we further agree with the Examiner that claim 33 is obvious. *See In re McDaniel*, 293 F.3d 1379, 1385 (Fed. Cir. 2002) (citations omitted) (indicating that anticipation is the epitome of obviousness).

Regarding claim 7, the Examiner does not discuss features missing from Amidi or what in Amidi renders the claim obvious. The rejection refers to proposed rejections presented by Requesters 1 and 2 and thus relies on the proposed analysis for these grounds. RAN 12 (referring to proposed rejections of Requesters 1 and 2 and "modified 2/13/13"), 61–62 (stating Requester 1's Comments filed February 13, 2013[14] related to claim 7 and 33 are convincing), and RAN 74 (stating "Requesters' (both 1 and 2) argument that Amidi discloses a logic element . . . is persuasive.") Requester 1 discusses that one skilled in the art would have recognized various memory modules that do not follow JEDEC standards. R1 February 13, 2013 Comments 4–5 (referring to 3d Wang Decl. ¶¶ 18–19); *see*

[14] Requester 1 filed comments both on February 13, 2012 (previously discussed) and February 13, 2013. Requester 2 also filed comments on February 13, 2012 and February 13, 2013. Requester 2's February 13, 2013 Comments were found defective, and corrected comments were subsequently filed on August 14, 2013. Requester 3 filed comments on February 23, 2012.

Copied from 95000579 on 02/08/2017

also February 13, 2012 Comments 4–5 (referring to 2d Wang Decl.), 15–19, 28–29, 41 (referring to claim charts in R1 Request).

Patent Owner contends there is no suggestion in Amidi (1) to make each of registers 408 and 418 into register 608 or (2) to duplicate the register function. PO App. Br. 21–23 (citing 2d Sechen Decl. ¶ 46); PO Reb. Br. 5–6, 10–12. Patent Owner admits that Amidi instructs ordinarily skilled artisans to deviate from JEDEC design specifications where expressly disclosed. PO Reb. Br. 9. But, Patent Owner contends "where Amidi does not expressly instruct a POSITA to depart from JEDEC reference designs, a POSITA—familiar with relevant JEDEC standards—would begin with JEDEC reference designs to achieve a JEDEC-compliant memory module." *Id.* Patent Owner also asserts one would closely adhere to these standards to avoid "operational failure." PO App. Br. 29.

Requester 1 disagrees, asserting that a skilled artisan "was not limited to constructing JEDEC compliant modules," including "dimensional and power requirements." R1 Resp. Br. 8 (citing 3d Wang Decl. ¶ 17). Requester 1 also argues that one skilled in the art would have known of the existence of "multitudes of memory modules . . . that did not follow JEDEC specifications." R1 Resp. Br. 8; *see* R1 Resp. Br. 9 (citing Wang Decl. ¶¶ 17–21 and 3d Wang Decl. ¶¶ 17–19).

Before we determine what Amidi suggests, we must resolve the level of skill in the pertinent art. *See Graham v. John Deere Co.*, 383 U.S. 1, 11 (1966). Requester 1 states that the level of skill "was high," but provides no further details describing the skill level. R1 Resp. Br. 4 (referring in general to the Wang Declarations); *see generally* Wang, 2d Wang, and 3d Wang Decls. Dr. Bagherzadeh states

> the level of skill in the art related to the '912 patent in my opinion is a person with a degree in either electrical or computer engineering or in

Copied from 95000579 on 02/08/2017

> a closely related discipline, and at least 1-2 years of experience in designing computer memory systems and would have an understanding of industry standards adopted by Joint Electronic Devices Engineering Council (JEDEC).

Bagherzadeh Decl. ¶ 16; 3d Bagherzadeh Decl. ¶ 10. Dr. Kozyrakis states he believes

> a person of ordinary skill in the art as of the priority date of the '912 patent would have the following training, knowledge, and experience: an undergraduate degree in Electrical Engineering or Computer Engineering, at least two years of professional experience in the design of memory systems, familiarity with the latest JEDEC standard specifications for memory devices and modules, and familiarity with the latest DRAM memory devices widely available in the market.

Kozyrakis Decl. ¶ 8; 2d Kozyrakis Decl. ¶ 12; 3d Kozyrakis Decl. ¶ 9; 4th Kozyrakis Decl. ¶ 12. Dr. Sechen does "not necessarily agree with Dr. Kozyrakis's definition of a POSITA in the technical field," but adopts this understanding for purposes of analysis. Sechen Decl. ¶ 10.

Based on the testimony of these various experts,[15] we determine a person of ordinary skill in the art is a person with (1) at least an undergraduate degree in either electrical engineering, computer engineering, or in a closely related discipline and (2) at least two years of experience in designing computer memory systems. This ordinarily skilled artisan would also have familiarity with and understanding of (1) JEDEC standards related to memory devices and modules, such as DDR SDRAM devices and DIMMs, and (2) the latest DRAM memory

[15] None of the parties in this proceeding dispute these individuals' qualifications. We thus presume these experts are qualified to address the technology in the '912 patent and the skill level in the art.

Copied from 95000579 on 02/08/2017

devices in the market. We additionally note that the prior art, including Amidi, reflects the appropriate skill level at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).[16]

Next, we turn to Amidi and the differences between Amidi and the claims at issue. *See Graham*, 383 U.S. at 11. As stated above, Amidi explicitly discusses address signals (e.g., A0-A11), but not bank address signals, are received by registers 408 and 418. Amidi ¶ 49. However, under an obviousness analysis, we consider further what an ordinary skilled artisan would have recognized from Amidi's disclosure, when employing one's inferences and creative steps. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

Amidi states "address lines A0-A11 go to module register 408 and 418 and address lines A12 goes into CPLD." Amidi ¶ 49. Amidi also shows address signals Add[n-1:0] (e.g., A0-A11) entering register 608 in Figure 6A and Add(n) (e.g., A12) entering CPLD 604. Amidi, Fig. 6A. When considering these teachings collectively, Amidi suggests that register 608 may be both registers 408 and 418 in Figures 4A and B. Amidi, Figs. 4A–B, 6A–B. That is, the teaching in paragraph 49 in Amidi related to where the address lines connect combined with the signals shown entering register 608 in Figure 6A suggests that register 608 represents both register 408 and 418. *See* R3 Resp. Br. 4. Importantly, this teaching in Amidi deviates from JEDEC standards, such as JEDEC 21-C, which shows only certain address signals are inputted into one register (e.g., register 1) and other address signals are inputted into another register (e.g., register 2). JEDEC 21-C, 4.20.4-18.

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[16] This position is consistent with at least IPR2014-00883. *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00883, Paper No. 33, slip op. at 13 (PTAB December 14, 2015).

Copied from 95000579 on 02/08/2017

Amidi's Figure 6A shows various other signal lines entering register 608, including bank address signal lines. Amidi, Fig. 6A. Following from the above discussion that Amidi's registers 408 and 418 receive address lines A0 through A11, Amidi's Figure 6A and B thus suggests that both registers 408 and 418 may receive other signals shown entering register 608, including bank address signals. *See* R3 Resp. Br. 4. We agree that combining the teachings in Amidi at least suggest to an ordinary skilled artisan that signals other than the explicitly-disclosed address signals A0-A11, such as bank address signals BA0 and BA1, may be received by each of register 408 and 418 in a similar fashion.

Moreover, Amidi teaches deviating from JEDEC design specifications in at least one other aspect. Amidi discusses creating a transparent four rank memory module that fits into a memory socket having two chip select signals (e.g., a configured two rank memory module). Amidi, Title, ¶¶ 1, 4, 8, 11–12, 49; 3d Wang Decl. ¶ 17; R3 Resp. Br. 2–3 (citing Amidi ¶ 10–12). Amidi further states its memory module emulates a two rank memory module with a four rank memory module. Amidi ¶¶ 23, 41, 49, 57, 59, 62, Fig. 7. As understood, JEDEC 21-C design examples do not discuss such a transparent four rank memory module. *See generally* JEDEC 21-C. Thus, Amidi discloses at least one more example of deviating from the JEDEC design specifications.

Even further examples include the register in JEDEC includes two additional input signals, S0 and S1, which are described as chip select lines (*see* JEDEC 21-C, 4.20.4-6 and 4.20.4-16), which contrast with Amidi's chip select lines, cs0 and cs1, entering CPLD 604 *(see, e.g.*, Amidi, Fig. 6A).

As previously stated when addressing the anticipation rejection, Patent Owner accepts that one skilled in the art would have recognized that Amidi

Copied from 95000579 on 02/08/2017

deviates from JEDEC design specifications where expressly stated. PO Reb. Br. 9. However, Patent Owner argues where Amidi is silent concerning departing from JEDEC, "a POSITA's default position would be to understand Amidi's registers in light of JEDEC specification, including JEDEC 21-C." PO Reb. Br. 10. Based on this understanding, Patent Owner asserts that one skilled in the art would have understood Amidi's register 608 in the context of the described register functional assignments in JEDEC 21-C, where only one register receives the bank address signals. PO App. Br. 14–15 (discussing and reproducing part of JEDEC 21-C 4.20.4-18), 20–21 (discussing and reproducing part of JEDEC 21-C4.20.4-16).

We agree with Patent Owner to the extent that an ordinary skilled artisan having two years of experience designing memory modules would have *consulted* with the JEDEC specifications, including JEDEC 21-C, when designing a circuit for a memory module or DIMM. However, we depart from Patent Owner's position that one skilled in the art would always adhere to JEDEC specifications wherever Amidi is silent. Other than the explicit disclosure to the "standard defined height limits by JEDEC" which restricts the number of TSSOP (thin-shrink small outline package) placements per side or per module (Amidi ¶ 7), Amidi does not discuss any further restrictions or adherence to JEDEC (*see generally* Amidi). As another example discussed above, Amidi teaches emulating a two rank memory module using a transparent four rank memory module. Amidi ¶¶ 23, 41, 49, 57, 59, 62, Fig. 7. As such, an ordinary skilled artisan would have recognized that not all designs, including Amidi's, follow JEDEC specifications.

Moreover, one having ordinary skill is not an automaton and would have employed their background knowledge and creative steps when designing memory modules. That is, one skilled in the art would have recognized that memory

Copied from 95000579 on 02/08/2017

modules that explicitly differ from JEDEC design specifications, such as Amidi's (e.g., emulating a two rank memory module on a four-rank memory module), may affect the memory module in other ways and require further unspoken differences, including other signals being received by registers in Amidi. For instance, one skilled in the art would have recognized that directing other signals, including bank address signals, to two registers can further assist in emulating a two rank memory module in a four rank memory module in a cost effective manner. *See* Amidi ¶¶ 11, 23, 41, 49, 57, 59, 62, Fig. 7.

And even if one skilled in the art would defer to JEDEC 21-C designs, JEDEC 21-C itself teaches the ordinarily skilled artisan that modifications to the reference design may be required. Specifically, JEDEC 21-C discusses reference design examples as "an initial basis for Registered DIMM designs" but further clarifies that modifications to the reference designs may be required to meet "all system timing, signal integrity, and thermal requirements." JEDEC 21-C, 4.20.4-5, *cited in* R3 Resp. Br. 3–4. Additionally, we agree with Requester 1 that JEDEC does not state that two registers are sufficient for all types of memory modules. *See* R1 Resp. Br. 10 (citing 3d Wang Decl. ¶ 19).

Accordingly, when comparing JEDEC 21-C with Amidi, an ordinary skilled artisan would have recognized Amidi's memory module design differs from JEDEC reference designs and that modification from the JEDEC reference designs would need to occur. JEDEC 21-C, 4.20.4-5, *cited in* R3 Resp. Br. 3–4; *see also* R1 Resp. Br. 10 (indicating that POSITA is not "limited to constructing JEDEC compliant modules" and citing 3d Wang Decl. ¶ 19). These modification suggests signals other than address signals (e.g., bank address signals) being received by registers to meet system timing, signal integrity, and thermal requirements. We

Copied from 95000579 on 02/08/2017

therefore disagree with Patent Owner that "there would be no suggestion or motivation in Amidi to have each Registers 408 and 418 be Register 608." PO App. Br. 21 (citing 2d Sechen Decl. ¶ 46).

Additionally, there is testimony supporting Requester 1's position that Amidi is not JEDEC compliant in all aspects where Amidi is silent. *See* R1 Resp. Br. 9–10; R3 Resp. Br. 3; 3d Wang Decl. ¶ 17. Dr. Wang indicates that an artisan is not limited by the conventional uses and is aware of variations from the JEDEC specification. 3d Wang Decl. ¶ 17. Requester 3 echoes Requester 1's position, contending that a person of ordinary skill is not limited to JEDEC reference designs. R3 Resp. Br. 3. Dr. Wang also states an ordinarily skilled artisan "would know that there exist multitudes of memory modules and supporting devices that do not follow JEDEC specification." 3d Wang Decl. ¶ 17, *cited in* R1 Resp. Br. 8, 10. Patent Owner contends Dr. Wang's testimony undermines (1) his own earlier testimony in this regard, (2) Dr. Bagherzadeh's, and (3) Dr. Sechen's. PO App. Br. 23 (citing Wang Decl. ¶ 9,[17] 2d Bagherzadeh Decl. ¶ 31, and 2d Sechen Decl. ¶ 34).

In response, Requester 1 asserts that Patent Owner took Dr. Wang's discussion in his first declaration "out of context." R1 Resp. Br. 11. In paragraph 9, Dr. Wang indicates that a logic circuit designer would have been guided by standard bodies such as JEDEC "[i]n many instances" and "would have configured a logic circuit to meet the functional requirements of the JEDEC standards." Wang Decl. ¶ 9. However, Dr. Wang further states that "the exact implementation is also driven by *other design requirements and designer preferences*." *Id.* (emphasis

[17] Requester 1 indicates that Patent Owner mistakenly referred to paragraph 10 of Wang's declaration. R1 Resp. Br. 11 n.2.

Copied from 95000579 on 02/08/2017

added). For example, "a logic circuit designer" would have weighed various factors, including the

> decision to combine control logic, flip-flops and other elements of a register with combinational logic may be made to obtain reduction in cost, gate count, reduced loading, reduced power consumption and to lower complexity of DIMM layout, although such decisions may also be influenced by the 'best practices' approach of JEDEC[.]"

Id. As such, we determine that Dr. Wang's later testimony related to deviating from JEDEC specifications is consistent. That is, artisans are influenced by JEDEC design specification but also weigh *other* design factor and preferences beyond JEDEC design specifications. *See id.*

Concerning the other experts, we agree with Dr. Bagherzadeh that an artisan would have looked to JEDEC 21-C for guidance when designing a DIMM, as stated previously, but disagree that "the DDR DIMMs taught by Amidi conform to [the] standards authorized by JEDEC" (2d Bagherzadeh Decl. ¶ 31) in *every* aspect as previously discussed. Notably, Dr. Bagherzadeh is not specific as to which JEDEC standards Amidi conforms. *Id*. Nonetheless, because Amidi differs from JEDEC design standards as previously explained, we determine Dr. Bagherzadeh's testimony is less probative than Dr. Wang's regarding JEDEC design specification conformance. Dr. Sechen also urges us that one skilled in the art would have followed JEDEC when the prior art is silent. PO App. Br. 23 (citing 2d Sechen Decl. ¶ 34). But, as stated previously, we disagree.

We further find that Dr. Wang's testimony is aligned with Amidi, which deviates from JEDEC designs, and has probative value in determining that there are a "broad range of design considerations that a logic circuit designer would take into account," and may also be influenced "by other design requirements and

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designer preferences [than JEDEC,]" including those concerning reducing costs, loading, power consumption, and complexity of DIMM layout. R1 Resp. Br. 11 (quoting Wang Decl. ¶ 9). When referring to Figure 6A of Amidi specifically and when designing a memory module, Dr. Wang states that one "would have understood . . . it would be prudent to connect all or substantially all of the address, control and other signals to . . . registers . . . in order to provide the logic designer with maximum flexibility." Wang Decl. ¶ 21. Amidi further recognizes that many memory device families or densities may be used to build Amidi's memory module. Amidi ¶ 71. Although the record may not support that one would have recognized to connect *all* signals to registers in Amidi, we agree with Dr. Wang that Amidi suggests to an ordinary artisan to connect some of signals in Amidi to both registers as previously discussed.

When considering collectively (1) Amidi deviates from JEDEC design specifications in multiple ways, including (a) disclosing receiving address signals A0–A11 at registers 408 and 418, (b) emulating a two rank memory module using a transparent four rank memory module, and (c) diverting its chip-select signals to a logic element, (2) the suggestion in Amidi that one skilled in the art would have recognized based on deviations from JEDEC design specifications that signals other than address signals also enter Amidi's register shown in Figure 6A, and (3) the background knowledge and creative steps of an ordinarily skilled artisan would have employed given Amidi's teachings and suggestions alone or in combination with JEDEC, we determine that one skilled in the art would have recognized both registers (e.g., one mapped to the recited "register' and the other mapped to the recited "logic element") receiving bank address signals to account for the design requirements of Amidi and preferences of the artisan. To the extent that changes

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are needed to Amidi to connect signals other than row/column address signals, such as bank address signals to the registers, such a change permits the logic circuit designer the flexibility to design a logic circuit for multiple purposes and applications as discussed previously. We therefore disagree with Patent Owner that Requesters have not provided any rebuttal to demonstrate why a person of ordinary skill in the art would have bank address signals enter both registers in Amidi. *See* PO Reb. Br. 11–12.

Patent Owner contends that bank address signals entering both registers (e.g., 408 and 418) implies duplication of the register function, including receiving "the same set of input signals" and that this duplication makes no sense to one skilled in the art when considering power and dimensional requirements as well as costs. PO App. Br. 21–22 (citing 2d Sechen Decl. ¶¶ 46–51); PO Reb. Br. 10–11. For support, Dr. Sechen testifies that an ordinarily skilled artisan would have been aware of dimensional requirements for JEDEC modules, including height requirements discussed by Amidi, and that given these concerns, one would not have understood Amidi suggests each register 408 and 418 to be the entire register function. 2d Sechen Decl. ¶ 47–48.

We are not persuaded. First, the above discussions concerning Amidi and what one of ordinary skill in the art would have understood from Amidi teach the input address signals are received by both registers 408 and 418 contrary to JEDEC 21-C. *See* Amidi ¶ 49, Fig. 6A. Also, these teachings in Amidi do not require that the *entire* register function be duplicated in each of register 408 and 418.

Second, even if duplicated in its entirety occurs, such as the *alternative* rejection presented for Ground 6 (RAN 33), Amidi's statement related to considering the "standard defined height limits by JEDEC" for TSSOP placement

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per side and per module (Amidi ¶ 7) do not require compliance in other design aspects as previously discussed. Third, there is inadequate evidence in the record between the height or dimensional requirements discussed in Amidi that are according to JEDEC specifications (*id.*) and how Dr. Sechen concludes that this sole dimensional requirement would lead an ordinarily skilled logic circuit designer not to understand Amidi suggests each of registers 408 and 418 to receive at least some of the signals shown in Figure 6A entering register 608. *See* 2d Sechen Decl. ¶ 47–48.

Dr. Sechen further discusses the power requirements that would result from each register 408 and 418 if duplicated. 2d Sechen Decl. ¶¶ 49, 51. In particular, Dr. Sechen states that one skilled in the art would have concluded that two registers behave as a single register according to JEDEC design specifications so as to "minimize power." 2d Sechen Decl. ¶ 51. To be sure, power consumption would be a factor to an ordinarily skilled artisan when designing a memory module. However, as explained above, Amidi does not possess a traditional JEDEC logic circuit design and requires modifications from JEDEC design specifications. Thus, although we appreciate Dr. Sechen's insights that "JEDEC 21-C at page 4.20.4-62 explains that a single Register (comprising Registers 1 and 2) is sufficient to handle a module having 36 DDR DRAM devices in a stacked arrangement" (2d Sechen Decl. ¶ 50), we are not persuaded sufficiently that any increased power consumption in Amidi resulting from directing bank address signals to both registers 408 and 418 would be unworkable.

Even if more power is consumed in Amidi's memory module when the registers are duplicated, balancing the relative advantages (e.g., flexibility of using less expensive chips) and disadvantages (e.g., increased power consumption) are

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engineering tradeoffs well within the level of ordinarily skilled artisans. That is, Amidi teaches creating a transparent four rank memory module that fits into a memory socket having two chip select signals (e.g., emulating the function of a two rank memory module) because such lower density memory devices are cheaper and more readily available. *See* Amidi ¶¶ 1, 4, 8, 11–12; R3 Resp. Br. 3. The record thus supports that a logic circuit designer employing their background knowledge would have considered various design factors (e.g., cost, loading, power consumption, complexity) when designing a memory module.

As to whether Amidi additionally suggests that CPLD 604 receives bank address signals, we indicated previously that Amidi does not disclose bank address signals are received by CPLD 604. Amidi, Figs. 6A–B; October 14, 2011 Non-Final Act. 15 (stating "Figure 6 clearly shows that only the register 608 receives the bank address signals.") But, as stated above, our analysis based on obviousness does not stop here.

When addressing Ground 4, the record reflects that the Examiner did not adopt Requester 1's position that "it would have been obvious to one or [sic] ordinary skill in the art at the time of the invention to provide such control signals to the [CPLD] to improve the active bank/rank determination." Non-Final Act. 15–16 (quoting from R1 Request 128). In particular, the Examiner states "[t]his is merely an allegation without any reasoned analysis as to how and why providing 'such control signals' to [the] CPLD would be obvious and improve . . . or duplicate the control signals so as to be received by [the] CPLD and how this improves the memory module." October 14, 2011 Non-Final Act. 16. We agree with Patent Owner that subsequent actions maintain this position. PO Reb. Br. 13. That is, when addressing claim 7, the Examiners adopted the analysis that Amidi

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teaches or suggests both registers received the bank address signals but not the CPLD. *See* November 13, 2012 Non-Final Act. 18, ACP 24, and RAN 24 (referring to "Figure 6, registers 408 and 418, shown as 608 in Figure 6, receive BA signals" for Grounds 3 and 4 when discussing claim 7); ACP 28 and RAN 28 (referring to Ground 3 when discussing Ground 4).

As such, the record reflects that the Examiner determined that there is insufficient reasoning with a rational underpinning why one skilled in the art would have recognized providing Amidi's CPLD with a bank address signal.

Dr. Wang, Requester 1's expert, addresses Amidi's CPLD (e.g., 410 in Figure 4A or 604 in Figure 6A) stating one skilled in the art "would have considered connecting all address signals, including bank address signals, to the Amidi CPLD to allow flexibility in design of an address mapping scheme." Wang Decl. ¶¶ 17, 21. Dr. Wang states:

> Amidi describes the use and operation of a logic element to reassign address signals when a memory module is designed to emulate a memory module having a different number of ranks. For example, where a memory module having two lower density ranks is used to emulate a memory module with one rank having double the memory density, Amidi would have been used to remap address signals, including rank address signals. A person of ordinary skill in the art of memory system design would have known to remap address signals by reassigning one or more bank address signals for rank selection purposes.

Wang Decl. ¶ 19.

Dr. Wang also states, when addressing supplying bank address signals to a logic device, "[p]ersons of ordinary skill in the art related to memory system design would have known that many different address mapping schemes . . . and that the choice of address mapping scheme would have been made based on various design goals." Wang Decl. ¶ 24. As such, Dr. Wang contends connecting

Copied from 95000579 on 02/08/2017

address signals, including bank address signals, to the CPLD allows for flexibility in design of address mapping scheme and for reconfiguring to receive different configurations and memory densities. Wang Decl. ¶¶ 17, 21. In an attempt to corroborate the position that an ordinary skilled artisan would have known to use different mapping schemes for the CPLD, including using a bank address signal as a density transition bit to generate a chip-select signal, Dr. Wang discusses an attached exhibit, Exhibit A, and an Intel 450NX chip set. 3d Wang Decl. ¶ 14 (citing Ex. A, 2-5, 212 – 2-15). Notably, this exhibit is not part of the obviousness rejections based on Grounds 4 and 6. Moreover, Dr. Wang does not demonstrate that these Intel chip sets were known to be used in DIMMs, like Amidi's. *See id.*

Upon review, we determine this exhibit is inconclusive and does not demonstrate adequately that a "RAS/CAS generator accepts External (Input) signals as Bank[2:0]#, CARD#, CMND[l:0], MA[13:0]# and decodes the Bank[2:0]# signals as CAS and RAS signals to directly drive banks of DRAM devices." Exhibit A, 2-5, 2-12–2-15. At best, the exhibit discusses column and row access strobes (CAS/RAS) signals are used to latch column and row addresses into the DRAMS. *See* Exhibit A, 2-14. This discussion in no way addresses why one skilled in the art would have recognized Amidi's CPLD receiving a bank address signal.

Moreover, Dr. Wang indicates "the Intel 82452NX RAS/CAS generator datasheet is a datasheet that describes the functionality of the chipset as a whole rather than a logic specification of the 82452NX RAS/ CAS generator." 3d Wang Decl. ¶ 14. Without further discussion, he further concludes that

> it would have been clear to a person of ordinary skill in the art at the relevant time that the 82452NX RAS/CAS generator accepts BANK[2:0]# signals as inputs, and upon assertion of the Access

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> command and Command strobe signals, the 82452NX RAS/ CAS generator creates command sequences, including RAS and CAS signals at least in part to the BANK address signals.

Id. Yet, even presuming without deciding that Dr. Wang is correct, we disagree that this data sheet, as discussed above, demonstrates to an ordinarily skilled artisan to use Amidi's CPLD to receive a bank address signal. *See id.*

Granted, Amidi has a general teaching to modify its memory module design. Amidi ¶ 71. But, as stated above, the record for Requester 1's adopted rejection does not support the specific modification of using a bank address signal in place of a row or column address signal (e.g., Add(n)) in Amidi. Amidi, Figs. 6A–6B. Other than conclusory remarks made by Dr. Wang, this is insufficient evidence in Amidi, JEDEC, or elsewhere in the record to demonstrate a reason with rational underpinning that one skilled in the art would have inputted a bank address signal, as opposed to a row/column address signal, into Amidi's CPLD.

Thus, to the extent Patent Owner has argued Requester 1's proposed obviousness rejections based on Amidi or Amidi and JEDEC (Grounds 4 and 6) do not demonstrate a CPLD receiving BA signals, we agree.

Lastly, although not argued by Patent Owner (*see* R1 Resp. Br. 2), we agree with the Examiner's findings and conclusion concerning the evidence of secondary considerations failing to outweigh the case for obviousness. RAN 65–66.[18]

For the above-discussed reasons, we sustain the adopted rejection of claims 7 and 33 based on Amidi alone (Ground 4) or Amidi in combination with JEDEC (Ground 6) under § 103.

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[18] The Examiner refers to the Declaration of Dr. Hyun Lee dated July 5, 2011 and the Declaration of Christopher Lopes dated July 5, 2011. RAN 65.

Copied from 95000579 on 02/08/2017

3. *Obviousness Rejection Based on Amidi and Dell 2 – Ground 5*

Claims 7, 26, and 33 are also rejected under 35 U.S.C. § 103 based on Amidi and Dell 2. RAN 12 (referring to "Proposed by Requesters 1 and 2; modified 8/14/13"[19]), 30. As a preliminary matter, the RAN states claim 26 is rejected under Ground 5. RAN 12, 30. However, the body of the rejection does not discuss claim 26 and refers to Ground 3, which does not reject claim 26. *See id.* The Examiner did not clarify this anomaly in the Answer. Both Patent Owner and Requester 1 indicate the discrepancy, each reaching the opposite conclusion as to whether this claim has been rejected under Ground 5. *See also* PO Reb. Br. 14; R1 Resp. Br. 10 n.1, 13–14.

We determine that Patent Owner has been put on notice that claim 26 is rejected under this ground and has had the opportunity to respond to the rejected claim. First, claim 26 has been included in the rejection for Ground 5 since November 13, 2012. *See* November 13, 2012 Non-Final Act. 7 and ACP 7–8. Second, Patent Owner states "the recitations of claim 26 do not differ much from the recitations of claim 7." PO App. Br. 6, *quoted in* R3 Resp. Br. 6. And Patent Owner also grouped claim 26 with claims 7 and 33 in its opening brief, presuming claim 26 had been rejected based on Amidi under Grounds 3–6. PO App. Br. 12, 24 (stating "the Examiner's adoption and maintenance of Grounds 3-6 for claims 7, 26 and 33 was accordingly in error"). Thus, given that the record, claim 26 has been rejected for reasons similar to claim 7, and for purposes of this appeal, we treat claim 26 as having been rejected under § 103 based on Amidi and Dell 2 (Ground 5).

[19] Requester 2 filed corrected comments on August 14, 2013.

Copied from 95000579 on 02/08/2017

Turning to the merits of the rejection, Patent Owner does not dispute the teachings of Dell 2 related to this rejection. *See generally* PO App. Br. 12–24. Because Dell 2 is not disputed, Requester 1 contends that Patent Owner has waived its rights to appeal to the rejection. R1 Resp. Br. 14. In the Rebuttal Brief, Patent Owner contends that the Examiner's rejection on this ground expressly relies on Amidi alone and that Patent Owner "did not need to address Dell 2 to properly appeal the rejection of claim 26." PO Reb. Br. 14. We agree that Patent Owner has appealed this ground of rejection.

For Ground 5, the Examiner refers to Ground 3, concluding that claims 7 and 33 are obvious because they are anticipated. RAN 30. For the reasons discussed above, we agree that claims 7 and 33 are rendered obvious based on Amidi and the registers 408 and 418 mapped to the recited "register" and "logic element."

However, contrary to Patent Owner's position (PO Reb. Br. 14), this rejection *also* refers to the obviousness rejection over Amidi and Dell 2 proposed by Requester 1 and 2. RAN 12 (referring to "Proposed by Requesters 1 and 2; modified 8/14/13"); *see also* R2 August 14, 2013 Comments 4–12 (citing Amidi ¶¶ 8, 40–43, 45–52, 71; Dell 2, Abstract, 2:40–3:5, 4:62–6:14, 8:5–64; 3d Bagherzadeh Decl. ¶¶ 12–17, 21–22, 24, 26, 37; 2d Bagherzadeh Decl. ¶ 25) and R1 February 13, 2012 Comments 22 (referring to claim charts in R1 Request, which cite Dell 2, 2:32–38, Fig. 1 at R1 Request 159, 166, 176, 182). Thus, the RAN indicates that the proposed rejections of Requester 1 and 2 were adopted by the Examiner. *See* RAN 30 (indicating the proposed rejection of claims 7, 26, and 33 are adopted and these claims were proposed by Requester 1), 12 (referring to the proposals of Requester 1 and 2 *as modified on August 14, 2013*, which is the

Copied from 95000579 on 02/08/2017

date of Requester 2's comments). Accordingly, when viewing the RAN as a whole, the adopted rejection does not just rely on Amidi but is a combination of Amidi and Dell 2.

Patent Owner contends that Requester 2's arguments for Ground 5 are not permitted. PO Reb. Br. 17. Specifically, Patent Owner argues that the adopted rejection for Ground 5 rejected claims 7 and 33 "for Requester 1, but not for Requester 2." *Id.* (citing RAN 30). As noted above, we disagree. Also, although the Examiner states that the proposed combination with Dell 2 as presented by Requester 2 does not overcome "the deficiency" of Amidi (RAN 32), the deficiency discussed appears to concern limitations recited in claim 52, for example, which differ in scope from claim 7. *Id.* (referring to Ground 3); *see also* RAN 26–27 (discussing Ground 3).

We therefore determine that the Examiner has adopted Requester 1's and 2's proposed rejection, including that concerning the bank address limitation. To summarize, Requester 2 relies on the discussion of claim 1 when rejecting claim 7. R2 August 14, 2013 Comments 45–46 (referring to claim 1). Requester 2 in general states Amidi suggests other types of memory devices or densities can be used to build the four rank memory module. Amidi ¶ 71, *cited in* R2 August 14, 2013 Comments 8, 10–12, 29, 38. Additionally, Dell 2 teaches a technique for using various types of memory devices or densities other than those in Amidi, where the memory device is configured with M banks, but the logic circuit receives address and bank address inputs corresponding to N bank memory device. Dell 2, Abstract, claim 1, *cited in* R2 August 14, 2013 Comments 9, 29–30, 38–39. For example, Dell 2 teaches a logic circuit that receives address and bank address inputs where the memory devices of the memory module are configured with a

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different number of banks than the system's expected number of banks (e.g., memory module has memory devices having greater or fewer internal banks than expected). Dell 2, Abstract, 2:40–3:5, claim 1, Fig. 1, *cited in* R2 August 14, 2013 Comments 9–10, 12, 30, 39, 45–46.

The above teachings in Dell 2 teach or suggest a logic element receiving and using free signals, including a bank address signal, to provide the needed bank address signals based on the difference between the actual and expected number of banks for the memory devices of the memory module system. Combining this teaching with Amidi's suggestion to use other types of memory devices (Amidi ¶ 71) would have predictably yielded the recited "both the bank address signals of the set of input control signals are received by both the logic element and the register" in claim 7 so that the necessary rank chip select signals discussed in Amidi are produced. That is, Amidi and Dell 2, collectively, teach that ranks and banks both may be expanded; therefore, a skilled artisan would recognize various combinations of inputs to achieve expansion including bank address inputs as broadly recited. This combination also addresses the demand for increased memory capacity and compatibility issues. *See*, *e.g.*, R2 August 14, 2013 Comments 12 (citing 3d Bagherzadeh Decl. ¶ 37), 29–30, 38 (citing Amidi ¶ 71). Moreover, this combination further teaches using the logic circuit or element (e.g., Amidi's CPLD) to receive bank address signals for the above-discussed purpose.

Finally, we agree with the Examiner's findings and conclusion concerning the evidence of secondary considerations not outweighing the case for obviousness. RAN 65–66.

Accordingly, for previously stated reasons, we sustain the adopted rejection of claims 7, 26 and 33 based on Amidi and Dell 2 under § 103.

Copied from 95000579 on 02/08/2017

B. *Claims 2, 5, 21, 23, 30, and 119 (Claims with the Storing Limitation) wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.*

1. Anticipation Rejection Based on Amidi (Ground 3)

Claims 2, 5, 21, 23, 30, and 119 have been rejected under 35 U.S.C. § 102 based on Amidi. RAN 22–26. Patent Owner argues these claims as a group. PO App. Br. 25–38. We select claim 21 as illustrative. Notably, claim 21 requires the circuit to be configured to store an input signal without reciting the type of input signal stored or the location within the circuit where the signal is configured to be stored.

To teach the "storing" limitation, the Examiner refers to (1) Amidi's Figure 6A, (2) the input signal RAS into the registers transmitted as rRAS, (3) Add(n) discussed in paragraph 52, and (3) Requester 2's Comments filed March 30, 2012 discussing using Add(n) as an input into CPLD 604 to generate rcs2 and rcs3, which Requester 2 contends are needed for the duration of the read/write cycle. RAN 24–25 (addressing both claims 2 and 21). The Examiner also adopts Requester 1 and 2's proposed rejections (RAN 22 (indicating proposed rejection by Requester 1 and 2 are adopted for claim 21)), which include a discussion of paragraph 61 of Amidi. *See, e.g.,* R2 Request 997 (citing Amidi ¶ 61). Thus, although Patent Owner asserts that the Examiner repeatedly relies on an input RAS signal being stored in a register and transmitted as output rRAS signal (PO App. Br. 32–33), we determine that this is only *part* of what the Examiner cites in formulating the rejection. *See also* R2 Resp. Br. 16.

Requester 1 contends Patent Owner is focusing on an improper low level of skill in the art, where the ordinary artisan would "blindly follow certain JEDEC

Copied from 95000579 on 02/08/2017

standards." R1 Resp. Br. 12. As stated above, we agree that Amidi is not JEDEC compliant in all aspects of its memory module design and thus one skilled in the art would not have followed all of the design specifications discussed in JEDEC designs.

Requester 1 also asserts that an ordinary artisan would have been familiar with DDR2 devices "which supports posted CAS [column access strobe] commands" and a DDR2 SDRAM memory controller will "treat a row activation command (part of a row access procedure) and a column access command as a unitary command pair to be issued in consecutive cycles." R1 Resp. Br. 13 (citing Wang Decl. ¶ 22). Requester 1 presumably contends that a posted CAS command is an input signal stored during a row access procedure for subsequent use during a column access procedure. *Id.* Yet, even assuming that Requester 1 is correct, this contention does not address sufficiently where the command or signal is stored. *Id.* In particular, Requester 1 states that the entire CAS command would be posted (e.g., stored) in the memory device (e.g., the DRAM device)— not the circuit recited as a separate component from the memory devices in claim 21. *See* PO Reb. Br. 22–23; Wang Decl. ¶ 22. Thus, even assuming that the RAS and CAS commands are treated as a unitary command and stored in memory devices (R1 Resp. Br. 13), there is insufficient disclosure that Amidi's circuit—separate from the memory devices — is configured to store input signals during a row access procedure for a subsequent column access procedure as recited.

Requester 2 contends Amidi discloses the "storing" feature in claim 21 when registering the row address for use with the column address in a separate cycle. R2 Resp. Br. 12–13 (citing Amidi ¶¶ 38, 61[20]). Amidi specifically discusses internal

[20] Requester 2 mistakenly referred to paragraph 60. R2 Resp. Br. 12.

Copied from 95000579 on 02/08/2017

circuity within a CPLD for Row Address Decoding (e.g., a row access procedure) and Column Address Decoding (e.g., a column access procedure). Amidi ¶ 61, *cited in* R2 Resp. Br. 12 and R2 Request 997. Here, Amidi states the column address decoding scheme is unique, requiring two sets of addresses rather than the standard DDR memory module where only one set of address lines is required in order to access a cell. Amidi ¶ 61. Amidi even further states the first set includes the row address provided with proper control and command signals and the second set, on a separate cycle, includes the column address provided with its proper control and command signals in order to read or write "to that particular cell." *Id.*

Although both the row and the column address require "control and command signals" (*id.*; *see* R2 Resp. Br. 12–13), Amidi does not discuss explicitly storing the proper control and command signals (e.g. input signals) during a row access procedure for later use during a column access procedure. Amidi ¶ 61. Amidi also does not state explicitly which "control and command signals" are used during each step. *See id.*

Amidi further states register 408, which is considered part of the recited circuit in claim 21, "may eliminate the loading of 36 devices in case of stacking or loading of 18 devices in case of monolithic memory devices from the main controller by separating the controller side signaling with memory side signal loading fan-out." Amidi ¶ 38, *cited in* R2 Resp. Br. 11. We fail to find a discussion of how the register stores signals *during a row access procedure* for subsequent use during a column access procedure. *Id.* Nor do we determine that eliminating loading of memory devices as discussed in Amidi implies that a logic element will inherently store the information during a row access procedure for subsequent use during a column access procedure as recited in claim 21.

Copied from 95000579 on 02/08/2017

Turning to cited paragraph 52, Amidi discusses generating signals (e.g., rcs0–rcs3) that exit CPLD 604 from the input signals (i.e., CS0, CS1, and Add(n)) to "ensure[] that all command for a two rank memory module . . . are also performed on the four rank memory modules." Amidi ¶ 52, *cited in* RAN 24–25. Amidi discusses generating rcs0-rcs3 signals, when various CS0 and CS1 commands are issued (e.g., Auto Precharge all Banks, Auto Refresh, Load Mode Register). *Id.* Yet, Requesters 1 and 2's proposed rejection, adopted by the Examiner, have not demonstrated sufficiently that the input signals (e.g., CS0, CS1, or Add(n)) are necessarily stored in part of the circuit (e.g., CPLD) during a row access procedure for later use during a column access procedure. As Patent Owner indicates, the Add(n) signal enter an OR logic in Figure 8 and then a multiplexer along with other signals. PO Reb. Br. 24–25 (citing Amidi ¶¶ 69–70, Fig. 8 (logic 812, 814)).

Although Requester 2 states that its rejection does not rely on the concept of inherency (R2 Resp. Br. 18), Patent Owner further discusses the "storing" claims in the context of inherency, asserting that Requester 2 is incorrect. PO App. Br. 34–36 (citing Requester 2's March 2012 Comments); PO Reb. Br. 25–26. In a nutshell, Requester 2 contends that Dr. Bagherzadeh's testimony supports that "the missing descriptive matter, *i.e.*, storing, is necessarily present." R2 Resp. Br. 19–20. We agree that this discussion relies on the concept of inherency and that Amidi's circuit necessarily at least temporarily stores an extra row address bit that is received in order to identify the correct memory device. R2 Resp. Br. 18–20 (citing 2d Bagherzadeh Decl. ¶ 22); *see also* PO App. Br. 35 (citing 2d Bagherzadeh Decl. ¶ 22).

Copied from 95000579 on 02/08/2017

However, Requester 2 presents insufficient evidence to support that Amidi's circuit *must* store the extra row address bit during a row access procedure for later use during a column access procedure. Whether Amidi's disclosure demonstrates that storing the bit between these procedures is probable or possible is not sufficient for an anticipation rejection. *See Robertson*, 169 F.3d at 745. Additionally, Patent Owner offers the testimony of Dr. Kozyrakis which describes at least two possible options (e.g., store an address bit for subsequent use during a column access procedure *or* store resulting signals— not the input address signals— from a decoding process) that one skilled in the art would have been aware of to address how Amidi's four rank memory module can emulate a two rank memory module. 2d Kozyrakis Decl. ¶ 33, *cited in* PO App. Br. 35.

Lastly, Requester 3 discusses Amidi only in the context of the obviousness, thus alluding to Requester 3's position that Amidi alone or in combination with at least one additional reference suggest or teach the storing limitation in claim 21 but does not anticipate the disputed features of claim 21. *See generally* R3 Resp. Br.

We therefore determine the Examiner erred in rejecting (1) claim 21, (2) claims 2, 5, 23, 30, which recite similar limitations, and (3) claim 119, which depends from claim 2, based on Amidi under § 102.

Because we determine Amidi does not anticipate claim 21, we need not reach whether Amidi is enabled for the storing limitation. PO App. Br. 36–38; PO Reb. Br. 32–34.

Copied from 95000579 on 02/08/2017

2. Obviousness Rejection Based on Amidi Alone or in Combination with JEDEC (Grounds 4 and 6)

Turning to the obviousness rejection of illustrative claim 21 based on Amidi, we initially note that "[a] non-enabling reference may qualify as prior art for the purpose of determining obviousness under [35 U.S.C.] § 103." *In re Antor Media Corp.*, 689 F.3d 1282, 1288, 1292 (Fed. Cir. 2012) (quoting *Symbol Techs. Inc. v. Opticon Inc.*, 935 F.2d 1569, 1578 (Fed. Cir. 1991)); *see also Beckman Instruments v. LKB Produkter AB*, 892 F.2d 1547, 1551 (Fed. Cir. 1989) (stating "[e]ven if a reference discloses an inoperative device, it is prior art for all that it teaches.") Thus, although Patent Owner argues Amidi is not enabled (PO App. Br. 36–38), Amidi is available as prior art for all that it teaches in the context of the adopted obviousness rejections.

Patent Owner repeats the argument that one skilled in the art would have adhered to the conventional JEDEC design standards. PO App. Br. 26–33; PO Reb. Br. 19. We are not persuaded for reasons previously discussed. As such, we determine that one skilled in the art would have recognized that at least some Amidi's input signals into the circuit of the memory module deviate from some of JEDEC's design conventions.

Moreover, in Grounds 4 and 6, the Examiner refers to the discussion of Ground 3. RAN 28, 33. As noted above, we determine that in formulating the rejection based on Amidi, the Examiner addresses various input signals, including Add(n), and control and command signals discussed in paragraph 61, in determining that input signals are stored during a row access procedure for later use in a column access procedure. RAN 25 (discussing address signal is needed for the duration of the read/write cycle); *see also* R2 Resp. Br. 16. The Examiner

Copied from 95000579 on 02/08/2017

further refers to pages 32 through 35 of Requester 2's Comments filed March 30, 2012 when rejecting claim 21. RAN 25. We thus disagree with Patent Owner's argument that the rejection only discusses storing an input RAS signal. PO App. Br. 32–33; PO Reb. Br. 19–21.

Turning to the storing of address signals and "proper control and command signals" for use during a column access procedure as discussed in Amidi, Patent Owner argues that "Amidi's register 408 appears to have conventional DDR command operation, including the conventional DDR one-clock-cycle, single-use operating principle." PO Reb. Br. 24 (underlining omitted). That is, in Patent Owner's view, each DDR operation (e.g., active, read, write) has its own complete instantiated set of signal values and each is handled for a single cycle only. PO App. Br 26–27, 29. As such, Patent Owner asserts that all input values are discarded and replaced in a subsequent command such that no values are stored for subsequent use. PO App. Br. 27–28, 31–32 (citing 2d Sechen Supp. Decl. ¶¶ 65–66).

As discussed above, we determined that Amidi is not a conventional DDR memory module in accordance with all JEDEC design specifications. We further note that even Patent Owner does not commit to Amidi using conventional DDR commands. PO Reb. Br. 24 (stating "Amidi's register 408 *appears* to have a conventional DDR command operation") (emphasis added). Amidi further supports that it is not conventional. *See* Amidi ¶¶ 8, 11–12, *cited in* R3 Resp. Br. 7 (stating "[c]ontrary to the assertions by the Appellant, a person of ordinary skill would understand that Amidi's non-standard module <u>must</u> deviate from standard DDR command processing in order to operate properly."). Based on the above

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discussion, the record has not illustrated adequately that Amidi behaves conventionally in accordance with JEDEC.

Patent Owner further contends that the input signals in Amidi are eliminated every cycle from Amidi's register 408 and 418 and adhere to JEDEC 79C design specifications. PO App. Br. 26–29; *see* 2d Sechen Decl. ¶¶ 65, 69; 3d Kozyrakis Decl. ¶ 13. Even presuming that Patent Owner is correct, registers 408 and 418 are not the only part of Amidi's memory module circuit that is separate from the memory devices. For example, Amidi's memory module circuit also includes at least a CPLD (e.g., 410 or 610). Amidi, Figs. 4A, 6A.

Amidi states that during row address decoding, the first address set is provided with proper control and command signals. Amidi ¶ 61. Amidi further states that, on a separate cycle, the column address decoding provides the second address set that includes its proper control and command signals in order to read or write "to that particular cell." *Id.* Although we indicated above that control and command signals used during row and column address decoding are not disclosed as being necessarily the same signals (*id.*), Amidi teaches that the later column address decoding step "needs to be provided with its proper control and command signals in order to read or write *to that particular cell*." *Id.* (emphasis added).

We determine that Amidi's teaching suggests that the *proper* control and command signals to read or write to the particular cell (e.g., address and bank address signals) would involve at least some of the same signals received during the row address decoding step, when applying the background and creative steps one skilled in the art would have employed. *See* R2 Resp. Br. 12–13; R3 Resp. Br. 8–9. As such, one skilled in the art would have recognized that some efficiencies are to be gained from designing a circuit that stores input signal values during a

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row access decoding procedure that are also *used later* during a column access decoding procedure. Additionally, there are a finite number of identified, predictable solutions (e.g., repeat or store values) for using the same signal values from one procedure to another (e.g., row to column) and one skilled in the art would have reasons to pursue these known options (e.g., design and processing considerations) in order to read or write to the correct cell at the column address step.

To illustrate this point, we refer to Truth Table 1a in JEDEC 79C. JEDEC 79C 12, *reproduced at* 2d Sechen Decl. ¶ 65. Some of the signals in Truth Table 1a or certain command/control signals are the same. *Id.* For example, each of an ACT or active command (e.g., a row access procedure) and a RD or read command (e.g., a subsequent column access procedure) have the same bank address (e.g., Bank under ADDR) and chip select signals (e.g., L under CS). *Id.* JEDEC 79C also explains READ or WRITE commands occur after ACTIVE commands and are issued "to that row." JEDEC 79C 21. JEDEC 79C even further discusses a subsequent ACTIVE command to a different row in the same bank can be only issued after the previous row has been closed. *Id.*

Patent Owner also identifies Bank Y values that are the same for the ACT and RD/WR commands. PO App. Br. 27 (discussing Figure 9 of JEDEC 79C); *see also* JEDEC 79C 21. This table along with Amidi's teaching in paragraph 61 suggest to one skilled in the art that some signals for both row access procedures and column access procedures are the same. Given that some of the values do not change between procedures (e.g., row and column address procedures), the teachings further suggest to an ordinary skilled artisan employing background knowledge and creative steps that Amidi's memory module can benefit (e.g., less

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Petitioners
Ex. 1016, p. 55

processing) from storing unchanged values for later use. *See, e.g.*, R3 Resp. Br. 7, 11–12 (citing 3d Kozyrakis Decl. ¶¶ 18–19 and 2d Kozyrakis Decl. ¶ 33).

As such, Amidi alone or in combination with JEDEC teach or suggests a circuit "configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure" as recited in claim 21. Thus, although not disclosing storing input signals explicitly as explained previously, JEDEC designs suggest a benefit to storing such signals for later use, and in particular, the combined teachings of the references suggest to a skilled artisan that modifying Amidi's CPLD, to the extent necessary, to store an input signal (in particular, an input signal used to perform expansion) during a row access procedure for subsequent use during a column access procedure would have been obvious.

Even more, Requester 2 discusses that the Truth Table in Amidi's Figure 5 shows storing the address signals, including transition bits, to determine the active rank. March 30, 2012 Requester 2 Comments 34–35. In order to determine the same rank during a later column access, Requester 2 argues that Amidi suggests storing relevant information. *See id.* Requester 3 similarly asserts that rank-multiplying memory modules must store information from the row access procedure to match later with the column access procedure that completes a read operation (e.g., while the row remains open) due to interleaving techniques. R3 Resp. Br. 5 (citing 3d Kozyrakis Decl. ¶¶ 15–19 and 2d Kozyrakis Decl. ¶ 33). Requester 3 indicates the proper bank is identified by using chip select and bank address signals. 3d Kozyrakis Decl. ¶ 17. But, in a rank-multiplying memory module, Requester 3 identifies that incoming bank and address signals are not

Copied from 95000579 on 02/08/2017

sufficient to identify the bank for the CAS command. R3 Resp. Br. 7 (quoting 3d Kozyrakis Decl. ¶ 18).

Dr. Kozyrakis testifies that a designer would have recognized in a rank-multiplying scheme, for every "activate, read or write command" issued, the controller of the memory module must identify a bank using bank address and chip select signals, and if the command is a CAS command, the controller must further identify the open row to execute the command using the same bank and chip select signals. 3d Kozyrakis Decl. ¶ 18. Dr. Kozyrakis states this can be achieved by using an address bit of the RAS command, which is later free to be used for this purpose during the CAS command because the address bit is not provided with the CAS command. 3d Kozyrakis Decl. ¶ 19 and 2d Kozyrakis Decl. ¶33, *cited in* R3 Resp. Br. 7–9; Sechen Decl. ¶ 96 (stating that in Amidi the row address bit is not available during column access command). This is further echoed by Requester 2 as indicated by Patent Owner. Requester 2's March 30, 2012 Comments 32–35 (citing 2d Bagherzadeh Decl. ¶¶ 21–22).

Given the record, we agree that one skilled in the art would have recognized the column access procedure for an open row occurs subsequent to a row access procedure and needs to be matched. We further determine, employing inferences and creatives steps, one skilled in the art would have recognized that storing and using previous input signals having information that is needed for subsequent column procedures would have improved Amidi's memory module design. And even though Dr. Kozyrakis offers two alternative options for generating the correct chip-select and bank address signals, we determine that both options, including storing an address bit from a row access procedure for use during a subsequent

Copied from 95000579 on 02/08/2017

column access procedure, were known by ordinary artisan. 2d Kozyrakis Decl. ¶ 33, *quoted at* PO App. Br. 35.

We also disagree that Dr. Kozyrakis's testimony conflicts with Dr. Bagherzadeh's. PO App. Br. 36. Rather, as discussed above, Dr. Kozyrakis provides alternatives ways of storing values— one of which is storing input values within the memory module's circuit as recited in claim 21.

Patent Owner contends that Requester 3's position is flawed. PO Reb. Br. 28. In particular, Patent Owner contends that the teachings come from Requester 3 (e.g., Dr. Kozyrakis) and not from Amidi. We find no error in formulating an obviousness rejection based on what one skilled in the art would have recognized given Amidi as well as one's inferences and the creative steps an artisan would have employed rather than precise teachings from Amidi. *See KSR*, 550 U.S. at 418. Nor do we determine that the position taken by Requester 3 is based on impermissible hindsight. PO Reb. Br. 28–30. For example, as discussed above, Amidi and JEDEC suggest that at least some of the same proper control and command signals are needed during both a row and column address procedure in order to isolate, read from, and write to the desired particular cell, such that storing relevant input signal values (e.g., bank address signal) for later use would create design efficiencies and benefits. *See* Amidi ¶ 61.

Patent Owner further argues that storing the address bit for subsequent use during a column access procedure introduces a new principle of operation to and intended purpose for Amidi's address bit and further argues that Requester 3's position implies that the storing necessarily occurs. PO Reb. Br. 28. We disagree. First, Requester 3's comment concerning Amidi are in the context of an obviousness rejection— not anticipation where features must be necessarily

Copied from 95000579 on 02/08/2017

present in one prior art reference. Second, Patent Owner does not demonstrate adequately that introducing a purportedly new operation into Amidi would teach away from Amidi, render Amidi inoperable, or destroy Amidi's device intended purpose. Moreover, as Requester 3 notes, such storage may "require storing only a single bit," further illustrating that if such design modifications are needed to Amidi, they are minor. R3 Resp. Br. 10.

Patent Owner further contends that the modification proposed by Requester 3 of Amidi "could not have been a predictable solution." PO Reb. Br. 30 (emphasis omitted). Rather, pointing to Dr. Kozyrakis' testimony, Patent Owner contends that there are barriers to overcome, including DDR standard-compliance and verification. *Id.* (citing 4th Kozyrakis Decl. ¶¶ 15–21). We are not persuaded. As stated previously, we disagree that Amidi is a DDR standard memory module. As a result, while we do not determine that an ordinarily skilled artisan would have necessarily performed every step discussed in Dr. Kozyrakis' testimony (4th Kozyrakis Decl. ¶¶ 15–21), we agree that some implementing, testing and verification of a logic circuit design would be commonplace to an ordinarily skilled artisan and not beyond this person's skill (*see* 4th Kozyrakis Decl. ¶ 21).

Concerning whether there is a reasonable expectation of success that the stored address bit in Amidi will perform as recited, Patent Owner repeats that such a change would create barriers to the "identified DDR standard-compliance and verification." PO Reb. Br. 30. Patent Owner also repeats the assertion that the modification introduces a new principle of operation. PO Reb. Br. 30–31. We are not persuaded for the above-stated reasons.

Further, Patent Owner contends that Dr. Kozyrakis' testimony demonstrates no reasonable expectation. PO Reb. Br. 31–32. Specifically, Patent Owner asserts

Copied from 95000579 on 02/08/2017

that Dr. Kozyrakis anticipates a mistake when designing a logic circuit that would require storage of an address bit as proposed by Requester 3 and thus teaches away from storing the address bit. PO Reb. Br. 31 (citing 4th Kozyrakis Decl. ¶ 23). We are not persuaded. Dr. Kozyrakis testifies to two mistakes that could occur when remapping logic in its circuit during simulation. 4th Kozyrakis Decl. ¶¶ 22–23. This does not imply there is no reasonable expectation of success of storing an address bit. Rather, Dr. Kozyrakis is highlighting what would occur during functional verification if the logic circuit designer made the identified mistakes. *Id.* Conversely, this paragraph implies that if the mistakes do not occur (e.g., address bit is stored) a successful and error-free simulation will result with proper verification. *See id.*

Finally, we agree with the Examiner's findings and conclusion related to the evidence of secondary considerations not outweighing the case for obviousness. RAN 65–66.

Based on the record, the Examiner has not erred in rejecting claims 2, 5, 21, 23, 30, and 119 when considering the background knowledge of an ordinary skilled artisan or Amidi in combination with JEDEC.

3. *Obviousness Based on Amidi and Dell 2 (Ground 5)*

For this ground, the Examiner adopts the proposed rejection of claims 2, 5, 21, 23, 26, and 30, referring to Requesters 1 and 2 as modified on August 14, 2013. *See* RAN 12. As explained above, we thus disagree with Patent Owner that Requester 2's remarks for this ground are improper. PO Reb. Br. 40. Also, according to the Examiner, Requester 1 proposed to reject claims 2, 5, 21, 23, and 30 on this ground, and Requester 2 proposed to reject other claims. RAN 30; *see also* R1 February 13, 2013 Comments 11–16 and R2 August 14, 2013 Comments

Copied from 95000579 on 02/08/2017

5–17 (citing Amidi ¶¶ 8, 40–43, 45–52, 71; Dell 2, Abstract, 2:40–3:5, 4:62–6:14, 8:5–64; 3d Bagherzadeh Decl. ¶¶ 12–17, 21–22, 24, 26, 37; and 2d Bagherzadeh Decl. ¶ 25).

As a preliminary matter, Requester 1 contends that claim 119 was missing from the Examiner's listing of its claims proposed to be rejected under Ground 5. R1 Resp. Br. 14 (citing RAN 30). Claim 119 is also missing in the summary of the adopted grounds. RAN 12 (omitting claim 119 from Ground 5). Even so, Requester 1 asserts that claim 119 should also be adopted due to the Examiner's statement that Amidi and Dell 2 is obvious because the claims are anticipated by Amidi. R1 Resp. Br. 14. Requester 1 also contends that it proposed to reject claim 119 based on Amidi and Dell 2 in its "response to the Second Office Action" at pages "43-48."[21] R1 Resp. Br. 14 n.3. Patent Owner contends that claim 119 has not been rejected. PO Reb. Br. 38. The Examiner fails to comment on the status of claim 119 in the Examiner's Answer.

Upon review, we agree that Requester 1 did propose to reject claim 119 based on Amidi and Dell 2 and that claim was omitted from the Examiner's listing of the proposed rejection in the RAN. R1 February 13, 2012 Comments 43–44; RAN 30 (listing only claims 1–43 and 45–50 when addressing Requester 1). Even so, the adopted rejection does not include claim 119. RAN 30. We thus ultimately agree with Patent Owner that claim 119 has not been rejected under Ground 5.

Turning to the merits of the rejection, Patent Owner does not address Dell 2 in its opening brief. *See generally* PO App. Br. In its rebuttal brief, Patent Owner contends that the rejection "presumably relies on Amidi's teachings alone as the

[21] We assume this response is Requester's Comments filed February 13, 2012 entitled "THIRD PARTY REQUESTER COMMENTS AFTER NETLIST RESPONSE TO THE SECOND OFFICE ACTION."

Copied from 95000579 on 02/08/2017

Examiner found the combination of Amidi and Dell 2 deficient." PO Reb. Br. 14 (citing RAN 30). We disagree. Although some portions of the RAN discussed that claims 2, 5, 21, 23, 30, and 33 are rejected based on Ground 3 (RAN 30), the Examiner adopts the proposed rejection of Requesters 1 and 2 as modified on August 14, 2013, which is the date Requester 2 filed comments, in other portions as previously explained. *See* RAN 12.

Accordingly, when viewing the RAN as a whole, the adopted rejection does not just rely on Amidi, but also on Dell 2. We therefore determine that the Examiner has adopted Requester 2's proposed rejection, including that concerning the "storing" feature. Moreover, any discussion related to Requester 1 and a lack of motivation to combine Amidi with Dell 2 (RAN 31) is addressed in the context of the non-adopted rejection of other claims based on Amidi and Dell 2.

As for the pending rejection, we refer to the reasoning above concerning Amidi, Dell 2, the background knowledge of one skilled in the art, and inferences and creative steps one skilled in the art would have employed. Additionally, regarding Dell 2, we refer to the further findings discussed by Examiner. *See* RAN 12, 32 (discussing Dell 2, 2:48–59); Requester 2's August 14, 2013 Comments 60–61 (referring to claim 2), 40–41 (citing Dell 2 8:36–41, which discusses the need to store bank address values applicable to each option). That is, Dell 2 also teaches that one skilled in the art would have recognized storing signals for later use, including during a column access procedures, to ensure the correct bank is addressed. Dell 2 8:36–40. Moreover, Requester 2 provides additional explanation concerning this rejection and Dell 2, which is essentially undisputed. R2 Resp. Br. 21–22.

Copied from 95000579 on 02/08/2017

Patent Owner also refers to its arguments in its Respondent Brief to Requester 1's appeal. PO Reb. Br. 39 (citing PO-R1 Resp. Br. 12–20). The arguments essentially repeat the discussions above concerning standard and compliant memory modules, how bank addresses are used in JEDEC designs, and there is no reason provided to combine the references. PO-R1 Resp. Br. 12–16. We are not persuaded for reasons previously discussed. That is, as discussed above, the combined teachings of the references suggest to a skilled artisan that modifying Amidi's CPLD, to the extent necessary, to store an input signal (e.g., an input signal used to perform expansion) during a row access procedure for subsequent use during a column access procedure would have been obvious.

Finally, we adopt the Examiner's findings concerning secondary considerations evidence not outweighing the case for obviousness. RAN 65–66.

Accordingly, we are not persuaded that the Examiner erred in rejecting claims 2, 5, 21, 23, 30, and 33 based on Amidi and Dell 2.

II. Micron and Amidi (Ground 13)

A. Claims 7, 26, and 33 (Claims with Bank Address Limitation)

Claims 7, 26, and 33 are even further rejected based on Micron and Amidi. RAN 14 (referring to Requester 3's proposed rejection). The Examiner refers to Grounds 3 through 6 and states that "[b]ecause these claims are anticipated or rendered obvious by Amidi they are obvious over Micron and Amidi." RAN 49. The Examiner also provides an alternative rejection. RAN 49–52 (stating "[a]lternatively" at RAN 49); November 13, 2012 Non-Final Act. 45–48. This alternative rejection does not specifically discuss Amidi when addressing claims 7, 26, and 33, but discusses Amidi's teaching of creating a four rank transparent memory module fitting into a memory socket intended for two ranks. RAN 51–52.

Copied from 95000579 on 02/08/2017

For claims 7 and 33, the Examiner also adopted the proposed rejection by Requester 3 that discusses Amidi's teachings and Dr. Kozyrakis's testimony. RAN 14 (indicating Requester 3's proposed rejection is adopted). That is, Requester 3 proposes that Amidi teaches the recited bank address limitation or alternatively one skilled in the art would have known to modify Amidi's CPLD to receive the input signals as recited for purposes of decoding and remapping signals. R3 Request 18–20 (referring to the claim chart in Appendix H), App'x. H, H-14–H-15, H-46.

Patent Owner only presents argument concerning Micron and Amidi individually. PO App. Br. 17–25, 32–34, 44, 46–47. We are not persuaded by such individual attacks. *See In re Merck*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). That is, the arguments that focus exclusively on Micron do not consider the collective teachings of Micron and Amidi as well as what an ordinarily skilled artisan would have recognized. For the previous set forth reasons, we are not persuaded of error by the Examiner and refer to the above discussion concerning Amidi. As discussed previously when addressing Ground 4 based on Amidi, which is referred to the RAN under Ground 13 (RAN 49), we determined that Amidi, when considering its teaching and the background knowledge of an artisan, suggests bank address signals being received by both a logic element and register. Also, as indicated above, claim 33 is anticipated by Amidi.

Moreover, Dr. Kozyrakis states that one skilled in the art would have recognized DDRs, like Amidi's (Amidi ¶¶ 37, 46–49) follow different generation specifications (e.g., DDR-1, DDR-2). Kozyrakis Decl. ¶ 26. Similarly, the '912 disclosure also discusses existing DRAMs at the time of the invention include DDR-1, DDR-2, and DDR-3. The '912 patent 6:15–16, 12:26–27. Dr. Wang acknowledges the same. Wang Decl. ¶ 29. Concerning DDRs, Dr. Kozyrakis

Copied from 95000579 on 02/08/2017

states an ordinary skilled artisan would have known more recent DDR-2 devices have a bank address field that is 3 bits rather than the conventional two bits used by DDR-1 devices, for example. Kozyrakis Decl. ¶ 26. Patent Owner does not rebut this finding. PO Reb. Br., PO-R3 Resp. Br.

Thus, Requester 3 provides additional evidence that one skilled in the art would have recognized, when using a more recent DDR-2 memory device, bank address signals are free in certain situations for address remapping in particular memory module designs. That is, like Amidi's teaching of using an extra row/column address bit for generating the proper chip-select signals (e.g., rank expansion) for emulating a two rank memory module (Amidi ¶¶ 51, 59), Dr. Kozyrakis provides a reason with some rational underpinning that an ordinary skilled artisan would have used other known, extra address bits (e.g., the extra bank address in more recent DDR devices) to create the desired rank expansion in Amidi by directing such extra signals to Amidi's CPLD.

Patent Owner argues that "bank address signals are not treated in the same way as row and column address signals." PO App. Br. 17 (citing Sechen Decl. ¶¶ 36, 48). Specifically, Patent Owner contends that bank address signals are used to supply certain initialization values to various control registers within DDR DRAM devices, including three identified purposes— (1) define a bank that a read, write, active, or precharge command is applied, (2) program a mode register used to define specific mode operations of a DDR SDRAM, and (3) to identify banks for deactivating an open row during a precharge command). *Id.* (citing Sechen Decl. ¶¶ 36, 48); *id.* at 13–14 (referring to JEDEC 79C 6–7, 11–12, 20). According to Patent Owner, one skilled in the art would not have recognized using bank address signals in a way other than that described by Patent Owner and

Copied from 95000579 on 02/08/2017

JEDEC 79C, such as directing bank address signals to a CPLD, and such use would result in failure. PO App. Br. 13–17. We are not persuaded.

We have been referred to no evidence of record to support the opinion testimony of Dr. Sechen that directing bank address signals to CPLD would result in failure in Amidi. *See* Sechen Decl. ¶¶ 36, 48. Nor has Patent Owner presented persuasive evidence on this record to provide that the modifications made to Amidi would have been beyond the level of an ordinarily skilled artisan. As such, we agree with Requester 3 that the functionalities of the bank address "would not present a barrier to [implementing] the techniques discussed in the [Patent Owner's] appeal brief." R3 Reb. Br. 2; *see also* R3 Resp. Br. 11–12 (citing 4th Kozyrakis Decl. ¶¶ 16, 19–23).

Additionally, in that the signals connections in Amidi's Figure 6A differ from Figure 6B. Amidi, Figs. 6A–6B, *cited in* Wang Decl. ¶ 20. Specifically, Amidi shows an address signal (e.g., Add(n)) entering CPLD 604 and a different address signal (e.g., Add[n-1:0]) entering register 608 in Figure 6A. Amidi ¶ 50–52, Fig. 6A. Amidi also shows address signals (e.g., Add[n:0] or A0-12) entering register 608 and one of the same address signals (e.g., Add(n-1) or A11) also entering CPLD 604 during a column address decoding. Amidi ¶ 57–60, Fig. 6B. These differences illustrates two points.

First, Amidi teaches and suggests address signals are being used in a manner that deviate from JEDEC specifications. For example, JEDEC 21-C states address signals are used to define row and column addresses during bank and read commands. JEDEC 21-C 4.20.4-7. But, Amidi uses an extra row or column address signal as an input to the CPLD to generate a rank chip-select signal for emulating a two rank memory module. Amidi ¶¶ 50–52, 57–60, Figs. 6A–B.

Copied from 95000579 on 02/08/2017

Thus, an ordinary skilled artisan in logic circuit design would have recognized based on Amidi's teaching to use address signals in an unconventional manner. Second, Amidi also teaches using the same column address signal (e.g., A11) in a memory module for multiple purposes. For example, Amidi teaches in Figure 6B using an address signal (e.g., A11) both to be inputted into a register (e.g., to determine the column within the memory device) and to be inputted into a CPLD (e.g., to select the proper rank). Amidi ¶¶ 57–60, Fig. 6B. Thus, Amidi also illustrates to one skilled in the art that address signals can have multiple purposes.

Granted, the address signals discussed in Amidi are row or column address signals— not the recited bank address signals. But, Dr. Kozyrakis' testimony discussed above concerning certain known DDRs would have an extra bank address bit, coupled with the recognition in the '912 patent that these DDRs existed, provides a reason with some rational underpinning to an ordinarily skilled artisan to use a bank address signal in a manner similar to the Amidi's free row/column address signals. We determine Requester 3 provides adequate evidence that one skilled in the art having (1) at least an undergraduate degree in either electrical engineering, computer engineering, or in a closely related discipline, (2) at least two years of experience in designing computer memory systems, and (3) familiarity with JEDEC standards, DRAMS, and DIMMS would have recognized using bank address signals in a manner similar to the row and column address signals taught as being received by Amidi's CPLD.

Patent Owner also refers to previous comments made in its respondent brief to Requester 3. PO Reb. Br. 12–13 (citing PO-R3 Resp. Br. 12–20). Although addressing the rejection based on Micron and Amidi (Ground 13) on page 12 through 20, many of the arguments concerning Amidi are similar to those above

Copied from 95000579 on 02/08/2017

and have been address previously. *See, e.g.,* PO-R3 Resp. Br. 14–16. Patent Owner also asserts that using a third address bit would present barriers with DDR standard-compliance and cast doubt on a reasonable expectation of success. *See* PO-R3 Resp. Br. 16–20. But, as stated above, Amidi's memory module is not JEDEC compliant. Thus, even if the third address bit is used for other purposes, we explained above that this does not establish that one of ordinary skill would not have recognized also using a free, third address bit in an address remapping scheme. Nor has Patent Owner presented persuasive evidence on this record to provide that the modifications made to Amidi would have been beyond the level of an ordinarily skilled artisan. *See* PO-R3 Resp. Br. 19–20 (citing 2d Kozyrakis Decl. ¶ 25).

According to Patent Owner, both Examiners Choi and Peikari dismissed the position taken by Requester 3. PO Reb. Br. 13. We disagree. As stated previously, the discussion in the Non-Final Action mailed October 14, 2011 was directed to Requester 1's proposed rejection and evidence — not Requester 3. *See* Non-Final Act. 15–16 (discussing Requester 1's proposed rejection). This however does not demonstrate that examiners have dismissed *Requester 3*'s proposal to modify Amidi's CPLD to receive bank address signals. Notably, as discussed above, the record for Requester 3 provides some additional evidence, not presented by Requesters 1 or 2, that one skilled in the art would have recognized, when using a more recent DDR-2 memory device, bank address signals are free in certain situations for address remapping in particular memory module designs. Accordingly, although we determine that Requester 1 and 2's adopted rejections and evidence does not demonstrate that bank address signals are received by Amidi's CPLD (e.g., a logic element), we determine that Requester 3 has provided

Copied from 95000579 on 02/08/2017

additional evidence sufficient to demonstrate that one skilled in the art would have recognized using extra bank address signals to be received by Amidi's CPLD for a remapping scheme to generate the needed rank signals.

Given that one skilled in the art have recognized that: (1) Amidi is unconventional memory module that is not compliant with JEDEC design specifications in various ways, (2) Amidi teaches emulating memory module having a lower rank of the memory devices by using extra address signals to generate the necessary chip-select signals for the actual memory device, (3) Amidi teaches address signals, including bank address signals, have multiple purposes, and (4) some DDR devices include bank address bits that are free to be used in certain situations, we determine that an ordinarily skilled artisan would have known to direct bank address signals to Amidi's CPLD in a similar manner to the row/column address signals explicitly taught by Amidi. As such, we disagree with Patent Owner that the record does not demonstrate to direct bank address signals to Amidi's CPLD such that they are received by both a register and a logic element (e.g., CPLD) as recited in claim 7.

Lastly, we adopt the Examiner's findings and conclusion concerning the secondary considerations not outweighing the case for obviousness. RAN 65–66.

Accordingly, we are not persuaded that the Examiner erred in rejecting claims 7, 26, and 33 based on Micron and Amidi.

B. Claim 21 (Claim with Storing Limitation)

As for claim 21, the proposed rejection for Requester 3 is similar to those for Requesters 1 and 2. *See* RAN 49 (referring to Grounds 3–6) and R3 Request, App'x H, H-29–H-30 (citing Amidi ¶ 61 and Kozyrakis Decl. ¶ 26). Patent Owner repeats that the Examiner relies upon Amidi's "Figure 6" and the input RAS and

Copied from 95000579 on 02/08/2017

output rRAS. PO App. Br. 33. As indicated above, the Examiner only relies on this finding for part of the adopted rejection. Patent Owner further asserts the Examiner has not identified a column access procedure. *Id*. Moreover, Patent Owner repeats the argument concerning the signals in the register of Amidi are gone during any subsequent column access procedure and that Amidi would be standardized and have conventional DDR command operations. PO App. Br. 33–34.

We disagree and refer to the above discussion of Amidi when addressing Ground 4 for more details. We also adopt that the Examiner's findings and conclusion related to evidence of secondary considerations not outweighing the case for obviousness. RAN 65–66.

Accordingly, we are not persuaded that the Examiner erred in rejecting claim 21 based on Micron and Amidi.

Remaining Rejections (Grounds 9, 11, 12, and 19)

The above discussions address all the claims on appeal and are dispositive, rendering it unnecessary to reach the propriety of the remaining, adopted rejections. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984); *In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009); 37 C.F.R. 41.77 (a) ("The Patent Trial and Appeal Board . . . may affirm or reverse each decision of the examiner on all issues raised on each appealed claim.")

III. Withdrawn or Non-Adopted Rejections

The Examiner withdrew or did not adopt the following proposed rejections:

Copied from 95000579 on 02/08/2017

Petitioners
Ex. 1016, p. 70

Reference(s)	Basis	Claims	RAN
Amidi (Ground 3)	§ 102	1, 3, 4, 6, 10, 11, 14, 15, 18–20, 24, 25, 28, 29, 31, 32, 34, 36, 37, 39–43, and 46	RAN 11
Amidi (Ground 4)	§ 103(a)	1, 3, 4, 6, 8, 10–20, 24, 25, 27–29, 31, 32, 34, 36–43, 45–48, 50, 52–54, 56, 58, 67–71, 75, 77–89, 92, 93, 120–126, 128–130, 132, 133, and 135	RAN 12
Amidi and Dell 2 (Ground 5)	§ 103(a)	1, 3–4, 6, 8, 10–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 120–122, and 132–136	RAN 12
Amidi and JEDEC (Ground 6)	§ 103(a)	56, 60–63, 90, 91, 109–111, 127, and 131	RAN 12
Murdocca and Dell 2 (Ground 7)	§ 103(a)	1–11, 14, 15, 19, 21, 23–25, 28–34, 36, and 39–42	RAN 12
Micron and Amidi (Ground 13)	§ 103(a)	1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 25, 27–29, 31,	RAN 14

Copied from 95000579 on 02/08/2017

Petitioners
Ex. 1016, p. 71

		32, 36–39, 41–43, 45, 50, 52–54, 56,[22] 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136	
Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19)	§ 103(a)	1, 15, 28, 39, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136	RAN 14
Amidi and Dell 184 (Ground 20)	§ 103(a)	52–54, 56, 67–71, 77–79, 82–84 and 87–89	RAN 15
Micron, Amidi, and Olarig (Ground 21)	§ 103(a)	52–54, 67–71, 77–79, 82–84, and 87–89	RAN 15
Micron, Amidi, Olarig, and Memory Explained (Ground 22)	§ 103(a)	56	RAN 15
Lack of written description (Ground 14)	§ 112, ¶ 1 (pre-AIA)	57, 58, 60, 68, 79, 84, 89–91, and 128–131	RAN 14

R1 App. Br. 6–7; R3 App. Br. 2–3.

We will address Requesters 1–3 appeals separately.

[22] As noted by Patent Owner, claim 57 is presently rejected under Micron and Amidi (Ground 13). RAN 98; PO-R3 Resp. Br. 6. We thus omit claim 57 from the non-adopted rejections under Grounds 13 and 19.

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1. Requester 1's Appeal

Requester 1 appeals the Examiner's decision not to adopt the proposed rejections of various claims based on Ground 3–7 and 14. R1 App. Br. 6–7. Requester 1 generally asserts that the subject matter of the claims that the Examiner confirmed "is actually directed to engineering design choices not properly entitled to patentable weight" and that "patentability [has been] based on design choices that would normally be readily dismissed[.]" R1 App. Br. 7. Requester 1 further asserts that the proper level of skill in the art has not been contemplated. *See* R1 App. Br. 8.

a. Amidi (Grounds 3)

Independent claim 52 is illustrative and recites a logic element generating a CAS or chip-select signal in response in part to an input bank address signal. Concerning Ground 3, Requester 1 explicitly states "[f]or purposes of this appeal" that it "focuses on the obviousness rejection," which is Ground 4. R1 App. Br. 16. By focusing on the obviousness rejection, Requester 1 has not discussed any error in the Examiner not adopting the anticipation rejection (Ground 3) of various claims based on Amidi. PO-R1 Resp. Br. 11 (stating that Requester 1 has waived the "ground in substance.")

However, Requester 1 expressly discusses what Amidi discloses. R1 App. Br. 8–11. From this discussion, Requester 1 asserts Amidi discloses receiving a bank address signal input in Figure 6A (R1 App. Br. 10) and that this circuit matches exactly Figure 1A and 1B of the '912 patent showing bank address input signals and chip-select output signals (R1 App. Br. 10–11). Amidi's Figure 6A shows bank address signals inputted into Register 608 and rCAS signals outputted out of Register 608. Yet, other signals are also outputted out of Register 608,

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including but not limited to rRAS, rAdd[n-1:0], and rWE. Amidi, Fig. 6A. As such, we do not find Requester 1's evidence probative that Amidi's Figure 6A discloses a logic element that generates a CAS signal *in response* at least in part to a bank address signal of the set of input control signals. *See* RAN 26–27. Also, as discussed above when addressing Patent Owner's appeal, Requester 1's comments, and the Examiner's response to Requester 1's comments, we determined that Amidi does not disclose a bank address signal inputted into CPLD 604 (e.g., a logic element) in Figure 6A. *Id.*

We additionally adopt the Examiner's comments related to Ground 3 and agree that Requester 1 and 2's comments do not illustrate Amidi discloses the limitation of generating a CAS or chip-select signal in response to a bank address signal as recited in claim 52 and other independent claims of similar scope. RAN 26–27.

We therefore refer to the above discussion related to Ground 3 and sustain the Examiner's decision not to adopt the anticipation rejection (Ground 3) of various claims based on Amidi.

b. *Amidi (Grounds 4 and 6)*

Concerning Ground 4, we must further consider what an ordinarily skilled artisan would have known, along with the creativity and common sense of a person of ordinary skill, and what Amidi would have suggested to one skilled in the art to determine whether the claimed invention would have been obvious under 35 U.S.C. § 103. *See* PO-R1 Resp. Br. 11. Requester argues claims 1, 15, 28, 39, 52, 58,[23] 67, 77, 82 and 87 as a group. R1 App. Br. 15–18; R1 Reb. Br. 4–7. These claims recite the same or similar recitations. We select claim 1 as illustrative.

[23] Claim 58 depends from independent claim 57, which was not argued.

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Claim 1 recites, in pertinent part, "wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals." Concerning this limitation, the RAN states

> Requester 1 has not presented any evidence of obviousness of modifying Amidi's circuits to generate CAS or chip-select signals in response to a bank address signal. As discussed above, in Amidi, bank signals are stored in registers and transmitted as output signals. They are not used to generate any other control signal. Conclusion of obviousness requires some teaching of usage of bank signals to generate control signals and *an articulation of some reason to combine the teaching with Amidi's teaching with some rational underpinning to support the conclusion*. Requester 1 has provided neither.

RAN 75–76 (emphasis added). For the following reasons, we agree with the Examiner.

As noted previously when addressing Grounds 4 and 6, the Examiner concluded that Amidi teaches or suggests that one skilled in the art would have recognized that bank address signals are received by the registers 408 and 418 and that one of these registers is mapped to the recited "register" and the other to the recited "logic element" in claim 7. RAN 28 (referring to the discussion of Ground 3 at RAN 24), 69, 74. However, we further agree that the record presented by Requester 1 does not provide sufficient evidence that one would have known to direct bank address signals to Amidi's CPLD. That is, other than the mere assertions presented by Dr. Wang to direct bank address signals to a CPLD to provide for "flexibility" and "various design goals" (*see, e.g.,* Wang Decl. ¶¶ 17, 19, 24), there is insufficient evidence to substantiate that one skilled in the art would have recognized to direct bank address signals in Amidi to CPLD 604. Accordingly, as the Examiner found, we agree that there is an insufficient rational

Copied from 95000579 on 02/08/2017

underpinning to support that the non-adopted claims are obvious based on Amidi's teachings.

Citing to paragraph 62, Requester 1 asserts Amidi teaches generating a command signal in response to another command signal. R1 App. Br. 17 (citing Amidi ¶ 62). Amidi discusses a CPLD receiving command (e.g., cs0, cs1) and address signals (e.g., Add(n)) from a controller to determine the correct rank to activate (e.g., rcs0–3). Amidi ¶¶ 60, 62, Figs. 6A–B, 7. Despite Requester 1's urging (*see* R1 App. Br. 17), there is no discussion to use a bank address signal (e.g., BA) to generate the chip-select (e.g. cs0, cs1) signal as recited in claim 1. *See* RAN 26; PO-R1 Resp. Br. 9–10.

Next, relying on Dr. Wang's testimony, Requester 1 contends that one skilled in the art would have known of techniques that use bank address bits to generate chip-select signal. R1 App. Br. 17 (citing 3d Wang Decl. ¶ 14). Requester 1 asserts that the type of transition bit (e.g., row, column, or bank) used by logical circuit design of memory density multiplication is "a simple design choice." R1 App. Br. 17 (citing RAN 75). Requester 1 further points to Dr. Wang's testimony in his first declaration to support one skilled in the art would have known to reassign address signal, including bank address signals, depending on the application. R1 Reb. Br. 5–6 (citing Wang Decl. ¶¶ 10–15, 19–21).

We indicated previously that Dr. Wang's testimony is uncorroborated. Although we recognized that bank address signals, along with row and column address signals, play a role in determining the location of memory in DRAMs (Wang Decl. ¶¶ 11–15), that relationship by itself does not provide a sufficient reason to substitute a bank address signal for the extra row and column address signals used in Amidi to generate chip-select signals. Amidi ¶¶ 51, 59. As such,

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we agree with the Examiner that Requester 1 has not provided an adequate reason with a rational underpinning that Amidi in combination with background knowledge of an ordinarily skilled artisan or JEDEC would yield the recited "logic element [that] generates . . . chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals" in claim 1. Moreover, Requester 1's "design choice" rationale does not provide ample reason to use interchangeably one signal over another for generating the chip-select signals in Amidi. *See* R1 App. Br. 16–17.

Notably, we agree with Patent Owner that Exhibit A,[24] which Dr. Wang discusses (3d Wang Decl. ¶ 14), forms no part of the rejection of Ground 4 as currently proposed. RAN 27; PO-R1 Resp. Br. 12. That is, the rejection as formulated relies solely on Amidi (Ground 4) or Amidi and JEDEC (Ground 6). RAN 27, 32–33. Nor as explained above, does Exhibit A illustrate or teach a feature in Amidi or does Dr. Wang illustrate that one skilled in the art would have recognized using an Intel® 450NX PCIset with Amidi's memory module. *See* 3d Wang Decl. ¶ 14; R1 App. Br., Evid. App'x, Ex. A. We therefore comment no further on Exhibit A.

Requester 1 further contends that the language "in response at least in part to" in claim 1 is ambiguous and should not be construed as "use." R1 App. Br. 17–18 (citing RAN 75). Rather, Requester 1 argues the limitation should be construed broader than the Examiner's understanding. R1 App. Br. 17. Yet, Requester 1 provides no alternative construction that would lead one skilled in the art to conclude that Amidi teaches or suggests the disputed limitation. *See id.*; PO-R1 Resp. Br. 14. Given the record, we agree with the Examiner that his

[24] Exhibit A is entitled "Intel® 450NX PCIset, Rev. 1.3" (March 1999).

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construction of this phrase is reasonable. *See* RAN 27 (stating "[i]f the bank signal is not used in any way to generate the output signals, the generation of output signals cannot be in response to the bank signal.")

Based on Requester 1's proposed rejection and evidence, one skilled in the art would not have recognized (1) receiving bank address signals at Amidi's CPLD and thus (2) generating chip-select signals in response to the bank address signals. We thus determine that the proposed rejection does not teach or suggest to an ordinarily skilled artisan the recitation of "the logic element generates . . . chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals" in claim 1. Requester 1 also does not provide any additional evidence of generating gated CAS signals in response at least in part to a bank address signal as recited. *See* R1App. Br. 15–18.

Patent Owner contends similar limitations to independent claim 1 are found in independent claims 15, 28, 39, 52, 67, 77, 82, and 87. PO-R1 Resp. Br. 9. We agree that these claims recite either generating a chip-select, CAS, or a rank-selecting signal in response at least to a bank address signal. As such, we further determine that the Examiner did not err in not adopting the rejection of these claims for the same reason as discussed above when addressing claim 1.

Concerning independent claim 16, Requester 1 argues that Amidi teaches the limitation of "the command signal is transmitted to only one DDR memory device at a time." *See* R1 App, Br. 18 (citing Amidi ¶ 61); R1 Reb. Br. 9. Amidi discloses that "the Column address needs to be provided with its proper control and command signals in order to read or write to that particular cell." Amidi ¶ 61. Requester further relies on Dr. Wang and Murdocca to support that Amidi

Copied from 95000579 on 02/08/2017

inherently teaches claim 16. R1 App. Br. 18 and R1 Reb. Br. 9 (citing 2d Wang Decl. ¶ 13 and Murdocca 248).

We agree that Amidi teaches using a command signal to read or write to a cell within a DDR memory device. *See* Amidi ¶ 61. Presumably, because Amidi discusses a particular cell within a bank, Requester 1 contends that the command signals are being transmitted to one DDR memory device at a time as recited. R1 App. Br. 18; R1 Reb. Br. 9. Yet, as the Examiner indicates:

> Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication [of Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned explanation to support the assertion. . . . . The claims require transmission of a command signal *to only one DDR memory device at a time*. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal *to only one DDR memory device at a time when there is a plurality of memory devices in a rank.*

RAN 29 (emphasis added).

That is, Figures 6A and 6B of Amidi show various command signals (e.g., CS0, CS1, CKE, CAS, RAS, and WE) being transmitted to more than one memory device. Amidi ¶ 62, Fig. 6A–6B (stating "Signals to Memory Devices" at the far right) Moreover, Amidi's Figures 6A and 6B undermines Requester 1's assertion that delivering command signals to two or more memory cells at a time would create data bus contention. *See* R1 Reb. Br. 9. That is, Amidi's Figures 6A and 6B further teach or suggest that the command signal is transmitted to a cell within *multiple* memory devices at a time. Thus, although Dr. Wang's testimony states that the RAS and CAS signals are used to isolate a particular memory cell in an array of a memory device (2d Wang Decl. ¶ 13), there is countering evidence in

Copied from 95000579 on 02/08/2017

Amidi to demonstrate that isolating a cell relates to isolating a cell within multiple memory devices at the same time.

Lastly, Murdocca does not form any part of the rejection based on Grounds 4 and 6. *See* R1 App. Br. 18. Even so, Murdocca's cell that is formed by an intersection of the row and column address does not refute Amidi's teaching that the command signals are transmitted to memory *devices*.

Accordingly, we are not persuaded that the Examiner erred in not adopting the rejection of claims 16 and 132, which has similar limitations, based on Amidi or Amidi and JEDEC.

Requester 1 provides arguments for dependent claims 17 and 133. R1 App. Br. 18–19. We will sustain the Examiner's decision not to reject these claims, because these claims depend from claim 16 and claim 132 respectively.

As for dependent claim 58, Requester 1 argues the rejection of this claim should be adopted based on its previous contention. R1 App. Br. 18. As discussed above, claim 57, from which claim 58 depends is not disputed. PO App. Br. 47. Claim 58 has similar limitations to claim 1. Thus, for the above reasons when addressing claim 1, we will sustain the Examiner's decision not to reject claim 58 based on Amidi.

Requester 1 further argues specifically that dependent claims 56 and 60 should be rejected based on Amidi and JEDEC (Ground 6). R1 App. Br. 25–26. These claims depend indirectly from claims 52 and 57 respectively. Because we agree that the Examiner did not err in not adopting the rejection of claims 52 and

Copied from 95000579 on 02/08/2017

57, we also determine the Examiner did not err in not adopting the rejection of claims 56 and 60.[25]

Accordingly, we sustain the Examiner's decision not to reject claims 1, 15–17, 28, 39, 52, 56, 58, 60, 67, 77, 82, 87, and 132 and the remaining claims not separately argued based on Amidi alone and in combination with JEDEC.

c. Amidi and Dell 2 (Ground 5)

Requester 1 disputes the Examiner non-adoption of the proposed rejection of claims 1, 3, 4, 6, 8, 10–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 120–122, and 132–136 based on Amidi and Dell 2. R1 App. Br. 7; RAN 12. The Examiner states "the assertions [presented by Requester 1] fail to provide any reason why one of ordinary skill in the art at the time the invention was made would have been motivated to combine the Amidi and Dell 2 systems. Absent a motivation to combine these references, the combination is deemed unobvious." RAN 31.

Requester 1 again argues the claims as a group, and we select claim 1 as illustrative. First, Requester 1 argues that the Examiner erred in determining that, because no motivation was provided to combine Amidi with Dell 2, the combination is deemed unobvious. R1 App. Br. 20 (citing RAN 31). Requester 1 argues that there are several places where motivation was provided. R1 App. Br. 20 (citing 3d Wang Decl. ¶ 16, quoting a portion of the February 13, 2013 Comments, and incorporating the R1 Request), 21–25 (citing 3d Wang Decl. ¶ 10–16).

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[25] Similar claim limitations to claims 56 and 60 were addressed by another panel in another reexamination proceeding. *See Google Inc. v. Netlist, Inc.*, Appeal No. 2014-007777, 2015 WL 799035, at *3–7 (PTAB February 24, 2015) (affirming a similar limitation based on Amidi and JEDEC for U.S. Patent No. 7,289,386) (ordering appeal dismissed at *Netlist, Inc. v. Google Inc.*, No. 16-1270 and 16-1271, slip op. at 1 (Fed. Cir. January 28, 2016)).

Copied from 95000579 on 02/08/2017

Petitioners
Ex. 1016, p. 81

The original request provides a reason with some rational underpinning for combining Amidi and Dell 2, including

> It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the methods for emulating larger RAMs using smaller RAMs disclosed in '152 publication with the logic element disclosed in the '074 patent to realize larger memory capacity at a lower cost.

R1 Request 162. The original request also states Dell 2 teaches addressing the demand for increased memory capacity and to overcome certain related compatibility issues. R1 Request 159–160 (citing Dell 2, 2:32–38). Additionally, Dell 2 discusses an address remapping function that provides a memory module with "more flexib[ility] in terms of its compatibility with different computer systems" and further creates a computer systems, which permits "dynamically to negotiate available memory module functions and modes." Dell 2, 2:33–36, *cited in* R1 Request 159. Thus, Dell 2 provides another reason to be combined with Amidi. We further note whether or not the Dell 2's memory devices can be bodily incorporated into Amidi's system is not the test for obviousness. *See In re Keller*, 642 F.2d 413, 425 (CCPA 1981)). "Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *Id.*

We therefore disagree with Patent Owner that Requester 1's explanation is merely "a technological result of what Requester 1's expert had the capability of building" or that Requester 1 provides no reason to combine Amidi and Dell 2. PO-R1 Resp. Br. 16.

On the other hand, Amidi teaches emulating a smaller memory module by using an address signal, such as an extra row or column line, but does not specifically discuss using a bank address line. We refer to our above discussion of

Copied from 95000579 on 02/08/2017

Grounds 4 and 6 for any details concerning Amidi and the evidence of record concerning what an ordinary skilled artisan would have recognized based on Requester 1's proposed rejection. As such, although Requester 1 provides a reason to combine Dell 2 with Amidi, the question remains whether the references when combined teach or suggest generating a chip-select, CAS, or rank selecting signal in response to a bank address signal.

As proposed, Dell 2 teaches remapping an address signal as a bank address signal using a logic circuit when the memory devices of memory module are configured for M banks but bank address signals inputted correspond to N bank memory devices. Dell 2, Abstract, 4:43–49, *cited in* R1 Request 162. This remapping is done, according to Requester 1, in order to save the bank address later for a CAS sequence. *See* R1 App. Br. 21. Requester 1 argues that this discussion in Dell 2 teaches that a logic element that generates a CAS signal in response to a bank address signal as recited in claim 1, because "the ASIC device will drive the stored output signal during a CAS command *depending on the bank address input*." *Id.* (citing 3d Wang Decl. ¶ 10).

Notably, Dell 2 is silent about driving a CAS command based on a bank address signal. Rather, as understood, the bank address is stored for later use, such as "the CAS sequence and each subsequent sequence for which the ASIC 24 has to address the correct bank." Dell 2, 9:32–34. Dr. Wang similarly testifies that a A12 signal is remapped to a BA1 signal and saved for later use "for the targeted bank." 3d Wang ¶ 10. Dr. Wang further testifies "the ASIC device will drive the stored output signal during a CAS command *depending on the bank address input*." *Id.* However, other than a mere assertion, there is no evidence to support this position. *Id.* We thus do not find this evidence probative.

Copied from 95000579 on 02/08/2017

Also, some of Requester 1's discussion focuses on storing a signal for subsequent use during a column access procedure (i.e., the storing limitations). R1 App. Br. 20–21. However, the claims at issue in the non-adopted rejection based on Amidi and Dell 2 include recitations that differs from the storing limitations previously discussed, including claim 1 reciting particular input and output signals of the logic element. Requester 1 does not address sufficiently why one skilled in the art would have recognized claim 1's limitations were obvious over Amidi and Dell 2 as proposed.

Requester 1 also presents "Figure 1" through "Figure 3," which are not found in Dell 2, to show how bank address signals are outputted from a logic element to memory devices. R1 App. Br. 22–24. According to Requester 1, these figures are derived from Dr. Wang's testimony. R1 App. Br. 23–26 (citing 3d Wang. Decl. ¶¶ 11–16). Yet, this evidence is not probative due to the lack of corroborating evidence. Even so, we note that "Figure 1" and "Figure 2" do not show an input bank address signal being used to generate the CAS signal. As for Figure 3, the record has insufficient supporting evidence, other than Dr. Wang's "belief." 3d Wang Decl. ¶ 15 (further referring to Intel 452NX RAS/CAS generator device that forms no part of Grounds 3–5).

On the other hand, we note that the discussion of Amidi's CPLD receiving bank address signals (e.g., bank address limitation in claim 7) based on Dell 2's teachings as previously discussed, does provide some evidence of generating a chip select or rank select signals in response at least in part to a bank address signal. We first refer to the previous discussion related to Amidi and Dell 2 concerning the bank address limitations and what these references collectively teach. In our discussion, we found that Dell 2 provides a teaching or suggestion to

Copied from 95000579 on 02/08/2017

direct bank address signals to a CPLD, such as Amidi's, in certain situations, such as when the actual and expected dimensions (e.g., the number of banks) of the memory devices differ for navigating to the correct bank within the rank multiplication scheme as suggested by both Amidi (Amidi ¶ 71) and Dell 2 (Dell 2, 2:32–37, 49–51, claim 1). *See also* R2 August 14, 2013 Comments 29–30, 37–38 (discussing different memory devices or densities of memory devices known by ordinary artisan for use with Amidi). We refer above for further details.

In Requester 1's respondent brief to Patent Owner's cross appeal, Requester 1 further contends that claim 119 should be included in the rejection based on Amidi and Dell 2. R1 Resp. Br. 14–19 (citing RAN ¶ 44, 49); R1 Resp. Br. 3. Patent Owner asserts Requester 1 improperly raised this issue because the response does not address an alleged error in Appellant's argument. PO Reb. Br. 38. We determine it is unnecessary to reach the propriety of this non-adopted claim, because of above discussions related to affirming the rejection based on Grounds 4 and 6 when addressing Patent Owner's cross appeal.

We further determine that the Examiner did not err in not rejecting claims 16 and 17 for the above reasons. Requester 1 does not address how Dell 2 cures the missing features of Amidi.

Lastly, we agree with the Examiner's findings and conclusion that the secondary evidence does not outweigh the case for obviousness.

Requester 1 states claims 120–122 and 132–136 were proposed to be rejected under Ground 5 and that these claims are missing from the Examiner's list of the proposed claims. R1 App. Br. 19–20 (referring to RAN and February 13,

Copied from 95000579 on 02/08/2017

2012[26] Comments). Patent Owner challenges Requester 1's contention, asserting the disputed claims form no part of the Examiner's rejection for Ground 5. PO-R1 Resp. Br. 2 (citing RAN 12).

We agree the Examiner does not list claim 120–122 and 132–136. RAN 12, 30–31. On the other hand, the Examiner refers to Requester 1's comments of February 13, 2013 (RAN 31), which do include claims 120–122 and 132–136 in the heading of the proposed rejection based on Amidi and Dell 2. R1 February 13, 2013, Comments 10. Moreover, the February 13, 2012 Comments discuss these claims in more detail. *See* R1 February 13, 2012 Comments 43–48. The Examiner thus should have considered these claims. We adopt Requester 1's position in the February 13, 2012 Comments for purposes of this Opinion. *See id.* (further referring to claim charts in R1 Request).

For the above reasons, we do not sustain the Examiner's decision not to reject (1) claims 1, 120–122, and 132–136, (2) claims 15, 28, and 39, which recite similar limitation to claim 1, and (3) the remaining claims not separately argued under § 103 based on Amidi and Dell 2. We sustain the Examiner's decision not to adopt the proposed rejection for claims 16 and 17 and do not reach the propriety of the non-adopted rejection of claim 119.

d. Murdocca and Dell 2 (Ground 7)

Requester 1 asserts the Examiner's decision not to adopt the proposed rejection of Murdocca and Dell 2 was in error. R1 App. Br. ii (listing claims 1–11, 14, 15, 19, 21, 23–25, 28–34, 36, and 39–42), 26–29; R1 Reb. Br. 12–13. We note

[26] Notably, there are no comments filed on February 13, 2014 by Requester 1. R1 App. Br. 19. Also as previously noted, Requester 1 filed comments on both February 13, 2012 and 2013. We presume Requester 1 intended to refer to the comments filed on February 13, 2012.

Copied from 95000579 on 02/08/2017

Petitioners
Ex. 1016, p. 86

that the Examiner indicated that Requester 1 has failed to raise a substantial new question (SNQ) of patentability based on Murdocca and Dell 2. September 1, 2010 ACP 11 and Order Granting/Denying Request for Reexamination for Inter Partes Reexamination 7–8. Given the Examiner's determination that there is no SNQ for this proposed rejection and such a determination is final, we agree that this ground is not appropriate for appeal. *See* PO-R1 Resp. Br. 21(citing 37 C.F.R. § 1.927). Moreover, given that there was no SNQ for this ground, we determine that the additional statements made by the Examiner beyond the determination that there is no SNQ and concerning the "non-adoption of the proposed claim rejection" (R1 Reb. Br. 12 (underlining omitted)) for Ground 7 are superfluous. We will not address this proposed rejection any further.

e. Lack of Written Description Support (Ground 14)

Requester 1 argues that the Examiner erred in not adopting the proposed rejection under 35 U.S.C. § 112, first paragraph (pre-AIA) of claims 57, 58,[27] 60, 68, 79, 84, 89–91, and 128–131 for failing to satisfy the written description requirement. R1 App. Br. 29–32; R1 Reb. Br. 13–15. To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. *See, e.g., Moba, B.V. v. Diamond Automation, Inc.,* 325 F.3d 1306, 1319 (Fed. Cir. 2003).

Claims 57 and 128 recite in pertinent part "the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase[-]lock loop device." R1 App. Br., Claims App'x 18–19, 29. We select claim 57 as illustrative.

[27] Claim 59 has been canceled.

Copied from 95000579 on 02/08/2017

Petitioners
Ex. 1016, p. 87

For claim 57, Requester 1 argues that Figures 1A and 1B of the '912 patent disclose logic element 40 as an empty box, failing to show how the box operates. R1 App. Br. 29–30. Additionally, Requester 1 states that one skilled in the art would not have known for certain how the signals from PLL 50 were used by logic element 40 and the corresponding disclosure provides no relationship between the output signals and the clock signals received from PLL 50. R1 App. Br. 30 (citing the '912 patent 5:25–31, 6[28]:55–63). Requester 1 and Patent Owner alike (R1 App. Br. 30; PO-R1 Resp. Br. 23) reproduce Figure 1A of the '912 patent but arrive at opposite conclusions concerning whether the '912 patent provides written description support for claim 57. R1 App. Br. 29–31, PO-R1 Resp. Br. 22–24.

Like the Examiner (RAN 53), we find Requester 1's arguments unavailing.

Referring to Figure 1A of the '912 patent reproduced earlier in this Opinion, this figure shows only chip select signals (e.g., CS_{0A-1B}) exiting PLL 40 and thus provides support for the recitation "the logic element generates a first number of chip-select signals of the set of output control signals" within claim 57. The '912 patent, Fig. 1A.

As for the remaining recitation that these signals are "in response at least in part to clock signals received from the phase[-]lock loop device," we note the figure also shows a clock signal from PLL 50, as well as other signals from the computer system (e.g., CS_{0-1}, A_{-n+1}, command signals, BA_{0-m}), enter logic element 40. The '912 patent 5:8–9, 28–36, Fig. 1A, *cited partly in* PO-R1 Resp. Br. 23. Although there is no discussion of the specific details of what happens within logic element 40 within these passages, Figure 1A shows the signals that enter logic element 40, including the clock signal of PLL 50. One skilled in the art would

[28] Requester 1 mistakenly stated column 5 rather than column 6.

Copied from 95000579 on 02/08/2017

Petitioners
Ex. 1016, p. 88

have reasonably concluded that the signals that enter logic element 40 have some purpose and affect the output signals which are *only* chip-select signals (e.g., CS_{0A}– CS_{1B}).

Requester 1 further contends that column 6 does not mention the clock signal when discussing the output control signals. R1 App. Br. 30 (citing the '912 patent 6:55–63). Yet, this passage discusses output signals that "include[] address signals and command signals" (the '912 patent 6:62–63)— not chip select signals— and in *certain* embodiments (the '912 patent 6:55–56), such as those shown in Figures 2A–3B— not Figure 1A. Requester 1 even further asserts that the clock signals can be used in various ways, "including counting, synchronization, timing, phase shifting, frequency multiplication, frequency division, etc. and that the '912 patent does not disclose the specific use of the signal from the phase lock loop." R1 App. Br. 31 (citing Wang Decl. ¶ 16). Even assuming Dr. Wang is correct, this evidence does not demonstrate sufficiently that one skilled in the art would not reasonably conclude that the clock signal is not used in some manner, whether directly or indirectly, to generate the chip select signals shown in Figure 1A.

Patent Owner further notes that the '912 patent discloses an exemplary Verilog code used for memory density multiplication that includes various logic transactions that occur at a positive or negative edge of a PLL clock signal. PO-R1 Resp. Br. 23–24 (citing the '912 patent 14:5–10, 20–23, cols. 13–19). In response, Requester 1 contends that Patent Owner introduces the Verilog code for the first time in the briefs. R1 Reb. Br. 13. Requester 1 contends that there is no expert testimony to support Patent Owner's position concerning the code and that Owner relies solely on attorney argument that should be given no weight. R1 Reb. Br.

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13–14. To be sure, mere attorney argument cannot take the place of evidence in the record and is not probative. *See Estee Lauder Inc. v. L'Oreal, S.A.,* 129 F.3d 588, 595 (Fed. Cir. 1997). However, this position is not merely an argument and has support in the '912 patent.

That is, the code in Example 1 (the '912 patent, cols. 13–18) describes logic element 40 receiving one chip-select signal and generating two output chip-select signals to achieve memory density multiplication. The '912 patent 14:17–23. In this example, the code includes the phrases "always@(posedge clk_in)" and "always@(negedge clk_in)" to begin certain operations. *See, e.g.*, the '912 patent, cols. 13 and 17. As such, Patent Owner's position is supported by the '912 patent's disclosure itself. Given the code, one skilled in the art would have recognized that the certain actions of logic element 40 that translate one input chip-select signal into two output chip-select signals occur at the positive and negative edges of the input clock signal.

Lastly, Requester 1 turns to Dr. Wang in arguing that one skilled in the art "could not have known for certain how the signal from the phase locked loop was used by the logic element of the '912 Patent[.]" R1 App. Br. 30 (citing Wang Decl. ¶ 16). Dr. Wang testifies that the '912 patent discusses the PLL being operatively coupled to the logic element, which means that the PLL is electrically connected directly or indirectly to the logic element. Wang Decl. ¶ 16, *cited in* R1 App. Br. 30–31. However, Dr. Wang determines that a digital logic circuit designer "could not have known for certain how the signal from the phase locked loop was used by the logic element of the '912 Patent[.]" *Id.* Even presuming Dr. Wang's statement is correct that one skilled in the art would not have to know exactly how the signal was used, one skilled in the art would still conclude

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reasonably that the signal was used in some fashion or "in part" to generate the output signals as previously discussed.

To the extent that this argument is further asserting that there is no support in the disclosure to support the phrase "operatively coupled" in claim 57 (*see* R1 App. Br. 31 and R1 Reb. Br. 14 (citing Sechen Decl. ¶ 15)), we disagree. Figure 1A above shows the PLL coupled electrically to memory devices 30, logic element 40, and register 60 (e.g., lines connects PLL to these components).

Based on the above discussion and Figure 1A in the '912 patent, we determine at minimum that an ordinarily skilled artisan looking at this figure would have reasonably concluded that the clock signals that enter logic element 40, which include clock signals from PLL 50, have some effect on the output signals of logic element 40. We thus agree with the Examiner and Patent Owner that logic element 40 uses the input clock signal from PLL 50 *at least in part* to generate the output chip select signals in Figure 1A. *See* RAN 53; PO-R1 Resp. Br. 23. Accordingly, we further determine that the '912 patent's disclosure describes in sufficient detail of the features of claim 57 that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention.

Claims 68, 79, 84, and 89 recite "a logic element that is timed to clock signals from a [PLL]." R1 App. Br. 29. We select claim 68 as illustrative. The '912 patent describes PLL 50 transmitting clock signals to logic element 40. The '912 patent 5:28–31, Fig. 1A. Concerning whether the disclosure supports that logic element 40 "is timed to" such signals as recited, Dr. Sechen explains "[b]y providing a single, common clock from the PLL 50 to both the logic element 40 and the register 60, the memory module of claim 1 of the '912 patent is configured to provide reliable synchronous operation." Sechen Decl. ¶ 16. On the other hand,

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Dr. Wang indicates that an ordinary skilled artisan would not know for sure the clock signals are used in such a fashion. Wang Decl. ¶ 16 (stating the signals "could be used for a variety of different purposes.")

For similar reasons to those discussed above in connection with claim 57, we determine that the clock signals transmitted to logic element 40 affects various operations within the logic element at a certain time (e.g., positive and negative edge of the clock signal). The '912 disclosure 14:20–23, cols. 13–18. Moreover, the descriptor itself, a *clock* signal, describes to one skilled in the art that the signal is used for timing. Accordingly, we further determine that one skilled in the art would have reasonably concluded based on the disclosure and Figure 1A that the clock signals from PLL 50 are used for timing as recited.

Finally, both Requester 1 and Patent Owner indicate claims 90 and 91 depend from claim 89. R1 App. Br., Claims App'x 26; PO-R1 Resp. Br. 22. However, a review of the record indicates that these claims depend from claim 39 directly or indirectly and do not recite the limitations discussed previously in this section. *See* January 14, 2012 Response/Amendment 39–40 (claiming that claim 90 depends from claim 39 and claim 91 depends from claim 90). We therefore determine that these claims should not be part of the proposed rejection. However, to extent that we are mistaken, we are not persuaded by Requester 1's argument for these claims for the same reasons discussed previously.

Accordingly, we are not persuaded that the Examiner erred in not adopting the § 112 ¶ 1 rejection of claims 57 and 68 and claims 58, 60, 79, 84, 89–91, and 128–131 which are not argued separately or have similar limitations.

Copied from 95000579 on 02/08/2017

2. Requester 2's Appeal

Requester 2's appeal concerns consideration of US 6,446,184 ("Dell 184") and a proposed rejection of Amidi and Dell 184 under 35 U.S.C. § 103 (Ground 20). R2 App. Br. 1, 10–18; R2 Reb. Br. 1–15. In particular, Dell 184 and the proposed rejection with Amidi was introduced into the reexamination proceeding subsequent to ordering granting reexamination in Requester 2's Comments dated February 13, 2012. R2 App. Br. 9. The Examiner indicated Requester 2's comments were improper. On August 30, 2012, the Office rendered a decision on a petition filed by Requester 2. R2 App. Br. 10. In its decision, the Office determined the introduction of Dell 184 and the newly-proposed rejection based on Dell 184 were improper and denied Requester 2's petition for entry. August 30, 2012 Dec. on Petition 7. Requester 2 seeks review of the Office's decision. August 30 2012 Dec. on Petition 1, 2.

Patent Owner urges us not to review the issues raised in Requester 2's appeal, because they are petitionable matters. PO-R2 Resp. Br. 12 (citing *S. Sales & Mktg. Grp., Inc. v. World Factory, Inc.*, Appeal No. 2012-008958, 2013 WL 5402207, *1 (PTAB January 10, 2013) (concerning Control No. 95/000,104)). We agree. The issues raised by Requester 2 in its appeal brief are not within the jurisdiction of the Board. *See* Manual of Patent Examining Procedure (MPEP) §§ 1002 and 1201, (9th ed. Rev. 07.2015 October 2015); *see also In re Hengehold*, 440 F.2d 1395, 1403–04 (CCPA 1971) (stating that there are many kinds of decisions made by examiners, "which have not been and are not now appealable to the board or to this court when they are not directly connected with the merits of issues involving rejections of claims, but traditionally have been settled by petition to the Commissioner.")

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In response, Requester 2 asserts that the Examiner did not perform the two-part analysis required under 35 U.S.C. § 103, and such failure is appealable. R2 Reb. Br. 5, 7. We disagree. The Examiner did not consider the proposed rejection given the Office's determination that the Examiner did not err in holding the February 2012 Comments non-compliant with Office regulations. August 30, 2012 Dec. on Petition 7–8. As such, the Examiner did not make a determination whether to adopt or not adopt the rejection proposed by Requester 2. And whether another Board panel set aside petitionable matters and addressed related appealable matter,[29] such a decision is not binding on this panel.

As an alternative, Requester 2 urges the Board to remand this proceeding for further consideration for this matter. R2 Reb. Br. 2. Office regulations state the Board *may* remand a reexamination proceeding. 37 C.F.R. § 41.77(a), *cited in* R2 Reb. Br. 2. We will not exercise our discretion to remand for further consideration of these issues in this circumstance,

There being no decision by the Examiner concerning a substantive matter to review at the Board for claims 1–43, 45–50, 57, 58, 60–63, 75, 80, 81, 85, 86, 90–93, 109–111, and 119–136,[30] we will not review this matter any further.

On the other hand, in a somewhat, apparent contradictory position, the Examiner discusses the proposed rejection of claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89 based on the same combination, Amidi and Dell 184 (Ground 20). RAN 56–57. Requester 2 contends that the Examiner is thus taking

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[29] *See Ex parte Taymac Corp.*, Appeal No. 2011-010682, 2012 WL 1573753 at *8–9 (BPAI April 23, 2012), *cited in* R2 Reb. Br. 7.

[30] The Examiner indicates that claims 1–43, 45–50, 57, 58, 60–63, 75, 80, 81, 85, 86, 90–93, 109–111, and 119–136 were not considered by the Examiner because they were not amended in the Patent Owner's January 14, 2013 response or depend on any such amended claims. March 21, 2014 ACP 9.

Copied from 95000579 on 02/08/2017

unexplainable, inconsistent positions by discussing some claims but not others. R2 Reb. Br. 6, 8–9. Yet, as Patent Owner indicates, Requester 2 has not addressed the Examiner's full explanation to this apparent inconsistency. PO-R2 Resp. Br. 17. That is, the Examiner explained that parts of Requester 2's comments were not defective and were considered in the interest of special dispatch. March 21, 2014 ACP 9–11. As such, we assume that the Examiner, when discussing Ground 20, found that the discussion of claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89 was not defective. *See id.* We also determine that this decision to address some of the claims is consistent with *Rexnord Indus., LLC v. Kappos*, 705 F.3d 1347, 1356 (Fed. Cir. 2013), *cited in* R2 Reb. Br. 8.

Turning to the merits of the proposed rejection for claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89, the Examiner states that Dell 184 does not overcome the deficiencies of Amidi when addressing the rejection of Amidi under 35 U.S.C. § 102 (Ground 3). RAN 56. Specifically, the Examiner finds that Amidi generates a chip-select signal in response to cs0, cs1, Add(n), CAS, RAS, and WE—not a bank address signal. RAN 56. Additionally, the Examiner finds that Dell 184 does not overcome these deficiencies, teaching a logic circuit receiving address and bank address signals as inputs, and remapping an address and bank address signals. RAN 56–57. Although relying on different expert testimony (i.e., Dr. Bagherzadeh's testimony), Requester 2 proposes to reject these claims for reasons similar to Requester 1 presented concerning the proposed Amidi and Dell 2 rejection. *Compare* R2 App. Br. 12–17 *with* R1 App. Br. 19–25.

The teachings in Dell 184 are similar to Dell 2 previously discussed. That is, both references teach and suggest using various types of memory devices or densities, where the memory device is configured with M banks, but the logic

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circuit receives address and bank address inputs corresponding to N bank memory devices. *Compare* Dell 184, Abstract, 2:48–3:5, claim 1, ad Fig. 1 *with* Dell 2, Abstract, 2:40–65, claim 1, and Fig. 1. Moreover, using the same findings and reasoning as discussed above, combining Dell 184's teaching with Amidi would have predictably yielded Amidi's CPLD receiving various inputs, including bank address signals, to achieve both the desired rank and bank expansion. Such a combination would also predictably result in a logic element generating a first number of chip-select or rank-selecting signals in response to a bank address signal as recited in rendering claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89 obvious.

Accordingly, we reverse the Examiner's non-adopted rejection of claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89

3. Requester 3's Appeal

The Examiner did not adopt Requester 3's proposal to reject various claims based on Amidi and at least one other reference under 35 U.S.C. § 103 (Grounds 13, 19, 21, and 22). RAN 14–15. Requester 3 appeals the Examiner's decision not to adopt these proposed rejections. R3 App. Br. 2–3.

a. Micron and Amidi (Ground 13)

Requester 3 asserts that the Examiner erred by not adopting the proposed rejection of claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 25, 27–29, 31, 32, 36–39, 41–43, 45, 50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 as obvious over Micron and Amidi. R3 App. Br. 5–13, 19–22. Specifically, under this ground, the Examiner refers to Grounds 3 through 6 in addressing why these claims under Ground 13 were not adopted. RAN 14, 49, 52 (referring to Grounds 3–6). When addressing Grounds 3 and 4, the Examiner found that Amidi does not disclose generating a CAS or chip-select signal in response to a bank address

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signal. RAN 28–29, *cited in* R3 App. Br. 5; *see also* RAN 26–27. We select claim 1 as illustrative.

Specifically, Requester 3 argues that "obviousness does not require an explicit disclosure" (R3 App. Br. 5) or "'precise teachings . . . for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ'" (*id.* (quoting *KSR*, 550 U.S. at 418)). As discussed above, we agree. Requester 3 further asserts that, given Amidi's disclosure of rank-multiplying memory module, it would have been obvious and even necessary for a logic circuit designer to use a bank address signal in the logic that generates chip-select signals for the memory devices on the memory module. R3 App. Br. 6 (citing 2d Kozyrakis Decl. ¶ 33, 3d Kozyrakis Decl. ¶¶ 15–19, 22–25, and 4th Kozyrakis Decl. ¶¶ 22–23).

In particular, Requester 3 contends that there are two cases when "it is necessary to generate chip-select signals using input bank address signals at column address time." *Id.* The first case occurs "when the incoming row addresses have one more row address bit than the actual memory devices use (Case 1)." *Id.* (citing 2d Kozyrakis Decl. ¶ 33, 3d Kozyrakis Decl. ¶¶ 15–19). The second case occurs "when the input bank addresses have one more bank address bit than the actual memory devices use (Case 2)." *Id.* (citing 3d Kozyrakis Decl. ¶¶ 22–25).

When addressing Amidi above related to Ground 13 and other claims, we determined that Amidi, when accounting for inferences and creative steps that a person of ordinary skill in the art would have employed, at least suggests generating a chip-select signal in response in part to a bank address signal. For example, Requester 3's *second case* of using a spare bank address signal to

Copied from 95000579 on 02/08/2017

generate the proper chip-select signals for rank multiplication as taught by Amidi is similar to our previous discussion of the collective teachings suggest a CPLD receiving a bank address signal. *See* R3 App. Br. 10–11. We refer to our previous discussion for more details. We thus further agree with Dr. Kozyrakis that such a chip-select signal may be generated in response to an address signal. 2d Kozyrakis Decl. ¶ 33; *see also* Kozyrakis Decl. ¶ 26.

Regarding the Requester 3's *first case*, Requester 3 describes Amidi's teaching of using an extra row address bit to generate a chip-select signal in place of an address bit. R3 App. Br. 7–8 (discussing Amidi ¶¶ 43–44, 52), 10. As noted previously, these passages in Amidi do not discuss using a *bank* address bit to generate the chip-select signals. *See* PO-R3 Resp. Br. 12–13. We thus turn to what Requester 3 contends an ordinarily skilled artisan would have recognized regarding bank address signals, as well as other signals, in the context of memory modules.

Patent Owner reasserts that bank address signals are known to be used in memory modules in specific ways and JEDEC does not suggest them being used any other way. PO-R3 Resp. Br. 7–10 (citing JEDEC 79-C 6, 8, 11, Figs. 4, 6). We agree that bank address signals in JEDEC are used for the discussed applications. Yet, as stated earlier, Amidi deviates from at least some of the JEDEC specifications and thus suggest modification from JEDEC designs. *See* R3 Reb. Br. 1 (citing Amidi ¶¶ 10–12).

Also, as previously discussed, Amidi also teaches performing a first row address and then a column address. Amidi ¶ 61. Amidi also states that the column address process needs to be provided with its proper control and command signals in order to read or write to "that" particular cell related to the row address, all

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while achieving rank multiplication. *See id.*; Amidi ¶¶ 10–12. Requester 3 further contends that, during subsequent column address time, a row address bit is not available to generate chip-select signals, and the module must store information from the row address time and match the information to a command (e.g., read). R3 App. Br. 7–8; R3 Reb. Br. 4. Requester 3 asserts some information must be carried from the row address time to the column address time and some control signals must be remapped to select the correct rank. R3 App. Br. 7–8.

According to Requester 3,

> Input bank address signals are necessary to determine which stored row address bit should be used to generate chip-select signals at column address time. *See* Kozyrakis Decl. III, at ¶ 19. It would have been obvious to generate chip-select signals in response to input bank address signals, because the input bank address signals <u>must</u> be used to identify the stored row address bit required to generate the chips-elect signals.

R3 App. Br. 7. Requester asserts "the nature of standard DDR commands motivates a person of ordinary skill in the art to use bank address signals to generate chip-select signals." R3 Reb. Br. 2; *see also* 3d Kozyrakis Decl. ¶ 17, *cited in* R3 App. Br. 8 and R3 Reb. Br. 4; Amidi ¶ 61, *cited in* R3 App. Br. 7 and *quoted in* R3 App. Br. 8.

We agree with Requester 3 that one skilled in the art would have recognized to use bank address signals for this purpose, because Amidi's rank-multiplied memory module requires more ranks and rank chip-select signals than the standard memory module for selecting the appropriate rank in the module, and some control signals must be used or remapped in order to create the needed, increased chip-select signals. R3 App. Br. 7, 9 (citing 3d Kozyrakis Decl. ¶ 18 (indicating that "[t]he incoming bank address and chip select signals from the memory controller are not sufficient for the rank-multiplying module to identify one of its 16 banks

Copied from 95000579 on 02/08/2017

for the CAS command.")) We refer to our previous discussion for more details. Dr. Kozyrakis supports this position, stating, in rank-multiplying scenarios, the bank address and chip-select signals are not adequate to identify the increased number banks for a command but do identify the original pair of banks for the original specified memory devices (e.g., 8). 3d Kozyrakis Decl. ¶¶ 18–19, *cited in* R3 App. Br. 9; 4th Kozyrakis Decl. ¶ 22. As discussed in more detail above, Amidi's Figure 6A and B support this testimony.

Moreover, as discussed above, an ordinarily skilled artisan employing their background knowledge would have known that additional signals are needed to generate the expanded number of chip select signals and would turn to extra signals, including bank address signals, in order to multiply the ranks in a memory module, like Amidi's.

Without citing to Amidi or a declaration, Requester 3 even further asserts that the chip-select signals are generated in response to the input bank address signals,

> because the input bank address signals are used to select the previously stored "highest [row] address number Add(n)" needed to generate the chip-select signals matching those generated at RAS time. In other words, the CPLD 604 would generate chip-select signals based on the stored row address bit, which is selected based on the input bank address signals from the memory controller.

R3 App. Br. 10. Requester 3 further states the ability to design and implement this technique is within the skill of ordinary skilled artisans. *Id.* (citing 4th Kozyrakis Decl. ¶¶ 15–25). However, Dr. Kozyrakis's testimony seems to repeat that an address bit is used to generate a chip-select signal or that the bank address and chip-select signals are each used during CAS commands, rather than the recitation

Copied from 95000579 on 02/08/2017

of a circuit, apart from the memory devices, generates chip-select signals in response to bank address signals as recited. *See* 4th Kozyrakis Decl. ¶¶ 15–25.

Turning, once again, to the second case presented by Requester 3 that occurs when the input bank addresses have one more bank address bit than the actual memory devices use (R3 App. Br. 10–11), Requester 3 cites to other portions of Dr. Kozyrakis' testimony. R3 App. Br. 6, 11 (citing 3d Kozyrakis Decl. ¶¶ 22–25, Kozyrakis Decl. ¶ 26). Requester 3 and Dr. Kozyrakis address the case of a rank-multiplication module from 512 MB devices to 1 GB DDR2 devices found in the '912 disclosure. R3 App. Br. 10–11; 3d Kozyrakis Decl. ¶ 22. Dr. Kozyrakis asserts that there are three input bank address signals (e.g., $BA_{0\text{-}2}$) in this scenario, and they are used to encode the number of the bank to execute a command and to determine the proper rank. 3d Kozyrakis Decl. ¶¶ 22, 25; Kozyrakis Decl. ¶ 26. As discussed, this testimony further illustrates the background knowledge of a person having ordinary skill in the art and, when combined with Amidi's teaching of using free address signals to generate the expanded chip select signals outputted a CPLD, renders claim 1 obvious.

Accordingly, we determine Requester 3 demonstrates Micron and Amidi suggest generating a chip-select signal in response at least in part to a bank address signal as recited in independent claim 1 and independent claims 15, 28, and 39, which recite commensurate limitations.

Requester 3 separately argues independent claim 52. R3 App. Br. 12. The arguments refer back to those discussed for claim 1. We are persuaded for the previously-discussed reasons.

Requester 3 also separately argues independent claims 67, 77, 82, and 87. R3 App. Br. 13. Requester 3 states that the chip-select signals in Amidi are used to

Copied from 95000579 on 02/08/2017

generate rank-selecting signals. *Id.* (citing Amidi ¶¶ 43–44; Fig. 5). We agree and reverse the non-adoption of the rejection for the same reasons already discussed.

Requester even further separately argues claims 56, 60–63, 80, 81, 85, 86, 90, 91, 109–111, 127, and 131. R3 App. Br. 19–22. Requester 3 refers to the arguments presented related to generating chip-select signals in response to input bank address signals. R3 App. Br. 19. Because these claims depend directly or indirectly from independent claims 1, 15, 28, 39, 52, and 57 discussed above and are not separately argued by Patent Owner (*see generally* PO-R3 Resp. Br.), we further determine the Examiner erred in not adopting the rejection of these claims based on Micron and Amidi.

b. Micron, Amidi, and Olarig (Ground 21)

This ground of rejection further illustrates known concepts to an ordinary skilled artisan. Requester 3 asserts that the Examiner erred by not adopting the proposed rejection of claims 52–54, 67–71, 77–79, 82–84, and 87–89 as obvious over Micron, Amidi, and Olarig. R3 App. Br. 17–19; R3 Reb. Br. 8–9 (citing 3d Kozyrakis Decl. ¶¶ 16–19). In not adopting the proposed rejection, the Examiner refers to Ground 13 (the rejection of Micron and Amidi) and further states "the citations of Olarig do not teach or suggest the signal response in each of these amended claims." RAN 57. The Examiner determines that the proposed combination with Olarig does not overcome the deficiencies of Micron and Amidi. RAN 57–58. For the above reasons, we disagree and refer above to our discussion of Ground 13 for more details.

Additionally, Requester 3 further relies on Olarig to teach the limitations of the claims on appeal. Requester 3 contends "the combination of Micron, Amidi, and Olarig does render obvious generating chip-select signals in response to an

Copied from 95000579 on 02/08/2017

input bank address signal." R3 App. Br. 17. Specifically, Requester 3 asserts "Olarig teaches storing information received with a row access command for later use with information from a column address command" and using input bank address signals in remapping control signals. *Id.* (citing Olarig 22:49–54, Fig. 6); R3 Reb. Br. 8–9. Even further, Requester 3 asserts Olarig's Figure 6 and its accompanying description teaches translating input control signals (e.g., bank address signals) for a memory device into output control signals that can be used by another memory device. R3 App. Br. 18–19 (citing Olarig 3:39–42, 22:3–58, Fig. 6); R3 Reb. Br. 9.

Olarig teaches combining a bank address signal with a column address bit. Olarig 22:49–51. As such, there is a teaching to use a bank address signal (e.g., an input bank address signal) with an address signal to generate another output signal during a read/write command. *Id.* Granted, there is no discussion in Olarig that this generated signal is a chip-select or rank-selecting signal as recited. *Id.* But, we agree with Requester 3 that this teaching in Olarig illustrates using bank address signals to generate other control signals was known. *See* R3 App. Br. 18–19.

Additionally, as Requester 3 notes, Olarig is used for a similar purpose to Amidi of remapping input signals into another signal so that when a new memory is introduced into the market a user can substitute the new-type memory module (e.g., a logical memory module) into a pre-existing memory array (e.g., Olarig's memory devices differ from what is expected) of the physical memory module. *See* R3 App. Br. 17–18 (citing Olarig 10:63–11:7, 11:30–40, 22:3–58); *see* Amidi ¶¶ 10–12, 47–49, 52, 55–57, 60, Figs. 6A–6B. Thus, as discussed above, when combined with Amidi's teachings, the collective teachings suggest that an

Copied from 95000579 on 02/08/2017

ordinarily skilled artisan would have recognized generating a chip-select signal in response at least in part to bank address signals.

Patent Owner contends that Olarig does not disclose a bank address bit being mapped to a chip-select signal. PO-R3 Resp. Br. 23. We agree. But, as discussed above, Olarig teaches combining address signals, including a bank address signal, to generate another control signal, and artisans armed with Olarig's and Amidi's teachings and employing their background knowledge, would have recognized using a bank address signal to generate other control signals, such as chip-select signals. Also, the proposed rejection does not suggest bodily incorporating Olarig's Figure 6 into Amidi. *See id.* Rather, the rejection proposes combining the teachings to generate the recited chip-select signals in response to a bank address signal as recited in claim 1.

According, we reverse the Examiner's decision not to adopt the proposed rejection of Micron, Amidi, and Olarig.

4. Remaining Rejections (Grounds 7, 19, 20, and 22)

The above discussions address all the claims on appeal and are dispositive, rendering it unnecessary to reach the propriety of any remaining, non-adopted rejections. *See Beloit*, 742 F.2d at 1423, *Gleave*, 560 F.3d at 1338, and 37 C.F.R. 41.77(a).

IV. CONCLUSIONS

We affirm the Examiner's decision to reject claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57, and 119.

We affirm the Examiner's decision not to reject: (1) claims 1, 3, 4, 6, 10, 11, 14, 15, 18–20, 24, 25, 28, 29, 31, 32, 34, 36, 37, 39–43, and 46 based on Amidi

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under § 102, (2) claims 1, 3, 4, 6, 10–20, 24, 25, 27–29, 31, 32, 34, 36–43, 45–48, 50, 52–54, 56, 58, 67–71, 75, 77–89, 92, 93, 120–126, 128–130, 132, 133, and 135 based on Amidi under § 103, (3) claims 56, 60–63, 90, 91, 109–111, 127, and 131 based on Amidi and JEDEC under § 103, (4) claims 16 and 17 based on Amidi and Dell 2, and (5) claims 58, 60, 68, 79, 84, 89–91, 128–131 under § 112, ¶ 1 as lacking written description support.

We reverse the Examiner's decision not to adopt the rejections of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 based on (1) Amidi and Dell 2, (2) Micron and Amidi, or (3) Micron, Amidi, and Olarig (Grounds 5, 13, and 21), designating our reversal as new grounds of rejection under 37 C.F.R. § 41.77(b).

We do not reach the propriety of the remaining adopted or proposed rejections.

V. TIME PERIOD FOR RESPONSE

Pursuant to 37 C.F.R. § 41.77(a), the above-noted reversal constitutes a new ground of rejection. Section 41.77(b) provides that "[a] new ground of rejection . . . shall not be considered final for judicial review." That section also provides that Patent Owner, WITHIN ONE MONTH FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of the appeal proceeding as to the rejected claims:

> (1) *Reopen prosecution.* The owner may file a response requesting reopening of prosecution before the examiner. Such a response must be either an amendment of the claims so rejected or new evidence relating to the claims so rejected, or both.

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> (2) *Request rehearing.* The owner may request that the proceeding be reheard under § 41.79 by the Board upon the same record. The request for rehearing must address any new ground of rejection and state with particularity the points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

In accordance with 37 C.F.R. § 41.79(a)(1), the "[p]arties to the appeal may file a request for rehearing of the decision within one month of the date of: . . . [t]he original decision of the Board under § 41.77(a)." A request for rehearing must be in compliance with 37 C.F.R. § 41.79(b). Comments in opposition to the request and additional requests for rehearing must be in accordance with 37 C.F.R. § 41.79(c)–(d), respectively. Under 37 C.F.R. § 41.79(e), "[t]he times for requesting rehearing under paragraph (a) of this section, for requesting further rehearing under paragraph (c) of this section, and for submitting comments under paragraph (b) of this section may not be extended."

An appeal to the United States Court of Appeals for the Federal Circuit under 35 U.S.C. §§ 141–144 and 315 and 37 C.F.R. § 1.983 for an *inter partes* reexamination proceeding "commenced" on or after November 2, 2002 may not be taken "until all parties' rights to request rehearing have been exhausted, at which time the decision of the Board is final and appealable by any party to the appeal to the Board." 37 C.F.R. § 41.81; *see also* MPEP §§ 2682, 2683 (8th ed., Rev. 8, July 2010).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

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Petitioners
Ex. 1016, p. 106

In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

AFFIRMED-IN-PART
37 C.F.R. § 41.77(b)

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Ex. 1016, p. 107

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Ex. 1016, p. 108

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/001,339	06/08/2010	7619912	043326-000-0021	5035

25224 7590 07/27/2018
MORRISON & FOERSTER, LLP
707 Wilshire Boulevard
LOS ANGELES, CA 90017

EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
07/27/2018	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

25224 7590 06/01/2018
MORRISON & FOERSTER, LLP
707 Wilshire Boulevard
LOS ANGELES, CA 90017

EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
06/01/2018	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORP.
Requester 1,

SMART MODULAR TECHNOLOGIES, INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

Appeal 2018-003618
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579
Patent No. 7,619,912 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and
JEREMY J. CURCURI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION UNDER 37 C.F.R. § 41.77(f)

STATEMENT OF THE CASE

These proceedings involve U.S. Patent No. 7,619,912 B2 ("the '912 patent), issued November 17, 2009 to Jayesh R. Bhakta and Jeffrey C. Solomon.

In our earlier Decision ("Dec.") mailed May 31, 2016, we affirmed the Examiner's decision not to reject: (1) claims 1, 3, 4, 6, 10, 11, 14, 15, 18–20, 24, 25, 28, 29, 31, 32, 34, 36, 37, 39–43, and 46 based on Amidi[1] under § 102, (2) claims 1, 3, 4, 6, 10–20, 24, 25, 27–29, 31, 32, 34, 36–43, 45–48, 50, 52–54, 56, 58, 67–71, 75, 77–89, 92, 93, 120–126, 128–130, 132, 133, and 135 based on Amidi under § 103, (3) claims 56, 60–63, 90, 91, 109–111, 127, and 131 based on Amidi and JEDEC[2] under § 103, (4) claims 16 and 17 based on Amidi and Dell 2[3] under § 103, and (5) claims 57,[4] 58, 60, 68, 79, 84, 89–91, and 128–131 under § 112, first paragraph, as lacking written description support. Dec. 101–02. We additionally reversed the Examiner's decision not to adopt the rejections of:

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[1] U.S. Publ. 2006/0117152 A1 (published June 1, 2006 and filed Jan. 5, 2004) (Amidi).

[2] JEDEC Standard No. 21-C, *PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Rev. 1.3* pages 4.20.4-1–4.20.4-82 (Jan. 2002) (JEDEC 21-C); *JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification JESD79C* (Rev. of JESD79B) 1-75 (Mar. 2003) (JEDEC 79C); *JEDEC STANDARD, Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications, JESD82-4B (Rev. of JESD82-4A)* 1-12 (May 2003) (JEDEC 82-4B). As indicated in the previous Decision, JEDEC 21-C, JEDEC 79C, and JEDEC 82-4B are often referred to collectively as JEDEC or JEDEC standards in the presented rejections, the briefs, and declarations. *See, e.g.*, Sechen Decl. ¶ 8.

[3] U.S. Patent No. 6,209,074 (issued Mar. 27, 2001) (Dell 2).

[4] The summary at the end of the Decision (Dec. 102) mistakenly omits independent claim 57. *See id.* at 84–89 (discussing claim 57 under the Lack of Written Description Support section).

Petitioners
Ex. 1016, p. 112

(1) claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–43, 45–50, 120–122, and 132–136 based on Amidi and Dell 2 (Ground 5[5]) (*see id.* at 78–83, 102), (2) claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 25, 27–29, 31, 32, 36–39, 41–43, 45, 50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 based on Micron[6] and Amidi (Ground 13) (*see id.* at 93–99, 102), (3) claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89 based on Amidi and Dell 184[7] (Ground 20) (*see id.* at 91–93, 102), and (4) claims 52–54, 67–71, 77–79, 82–84, and 87–89 based on Micron, Amidi, and Olarig[8] (Ground 21) (*see id.* at 99–102). We designated the reversed, non-adopted rejections as new grounds. *Id.* at 102.

In Patent Owner's Response Requesting to Reopen Prosecution submitted August 1, 2016 (PO Response), Patent Owner canceled claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–130 of the '912 patent. PO Response 2. Previously, claims 44, 51, 55, 59, 64–66, 72–74, 76, 94–108, and 112–118 were canceled. *Id.* at 46. According to Patent Owner, claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–136 have been amended. *See id.* at 46. Patent Owner also submitted a declaration of Dr. Carl Sechen, dated July 31, 2016. Requesters 1 through 3 submitted comments (R1 Comments, R2 Comments, and R3 Comments) pursuant to 37 C.F.R. § 41.77(c) on August 31, 2016. Requester 1 presents a declaration of Dr. David Wang, dated August 30, 2016; Requester 2

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[5] Throughout the documents in this proceeding, the Examiner, Patent Owner and Requesters refer to the various rejections by ground number. *See, e.g.*, RAN 11–15. We include the ground number here and throughout the Decision.
[6] Micron, *DDR SDRAM RDIMM, MT36VDDF12872-1GB, MT36VDDF25672-2GB* I-20 (2002) (Micron).
[7] U.S. Patent No. 6,446,184 B2 (issued Sept. 3, 2002) (Dell 184).
[8] U.S. Patent No. 6,260,127 B1 (issued July 10, 2001) (Olarig).

Petitioners
Ex. 1016, p. 113

presents a declaration of Dr. Nader Bagherzadeh, dated August 31, 2016. Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 were the subject of the remand order mailed February 9, 2017. Order 5.[9]

On remand, the Examiner maintained the following rejections in the Examiner's Determination (Ex. Deter.):

(1) claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136[10] based on Amidi and Dell 2 (Ground 5),

(2) claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Amidi and Dell 184 (Ground 20),

(3) claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Micron and Amidi (Ground 13), and

(4) claims 52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Micron, Amidi, and Olarig (Ground 21). Ex. Deter. 21.

The Examiner further adopted Requester 1's proposed rejection of (5) claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and JEDEC 21-C. *Id.*

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[9] A subsequent remand order was mailed May 2, 2017, and a Petition Decision related to the subsequent remand order was mailed June 5, 2017.

[10] The Examiner adds claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 to, and omits claims 120, 122 and 132–136 from, Ground 5. Ex. Deter. 21. We agree with Patent Owner that these additions and omissions were in error. PO Comments 2 n.1.

Petitioners
Ex. 1016, p. 114

After the Examiner's Determination, Patent Owner submitted comments (PO Comments) on November 3, 2017 and Requester 1 responded (R1 Reply) on December 1, 2017 pursuant to 37 C.F.R. § 41.77(e).

This proceeding has returned to the Board under 37 C.F.R. § 41.77(f). Our new Decision is deemed to incorporate our earlier Decision, except for any portion specifically withdrawn. 37 C.F.R. § 41.77(f).

Claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 are independent claims; claim 58 depends from independent claim 57. Claim 57 was not part of the remand. The remaining claims on remand depend directly or indirectly from these claims. Illustrative, independent claim 1 reads as follows:

> 1. (Twice Amended) A memory module connectable to a computer system, the memory module comprising:
>
> a printed circuit board;
>
> a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
>
> a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the

Petitioners
Ex. 1016, p. 115

> plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and
>
> a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
>
> *wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,*
>
> *wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and*
>
> wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to *(i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal*.

PO Response 2–3 (underlining amendments relative to the originally issued claims and italicizing newly added subject matter relative to the claims as originally appealed).

The following summarizes various declarations in this proceeding:

Declaration of Dr. Carl Sechen dated July 5, 2011 (Sechen Decl.),

Declaration of Dr. Carl Sechen dated January 13, 2013 (2d Sechen Decl.),

Petitioners
Ex. 1016, p. 116

Declaration of Dr. Carl Sechen dated July 31, 2016 (2d Supp.[11] Sechen Decl.),

Declaration of Dr. David Wang dated August 29, 2011 (Wang Decl.),

Declaration of Dr. David Wang dated February 13, 2012 (2d Wang Decl.),

Declaration of Dr. David Wang dated February 13, 2013 (3d Wang Decl.),

Declaration of Dr. David Wang dated August 30, 2016 (4th Wang Decl.),

Declaration of Dr. Nader Bagherzadeh dated August 25, 2011 (Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 10, 2012 (2d Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 13, 2013 (3d Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated August 31, 2016 (4th[12] Bagherzadeh Decl.),

Declaration of Dr. Christoforos Kozyrakis dated October 21, 2010 (Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated August 28, 2011 (2d Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated February 23, 2012 (3d Kozyrakis Decl.), and

Declaration of Dr. Christoforos Kozyrakis dated February 13, 2013 (4th Kozyrakis Decl.).

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[11] We deviate from our nomenclature for other declarations to be consistent with Patent Owner's discussion. *See, e.g.,* PO Response 47.

[12] Requester 2 describes this declaration as "Bagherzadeh Decl. V" (R2 Comments 8). We however number the declaration sequentially as part of this list.

Petitioners
Ex. 1016, p. 117

Maintained/Adopted Rejections

In the Examiner's Determination, the Examiner maintains or adopts the following grounds of rejection:

References	Basis	Claims	Presented/Maintained
Amidi and Dell 2 (Ground 5)	§ 103(a)	1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136	Dec. 78–83; Ex. Deter. 21; *see also* above footnote 10
Amidi, Dell 2, and JEDEC 21-C	§ 103(a)	1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136	Ex. Deter. 21

Petitioners
Ex. 1016, p. 118

Amidi and Dell 184 (Ground 20)	§ 103(a)	52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88	Dec. 91–93; Ex. Deter. 21
Micron and Amidi (Ground 13)	§ 103(a)	1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136	Dec. 93–99; Ex. Deter. 21
Micron, Amidi, and Olarig (Ground 21)	§ 103(a)	52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88	Dec. 99–102; Ex. Deter. 21

II. ISSUES

The main issues are whether Patent Owner has presented sufficient arguments and evidence to overcome the new grounds of rejection for and the newly adopted rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 presented in the May 31, 2016 Decision and the Examiner's Determination.

Petitioners
Ex. 1016, p. 119

III. ANALYSIS

A. Amidi and Dell 2 (Ground 5)

In our May 31, 2016 Decision, claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136 (canceled claims omitted) were rejected under 35 U.S.C. § 103 based on Amidi and Dell 2. Dec. 78–83. Patent Owner presents several argument related to this ground, asserting the amendments to independent claims 1, 15, 28, and 39 overcome the new grounds. PO Response 50–53. Patent Owner asserts the claimed "logic element [now] generates certain output control signals (e.g., gated column access strobe (CAS) signals or chip-select signals recited in claim 1) in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and [sic] (iii) the at least one chip-select signal of the set of input control signals, and (iv) the PLL [phase lock loop] clock signal." *Id.* at 52; *see also id.* at 3 (underlining omitted). Throughout this Decision, we will refer to this new limitation as the "logic element" limitation and the response signals collectively as signals (i)–(iv) or individually as signal (i), (ii), (iii), or (iv).

Regarding the "logic element" limitation, Patent Owner argues (1) "Amidi's CPLD 604 never receives bank address signals," instead generating control signals (e.g., chip select signals rcs0a–rcs3b) based on a row address signal and chip-select signals and (2) Dell 2 does not cure Amidi's deficiencies. *Id.* at 52 (citing 2d Supp. Sechen Dec. ¶¶ 21–22, 25). Additionally, Patent Owner argues combining Amidi and Dell 2 would not teach or suggest to one skilled in the art generating control signals based on a row address signal and bank address signals as now recited in the claims. *See id.* at 52–53 (citing 2d Supp. Sechen Dec. ¶¶ 23–24, 26).

Petitioners
Ex. 1016, p. 120

The Examiner maintained the Amidi/Dell 2 rejection on remand. Ex. Deter. 21. Citing to Requester 1–3's Comments, the Examiner determined the newly amended claim recitations, including the "logic element" limitation, have already been rejected in our previous Decision when addressing then existing claims 123, 128, and 129 (claims 128 and 129 are now canceled). *Id.* at 18 (citing R1 Comments 9, R2 Comments, and R3 Comments). Specifically, Requester 1 contends our previous Decision already determined Amidi and Dell 2 teach the recited "logic element" limitation. R1 Comments 7, 10–11 (citing 4th Wang Decl. ¶ 26 and Dec. 80–82, which refer to "the previous discussion related to Amidi and Dell 2 concerning the bank address limitations and what these references collectively teach" (*id.* at 81)); *see also id.* at 40–43 (citing Amidi ¶ 71, Dell 2, Abstract, 2:40–3:5, claim 1, Fig. 1, and 3d Bagherzadeh Decl. ¶ 37), 57–60 (citing Dell 2, 2:48–59, 8:36–41), 78–79 (citing Dell 2, 2:32–38). Requesters 2 and 3 present similar remarks. *See* R2 Comments 8–9 (discussing the similarities of the new claim amendments to claims 52, 123 (previously existed),[13] and 129 (now canceled)); *see also* R3 Comments 7–8 (discussing the previously existing claim 123).

We agree independent claim 52 and claim 123 (previously recited) included a recitation similar to the "logic element" limitation. For example, claim 52 previously recited "the logic element responds to at least a row address bit of the at least one row/column address signal, the bank address signals, and the at least one

[13] Requester 2 cites to "RAN Claims 42." R2 Comments 8. Requester 2 states "RAN Claims" refers to "Patent Owner Response/Amendment" submitted on January 14, 2013. *Id.* at 1. Because the amendment to claim 123 is located on page 38 (RAN Claims 38), we presume Requester 2 is referring to page 38 in the comments.

Petitioners
Ex. 1016, p. 121

chip-select signal by generating a first number of chip-select signals of the set of output control signals." R1 App. Br., App'x A 17 (Claims App'x). Dependent claim 123 depends from claim 1 and previously recited "the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select signals of the set of output control signals." *Id.*, App'x A 27 (Claims App'x). That is, other than the additional signal (iv) or the PLL clock signal now in claim 1 (PO Response 3), claim 1's "logic element" limitation generates chip-select signals in response to the same signals listed in previously recited claims 52 and 123.

However, when addressing Ground 5 (i.e., Amidi and Dell 2), we did not present a new ground of rejection for claim 52, 123, or 129. Dec. 78–83. Rather, we only presented a new ground of rejection for claims 52, 123, and 129 collectively based on Micron and Amidi (Ground 13). Dec. 93–99. As such, although these claims include similar subject matter to claim 1 as currently amended, we did not previously determine Amidi and Dell 2 teach or suggest the limitations found in claims 52, 123, and 129. Moreover, claim 1 previously recited the logic element "generates gated column access strobe (CAS) signals or chip-select signals . . . in response at least in part to a bank address signal" (R1 App. Br., App'x A 1) but did not recite that the CAS signals or chip-select signals were in response to bank address signal*s* as well as signals (i), (iii), and (iv) as now recited in claim 1.

For reasons discussed below and based on the record, we agree with Patent Owner that Amidi and Dell 2 would not teach or suggest to an ordinarily skilled

Petitioners
Ex. 1016, p. 122

artisan the "logic element" limitation, which claims the logic element generates chip-select signals[14] in response to all four enumerated signals (i)–(iv) in claim 1.

In our previous decision, a register (e.g., 408) and a CPLD (e.g., 604) collectively were mapped to the recited "logic element." Dec. 18 (stating "we also do not find the Examiner erred in further mapping CPLD 410 in combination with register 408 to the separately recited 'logic element.'") We analyzed whether Amidi taught or suggested a register (e.g., 408) receiving bank address signals. *See, e.g.,* Dec. 18–21, 27–34. As part of that analysis, we concluded Amidi at least suggests to an ordinarily skilled artisan some embodiments where signals other than those explicitly disclosed, including bank address signals, may be received by register 408. *See, e.g.,* Dec. 28, 30, 33.

However, as now claimed, claim 1 recites the logic element "generates chip-select signals" in response to signals (i)–(iv). In Amidi, its CPLD (e.g., 604 in Figures 6A-B)—not its registers—generates chip-select signals (e.g., rcs0a–3b). Amidi, Figs. 6A–B. Because Amidi's registers (e.g., 408, 418, and 608) do not teach or suggest "generat[ing] chip-select signals" (e.g., rcs0a–3b) and the signals Amidi's registers received do not attribute to the generated chip-select signals at Amidi's CPLD (*see* Amidi, Figs. 6A–B), Amidi's register (e.g., 408) can no longer be a component of claim 1's "logic element" limitation that generates the recited "chip-select signals" in response to signals (i)–(iv).

Amidi shows chip-select signals[15] (e.g., rcs0a–rcs3b) generated by CPLD 604 (e.g., a logic element). Amidi ¶¶ 52, 60, Figs. 6A–B. Also, Amidi teaches and

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[14] We discuss the alternatively generated, "gated column access strobe (CAS) signals" of claim 1 later in the Opinion.
[15] The '912 patent explains "rank-select signals" are "also called chip-select signals." The '912 patent 2:36–38.

Petitioners
Ex. 1016, p. 123

shows a row address signal (e.g., Add(n) or signal (i)) and a chip-select signal (e.g., cs0 or cs1 or signal (iii)) are inputted into Amidi's CPLD 604. Amidi ¶¶ 49, 52, 58, 60, Fig. 6A. As such, Amidi generates chip-select signals in response to both signals (i) and (iii) in claim 1. But, as we previously found, Amidi "fails to describe or show in Figures 4A–B and 6A–B a bank address signal entering CPLD 410 or 604. *See* Amidi, Figs. 4A–B, 6A–B." Dec. 20; *see id.* at 36. Additionally, we agreed with Patent Owner that "Requester 1's proposed obviousness rejections based on Amidi or Amidi and JEDEC (Grounds 4 and 6) do not demonstrate a CPLD receiving BA signals." Dec. 39.

When discussing the obviousness rejection based on Amidi and Dell 2 (Ground 5), we stated "Amidi teaches emulating a smaller memory module by using an address signal, such as an extra row or column line, but does not specifically discuss using a bank address line." Dec. 79; *see id.* at 79–80 (referring to Grounds 4 and 6 for details). However, we additionally stated Dell 2's teaching "provide[s] some evidence of generating [] chip select or rank select signals in response at least in part to a bank address signal." Dec. 81 (referring to our discussion of "bank address limitation in claim 7"). Notably, the "bank address limitation in claim 7" addressed the previously recited "bank address signals of the set of input control signals are received by both the logic element and the register" (R1 App. Br., App'x A 4 (Claims App'x)), not the logic element generating chip-select signals in response to signals (i)–(iv) as claim 1 now recites (PO Response 3).

Even so, we stated "Amidi suggests other types of memory devices or densities can be used to build the four rank memory module" (Dec. 42 (citing Amidi ¶ 71)) and "Dell 2 teaches a technique for using various types of memory

Petitioners
Ex. 1016, p. 124

devices or densities other than those in Amidi, where the memory device is configured with M banks, but the logic circuit receives address and bank address inputs corresponding to N bank memory device. Dell 2, Abstract, claim 1." *Id.; see also id.* at 42–43 (citing Dell 2, Abstract, 2:40–3:5, claim 1, Fig. 1). We also stated "the discussion of Amidi's CPLD receiving bank address signals . . . based on Dell 2's teaching as previously discussed, does provide some evidence of generating [] chip select or rank select signals in response at least in part to *a* bank address signal." *Id.* at 81 (italics added), *quoted in* R1 Comments 10; *see id.* at 94 (stating "Amidi . . . 'at least suggests generating a chip-select signal in response in part to *a* bank address signal'") (emphasis added), *quoted in* R3 Comments 11. These discussions do not address Amidi's and Dell 2 generating chip select signals in response to signals (ii) or "the bank address signal*s*" as now recited.

The previous Decision also states "Dell 2 provides a teaching or suggestion to direct bank address signals to a CPLD, such as Amidi's, in certain situations, such as when the actual and expected dimensions (e.g., the number of banks) of the memory devices differ for navigating to the correct bank within the rank multiplication scheme as suggested by both Amidi (Amidi ¶ 71) and Dell 2 (Dell 2, 2:32–37, 49–51, claim 1)." *Id.* at 81–82 and *see also* 4th Wang Decl. ¶ 26, *cited in* R1 Comments 11. Requester 2 also states Dell 2 discloses the bank address signals of the "logic element" limitation and one skilled in the art would have recognized generating a CAS or chip-select signal in response to a bank address signal in order to ensure the correct bank is addressed. R2 Comments 9–10 (citing 4th Bagherzadeh Decl. ¶ 10[16], which cites Dell 2, 8:29–44).

[16] Requester 2 provides no paragraph number. For purpose of this decision, we presume Requester 2 is referring to paragraph 10.

Petitioners
Ex. 1016, p. 125

Specifically, Dell 2 teaches a logic circuit (e.g., a switch circuit) that performs a remapping function (e.g., 50) of at least one address signal (e.g., A12) to an additional bank address signal (e.g., BA1) at CAS time to ensure the correct *bank* is addressed. Dell 2, 2:32–37, 49–51, 8:20–40, Fig. 1A. Thus, based on Dell 2's teachings or suggestions and what one skilled in the art would have recognized, we agree with Requester 1 (R1 Comments 10–11), Dr. Wang (4th Wang Decl. ¶ 26), Requester 2 (R2 Comments 9–10), and Dr. Bagherzadeh (4th Bagherzadeh Decl. ¶ 10) that one skilled in the art would have recognized using a logic element, like Amidi's CPLD, to generate a control signal in response to a bank address signal for navigating to the correct *bank* during bank expansion (e.g., generate *bank-select* signals in response to bank address signals).

Although this discussion addresses why bank address signals may be received by a CPLD, this reasoning does not sufficiently address why one skilled in the art would have recognized a CPLD, like Amidi's, (e.g., a logic element) generates *chip-select* signals in response to received bank address signals and the other recited signals (i.e., signals (i), (iii), and (iv) recited in claim 1. That is, having a logic element specifically generate "rank-selecting signals . . . in response to" bank address signals in combination with signals (i), (iii), and (iv) as now claim 1 presently recites does not follow from the above teaching to generate signals for *bank* selection. Nor does the current record sufficiently establish that one skilled in the art would have recognized applying Dell 2's bank expansion technique to Amidi's rank expansion process, such that the combination suggests the "logic element" limitation recited in claim 1. Moreover, even assuming, without deciding, one skilled in the art would have recognized to apply such a regime to Amidi's rank expansion process, the teachings would at best suggest

Petitioners
Ex. 1016, p. 126

using one stored bank address signal—not bank address signals or signals (ii) required in claim 1—to generate chip-select signals.

The above-discussed teachings are inadequate to suggest generating *chip-select* signals (e.g., rank select signals) in response to both a row address signal and bank address signal*s* as recited in claim 1. *See* 2d Supp. Sechen Decl. ¶¶ 25 (stating "[t]here is no disclosure or suggestion [in Dell 2] of using [a] bank address to generate a control signal, such as a chip-select signal or a CAS signal"), 26 (stating "[t]here is no suggestion to repurpose a bank address signal for rank multiplication purposes."). Thus, in view of the record as it currently stands, we have reconsidered and withdraw our statement in the previous Decision that combining Dell 2's teaching with Amidi "would have predictably yielded" the logic element receiving bank address signals "so that the necessary rank chip select signals discussed in Amidi are produced" (*id.* at 43) as well as any other similar statements.

We additionally referred to "the previous discussion related to Amidi and Dell 2 concerning the bank address limitations and what these references collectively teach." *Id.* at 81; *see also id.* at 82 and R1 Comments 23 (citing Dec. 81–82). For example, we discussed Dell 2 teaches "storing signals for later use, including during a column access procedure[], to ensure the correct bank is addressed." Dec. 59; *see also id.* at 80. As explained above, this teaching in Dell 2 does not teach or suggest sufficiently to one skilled in the art a "logic element" limitation generating *chip-select* signals in response to both a row address signal (i.e., signal (i)) and bank address signal*s* (i.e., signal (ii)) as well as signals (iii) and (iv). *See also* 2d Supp. Sechen Decl. ¶ 26.

Petitioners
Ex. 1016, p. 127

Claim 1's "logic element" limitation alternatively recites generating "gated column access strobe (CAS) signals . . . in response at least in part to (i) row address signal, (ii) the bank address signals, and (iii) the chip-select signal of the set of input control signals and (iv) the PLL clock signal." PO Response 3. Amidi's CPLD 604 does not teach or suggest generating a CAS signal. *See* Amidi, Fig. 6A. Instead, CAS signals enter (e.g., CAS) and exit (e.g., rCAS) register 608. *See id.* Granted, Amidi's register 608 receives row address signals (e.g., Add[n-1:0]), bank address signals (e.g., BA[1:0]), and PLL signals (e.g., CLK0, CLK0_N). *See id.* ¶ 50, Fig. 6A. Yet, Amidi does not describe how the rCAS signal is generated. *See id.* Moreover, Amidi does not teach or suggest register 608 receiving chip-select signals (i.e., signal (iv) in claim 1) or operates as a logic element to generate gated CAS signals as recited. *See id.* As such, Amidi does not teach and suggest the "logic element" limitation in claim 1.

Additionally, Dell 2 does not teach or suggest the above missing feature. As explained above, Dell 2 teaches or suggests storing a bank address signal for use with a logic element (e.g., ASIC 24) during CAS time. Dell 2, 8:29–40, 9:32–34. Yet, there is no discussion of generating a CAS signal in response to signals (i) through (iv) as recited in claim 1. In particular, Dell 2 fails to teach or suggest generating a CAS signal in response to a chip-select signal (i.e., signal (iii)). Nor do we find Dr. Wang's testimony persuasive in teaching or suggesting generating a CAS signal in response to a chip-select signal. *See* Dec. 80–81 (citing 3d Wang Decl. ¶¶ 10–16). On the record, we therefore determine Amidi and Dell 2 collectively do not teach or suggest sufficiently to one skilled in the art the "logic element" limitation generating CAS signals in response to both a row address

Petitioners
Ex. 1016, p. 128

signal (i.e., signal (i)) and bank address signals (i.e., signal (ii)) as well as signals (iii) and (iv). *See also* 2d Supp. Sechen Decl. ¶ 26.

Lastly, Requester 1 points out Dr. Sechen's statement in paragraph 26 regarding "the narrower claim dictates that a row address signal, and not a bank address signal, is received by the logic element separate from the signals received by the registers." 2d Supp. Sechen Decl. ¶ 26, *cited in* R1 Comments 11. We agree with Requester 1 that claim 1's "logic element" limitation as currently recited requires the logic element to receive both a row address signal *and* bank address signals. *See* PO Response 3. From this perspective, Dr. Sechen's statement is confusing. *See* R1 Comments 11. Yet, when focusing on the recitation "the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element" in claim 1 (PO Response 3), Dr. Sechen's testimony is consistent with claim 1's recitation requiring the logic element to receive a separate or different row/column address signal from the row/column address signals entering the register. *See* 2d Supp. Sechen Decl. ¶ 26.

Independent claims 15, 28, and 39 each recite a similar "logic element" limitation to claim 1, which generates gated CAS signals or chip-select signals in response to signals (i) through (iv), including both a row address signal and bank address signals. PO Response 11, 18, 23–24. For the above reasons, we determine Amidi's and Dell 2's teachings are inadequate to teach or suggest the "logic element" limitation in these claims.

Upon reconsideration of the record, we withdraw the rejection of claims 1, 15, 28, and 39 and dependent claims 3, 4, 6, 8, 10–14, 18–20, 22, 24, 27, 29, 31,

Petitioners
Ex. 1016, p. 129

32, 34–38, 40, 41, 43, 45–50, 120, 122, and 132–136, which variously depend from claims 1, 15, 28, and 39, based on Amidi and Dell 2.

B. Amidi, Dell 2, and JEDEC 21C

The rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and JEDEC 21-C was newly proposed by Requester 1 in its comments. R1 Comments 12–77. The Examiner adopted this proposed rejection. Ex. Deter. 11. Specifically, concerning the "logic element" limitation found in independent claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 and dependent claim 58, Requester 1 proposes a similar mapping and reasoning for combining Amidi with Dell 2 to teach or suggest this recitation. *See, e.g.,* R1 Comments 23. Requester 1 adds JEDEC 21-C teaches or suggests transmitting PLL clock signals to a CPLD and, and when combined with Amidi, generating its output control signals (e.g., rank-selecting or chip-select signals) in response to a PLL signal for clocking additional devices on a DIMM. *See* R1 Comments 22 (citing JEDEC 21-C, pp. 38–43), 23. In essence, based on JEDEC 21-C's teaching, Requester 1 states one skilled in the art would have known or recognized modifying Amidi so that the clock signals comes Amidi's PLL 606 (e.g., PLL clock signals) rather than memory connector 602 for clocking DIMM devices. *See id.* at 22–23. This modification, in turn, generates chip-select or rank-selecting signals in response to a PLL clock (i.e., signal (iv)) as recited. *See id.*

Yet, JEDEC 21-C's teaching is not relied upon and does not cure the above-noted deficiencies in Amidi and Dell 2—namely the "logic element" limitation generates gated CAS, chip-select or rank-selecting signals in response to

Petitioners
Ex. 1016, p. 130

both a row address signal (i.e., signal (i)) and bank address signals (i.e., signals (ii)) as well as signals (iii) and (iv). We refer above for more details.

Accordingly, we withdraw the adopted rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and JEDEC 21-C.

C. Amidi and Dell 184 (Ground 20)

In our May 31, 2016 Decision, claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 (canceled claims omitted) are rejected under 35 U.S.C. § 103 based on Amidi and Dell 184. Dec. 91–93. Independent claims 52, 67, 77, 82, and 87 include similar recitations to the "logic element" limitation in claim 1 that generates rank-selecting or chip-select signals in response to signals (i) through (iv). *Compare* PO Response 27, 33, 36, 38, and 41 *with id.* at 3. Notably, claims 52, 57, 77, 82, and 87 exclude the alternative recitation of generating a gated CAS signal. *Id.* at 27, 33, 36, 38, and 41.

Our rationale for rejecting these claims based on Amidi and Dell 184 was similar to that proposed for Amidi and Dell 2. Specifically, we noted in the opinion

> The teachings in Dell 184 are similar to Dell 2 previously discussed. That is, both references teach and suggest using various types of memory devices or densities, where the memory device is configured with M banks, but the logic circuit receives address and bank address inputs corresponding to N bank memory devices. *Compare* Dell 184, Abstract, 2:48-3:5, claim 1, a[n]d Fig. 1 *with* Dell 2, Abstract, 2:40–65, claim 1, and Fig. 1. Moreover, using the same findings and reasoning as discussed above, combining Dell 184's teaching with Amidi would have predictably yielded Amidi's CPLD receiving various inputs, including bank address signals, to achieve both the

Petitioners
Ex. 1016, p. 131

> desired rank and bank expansion. Such a combination would also predictably result in a logic element generating a first number of chip-select or rank-selecting signals in response to a bank address signal . . . .

Id. at 92–93.

Similar to that noted above when addressing Dell 2, Dell 184 in combination with Amidi may provide a reason why bank address signals may be received by a CPLD, but does not sufficiently address why one skilled in the art would have specifically recognized Amidi's CPLD (e.g., a logic element as recited in claim 52) generates *chip-select* or *rank-selecting* signals in response to signals (i)–(iv) as recited in claims 52, 67, 77, 82, and 87. We refer above for more details.

Requester 2 asserts Patent Owner provided no argument related to the patentability of the claims rejected based on Ground 20 and relied upon the arguments presented for Micron and Amidi. *See* R2 Comments 10 (stating "Patent Owner did not provide any individual analysis concerning the patentability of those claims in view of this rejection, but rather relied on its analysis for the rejections under Micron and Amidi."). We disagree.

Patent Owner states "[t]hese amendments [to the claims presented after the previous Decision] distinguish the claims from the combination of Amidi and Dell 184, as discussed above. *See also* Second Supp. Sechen Decl. Section IV." PO Response 56. In "Section IV" of the declaration, Dr. Sechen discusses the similarities between the teachings of Dell 184 and Dell 2 and further articulates how Dell 184 does not use bank address inputs for rank multiplication. *See* 2d Supp. Sechen Decl. ¶¶ 38, 40–42. As such, when stating "as discussed above" (PO Response 56), Patent Owner was referring to the rejection of Amidi and Dell 2 and not Micron and Amidi as argued.

Petitioners
Ex. 1016, p. 132

Accordingly, we withdraw the rejection of claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Amidi and Dell 184.

D. Micron and Amidi (Ground 13)

In our previous Decision, we determined claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41–43, 45, 50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 (canceled claims omitted) were obvious over Micron and Amidi. Dec. 93–99. For this rejection, Patent Owner reasserts Amidi does not use both bank address signals and row address signal for rank multiplication or for generating chip-select signals/CAS signals. PO Response 54 (citing 2d Supp. Sechen Decl. ¶¶ 29–30). As to whether one skilled in the art would be motivated to use bank address signals for proper operation of chip select signals, Patent Owner contends "this is a conclusion of fact and not an indication of what a POSITA[17] would recognize." *Id.* at 55 (citing 2d Supp. Sechen Decl. ¶¶ 32–33); *see also id.* at 55–56 (citing 2d Supp. Sechen Decl. ¶¶ 34–35). Patent Owner argues combining Micron and Amidi to arrive at the claimed invention as amended would not be obvious to one skilled in the art. *Id.* at 56. For reasons discussed below, we are persuaded Micron and Amidi do not teach or suggest the newly recited "logic element" limitation in claim 1 or similar independent claims.

At the outset, we address Patent Owner's argument that Dr. Kozyrakis's testimony represents how an expert—not an ordinarily skilled artisan—would have understood Amidi and that Amidi, which does not teach using bank signals to generate chip-select or CAS signals for rank expansion, is representative of what one skilled in the art would have understood. *Id.* at 54–55 (citing 2d Supp. Sechen Decl. ¶¶ 31–32). We agree with Requester 3 that Dr. Kozyrakis's testimony is

[17] "POSITA" stands for a person of ordinary skill in the art.

Petitioners
Ex. 1016, p. 133

from the point of view of what an ordinarily skilled artisan would have known or recognized. *See* R3 Comments 12 (citing Kozyrakis Decl. ¶ 8, 2d Kozyrakis Decl. ¶¶ 12–14, 3d Kozyrakis Decl. ¶¶ 9–11, 4th Kozyrakis Decl. ¶¶ 12–14). For example, Dr. Kozyrakis testifies that one of ordinary skill in the art (e.g., two or more years of professional experience in memory design)[18] would have an understanding of "the latest memory devices," including DDR, DDR-2, and DDR-3 devices, and "the number of rows, columns, banks, and input/output bits of each device." 2d Kozyrakis Decl. ¶ 14, 3d Kozyrakis Decl. ¶ 11, and 4th Kozyrakis Decl. ¶ 14. On the other hand, we also agree with Patent Owner that "Amidi is representative evidence of what a POSITA would understand." PO Response 55; *see also* Dec. 27 (stating Amidi "reflects the appropriate skill level at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).").

Next, the amendments to independent claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 and dependent claim 58 have been made to include the "logic element" limitation that generates gated CAS, chip-select, or rank-selecting signals in response to four enumerated signals, signals (i) through (iv). *See* PO Response 2–3, 10–11, 17–18, 22–27, and 29–41. As stated above when addressing Ground 5, Amidi does not teach to an ordinarily skilled artisan using bank address signals to generate CAS signals or chip-select signals. *See also* Dec. 95 (stating "these

[18] Our previous Decision established that one of ordinary skill in the art "is a person with (1) at least an undergraduate degree in either electrical engineering, computer engineering, or in a closely related discipline and (2) at least two years of experience in designing computer memory systems. This ordinarily skilled artisan would also have familiarity with and understanding of (1) JEDEC standards related to memory devices and modules, such as DDR SDRAM devices and DIMMs, and (2) the latest DRAM memory devices in the market." Dec. 26–27.

Petitioners
Ex. 1016, p. 134

passages in Amidi do not discuss using a *bank* address bit to generate the chip-select signals.") (referring to Amidi ¶¶ 43–44, 52). However, we previously noted "Amidi suggests other types of memory devices or densities can be used to build [its] four rank memory module." Dec. 42 (citing Amidi ¶ 71); *see also* Amidi ¶¶ 10–12, *cited in* Dec. 96. We therefore turned to what "an ordinarily skilled artisan would have recognized regarding bank address signals, as well as other signals, in the context of memory modules." Dec. 95.

In referring to "our previous discussion," (*id.*), we stated

> Amidi, when accounting for inferences and creative steps that a person of ordinary skill in the art would have employed, at least suggests generating a chip-select signal in response in part to a bank address signal. For example, Requester 3's *second case* of using a spare bank address signal to generate the proper chip-select signals for rank multiplication as taught by Amidi is similar to our previous discussion of the collective teachings suggest a CPLD receiving a bank address signal.

Id. at 94–95. For example, Dr. Kozyrakis stated one skilled in the art would have recognized different generation of DDRs (e.g., DDR-1, DDR-2, and DDR-3) and that some DDR-2 devices have an extra bank address field (e.g., 3 bits rather than the conventional 2 bits). *Id.* at 61–62 (citing Kozyrakis Decl. ¶ 26); *see also* 3d Kozyrakis Decl. ¶¶ 22–25. We then concluded this provides evidence that one skilled in the art would have recognized or known a bank address signal is free in certain DDR devices to assist in creating the desired rank expansion for certain memory modules. *See id.* at 62; *see id.* at 65–66 and 98.

In particular, we stated:

> [L]ike Amidi's teaching of using an extra row/column address bit for generating the proper chip-select signals (e.g., rank expansion) for

Petitioners
Ex. 1016, p. 135

> emulating a two rank memory module (Amidi ¶¶ 51, 59), Dr. Kozyrakis provides a reason with some rational underpinning that an ordinary skilled artisan would have used other known, extra address bits (e.g., the extra bank address in more recent DDR devices) to create the desired rank expansion in Amidi by directing such extra signals to Amidi' s CPLD.

Id. at 62. We maintain our position that the record provides a reason with a rational underpinning to use *a* free signal—whether a row address or a bank address signal—to achieve desired rank expansion. Despite Patent Owner asserting this "second case" no longer applies "to the amended claims" (PO Response 54), neither Patent Owner nor Dr. Sechen's testimony (2d Supp. Sechen Decl. ¶ 29) sufficiently explains why this scenario no longer pertains to the amended claims or why bank signals cannot be used by both the registers and a logic element. *See* R3 Comments 10.

Additionally, in the previous Decision, we noted Amidi uses an extra row or column address signal as an input to the CPLD to generate chip-select signals and uses a column address signal (e.g., A11) for multiple purposes. Dec. 63–64 (citing Amidi ¶¶ 50–52, 57–60, Figs. 6A–B). Based on Amidi's teaching, we concluded an ordinary skilled artisan having two years of experience in logic circuit design would have recognized to use address signals in an unconventional manner and for multiple purposes. We additionally found Requester 3 provides adequate evidence that one skilled in the art would have recognized using bank address signals in a manner similar to the row and column address signals, some of which are received by Amidi's CPLD. *Id.* at 64, 66. Yet, the evidence of record does not teach or suggest generating the specifically recited chip-select signals using more than one bank address signal and, more particularly, both bank address

Petitioners
Ex. 1016, p. 136

signal*s* (i.e., signals (ii)) and a row address signal (i.e., signal (i)) as well as signals (iii) and (iv) claimed in claim 1.

Requester 3 offers yet another reason for a logic element to generate chip-select signals in response to both multiple bank address signals and a row address signal. *See* Dec. 96–97 (citing R3 App. Br. 7–10, R3 Reb. Br. 2, 4, 3d Kozyrakis Decl. ¶¶ 17–19, 4th Kozyrakis Decl. ¶¶ 15–25, and Amidi ¶ 61). In particular, Requester 3 stated previously (*see* R3 App. Br. 10) and now (*see* R3 Comments 13) "[b]ecause the extra row address bit [used during row address time] is unavailable at column address time, the rank-multiplying module must store information from row address time for use during column access time." R3 Comments 13 (citing 3d Kozyrakis Decl. ¶ 19). According to Requester 3, "[i]nput bank address signals are necessary to determine which stored row address bit should be used to generate chip-select signals at column address time. Kozyrakis Decl. III ¶ 19." R3 Comments 13; *see also* R3 App. Br. 7. Requester 3 thus asserts chip-select signals are generated in response to both a row address signal and bank address signals

> because the input bank address signals are used to select the previously stored "highest [row] address number Add(n)" needed to generate the chip-select signals matching those generated at RAS time. In other words, the CPLD 604 would generate chip-select signals based on the stored row address bit, which is selected based on the input bank address signals from the memory controller.

R3 App. Br. 10, *quoted in* Dec. 97.

Turning to Amidi, this reference teaches CPLD 410's circuitry for row address decoding and column address decoding (e.g., row address time and column address time) differs. Amidi ¶ 61. Amidi states the "Row

Petitioners
Ex. 1016, p. 137

address" cycle and "the Column address" cycle need to be provided with "the proper control and command signals" but fails to provide any specifics related to which control and command signals are provided during these cycles. *Id.* Nor does Amidi show or suggests bank address signals entering CPLD 604 during row address or column address decoding. *See id.*, Figs. 6A–B; *see also* PO Response 54 (citing 2d Supp. Sechen Decl. ¶¶ 29–30).

Concerning row and column address time, Dr. Kozyrakis states an ordinary artisan would have known of alternative scenarios from Amidi where the logic element can decode or pre-process the one row address bit, store the resulting signals from decoding or pre-processing, and then use the stored, resulting signals during column access operations "to generate chip-select signals or the bank address field." 2d Kozyrakis Decl. ¶ 18(d)(ii); *see also id.* ¶ 33. In this scenario, decoded or pre-processed signals—not bank address signals—are used during column access time to generate chip-select signals. Dr. Kozyrakis further states "bank address are not always necessary in order to determine the output control signals for the lower density memory devices," such as in Amidi. 2d Kozyrakis Decl. ¶ 23. As such, Dr. Kozyrakis's testimony conflicts with Requester 3's position that bank address signals *are necessary* (R3 Comments 13) to generate the chip-select signals during column access time.

Nevertheless, Dr. Kozyrakis also asserts an "obvious way to know which of the two banks has the proper row open" during subsequent CAS commands is to store the address bit (e.g., A_{13}) and to reuse the stored address bit to identify the correct pair of banks (e.g., reuse as a bank address signal). *See* 3d Kozyrakis Decl. ¶¶ 18–19. Notably, Dr. Kozyrakis does not

Petitioners
Ex. 1016, p. 138

discuss how the stored address bits are located during subsequent CAS commands (*see id.*), such as by using bank address signals as Requester 3 asserts (R3 Comments 13).

To elaborate, Dr. Kozyrakis testifies that a memory module's controller must identify which bank should receive the CAS command using bank address and chip-select signals. 3d Kozyrakis Decl. ¶¶ 17–18. Dr. Kozyrakis also states the incoming bank address and chip-select signals from a memory controller are not sufficient for certain rank-multiplying modules. *Id.* ¶ 18 (discussing "the case where the originally specified module uses two ranks of 512Mbit DDR2 devices [having four banks] and the rank-multiplying module uses four ranks of 256Mbit DDR2 devices [having four banks]."). Specifically, during a RAS command to a bank in a 512Mb device, Dr. Kozyrakis states a rank-multiplying module designer would use bank address and chip-select signals to identify a bank pair from eight banks and would use a free address bit (e.g., A_{13}) to identify which of the two banks in the bank pair will receive a command. *Id.* ¶ 19.

During a subsequent CAS command, Dr. Kozyrakis further states the memory controller does not provide the free address (e.g., A_{13}) bit to identify the correct bank in the bank pair. *Id.* Thus, Dr. Kozyrakis states an obvious way to identify the correct bank in a pair with the proper row open is to store the address bit of the last RAS command (e.g., A_{13}) and to reuse the stored address bit. *Id.* However, unlike Requester 3's assertion that bank address signals are used to identify this stored address bit (R3 Comments 13), Dr. Kozyrakis does not additionally testify the incoming bank address signals are used to identify the stored address bit. 3d Kozyrakis Decl. ¶ 19.

Petitioners
Ex. 1016, p. 139

Instead, Dr. Kozyrakis states "the module must have a total of 8 bits of storage for A_{13} address bits" without discussing how the proper address bit is identified. *Id.*

Dr. Kozyrakis's testimony in his fourth declaration also cited by Requester 3 (R3 Comments 13) does not further explain or address how stored address bits are identified—namely, whether or not using bank address signals are used. *See, e.g.*, 4th Kozyrakis Decl. ¶¶ 15–25, *cited in* R3 Comments 13. Similarly, Dr. Bagherzadeh also states storing the extra address bit is "a standard feature in transparent memory modules like the embodiments disclosed in Amidi" and the circuit "will be unable to identify the correct chip to access during the column access procedure" if the extra bit is not stored. 2d Bagherzadeh Decl. ¶ 22. But, once again, Dr. Bagherzadeh does not explain how the stored address bit is later identified.

Granted, Dr. Kozyrakis and Dr. Wang point to references in asserting one skilled in the art would have known to store some address bits for each bank in a logic device and use them later during column commands. 4th Kozyrakis Decl. ¶ 24 (citing Olarig); *see* 3d Wang Decl. ¶ 10 (citing Dell 2). Nevertheless, Olarig and Dell 2 form no part of this rejection based on Micron and Amidi and thus are not persuasive. Moreover, these references do not teach or suggest using bank address signals later to identify the stored bits.

Moreover, to the extent Dr. Kozyrakis's testimony does suggest bank address signals are used to identify the stored bits, this position clashes with his earlier testimony stating

> bank address signals must be used as one of the inputs for the calculation of the output chip-select signals *only if* the number of

Petitioners
Ex. 1016, p. 140

> banks in the memory devices used in the lower cost memory module is *smaller* than the number of banks in the memory devices in the originally specified module. In all other cases, the bank address signals can be simply clocked through the logic element . . . without further processing.

2d Kozyrakis Decl. ¶ 23 (italics added). In the example provided in the third declaration (3d Kozyrakis Decl. ¶¶ 18–19), the bank number of the lower cost memory module's memory devices (e.g., 256Mb devices having four banks) is not smaller than the originally specified module's memory devices (e.g., 512Mb devices also with four banks), implying that bank address signals will only be clocked through the logic element. *See id.* Additionally, Dr. Kozyrakis states the bank address signals "must be used as *one* of the inputs for the calculation of the output chip-select signals" (2d Kozyrakis Decl. ¶ 23 (italics added)) when the bank number in the lower cost memory module is smaller than the bank number of the originally specified module, suggesting at most one bank address signal—instead of bank address signals (i.e., signals (ii))—is used.

Thus, Requester 3's assertions that Amidi's "CPLD 604 would generate chip-select signals based on the stored row address bit, *which is selected based on the input bank address signals from the memory controller*" (R3 App. Br. 10) (emphasis added) is not corroborated adequately with Dr. Kozyrakis's testimony. Likewise, Requester 3's conclusion that it would have been obvious to an ordinarily skilled artisan to generate chip-select signals in response to both a row address signal and "input bank address signals during column address time, because the input bank address signals must be used to identify the stored row address bit

Petitioners
Ex. 1016, p. 141

required to generate the chip select signals" (*see* R3 Comments 13; *see also* R3 App. Br. 7) is not corroborated sufficiently by Dr. Kozyrakis.

Additionally, Dr. Sechen provides countering evidence and arrives at the opposite conclusion of Requester 3. 2d Supp. Sechen Decl. ¶¶ 22 (citing Sechen Decl. ¶ 23, 2d Sechen Decl. ¶¶ 14–15), 29 (citing "Section II"). Specifically, Patent Owner and Dr. Sechen focus on Amidi and assert this reference demonstrates what one skilled in the art would have recognized. PO Response 55. Patent Owner and Dr. Sechen state Amidi provides no recognition to one of ordinary skill that bank address signals are necessary for generating chip-select signals. 2d Supp. Sechen Decl. ¶¶ 33, 35; PO Response 54–55. Dr. Sechen further states Amidi does not recognize generating chip-select signals using both the bank address signals and a row address signal as recited in claim 1 for rank multiplication. *See* 2d Supp. Sechen Decl. ¶¶ 29, 31, 32; *see also* PO Response 55. Dr. Sechen testifies additionally Amidi and Micron do not teach using bank address signals to generate rank or chip-select signals and that using the bank address signals in this manner would not have been known by one of ordinary skill based on Micron and Amidi. Sechen Decl. ¶¶ 35, 37. Patent Owner and Dr. Sechen argue one skilled in the art "would conclude that Amidi is operative without bank address signals for generating control signals." 2d Supp. Sechen Decl. ¶ 33; *see also* PO Response 55.

As previously noted, we agree that Amidi provides evidence of what one skilled in the art would have known or recognized at the time of the invention. *See Okajima*, 261 F.3d at 1355. As such, we agree with Dr. Sechen that one skilled in the art "would conclude that Amidi is operative without bank address signals for

Petitioners
Ex. 1016, p. 142

generating control signals," and thus a memory module's logic element (e.g., Amidi's CPLD) can generate chip-select signals without using bank address signals. *See* 2d Supp. Sechen Decl. ¶ 33. Although an obviousness "analysis need not seek out precise teachings" and we further consider an ordinarily skilled artisan's background knowledge (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)), Dr. Kozyrakis's testimony and Requester 3's articulated reason that bank address signals are known to be used to identify the row address signal, which in turn is used generate chip-select signals, lacks sufficient corroborating evidence to provide a rational underpinning to support an obviousness conclusion. *See id.*

Lastly, Requester 3 notes that claims 52, 123, and 129 recite similar limitations to claim 1 (excluded a PLL clock signal (i.e., signal (iv)) and were addressed in our previous Decision. R3 Comments 8–9. We acknowledge claims 52, 128, and 129 were previously rejected based on Micron and Amidi. Dec. 93–99. However, the specific limitations found in claims 52, 128, and 129 similar to the "logic element" limitation in claim 1 as now amended were not disputed in Requester 3's brief. For example, regarding claim 52, Requester 3's arguments referred back to claim 1 as previously recited (*see* Dec. 98 (citing R3 App. Br. 12 (stating "[a]s discussed above, it would have been obvious for the chip-select signals generated as CAS time to be generated based on *an* input bank address") (italics added))), which did not include the "logic element" limitation found in claim 1 as now amended.

Upon reconsideration of claim 1 as now amended, we withdraw our conclusion of obviousness for these claims based on Micron and Amidi. We also withdraw the remarks made in our previous Decision concerning one skilled in the art would have recognized using bank address signal*s* for generating chip-select

Petitioners
Ex. 1016, p. 143

signals (*see* Dec. 96–97), in view of the above discussion. Weighing all the evidence in the record, we determine one skilled in the art would not have recognized using a known logic element, such as Amidi's, to generate chip-select signals in response to a row address signal (i.e., signal (i)), multiple bank address signals (i.e., signals (ii)), a chip-select signal (i.e., signal (iii), and a PLL clock signal (i.e., signal (iv)) as recited in claim 1.

Regarding the logic element alternatively generating gated CAS signals in response to signals (i) through (iv) as recited in claim 1 (PO Response 3), there is insufficient evidence to support such CAS signals are generated in response at least in part to these signals. *See* R3 Comments 11–13 (focusing on generating chip-select signals); *see also* 3d Kozyrakis Decl. ¶¶ 16–19, 22–25 (discussing receiving a CAS command and generating chip-select signals) and 4th Kozyrakis Decl. ¶¶ 22–24 (same). As discussed above, Amidi's CPLD 604 does not teach or suggest generating a CAS signal but rather a CAS signal entering (e.g., CAS) and exiting (e.g., rCAS) register 608. *See* Amidi, Fig. 6A. Amidi also does not (a) describe how the rCAS signal is generated or (b) teach or suggest chip-select signals entering register 608. *See id.* ¶ 50, Fig. 6A. Micron similarly does not disclose or teach how gated CAS signals are generated. *See* Micron 5–8.

For the above reasons, we withdraw our rejection of claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Micron and Amidi.

E. Micron, Amidi, and Olarig (Ground 21)

Above, we stated Requester 3 provided insufficient evidence to support the assertion that bank address signals are necessary for generating

Petitioners
Ex. 1016, p. 144

gated CAS/chip-select signals or that one skilled in the art would have recognized using both a row address signal and bank address signals as well as signals (iii) and (iv) for this purpose. Unlike Ground 20, Olarig is also being relied upon in Ground 21. Thus, Dr. Kozyrakis's testimony concerning storing some address bits for each bank in a logic device and using them later during column commands illustrates storing and reusing an address bit for a later operation is known to an ordinary skilled artisan. 4th Kozyrakis Decl. ¶ 24 (citing Olarig). But, this teaching does not further illustrate using bank address signals to identify the stored row address bit as Requester 3 asserts. *See* R3 Comments 13.

Nevertheless, as indicated in our previous Decision,

> Olarig teaches combining a bank address signal with a column address bit. Olarig 22:49-51. As such, there is a teaching to use a bank address signal (e.g., an input bank address signal) with an address signal to generate another output signal during a read/write command. *Id.* Granted, there is no discussion in Olarig that this generated signal is a chip-select or rank-selecting signal as recited. *Id.* But, we agree with Requester 3 that this teaching in Olarig illustrates using bank address signals to generate other control signals was known. *See* R3 App. Br. 18-19.

Id. at 100. We then concluded "Olarig teaches combining address signals, including a bank address signal, to generate another control signal, and artisans armed with Olarig's and Amidi's teachings and employing their background knowledge, would have recognized using a bank address signal to generate other control signals, such as chip-select signals." *Id.* at 101.

This analysis indicates an ordinary artisan would have recognized to combine address signals with *a* bank address signal to generate control signals. But, even this teaching falls short of suggesting generating a control

Petitioners
Ex. 1016, p. 145

signal, such as a chip-select signal, in response to both at least one row address signal (e.g., recited signal (i)) and bank address *signals* (i.e., signals (ii)) recited in claim 1. *See* 2d Supp. Sechen Decl. ¶¶ 46–48. Granted, we also concluded "when combined with Amidi' s teachings, the collective teachings suggest that an ordinarily skilled artisan would have recognized generating a chip-select signal in response at least in part to bank address signal*s*." *Id.* at 100–101 (italics added). In light of the record before us now, we no longer conclude Amidi, Dell 2, and Olarig collectively teach or suggest combining multiple bank address signals with a row address signal as well as signals (iii) and (iv) to generate chip-select (or gated CAS signals for that matter).

Requester 3 asserts Patent Owner relies on "Section IV," which is directed to the rejection based on Micron and Amidi, and does not address Olarig. R3 Comments 13. For this reason, Requester 3 argues Patent Owner fails to show the claims rejected based on Micron, Amidi, and Olarig are unobvious. *Id.*

Patent Owner refers to its previous discussion when address the rejection based on Micron, Amidi, and Olarig. PO Response 56–57. As noted above, based on the record, we are persuaded that Micron and Amidi do not sufficiently demonstrate the "logic element" limitation found in the independent claims as now amended. We refer above for more analysis. Patent Owner also refers to "Second Supp. Sechen Decl. Section V" (*id.* at 57), which discusses Olarig. *See* 2d Supp. Sechen Decl. ¶¶ 45, 48–52. We thus disagree with Requester 3 that Patent Owner does not address Olarig in its remarks.

Petitioners
Ex. 1016, p. 146

In "Section V" of the declaration, Dr. Sechen notes our previous Decision stating Olarig teaches combining a bank address signal with a column address bit to generate an output signal. 2d Supp. Sechen Decl. ¶ 45. Dr. Sechen further asserts that one skilled in the art would not reach the conclusion that Amidi and Olarig teach the claims as now amended. *Id.* ¶¶ 46–48. Although we disagree with Dr. Sechen that one skilled in the art would not recognized using a bank address signal to generate chip-select signals (*see id.*) for reasons previously stated, we agree that Amidi and Olarig alone or in combination with Micron do not suggest generating gated CAS, chip-select, or rank-selecting signals in response to both a row address signal (i.e., signal (i)) and bank address signals (i.e., signals (ii)) as well as signals (iii) and (iv) as now recited in claim 1. Requester 3 provides no rebuttal to Dr. Sechen's testimony. *See* R3 Comments 13.

For the above reasons, we withdraw our rejection of claims 52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Micron, Amidi, and Olarig.

F. Proposed Rejections based on Micron, Amidi, and Additional References

In the earlier Decision, we did not reach the proposed rejections set forth in Ground 19 (Micron, Amidi, Dell 2, and JEDEC 79C) and Ground 22 (Micron, Amidi, Olarig, and Memory Explained[19]). Dec. 101.[20] Based on the amendments

[19] *HP Printer Memory Explained* 1-7 (Jan. 21, 2004), *available at* http://warshaft.com/hpmem.htm (Memory Explained).

[20] We mistakenly included Grounds 7 and 20 in Section (III)(4)'s heading. Dec. 101. Ground 7 was addressed in the previous Decision, indicating that the Examiner determined there was no substantial new question (SNQ) of patentability for this proposed rejection. *Id.* at 83–84. Further, as discussed above in Section (III)(C), Ground 20 was also addressed. *Id.* at 90–93.

Petitioners
Ex. 1016, p. 147

to claims 1, 15, 58, 67, 77, 82, and 87 and our withdrawal of the other grounds, we now consider the Examiner's decision not to adopt these proposed rejections.

Specifically, the Examiner did not adopt the following proposed rejections:

Reference(s)	Basis	Claims (canceled claims omitted)	
Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19)	§ 103	1, 15, 28, 39, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136	RAN 14–15; R3 App. Br. 13
Micron, Amidi, Olarig, and Memory Explained (Ground 22)	§ 103(a)	56	RAN 15

1. Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19)

Above, we addressed the rejection of Micron and Amidi in Section (III)(D), concluding that one skilled in the art would have not recognized based on the references' teachings a logic element generates gated CAS signals or chip-select signals in response to signals (i)–(iv) as now recited in claims 1, 15, 58, 67, 77, 82, and 87. We additionally addressed rejections based on Amidi and Dell 2 (Section (III)(A) and Amidi, Dell 2, and JEDEC 21-C (Section (III)(B)), also concluding one skilled in the art would have not recognized based on the references' teachings a logic element generates gated CAS signals, chip-select or rank-selecting signals in response to signals (i)–(iv) as now recited. We refer above for more details.

Petitioners
Ex. 1016, p. 148

As discussed in the context of the rejection of Amidi and Dell 2 (Ground 5), Dell 2 does not teach or suggest the missing feature of using both signal (i) and signals (ii) to generate gated CAS, chip-select, or rank-selecting signals as now recited in claims 1, 15, 52, 58, 67, 77, 82, and 87. We refer above for more details.

Regarding JEDEC 79C, Requester 3 does not explain how this reference is being relied upon in its Appeal Brief. *See* R3 App. Br. 13–17. Moreover, the cited comments, submitted August 29, 2011, in the Appeal Brief do not address JEDEC 79C. *Id.* at 14 (citing pages 18 and 19). As for Appendix L also cited in the Appeal Brief, (*id.*), the proposed rejection discusses how JEDEC 79C teaches a read operation reads from the row selected by the preceding activate command on the same bank. Requester 3's August 29, 2011 Comments, App'x L, p. 1 (addressing claim 52). Yet, this teachings do not suggest the missing feature of generating gated CAS signals or chip-select signals in response to both a row address signal (i.e., recited signal (i)) and bank address signals (i.e., recited signals (ii)). *See id.*, App'x L, pp. 1–2. We thus determine Requester 3 has not sufficiently demonstrated how JEDEC 79C teaches or suggests the claimed features missing from Micron, Amidi, and Dell 2.

Accordingly, we determine the Examiner has not erred in not adopting the proposed rejection of claims 1, 15, 28, 39, 52, 54, 56, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 (canceled claims omitted) based on Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19).

2. Micron, Amidi, Olarig, and Memory Explained (Ground 22)

Above, we addressed the rejection of Micron, Amidi, and Olarig in Section (III)(E), concluding that one skilled in the art would have not recognized based on

Petitioners
Ex. 1016, p. 149

the references' teachings a logic element generates gated CAS signals or chip-select signals in response to signals (i)–(iv) as recited in claims 1, 15, 28, 39, 52, and 58.

As for Memory Explained, the Examiner stated and we agree that this reference, even when combined with Micron, Amidi, and Olarig, does not teach or suggest generating CAS or chip-select signals in response to bank address signals (i.e., signals (ii)) as well as recited signals (i), (iii), and (iv). RAN 58–69. Requester 3 does not rebut this determination. R3 App. Br. 19 (asserting Micron, Amidi, and Olarig teach these features). In particular, Requester 3 turns to Memory Explained to teach the features recited in dependent claim 56, not the features in independent claim 52. *See* Requester 3's February 13, 2013 Comments 24–25, App'x S.

For the above reasons, we determine the Examiner has not erred in not adopting the proposed rejection of claim 56 (as well as claims 60–63, 80, 81, 85, 86, 90, 91, 109–111, 127, and 131)[21] based on Micron, Amidi, Olarig, and Memory Explained (Ground 22).

V. CONCLUSIONS

We withdraw the following rejections maintained or adopted by the Examiner.

(1) Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136 are rejected under 35 U.S.C. § 103 based on Amidi and Dell 2 (Ground 5).

[21] Despite including only claim 56 in our previous Decision (Dec. 69), Requester 3 appealed the Examiner not adopting the rejection of claim 56 as well as the remaining claims listed above. R3 App. Br. 19–22.

Petitioners
Ex. 1016, p. 150

(2) Claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 are rejected under 35 U.S.C. § 103 based on Amidi and 184 (Ground 20).

(3) Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 are rejected under 35 U.S.C. § 103 based on Amidi, Dell 2, and JEDEC 21-C.

(4) Claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 are rejected under 35 U.S.C. § 103 based on Micron and Amidi (Ground 13).

(5) Claims 52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88 are rejected under 35 U.S.C. § 103 based on Micron, Amidi, and Olarig (Ground 21).

We further affirm the Examiner's decision not to adopt the rejection of certain claims based on Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19) or Micron, Amidi, Olarig, and Memory Explained (Ground 22), previously not reached.

Based on our previous Decision, we note the following rejections are affirmed.

(1) Claim 9 and 33 is rejected under 35 U.S.C. § 102 based on Amidi. Dec. 11, 13, 23.

(2) Claims 2, 5, 7, 9, 21, 23, 30, 33, 57, and 119 are rejected under 35 U.S.C. § 103 based on (a) Amidi or (b) Amidi and JEDEC. Dec. 12–13, 39, 57.

(3) Claims 2, 5, 7, 9, 21, 23, 26, 30, and 33 are rejected under 35 U.S.C. § 103 based on Amidi and Dell 2. Dec. 12–13, 43, 60.

Petitioners
Ex. 1016, p. 151

(4) Claims 7, 9, 21, 26, 33, and 57 are rejected under 35 U.S.C. § 103 based on Micron and Amidi. Dec. 12–13, 66–67.

(5) Claim 9 is rejected based on (a) Dell 1[22] and JEDEC under 35 U.S.C. § 103 (RAN 13, 36–39) (Ground 9), (b) Wong[23] and JEDEC under 35 U.S.C. § 103 (RAN 13, 41–43) (Ground 11), and (c) Micron and Connolly[24] under 35 U.S.C. § 103 (RAN 13, 44–47) (Ground 12). Dec. 12–13.

We also note the Examiner's decision not to adopt the proposed rejection of claims 16 and 17 based on Amidi and Dell 2 remains affirmed and we do not reach the propriety of the non-adopted rejection of claim 119 under Ground 5. Dec. 82–83.

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

<u>37 C.F.R. § 41.77(f)</u>

[22] U.S. Patent No. 5,926,827 (issued July 20, 1999) (Dell 1).
[23] U.S. Patent No. 6,414,868 (issued July 2, 2002) (Wong).
[24] U.S. Patent No. 5,745,914 (issued April 28, 1998) (Connolly).

Petitioners
Ex. 1016, p. 152

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Petitioners
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The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES, INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

Appeal 2018-003618
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579
Patent No. 7,619,912 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and
JEREMY J. CURCURI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION ON REHEARING

This merged proceeding involves U.S. Patent No. 7,619,912 B2 ("the '912 patent), issued November 17, 2009 to Jayesh R. Bhakta and Jeffrey C. Solomon. This is a request by Requester 3, Google Inc., for a rehearing under 37 C.F.R. § 41.79 ("Req. for Reh'g") of our Decision Under 37 C.F.R. § 41.77(f) ("Decision 2") dated July 27, 2018, on the Examiner's Determination Under 37 C.F.R. § 41.77(d) ("Ex. Deter.") mailed October 3, 2017. Decision 2 is subsequent to and incorporates a Decision dated June 6, 2016 ("Decision 1")[1] in which new grounds of rejection were entered under 37 C.F.R. § 41.77(b).

In response to the new grounds of rejection, Patent Owner reopened prosecution, amending claims and submitting new evidence for consideration. Patent Owner's Response Requesting to Reopen Prosecution Pursuant to 37 C.F.R. § 41.77(b)(1) ("PO Request"), pp. 2–57 (August 1, 2016). Requester 3 responded, urging the new grounds of rejection be maintained. *See generally* Requester 3's Comments Pursuant to 37 C.F.R. §41.77(c) ("R3 Comments") (August 31, 2016). In Decision 2, we withdrew many rejections maintained or adopted by the Examiner (Decision 2, pp. 40–41) while other rejections of certain claims remain affirmed (Decision 2, pp. 41–42).

Requester 3 sets forth three occasions in Decision 2 where we allegedly misapprehended or overlooked points in withdrawing the new grounds of rejection presented in Decision 1. First, Requester 3 contends we overlooked findings in concluding that cited prior art does not render the "logic element" limitation in claim 1 and other independent claims obvious. Req. for Reh'g 2–6. Second, Requester 3 argues we misapprehended the meaning of the "logic element"

[1] In Decision 2, we state "Our new Decision is deemed to incorporate the earlier Decision, except for those portions specifically withdrawn. 37 C.F.R. § 41.77(f)." Decision 2, 5.

Petitioners
Ex. 1016, p. 156

limitation in determining this limitation has written description support. Req. for Reh'g 6–7. Third, because we determined there is written description support for the recitation "logic element," Requester 3 asserts we overlooked that the prior art supports the obviousness rejection grounds. Req. for Reh'g 8–9. We are not persuaded.

Requester 3 presents arguments for the claims as group. *See generally* Req. for Reh'g. We select claim 1 as representative. *See* 37 C.F.R. § 41.67(c)(1)(vii).

"Logic Element" in Claim 1 is Purportedly Taught by Requester 3 Newly Proposed Ground

Requester 3 asserts we found Amidi discloses receiving all four claimed signals "by its logic elements and some use of all four claimed signals in logic operations performed by those logic elements." Req. for Reh'g 3 (citing Decision 2, p. 18). Requester 3 further states we found Amidi teaches its CPLD (complex programmable logic device) receives a row address signal and a chip select-select signal and generates a chip-select signal in response. Req. for Reh'g 3 (citing Decision 2, pp. 13–14). We are not persuaded we misapprehended Amidi such that it teaches the claimed "logic element" limitation in claim 1.

The "logic element" limitation recites "the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal."[2] PO Request 3. In Decision 2, we stated Amidi teaches register 608 (e.g., a logic element) receiving row address

[2] In Decision 2, we referred to this limitation as "the 'logic element' limitation" and "the response signals collectively as signals (i)–(iv) or individually as signal (i), (ii), (iii), and (iv)." Decision 2, p. 10. We similarly do so here.

Petitioners
Ex. 1016, p. 157

signals, bank address signals, and PLL (e.g., signals (i), (ii), and (iv)). Decision 2, p. 18, *noted in* Req. for Reh'g 3 and 5. We further stated Amidi does not teach a register receiving a chip-select signal, recited signal (iii). Decision 2, p. 18. Thus, Amidi's register 608 (e.g., a logic element) receives row address signals, bank address signals, and PLL signals (e.g., signals (i), (ii), and (iv))—not all four recited signals in claim 1. Additionally, we stated "Amidi does not describe how the rCAS signal is generated." Decision 2, p. 18. Requester 3 has not demonstrated how these findings related to Amidi teach or suggest the rCAS signal is generated in response to signals (i) through (iv) as recited in claim 1.

Requester 3 also notes Decision 2 states Amidi teaches generating chip-select signals in response to a row address signal and a chip-select signal (e.g., signals (i) and (iii)). Decision 2, pp. 13–14 (citing Amidi ¶¶ 49, 52, 58, 60, Figs. 6A–B), *cited in* Req. for Reh'g 3. In Decision 2, when addressing Amidi's CPLD (e.g., another logic element), we stated Amidi fails to describe or show a bank address signal (i.e., one of signal (ii)) entering CPLD 410 or 604. Decision 2, p. 14 (citing Decision 1, p. 20, 36). Specifically, these findings related to Amidi do not suggest generating chip-select signals in response to signals (i)–(iv) as required by claim 1. Nor has Requester 3 persuasively shown how we overlooked or misapprehended points related to Amidi on pages 13 and 14 in rendering our determination in Decision 2 that this reference alone fails to teach the "logic element" limitation.

Requester 3 even further indicates (Req. for Reh'g 5) we stated "Requester 3 provides adequate evidence that one skilled in the art would have recognized using bank address signals in a manner similar to the row and column address signals, some of which are received by Amidi's CPLD." Decision 2, p. 26, *quoted in* Req.

Petitioners
Ex. 1016, p. 158

for Reh'g 26. But, Requester 3 omits the sentence that follows from this statement; "[y]et, the evidence of record does not teach or suggest generating the specifically recited chip-select signals using more than one bank address signal, and more particularly, both bank address signal*s* (i.e., signals (ii)) and a row address signal (i.e., signal (i)) as well as signals (iii) and (iv) claimed in claim 1." Decision 2, pp. 26–27.

Accordingly, Requester 3 has not pointed out how these findings demonstrate we overlooked or misapprehended Amidi's teachings related to the "logic element" limitation, which requires generating chip-select or CAS signals in response to signals (i)–(iv) as claim 1 now requires.

Requester 3 further discusses findings and conclusions related to Amidi *as modified by* JEDEC 21-C and Olarig. Req. for Reh'g 4–6 (citing Decision 2, pp. 20 and 35). Requester 3 raised issues in its brief submitted September 30, 2014, concerning its proposed rejections based on (1) Micron and Amidi (Ground 13), (2) Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19), (3) Micron, Amidi, and Olarig (Ground 21), and (4) Micron, Amidi, Olarig, Memory Explained (Ground 22) in its original brief. Appeal Brief of Third Party Requester Google Inc. Pursuant to Pre-AIA 35 U.S.C. 134(c) and 37 C.F.R. § 41.67 (dated September 30, 2014) ("R3 Appeal Br.") 5–22. Notably, JEDEC 21-C differs from JEDEC 79C. *See* Decision 1, p. 10. Requester 3 appealed the Examiner's decision not adopting proposed rejections of certain claims based on Micron and at least one other reference, including Amidi (i.e., Grounds 13, 19, 21, and 22). R3 Appeal Br. i (Table of Contents); *see also* Decision 1, pp. 68–69, 93–101.

Rule 41.79(b)(1) states, in relevant part, "[a]rguments not raised in the briefs before the Board and evidence not previously relied upon the briefs are not

Petitioners
Ex. 1016, p. 159

permitted in the request for rehearing except as permitted by paragraphs (b)(2) and (b)(3) of this section." 37 C.F.R. § 41.79(b)(1). Additionally, the Decision *Sua Sponte* to Merge Reexamination Proceedings ("Merger Decision"), mailed February 28, 2011, further explains "each *inter partes* reexamination requester's appeal must only be taken from the finding(s) of patentability of claims in the RAN that the individual third party requester proposed in the request" under the section entitled "2. Appeal Rights." Merger Decision 4. As acknowledged by Requester 3's arguments (Req. for Reh'g 6 n.2) related to Amidi, JEDEC 21-C, and Olarig collectively (Req. for Reh'g 4 and 5 (citing Decision 2, pp. 20 and 35 respectively)) were not raised by Requester 3 in its brief before the Board. Also, Requester 3's request proposed rejections based on at Micron and Amidi but not Amidi, JEDEC 21-C, and Olarig. Request for *Inter Partes* Reexamination Under 35 U.S.C. § 311 and 37 C.F.R. § 1.913 ("R3 Request") 18–20. Thus, this proposed new ground is not permitted by Rule 41.79(b)(1) or the Merger Decision.

To be sure, Rule 41.79(b)(1) indicates arguments not raised in the briefs before the Board and evidence not previously relied upon the briefs are "permitted by paragraphs (b)(2) and (b)(3) of this section." 37 C.F.R. § 41.79(b)(1). Paragraph (b)(2) permits new arguments related to recent relevant Board or Federal Circuit decision upon a showing of good cause. 37 C.F.R. § 41.79(b)(2). Requester 3 does not discuss a relevant decision Federal Circuit decision. *See* Req. for Reh'g 4–6. Also, to the extent Requester 3 asserts Decision 2 is a relevant Board Decision (*see* Req. for Reh'g 6 n. 2), Requester 3 has not provided sufficient good cause to consider any such argument for the below reasons.

Rule 41.79(b)(3) permits new arguments to respond to a new ground of rejection made pursuant to 37 C.F.R. § 41.77(b). 37 C.F.R. § 41.79(b)(3).

Petitioners
Ex. 1016, p. 160

Decision 1 included new grounds of rejection, including rejections based on (1) Amidi and Dell 2, (2) Micron and Amidi and (3) Micron, Amidi, and Olarig (Grounds 5, 13 and 21)—the latter two grounds proposed by Requester 3. Decision 1, pp. 102 (reversing identified, proposed rejections not adopted by the Examiner). As such, Requester 3 was permitted to present arguments responding to the new grounds of rejection based on (a) Micron and Amidi and (b) Micron, Amidi, and Olarig in a request for rehearing.

Additionally, Requester 3 submitted comments according to 37 C.F.R. § 41.77(c) responding Patent Owner's response requesting reopening of prosecution. Although having the opportunity to propose a new ground of rejection based on Amidi and JEDEC 21-C or Amidi, JEDEC 21-C, and Olarig in Requester 3's comments, no such ground was proposed. *See* R3 Comments 4–14. Moreover, Requester 3 acknowledges this fact. Req. for Reh'g 6 n.2. However, Requester argues that "the necessity of such a ground only arose from the Board's Decision rejecting the Examiner's findings in view of the other stated grounds." Req. for Reh'g 6 n.2 (citing 37 C.F.R. § 1.948(a)(2)). We presume Requester 3 is arguing it only now needed to propose the new rejection ground based Amidi, JEDEC 21-C, and Olarig in its request for rehearing because we withdrew various grounds of rejection in Decision 2.

As noted above, Requester 3 was permitted to propose new grounds in its comments when Patent Owner amended the claims in its request to reopen prosecution. *See* 37 C.F.R. § 41.77(c) and 37 C.F.R. § 1.947. Rule 1.948, which is cited by Requester 3 (Req. for Reh'g 6 n.2), indicates a third party requester is permitted to cite additional prior art if it is filed as part of a comment submitted under § 1.947, which permits comments on "[e]ach time the patent owner files a

Petitioners
Ex. 1016, p. 161

response to an Office action on the merits pursuant to § 1.945." 37 C.F.R. § 1.947. Requester 3 thus had a chance to propose a new ground when commenting on Patent Owner's response requesting reopening prosecution. *See* 37 C.F.R. § 41.77(c); *see* the Manual of Patent Examining Procedure (MPEP) § 2682(II)(B)(2) (stating "[t]he comments [under 37 C.F.R. § 41.77(c)] may include new evidence and arguments if limited to support the new grounds of rejection by the Board, *including new evidence and arguments directed towards amended or new claims* if necessitated by patent owner's submission under 37 CFR 41.77(b)(1)) (emphasis added). *See also IPCom GmbH & Co. v. HTC Corp.*, 861 F.3d 1362, 1372 (Fed. Cir. 2017) (corrected Aug. 21, 2017) (citing to Rule 1.948(a)(2) and stating "Section 41.77(c) requires only that HTC's comments be limited to the Board's decision and issues raised by IPCom's request to reopen prosecution. 37 C.F.R. § 41.77(c)."); *see also Airbus S.A.S. v. Firepass Corp.*, 793 F.3d 1376, 1380 (Fed. Cir. 2015) ("Airbus's proposed citation of prior art is well within § 1.948(a)'s permission to cite prior art 'which is necessary to rebut a response of the patent owner.' That response that Airbus is entitled to rebut was the addition of new claims 91–94.").

Contrary to Requester 3's assertion, the need to present a new ground of rejection did not arise only from our findings and conclusions in Decision 2. Moreover, Requester 3 does not indicate which claims of the '912 patent are to be rejected under this newly proposed ground in its request for rehearing.

For the above reasons, Requester's proposed ground based Amidi, JEDEC 21-C, and Olarig and arguments related to the proposed combination (Req. for Reh'g 4–6) are unpersuasive and improperly raised at this juncture.

Petitioners
Ex. 1016, p. 162

"Logic Element" in Claim 1 is Allegedly Misconstrued and Lacks Written Description Support as Construed By the Board

Requester 3 states "the Board appears to have disagreed with Google's argument that the broadest reasonable interpretation of the 'logic element' limitation requires that the four signals be construed in the disjunctive, and instead construed them in the conjunctive." Req. for Reh'g 6. We agree with Requester 3 that we construed the "logic element" limitation in the conjunctive in Decision 2. *See, e.g.,* Decision 2, pp. 13–14 and 18–19. Although presenting an argument that the "logic element" limitation must be construed in the disjunctive in its comments (Req. for Reh'g 6 n.3), Requester 3 did not present a separate argument that the "logic element" limitation lacks written description support if construed in conjunctive. *See, e.g.,* R3 Comments 8–9. As such, Requester 3 has not pointed out an argument we overlooked or misapprehended as set forth in § 41.79(b)(1).

Additionally, similar to the above discussion, we disagree that the newly proposed ground under 35 U.S.C. § 112, first paragraph[3] (Req. for Reh'g 6–8) is permitted under § 41.79(b)(3) at this juncture. To reiterate, Rule 41.79(b)(3) permits parties to an appeal to present a new argument when responding to a new ground of rejection in a decision. Yet, no new ground of rejection, including one based on failing to satisfy the written description requirement, was presented in Decision 2. Thus, presenting a new argument related to lack of written description in Requester3's request for rehearing is improper. The appropriate time for Requester 3 to have presented the new ground based on 35 U.S.C. § 112, first paragraph contending claims in the '912 patent lack written description support

[3] Because of the '912 patent's filing date, we refer to pre-AIA sections of Title 35 of the United States Code.

Petitioners
Ex. 1016, p. 163

was when Requester 3 submitted comments responding to Patent Owner's amendments to the claims in Patent Owner's response requesting to reopen prosecution. *See* 37 C.F.R. § 41.77(c).

The Prior Art Purportedly Supports the Obviousness Rejections as "Logic Element" in Claim 1 is Construed

Lastly, Requester 3 argues "the Board's Decision evidences additional error" to the extent we "find[] the '912 Patent's written description supports the Board's claim construction." Req. for Reh'g 8. Requester 3 implies we have misapplied the law by "constru[ing] the claims [of the '912 patent] to require the prior art teach more than the patent itself." Req. for Reh'g 8 (citing *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1349, 1351 (Fed. Cir. 2010) (en banc)). We are not convinced.

As indicated above, we did not address whether the "logic element" limitation has written description support because no such issue was raised by Requester 3 (or any Requester for that matter). Thus, we disagree that we have overlooked or misapprehend any points made by Requester 3 or misapplied the law in this regard as asserted. *See* Req. for Reh'g 8–9. Moreover, given that the '912 patent and the cited prior art are not coextensive, we disagree with Requester 3's contention that we must determine "the cited prior art sufficiently supports the Examiner's prior findings that the 'logic element' limitation is obvious" "if the '912 Patent specification sufficiently supports the Board's claim construction." Req. for Reh'g 9.

In summary, we have considered the arguments raised by Requester 3 in the Request for Rehearing, but the arguments are not persuasive to find that Decision 2 was in error. We have granted the Request for Rehearing to the extent that we

Petitioners
Ex. 1016, p. 164

have reconsidered Decision 2, but we deny the request for hearing with respect to making any changes to the new grounds of rejection.

REHEARING DENIED

Petitioners
Ex. 1016, p. 165

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Petitioners
Ex. 1016, p. 166