US007619912C1

(12) **INTER PARTES REEXAMINATION CERTIFICATE** (1643rd)

United States Patent

Bhakta et al.

(10) **Number: US 7,619,912 C1**

(45) **Certificate Issued: Feb. 8, 2021**

(54) **MEMORY MODULE DECODER**

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Reexamination Request:
No. 95/001,339, Jun. 8, 2010
No. 95/000,578, Oct. 20, 2010
No. 95/000,579, Oct. 21, 2010

Reexamination Certificate for:

Patent No.:	**7,619,912**
Issued:	**Nov. 17, 2009**
Appl. No.:	**11/862,931**
Filed:	**Sep. 27, 2007**

Certificate of Correction issued Aug. 10, 2010

Related U.S. Application Data

(63) Continuation of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, and a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436.

(60) Provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004.

(51) **Int. Cl.**

G11C 15/02	(2006.01)
G11C 7/10	(2006.01)
H05K 1/14	(2006.01)
G11C 8/12	(2006.01)
G06F 12/02	(2006.01)
G11C 5/04	(2006.01)
G11C 5/06	(2006.01)
H05K 1/18	(2006.01)

(52) **U.S. Cl.**

CPC ***G11C 8/12*** (2013.01); ***G06F 12/0207*** (2013.01); ***G06F 12/0215*** (2013.01); ***G11C 5/04*** (2013.01); ***G11C 5/066*** (2013.01); ***G11C 7/1048*** (2013.01); ***H05K 1/181*** (2013.01); *G11C 2207/105* (2013.01); *H05K 2201/10159* (2013.01); *H05K 2203/1572* (2013.01); *Y02P 70/50* (2015.11)

(58) **Field of Classification Search**

None

See application file for complete search history.

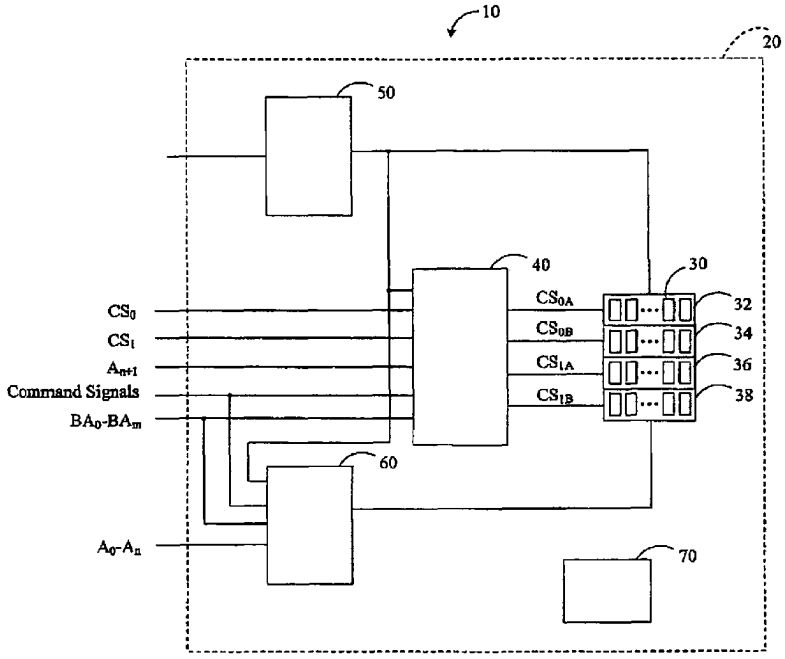
(56) **References Cited**

To view the complete listing of prior art documents cited during the proceedings for Reexamination Control Numbers 95/001,339, 95/000,578 and 95/000,579, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

Primary Examiner — B. James Peikari

(57) **ABSTRACT**

A memory module connectable to a computer system includes a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.



INTER PARTES REEXAMINATION CERTIFICATE

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **2**, **5**, **7**, **9**, **21**, **23**, **25**, **26**, **30**, **33**, **42**, **44** and **51** are cancelled.

Claims **1**, **15**, **16**, **28**, **39** and **43** are determined to be patentable as amended.

Claims **3**, **4**, **6**, **8**, **10-14**, **17-20**, **22**, **24**, **27**, **29**, **31**, **32**, **34-38**, **40**, **41** and **45-50**, dependent on an amended claim, are determined to be patentable.

New claims **52-91** are added and determined to be patentable.

1. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.

15. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR memory device of the selected one or two ranks of the first number of ranks, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are

separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals and (iii) the at least one chip-select signal of the set of input signals and (iv) the PLL clock signal.

16. [The memory module of claim **15**] *A memory module connectable to a computer system, the memory module comprising:*

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the command signal is transmitted to only one DDR memory device at a time.

28. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR DRAM memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR DRAM device of the selected at least one rank, wherein the row/column address signal received by the logic element comprises a row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the row address signal, (ii) the bank address signals, and (iii) the chip-select signal of the set of input control signals and (iv) the PLL clock signal.

39. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives *at least one row address signal,* the bank address signals, *at least one chip-select signal,* and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one

rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from among the plurality of input signals, and (ii) buffers, in response to the PLL clock signal, the bank address signals and a plurality of the row address signals, and (iii) transmits the buffered bank address signals and the buffered row address signals to the at least one DDR memory device of the selected at least one rank, and wherein the plurality of the row address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the plurality of input signals and (iv) the PLL clock signal.

43. The memory module of claim **[42]** *39*, wherein the logic element receives the second number of chip-select signals.

52. The memory module of claim 1, wherein the plurality of DDR memory devices has at least one attribute selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different from an actual value of the at least one attribute of the plurality of DDR memory devices.

53. The memory module of claim 52, wherein the at least one attribute comprises the number of ranks of DDR memory devices and the memory density per rank.

54. The memory module of claim 53, wherein the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

55. The memory module of claim 1, wherein each DDR memory device of the plurality of DDR memory devices is a DDR dynamic random-access memory (DRAM) chip package with a bit width, and each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages having a total bit width equal to the summed bit widths of the DDR DRAM chip packages of the rank, wherein the memory module further comprises a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has.

56. The memory module of claim 1, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

57. The memory module of claim 1, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the first memory density greater than the second memory density.

58. The memory module of claim 1, wherein the register comprises a plurality of register devices.

59. The memory module of claim 1, wherein the chip-select signals generated by the logic element are a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

60. The memory module of claim 59, wherein the at least one row address signal and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation.

61. The memory module of claim 60, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

62. The memory module of claim 60, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of plurality of DDR memory devices.

63. The memory module of claim 1, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

64. The memory module of claim 15, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per

DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

65. The memory module of claim 64, wherein the one or more attributes comprise the number or ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

66. The memory module of claim 15, wherein the command signal is transmitted to only one DDR memory device at a time.

67. The memory module of claim 66, wherein the command signal comprises a read command signal.

68. The memory module of claim 15, wherein the logic element receives the command signal from the computer system and the register receives the command signal from the computer system.

69. The memory module of claim 28, wherein the plurality of DDR DRAM devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR DRAM device, a number of column address bits per DDR DRAM device, a number of bank address bits per DDR DRAM device, a number of DDR DRAM devices, a data width per DDR DRAM device, a memory density per DDR DRAM device, a number of ranks of DDR DRAM devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR DRAM devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR DRAM devices.

70. The memory module of claim 69, wherein the one or more attributes comprise the number of ranks of DDR DRAM devices and the memory density per rank and the data characterizes the plurality of DDR DRAM devices as having fewer ranks of DDR DRAM devices than the plurality of DDR DRAM devices actually has, and as having a greater memory density per rank than the plurality of DDR DRAM devices actually has.

71. The memory module of claim 28, wherein the memory module comprises means for characterizing the plurality of DDR DRAM devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

72. The memory module of claim 28, wherein the register receives the input command signal of the set of input control signals.

73. The memory module of claim 39, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from one or more attributes of the plurality of DDR memory devices.

74. The memory module of claim 73, wherein the one or more attributes comprises the number of ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

75. The memory module of claim 39, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

76. The memory module of claim 43, wherein both the register and the logic element receive at least one command signal of the plurality of input signals.

77. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller thank the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buff-

ered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

78. The memory module of claim 77, wherein the row address bit and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation.

79. The memory module of claim 78, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of plurality of DDR memory devices.

80. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board:

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks:

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device and the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks,

wherein the bank address signals of the set of input control signals are received by the logic element,

wherein a plurality of row/column address signals and the bank address signals are received from the computer system and buffered by the register, the register transmitting the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the generation of the first number of chip-select signals of the output control signals by the logic element is based on the logic element responsive at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals received by the logic element and (iv) the clock signals received from the phase-lock loop device.

81. The memory module of claim 80, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

82. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the

computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element,

wherein the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input control signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

83. The memory module of claim 82, wherein the memory module is operable to perform successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices.

84. The memory module of claim 82, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

85. The memory module of claim 82, wherein the bank address signals include bank address signals received during an activate command operation and bank address signals received during a read or write command operation subsequent to the activate command operation, and the rank-selecting signals are used for the read or write command operation.

86. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR memory device of the selected one or two ranks of the first number of ranks, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input signals.

87. The memory module of claim 86, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

88. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR DRAM devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR DRAM device of the selected at least one rank, wherein the row/column address signal received by the logic element comprises a row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the row address signal received by the logic element, and

wherein the logic element responds to at least (i) the row address signal, (ii) the bank address signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

89. The memory module of claim 88, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR DRAM device boundaries.

90. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives at least one row address signal, the bank address signals, the second number of chip-select signals, and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein, in responsive to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from among the plurality of input signals, and (ii) buffers, in response to the PLL clock signal, the bank address signals and a plurality of the row address signals, and (iii) transmits the buffered bank address signals and the buffered plurality of row address signals to the at least one DDR memory device of the selected at least one rank, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of the row address signals received by the register are separate from the at least one row address signal received by the logic element,

wherein the logic element responds to at least (i) the at least one row signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals.

91. The memory module of claim 90, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

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